Devices selection for S to X bands low phase noise oscillator design

G. Cibiel, O. Llopis, L. Escotte, G. Haquet*

LAAS-CNRS, 7 Avenue du Colonel Roche - 31077 Toulouse - France
*__THALES-MICROELECTRONICS__, ZI de Bellevue – 35221 Châteaubourg Cedex – France

Contact: gcibiel@laas.fr, llopis@laas.fr

***Abstract* — In this paper, a comparative study of various transistors dedicated to low phase noise S to X bands oscillator design is proposed. Then, a transistor selection factor for low phase noise oscillator design is introduced.**

INTRODUCTION

Phase noise of microwave free running sources has always been an important problem in various applications. This noise generates an increased bit error rate in a telecommunication link and degrades the sensitivity of a radar (particularly in the case of Doppler or FM-CW radar).

Reducing this noise contribution is a difficult challenge for microwave engineers and circuit designers. It cannot be done without a good knowledge of the noise mechanisms involved in the circuit. The main contributor to this noise is the microwave transistor and selecting the appropriate device is one of the key of success in low phase noise oscillator design.

In this paper the phase noise properties of some amplifiers dedicated to low phase noise S to X bands oscillator design are investigated. Firstly, the interest of the corresponding open loop configuration and the phase noise measurement bench, able to characterize ultra low phase noise devices, are presented. The mechanisms of transistor phase noise generation are reported. Then, devices and test configurations are described. Finally, the devices measured performance is discussed and a transistors selection factor for low phase noise oscillator design is established.

I. OPEN LOOP PHASE NOISE APPROACH

An oscillator is an amplifier embedded in a feedback loop. Inside the loop bandwidth, a simple perturbation equation of the oscillator loop [1], with the assumption that the total phase is constant on one loop turn, leads to the following relation :

$$S_{\Delta f} = \left(\frac{f_0}{2Q_L}\right)^2 S_{\Delta\phi} \qquad (1)$$

$S_{\Delta f}$ being the oscillator frequency fluctuations spectral density, $S_{\Delta\phi}$ the amplifier phase noise spectral density, f_0 the oscillation frequency and Q_L the resonator loaded quality factor. This equation shows different important fundamental elements of oscillation, such as the inverse proportionality of the oscillation frequency stability versus the resonator quality factor. But one of the most important point is probably in the equivalence it involves between the oscillator frequency fluctuations $S_{\Delta f}$ and the amplifier phase fluctuations $S_{\Delta\phi}$. It is thus interesting to study $S_{\Delta\phi}$ instead of $S_{\Delta f}$, because a device in an open loop configuration is easier to model or to characterize. Simulation on an amplifier features fast convergence, because it is a driven circuit (contrarily to an oscillator which is an autonomous circuit). Phase noise measurement on an amplifier allows a better control of the experimental parameters, such as the microwave input power. Moreover, there is no loop condition, and the loop phase is well known to be one of the most difficult parameter to control in oscillators experiments.

We have thus chosen to perform our experiments on transistors in an open loop configuration rather than on oscillators. To this purpose, a residual phase noise measurement bench has been used (Fig. 1). This set-up allows residual phase noise characterization in the microwave range (1 to 18 GHz) of amplifiers, mixers, frequency dividers, and multipliers. Some special techniques have been implemented to characterize very low noise devices such as Si BJT and SiGe HBT amplifiers [2] and we are able to demonstrate a noise floor of –180 dB_{rad}/Hz (–172 dB_{rad}/Hz) at 10 kHz offset from a 3.5 GHz (10 GHz) carrier.

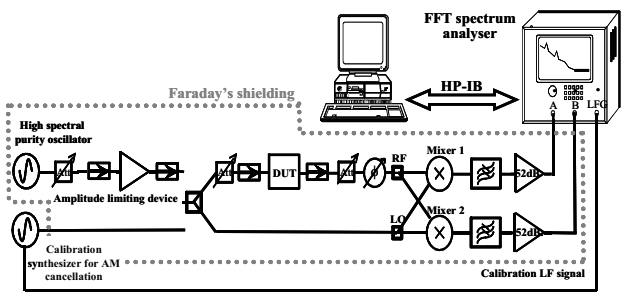

Figure 1 : Residual phase noise measurement set-up (phase detection : 1 to 18 GHz ; observation LF band : 1 Hz to 100 kHz).

III. Transistor Phase Noise Generation

Two different mechanisms may be at the origin of amplifier phase noise. The first one involves the conversion to high frequencies of the transistor LF noise. The second one is due to the direct superposition of the transistor HF noise.

At low offset frequencies, a 10 dB/dec slope is clearly the result of a 1/f LF noise conversion (this part of the spectrum corresponds to the 30 dB/dec slope in an oscillator). This noise makes fluctuating the transistor nonlinear elements, and this causes a phase fluctuation of the signal. This leads to the following expression :

$$S_{\phi\,conv} = k_{v1}^{\,2}\ S_{v1} + ... + k_{i1}^{\,2}\ S_{i1} + ... \qquad (2)$$

k_{vn} (k_{in}) being the conversion factor of the voltage (current) noise source vn (in), described by its voltage (current) noise spectral density S_{vn} (S_{in}).

At higher offset frequencies, two different noise floor are competing for bipolar transistor. The first one is the noise floor due to the conversion of the LF noise. The second one is the noise floor due to the device HF noise : the HF noise of the amplifier is added to the carrier, and this contribution may be described using the amplifier noise figure F_{DUT}. The additive noise power level is expressed by $F_{DUT}\ k\ T_0$, with k and T_0 being respectively the Boltzmann coefficient and the reference temperature (290 K). This leads to the following expression for the additive phase noise :

$$S_{\phi\,add} = \frac{F\ k\ T_0}{P_{IN}} \qquad (3)$$

This noise contribution has been found to be predominant in some bipolar transistor devices above approximatively 10 kHz offset frequency [3]. A complete theory of this mechanism, including a non-linear noise figure approach, is described in reference [3].

III. Devices And Test Configurations

Eight different devices have been characterized with this measurement bench : seven bipolar transistors (BT) four Si BJT, two SiGe HBT, one GaAs HBT ; and two field effect transistors (FET) one PHEMT and one MESFET. These transistors are all commercially avaible devices, in surface mount plastic package.

Because the residual phase noise is strongly dependant on the test conditions, a set of eight measurements has been performed on each transistor by varying different parameters : the carrier frequency, two values 3.5 GHz* and 10 GHz ; the bias network, low impedance bias* (LI) and high impedance bias (HI) ; the DC bias ; the input microwave power, linear regime (–10 dBm and –1 dBm respectively at 3.5 GHz and 10 GHz carrier frequencies) and non-linear regime, 1 dB compression. This approach generates a large amount of information which is the base of our device selection. In each case, the transistor is loaded onto 50 Ω on the input and the output at microwave frequencies. The Fig. 2–4 represent a part of this exhaustive open loop phase noise characterization. From these measurements, different arguments can be pointed out for devices selection.

IV. Discussion

Firstly the effect of the low frequency noise (LF) load (bias network impedance) has been found to be very important for all the BT devices, with the exception of the transistor with the highest emitter dimension (Si BJT4) which features almost the same performance when it is biased with the usual high impedance bridge than with the low impedance bias network. The influence of such a noise LF filtering network can be explained as follows [4]. The main excess noise source in a bipolar transistor is the base-emitter junction current noise ; when the transistor is biased with a high impedance network, "high" meaning higher than the transistor LF input impedance, this noise current flows into the transistor input impedance and creates a fluctuation of the control voltage V_{BE} which is directly converted into phase modulation ; when the transistor is voltage biased at LF, this noise current is short circuited and V_{BE} is stabilized. The simplest way to realize such a bias network is to use a high capacitance value [4] on the base-emitter bias access (a 1 000 µF value capacitance has been used in the measurement data of Fig. 2 to 4). Another solution is to use a real low impedance bias network [5]. The main drawbacks associated with these techniques are : both circuits may change the oscillation stability ; in the second case, the oscillator nonlinear steady state is also modified ; both circuits are difficult to integrate in a MMIC approach. However, the improvement on phase noise is such than we can take benefit of the real potential of silicon bipolar devices only if such a bias network is implemented. An example is shown in Fig. 2 for the GaAs HBT device. An improvement of 20 dB is observed at 1 kHz offset frequency. The spectrum is plotted only up to 10 kHz in the high impedance configuration, because the intrinsic capacitance of the bias Tee already filters the current at higher frequencies. Further devices comparison have been made with BT always biased with such a network. In these conditions, FET devices are much noisier and should be avoided (Fig. 4). Moreover the phase noise performance of the GaAs BT is very close to the performance of the silicon BT devices, which is quite surprising (LF noise in Si and AsGa materials is generally much different). But the

* bipolar transistors only

phase noise in an amplifier is not entirely related to the device LF noise properties.

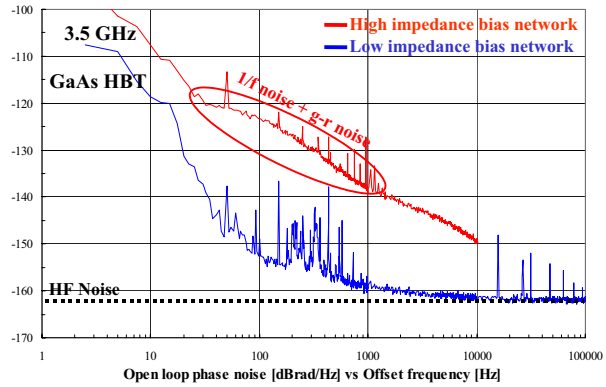

Figure 2 : Measured phase noise of the GaAs HBT device loaded onto 50 Ω versus the offset frequency at P_{IN}(3.5 GHz)= -10 dBm with different bias network configuration. Dotted line represents the calculated HF noise.

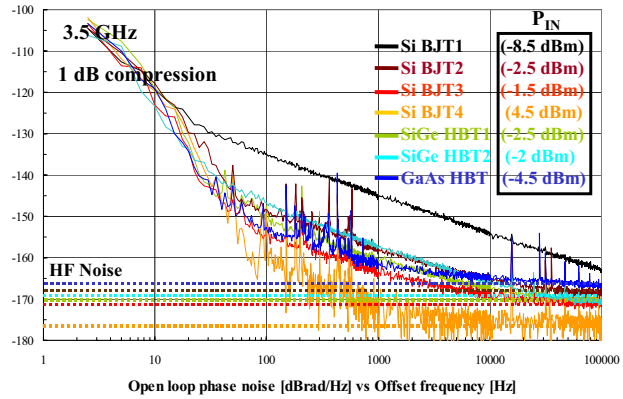

Figure 3 : Measured phase noise of each BT loaded onto 50 Ω versus the offset frequency at –1 dB compression and 3.5 GHz with a low impedance bias network configuration. Dotted line represent the calculated HF noise.

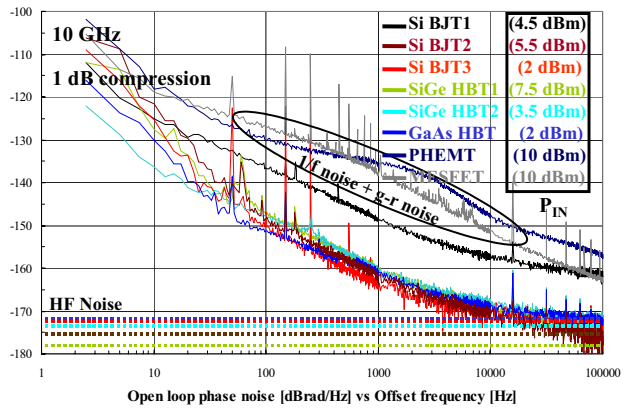

Figure 4 : Measured phase noise of each DUT loaded onto 50 Ω versus the offset frequency at –1 dB compression and 10 GHz with a low (high) impedance bias network configuration for the BT (FET). Dotted line represent the calculated HF noise.

The Eq. 3 clearly shows that the additive phase noise is inversely proportional to the carrier power P_{IN}. This noise contribution has been found to be predominant in some bipolar transistor devices above approximately 10 kHz offset frequency [3]. In this study, the calculated HF noise (using relation 3) of each BT has been plotted (dotted line) and compared with the measured residual phase noise on Fig. 2–4 ; a good agreement is found at each time. The [10 kHz–1 MHz] offset frequency range is the most important frequency range for many microwave oscillators applications and finally an improvement of the transistor (or oscillator) phase noise in this frequency range will result from an optimisation of its additive phase noise.

However the LF converted noise may feature a maximum value versus the carrier frequency [3] and the competition between these two noise contributions must systematically be checked.

V. Transistors Selection Factor

The phase noise performance onto 50 Ω has to be considered together with the gain performance (Tab. 1). It is indeed essential that the amplifier used in the oscillator should be able to compensate for the losses of the moderately coupled resonator.

In a oscillator, the phase noise is inversely proportional to the resonator loaded Q factor (Eq. 1) [1]. However this assumption is valid only if the other cirucit parameters are hold constant while varying the Q factor. Many circuits make use of a transistor matched for the highest small signal gain at a given frequency, associated with a resonator featuring approximately 2 dB less losses than the available small signal gain. This approach leads to very poor phase noise results, both for FET [6] or bipolar transistors oscillators [7]. Indeed previous work has shown that improving the small signal gain using an appropriate matching network creates a resonant behaviour which enhances the phase fluctuations. In fact, the higher gain does not coincide at all, unfortunately, with the smaller $S_{\Delta\phi}$ [6].

In order to take into account this problem, an expression of the phase noise degradation coefficient γ versus the transistor 50 Ω small signal gain G has been calculated (4). This expression is obtained considering that the losses in the resonator L are 1 dB lower than the transistor small signal gain (L = G - 1) or in other words, that the oscillator performs at 1 dB compression.

$$\gamma = \left| 20 \, \mathrm{Log} \left(\frac{10^{\frac{G-1}{20}}}{10^{\frac{G-1}{20}} - 1} \right) \right| \qquad (4)$$

This equation is obtained considering the expression of the loaded quality factor Q_L versus the unloaded quality factor Q_0 and the coupling coefficients (β_1 and β_2 in a transmission case) [8] :

$$Q_L = \frac{Q_0}{1 + \beta_1 + \beta_2} \qquad (5)$$

β_1 and β_2 are defined by (6) expression under the assumption of a symmetric coupling.

$$\beta_1 = \beta_2 = \frac{1}{2\left(10^{\frac{L}{20}} - 1\right)} \qquad (6)$$

The phase noise degradation versus the transistor gain onto 50 Ω is represented in Fig. 5. The 0 dB degradation corresponds to the (theoretically impossible) case of a loaded quality factor Q_L equal to the unloaded quality factor Q_0. Above $Q_L = Q_0/2$ (G= 7 dB), the phase noise improvement is weak, and only obtained at a cost of a strong improvement of the transistor gain.

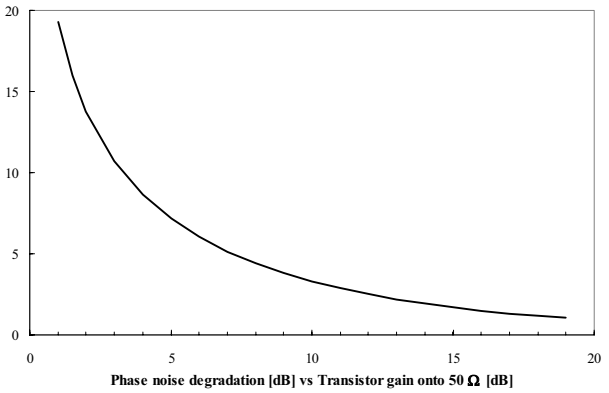

Figure 5 : Visualization of the phase noise degradation due to the cavity coupling in a parallel feedback oscillator through the transistor gain onto 50 Ω. The 0 dB degradation corresponds to the (theoretically impossible) case of a loaded quality factor Q_L equal to the unloaded quality factor Q_0.

From this observation (Eq. 4) and considering the transistor phase noise data, we propose a new figure of merit χ which takes into account both the transistor gain and phase noise performance :

$$\chi = \gamma + S_{\Delta\phi} \qquad (5)$$

The transistors 50 Ω small signal gain, the phase noise data at 100 kHz offset and the figure of merit χ are reported in Table 1 and 2.

3.5 GHz	Gain onto 50 Ω	Phase noise at 100 kHz offset	Selection Factor χ	Selection
Si BT 1	14	-163 dBrad/Hz	-160.8 dBrad/Hz	7
Si BT 2	14	-168 dBrad/Hz	-165.8 dBrad/Hz	5
Si BT 3	12	-171 dBrad/Hz	-168.1 dBrad/Hz	2
Si BT 4	5	**-176 dBrad/Hz**	-167.3 dBrad/Hz	3
SiGe HBT 1	15.5	-170 dBrad/Hz	-168.2 dBrad/Hz	1
SiGe HBT 2	15	-169 dBrad/Hz	-167.1 dBrad/Hz	4
AsGa HBT	**16**	-166 dBrad/Hz	-164.3 dBrad/Hz	6

Table 1 : Gain, phase noise at 100 kHz offset frequency, selection factor and selection level of each device loaded onto 50 Ω at 3.5 GHz.

It can be noticed that the transistors featuring either the best gain performance or the best phase noise performance are not necessarily the more appropriates for oscillator design, and we believe a good trade-off can be found using the χ factor.

10 GHz	Gain onto 50 Ω	Phase noise at 100 kHz offset	Selection Factor χ	Selection
Si BT 1	5	-162 dBrad/Hz	-153.3 dBrad/Hz	7
Si BT 2	2	-176 dBrad/Hz	-156.7 dBrad/Hz	5
Si BT 3	4	-173.5 dBrad/Hz	-162.8 dBrad/Hz	4
SiGe HBT 1	3	**-179 dBrad/Hz***	-165.3 dBrad/Hz	2
SiGe HBT 2	4	-175 dBrad/Hz	-164.3 dBrad/Hz	3
HBT AsGa	**6.5**	-173 dBrad/Hz	-166.4 dBrad/Hz	1
HEMT	4	-157 dBrad/Hz	-146.3 dBrad/Hz	8
MESFET	4.5	-164 dBrad/Hz	-154.4 dBrad/Hz	6

Table 2 : Gain, phase noise at 100 kHz offset frequency, selection factor and selection level of each device loaded onto 50 Ω at 10 GHz. (*estimated result)

CONCLUSION

The open loop phase noise approach and the corresponding measurement bench has allowed to select devices featuring exceptional phase noise performances at S and X bands. These performances are reached not only by selecting the devices, but also the devices operating condition : bias network (low impedance), microwave noise, carrier frequency (conversion process) and gain / phase noise trade-off. Then, from the transistors selection factor χ introduced in this paper, a very low phase noise oscillator could be designed including one of the best selected device.

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