Sub-Micron CMOS Characterisation for Single Chip Wireless Applications

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ABSTRACT

This paper describes a multifunctional, electronically reconfigurable, small/large signal load pull measurement system and its integrated use with BSIM 3v3 for modelling of sub-micron CMOS transistors and sub-circuits. This turnkey measurement system can be electronically configured from a battery of instruments in order to characterise minimum noise, optimum power, intermodulation, dc and S-parameters, together with harmonic response and dynamic load line information under both source and load pull conditions. The instrumentation provides validation data against the BSIM physical model simulator. Hence, for the first time measurement of all of the significant devices parameters can be made for the device operated under all possible primary modes for model validation so that optimal circuit design can be carried out in a holistic fashion.

INTRODUCTION

The cost of a single chip transceiver e.g. for Bluetooth is expected to be around $5-10. With such constraints, sub-micron CMOS is chosen because of its low cost and potential performance at the operating frequency of 2.4 GHz. Recent advances in CMOS processing have provided devices with f_T values in excess of 30 GHz. To model these devices at high frequencies industry have adopted the BSIM 3v3 physical model. Therefore, the utility of this model when used in conjunction with the multifunctional measurement system will be considered in this paper.

PARAMETER EXTRACTION AND MODELLING

The model developed and verified in this paper is shown in the diagram of Fig. 1, here two additional resistors have been added to the intrinsic BSIM model. The gate resistance is added to account for the distributed gate fingers and channel resistance with the substrate resistance added to model the signal coupling through the lossy substrate. The bias dependence of these components[1] has been neglected in order to maintain the simplicity of the extrinsic sub-circuit. The components were extracted in accordance to the procedure reported in [2] at the operating bias point.

MEASUREMENT SYSTEM

The system components are configured according to the diagram of Fig. 2. Electronically controlled coaxial switches allow different instruments access to the on-wafer probe station. This allows different measurements to be completed. Passive source and load tuners allow any given impedance to be presented to the device under test. The addition of a Microwave Transition Analyser (MTA) provides time domain analysis capabilities to the system and is used for all power measurements and load pull.

SYSTEM CALIBRATION

The MTA is a general purpose instrument and is variously used as a Network Analyser, Vector Power meter and Spectrum Analyser within the system. A single calibration is needed to the DUT

plane, which allows all measurements to be completed to the on-wafer probe tips. Firstly a twelve term calibration [3] is performed to the DUT plane (plane B), as in the case of a network analyser. However the non-reciprocal nature of the directional couplers imposes the requirement of a further coaxial calibration to plane C in order to separate the reflection tracking error coefficients[3]. Therefore a one-port calibration is performed whereby open, short and load standards are placed at port C and the first stage small signal calibration used to provide corrected S-Parameter measurements of the output network between planes B and C. Transmission measurements are then performed between the MTA input (plane A) and plane C. Since the output S-Parameter block is known the input error coefficients($e_{10}e_{01}$) can be separated. A similar procedure is repeated for the input to provide a full two port calibration. Both the on-wafer and coaxial calibrations are performed using an interchangeable SOLT scheme.

MODEL VERIFICATION

To illustrate some of the capabilities some sample measurements have been completed to both illustrate the accuracy of the BSIM model at high frequencies and to provide an independent benchmark for the measurement system. A 0.25um/300um NMOS device was used in this process. The diagram of Fig. 3 illustrates good agreement for S-Parameters up to 10 GHz. In the harmonic power measurement of Fig.4 the input of the device was matched for maximum output power with the output held at 50Ω. The results of Fig. 5 illustrate the comparison between measured and simulated noise figures. Using the source tuner it is possible to change the source impedance to obtain minimum noise figure. Advanced load pull and power measurements can also be made using the MTA. The systems ability to simultaneously measure reflection coefficient and power during load pull is useful for CMOS transistors because of their inherent instability. A load pull for maximum gain or power could be misleading as the resulting operating point could be in an unstable region. Therefore the additional reflection measurements help avoid any potential oscillation problems and thus provide maximum stable gain and power points. When suitable terminations for the transistor have been chosen, power sweeps, time domain waveforms and dynamic load lines can be obtained for different operating conditions. Using the MTA, the amplitude and phase of the power waves can be referred to the DUT plane and converted to voltages and currents. As can be seen good agreement is achieved for drain voltage (Fig. 6) but there is some discrepancy for the drain current (Fig. 7). This is due to the BSIM model not compensating for the self-heating of the device during measurement under high power conditions [4]. From the voltage and current waves dynamic load lines can be produced. Fig. 8 illustrates load line variation with increasing power level for a 50Ω load and for an inductive load, matched to yield greater output power.

CONCLUSIONS

This paper details the development of an integrated on-wafer measurement system to be used in the modelling of transistors, small/large signal verification of models and the testing of circuits. The accuracy of the adapted BSIM 3v3 model used here is verified through all measurements and therefore its suitability in modelling high frequency MOS transistors has been confirmed. The resultant system provides a universal test bench for on-wafer measurement for devices and circuits.

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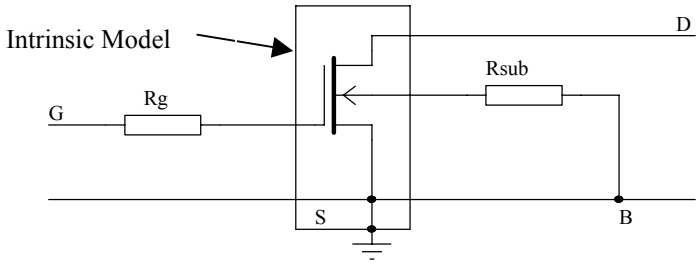

Fig. 1. Intrinsic BSIM 3v3 model with extrinsic resistors

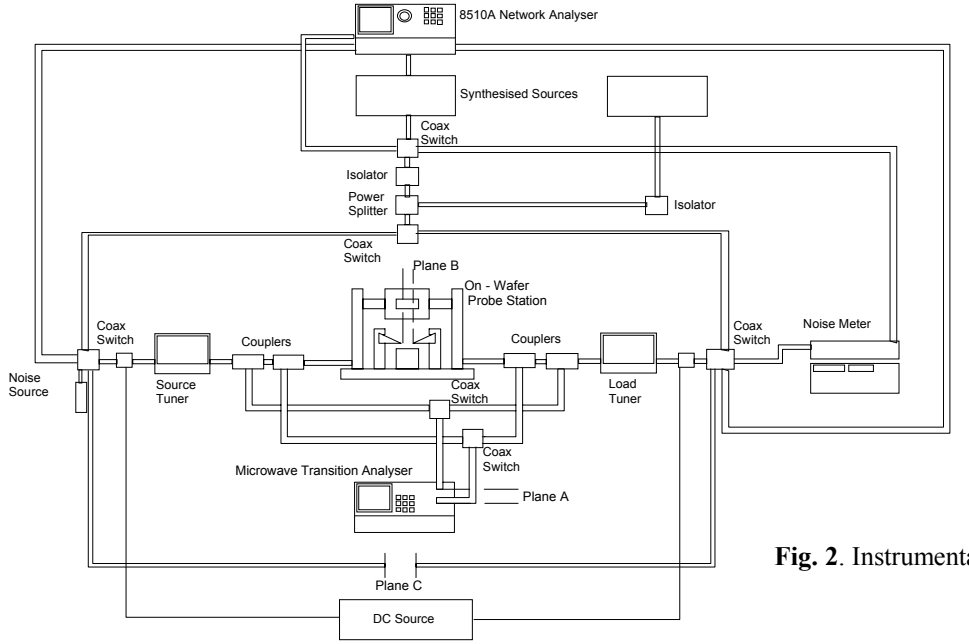

Fig. 2. Instrumentation Configuration

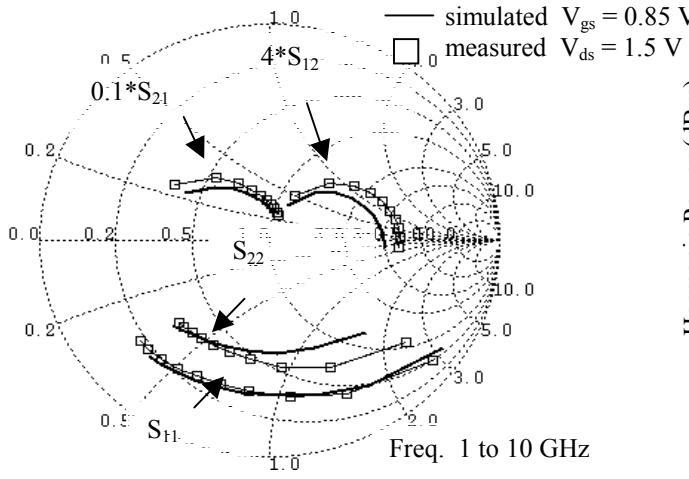

Fig. 3. Measured and simulated S-Parameters

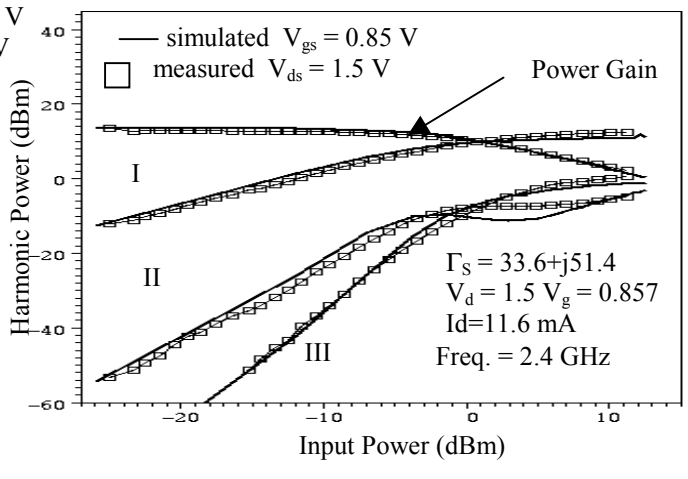

Fig. 4. Harmonic Power and Power Gain

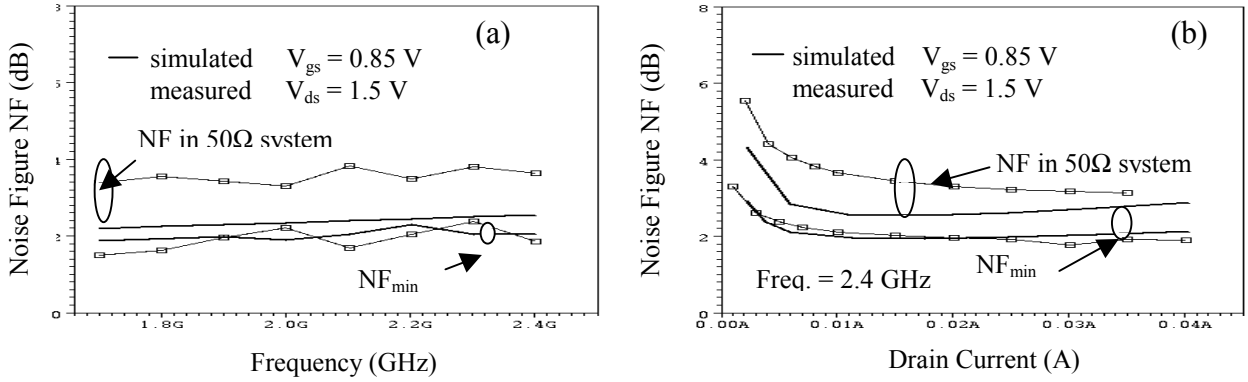

Fig. 5. (a) 50Ω and minimum N.F. over Frequency (b) 50Ω and minimum N.F. over bias current

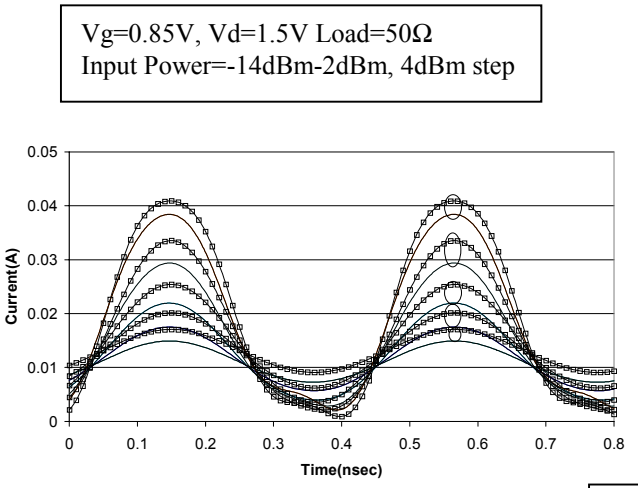

Fig. 6. Drain Voltage

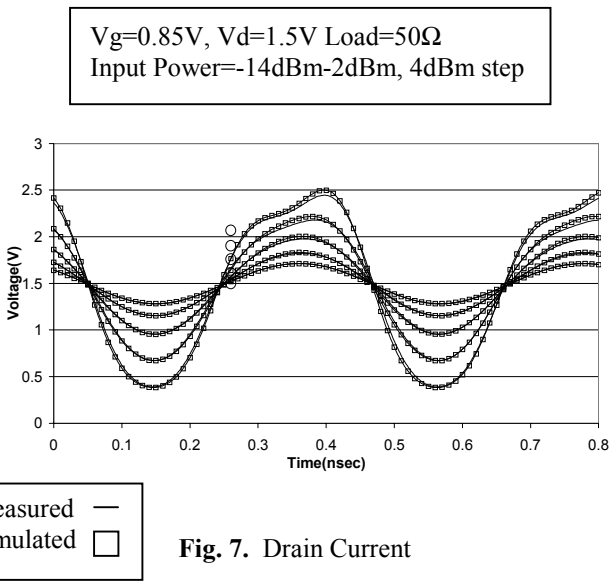

Fig. 7. Drain Current

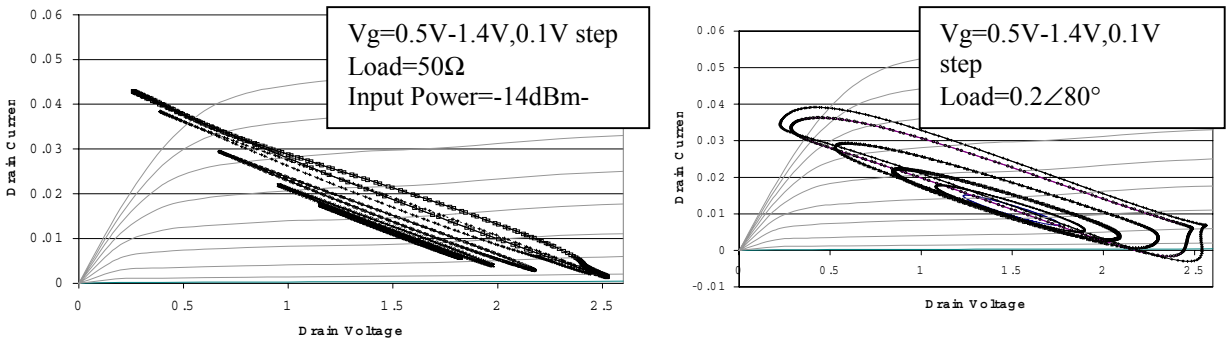

Fig. 8. Dynamic Load Lines