Unveiling the carrier transport mechanism in epitaxial graphene for forming wafer-scale, single-domain graphene

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Graphene epitaxy on the Si face of a SiC wafer offers monolayer graphene with unique crystal orientation at the wafer-scale. However, due to carrier scattering near vicinal steps and excess bilayer stripes, the size of electrically uniform domains is limited to the width of the terraces extending up to a few microns. Nevertheless, the origin of carrier scattering at the SiC vicinal steps has not been clarified so far. A layer-resolved graphene transfer (LRGT) technique enables exfoliation of the epitaxial graphene formed on SiC wafers and transfer to flat Si wafers, which prepares crystallographically single-crystalline monolayer graphene. Because the LRGT flattens the deformed graphene at the terrace edges and permits an access to the graphene formed at the side wall of vicinal steps, components that affect the mobility of graphene formed near the vicinal steps of SiC could be individually investigated. Here, we reveal that the graphene formed at the side walls of step edges is pristine, and scattering near the steps is mainly attributed by the deformation of graphene at step edges of vicinalized SiC while partially from stripes of bilayer graphene. This study suggests that the two-step LRGT can prepare electrically single-domain graphene at the wafer-scale by removing the major possible sources of electrical degradation.

epitaxial graphene | single domain | single crystal | carrier transport

Since the first discovery of graphene (1), its outstanding properties have drawn a great deal of attention (2–11). Among the methods to synthesize large-scale graphene (12–14), the growth of epitaxial graphene on a SiC wafer has been investigated as one of the most promising methods. Specifically, graphene growth on the Si face of a SiC (0001) wafer offers unique crystallographic orientation and monolayer controllability at the wafer-scale via a self-limiting sublimation of Si (15–18). However, graphene formed near SiC vicinal steps exhibits high resistance; thus, the region of graphene demonstrating high uniform carrier mobility is limited to the size of the terrace on a SiC substrate (19–23). The resistivity jump at the 10-nm-high single step on a SiC substrate was reported to be 21 kΩ·μm (21), whereas the intergrain resistivity from chemical vapor deposition (CVD)-grown polycrystalline graphene is measured to be 5 kΩ/sq (24). Thus, the use of this oriented graphene on SiC has been less favored over the use of CVD-grown polycrystalline graphene because the practical domain size of oriented graphene is much smaller than that of CVD-grown graphene (typically ranging from tens to hundreds of microns) (25). To overcome the limitation of graphene grown on SiC substrates, it is necessary to elucidate the cause of carrier scattering near vicinal steps and progress toward removing the factors causing this phenomena. However, the cause of enhanced carrier scattering in graphene near the SiC vicinal steps has not been fully understood yet. This is mainly due to the difficulty of resolving the complicated form of graphene near the step edges—(*i*) monolayer graphene formed at the step edges is subject to deformation, (*ii*) bilayer stripes of graphene are known to form near the edges, and (*iii*) the side-wall surface is not a hexagonal (0001) plane, which may not allow the formation of high-quality graphene at the side wall (15, 16, 18).

Here, we revealed the role of each parameter affecting carrier transport in epitaxial graphene by performing a layer-resolved graphene transfer (LRGT) process. We also confirmed that the graphene fabricated by the LRGT process is electrically single-domain graphene, whereas its ability to produce crystallographically single-crystalline graphene has been proven in the previous work (26). A one-step LRGT causes flattening of the epitaxial graphene on SiC step edges, which contains deformed monolayer, bilayer stripes, and graphene formed at the side wall of steps (26). We discovered that resistance of flattened graphene across the single bilayer stripe is ∼2.9 kΩ·μm where the measured area contains a bilayer stripe and side-wall graphene. Our simulation showed that such a resistance jump is solely due to the mobility drop at the bilayer, suggesting that the side-wall graphene is pristine. We additionally confirmed this by fabricating the field effect transistors (FETs) on the stripe-removed region and terrace region of the transferred graphene, both of which exhibit comparable FET mobility. Thus, we conclude that the graphene prepared by the two-step LRGT, where the all-bilayer stripes are completely removed, is electrically single domain at the wafer-scale. This is

Significance

The use of epitaxial graphene has been less favored over the use of chemical vapor deposition (CVD)-grown polycrystalline graphene because graphene formed near SiC vicinal steps accompanies carrier scattering, which makes the practical domain size of epitaxial graphene much smaller than that of CVD-grown graphene. Nonetheless, the origin of carrier scattering at the SiC vicinal steps has not been fully understood. Here, we experimentally reveal that graphene formed at side walls is pristine, and the scattering near the steps mainly originates from the deformation of graphene and partially from stripes of bilayer graphene. This understanding of the origin of scattering allows us to demonstrate large-size single-domain graphene, removing major scattering sources through a layer-resolved transfer.

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clear contrast to our previous report where we have shown only crystallographic single crystallinity in graphene through LRGT due to the uncertainty of the quality of graphene near the terrace edges of SiC (26). Further elimination of the process residues during the LRGT leads to a notable maximum mobility of 7,496 $cm^2/V{\cdot}s$ measured at room temperature for a single-crystalline, single-domain graphene transferred on a SiO_2/Si substrate, which supersedes as the highest value ever reported from graphene formed on the Si face of an SiC wafer (15, 16, 21–23, 27–29).

Results and Discussion

We have performed a one-step LRGT process using a graphitized SiC wafer where graphene is mechanically exfoliated using a high-stress Ni film (26) (see *Materials and Methods* for the detailed process parameters). The entire graphene, successfully released from the SiC surface, was then transferred onto an oxidized Si wafer followed by Ni etching. Fig. 1*A* shows a photograph of 4-inch wafer-scale graphene transferred on an 8-inch oxidized Si wafer using the LRGT process. A schematic of this process is depicted in Fig. 1*B*, showing the flattening of deformed graphene at the step edge and side-wall graphene. We first measured a Raman spectra on graphene/SiC to evaluate the quality of grown graphene on SiC (Fig. S1). As shown in the map of the 2D/G peak ratio from a Raman spectra taken on a transferred single-crystalline graphene layer (Fig. 1*C*) (30), this graphene is composed of a monolayer sheet and around 20% bilayer stripes, called 1.2 ML hereafter (blue, bilayer; green, monolayer). Through atomic force microscopy (AFM), we investigated the surface topography of original epitaxial graphene on the Si-face SiC wafer and transferred epitaxial graphene on the SiO_2/Si substrate. As shown in Fig. 1 *D* and *E*, ∼10-nm-high steps periodically exist at every ∼10-μm-wide terrace; after transferring graphene to a flat SiO_2/Si surface, these steps in graphene were no longer present and graphene was well-flattened to the substrate without formation of wrinkles (31). The flattening of graphene may improve carrier transport because mobility degradation in epitaxial graphene on SiC is known to arise from the curved morphology of graphene at step edges (19, 20). However, the presence of bilayer stripes in the transferred graphene can still increase carrier scattering.

It has been known that the resistance of bilayer graphene was substantially greater than that of monolayer graphene due to enhanced backscattering in bilayer graphene (32, 33). Therefore, periodically distributed bilayer stripes in flat 1.2-ML graphene transferred on SiO_2/Si would certainly account for carrier scattering. For further investigation on carrier transport in 1.2 ML, we fabricated backgated FETs on the transferred graphene on SiO_2/Si substrates. (Fig. S2) FET channels were formed orthogonal to the bilayer stripes as shown in Fig. 2 *A* and *B*, which contain bilayer stripes of varying periodicity across the channel, where the width of stripes had a uniformly distributed average of 800 nm. The scanning electron microscope (SEM) images shown in Fig. 2 *A* and *B* represent the graphene FET channels, including one and four bilayer stripes located in a 10-μm-long channel, respectively. Field effect (FE) electron mobility and channel resistance were extracted at a maximum transconductance where the carrier density was $\sim 1 \times 10^{12}\ cm^{-2}$ at a room temperature. Fig. 2 *C* and *D* show average resistance and average electron FE mobility of a graphene channel with 10-μm length and 2-μm width as a function of the number of stripes in the channel, respectively. A monotonic increase in the average resistivity of graphene was observed as the number of stripes in the channel increased, reducing the mobility of graphene. The resistance increment attributed by one bilayer stripe in the channel was measured by taking a slope of the plot in Fig. 2*C*; the value normalized by the channel width was

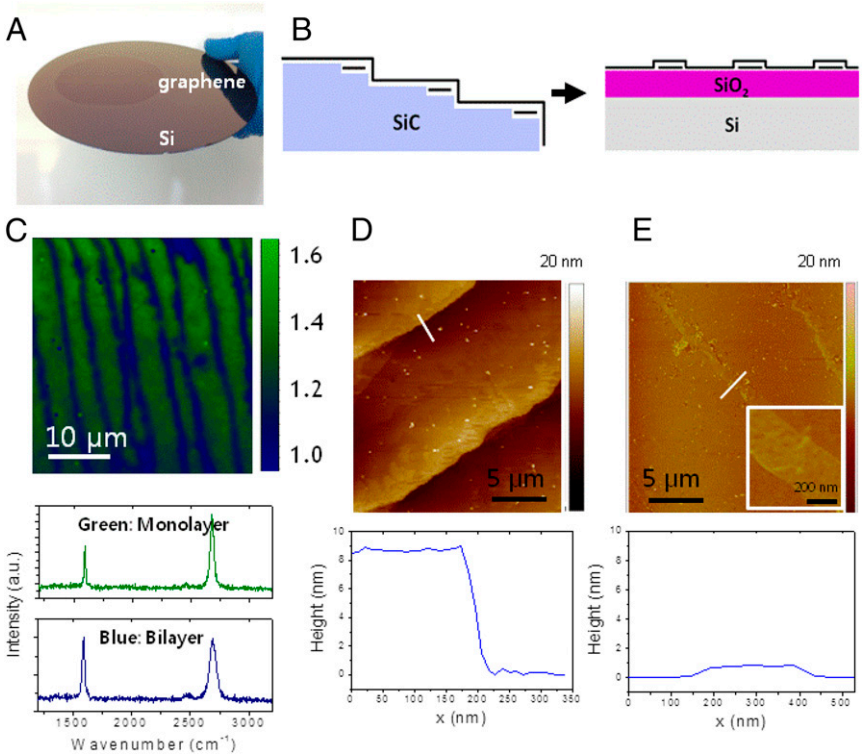

Fig. 1. Optical properties and topography of single-oriented graphene. (*A*) Four-inch wafer-scale single-oriented graphene on 8-inch oxidized Si wafers via LRGT. (*B*) Schematic graphene structures before and after LRGT. (*C*) Map of the 2D/G peak ratio from Raman spectra (green color, monolayer graphene; blue color, bilayer graphene). (*D*) Tapping mode AFM images from graphene on Si-face SiC wafer and profile information. (*E*) Tapping mode AFM images from graphene transferred on SiO/Si wafer via LRGT and profile information.

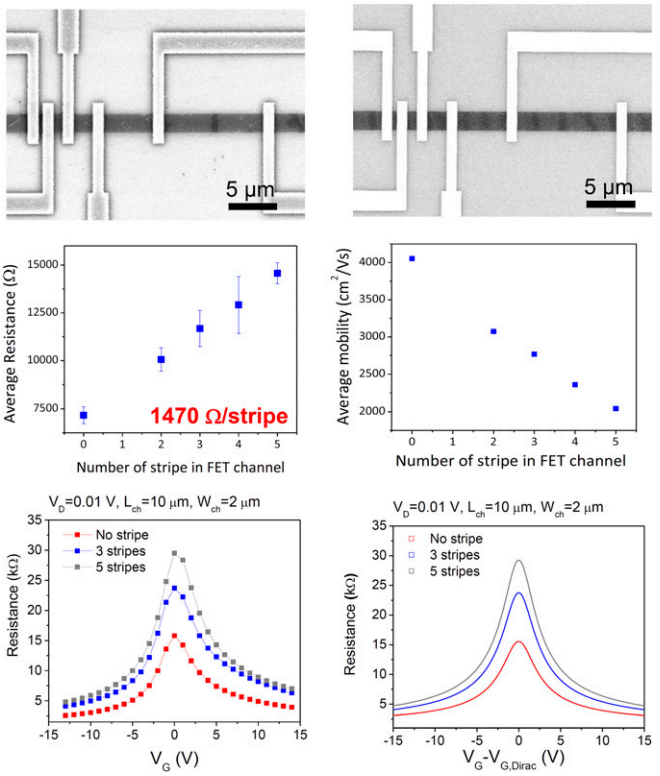

Fig. 2. Influence of bilayer stripes. (*A*) SEM images on graphene FET channels containing one bilayer stripe in a 10-μm-long channel and (*B*) four bilayer stripes in a 10-μm-long channel. (*C*) Monotonic increase in average resistance as a function of number of stripes in the channel. The resistance increment by a single bilayer stripe is 1,470 Ω. (*D*) Average electron FE mobilities of a graphene channel according to the number of stripes in FET channel. (*E*) Experimentally measured R_{CH}–V_G characteristics and (*F*) simulated R_{CH}–V_G characteristics of graphene channel vs. number of stripes.

2.94 kΩ·μm. This resistance value is an order of magnitude lower than the reported value of 21 kΩ·μm obtained from a 10-nm-high single step in our graphene on SiC (21) where the resistance jump occurs from the multiple causes such as graphene bending, local thickness variation due to bilayer stripes, and lower-quality graphene at the side wall of the step. This indicates that most of the carrier-scattering sources in epitaxial graphene before exfoliation were removed during the graphene transfer process in LRGT. However, graphene near bilayer stripes still plays a role in disturbing carrier transport due to backscattering at the body of bilayer graphene (32) or variations in electrical quality of graphene formed at the SiC side wall. However, wavefunction mismatch at a bilayer–monolayer junction does not play a major role in the mobility of 1.2-ML graphene (19) because the extra resistance from the wavefunction mismatch is much smaller (at least an order of magnitude lower) compared with what we observed. The effect of intensified scattering at the bilayer on the resistance of 1.2-ML graphene can be isolated by modeling electrical characteristics of flat monolayer graphene FETs containing periodic bilayer stripes. Under the assumption that the rise in resistance with increasing number of stripes is solely due to enhanced backscattering at the body of a bilayer stripe, we simulated a graphene FET with a channel that had a series connection of monolayer graphene and bilayer graphene stripes (average width of 700 nm) by varying the number of bilayers in the channel (Fig. S3). This allowed us to predict the increase in resistance from adding a single bilayer stripe in a graphene channel, which was measured to be 3 kΩ·μm, comparable to the value obtained from experiment. Moreover, simulated resistance-gate voltage characteristics of graphene channels for varying number of stripes showed excellent agreement with those experimentally measured (Fig. 2 *E* and *F* and Table S1). In the simulation result, monolayer mobility, residual carrier density, and the contact resistance were taken from the monolayer resistance without any bilayer stripe (Fig. S4 and Fig. 2*E*), and then the bilayer device parameters were extracted from samples with bilayer stripes. We simulated the result with extracted parameters, which are summarized in Table S2. With extracted information, we ensure that the resistance increase with stipes originates from the carrier transport through the monolayer and bilayer regions connected in series (see *SI Text* for details). This confirms that (*i*) electrical degradation in flat graphene transferred from SiC is solely attributed to the existence of bilayer stripes, (*ii*) substantial resistance jump at epitaxial graphene on SiC steps is mainly attributed to the sharp bending of graphene that may cause π–σ hybridization (19, 20), and (*iii*) graphene grown at the side wall of a SiC step does not contribute to electrical degradation in transferred graphene.

For further confirmation, we fabricated FETs following specific locations pointed in the SEM image in Fig. 3*A*: (A) between the bilayer stripes, (B) on the graphene where the stripe was accidentally removed during the process, and (C) on the bilayer stripe. The electron mobility measured from regions A and B were comparable, whereas region C showed degradation of mobility (Fig. 3*B*). This suggests that graphene on the location where the bilayer stripe was accidentally removed during the transfer process does not have any memory effect of having had a bilayer stripe or having been deformed, and again graphene grown at the SiC step side wall is pristine. To support this claim, scanning tunneling microscopy (STM) was performed to obtain atomic-resolution images. A scan was performed across the bilayer stripes in the graphene; the trace of the scan is depicted by the red line in Fig. 3*A*. Fig. 3 *C* and *D* shows STM surface topologies, and we could identify (*i*) a honeycomb lattice structure with a lattice constant of

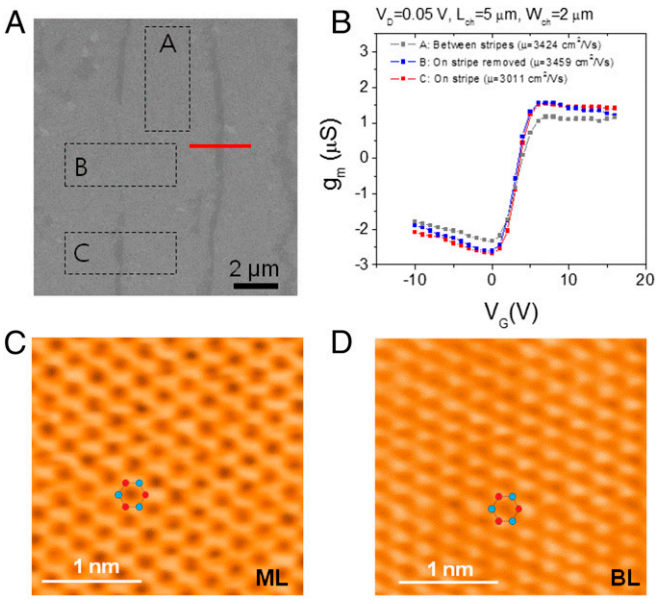

Fig. 3. Graphene grown at side-wall surfaces of SiC vicinal steps. (*A*) SEM images of graphene after LRGT on SiO/Si wafer. FET was fabricated on three different regions: A region, between the bilayer stripes; B region, on the graphene where the stipe was removed during the process; and C region, on the bilayer stripe. (*B*) FET output characteristics from three different sites at A region, B region, and C region. From the result, we can conclude the device performances from A region and B region are similar, whereas the device performance from C regions shows degradation of mobility. (*C* and *D*) Atomic-resolution STM images of single-crystalline graphene from monolayer graphene and bilayer graphene.

2.4 Å from monolayer graphene and (*ii*) a hexagonal lattice structure from bilayer graphene due to the AB stacking of the layers breaking the symmetry, leading to two inequivalent C atoms per unit cell. Throughout scanning across the stripe along the red line in Fig. 3*A*, we could only identify perfect hexagonal monolayer and bilayer images, which supports the fact that the graphene coming from the SiC step side wall is pristine.

Although carrier scattering arising from geometric factors can be suppressed by flattening, uniform electrical quality of our single-crystalline graphene is still limited by the existence of periodic bilayer stripes. Considering the fact that the mobility measured from the location where the stripe was locally removed is comparable to that from the location between the stripes (Fig. 3*A*), the graphene transferred from SiC can be domain-free if the stripes are completely removed. We have performed a two-step LRGT process to selectively remove the bilayer stripes with single-atom thickness precision (25). In this process, Au is deposited on the as-exfoliated graphene on Ni film. Because the Au–graphene interface bonding energy is higher than that of the graphene–graphene interface, graphene stripes on a graphene sheet can be selectively lifted off by Au. During the exfoliation process, the monolayer graphene sheet remains bonded to Ni because the bonding energy between Ni and graphene is much higher than the bonding energy between Au and graphene. As shown in the map of the 2D/G peak ratio from a Raman spectra taken on the graphene layer transferred by this two-step LRGT process (Fig. 4*A*), bilayer stripes were completely removed from the monolayer graphene sheet, leaving only a monolayer sheet. This monolayer graphene sheet was transferred on a SiO_2/Si wafer. To quantify the electrical properties and uniformity of graphene, FETs were fabricated on the monolayer of graphene prepared using the two-step LRGT (1-ML graphene) as well as on monolayer graphene with 20% bilayer stripes prepared by a one-step LRGT (1.2-ML graphene). The electron FE mobility was recorded at the maximum transconductance; the mobility distribution is shown in Fig. 4*B*. The 1-ML graphene presented a marked improvement in mobility compared with 1.2-ML graphene with measured values concentrating near 4,000–5,000 cm^2/V·s.

The single crystallinity was confirmed by microspot electron diffraction measurements using a low-energy electron microscope (LEEM), where we observed identical diffraction patterns across the sample (Fig. 4*C*). A maximum FE electron mobility of 7,496 cm^2/V·s obtained from our single-crystalline, single-domain graphene at room temperature (Fig. 4*D* and Fig. S5) is the highest value ever reported from the graphene grown on Si-face SiC wafer (Fig. S6) (15, 16, 21–23, 27–29). It should be noted that, in our previous report (26), enhanced mobility due to flattening the epitaxial graphene is screened by the Ni residues on graphene after chemical etching of the Ni stressor. As shown in Fig. S7, choice of Ni etching solution substantially affects the mobility of single-domain graphene due to the effectiveness of removing the residues. When typical acid solutions such as HCl and $FeCl_3$ for metal etching are used to remove Ni stressors, the substantial Ni residues reside on the graphene surface, resulting in the mobility of around 3,000 cm^2/V·s, which is a comparable value typically measured from the epitaxial graphene on SiC substrates. Substantial mobility enhancement to 7,496 cm^2/V·s is observed from the epitaxial graphene with the reduction of Ni residues with postetching treatment by a TFB transene Ni etchant. The device result shows the actual improvement of the mobility of epitaxial graphene by separating it from the SiC substrate and flattening it on the flat SiO_2 surface. There is more room for improving the mobility of this graphene because Ni residues with average size of 2 nm still remained after etching, as shown in the AFM image (Figs. S7 and S8) (33), and graphene FETs fabricated on SiO_2 substrates accompany carrier scattering from charged surface states and impurities of SiO_2 (34, 35).

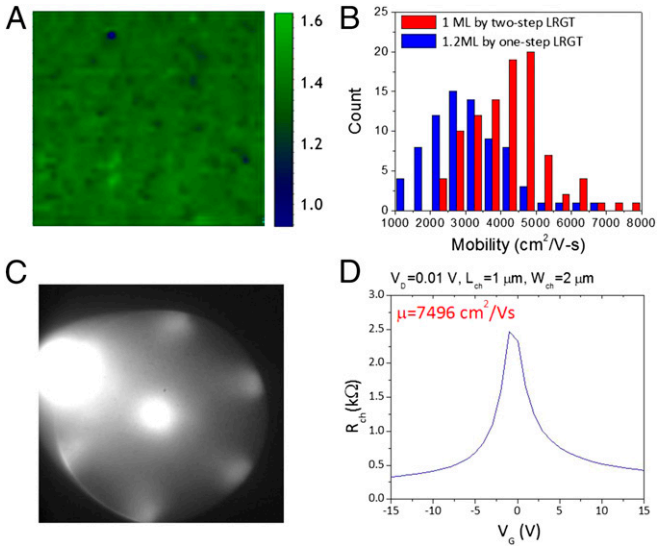

Fig. 4. Device performances of monolayer, single-oriented graphene. (*A*) Raman mapping result of the 2D/G peak ratio on the graphene. Because the bilayer stripes were removed by LRGT, the mapping color is almost uniform. (*B*) The electron FE mobility distribution comparison between device based on graphene before and after LRGT. (*C*) Microspot electron diffraction from low-energy electron microscope (LEEM). Identical diffraction patterns across the sample were observed. (*D*) Channel resistance as a function of gate voltage from single-crystalline graphene. Maximum electron mobility of 7,496 cm^2/V·s was obtained.

Conclusions

In summary, we demonstrated that geometry-induced carrier scattering at epitaxial graphene on SiC can be avoided by transferring this graphene to a flat surface. Finally, this graphene is rendered domain-free by selectively removing intrinsically present bilayer stripes. We further identified the origin of carrier scattering at SiC vicinal steps, the role of each bilayer stripe, and evidence that the LRGT process can prepare domain-free graphene.

Materials and Methods

Growth of Epitaxial Graphene. A 4-inch epitaxial graphene was grown on a Si-face (0001) 4H-SiC wafer with 0.05° miscut. The SiC substrate was annealed at 850 °C for 20 min for surface cleaning in vacuum (<1 × 10^{-6} mbar). The substrate temperature was raised to 1,555 °C for 30 min, and H_2 was introduced into the chamber (800 mbar) for 30 min for a second surface cleaning by thermally etching the top layers of SiC. The graphene was subsequently formed on the SiC surface in Ar ambient (100 mbar) at 1,575 °C for 60 min by sublimating the Si atoms from the SiC surface.

LRGT (One-Step Exfoliation). Epitaxial graphene formed on SiC was exfoliated from the SiC wafer by depositing highly strained, adhesive nickel (Ni) film on graphene followed by application of a thermal-release tape handler for mechanical exfoliation of Ni bonded with graphene. Because the bonding energy of Ni–graphene is greater than that of SiC–graphene (16), Ni was used as an adhesive layer to compete for graphene bonding during the exfoliation process. In the graphene release process, SiC–graphene bonding energy was overcome by the strain energy provided by Ni film, leading to complete mechanical exfoliation of graphene from SiC (12). It was essential to evaporate 30-nm Ni initially to protect the damage on graphene and subsequently sputter 500-nm Ni to provide the strain energy. The graphene released from the SiC surface was then transferred onto an oxidized Si wafer, followed by removal of the handling tape and wet etching of the nickel film.

LRGT (Two-Step Exfoliation). To obtain a domain-free graphene, the bilayer stripes must be completely removed from the one-step–exfoliated graphene. A two-step LRGT process was applied to selectively remove the bilayer stripes with single-atom thickness precision. In this process, after the graphene

exfoliation using a Ni film, Au is deposited on the as-exfoliated graphene on Ni. Because the Au–graphene interface bonding energy is higher than that of the graphene–graphene interface, graphene stripes on a graphene sheet can be selectively lifted off by Au. During the selective exfoliation process, monolayer graphene sheet remains bonded to Ni because the bonding energy of the Ni–graphene interface is much higher than that of the Au–graphene interface. The complete monolayer graphene on Ni/tape was then transferred onto an oxidized Si wafer, followed by removal of the tape and wet etching of the nickel film.

Device Fabrications and Electrical Characterizations. The FETs were fabricated on graphene sheet on oxidized Si wafers (90-nm-thick SiO_2/highly doped *n*-type Si). The channel length of transistors was defined from 0.5 to 10 μm with 2-μm width by LEICA VB6 e-beam writer. The electrodes were made of Ti (0.2 nm)/Pd (20 nm)/Au (20 nm). After patterning electrodes via electron beam lithography, Agilent B5100 semiconductor parameter analyzer was used for all current–voltage measurement at room temperature in $\sim 10^{-7}$ torr. The SiO_2 was used as a gate insulator and Si worked as a backgate.

Surface Imaging via STM. STM experiments were performed with a cryogenic ultrahigh-vacuum STM system combined with SEM. The ability to carry out SEM in our system allowed us to easily locate and measure monolayer and bilayer graphene, respectively. The STM topography was taken in the constant current mode using a Pt–Ir tip for imaging. All of the STM measurements were conducted at 77 K.

1. Novoselov KS, et al. (2004) Electric field effect in atomically thin carbon films. *Science* 306:666–669.
2. Lee C, Wei X, Kysar JW, Hone J (2008) Measurement of the elastic properties and intrinsic strength of monolayer graphene. *Science* 321:385–388.
3. Seol JH, et al. (2010) Two-dimensional phonon transport in supported graphene. *Science* 328(5975):213–216.
4. Zhang Y, Tan Y-W, Stormer HL, Kim P (2005) Experimental observation of the quantum Hall effect and Berry's phase in graphene. *Nature* 438:201–204.
5. Novoselov KS, et al. (2005) Two-dimensional gas of massless Dirac fermions in graphene. *Nature* 438:197–200.
6. Grantab R, Shenoy VB, Ruoff RS (2010) Anomalous strength characteristics of tilt grain boundaries in graphene. *Science* 330:946–948.
7. Lin Y-M, et al. (2011) Wafer-scale graphene integrated circuit. *Science* 332:1294–1297.
8. Lin Y-M, et al. (2010) 100-GHz transistors from wafer-scale epitaxial graphene. *Science* 327:662.
9. Bae S, et al. (2010) Roll-to-roll production of 30-inch graphene films for transparent electrodes. *Nat Nanotechnol* 5:574–578.
10. Han T-H, et al. (2012) Extremely efficient flexible organic light-emitting diodes with modified graphene anode. *Nat Photonics* 6:105–110.
11. Bae S-H, et al. (2013) Graphene-based transparent strain sensor. *Carbon* 51:236–242.
12. Dikin DA, et al. (2007) Preparation and characterization of graphene oxide paper. *Nature* 448(7152):457–460.
13. Kim KS, et al. (2009) Large-scale pattern growth of graphene films for stretchable transparent electrodes. *Nature* 457:706–710.
14. Li X, et al. (2009) Large-area synthesis of high-quality and uniform graphene films on copper foils. *Science* 324:1312–1314.
15. Emtsev KV, et al. (2009) Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide. *Nat Mater* 8:203–207.
16. Avouris P, Dimitrakopoulos C (2012) Graphene: Synthesis and applications. *Mater Today* 15:86–97.
17. Borovikov V, Zangwill A (2009) Step-edge instability during epitaxial growth of graphene from SiC (0001). *Phys Rev B* 80:121406.
18. Tanaka S, Morita K, Hibino H (2010) Anisotropic layer-by-layer growth of graphene on vicinal SiC (0001) surfaces. *Phys Rev B* 81:041406.
19. Ji S-H, et al. (2011) Atomic-scale transport in epitaxial graphene. *Nat Mater* 11: 114–119.
20. Low T, Perebeinos V, Tersoff J, Avouris P (2012) Deformation and scattering in graphene over substrate steps. *Phys Rev Lett* 108:096601.
21. Lin Y-M, et al. (2011) Enhanced performance in epitaxial graphene FETs with optimized channel morphology. *IEEE Electr Device L* 32:1343–1345.
22. Yakes MK, et al. (2010) Conductance anisotropy in epitaxial graphene sheets generated by substrate interactions. *Nano Lett* 10:1559–1562.
23. Dimitrakopoulos C, et al. (2011) Effect of SiC wafer miscut angle on the morphology and Hall mobility of epitaxially grown graphene. *Appl Phys Lett* 98:222105.
24. Yu Q, et al. (2011) Control and characterization of individual grains and grain boundaries in graphene grown by chemical vapour deposition. *Nat Mater* 10: 443–449.
25. Li X, et al. (2010) Graphene films with large domain size by a two-step chemical vapor deposition process. *Nano Lett* 10:4328–4334.
26. Kim J, et al. (2013) Layer-resolved graphene transfer via engineered strain layers. *Science* 342:833–836.
27. Kageshima H, Hibino H, Tanabe S (2012) The physics of epitaxial graphene on SiC(0001). *J Phys Condens Matter* 24:314215.
28. Pallecchi E, et al. (2014) High electron mobility in epitaxial graphene on 4H-SiC(0001) via post-growth annealing under hydrogen. *Sci Rep* 4:4558.
29. Dimitrakopoulos C, et al. (2010) Wafer-scale epitaxial graphene growth on the Si-face of hexagonal SiC (0001) for high frequency transistors. *J Vac Sci Technol B* 28:985–992.
30. Ferrari AC, et al. (2006) Raman spectrum of graphene and graphene layers. *Phys Rev Lett* 97:187401.
31. Suk JW, et al. (2011) Transfer of CVD-grown monolayer graphene onto arbitrary substrates. *ACS Nano* 5:6916–6924.
32. Adam S, Sarma SD (2008) Boltzmann transport and residual conductivity in bilayer graphene. *Phys Rev B* 77:115436.
33. Pi K, et al. (2009) Electronic doping and scattering by transition metals on graphene. *Phys Rev B* 80:075406.
34. Banszerus L, et al. (2015) Ultrahigh-mobility graphene devices from chemical vapor deposition on reusable copper. *Sci Adv* 1:e1500222.
35. Dean CR, et al. (2010) Boron nitride substrates for high-quality graphene electronics. *Nat Nanotechnol* 5:722–726.
36. Park H, et al. (2012) High-density integration of carbon nanotubes via chemical self-assembly. *Nat Nanotechnol* 7:787–791.
37. Kim S, et al. (2009) Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric. *Appl Phys Lett* 94:062107.
38. Lee K, et al. (2011) Magnetotransport properties of quasi-free-standing epitaxial graphene bilayer on SiC: Evidence for Bernal stacking. *Nano Lett* 11:3624–3628.
39. Adam S, Hwang EH, Galitski VM, Das Sarma S (2007) A self-consistent theory for graphene transport. *Proc Natl Acad Sci USA* 104:18392–18397.
40. Liang X, et al. (2011) Toward clean and crackless transfer of graphene. *ACS Nano* 5:9144–9153.