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Analog/Mixed Signal Circuit Design with Transparent Oxide Semiconductor Thin-Film Transistors

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Dedicated to my family members

Abstract

Amorphous Gallium Indium Zinc Oxide (a-GIZO) belongs to the new class of amorphous oxide semiconductors (AOS) that have gained a significant interest in recent years as active layers for thin-film transistors (TFTs). Fabrication with a-GIZO is highly cost effective due to possible low-temperature processes, and the material itself is almost fully transparent to the visible spectrum of light, opening a panoply of new application possibilities. Low-temperature fabrication allows the use of different substrates, with direct device level printing, such as in paper, plastic or glass, allowing the construction of flexible as well as transparent electronic devices at exceedingly competitive prices. Furthermore, a-GIZO presents better electrical characteristics than other TFT technologies, such as a-Si:H and organic TFTs (OTFTs). All these features will push even more the a-GIZO to the mainstream consumer electronics. Up to date, however, the TFT technologies have been almost exclusively used for displays, RFIDs [1, 2] and sensor fabrication [3, 4]. Nevertheless, there is still little emphasis towards circuit design with a-GIZO TFTs. The main goal of this PhD work is then to develop a framework and circuits, which will ultimately accomplish the necessary conditions to design electronic systems with post-silicon technology, specifically with a-GIZO TFTs.

Particular attention will be given in this dissertation to circuit design, with the goal of achieving an integrated system based on a single substrate, where the sensors and signal processing or conditioning circuits can be realized with the same technology. In order to make such system feasible with a-GIZO, the development of analog processing and conditioning circuits are required. Then the present work focuses on the development, design and fabrication of various important analog/mixed signal building blocks needed to perform signal processing and conditioning. Further testing, feasibility and limitations of the technology for circuit design is analysed. As a first step, a neural-based equivalent circuit model is developed from the measured characteristics of the device, both from the static and dynamical perspective. Finally, simulation outcomes are validated against the measured response from the fabricated circuits.

Basic analog building blocks, such as different types of current mirrors, buffers, (common source) CS amplifier, differential pair, novel high-gain amplifiers, adders, multipliers, logic gates, high-gain comparator and four-bit folding analog to digital converter (ADC) were designed, simulated and fabricated. Some of these circuits were successfully characterized. During the comparator design, care has been taken to minimize the bias stress impact. The single stage novel amplifier, in this work, resulted in the highest gain with a-GIZO TFT technology so far. Similarly, the comparator and the folding ADC are the first mixed signal building blocks designed with a-GIZO, at least until the time of writing of this document.

The research work was developed in collaboration with CENIMAT group at UNL, where all the above mentioned circuits were fabricated.

Keywords: a-GIZO TFTs. Neural modeling. Circuit design.

Resumo

Os óxidos amorfos de Índio Gálio e Zinco (a-GIZO) pertencem a uma nova classe de óxidos semicondutores amorfos (AOS) que nos últimos anos tem ganhado um interesse significativo da comunidade científica, como elemento na camada ativa de transístores de filme fino (TFT). A fabricação a baixa temperatura, com consequentes baixos custos de fabricação e melhores características elétricas em comparação com outras tecnologias TFT, como a-Si:H e TFTs orgânicos (OTFTs), são as principais características responsáveis pela atenção que os TFTs baseados em a-GIZO têm recebido. O material a-GIZO é transparente no espectro de luz visível e a fabricação de baixa temperatura possibilita o uso de diferentes substratos, como papel, plástico ou vidro, permitindo a construção de dispositivos eletrónicos flexíveis e transparentes, a custos extremamente competitivos. Sendo um processo de baixo custo que tem como base dispositivos eletrónicos flexíveis e transparentes, potencia um vasto conjunto de novas aplicações. No entanto, e até ao momento, as tecnologias TFT têm sido usadas quase exclusivamente para monitores (flat displays), dispositivos RFID [1, 2] e na fabricação de sensores [3, 4], havendo muito pouca ênfase no projeto de circuitos com dispositivos a-GIZO. O principal objetivo deste trabalho de doutoramento é, então, desenvolver uma estrutura que permita reunir as condições necessárias para projetar circuitos eletrónicos com tecnologia de pós-silício, especificamente com TFTs a-GIZO. Um dos objetivos principais desta dissertação é a concepção de circuitos, no sentido de alcançar um sistema totalmente integrado usando um único substrato, onde os sensores e circuitos de processamento e condicionamento de sinal possam ser realizados com a mesma tecnologia. A fim de tornar possível tal realização com a-GIZO, é necessário desenvolver os respetivos circuitos. Por essa razão o presente trabalho concentra-se no desenvolvimento, projeto e fabricação de vários blocos analógicos e mistos importantes e necessários para a realização do processamento e condicionamento de sinal. Numa primeira fase é desenvolvido um modelo equivalente elétrico, com base em redes neuronais e a partir das características de medição do dispositivo, que caracterize corretamente o comportamento estático e dinâmico do dispositivo, tendo como objeto a possibilidade de simulação elétrica. De seguida, com base neste modelo, circuitos clássicos bem como novas propostas são simulados apenas com TFTs de enriquecimento do tipo n. Finalmente, os resultados da simulação de circuitos são validados com a resposta medida dos respetivos circuitos fabricados. São desenvolvidos e fabricados vários blocos analógicos básicos, tais como diferentes tipos de espelhos de corrente, buffers, amplificador de CS (*Common Source* ou fonte comum), par diferencial, novos amplificadores de alto ganho, somadores, multiplicadores, portas lógicas, comparador de elevado ganho e um conversor analógico/digital (ADC) de 4 bits. Durante o projeto do comparador, vários cuidados foram tomados no sentido de minimizar o stress de polarização. O amplificador de andar único proposto resultou no maior ganho obtido com TFTs a-GIZO até ao momento. Da mesma forma, o comparador e o ADC são os primeiros blocos de sinal misto até a data. Este trabalho desenvolve-se com o grupo do CENIMAT na UNL, responsáveis pela

fabricação dos circuitos descritos no presente trabalho.

Keywords: a-GIZO TFTs. Neural modeling. Circuit design.

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Pydi Ganga Mamba Bahubalindruni

"Arise, awake, and stop not till the goal is reached"

Swami Vivekananda

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Abbreviations, Acronyms and Symbols

$\Delta\Sigma$	Delta sigma
σ	Gaussian function spread
AC	Alternating current
ADC	Analog-to-digital converter
AOS	Amorphous oxide semiconductor
ANN	Artificial neural network
a-GIZO	Amorphous gallium-indium-zinc-oxide
a-Si:H	Hydrogenated amorphous silicon
BP	Back propagation
CAD	Computer-aided design
CMOS	Complementary metal-oxide-semiconductor
CMRR	Common-mode rejection ratio
CS	Common source
DAC	Digital-to-analog converter
DC	Direct current
DRC	Design rule check
FPD	Flat-panel display
FPGA	Filed programmable gate array
IC	Integrated circuit
IZO	Indium zinc oxide
LPCVD	Low temperature chemical vapor deposition
LS-SVM	Least square support vector machine
LSB	Least significant bit
LTPS	Low temperature poly silicon
LVS	Layout versus schematic
MLP	Multi layer perceptron
MSB	Mostt significant bit
Mo	Molybdenum
Ti-Au	Titanium gold
MOSFET	Metaloxidesemiconductor field-effect transistor
MSE	Mean square error
NMOS	N-type metal-oxide-semiconductor
OTFT	Organic thin-film transistor
Opamp	Operational amplifier
PP	Piece-wise polynomial
PV	photo voltaic
RBF	Radial basis function

RFID	Radio frequency identification
RPI	Rensselear polytechnic institute
SAR	Successive approximation register
SIC MESFET	Silicon carbide metal semiconductor field effect transistor
SPICE	Simulation program with integrated circuit Emphasis
TCO	Transparent conductive oxide
TFT	Thin-film transistor
ZnO	Zinc-oxide

dB	decibel
g_{ds}	Output transconductance
g_m	transconductance
Hz	Hertz
r_{ds}	Intrinsic output resistance of a transistor
μ	Charge carrier mobility
V_{TH}	threshold voltage
μ_n	Charge carrier mobility in n-type semiconductor
mW	milli Watt
ε_r	Relative dielectric constant

Chapter 1

Introduction

Although the first thin-film transistors (TFTs) and metal oxide semiconductor field-effect transistors (MOSFETs) were both conceived during the 1960s, TFT mass production only happened during the 1980-90s, motivated by their application in active matrix liquid crystal displays (AMLCDs) [6]. Low temperature poly-crystalline silicon (LTPS) [7], amorphous hydrogenated silicon (a-Si:H) [8], organic (O) [9] and amorphous oxide semiconductor based (AOS) TFTs [10] are some of the most reported TFT technologies. Even though TFTs are mainly used for displays [7, 8, 11, 12], their application scope is rapidly expanding to the fields of radio-frequency identification (RFID) tags [2], sensing devices [13, 14, 15], X-ray image sensors [3, 4], transparent, large flexible antenna arrays, medicine and low-cost disposable electronics [16].

Amorphous gallium-indium-zinc-oxide (a-GIZO) is an example of a multi-component AOS material. Its usage in active devices is relatively new, but has already gained significant attention from both academia and industry. Competing TFT technologies such as LTPS TFTs provide high-speed electronics due to their high field-effect mobility (μ), which is exceeding 100 $cm^2/V{\cdot}s$, but their poly-crystalline nature hinders uniformity in large area electronics. On the other hand, a-Si:H TFTs and OTFTs are suitable for large area fabrication but the range of applications is limited by the low μ, typically below 1 $cm^2/V{\cdot}s$. a-GIZO TFTs provide a combination of the good properties of these technologies, exhibiting high μ (10-50 $cm^2/V{\cdot}s$), reliability, uniformity, low-temperature and low-cost fabrication - allowing for flexible electronics - and transparency in the visible spectrum. In fact, fully transparent TFTs can be realized with a-GIZO when accompanied by transparent conductive oxides (TCOs) [17, 18, 19] for source/drain electrodes, such as indium-zinc oxide (IZO) [20]. Even though, thin-film technologies should not be seen as an alternative to the conventional complementary metal oxide semiconductor (CMOS) technologies, a-GIZO TFT based circuits can find niche applications in some specific areas where CMOS is not able to meet the requirements. For example, cost-effective analog/mixed-signal circuits for signal conditioning could in principle be directly printed on the photovoltaic (PV) panels, by using a-GIZO TFTs with TCO electrodes. Transparent displays with transparent driving circuits can also be realized with this technology. Unique properties of TCOs [21], such as, good optical transparency and low-temperature fabrication makes the above applications realizable. In addition, by integrating

sensors with the signal conditioning circuits in the same technology results in low-cost and reliable integrated systems that can avoid complex interfacing connections. The above potential applications and good device characteristics strongly incentivize the design of analog/mixed-signal circuits with a-GIZO TFTs, which serves as a token of motivation for the work presented along this dissertation.

Current mirrors, high-gain amplifiers, buffers, logic gates, comparator, adders, subtractor and multipliers are some of the essential building blocks needed in the design of analog/mixed signal circuits. Several of these circuits have already been reported with a-Si:H TFTs and OTFTs, namely basic analog blocks [22, 23, 5], a high-gain operational amplifier [24], comparator [25] and data converters [26, 27, 28]. On the other hand very few are presented with a-GIZO TFTs [29, 30].

1.1 Main objectives

Although a-GIZO TFT technology is very appealing, it still has many shortcomings that results in a number of challenges. Lack of stable complementary (p-type) transistors, bias stress and inferior mobility, compared to the crystalline silicon, are some of the main limiting factors for circuit design. Being a-GIZO TFT an emerging technology, device models or technology libraries that support standard IC design are also not available. In this context, the main objective of the dissertation is to develop a platform in which a-GIZO TFT based circuits can be designed in the same way as any other standard semiconductor integrated circuits and develop and characterize traditional and novel circuits that can be employed in generic electronic design. This goal is accomplished by the following four phases:

1. **Model Development:** As the semiconductor material (GIZO) is amorphous, the MOSFET models cannot be adopted, since they use crystalline silicon as semiconductor. In addition, MOSFETs operate in inversion modes and strongly depend on the properties of the several p-n junctions existing in the device, contrarily to TFTs, where the device operation relies on accumulation mode and metal-semiconductor junctions. On the other hand, Rensselear polytechnic institute (RPI) model, which is widely used to characterize a-Si:H TFT, is also insufficient to predict unique properties of AOS (a-GIZO) TFT behavior accurately [31, 32]. In literature, very few articles report physical-based modeling for basic characterization of the a-GIZO TFT i.e., static and dynamic behavior and even these models are not optimized for circuit simulators. Consequently, they take a good amount of simulation time when complex circuits are involved. Many groups are working to ensure better behavior of a-GIZO TFTs either by employing new materials (for source/drain, dielectric) [18, 33, 34], different structures for the devices (bottom gate, top gate, multi-channel, dual gate) [35, 36] and alternative fabrication techniques [37]. Whenever there is a change in the material or process, certainly there will be an impact on the carrier flow. Thus, the corresponding device physics needs to be studied further, in order to contemplate the model with the new characteristics. Therefore, for the new technologies, when a quick circuit design is important, physical modeling is not an ideal choice, even though it is required for process optimization. Subse-

quently, in this dissertation, artificial neural networks (ANNs) have been employed as they are universal approximators, simple, accurate and continuous (model and its derivatives). In addition, their memory requirements are lower compared to the table-based modeling. Different ANN techniques, such as, multi-layer perceptron (MLP), radial basis functions (RBF) and least square support vector machine (LS-SVM) are experimented and compared in order to characterize the static behavior of the device. These models are developed from the measured characteristics of the device. Among the above mentioned ANN methods, MLP shows a reasonable accuracy level, with minimum complexity. Consequently, MLP network has been further implemented in Verilog-A for circuit simulation. The incorporation of dynamics in the model follows an equivalent-circuit approach, in which the electrical equivalent-circuit, using lumped elements, is firstly devised. Then all the individual elements are modeled by means of ANNs. Later, all the ANN networks are joined as per the equivalent circuit of the device. Finally the model outcome is validated with the measured circuit response. The developed model is able to simulate complex circuits with more than 600 transistors along with few tens of passive elements (resistors and capacitors). Further, characterization of passive devices, namely resistors and capacitors was also carried out. Nonetheless, the interconnect parasitic capacitance to substrate is irrelevant since the substrate is in fact an insulator (glass or plastic).

2. **Circuit design and simulation:** Due to unavailability of stable, and reproducible, p-type TFTs, the circuit design must be confined to only n-type enhancement TFTs. In fact, for the case of high-gain amplifiers, depletion TFT loads would make the design simpler and straight forward. However, fabrication of enhancement and depletion TFT types, on the same chip, demands at least one more mask than with a single type TFT. Thus, by overcoming the design challenges with enhancement TFTs, low-cost circuits can be accomplished. Circuit design was started with fundamental blocks, namely, various types of current mirrors, source follower (buffer), single stage common-source amplifier, differential amplifiers, and amplifiers with various kinds of loads (passive, diode connected transistors and bootstrapping). A single TFT application in a half-wave rectifier and peak detector is also reported. Along with the above, basic signal processing circuits, such as, adder, subtractor, multipliers and individual elements were also fabricated on a single chip. Later, a high-gain comparator was developed. Finally a four-bit folding analog to digital converter (ADC) with resistive interpolation was developed, taking into account the limitations and constraints of the technology. This ADC uses two-bit fine and coarse flash converters, folding blocks and source followers. Such topology tends to be less complex, with conversion speeds close to the flash type converter, which is important given the limited bandwidth, natural for devices with low mobility. The digital decoding logic in the ADC is also completely implemented with n-type enhancement a-GIZO TFTs. This is the first ADC with a-GIZO TFT technology. All the above mentioned circuits simulation were carried out with the MLP Verilog-A model.

3. **Library development:** An embodiment framework is needed to facilitate IC design. Technology files should be developed to enable the use of IC-CAD software tools for a flexible and accurate layout design, with design verification. Development of device libraries for layout drawing, design rule check (DRC), and layout versus schematic (LVS) in cadence tools is carried out within a team work. The use of technology libraries mainly comes into picture for complex error-free circuit design.

4. **Circuit fabrication and validation:** Finally, circuit simulation outcomes are validated with fabricated circuit response to verify the ability of the device models to predict its real behaviour. The measured or simulated circuit response also demonstrates that a-GIZO TFTs are possible candidates for complex circuit design and also validates the proposed circuits. For complex circuits, chips have been diced in order to obtain individual blocks that were wire-bonded to PCBs for testing.

1.2 Contribution

This work proposes and validates an accurate compact behavioral model for a-GIZO TFTs based on equivalent circuit approach using neural networks. By using this model, various analog and mixed signal building blocks such as current mirrors, traditional and novel amplifiers, adders, subtractor, multipliers, logic gates, comparator and ADC were designed, simulated and characterized. The proposed single-stage amplifier has accomplished the highest gain ($> 34\,$dB), up to the date, with a-GIZO TFT technology. From simulations, a comparator is promising a gain of 55 dB and bandwidth more than 25 kHz, while the folding ADC presents -0.26 LSB DNL, 0.31 LSB INL and 24 mW power consumption. To the authors knowledge, these are the first comparator and ADC also done in a-GIZO technology.

1.3 publications

1.3.1 Journals

1. P. Bahubalindruni, V. Tavares, P. Barquinha, C. Duarte, P. de Oliveira, R. Martins, and E. Fortunato, "Transparent Current Mirrors With a-GIZO TFTs: Neural Modeling, Simulation and Fabrication," IEEE J. Display Tech., vol. 9, pp. 1001-1006, 2013.

2. P. Bahubalindruni, V. Tavares, P. Barquinha, C. Duarte, N. Cardoso, P. de Oliveira, R. Martins, and E. Fortunato, "a-GIZO TFT Neural Modeling, Circuit Simulation and Validation" (accepted - J. of Solid State Electronics).

3. P. Bahubalindruni, B. Silva, V. Tavares, P. Barquinha, N. Cardoso, P. de Oliveira, R. Martins, and E. Fortunato, "Analog circuits using a-GIZO TFTs" (Revision submitted to IEEE J. Display Tech).

4. P. Bahubalindruni, V. Tavares, P. Barquinha, N. Cardoso, J. Borme, P. de Oliveira, R. Martins, and E. Fortunato, A Compact model for Amorphous Gallium Indium Zinc Oxide Thin-Film-Transistor Using Artificial Neural Networks" (Submitted to Electron Device Letters)

1.3.2 International Conferences

1. P. Bahubalindruni, V. Tavares, P. Barquinha, J. Borme, N. Cardoso, R. Martins, E. Fortunato, P. Oliveira, "IGZO TFT Based Circuits: Logic Gates, Peak Detector and Switch," ISCAS 2015 (submitted).

2. P. Bahubalindruni, V. Tavares, P. Barquinha, J. Borme, N. Cardoso, R. Martins, E. Fortunato, P. Oliveira, "Fundamental Analog Circuits on Glass with a-IGZO TFTs," ISCAS 2015 (submitted).

3. P. Bahubalindruni, V. Tavares, C. Duarte, N. Cardoso, P. Oliveira, P. Barquinha, R. Martins, and E. Fortunato, "Transparent Current Mirrors Using a-GIZO TFTs: Simulation with RBF Models and Fabrication". In Proceedings of the UKSim. pp. 582-586, 2014.

4. P. Bahubalindruni, B. Silva, V. Tavares, P. Barquinha, N. Cardoso, P. Oliveira, R. Martins, E. Fortunato, "Basic Analog Circuits Using a-GIZO TFTs: Simulation Using Neural Models and Validation," ITC 2014 (Poster).

5. Bahubalindruni, P.; Grade Tavares, V.; Barquinha, P.; Martins, R.; Fortunato, E., "High-gain topologies for transparent electronics," EUROCON, pp.2041-2046, 1-4 July 2013

6. Bahubalindruni, P.; Grade Tavares, V.; Guedes de Oliveira, P.; Barquinha, P.; Martins, R.; Fortunato, E., "High-gain amplifier with n-type transistors," International Conference of Electron Devices and Solid-State Circuits (EDSSC), pp.1-2, 3-5 June 2013

7. Bahubalindruni, G.; Duarte, C.; Tavares, V.G.; Barquinha, P.; Martins, R.; Fortunato, E.; de Oliveira, P.G., "Multipliers with transparent a-GIZO TFTs using a neural model," Telecommunications Forum (TELFOR), 2012 20th , pp.955-958, 20-22 Nov. 2012

8. Bahubalindruni, G.; Tavares, V.G.; Barquinha, P.; Duarte, C.; Martins, R.; Fortunato, E.; de Oliveira, P.G., "Basic analog circuits with a-GIZO thin-film transistors: Modeling and simulation," International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), 2012 , pp.261-264, 19-21 Sept. 2012

1.3.3 Other Publications

1. P. Bahubalindruni, V. Tavares, P. Barquinha, P. Oliveira, R. Martins, E. Fortunato, "Analog/Mixed Signal Circuits using a-GIZO TFTs" DATE PhD forum, 2014.

2. Bruno Silva, Pydi Ganga Bahubalindruni, Vitor Grade Tavares, Pedro Barquinha, Rodrigo Martins, Elvira Fortunato, and Pedro Guedes de Oliveira ,A Study of High-Gain Amplifiers for TTFTs in 2nd PhD Student Conference in Electrical and Computer Engineering (StudECE'2013), pp.1-2, 2013

3. Ganga Bahubalindruni, Vtor Grade Tavares, Pedro Barquinha, Cndido Duarte, Rodrigo Martins, Elvira Fortunato, Pedro Guedes de Oliveira ,Circuits for Analog Signal Conditioning with a-GIZO Transparent TFTs in 1st PhD Student Conference in Electrical and Computer Engineering (StudECE'2012), pp.36-37, 2012

1.4 Document outline

The remaining of the dissertation is organized as follows.

- Chapter. 2: Introduces a-GIZO TFT technology and characterization, main advantages and challenges imposed for circuit design, fabrication information, device operation and impact of contact resistance.

- Chapter. 3: Illustrates the modeling requirements, benchmark tests and classification of modeling methodologies along with their pros and cons. Then, a-GIZO TFT static model, which is developed from the measured characteristics of the device, is presented, using different types of ANNs, such as, MLP, RBF and LS-SVM. This is followed by a comparison among these methods in terms of accuracy and complexity. In addition, the complete model is developed based on the equivalent circuit approach that can characterize static and dynamic behavior of the device. Finally, the neural based equivalent circuit model is implemented in Verilog-A for circuit simulations. Before applying the modeling method to a-GIZO TFT, it is experimented with the MOSFET to validate the modeling approach, whose data was obtained from BSIM3V3 model.

- Chapter. 4 : Characterizes the basic analog/digital building blocks, namely different types of current mirrors, buffer, logic gates, single-stage amplifiers (common-source, differential, bootstrapping, with positive feedback load) and cascade amplifiers, only with n-type enhancement transistors. A single TFT application in half-wave rectifier and peak detector is also characterized. The novel single-stage high-gain amplifier topologies are demonstrated. Analog signal processing circuits, such as, traditional and novel adders, subtractor, multipliers are explained. Novel high-impedance load to accomplish high-gain is presented.

- Chapter. 5 : This chapter is dedicated to the mixed signal circuits. First a high-gain comparator is presented, where the bias stress is compensated to some extent. Finally a four-bit folding ADC is also demonstrated.

- Chapter. 6 : This chapter is devoted to the conclusions from the PhD work and the possible future work in terms of modeling and circuit design with a-GIZO TFTs.

Chapter 2

a-GIZO Technology: What it is and what are its Challenges

This chapter presents a brief description of the thin film transistor (TFT) technologies, focused on amorphous gallium indium zinc oxide (a-GIZO) materials, in the context of display panel applications, which has been the main driving engine for worldwide research in the area. Well known TFT device structures and device fabrication information, of actual devices used along this work, will also be object of analysis, in addition to the impact of materials on the device performance. This is followed by a description of TFT operation, using a real fabricated TFT as a basis. Finally, different layouts of transistors are discussed.

2.1 Thin-Film Transistors Technologies

TFT technologies have emerged into a huge industry, dedicated mainly for display applications. Since the beginning days that the common choice for TFT material was the hydrogenated amorphous silicon (a-Si:H). This technology was (and still is) devoted principally for active elements of liquid crystal display (LCD) or organic light emitting diode (OLED) active matrix backplanes. However, a-Si:H TFT devices present a relevant threshold-voltage (V_{TH}) variation, low carrier mobility (μ) and non-transparency in visible spectrum. For these devices, V_{TH} variation takes place not only during the gate-bias stress but also in off-state bias [38]. Here, the gate-bias stress refers to the variation in the V_{TH}, with continuous application of gate voltage (V_{GS}) that consequently changes the electrical characteristics of the device. The bias stress is not a critical issue in case of LCD drivers, as the gate voltage is applied only for a small fraction of time. But in OLED displays, the driver TFT contained in the pixel circuitry needs to drive a specific current and keep it on as long as the pixel is emitting light. In this case V_{TH} shift becomes a critical issue, as it will affect the current being supplied to the OLED, changing its brightness [16]. Nevertheless, the design of pixel circuits can be compensated for some of the threshold shifting at the expense of more TFTs per pixel [16]. Low temperature poly-silicon (LTPS) is an alternative option. The fabrication temperature is around 600°C, which being slightly lower than the melting temperature of glass,

naturally establishes this technology as a possible candidate for display applications. Moreover, LTPS TFTs are less prone to bias stress, present higher electrical mobility and also complementary type devices are possible (which are not yet stable in other TFT technologies). In spite of these advantages, LTPS TFTs are not able to easily replace a-Si:H TFTs in displays due to higher manufacturing cost (as it requires more processing steps and masks than a-Si:H TFTs) and lack of uniformity in large areas, as a consequence of the polycrystalline structure of the semiconductor material. Notwithstanding, many research groups still continue working towards obtaining devices with better electrical characteristics, to ensure large-area electronics with better uniformity, either by means of finding new materials, processing steps or different device structures, while keeping fabrication costs low. In this process, other TFT technologies have emerged, mainly focused on organic and metal-oxide semiconductors. Organic semiconductor based (O)TFTs, despite exhibiting great potential for flexible and large area electronics, have shown poor mobility. On the contrary, TFTs based on the conventional metal-oxides (i.e., binary compounds) such as Zinc oxide (ZnO) have shown relatively higher mobility, in some cases even exceeding 20 $cm^2/V{\cdot}s$ with room-temperature processing [39]. However, as with LTPS, ZnO and other well known binary compounds such as Indium oxide (In_2O_3) and Tin oxide (SnO_2) are polycrystalline, limiting large area fabrication. Furthermore, depending on grain size and doping level, grain boundaries can significantly affect device performance/stability by trapping free carriers [38]. These difficulties can be overcome by using multicomponent oxides, i.e., materials combining different cations of post-transition metals with electronic configuration $(n\text{-}1)d^{10}\ ns^2$, where $ns \geq 4$ [17]. In this case, given the structural disorder imposed by mixing different cations, amorphous structures are obtained. Still, contrarily to covalent semiconductors like Si, the increased disorder does not lead to a significant degradation of electrical performance, since the conduction band of these multicomponent oxides is primarily derived from spherically symmetric and large radii 4s or 5s orbitals. This results in overlap of adjacent orbitals, hence to the formation of a conduction path to free carriers, regardless of the degree of disorder. In such a case, mobilities in the range of 10-50 $cm^2/V{\cdot}s$ are possible, even with processing temperatures below 200°C [40]. One of the most successful multicomponent oxides studied to date has been amorphous Gallium-Indium-Zinc oxide (a-GIZO). Despite having in its composition two cations identified by the European Comission as critical raw materials (In and Ga), compared with other multicomponent oxides such as Zinc-Tin oxide (ZTO), a-GIZO allows for higher mobility at lower processing temperatures [40].

As Table 2.1 summarizes, when compared to CMOS, except for LTPS, all TFT technologies present orders of magnitude less mobility, and also much higher feature sizes. But one should understand that for specific application areas that demand flexible and or transparent and large-area electronics, at very low-cost, or even for generic low-frequency applications, TFTs are highly competitive.

2.1.1 a-GIZO TFTs as the Next Mainstream TFT technology

Room temperature fabrication of TFTs, using a-GIZO as a semiconductor layer, was introduced in 2004 [17]. Since then, intensive research was conducted to obtain devices with improved per-

Table 2.1: Comparison of the main TFT technologies with CMOS

Technology	Feature size	Polarity	Mobility ($cm^2/V \cdot s$)	Semiconductor fabrication process	Process temperature	Substrate	Supply voltage (V)*	Transparency to visible light	Ref.
CMOS	32/22 nm	p-type, n-type	1500	Chemical vapor deposition (CVD)-based epitaxial growth	1000°C	Si wafer	1	Opaque	[41]
LTPS	3 μm	p-type, n-type	>100	Low-pressure chemical vapor deposition (LPCVD)	600°C	Glass	9	Opaque	[42], [43]
a-Si:H TFT	8 μm	n-type	0.1–1	Plasma enhanced chemical vapor deposition (PECVD)	250°C	Glass or Plastic	20	Opaque	[41]
OTFT	5 μm	p-type	0.1–1	Evaporation, spin-coating, inkjet	150°C	Glass or Plastic	15	25-30%	[28]
a-GIZO TFT	6 μm	n-type	10–50	Sputtering, spin-coating, inkjet	150°C	Glass or Plastic	5	86%	[18], [30]

* Highly dependent on the capacitance of dielectric layer

formance/stability and reduced processing temperatures, mostly targeting its application in the active matrix backplanes of next generation LCD and OLED displays. The semiconductor oxide (a-GIZO) is amorphous in nature. Its high spatial uniformity over large areas, together with its compliance with low-cost and low-temperature manufacturing methods such as sputtering and spin-coating [41] are the main ingredients that foster the commitment of research groups and companies towards this technology. In effect, commercial products including this TFT technology are already available in the market, such as Sharp's AMLCD smartphone [44] or LG's 55" OLED display [45].

Transparency, Flexibility and Mobility

Neither LTPS nor a-Si:H TFTs are transparent at visible spectrum, and organic semiconductors, although transparent, exhibit an optical transparency that falls between 25% and 30% [46]. These are not the perfect choice for high-demanding transparent applications, as in see-through active matrix displays, where good optical transparency is required. In contrast, visible light can penetrate through the a-GIZO material up to 86% [41]. Consequently, TFTs or circuits based on this material will appear to be almost totally transparent if the source/drain materials are also transparent conductive oxides (TCOs),e.g.: Indium Zinc oxide (IZO) or indium tin oxide (ITO).

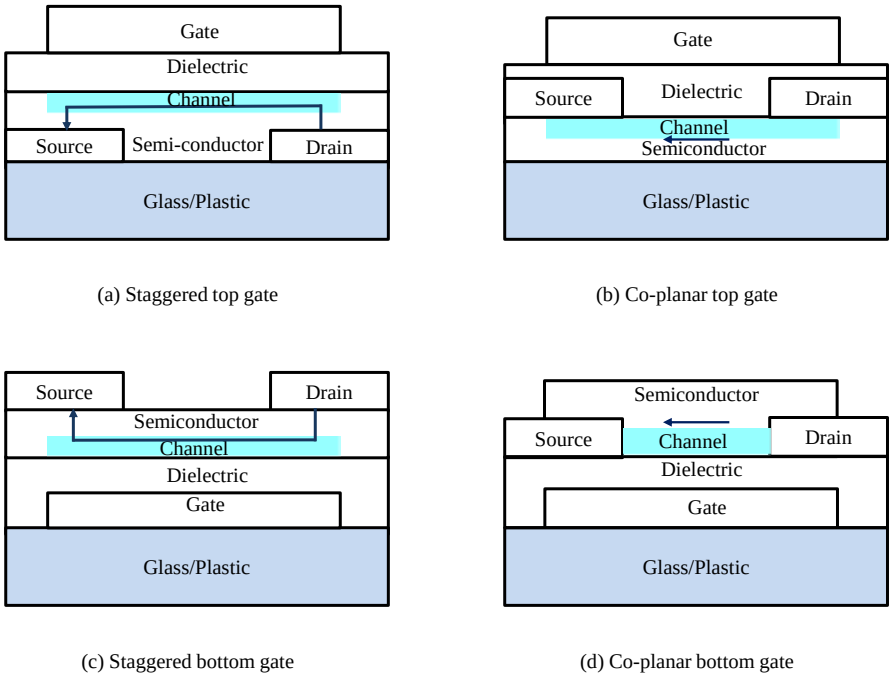
The realization of flexible electronics is another motivating factor in favor of a-GIZO TFT technology. The fabrication and annealing temperatures are low, as seen in Table. 2.1. Such low temperatures opens the ground for a panoply of different types of substrates, namely glass, paper and plastic. Glass substrate is not an option for light-weight, rollable, bendable or foldable

displays, since glass is fragile and relatively heavy. In addition, future roll-to-roll fabrication processes demand flexible substrates. a-GIZO TFT technology with plastic substrate can make most of the referred applications a reality. It is worth noting that other TFT technologies, such as, a-Si:H and OTFT can also accomplish flexible electronics but their performance is limited due to lower charge-carrier mobility (μ). On the other hand, chemical bonding in amorphous oxide semiconductor (AOS) is ionic, as opposed to covalent bonding in a-Si:H. As explained before, this brings to a-GIZO unique carrier transport properties, despite its amorphous structure [17]. Note that high mobility of a TFT technology is a critical demand for the next generation displays: even considering LCDs, where TFT specifications are considerably more relaxed than for OLED displays, higher resolutions and higher refresh rates result in reduced row/column addressing times, demanding higher speed transistors. Hence, next generation 4k and 8k displays will require switching TFTs with μ >15-20 $cm^2/V{\cdot}s$. Moreover, this level of TFT performance allows to integrate some of the drivers (particulary the gate ones) in the display backplane, resulting in yield improvement and reduction of overall production costs. All this constitutes a great market opportunity for a-GIZO TFTs.

2.2 TFT Device Structures

TFT device structures are classified according to the relative position of the gate and source/drain contacts with respect to the semiconductor layer. If all the three contacts are laid on a single plane then the device structure is known as coplanar. Alternatively, if the gate and source/drain contacts lie on opposite planes, with respect to the semiconductor layer, then the device structure is known as staggered. The TFT device structures are further classified as either top-gate or bottom-gate, depending on the relative position of gate contact. The four described structures are shown in Fig. 2.1, namely, staggered top-gate, coplanar top-gate, staggered bottom-gate and coplanar bottom-gate. Generally, coplanar structures are used for poly-silicon TFT and crystalline silicon field effect transistors (CMOS) [19]. In case of top-gate TFT structures, the gate electrode and dielectric act as passivation to the semiconductor channel, thus protecting the channel from reacting with the ambient. Bottom-gate staggered structured TFTs need an external passivation layer to grant such protection. This structure has been the preferred layout design for display driving circuits in the backplane, and being the display industry the mainstream for this technology, it is also adopted in the present work.

It should be stressed at this point that the definition of new structures for the devices is not yet a closed issue because of its impact on performance. Any gain is important considering the inherent limitations of these technologies, and not surprisingly then, efforts are still ongoing to find different structures that may improve electrical performances and reliability. A top-gate self aligned structure [35] and a new structure [47] with ”I” shaped gate layer that minimizes the parasitic capacitance have been demonstrated. Such accomplishment can be very useful for the design of fast circuits. A multi-channel structure, with spacing between the sub-channels to improve the bias stability has also been reported [48].



(a) Staggered top gate

(b) Co-planar top gate

(c) Staggered bottom gate

(d) Co-planar bottom gate

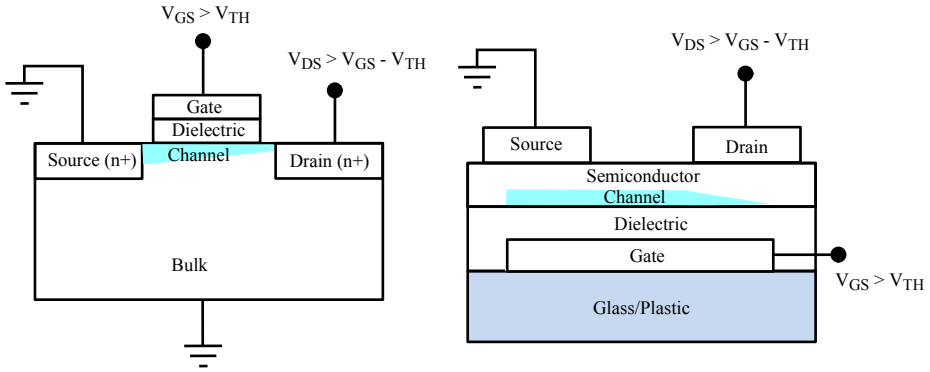
Figure 2.1: Four possible TFT structures: solid line with arrow shows the current flow direction

2.3 TFT Operation and Electrical Characterization

Despite metal oxide semiconductor field effect transistor (MOSFET) and a-GIZO TFT being structurally different from each other, as shown in Fig. 2.2, both behave as field-effect transistors. In either case, the drain current is controlled by the bias voltages (V_{GS} and V_{DS}). For long channel, bulk based, CMOS transistors, generally V_{TH} corresponds to the V_{GS} value at which the charge carrier concentration, on the created inversion layer underneath the gate, equals to the bulk. From this value on it is said that a moderate to strong inversion channel is formed between the source and drain terminals in the bulk. However, for TFTs, the source and drain electrodes are not deposited in the bulk unlike MOSFETs, as shown in Fig. 2.2b. Besides, bulk is a pure insulator for the devices in this work. Subsequently, no inversion takes place in the channel. For TFTs, the term turn-on voltage (V_{ON}) is more generally used, which corresponds to the V_{GS} value at which there is a significant increase in the drain current (I_D), as seen in a semi-log I_D-V_{GS} plot. Fig. 2.3 demonstrates V_{ON} of the devices in this work, which is very close to 0 V, for a transistor whose width (W) is 40 μm and length (L) is 20 μm, where V_{GS} varies from 0 to 10 V at a drain voltage (V_{DS}) 14 V. As the positive V_{GS} increases, more free charge-carriers (electrons) are attracted towards the gate side and accumulated near the semiconductor-dielectric interface, forming a conductive channel between the source and drain electrodes. A channel is then created through accumulation and not by inversion. In such case, V_{TH} is the V_{GS} value that results from extending the best line fit to a Sqrt(I_D)–V_{GS} plot (in saturation regime) until I_D is zero, as shown in Fig. 2.4 for the same

device. If V_{TH} is positive, then the TFT is treated as enhancement type, if negative, it is considered to be of depletion type. Apart from V_{ON} and V_{TH}, on-off current ratio and sub-threshold swing (S) are also important performance metrics for a TFT. The on-off ratio is simply the ratio of the maximum on-state current to the off-state current, as shown in Fig. 2.3. This is a very important parameter defining the efficient discrimination between *on* and *off* states in switching applications. S is given by (2.1), which for the current device it is found to be 0.20 V/dec. S essentially defines the efficiency of gate switching, i.e., how much V_{GS} is required to increase I_D for one decade, being highly dependent on the dielectric layer and its interface quality with the semiconductor.

$$S = \left(\frac{dlog(I_D)}{dV_G} \right)^{-1}_{max} \tag{2.1}$$



(a) N-channel MOSTFT (b) TFT with bottom gate staggered structure

Figure 2.2: Structural difference between MOSFET and a-GIZO bottom gate staggered TFT. Schematic shows device operation in saturation regime.

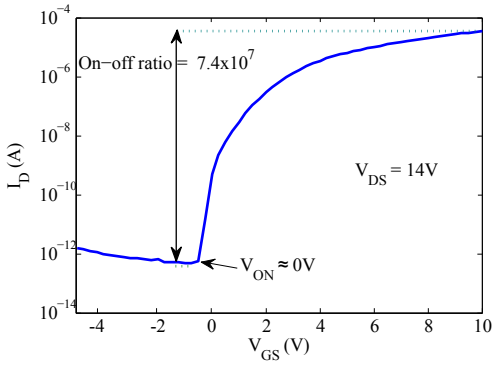
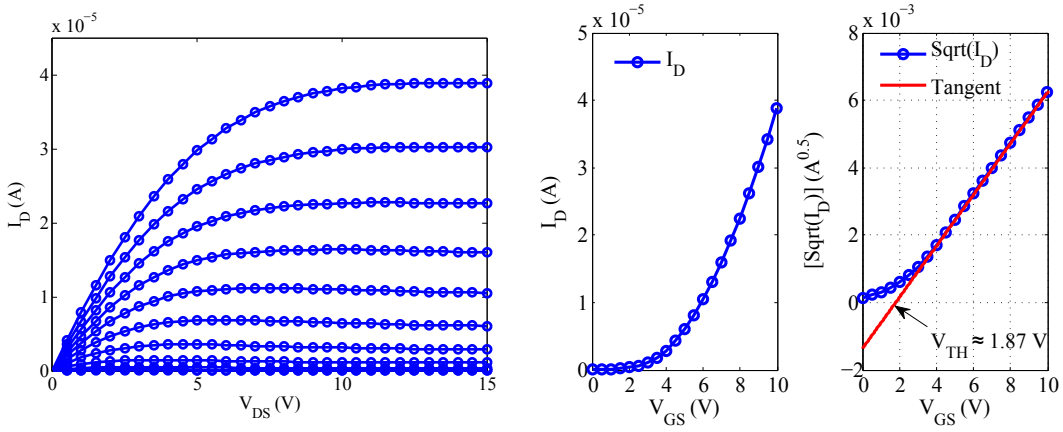


Figure 2.3: Transfer characteristics of a-GIZO staggered bottom gate TFT with W = 40 μm and L = 20 μm.

As far as literature goes, and to the best of our knowledge, the complete device physics for carrier transportation mechanisms is not yet clearly understood. Finding accurate physical relationships between the electrical variables is still a very hot-topic. But since a-GIZO TFT is a field effect transistor, Level-1 MOSFET model is often used, though giving a very crude approximation.



(a) Output characteristics : for V_{GS} : 0 to 10 V in steps of 1 V and V_{DS} : 0 to 15 V in steps of 0.5 V

(b) Threshold voltage calculation from Sqrt(I_D) in deep saturation regime: V_{DS} : 14 V and V_{GS} : 0 to 10 V in steps of 0.5 V

Figure 2.4: Electrical characteristics of the TFTs for W = 40 μm and L = 20 μm

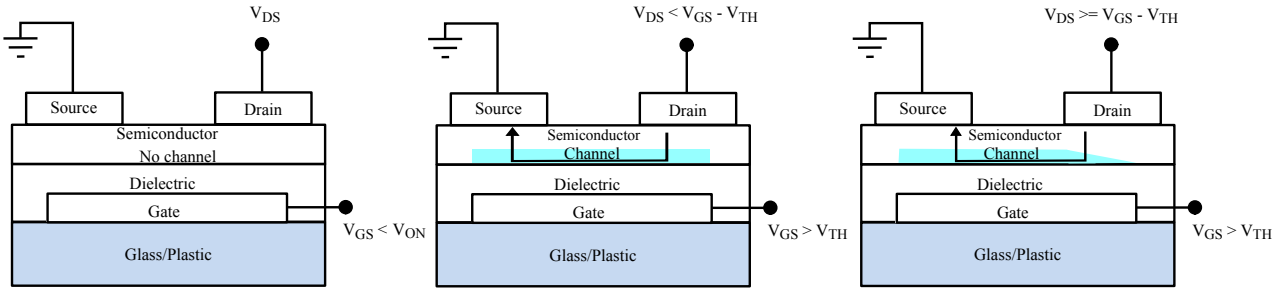
In fact, MOSFET models cannot predict the a-GIZO TFT behavior to a good accuracy, because MOSFET employs crystalline silicon, inversion layers and p-n junctions, all these are absent in a-GIZO TFTs. Similarly, a-Si:H TFT models are also incapable of anticipating the a-GIZO TFT electrical behavior, although being amorphous in nature. This is because of the distinctive property of the amorphous semiconductor oxides, where the localized charge carriers are less than the free charge carriers, unlike a-Si:H TFT [38, 31].

Enhancement n-type TFT operation in different regimes is depicted in Fig. 2.5. When V_{GS} is lower than V_{ON}, there is no channel in the semiconductor and hence no current can flow in the device, then the device is said to be in cut-off. When $V_{ON} < V_{GS} < V_{TH}$, a very-low concentration accumulation-channel is formed. Very small sub-threshold current is present and the device is said to be in the sub-threshold regime of operation (since charge density in this region is still very small, it is not shown in the picture). As V_{GS} increases above V_{TH}, a conductive channel is formed with enough charge concentration for current to flow. Positive V_{DS} drifts a flow of charge carriers towards the drain electrode. A current flow I_D is then detected in the opposite direction to the flow of charge carriers i.e., from drain to source. When $V_{DS} < V_{GS}$ - V_{TH} the device is said to be in the linear region of operation and there is an almost uniform conductive channel near the dielectric and semiconductor interface as shown in Fig. 2.5b. On the other hand, when $V_{DS} \geq V_{GS}$ - V_{TH}, then the channel is pinched-off near the drain electrode due to a weaker vertical electric-field ($V_{GD} < V_{TH}$) and the device is said to be in the saturation region, as shown in Fig. 2.5c. As per the Level-1 MOSFET model, the drain current in saturation region can be approximated as follows,

$$I_D = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2, \tag{2.2}$$

where μ_n is the mobility of the device and c_{ox} is the capacitance due to dielectric. Since the

mobility of the a-GIZO TFT is much smaller than the crystalline silicon, the drain current is also significantly lower in a-GIZO TFT for the same relative size and voltages.



(a) Cut-off (b) Linear (c) Saturation

Figure 2.5: TFT operation in different regimes

2.3.1 Parasitic Resistors and Capacitors

Before reaching the channel, charges drifting through the TFT under external excitation travel along resistive paths and potential barriers that negatively affect the device performance, namely μ and V_{TH}. The series resistance results from the source/drain metal, the semiconductor contact resistance (R_C) and the resistance of the intrinsic semiconductor (R_I) between the source/drain metal and the conductive channel near the semiconductor-dielectric interface [49, 50]. This amounts to a total drain and source resistance:

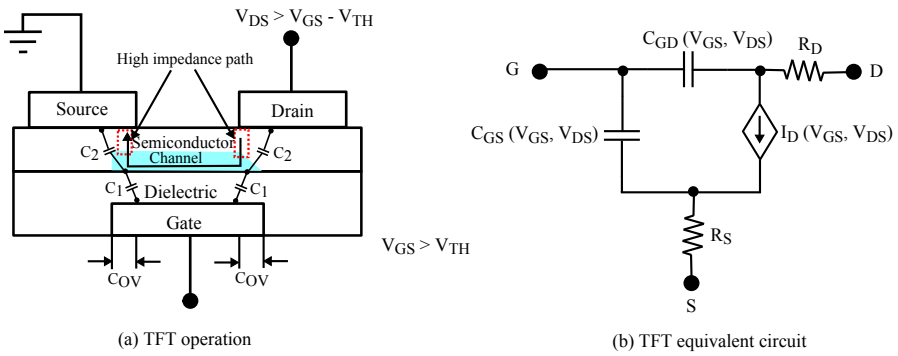
$$R_C + R_I = R_S + R_D, \tag{2.3}$$

here R_S and R_D represent lumped series resistances at source and drain terminals respectively. In particular for bottom-gate staggered layouts, the charge carriers have to travel through R_I, which is an high impedance path where part of the bias voltages are dropped, as shown in Fig. 2.6a. Consequently, less current results in the TFT and accordingly the effective mobility is also reduced by the series resistance of the device.

Constructive constrains during fabrication, like mask alignment limitations, require minimum overlapping areas between specific layers, in particular at the source/drain and gate regions to eliminate any possibility of having ”gaps” between the formed channel and drain/source electrode; otherwise any misalignments would greatly increase R_I, which would severely hinder the transistor performance. Such need directly influences the total overlap capacitance (C_{OV}) that will materialize between those overlapping areas. The capacitor C_{OV} is in fact a result of the series combination of C_1 and C_2 as shown in Fig. 2.6a, where C_1 is due to the gate-dielectric-semiconductor and C_2 is due to the channel-intrinsic semiconductor-source/drain metal.

Finally, a large-signal equivalent circuit for the TFT can be foreseen as shown in Fig. 2.6b by taking into account the different components discussed above. As referred earlier, unlike the CMOS, the bulk is a pure insulator in the current TFT devices, so any parasitic components related

to the bulk are perfectly negligible, specially because these are low-frequency operation devices. This results in a much simpler equivalent circuit when compared to the regular MOSFET.



(a) TFT operation (b) TFT equivalent circuit

Figure 2.6: TFT equivalent circuit

2.3.2 Channel Length Modulation

In an ideal case, (2.2) gives the drain current of the device in saturation, which is completely independent of the V_{DS}. Nevertheless, in practice, the drain current varies with respect to the V_{DS}, which can be seen as a finite output resistance (r_{ds}), as shown in Fig. 2.7. Since the channel gets pinched off in saturation, the effective channel length is smaller than the actual channel geometric length, and contributes to raise the drain current. This effect can be approximated by,

$$I_D = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS}), \tag{2.4}$$

where λ is the channel length modulation parameter and $\lambda \propto \frac{1}{L}$. For short channel devices, channel length-modulation effect is then more predominant.

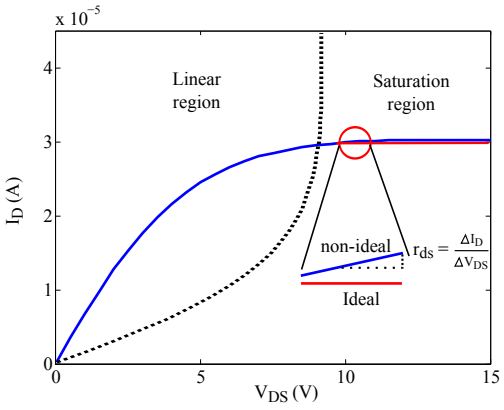


Figure 2.7: Channel length modulation

2.3.3 On-Resistance

The *on* resistance (R_{ON}) is a very important metric, especially when the device is used for switching applications, where R_{ON} should be ideally zero. For switching, the TFT will operate either cut-off or in the linear (or triode) region (with very small V_{DS}), in which case, the drain current is approximately given by the following expression,

$$I_D = \mu_n c_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS} \tag{2.5}$$

and R_{ON} is given by,

$$R_{ON} = \frac{V_{DS}}{I_D} = \frac{L}{\mu_n c_{ox} W(V_{GS} - V_{TH})}. \tag{2.6}$$

In order to get a low R_{ON}, wider device with small length and $V_{GS} >> V_{TH}$ should be used at very low V_{DS}. Furthermore, the mobility should also be as high as possible.

2.4 Challenges for Circuit Design

The challenges that an emerging technology poses begin with inventing suitable materials for conductors (source/drain and other electrodes), semiconductor and insulator (dielectric) for the device. All materials should be selected in such a way that the devices encompass very low hysteresis and instability [51]. The very next challenge is the fabrication of near-ideal devices; for example, devices with smaller dimensions and minimal or no source/drain overlaps, which are essential for faster applications. This aspect is out of the scope of this dissertation, however many other technological limitations also need to be addressed during circuit design in specific. The main challenges are the lack of stable and reproducible complementary device (p-type transistor), poor mobility compared to crystalline silicon and gate bias stress susceptibility. Proper designing tools strictly dedicated for circuits with a-GIZO, or TFTs in general, are also absent or at least not widely spread. The nonexistence of accurate device models and technology libraries that support layout drawing tools, design rule check (DRC) and layout versus schematic (LVS) comparison for this specific technology, in order to ensure error free layout designs, is a big handicap that prevents a smooth development of integrated circuits, being normally present in a typical design flow. All of these factors make the design of analog/mixed circuits very challenging, and certainly it is also part of the reason why the applications are mostly confined to sensors, displays and simple peripheral circuits; although, very recently some simple analog circuits have been reported [20, 30].

2.4.1 Design Flow

The basic steps involved in analog IC, full-custom, design are depicted in Fig. 2.8. As a first step, circuit design should be carried out, once the specifications are described. Then the circuit schematics should be simulated to verify its functionality. If the simulation results are not meeting the requirements, the circuit should be redesigned until the results are in agreement with the

specifications. Accurate compact device models are essential for the success of this step, and for higher yield under production, corner and Monte-Carlo analysis should also be carried out at this phase.

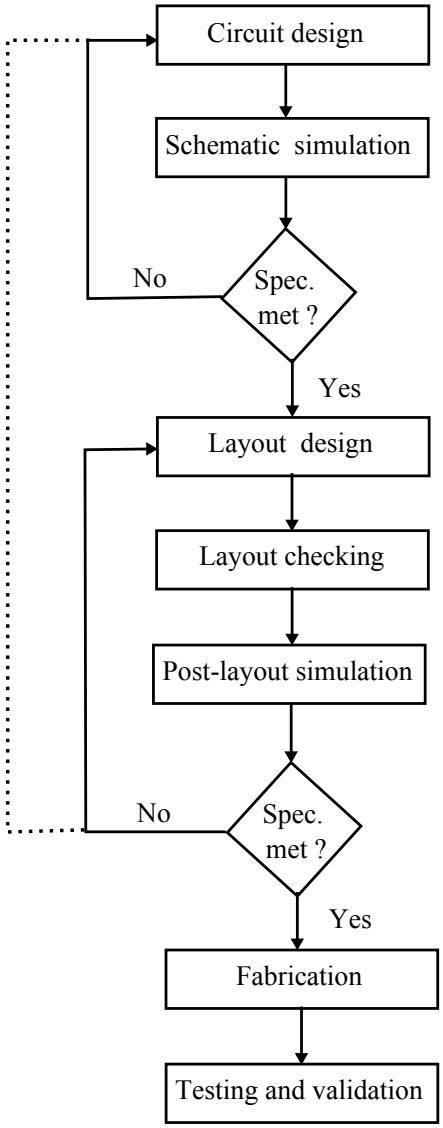


Figure 2.8: Analog design basic steps

Once the simulation results are in agreement with the desired specifications, circuit layout should be designed and then subjected to DRC and LVS checking. DRC determines whether the circuit layout satisfies a series of ”design rules” for a specific semiconductor technology. The design rules refer to a specific set of geometric restrictions that ensure adequate margins for mask alignment between the different layers of materials. Generally it also takes into consideration the variations of the fabrication processes and mask generation, preventing abnormal short- or open-circuits and device defects as a result of known systematic and random errors that are generated during production. Successful DRC can just grant that the layout can be fabricated because it is

conformal with a set of geometric rules defined by specific semiconductor technology provider, however it does not guarantee if the layout corresponds to the desired circuit. At this stage, LVS checks is mandatory to realize if the circuit schematic and the designed layout are matching each other. Once the DRC and LVS checks are done, post-layout simulations should be carried out to confirm whether the designed layout is promising the desired response even after including all the parasitics associated with the interconnections. With successful post-layout simulations, the layout is ready for fabrication, which is followed by testing in order to validate the circuit design. These are fundamental steps to accomplish what is generally coined as "first time right" design. Every step is extremely important to assure a successful working circuit after fabrication, but probably the most important item in all is the device model accuracy. For a-GIZO TFT in particular, there is no built-in platform that can support the basic steps shown in Fig. 2.8. There are no commercial device models that can be used for circuit simulations. In addition, the non-existence of the technology libraries make the circuit design quite challenging.

2.4.2 Hindrances in the Design of Analog Circuits

Even though a-GIZO TFT mobility is superior compared to the other TFT technologies, such as a-Si:H and OTFT (see Table. 2.1), it has a much inferior electrical mobility (orders of magnitude) when compared to the crystalline silicon. Taking the transconductance (signal level) of the transistor, given by

$$\left.\frac{\mathrm{d}i_D}{\mathrm{d}v_{GS}}\right|_{@\text{bias}} = \mu_n c_{ox} W/L(V_{GS} - V_{TH}) \tag{2.7}$$

it immediately stands that the transconductance term $g_m = \mu_n c_{ox} W/L(V_{GS} - V_{TH})$ is strongly limited by the poor mobility, which inevitably conditions the overall gain and imposes strong restrictions when designing high-gain topologies.

Interestingly, the path that the present state of the oxide TFT technology is taking is, in many aspects, similar to the IC silicon MOSFETs in the early days. Now, as then, the p-type transistor is not keeping up with its n-type counterpart. Forming p-type oxide semiconductors [52, 53] is showing to be very difficult to accomplish, and those reported present a very poor hole-mobility [54]. Copper and tin based semiconductor oxides are gaining evermore supporters as a possible basis for p-type oxide material. However, p-type devices with good electrical characteristics, closer to the n-type presently available, have not yet been reported, at least up to the time of the writing of this document. Such fact determines that oxide semiconductor based TFT technologies are now essentially limited to n-type transistors, using n-type semiconductor materials such as a-GIZO.

High-gain stages are crucial blocks in operational amplifiers, which are well known for their remarkable applications in integrated circuit design, or electronics in general. When a simple common-source (CS) amplifier is considered in CMOS technology, high gain can be obtained by employing a simple-current mirror formed by p-type transistors, acting as an active load for a n-type driver transistor (vice-versa is also possible), as Fig. 2.9 shows.

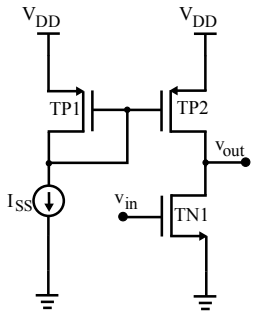


Figure 2.9: Simple common-source amplifier with complementary transistors

The amplifier small signal gain is given by the following expression.

$$A_V = \frac{v_{out}}{v_{in}} = -g_{mn} \times (r_{dsn} // r_{dsp}), \tag{2.8}$$

where g_{mn} is the transconductance of the driver transistors, r_{dsn} and r_{dsp} are the output resistance of the driver and load transistors, respectively. In this case, even a simple single-stage amplifier can provide a reasonably good amount of gain.

When a complementary (p-type) device is not available, a depletion transistor (connecting its source to the gate) is the simpler and straight forward alternative to realize an active load. This topology can also provide a high gain, very similar to that of Fig. 2.9. However, if mixed-signal ICs are considered, then enhancement devices will also be required to guarantee good *on/off* states in logic circuits. Having both enhancement and depletion mode devices on a single chip will imply additional lithographic masks and processing steps than in chips having a single type of device. In addition, negative voltages are required to turn off depletion-mode devices. Hence, although using enhancement-only TFTs results in more design challenges, at an initial development stage this route is preferable to minimize processing time and cost.

2.4.3 Instabilities

Long-term stability and reliability are the most important aspects to have in mind when considering the viability of a given TFT technology for mass production. It is well known that a-Si is an inherently unstable material [55]. Hydrogen has to be incorporated in the amorphous network to compensate dangling bonds and passivate some of the associated trapping states distributed across the bandgap. Even when properly hydrogen passivated, a-Si:H TFTs show significant instability under constant gate voltage of drain current stress [55, 56]. Typically, this is translated in a threshold voltage shift (ΔV_{TH}) due to charge trapping at the insulator and/or its interface with the semiconductor and due to metastable state creation within the semiconductor. In addition, when exposed to visible light a-Si:H properties can be degraded due to the creation of dangling bonds according to the Staebler-Wronski effect, being the initial properties only reestablished after an annealing treatment [57]. Despite all this, a-Si:H TFTs found tremendous commercial success in relatively simple voltage switching applications, such as in active matrix backplanes for liquid

crystal displays (AMLCDs). But when considering more demanding tasks, such as driving TFTs for OLEDs (where the transistor has to supply a constant and stable current to the electroluminescent device) or more generally, analog and/or mixed signal circuits, the inherent instability of a-Si hinders its successful usage.

Besides all the advantages of oxide TFTs already pointed out in this section, they also have the potential to exhibit considerably improved stability over a-Si:H TFTs. In fact, oxide semiconductors in general and a-GIZO in particular are not significantly affected by the dangling bond effects of the distorted a-Si structure, as they are composed of large spherical and isotropic atomic orbitals that can overlap despite the degree of disorder of the films [40]. Despite this, these devices also suffer from reversible ΔV_{TH} under constant positive gate voltage stress, which can be considerably enhanced if good quality insulators and oxide semiconductor compositions and deposition conditions are used, i.e., instability is not attributed to an intrinsic semiconductor material limitation [19]. It is typically found that stability is improved for higher annealing temperatures (200-300°), as this removes weak chemical bonds and improves insulator/semiconductor interface; in addition, dense passivation layers also contribute to achieve stable devices, as the exposed back channel of oxide semiconductors in staggered bottom-gate structures is prone to adsorb/desorb oxygen and water molecules when an electric field is applied [19]. Properly passivated a-GIZO TFTs can exhibit ΔV_{TH} <0.4 V under constant drain current stress during 24 h [58]. Negative-bias stress is reported not to significantly affect the stability of oxide TFTs [19], as it was also confirmed in FCT-UNL's devices.

Up to now, stability tested under dark conditions was mentioned. Nevertheless, given the potential to use oxide TFTs close to the backlight of AMLCDs or even in transparent electronic applications used under typical daylight environments, it is imperative to understand how they behave under illumination. a-GIZO TFTs respond to photon energies above 2.3 eV, which is considerably lower than its bandgap of ≈3.1 eV. Illumination with increased photon energies (i.e., decreased wavelength) increases off-current and induces a negative ΔV_{TH}, which is attributed to the excitation of electrons from deep subgap states to the conduction band [59]. This is further enhanced if both negative bias and illumination stress (NBIS) are combined, constituting the most challenging testing condition for oxide TFTs. In fact, given its crucial importance to define the commercial viability of oxide TFT technology, NBIS effects have been reported in the last years by several groups [52]. Several degradation models have been proposed, including the trapping of photogenerated hole carriers [60], the creation of ionized oxygen vacancies [61] and the photodesorption of oxygen molecules [62]. Even if a full understanding of all the physical mechanisms behind NBIS is still lacking, it was already shown that the formation of a passivation layer and of a high quality semiconductor with low density of states above the valence band is critical to reduce NBIS effects [63, 64].

2.5 Comparison of TFT Layouts

There are different possibilities in what concerns the geometry of transistor layouts. The most common for TFTs are the direct and fingered designs, which will also be considered in this work. Fingered layout basically is a geometric design of a transistor by partitioning it into n devices of size $(W/n)/L$ connected in parallel, as shown in Fig. 2.10 and Fig. 2.11.

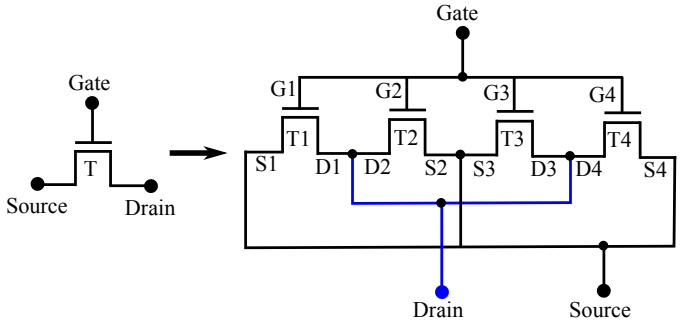


Figure 2.10: Wider TFT equivalent in terms of TFT with smaller widths when the transistors have same length and $W_T = W_{T1} + W_{T2} + W_{T3} + W_{T4}$.

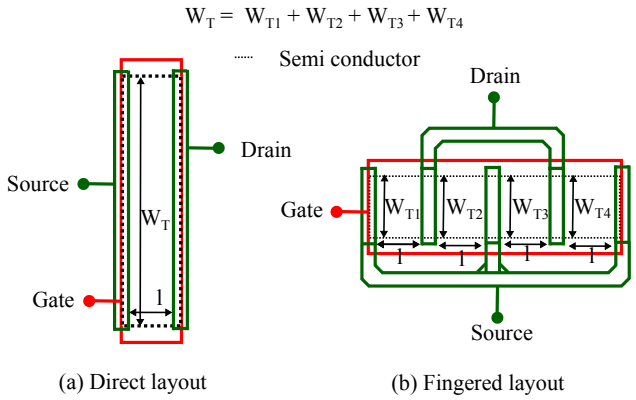
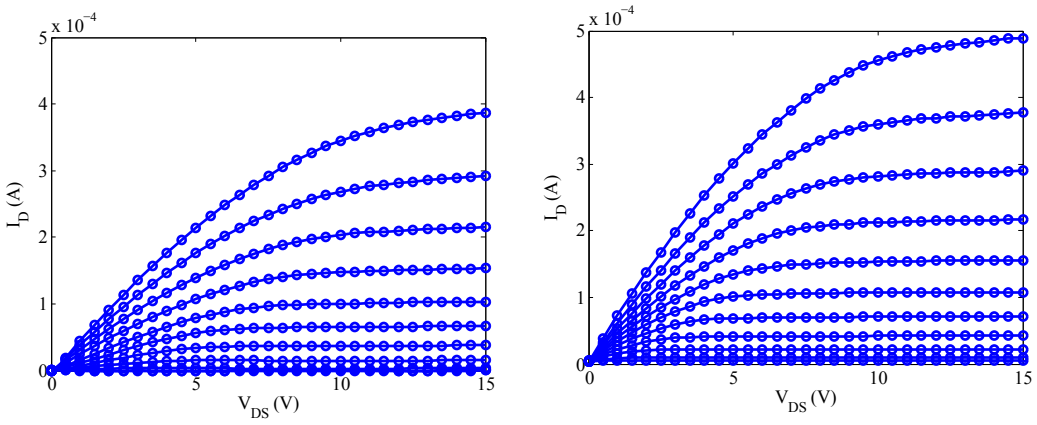


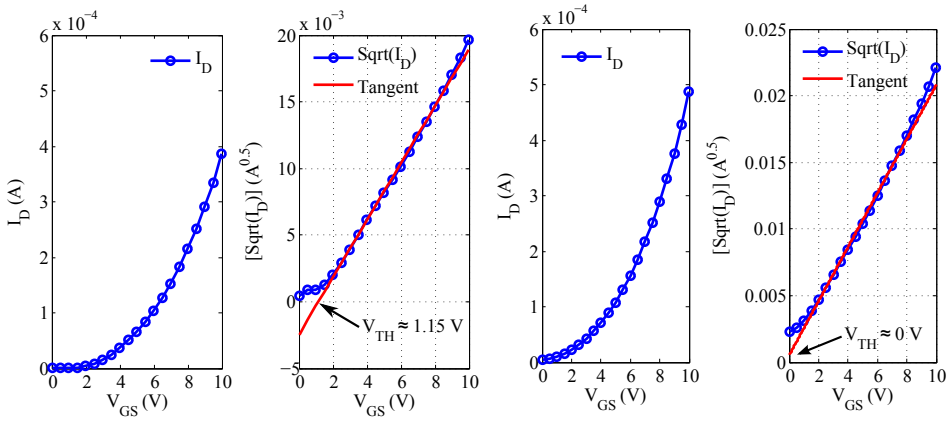
Figure 2.11: Wider TFT direct and fingered layout, when the TFTs have same length.

As referred in section 2.4.2, the electrical mobility of TFTs is very small compared to CMOS technology. In order to design circuits with high-gain it is essential to use wide devices. Considering the staggered bottom gate structure, the inherent overlap (parasitic) capacitance needs to be well regarded in wider devices due to consequent bandwidth limitations. In addition, the contact resistors ($R_{S/D}$), at the source and drain terminals, will come in series with the drain current, consequently part of the applied bias voltages will be dropped in these, which shows impact on circuit performance. In order to circumvent this problem, to some extent, when the transistor width is greater than $40\,\mu$m, fingered layout is then employed to minimize $R_{S/D}$ on each transistor. This will result on a bigger effective V_{GS} and V_{DS} (transistors are in parallel) for the same external bias, when compared to the single full width (direct layout) transistor, and the lower total resistance also results in increased mobility, thereby improving the overall performance of the transistor.



(a) Direct layout (b) Fingered layout

Figure 2.12: Drain current of the TFTs with direct and fingered layouts, where width = 320 μm and length = 20 μm from the same chip; for V_{GS} : 0 to 10 V in steps of 1 V and V_{DS} : 0 to 15 V in steps of 0.5 V



(a) Direct layout (b) Fingered layout

Figure 2.13: Threshold voltages of the TFTs with direct and fingered layouts, where W = 320 μm and L = 20 μm from the same chip; for V_{GS} : 0 to 10 V in steps of 0.5 V and V_{DS} 15 V i.e., under deep saturation.

The output characteristics of TFTs with W = 320 μm and L = 20 μm, for a direct and fingered layout are shown in Fig. 2.12. Since these two devices are from the same chip, they are supposed to have similar electrical characteristics. However, as it can be noticed that the fingered layout TFT exhibits more drain current than that of the direct layout TFT, under the same bias conditions. In addition, the threshold voltage for these two devices is also different as shown in Fig. 2.13. It is clear from Fig. 2.13 that the direct layout TFT behaves as enhancement device, since $V_{TH} > 0$ V, on the other hand fingered layout device characteristics are very close to the depletion type device, since $V_{TH} \approx 0$ V. This in fact is explained by the lower series resistance of the fingered layout when compared to the direct layout, however, it is well known, not only for TFTs, but also

in CMOS that the V_{TH} suffers strong variations along a single die, which may also explain the difference.

2.6 TFT Fabrication Process

This section presents a very brief description of device fabrication techniques that have been used to process the devices in this work, produced at CENIMAT, FCT - UNL facilities.

2.6.1 Thin-film Deposition Techniques

The circuit dies were produced through a sputtering technique for semiconductor oxide deposition and for dielectric formation. Whereas, electron-beam evaporation and spin-coating (non-vacuum) techniques were used for electrode deposition (gate,source and drain) and passivation.

- **Sputtering:** It refers to the process of dislodging molecules from a target material, through bombardment with a ionized inert gas (e.g.: Argon) that are transported through vacuum to a substrate, leading to the formation of a thin-film. In the vacuum chamber, the source material is placed on the top of cathode and the substrate placed on the anode. The strong electric field ionizes the inert gas. For the current devices, RF excitation was used at a frequency 13.56 MHz.

- **Electron beam evaporation:** The target material is heated up by a highly energetic electron beam to its vaporization point, allowing the evaporated molecules to be deposited on the substrate.

- **Spin-coating:** This method is initiated by dropping a liquid precursor on top of the substrate, then it is rotated at a high speed (above 1000 rpm), in order to spread the liquid precursor uniformly through out the substrate, forming a thin film.

2.6.2 Pattering Techniques

- **Photo-lithography:** It is used to pattern parts of a thin film. It uses UV light to transfer a geometric pattern from a photomask to a photoresist on the substrate. The undesired part is subjected for etching. This results in the desired material pattern underneath the photo resist. Finally photoresist stripping will take place.

- **Wet-etching and dry-etching:** In wet-etching the substrate is dipped in an adequate solution that dissolves the material to be etched. In dry-etching, the material is subjected to a chemical reaction and/or physical bombardment with gas ions that etches the material.

- **Lift-off:** It can be seen as a highly flexible patterning process, using photo-lithography to define in the photoresist the negative of the desired thin film pattern, followed by thin film deposition and finally by photoresist stripping. The final result is a similar thin film pattern

as the one obtained with the methods mentioned above, requiring either a negative photomask or a negative photoresist. The major advantage of lift-off is the very high selectivity (in etching processes a suitable etchant that does not affect the layers beneath has to be chosen)

2.6.3 Annealing:

Annealing is a ”cocking” process of samples that by temperature effect allows for some atomic re-arrangement. In fact, post-deposition annealing can alter the device properties to a great extent. For the current devices, annealing is performed with temperatures ranging from 150° C to 200° C. The temperature is either increased or decreased with a rate of 10° C/min. The substrate is subjected to the annealing at a desired temperature for 1 hour. Then the samples are removed only after cooling below 60° C. This process can be done after the deposition of the semiconductor layer and before source/drain electrode deposition, or it can be done after the deposition of both, depending on the materials' combinations and which layers/interfaces one wants to affect with annealing. In either case, annealed devices show better performance (channel mobility, sub-threshold voltage swing, on/off current ratio and they present decreased shifts in the threshold voltage due to biasing stress) [65].

2.6.4 Fabricated Devices

The devices used in this work (as those presented in previous sections) are fabricated at room temperature by RF magnetron sputtering and e-beam evaporation, being the patterns of the composing layers defined by lift-off and dry-etching processes. A SU-8 passivation layer on top of the structure was deposited by spin-coating [58]. Final devices were annealed in air, for one hour, at 150° C.

The semiconductor is composed by a multi-component of amorphous oxides (Gallium oxide, Indium oxide and Zinc oxide). The composition ratio [66] and the thickness of the semiconductor shows impact on the device performance, such as, switching characteristics and the V_{TH} [18, 67]. Compositions richer in indium lead to higher mobility but also higher carrier concentration, turning difficult to achieve transistors with V_{ON} close to 0 V. An increase in thickness of the active layer leads to higher off-current and lower V_{TH}. This augmented off-current results from a lower semiconductor effective resistance ($\propto \frac{1}{thickness}$), and the consequent increase of free charge carriers available for conduction in off-state. A a-GIZO composition of 2:4:2 (Ga:In:Zn atomic ratio) and thickness around 40 nm were selected in this work, based on the baseline process established at CENIMAT.

Source and drain electrodes also influence the device performance. In the present dissertation, different materials for this end have been experimented, namely, IZO, molybdenum (Mo) and Titanium / Gold (Ti/Au). A study of source/drain material impact on the device performance is demonstrated in [65]. The contact resistance (which is part of the series resistance in the device) between the source/drain metal and the semiconductor is affected by the metal properties. By us-

ing IZO as source/drain material, transparent devices can be obtained, however, IZO contacts typically lead to noiser electrical measurements compared to the Ti/Au contacts, due to IZO's higher resistivity. On the contrary, use of Ti/Au contacts make the device opaque, but show increased compatibility with wire-bonding. In order to overcome the IZO contact noise during device characterization, average value of different samples (that are fabricated in the same conditions) were considered instead of a single device.

The type of dielectric material used for the device also shows a strong impact on device performance [33, 34, 68, 69]. Multi-component dielectric structures show excellent characteristics, such as, low-leakage current, good reliability and high relative dielectric constant (ε_r) [68]. In addition, this type of material (Ta_2O_5-SiO_2) improves the dielectric-semiconductor interface properties. For this reason, a multi-component dielctric material was adopted.

Device performance is also greatly effected by the deposition conditions, such as, oxygen content (during deposition), annealing time, temperature, and RF power (sputtering). Even the deposition conditions can decide the mode of operation i.e., enhancement or depletion type. A clear study of the above mentioned parameters impact on the device performance is reported in [37].

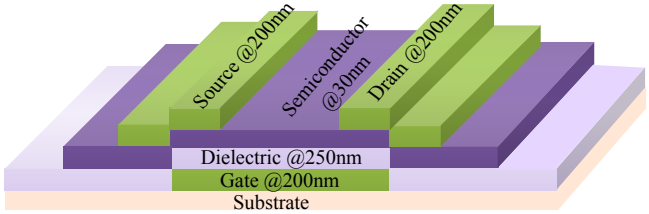
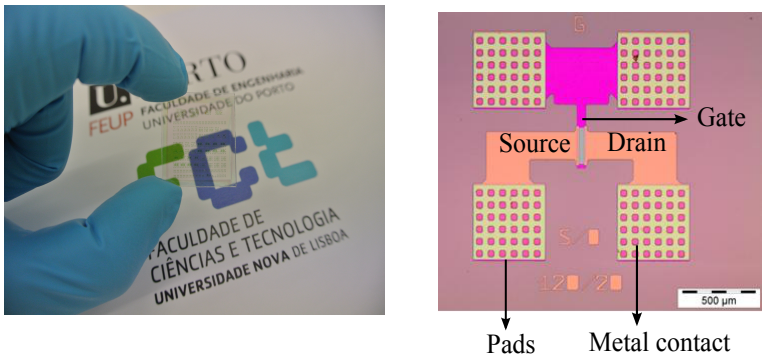


Figure 2.14: TFT structure

The device structure and thickness of the materials are shown in Fig. 2.14, and an example of a fabricated transparent chip, which contains TFTs used along this chapter, is shown in Fig. 2.15. The material structure of the devices used throughout this dissertation were stabilized in the fol-



(a) (b)

Figure 2.15: (a) Fabricated Transparent chip (b) Micrograph of a single a-GIZO TFT.

lowing form. The gate material was In_2O_3-ZnO (IZO, 200 nm thick). Different materials for source/drain electrodes were employed, such as, IZO, Mo and Ti/Au, 200 nm thick. The oxide

semiconductor is Ga_2O_3-In_2O_3-ZnO (GIZO, 30 nm thick) and the dielectric layer is a multicomponent/multilayer structure composed of SiO_2/Ta_2O_5-SiO_2/SiO_2, 350 nm thick. The substrate is a pure insulator (glass).

Chapter 3

Modeling

This chapter presents a generic introduction to modeling, benchmark tests, and a brief description of well known modeling methods, namely, physical, table-based, and empirical. The main focus is given to ANNs methodologies. An equivalent circuit (EC) based ANN model is proposed to describe the static and dynamic behavior of the transistor. Since this model is developed from the measured characteristics, bias dependent, static and dynamical characterization of the device is detailed. Here static characterization refers to the dc measurements (related to static nonlinearities) and dynamic characterization refers to the measurement of nonlinear capacitive components between different electrodes of the device. The model is further implemented in Verilog-A (hardware description language for analog circuits) to enable electric circuit simulations using Simulation Program with Integrated Circuit Emphasis (SPICE) like tools. Before applying this modeling method on a-GIZO TFTs, MOSFETs are used as a test-bed to verify the reliability of the ANN modeling methods for nonlinear semiconductor devices.

3.1 Introduction to Modeling

The design of electronic systems, in modern times, is inextricable from the world of simulation. The simulation unfolds in a virtual test-bed that mimics an experimental scenario in the real world, with virtual measurement equipment and devices. The electrical simulator is responsible in this environment for finding the solutions (response) of circuits in different domains. It is a software engine that incorporates mathematical representations of different electrical devices, including resistors, capacitors, transistors and so on, or even circuit-block level (behavioral) representations. It also embodies in its core the Kirchoff laws that mutually constrained by circuit interconnectivity descriptions (either textual or pictorial, in a form of a schematic), together with those mathematical representations, engenders a set of equations (in general a nonlinear differential equation) that are solved through numerical methods. If everything goes as expected, the solution for a given set of external excitations should be in accordance, within a given interval of verisimilitude, to that measured response from a real circuit that is setup in a similar manner. Obviously this corresponds to an ideal situation, but if the design is prepared with care and real operation conditions are

predicted well, with the aid of a good circuit simulation environment, it is possible to accomplish a first-time right design, i.e., a design that after production behaves within the predicted boundaries (especially for digital CMOS design this is well stated). What makes this a fact or not is the level of accuracy of the device representations. The method employed to get these representations is called modeling, and the representation itself is the model. Typically, a model is ultimately defined by a set of model parameters (with or without physical meaning). The process of finding the parameter values from measurement setups on real devices is called parameter extraction. This can follow an optimization procedure based on measurements; seldom in this case the parameters entail a direct physical interpretation, while in other cases the measurement may predominately emphasize some particular physical behavior that may be reflected on a model parameter.

It is clear by now that the development of circuits for any integrated circuit technology demands accurate models in order to predict the device(s) behavior with good precision under circuit simulations. A transistor model should then at least describe well its static and dynamic response, in all regions of operation (cutoff to saturation). The level of faithfulness needed from the model typically depends on the purpose, some may need to be more comprehensive and general, others may be more specific or directed towards a definite goal. In this respect, when compared to digital circuits, analog circuits are in general more demanding from the models. Transistors in digital systems mostly operate in either *on* or *off* state. The most important information comes from the extraction of the binary number ”1” or ”0”, whereas in analog circuits, signal integrity analysis is fundamental for matters of distortion and dynamical specs. Nevertheless, it should be noted that for high-speed digital systems signal integrity is also becoming evermore important, specially in driver circuits. The device model can be developed in two fundamental ways: a single model that covers all regions of operation, or by developing different models for different regions of operation. Problems rise with the last approach due to discontinuities at the transitions between regions of operation. This is critical because it may cause convergence difficulties during numerical solving.

The past few decades have been prolific in models for complementary metal oxide semiconductor (CMOS) technology. There are more than 70 models [70] for MOSFETs, addressing various effects like derivative discontinuity, geometry effects, self heating, negative conductance, bulk charge effect on current, velocity saturation, hot carriers and impact ionization. Some of these models are empirical, some are semi-empirical and others are physical (more details later). For CMOS, Level 1 SPICE model is the simplest and fastest, but it is far from meeting industrial needs, specially for sub-micron technologies [71, 72]. However, it is often used to represent the fundamental behavior of TFTs. As with almost all TFT technologies, a-GIZO TFT is yet in an early development phase, and still far from being in a standardised form, which is reflected in a limited amount of modeling results [32, 73, 74], thus making the design of circuits very challenging. To meet the requirements of productive and complex circuit design, an accurate model should a priori be formulated according to the following basic guidelines:

- Generically, the model should be simple for easy implementation and minimal simulation time [71, 72]. This typically implies on the time to market. The development time of inte-

grated circuit (IC) systems is indeed strongly determined by design, and simulation can take a big slice of the overall process. After the circuit is defined, and all geometric and parametric variables are set, in general many simulation cycles will befall before all specifications are met. If many errors persist along the way, or if the circuit is not meeting the design specifications, it needs to be redesigned and re-simulated, which is aggravated in a post-layout phase where extra parasitics are added. If the model is then too complex, it will amount on the time to reach an error free circuit with the required design specifications. Nevertheless, complex device models are more likely to be accurate, whilst a simple model might be less accurate, in principle it is faster. Consequently, there is always a tradeoff between simplicity and accuracy that needs to be assessed as the model is being devised.

- The model and its derivatives (even higher order) should be continuous in the complete region of operation, which is a requirement in ac analysis and intermodulation distortion calculation. Besides, discontinuity in the model may cause convergence problems.

- The model should, as possible, involve some physical properties, with parameters embodying some physical meaning. When the model is based on device physics, it is highly accurate and can be extended to the complete operating region of the devices. In addition, it allows for separability of various physical effects, which can be of help during trouble shooting.

- Sometimes modeled drain current may present a good agreement with the measured data, but the small signal parameters, namely, transconductance (g_m) and output conductance (g_d) may show discrepancies. Validating small signal parameters from the model is one of the benchmark tests suggested in literature [75] as they have a direct impact on small signal behavior.

3.2 Traditional Modeling Methods

Transistor modeling methods can be broadly classified into physical, table-based and empirical. A brief description of these modeling methodologies are given in the sequel.

3.2.1 Physical Modeling

In general, the equations of a physical model are developed from the device physics, based on carrier transport principles and characteristics of the materials [76]. The resultant equations hold several parameters with physical meaning. Nevertheless, often some fitting functions or new parameters (empirical) are added to help the model to better match the device characteristics. This approach is known as semi-empirical modeling and is the preferred method in commercial models. In general, physical and semi-empirical models are accurate, continuous, valid for all regions of operation and are required for fabrication process optimization (since the model parameters are directly related to the fabrication process). For this reason, there has been a good effort along

the time to come up with good physical and/or semi-empirical models to describe different physical phenomenas, and for various types of transistors like MOSFETs [77, 78, 79, 80], a-Si:H TFT [81, 82], poly-Si TFT [83], organic TFT [84, 85] and a-GIZO TFT [73, 31, 86, 87]. However, physical models frequently result in complex mathematical representations, and building the model itself is very time-consuming; this is probably its main disadvantage. In addition, getting process information from the foundry is not always possible. As the parameters in these models are mostly related to the fabrication process or technology, and fabs generally need to protect this information from the competition, the complete description of the model may, in many cases, not be disclosed to the end user (circuit designer).

3.2.2 Table Based Modeling

Table based models are in the form of lookup tables, in which, the drain current of the transistor is stored for different values of bias voltages [88, 89]. For un-stored voltages, the drain current can be obtained through interpolation techniques. The benefits associated with the approach are mainly (i) fast development time, as the measured drain current can be directly stored without any further parameter evaluation and (ii) good simulation speed since the amount of computation involved is minimal. However, the accuracy of the model depends on the resolution of the stored data. Interpolation techniques provide high accuracy when the the number of stored data points is high, which may impose huge memory requirements. In addition, it is not possible to extend the model outside the dataset boundaries.

3.2.3 Empirical Modeling

Empirical modeling is a black-box approach. That is, the model predicts the device behavior for a given stimulus regardless of the underlying device physics. In general, empirical models are developed from the measured device characteristics through curve fitting or function approximation that is optimized according to some criteria. One approach is to partition the total operating region into few regions, and each region is approximated by a linear function along with some smoothing function in the boundaries. This corresponds to a piecewise linear approximation with smoothing between transitions of linear regions, also known as smooth canonical approach [90]. Another form of empirical modeling is polynomial curve fitting, where the device characteristics are approximated with a suitable polynomial equation(s) by finding suitable coefficients. ANNs also belong to the empirical modeling category, as they do not rely on the device physics [91]. The main advantages of this modeling approach is lower development time, simplicity and accuracy. Unlike physical models, the tuning parameters do not hold any explicit physical meaning, however the intelectual property is better protected because it becomes very hard, if not impossible, to get insight on the technological process from modeled parameters.

3.3 Model Selection for a-GIZO TFT IC Design

The main objective of this dissertation is to design analog/mixed signal circuits using a-GIZO TFTs. After the above, it becomes apparent that the development of an accurate compact model for a-GIZO TFT is essential to accomplish such goal. Furthermore, it should facilitate immediate circuit design and serve as a viable alternative to conventional methodologies used with a-GIZO devices.

Technologies based on a-GIZO TFT are still emergent, with experiments almost continuously being performed to attain solid and consistent electrical characteristics by employing: different structures [47], multiple channels [48], varying processing parameters, source and drain [37] or dielectric materials [92, 93]. Therefore, whenever there is an effort to obtain better performance, every time the envisioned model needs to be modified to incorporate the device physics corresponding to the new changes. In this context, even though physical models are accurate and desirable for circuit design and process optimization, the development time tends to be long and the existent physical models are yet somehow incipient for a-GIZO TFTs. Nevertheless, some work on physical models for these devices is already reported [73, 31, 86, 87], but most of them are confined to only static behavior. On the other hand, models that are developed from the measured characteristics, such as with empirical approaches, are good alternatives to physical modeling, and in general involve less development time.

It should be kept in mind that both static and dynamic nonlinear behaviors should be captured by the model. If some knowledge is added about the device structure, in a form of an electric circuit with lumped elements, then both static and dynamics can be separated. This is the method adopted in this work, which is commonly referred as the EC (equivalent circuit) approach. It will simplify the modeling process and will bring more insight into how the device operates. The method is envisioned here as empirical but where some insight about the physical structure is preserved. In this modeling method, an EC is derived from the device structure (please refer to Fig. 2.14) to characterize its electrical behavior. The proposed circuit consists of parasitic components and dependent sources, as shown in Fig. 3.1. The parasitic components are capacitances between gate to source (C_{GS}) and gate to drain (C_{GD}) electrodes. The voltage dependent drain current that flows from drain to source, is denoted by the dependent current source in Fig. 3.1a. In addition, there is an inevitable series resistance (R_D and R_S) present in the device, as explained in section. 2.3.1. Since the bulk (glass) is a pure insulator, there are no parasitic components related to it (unlike MOSFETs). As the a-GIZO TFT model is developed from the measured data, this method includes extrinsic device behavior, i.e., intrinsic behavior along with the impact of the series resistance (R_S and R_D) as shown in Fig. 3.1b. If only the intrinsic behavior of the device needs to be modeled, the impact of R_S and R_D should be de-embedded from the measured data. Then, this new data should be used for the model development.

In order to model the electric elements (capacitors and dependent sources) in the EC, empirical modeling approach with ANNs is adopted, because ANNs show enough flexibility to include other input parameters with physical meaning (e.g. device dimensions and temperature) beyond

the terminal electrical variables, such as voltages and currents. These models are accurate, simple, continuous (the model and its derivatives), and it is able to effectively characterize all the physical properties of the device in the complete region of operation because ANNs are universal approximators [94]. Polynomial curve fitting follows that same characteristic and could be employed for the same purpose, but with ANNs the error is independent of the input dimensionality [95] and polynomials are continuously differentiable only up to the finite order of the approximator. Furthermore, despite the fact that ANN parameters lack explicit physical meaning, it satisfies most of the basic model requirements and benchmark tests suggested in literature [71, 72, 96].

Once the individual elements are modeled through the ANNs, they are connected as per the EC configuration to fully describe the static and dynamic behavior of the device. One should note, as stated earlier that the proposed model cannot be seen as purely empirical, because it partially uses device physics by deriving the EC from the known device structure; but, as discussed below, it allows the separation of the static problem from the dynamics, which diminishes the complexity in finding the approximator.

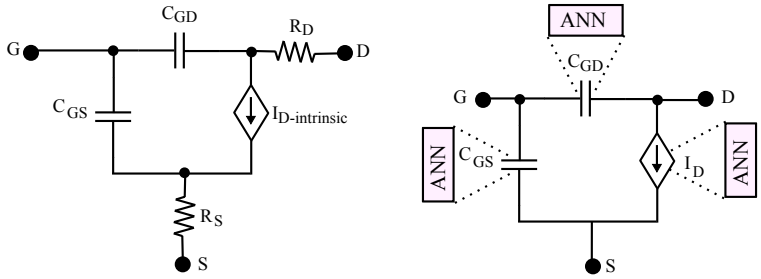


Figure 3.1: Employed equivalent circuit from the device structure when the bulk is an insulator (a) TFT equivalent circuit with series resistance components (b) Equivalent circuit components, to be modeled with ANNs : measured I_D includes R_S and R_D impact.

3.4 ANNs for Nonlinear Semiconductor Modeling

From past two decades, ANNs have become popular for static nonlinear device modeling. Results have shown their ability in capturing both large and small signal behavior, and several examples can be found in literature to support this claim. Litovski proposed multilayer perceptron (MLP) for MOSFET modeling [91] that has also been successfully applied to nanoscale MOSFETS [97, 98], microwave transistors [99, 100], and organic TFTs [101]. On the other hand, support vector machine (SVM) ANN model was developed for silicon carbide metal semiconductor field effect transistor (SIC MESFET) [102].

As referred in last section, ANNs are universal approximators. Thus, they can estimate any function to the desired level of accuracy, and accomplishes the goal through a data driven process. This is the reason why it is popular for device modeling. Unfortunately, however, it is neither possible to know a priori nor does exist a systematic way to find the dimension of the system that will accomplish the goal, which hardens the process of finding the optimal network. Generically,

the architecture of an ANN corresponds to that of a parallel computing machine, formed from the interconnection of a set of artificial neurons, as shown in Fig. 3.2. Each neuron in the network, commonly known as processing element, has a set of inputs, synaptic weights and bias. An amount of training samples are then applied at the input layer of the network so that it can learn the underlying physical process, subjected to a cost-function minimization. Functionally, the input layer in the ANN consists of sensory units, which connect to the outside environment (input data). The Hidden layer(s) then maps the input space into a hidden space through projecting weights and nonlinearities, often called activation functions. Finally, the output layer provides response to the input activations by a linear combination of the hidden layer outputs. Three different architectures will be considered for the purpose of a-GIZO TFT model development, namely: MLP, radial basis function (RBF) and least square support vector machine (LS-SVM). The last two are known to be good interpolators and MLPs in general render a lesser complex network. Confronting these techniques will help to identify the proper method to be used for circuit simulations.

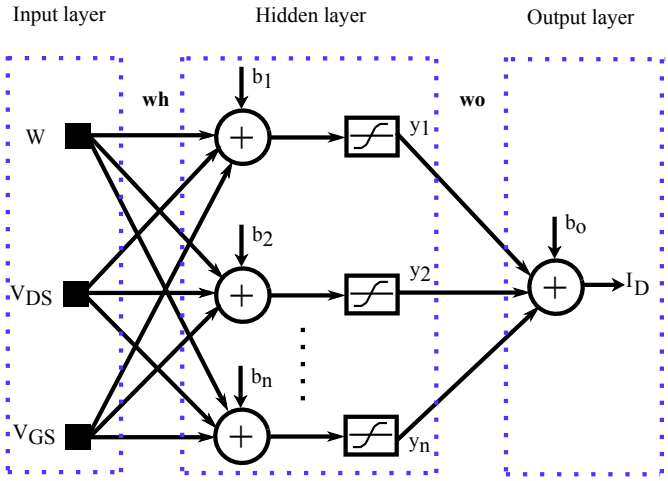


Figure 3.2: ANN topology with a single hidden layer

The reliability of the proposed ANN modeling technique is first verified with MOSFETs. The training data is generated from BSIM3V3 [103] using Cadence simulator. Although real-data collection would be the best, because all environmental factors would be present, BSIM3V3 is a well established model that has been ”silicon” proofed, and in this way data can be readily obtained through simulation, at any instant. All the above mentioned ANN modeling methods are tested with a single MOSFET, as a first step, in order to check the impact of the input data size on the model performance and also to determine the most suitable approach for circuit simulations that can show good accuracy with minimal complexity. Then, the best ANN modeling approach is used for multiple MOSFETs with different widths, so that the actual circuit design is not confined to single sized transistors. Later the model is extended to include device dynamics. Once the reliability of the modeling method is confirmed with MOSFET, the same procedure is followed for the a-GIZO.

Modeling Method: The proposed method consists of the following steps:

1. Acquire data from the simulator/measurements for MOSFET/a-GIZO TFT respectively, to train the network. Body effect in the MOSFET is eliminated by connecting the source terminal to the bulk. This is done to bring a platform where the proposed modeling method can be more directly applied to devices where the bulk is an insulator. The measurements for a-GIZO TFT were collected using a semiconductor parameter analyzer Keithley 4200-SCS, and probe station Cascade Microtech M150 under darkroom conditions.

2. Train the neural network with the data and ensure that there is no overfitting. The following are possible alternative methodologies:

   - A single network for all the parameters I_D, C_{GD} and C_{GS} (shown in Fig. 3.1) in the complete region of operation i.e. from cutoff to saturation. This method may diminish accuracy, as the parameters that need to be modeled do not follow similar relationships with the inputs and also their values are spread in a wide range. So, this approach is not, in principle, the better choice for the current case.
   - A different network for each parameter I_D, C_{GD} and C_{GS} (as shown in Fig. 3.1b) for the complete region of operation, i.e. from cutoff to saturation, can mitigate the problem of a single network and was employed in the modeling process.
   - Different networks for different regions of operation. This allows each network to specialize in a particular local behavior of the device. However, It may lead to convergence problems when a transition from one region to another occurs during simulation, which normally demands some sort of smoothing function to attenuate the transitions. For this reason, this possibility was not considered during model development.

3. Implement Verilog-A model (for Fig. 3.1) for the resultant networks from training and create a generic cell for circuit simulations.

4. Validate the neural model performance for both static and dynamic characterization.

All the above mentioned ANN methodologies (MLP, RBF and LS-SVM), its details and preliminary results for the MOSFET modeling, are presented in the following sections. A comparison of models performance is then carried out to select the most suitable approach for circuit simulations.

3.4.1 Multi Layer Perceptron

An MLP network, with a single hidden layer, is depicted in Fig. 3.3. Proper number of neurons in the hidden layer should be selected to ensure good training performance without overfitting. If the number of neurons in the hidden layer is too high, then, even though the network guarantees good training performance, its generalization will be poor because of overfitting. If the number of neurons in the hidden layer is small, then the network will show insufficient performance. Proper selection of the number of neurons is critical and it is normally accomplished through a trial and error process.

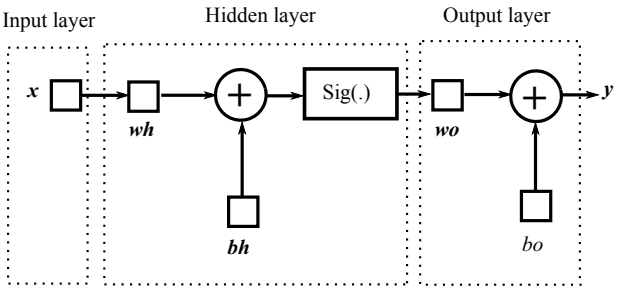


Figure 3.3: MLP Network topology

Mathematically, the MLP network hidden layer outputs can be expressed by,

$$yh = \text{Sig}(\mathbf{x} \cdot \mathbf{wh} + \mathbf{bh}), \tag{3.1}$$

and the output of the MLP network given by,

$$\mathbf{y} = \mathbf{yh} \cdot \mathbf{wo} + bo, \tag{3.2}$$

where $\text{Sig}(\cdot)$ represents the tanh sigmoid function (activation function), $\mathbf{x}$ represents the input vector, **wh** and **bh** denote the synaptic-weight vector, connecting inputs to the hidden layer neurons, and the hidden neurons bias vector, respectively. The output layer weight vector and bias are represented by **wo** and bo. Weights and biases are trained in a supervised fashion, as depicted in Fig. 3.4, using backpropagation [104]. Parameters are iteratively updated such that the error surface is covered to a minimum value.

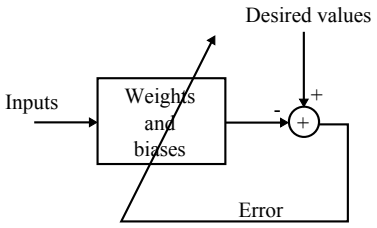


Figure 3.4: Backpropagation pictorial representation

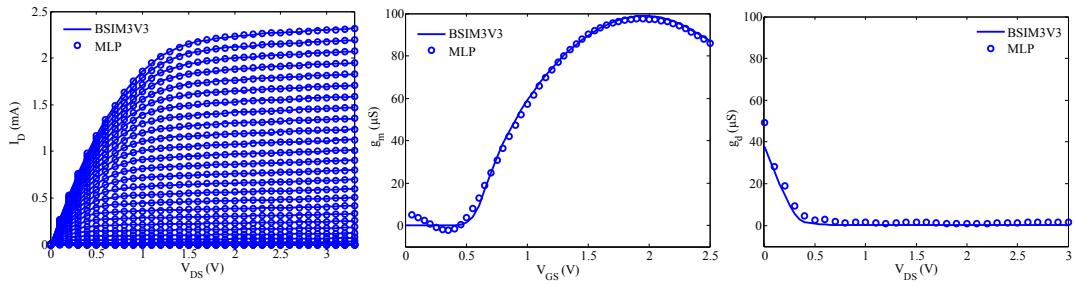
Preliminary Results with MOSFET: The MLP network is trained with the BP algorithm, in MATLAB20011b. The input and output data are preprocessed in such a way that the complete training data-set lies within the linear region of the activation function. Various number of neurons in the hidden layer are used to check their impact on the modeling accuracy. During the training phase, the input data is divided into training (60 %), validation (20 %) and testing (20 %), selected in a random fashion from the overall input samples. Training data is used to train the network, from which the network learns the function that needs to be estimated. Validation data is used to check the ANN modeling performance for unseen data during training, and used as a stopping criteria in

training. On the other hand, testing data is used to check the ANN generalization capability after training.

The input parameters of the network are V_{GS} and V_{DS}. These inputs are varied in the range of 0 to 3 V and 0 to 3.3 V respectively, for a transistor with 5 μm width. In order to test the network performance, with respect to the training data size, training inputs are given in steps of 0.05 V, 0.1 V, 0.2 V and 0.3 V, referred to as *data-set1*, *data-set2*, *data-set3* and *data-set4* respectively. The MLP performance for all data-sets can be observed in Table 3.1. A quick view reveals that when *data-set4* is used for training, all the three ANN networks showed poor performance, which implies insufficient training data. For this reason, the step used in future experiments is confined to a maximum of 0.2 V.

Table 3.1: MLP results for single MOSFET

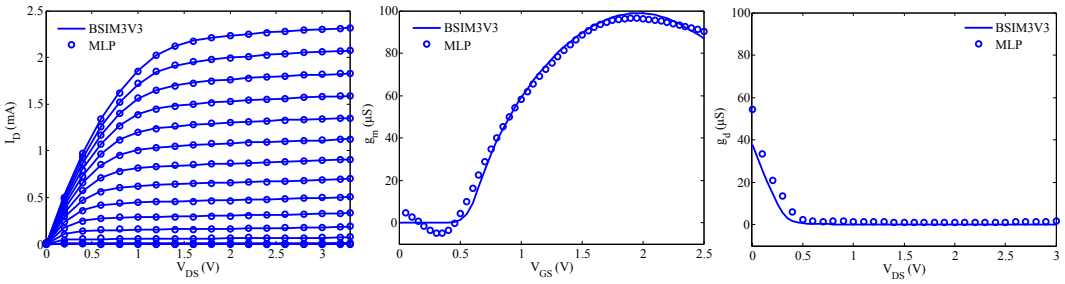
No.of Neurons	data-set1		data-set2		data-set3		data-set4	
	MSE	Epochs	MSE	Epochs	MSE	Epochs	MSE	Epochs
10	5.1e-11	82	1.5e-10	46	6.05e-11	35	1.82e-08	11
15	9.5e-12	122	5.1e-11	41	4.18e-11	124	5.51e-10	15
20	5.78e-11	30	5.05e-12	111	1.29e-11	47	8.1e-12	17
25	8.51e-12	46	5.11e-11	24	9.49e-11	23	1.36e-08	11
30	2.02e-11	27	6.42e-12	98	5.08e-11	24	2.66e-08	10
35	5.31e-12	77	1.11e-11	27	1.37e-12	31	2.74e-10	12
50	3.75e-12	40	3.3e-12	35	4.4e-10	14	1.24e-10	11
60	1.18e-12	36	2.49e-12	43	2.57e-10	15	5.75e-08	6
75	5.87e-12	40	2.69e-12	27	2.29e-11	16	1.09e-07	10
100	3.08e-12	32	8.03e-12	28	1.14e-9	11	4.08e-08	8



(a) (b) (c)

Figure 3.5: MLP model results, when the network has 20 hidden layer neurons and trained with *data-set2* (a) MOSFET output characteristics (b) Transconductance at V_{DS}=1 V (c) Output conductance at V_{GS}=1 V.

The MLP model response for I_D, g_m and g_d for the training sets – *data-set2* and *data-set3* – are presented in Fig. 3.5, and 3.6, respectively. The small signal parameters are calculated from numerical approximation. The importance of these parameters come from the fact that if overfitting occurs, the variations in the characteristic predicted by the model will be emphasized in small



(a) (b) (c)

Figure 3.6: MLP model results, when the network has 20 hidden layer neurons and trained with *data-set3* (a) MOSFET output characteristics (b) Transconductance at V_{DS}=1 V (c) Output conductance at V_{GS}=1 V.

signal parameters due to their derivative nature, and thus helps to infer about the generalization capability of the network. Moreover, they are also fundamental for small signal analysis and simulation and thus need to be benchmarked. Discussion on these results and comparison with the other ANN approaches presented next are left for the end of the section. However, a simple visual inspection reveals that the model seems to be approximating well the different characteristics of the device.

3.4.2 Radial Basis Function

Basically, RBF performs curve fitting/approximation in a high dimensional space [105]. During the training phase, the RBF network finds a surface in a multi-dimensional space that provides the best fit to the training data. Generalization of the network refers to interpolated test data in the multi-dimensional space. RBF network topology is shown in Fig. 3.7. Similar to the MLP, the input layer comprises sensory units, where the stimulus can be applied from the outside environment. The hidden layer maps the input to a high dimensional hidden space to guarantee accurate and smooth functional approximation (since the accuracy of functional approximation increases with respect to dimension of the hidden space) [105].

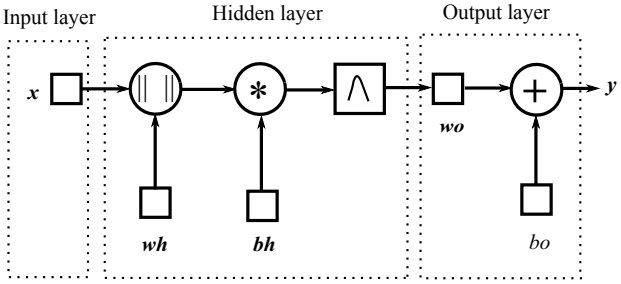


Figure 3.7: RBF/LS-SVM network topology

The hidden layer output can be described as,

$$\mathbf{yh} = \mathbf{G}(||(\mathbf{x} - \mathbf{wh})||\mathbf{bh}) = exp^{-(||(\mathbf{x}-\mathbf{wh})||\mathbf{bh})^2}. \tag{3.3}$$

The resulting RBF is then built from kernels that are Gaussian functions, with an output that is also given by (3.2). The input weight vector is again **wh** (centers of the Gaussian functions), **x** is the training data vector i.e., input to the network. The hidden layer bias is given by $bh = \frac{0.8326}{\sigma}$, where σ is the spread or standard deviation of the basis function. This *bh* value was chosen such that the output of the hidden layer neuron is $\geqslant 0.5$ when the distance between the input vector and the input-weight vector is $\leqslant \sigma$. The centers of the Gaussian functions (which directly gives the number of neurons in the hidden layer), are determined from the training samples. The output weight vector (**wo**) and output bias (*bo*) are calculated by solving linear expressions formed by the output layer.

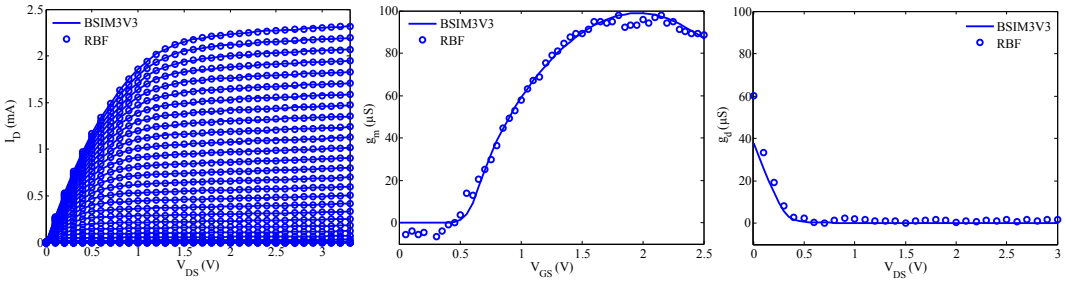
The standard deviation σ of the Gaussian function plays an important role on the ability of the network to find the best interpolator. If σ is too small, then the basis function is highly localized, hence the network cannot guarantee good generalization. If it is too high, neurons respond in the same way to all the activation samples, consequently the network is not able to learn from the training samples. Therefore, σ should be greater than the smallest difference between neighboring input training samples and less than the largest difference in the set, so that the basis function is neither localized nor too flat. The parameters that need to be calculated during the training phase are **wh**, **wo**, and *bo* for the given σ and **goal**.

Preliminary Results with MOSFET: Again, MATLAB2011b is used for RBF modeling, which supports two types of radial basis functions:

1. Exact fit (Matlab function – newrbe): This function minimizes the MSE to the maximum extent by employing more number of neurons. This method results in a network whose size (number of hidden neurons) is equal to the number of training samples. With this function the user can provide only the kernel spread in the hidden layer. This technique is not helpful for the current application, because with large number of training patterns the resulting network becomes massive. It implies more complexity and consequent longer simulation time.

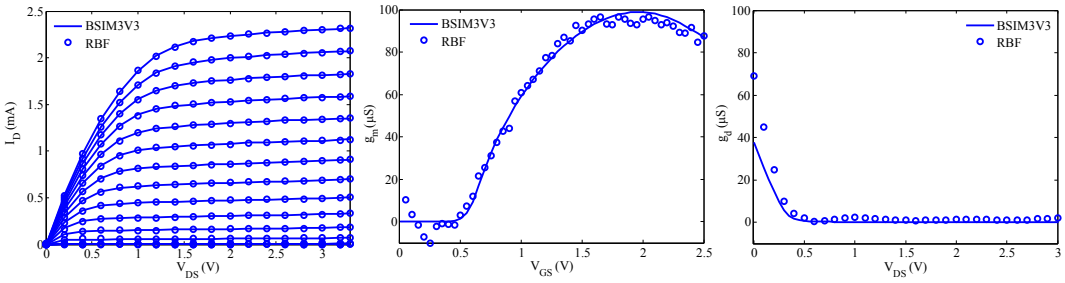
2. Fewer neurons (Matlab function – newrb): Here the user can provide a goal and spread. This method uses the minimum number of neurons possible to meet the goal.

When the network is trained with *data-set2* and *data-set3*, the modeled I_D, g_m and g_d can be observed in Fig. 3.8 and 3.9 respectively. The modeling performance, with all data-sets, can be observed in Table 3.2.



(a) (b) (c)

Figure 3.8: RBF model results, when the network has 100 hidden layer neurons and trained with *data-set2* (a) MOSFET output characteristics (b) Transconductance at V_{DS} 1 V (c) Output conductance at V_{GS} 1 V.



(a) (b) (c)

Figure 3.9: RBF model results, when the network has 100 hidden layer neurons and trained with *data-set3* (a) MOSFET output characteristics (b) Transconductance at V_{DS} 1 V (c) Output conductance at V_{GS} 1 V.

Table 3.2: RBF results for MOSFET

No.of Neurons	Spread	MSE			
		data-set1	data-set2	data-set3	data-set4
50	2	2.0e-11	1.42e-11	1.27e-11	1.65e-12
75	2	1.42e-11	8.42e-12	9.43e-12	-
100	2	1.25e-11	7.65e-12	8.1e-12	-
50	3	2.75e-11	5.73e-11	3.5e-11	3.3e-12
75	3	2.96e-11	3.1e-11	1.61e-11	-
100	3	2.94e-11	2.98e-11	1.66e-11	-
50	5	9.71e-11	1.19e-10	9.7e-11	2.01e-11
75	5	6.95e-11	4.83e-11	6.94e-11	-
100	5	8.35 e-11	4.7e-11	8.35e-11	-

3.4.3 Least Square-Support Vector Machine

LS-SVM is a powerful technique for nonlinear regression or functional approximation problems. Its structure is basically the same as RBF (Fig. 3.7), since the kernel (K) chosen is in fact a radial basis function, but differs in the learning process. For function estimation, in its primal and dual

form, it can be expressed as (3.4) and (3.5) respectively [95].

$$\begin{aligned} \text{Min.}_{(w,b,e)} J_p(w,e) &= \frac{1}{2} w^T w + \gamma \frac{1}{2} \sum_{i=1}^{N} e_i^2, \\ \text{such that} & \\ y_i &= w^T \phi(x_i) + b + e_i, i = 1, ..., N. \end{aligned} \tag{3.4}$$

$$\begin{aligned} L(w,b,e;\alpha) &= J_p(w,e) - \sum_{i=1}^{N} \alpha_i [w^T \phi(x_i) + b + e_i - y_i], \\ \text{such that} & \\ \frac{\partial L}{\partial w} &= 0 \rightarrow w = \sum_{i=1}^{N} \alpha_i \phi(x_i), \\ \frac{\partial L}{\partial b} &= 0 \rightarrow \sum_{i=1}^{N} \alpha_i = 0, \\ \frac{\partial L}{\partial e_i} &= 0 \rightarrow \alpha_i = \gamma e_i, i = 1, ..., N, \\ \frac{\partial L}{\partial \alpha_i} &= 0 \rightarrow w^T \phi(x_i) + b + e_i - y_i = 0, i = 1, ..., N. \end{aligned} \tag{3.5}$$

The factor γ is a regularization parameter, which impacts on the network generalization capability and e gives the accuracy of the model. α_i is a Lagrange multiplier and ϕ is nonlinear transformation from input space to feature space. After solving (3.5), the resulting LS-SVM model for function estimation can be expressed as (3.6)

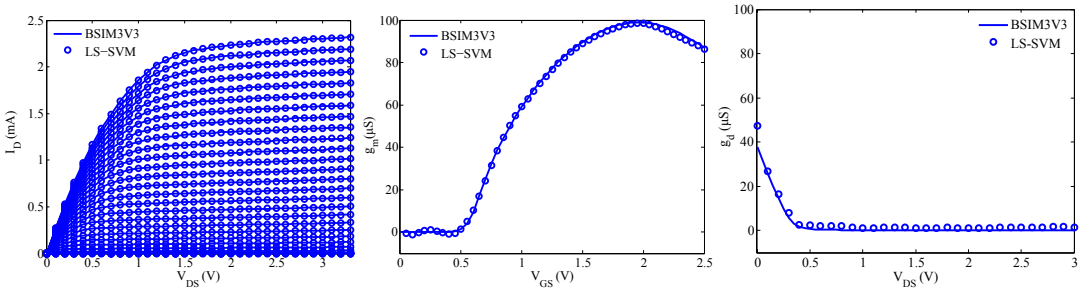
$$y(x) = \sum_{i=1}^{N} \alpha_i K(x, x_i) + b, \tag{3.6}$$

where $K(x, x_i) = \phi(x)^T \phi(x_i)$. It should be noted that LS-SVM employs structural risk minimization principle, since it deals with both generalization and training error, while the other two previous networks employ empirical risk minimization principle, i.e., minimization of the training error [105]. In this sense, LS-SVM promises better generalization results when compared to the other two methods.

Preliminary Results with MOSFET: The LS-SVM input and output training data-sets are the same as that used with MLP and RBF. LS-SVMlab toolbox in [106] is used to find the LS-SVM network parameters. Modeling results with all the data-sets can be observed in Table 3.3. The model results for I_D, g_m and g_d with *data-set2* and *data-set3* can be observed in Fig. 3.10 and 3.11 respectively, when radial basis kernels are adopted.

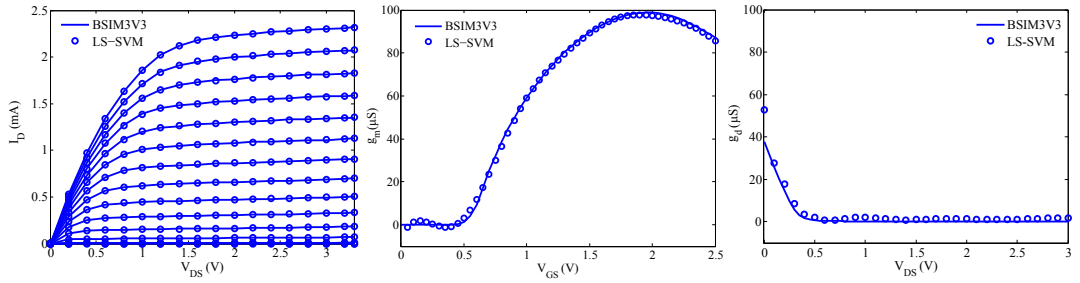
Table 3.3: LS-SVM results for MOSFET

Data	No.of.support vectors	MSE	Epochs
data-set1	4087	2.519e-12	13
data-set2	1054	2.84e-12	12
data-set3	288	4.99e-12	10
data-set4	56	5.8e-11	12



(a) (b) (c)

Figure 3.10: LS-SVM model results, when the network has 1054 support vectors and trained with *data-set2* (a) MOSFET output characteristics (b) Transconductance at V_{DS} 1 V (c) Output conductance at V_{GS} 1 V.



(a) (b) (c)

Figure 3.11: LS-SVM model results, when the network has 288 support vectors and trained with *data-set3* (a) MOSFET output characteristics (b) Transconductance at V_{DS} 1 V (c) Output conductance at V_{GS} 1 V.

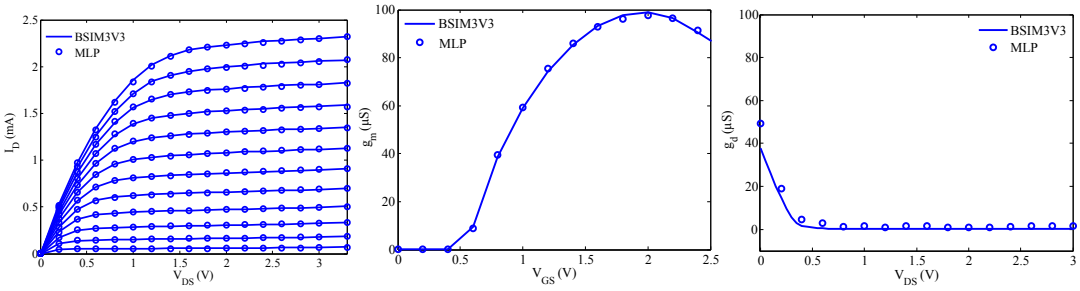
3.4.4 Discussion from MOSFET Modeling Results

All the above ANN methods are potential candidates for nonlinear semiconductor modeling. However, these methods are compared to evaluate the best technique among the three that can be more suitable for circuit design. Best performances of all the ANNs for *data-set2* (reasonable training data size), is highlighted in Tables. 3.1, 3.2, 3.3. From these metrics, it is clear that the LS-SVM performance is the best, but its complexity is the highest (which imposes strict limitation on the simulation speed of complex circuits), whereas, RBF complexity is higher than MLP and its performance is also relatively lower. The MLP shows reasonable accuracy with minimal complexity.

Hence, this technique will be used to extend the model for multiple MOSFETs. Data taken from nine transistors is used for training and one transistor is used for testing (i.e., data not used during training). In both training and testing cases, the inputs are W, V_{GS} and V_{DS}, whereas the output is I_D. In the training data, W is ranging from $1\,\mu$m to $4\,\mu$m and $6\,\mu$m to $10\,\mu$m. The bias voltages are : $0 \leq V_{GS} \leq 3\,V$ and $0 \leq V_{DS} \leq 3.3\,V$, in steps of $0.2\,V$, while for the testing data, W is $5\,\mu$m, $0.8 \leq V_{GS} \leq 3\,V$ and $0 \leq V_{DS} \leq 3.3\,V$, in steps of $0.2\,V$. The MLP modeling performance for multiple MOSFETs is shown in Table 3.4, and the respective testing results (I_D, g_m and g_d) for unseen transistor data during training are shown in Fig. 3.12.

Table 3.4: MLP results for multiple MOSFETs

No.of Neurons	MSE	Epochs
10	2.35e-10	374
15	2.82e-11	781
20	1.35e-11	659
25	7.45e-12	938
30	8.36e-12	200
35	3.07e-11	57
50	3.09e-12	532
60	2.21e-12	279
75	1.67e-12	436
100	1.84e-12	101



(a) (b) e (c)

Figure 3.12: MLP model response for the testing data, where the transistor W = $5\,\mu$m, $0.8 \leq V_{GS} \leq 3\,V$ and $0 \leq V_{DS} \leq 3.3\,V$, in steps of $0.2\,V$ and the number of hidden neurons is 50 (a) MOSFET output characteristics (b) Transconductance at V_{DS} $1\,V$ (c) output conductance at V_{GS} $1\,V$.

3.5 TFT Static Modeling

From the previous section it is clear that ANN models, namely, MLP, RBF and LS-SVM are potential candidates to model the nonlinear behavior of the semiconductor. Accordingly, all these techniques were also applied to model the a-GIZO TFT. Similar to the procedure followed with

the MOSFET, MATLAB2011b tool is used to get the trained network for MLP and RBF, while for the LS-SVM a Matlab toolbox found in [106] is used instead. Initially, TFTs with different widths (40 μm, 80 μm, 160 μm, and 320 μm) were characterized for static behavior (I_D as a function V_{GS} and V_{DS}). Then, I_D in terms of V_{GS}, V_{DS} and W is modeled [107], similar to the previous MOSFET MLP approach. The input data to the MLP network is as follows: V_{GS} and V_{DS} are in the range of 0 to 20 V in steps of 2 V and 0.5 V, respectively. The W values are 40 μm, 80 μm, 160 μm, and 320 μm. The network performance in terms of MSE is shown in Fig. 3.13. Post training regression plots are shown in Fig. 3.14, which shows that the model is capable of predicting the device behavior to good accuracy, as a correlation factor very close to 1 shows, and also the error is very small.

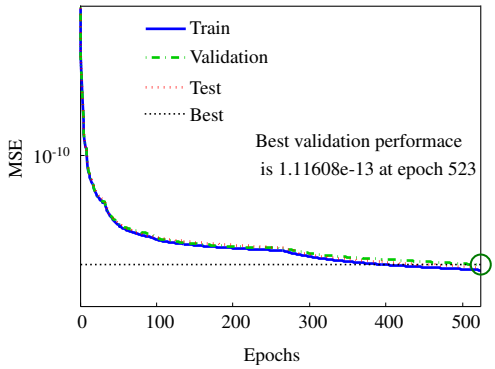


Figure 3.13: ANN performance.

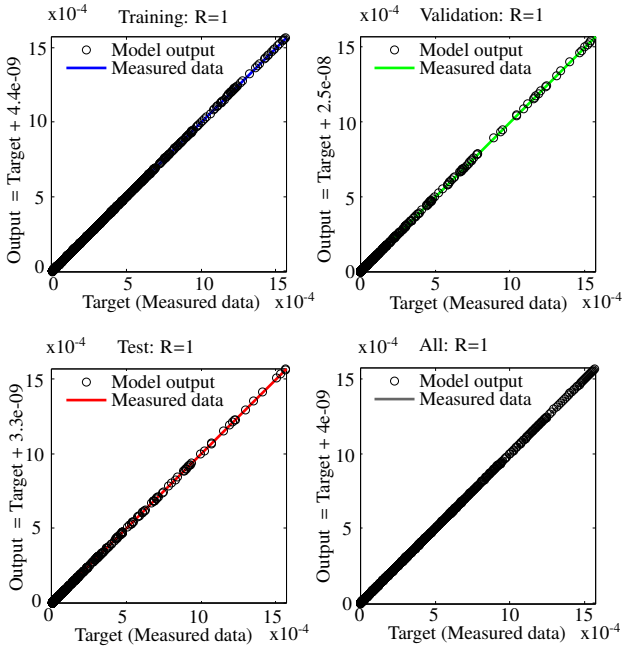


Figure 3.14: ANN post-training performance.

Once the network has met the required performance goal, from the measured data, the resulting ANN model (with 50 neurons) is implemented in Verilog-A to creat a generic cell that is then used

in circuit simulations.

3.5.1 Discussion

A comparison of all the above mentioned ANN modeling methodologies are presented in terms of MSE and complexity of the network, where the modeling outcome is always compared with measured data from a real device to validate its accuracy. Drain current modeling performance (for training as well as testing data) with MLP, RBF and LS-SVM can be observed in Table 3.5, 3.6 and 3.7, respectively.

Table 3.5: MLP results

No.of Neurons	MSE		Epochs
	Training data	Testing data	
5	5.7e-15	7.1e-15	87
10	6.9e-17	1.4e-16	112
15	9.2e-18	1.2e-16	73
30	3.4e-18	3.6e-15	95
60	3.1e-18	6.1e-14	31

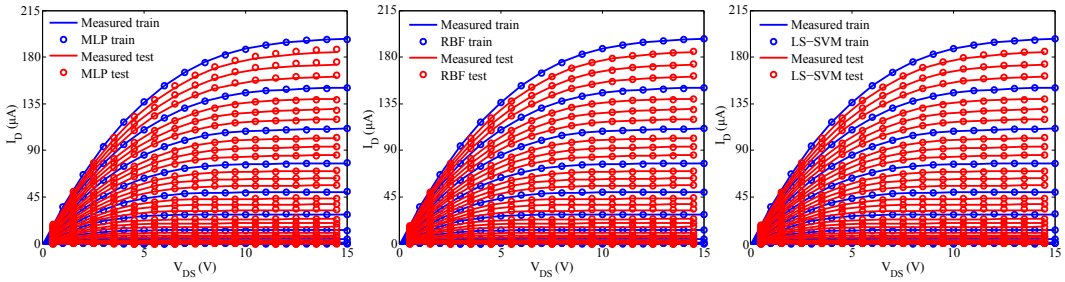
Table 3.6: RBF results

No.of Neurons	Spread	MSE		Epochs
		Training data	Testing data	
15	1.5	8.2e-14	6.3e-14	15
30	1.5	1.0e-14	1.4e-14	30
60	1.5	5.6e-16	4.0e-15	60
120	1.5	4.4e-18	2.7e-15	120
15	3.0	1.0e-14	8.1e-15	15
30	3.0	3.9e-16	4.8e-16	30
60	3.0	2.7e-17	9.4e-17	60
120	3.0	1.1e-18	1.6e-16	120
15	6.0	2.0e-15	1.7e-15	15
30	6.0	1.3e-16	1.8e-16	30
60	6.0	1.7e-17	4.6e-16	60
120	6.0	4.3e-18	4.5e-16	120
15	9.0	1.4e-15	1.3e-15	15
30	9.0	1.6e-16	2.1e-16	30
60	9.0	3.6e-17	1.1e-16	60
120	9.0	2.5e-17	9.6e-17	120

The modeled drain currents (for TFT width 160 μm) with all the ANN methods previously discussed are shown in Fig. 3.15. The blue color represents the training data and the red the testing data. In all the I/V plots, the real data refers to measured data from actual fabricated TFTs. In addition, g_m and g_d are presented in Fig. 3.16 (for all regions of transistor operation – linear

Table 3.7: SVM results

No.of Neurons	spread	MSE		Epochs
		Training data	Testing data	
176	4.5	5.3e-17	2.4e-16	9



(a) (b) (c)

Figure 3.15: TFT output characteristics, including training (blue - $0 \leq V_{GS} \leq 10\,V$ and $0 \leq V_{DS} \leq 15\,V$, in steps of 1 V) and testing data (red - $0.25 \leq V_{GS} \leq 9.75\,V$ and $0.5 \leq V_{DS} \leq 14.5\,V$, in steps of 0.25 V and 1 V, respectively) from: (a) MLP (b) RBF (c) LS-SVM.

to saturation). The mean absolute relative error (MARE) for these parameters are reported in Table. 3.8 and the corresponding network complexity is shown in Table 3.9. MARE is defined as,

$$MARE = \frac{1}{N}\sum_{i=1}^{N}\left[\frac{|I_{Dmes}(i) - I_{Dmodel}(i)|}{I_{Dmes}(i)}\right], \tag{3.7}$$

where $I_{D\,mes}(i)$ and $I_{D\,model}(i)$ refer to the measured and modeled drain current respectively.

Table 3.8: MARE of small signal parameters from all the ANN modeling methods

Operating region	g_m			g_d		
	MLP (%)	RBF (%)	LS-SVM (%)	MLP (%)	RBF (%)	LS-SVM (%)
Linear	1.4	1.6	1.2	3.4	4.8	2.3
Saturation	0.7	1.45	0.4	5.5	6.2	2.5

Table 3.9: Number of neurons in the ANNs hidden layer

MLP	RBF	LS-SVM
15	60	176

These results show that when a single transistor is considered, under the same training conditions, LS-SVM performance is the best, but its complexity is the highest, whereas RBF shows relatively less performance among the three methods. On the other hand, MLP shows good accuracy with minimal complexity, similar to the MOSFET case. Since the MLP reveals the lower

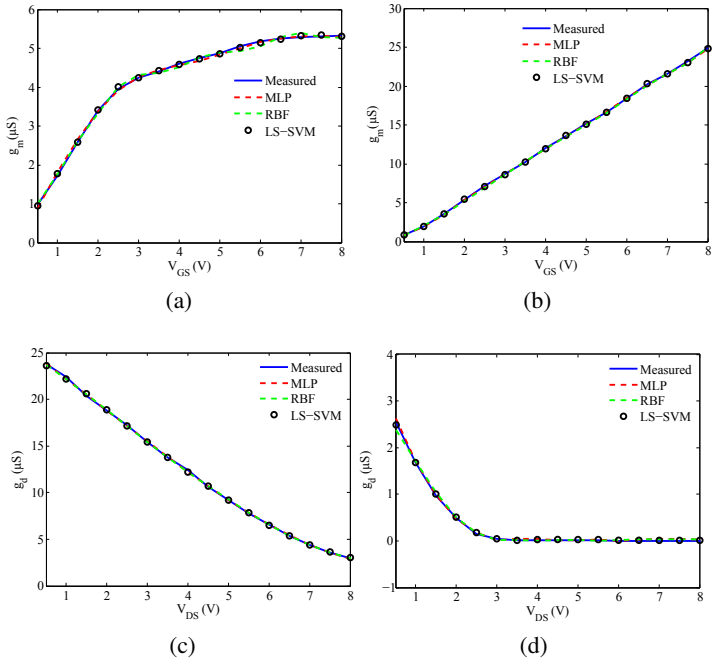


Figure 3.16: Small signal parameters (a) g_m : when V_{DS} = 1.5 V (b) g_m : when V_{DS} = 10 V (c) g_d : when V_{GS} = 8 V (d) g_d : when V_{GS} = 1.5 V

complexity of all the networks, the price to pay for a relatively lower accuracy is well compensated by the lower simulation time. Accordingly, MLP was extended for multiple TFTs with different widths (10, 60, 80, 100, 120, 160, 180, 220, 260, 300 and 320 μm) and then the network implemented in Verilog-A for circuit simulations.

3.5.2 Verilog-A Neural Model Results

Verilog-A is a high-level language, with which the analog behavior of a component or a system can be described [108]. This language is supported by many commercial CAD simulators. Generally Verilog-A modules consist of ports (either to apply stimulus or to acquire response of the circuit/system), parameters (used to pass circuit component information to the model ex: temperature or resistance) and analog blocks (a set of procedural statements that describe the analog behavior). A model can then be implemented in Verilog-A by emulating the current in the transistor with a functional current source. In the present case, the current is defined by the MLP function. The input parameters of the model will be V_{GS}, V_{DS}, in the form of circuit nodes. The other physical parameter is the width of the transistor. Figure 3.17a shows the result of a simple experiment with the implemented model. The I/V characteristics of a TFT, with a width of 200 μm are generated from the Verilog-A ANN model using Cadence Spectre simulator. It should be underlined that the generated data is for a transistor that was not part of the transistor set that constituted the training data. The simulation results are compared with the measured data, as shown in Fig. 3.17a, collected from an I/V measurement setup as shown in Fig. 3.17b. In Fig. 3.17a, V_{DS} is varied from

0.5 to 14.5 V in steps of 0.5 V; V_{GS} is varied from 2 to 10 V in steps of 1 V. From these results it can be understood that the network is capable of predicting the I/V relation for any aspect ratio that lies within the training range, and that the model can successfully be used in an electric simulator.

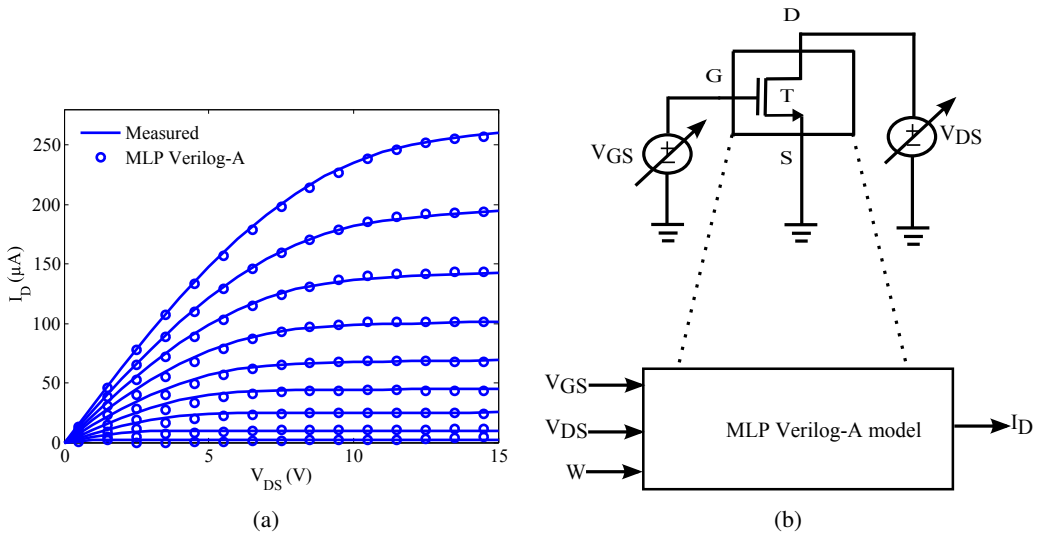


Figure 3.17: Verilog-A ANN model (a) TFT output characteristics ($2 \leq V_{GS} \leq 10$ V and $0.5 \leq V_{DS} \leq 14.5$ V, in steps of 1 V) (b) Test setup

Some other insights can be taken from the simulation (Verilog-A) and measurements to further attest the validity and ability of the model to capture the major characteristics of the device. The threshold voltage, V_{TH}, of the TFT can be calculated either from the simulated data using the developed Verilog-A model or from the measured data as shown in Fig. 3.18a.

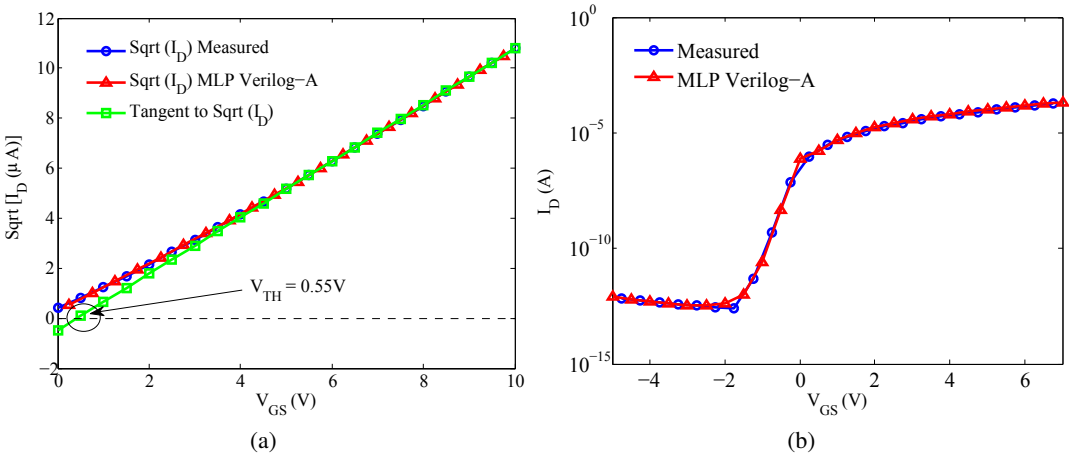


Figure 3.18: (a) Threshold voltage (V_{TH}) calculation from the measured and simulated data (using the Verilog-A model — example with the 80 μm TFT) (b) Measured and modeled transfer characteristics of transistor whose width is 320 μm

Fig. 3.18b exhibits a very good agreement between measured and simulated transfer charac-

teristics of a TFT at V_{DS} 15V, with a width of 320 μm,. These results reinforce the validity of the model in the complete region of operation. However, a separate network has been used to represent the region where $V_{GS} \leq 0\,V$, because the current in the cut-off region spreads over several orders of magnitude. Nevertheless, one should note that the model is built with the intention of designing analog circuits, where generally, $V_{GS} \geq 0\,V$.

3.6 Dynamic Modeling

In literature the typical use of ANNs for modeling transistors has mostly been demonstrated for static behaviour [91, 107, 109, 110, 111]. Nevertheless, EC approaches with ANNs have been used before for microwave devices [112], and also dynamical neural networks in a form of TDNNs (time delay neural networks) have also been widely used in behavioral modeling of RF power amplifiers [113, 114]. Typically a TDNN is a static MLP (feedforward network) with a tap delay line at the input, which basically works as a sliding window that retains the recent past of the signal. It is the memory that brings dynamics to the MLP. But normally in this approach the training data (from measurements) needs to be carefully set in order to span over the dynamics of the device, with appropriate signals that should capture the bandwidth of use. The EC model (Fig. 3.1) simplifies this setting by allowing the normal use of a static ANN. The dynamics is brought into the model in the sense that the network will learn the charge dynamics through a nonlinear capacitor characterization, although in this approach the capacitor value is assumed not to change with the signal frequency. So, up to now the ANN models were developed for static behavior characterization of the TFT. To complete the EC model, the bias dependent capacitors (C_{GD} and C_{GS}), responsible for the dynamics, need also to be modeled. By these means, the complete model will be ready to be used for transient (large signal) or ac (small signal) analysis. Based on the arguments provided for selecting the model, C_{GD} and C_{GS} will also be represented by ANNs, in a similar way as done with I_D.

As with static modeling, MOSFETs have also been chosen to attest first the proposed method. Since the MLP has proven to be a suitable technique that results in a simple model with reasonable good accuracy, the modeling of C_{GD} and C_{GS} will also follow the same approach.

3.6.1 MOSFET Dynamic Modeling

In the EC model (Fig. 3.1), the transistor dynamics is represented by the gate to channel capacitor. This is, in fact, a distributed capacitor. However, given the low frequency bandwidth expected from TFT devices, a lumped representation with two terminal capacitors is a reasonable approximation. In order to verify the method, the same MOSFET used during the static characterization is repeated here, C_{GS} and C_{GD} are obtained by sweeping V_{GS} and V_{DS} in the range of 0 to 3 V and 0 to 3.3 V in steps of 0.1 V. Then, separated MLPs are developed for each of the capacitors. In this case the target data for the network is log-scaled a priori to minimize the spread of measured values. After the training phase is finished, the network output is re-scaled back in order get the actual values of the capacitors. Fig. 3.19a and 3.19b show the performance of the networks in terms of mean

square error (MSE). It can be noticed that if a small network, i.e. with very few neurons in the hidden layer, is chosen, then a poor performance results. On the other hand, if high accuracy is the sole parameter for selecting the best network, then higher complexity will result. In order to implement the ANNs in Verilog-A, a trade-off between accuracy and complexity was in play. The final selected networks are marked in Fig. 3.19.

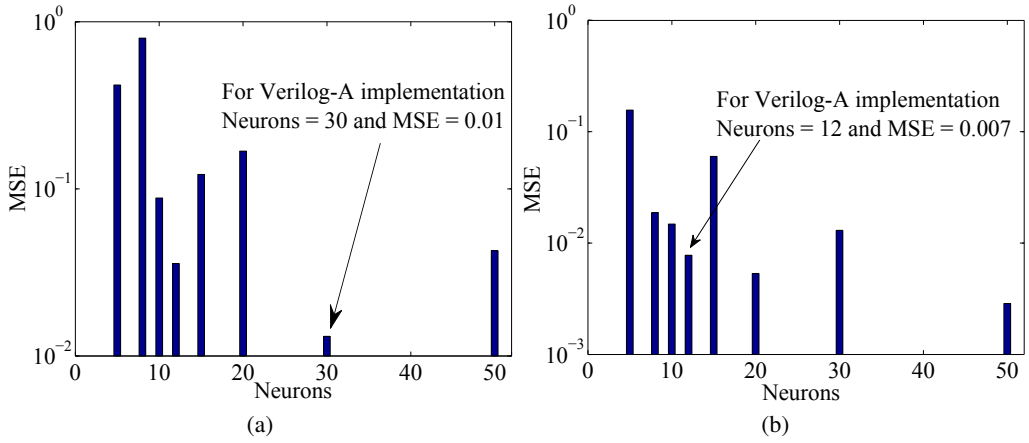


Figure 3.19: ANN performance and complexity (number of neurons): (a) C_{GD} (b) C_{GS}

The ANN and BSIM3V3 models for C_{GD} and C_{GS} will now be compared using Cadence Spectre simulator, under similar bias conditions. For testing purposes, and to check the generalization ability of the network, new data was generated for C_{GD} and C_{GS}. For this purpose, the capacitor values were found with input voltages, V_{GS} and V_{DS}, varied from 0.05 to 2.95 V and 0 to 3.3 V in steps of 0.1 V, respectively. Fig. 3.20a and Fig. 3.20b show that ANN model response is in good agreement with the BSIM3V3 model response even for the testing data, which demonstrates the generalization capability of the network.

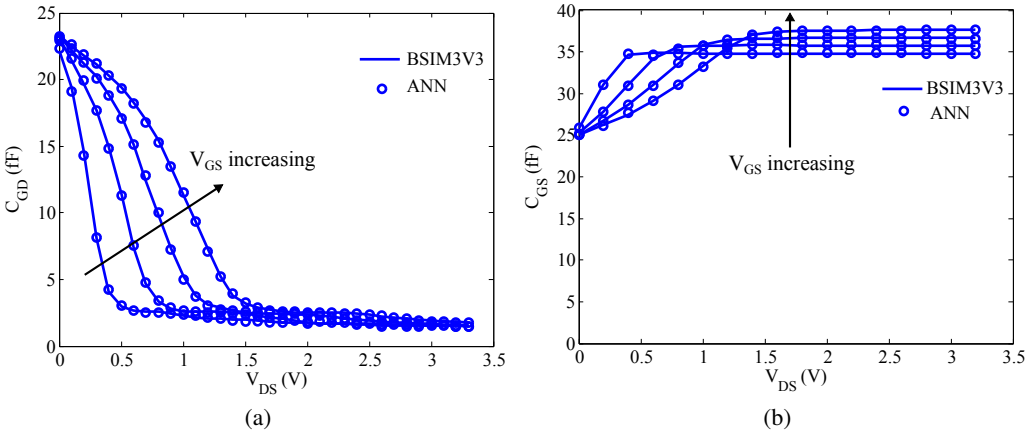


Figure 3.20: MLP modeling results for the bias dependent capacitances : $0.05 \leq V_{GS} \leq 2.95$ V and $0 \leq V_{DS} \leq 3.3$ V, in steps of 0.1 V (a) C_{GD} (b) C_{GS}.

3.6.2 TFT Dynamic Modeling

Similar to MOSFET, the TFT static model (that was developed in section 3.5) should be extended to predict the device dynamical behavior in circuit simulations. The procedure implies a characterization of the parasitic elements (C_{GD} and C_{GS}), given that the model is developed from measured characteristics. The validation of the model, with an actual circuit response, will be given at the end of the chapter, from a simple common source (CS) amplifier. The following sections explain the intrinsic capacitance characterization and the resulting complete model.

3.6.3 TFT Capacitance Characterization

The total gate capacitance of an a-GIZO TFT (with shorted drain and source electrodes, as shown in Fig. 3.22a), at different frequencies, has been previously reported in [115]. Results reveal that the total capacitor value does not change significantly with the signal frequency. Supported on this claim, the following characterization assumes no dependency of the capacitor with frequency, which means that the nonlinear capacitor values can be represented by a static ANN.

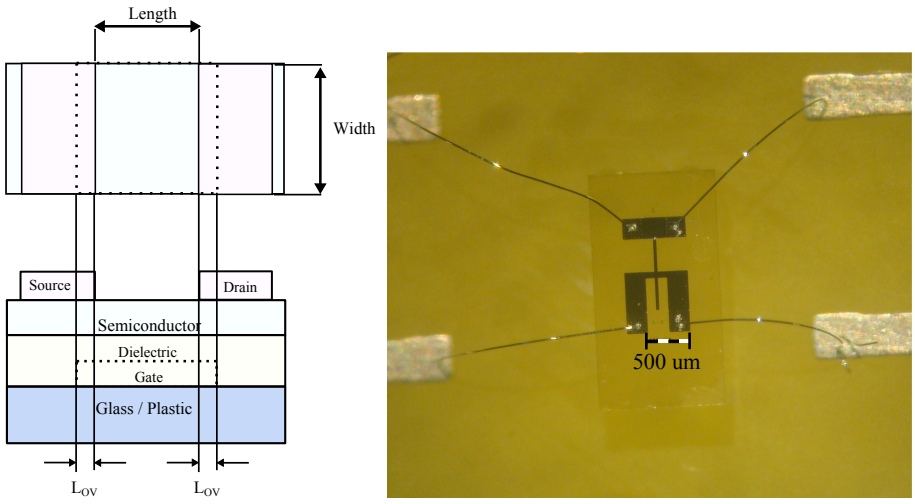


Figure 3.21: (a) Schematic view of the a-GIZO TFT fabricated in this work. Channel length L = 20 μm, and channel width W = 640 μm. L_{OV} represents source/drain overlaps to the gate (5 μm for each side) - figure dimensions are not as per scale (b) Fabricated TFT with wire-bonding

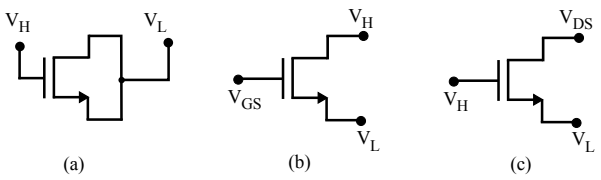


Figure 3.22: Capacitor measurement setup (a) $C_{G\text{-}DS}$ (b) C_{GD} (c) C_{GS} + C_{GD}

In addition to the total gate capacitance ($C_{G\text{-}DS}$), intrinsic capacitances (C_{GDi} and C_{GSi}) between different electrodes of the a-GIZO TFT are experimentally measured at different bias voltages. All these measurements are presented for a TFT with W = 640 μm, L = 20 μm and L_{OV} = 5 μm, as an example. The TFT schematic and its fabricated circuit with wire-bonding are shown in Fig. 3.21. For the above listed capacitor components, the measurement test setup is shown in Fig. 3.22. The measurements were carried out with a PM6306 LCR meter.

$C_{G\text{-}DS}$ Measurement: The test setup shown in Fig. 3.22a is used to measure $C_{G\text{-}DS}$, in which the gate terminal is connected to the high voltage node and the shorted source-drain terminal is connected to the low voltage node (ground) of the LCR meter. At the gate terminal, a small signal is superimposed on the bias voltage (V_{GS}). When V_{GS} is very small, no accumulation channel is formed in the semiconductor. Consequently, the resulting capacitor is the sum of the overlap values between gate to source ($C_{OV\text{-}GS}$) and gate to drain ($C_{OV\text{-}GD}$). In our transistors, the overlap area between gate to source is the same as gate to drain, so $C_{OV\text{-}GD} = C_{OV\text{-}GS}$. As V_{GS} increases, a conduction channel will form close to the semiconductor and dielectric interface. Once the channel is formed, the total capacitance will correspond to the sum of the overlap capacitances and the channel capacitance (C_{CH}). For the TFT shown in Fig. 3.21b, the gate capacitance at different frequencies is presented in Fig. 3.23. From this plot, it can be noticed that the total overlap capacitance ($C_{OV\text{-}GS}$ + $C_{OV\text{-}GD}$) is $\approx$ 6.4 pf and C_{CH} is $\approx$ 3.3 pf. This result supports the assumption for capacitive independence with frequency, except for the subthreshold region. But even here, the change is around 15% within a decade span in frequency, a variance that is probably well within the technology tolerance.

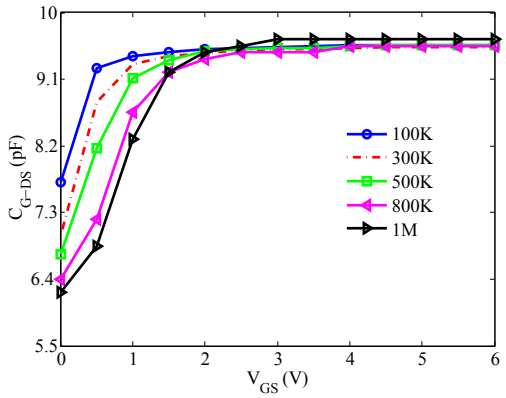


Figure 3.23: Measured $C_{G\text{-}DS}$ at different frequencies for a gate voltage sweep from 0 to 6 V

C_{GDi} Measurement: The test setup shown in Fig. 3.22b was used to measure C_{GD}. A small signal (with frequency = 300 KHz and amplitude = 100 mV) is applied at the drain terminal, which is connected to the high voltage node of the LCR meter, while the source terminal is connected to the low-voltage. Bias voltages at the gate are swept between 0 to 6 V in steps of 1 V, whereas the voltage at the drain terminals are swept in the range of 0 to 10 V in steps of 0.5 V. The intrinsic bias

capacitance between gate and drain (C_{GDi}) is shown in Fig. 3.24, which is obtained by subtracting $C_{OV\text{-}GD}$ from the measured C_{GD}.

C_{GSi} Measurement: Finally, the test setup shown in Fig. 3.22c is used to measure C_{GS}. A small signal superimposed on the gate bias voltage is applied at the gate terminal, which is connected to the high voltage node of the LCR meter. The source terminal is connected to the low-voltage node of the of the LCR meter. The dc bias voltage is applied to the drain terminal. The small signal frequency and bias voltages are the same as for the C_{GDi} case. In fact, this measurement will result in the total gate capacitance, $C_{GD}+ C_{GS}$, for the applied bias voltages. By subtracting C_{GD} and the overlap capacitance ($C_{OV\text{-}GS}$), the intrinsic capacitance between gate and source (C_{GSi}) is obtained, which is shown in Fig. 3.24. Interesting enough, the C_{GSi} and C_{GDi} measurements are in agreement with Meyers FET capacitive model [116] i.e., in the linear region $C_{GSi} = C_{GDi} \approx \frac{1}{2}C_{CH}$ and in the deep saturation, $C_{GSi} \approx \frac{2}{3} C_{CH}$ and $C_{GDi} \approx 0$.

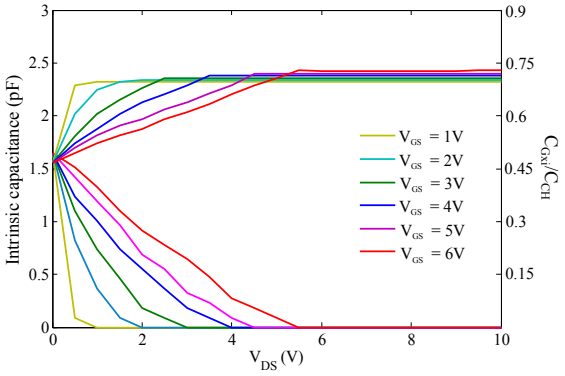


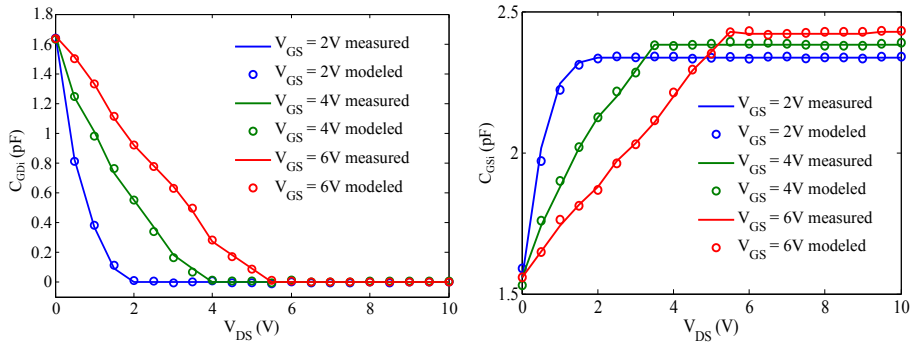
Figure 3.24: C_{GSi} and C_{GDi} measurements validation with Meyers FET capacitance model

3.6.4 TFT Bias-Dependent Capacitor Modeling

The above measured values of the bias dependent capacitors are now used to develop the neural model, in a similar fashion as performed with the I_D static modeling. The network performance (MSE), with respect to its complexity in terms of the number of neurons, is shown in Table.3.10, for both C_{GDi} and C_{GSi}. As a trade-off between accuracy and overfitting, a network with 10 hidden neurons was employed for both cases. The measured and verilog-A model responses are presented in Fig. 3.25, where the outcome of the model shows a good agreement with the measured data with a MARE of 8% and 6% for C_{GD} and C_{GS} respectively. Meyers approximation of the intrinsic capacitances (C_{GDi} and C_{GSi}) are presented in Fig. 3.26. Model validation with this approximation (for the intrinsic capacitors) is also presented in the next section.

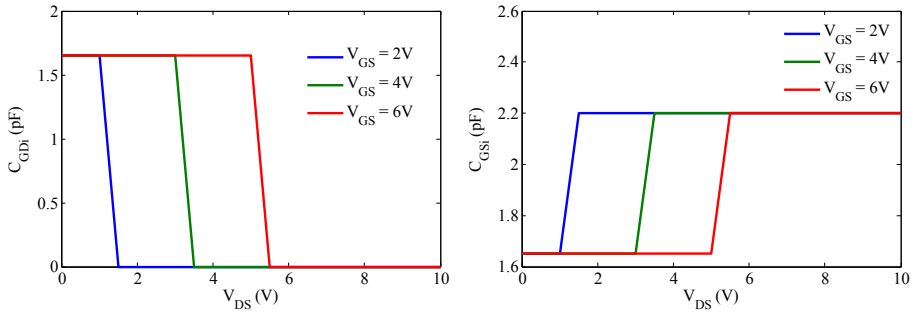
Table 3.10: MLP results for the bias dependent intrinsic capacitances

No.of Neurons	C_{GDi}		C_{GSi}	
	MSE	Epochs	MSE	Epochs
5	3.74E-03	15	2.15E-04	106
10	5.12E-04	12	5.0E-04	24
15	3.94E-04	13	9.56E-05	25
20	4.81E-04	19	5.51E-05	8
30	1.34E-04	15	4.55E-05	10
40	5.32E-05	40	1.98E-05	15
50	4.29E-06	10	8.75E-06	9



(a) (b)

Figure 3.25: Measured and modeled intrinsic capacitances (a) C_{GDi} (b) C_{GSi}



(a) (b)

Figure 3.26: Meyers approximation of the intrinsic capacitances (a) C_{GDi} (b) C_{GSi}

3.7 TFT Model Validation

For further validation of the final model, a simple common source (CS) amplifier was designed based on simulations that are to be confronted with the real circuit measurements, whose schematic is shown in Fig. 3.27a. The real circuit was made out of two isolated wire-bonded transistors, as shown in Fig. 3.27b. This circuit has a load of 4 pF (minimum input buffer capacitance), that was taken into account during simulations. All the transistors in the circuit have the same channel

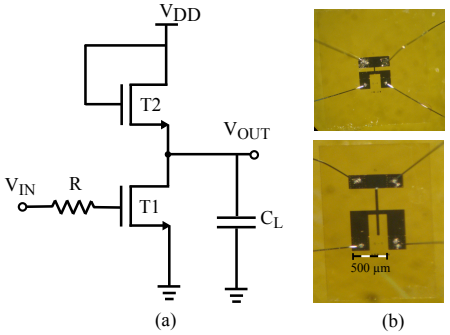


Figure 3.27: (a) CS amplifier schematic with $W_{(T1)} = 640\,\mu$m and $W_{(T2)} = 40\,\mu$m (b) Micrographs of the TFTs that are used to form the CS amplifier.

length ($20\,\mu$m). The frequency response of the circuit is shown in Fig. 3.28a with different values of resistor R ($0\,\Omega$, $100\,\text{K}\Omega$ and $1\,\text{M}\Omega$). This amplifier resulted in 13.3 dB gain $\left(20log\sqrt{\frac{W_{T1}}{W_{T2}}}\right)$, as expected. The circuit transient response is presented in Fig. 3.28b and the transition part is magnified to emphasize the model ability in predicting the dynamic behavior of the device. Then, the circuit is characterized for an input signal of the form: $1.5 + 0.5\sin(2\cdot\pi\cdot 100\text{k}\cdot t)$, with $V_{DD} = 6\,\text{V}$. Fig. 3.29 shows the output and the error signals (taken as the difference between the measurement and simulation) for the above mentioned test setup. The MARE of the signal output is 2.5%. The THD calculated from the simulated result and measurements is 14% and 11.2%, respectively. All these results demonstrate that the model is able to capture well the small and large signal behavior of the device including nonlinear effects of the intrinsic capacitance.

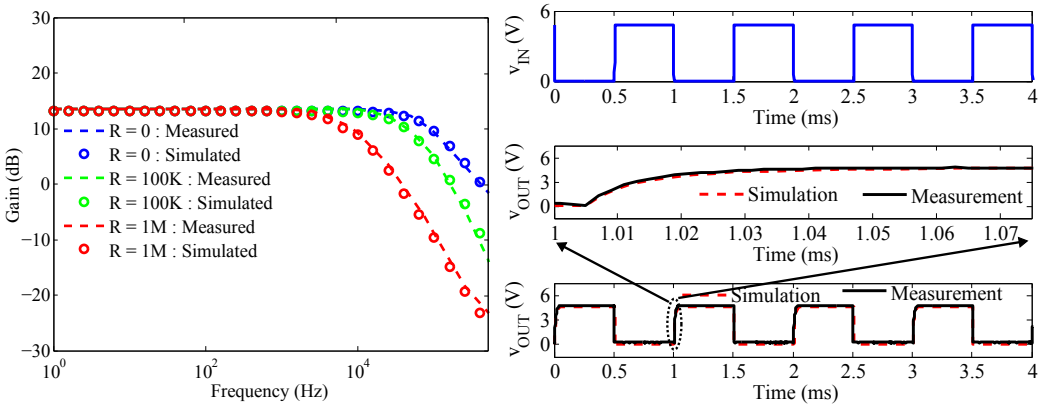
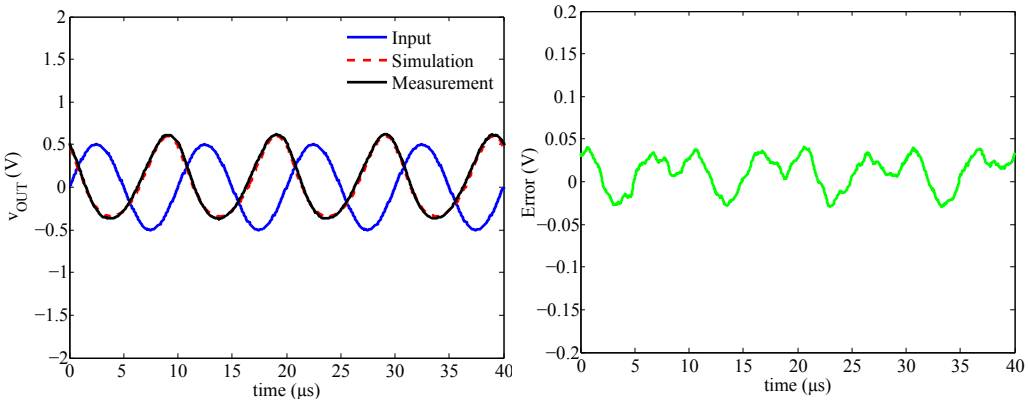


Figure 3.28: CS amplifier response with 4 pF load : (a) Frequency response with different values of R (b) transient response for 1 KHz input signal frequency - transition part is zoomed to show the model accuracy in predicting parameters that are responsible for the dynamic behavior.

In order to understand if further simplification to the model could be included, without creating a great impact of the final accuracy, the same CS amplifier was simulated again, but now taking the Meyers approximation presented in Fig. 3.26, for the intrinsic capacitors. The simulated responses



(a) (b)

Figure 3.29: CS amplifier response form the proposed model and measurements, when the input signal frequency is 100 KHz (a) Output (b) Difference between the measured and simulated response.

from both ac and transient analysis and measurements can be found in Figs. 3.30 and 3.31.

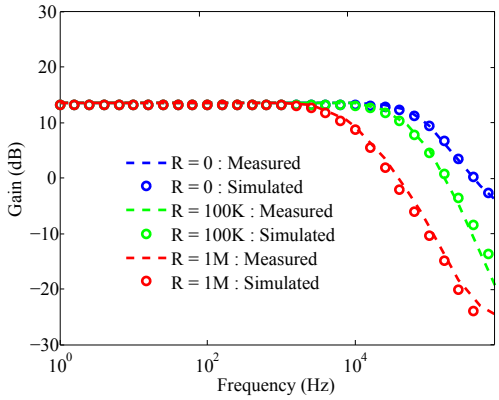
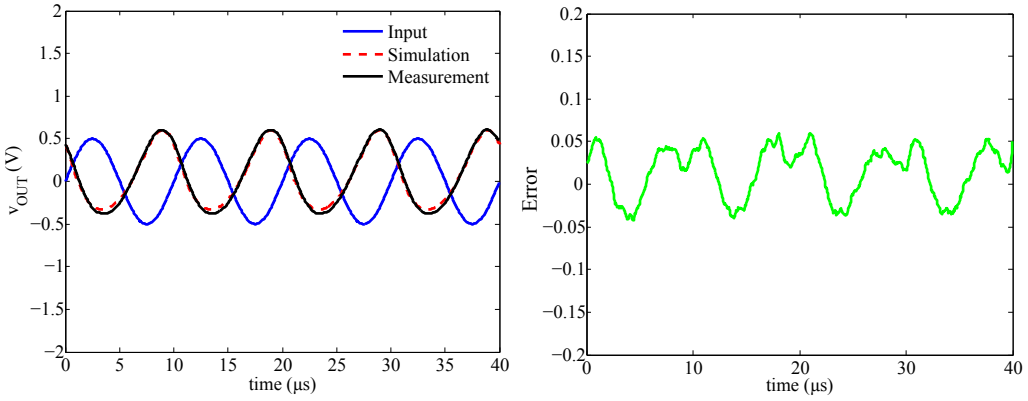


Figure 3.30: CS amplifier ac response form the Meyers model and measurements.

Table 3.11: Dominant pole location from simulation and measurement

	Frequency (KHz)		
	R = 0	R = 100 KΩ	R = 1 MΩ
Simulation (EC)	84	44	7.5
Simulation (Meyers)	82	41.2	7
Measurement	85	45	8

The dominant pole locations and the THD from simulations (EC and Meyer models) and measurements are all listed in Table. 3.11 and 3.12. The MARE of the error signal with the Meyer model is 3% (whereas MARE of the error signal from the EC model simulation is 2.5%). These results reveal that the Meyers model performance stands very close to the proposed model. The main advantage of using the Meyers model is the final lower complexity that is accomplished



(a) (b)

Figure 3.31: CS amplifier response form the Meyers model and measurements, when the input signal frequency is 100 KHz (a) Output (b) Difference between the measured and simulated response.

Table 3.12: THD from simulation and measurement

THD	
Simulation (EC)	14%
Simulation (Meyers)	16%
Measurement	11.2%

when compared to the ANN, which results in fewer computations. Given the fact that the accuracy is not dramatically compromised, the Meyers model will be adopted in the coming chapters for circuit simulations. It should be noted that this is done just for the case of transistors operating in the saturation region, which will be the majority of the cases.

Chapter 4

Basic Building Blocks for a-GIZO TFT IC Design

This chapter focuses on the design and characterization of basic analog/mixed circuit blocks that are important for signal processing and conditioning. It includes logic gates (inverter, two-input NAND, NOR and XOR), half-wave rectifier and peak detector. In addition, current mirrors, single stage amplifiers (both single ended and differential), signal processing circuits, namely, subtractor, adder and multiplier, are also characterized. Novel high-gain topologies are proposed in order to overcome some of the technology limitations. Most of these circuits are analyzed from both simulation (using the developed model) and measurements.

4.1 Introduction: Basic AOS Circuits

As discussed in section 2.4, low intrinsic carrier mobility (compared to crystalline devices), lack of a stable complementary device (p-type), bias stress, unavailability of accurate device models and technology libraries that can support typical IC design with a-GIZO TFTs are the main detrimental factors that make circuit design a quite challenging task. However, as referred earlier, the level of performance attained by a-GIZO enables the integration of these devices in drivers on display backplanes, resulting in yield improvement and reduction of overall production costs. Therefore, it is not surprising to find that most of the technical articles are focused on the development of driving circuits [117, 118] and ring oscillators [36, 119]. Logic circuits, such as an OR gate operating at 10 Hz [120], NAND and NOR gates operating up to 5 kHz have been reported, but fabricated at temperatures that round about 600 °C [121]. All circuits proposed in this dissertation, however, were fabricated at room temperature, and annealed to temperatures lower than 200 °C. It represents a leap towards very low-cost circuit fabrication and the next sections will assess its effectiveness for the design of fundamental blocks, such as logic gates.

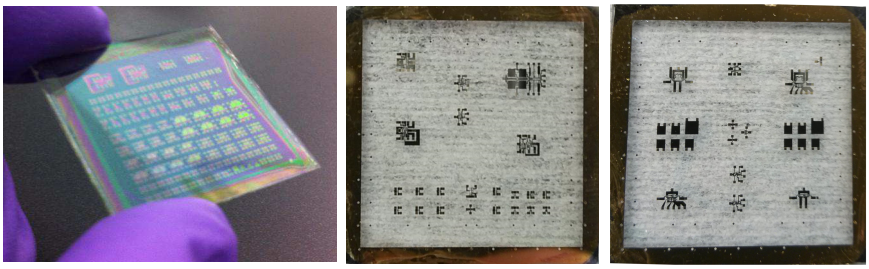
Limiting the application of AOS emerging technologies to switching pixels and back plane drivers (and logic circuits) is somehow a reductionist view. The unique properties of a-GIZO, such as low-temperature fabrication, relatively high mobility and transparency are stimulating a slowly

but steadily expansion of the technology to more diverse application areas. An example is the RFID tags where strong reductions in costs could be expected [1]. Rectifiers play a fundamental role in passive RFID tags for harvesting the power from the RF signals. A full wave rectifier with four TFTs using either indium gallium oxide (IGO) or zinc tin oxide (ZTO), with a fabrication temperature of 400°C, is demonstrated in [122]. Aiming to understand the effectiveness of a-GIZO for this purpose, a single TFT will be tested in a peak-detector circuit and in a half-wave rectifier. The current mirror is another important functional block, frequently used in analog circuit design, providing bias, acting as active loads and as pixel driving circuits in OLED displays [8] – very important in the last because current mirroring mitigates, in good extent, the effects of threshold-voltage drifts. ZTO TFT-based current mirrors, using metallic electrodes, have been already reported in the past, however it requires a high post-processing temperature of around 400°C [123]. In subsequent sections, simple transparent current mirrors with two TFTs having different mirroring ratios, with and without a passive load, as well as a cascode current mirror processed at low-temperatures, will be presented to attest that low-temperature a-GIZO devices can also achieve good performances in this respect.

High-gain amplifiers are basic building blocks in analog or mixed-signal IC design. Although a few steps have been made towards designing amplifiers with a-GIZO, such as in [30], the number and complexity of circuits found in the literature is still small, and with relatively low gain levels (18.7 dB in [30]). In order to better understand the limitations that a-GIZO may pose to the design of generic amplifiers, some fundamental topologies belonging to different sections of multistage amplifiers are also characterized, such as a single-stage single-ended common-source (CS), common-drain (CD – source follower or level shifter) and the differential pair. A capacitive bootstrapping amplifier is also presented, and based on this topology a novel high-gain amplifier is proposed. Up to the date, this topology in indeed promising the highest gain ever reported with the technology in question. Other signal processing circuits were also designed and tested, namely, an analog subtractor and adder based on an a-Si:H TFT [22] circuit, and a novel circuit is proposed, which can add or average the input signals. Higher-order processing circuits, including the design of multipliers [111], and the inclusion of positive feedback for gain improvement is also a subject of study in the following sections.

4.2 Basic Analog/Mixed Signal Building Blocks

The results found from measurements made with the circuits listed above, and analyzed below, come from three different chips fabricated on $2.5\times2.5\,\text{cm}^2$ glass substrates (the fabrication details can be found in section 2.6), as shown in Fig. 4.1. These chips contain the basic analog/digital circuits and isolated active and passive elements. The simpler circuits were measured with a probe station together with a semiconductor parameter analyzer when appropriate. However, for more complex designs, the chip was diced to individual circuits, followed by wire-bonding to allow a more flexible testing. Having in mind a minimum (total) overlap between gate-drain/source of $10\,\mu$m, all the TFTs were set with a (minimum) channel length (L) of $20\,\mu$m to minimize the



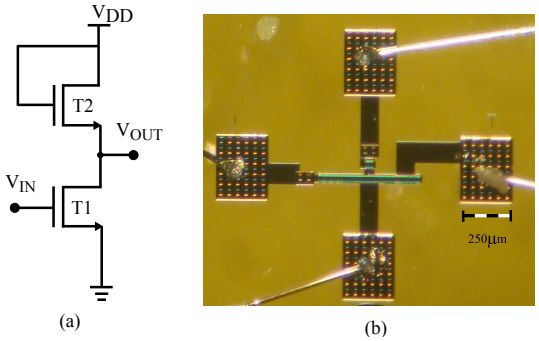
(a) (b) (c)

Figure 4.1: Fabricated circuits on glass substrate.

contact effects over the transistor operation. Different materials were employed for electrodes in different IC runs. Especially in those cases where the circuit complexity demanded wire-bonding, the material of choice was either Ti/Au or Mo. In other cases the electrodes were with IZO.

4.2.1 Logic Gates

Inverter: A simple inverter was designed with a diode connected load. The schematic and respective micrograph, with wire-bonding, are shown in Fig. 4.2. The driving transistor (T1) has a width of W1 = 480 μm and the diode-connected transistor (T2) a width of W2 = 40 μm. When in operation, if the input voltage (V_{IN}) is set to a low value, T1 is almost turned *off* and nearly no current flows through the device. Consequently, the output voltage (V_{OUT}) approaches to V_{DD}. As V_{IN} gets higher, the drain current increases so thus the voltage drop at T2, which results in a lower V_{OUT}.



(a) (b)

Figure 4.2: Inverter: (a) schematic (b) Micrograph of the inverter (source/drain material is Mo) based on a-GIZO TFTs : T1 dimensions - W = 480 μm and L = 20 μm and T2 dimensions - W = 40 μm and L = 20 μm.

Fig. 4.3a shows the inverter voltage transfer characteristics (VTC), for V_{DD} equal to 5 and 10 V, with the input swept from 0 to 5 V. Owing to the relatively high ratio of transistor widths, an almost full swing of the output voltage is observed (high level $\approx V_{DD}$ and low level $\approx$ 0.15 V). Fig. 4.3b, 4.3c and 4.3d presents the result for a functional verification of the inverter, using square-wave inputs of different frequencies:100 Hz, 1 kHz and 10 kHz, respectively, with V_{DD} =

5 V and a load of 4 pF. Small peaks can be distinguished in the output waveform at instants of time where the input transitions occur, mainly visible with the high frequency signal (10 kHz) . This is caused by charge injection from the transistor gate capacitance.

Transistor intrinsic-capacitors together with the total load capacitance are responsible for the rise and fall times. Since the load transistor possesses less current capability (higher equivalent resistance) and the lower transistor (T1) much higher current driving capabilities (wider transistor), it justifies the much higher rise time than the fall time. Such is a consequence of a design that favours some gain ($\sqrt{\frac{W1}{W2}}$) in detriment of symmetric swings. This analysis is equally valid for the other logic gates presented next.

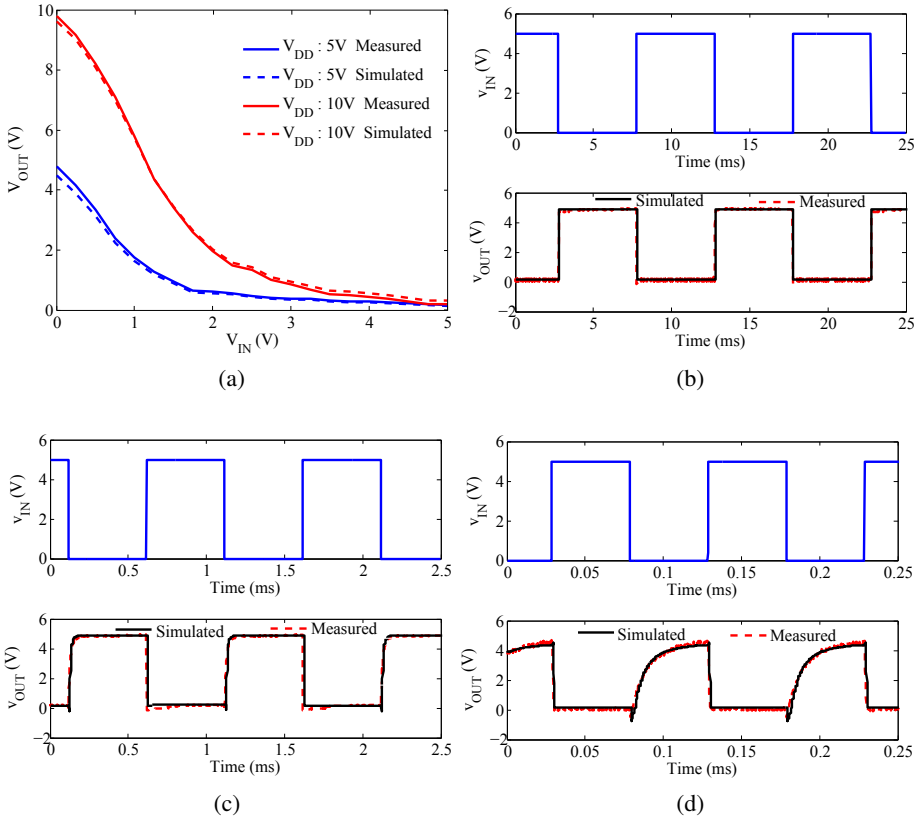


Figure 4.3: Inverter static and dynamic response (a) Voltage transfer characteristics (VTC) (b) input signal frequency: 100 Hz (c) input signal frequency:1 kHz (d) input signal frequency:10 kHz.

NAND Gate: Fig. 4.4 shows a two-input NAND gate schematic together with its fabricated circuit with wire-bonding. Again the width of the diode-connected transistor (T3) is made much smaller than the two driver transistors (T1 and T2). Using a similar reasoning made above with the inverter, if any of the inputs (In1 or In2) is at logic '0', either transistors (T1 or T2) will be cutoff. Then, no current flows in the circuit. The result is in a high output voltage (V_{OUT}), very close to V_{DD}. When both inputs raise to logic '1', T1 and T2 come into conduction, pulling the output to a low voltage (logic '0'), now very close to zero (due to the asymmetry of widths). This expected

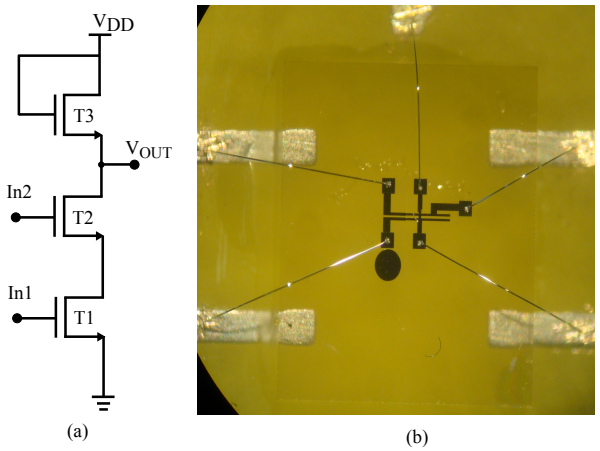


Figure 4.4: Two input NAND gate (a) Schematic (b) Micrograph of the NAND gate based on a-GIZO TFTs : T1 and T2 dimensions - W = 480 μm and L = 20 μm and T3 dimensions - W = 40 μm and L = 20 μm.

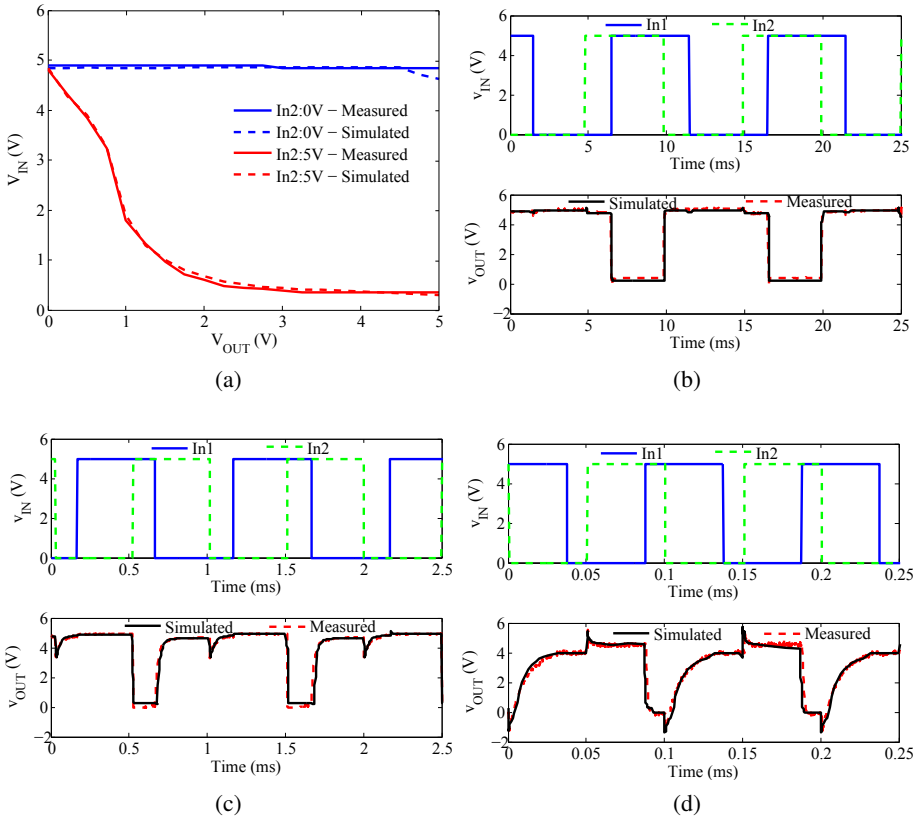


Figure 4.5: NAND static and dynamic response (a) VTC (b) input signal frequency: 100 Hz (c) input signal frequency:1 kHz (d) input signal frequency:10 kHz.

behavior can be observed in Fig. 4.5, from both simulation and measurements, at dc as well as for input signals with different frequencies (4 pF at the load and $V_{DD} = 5$ V). Once more, spikes are observed at higher frequencies (both from measurements and predicted from simulation). The

asymmetric time response is perceivable anew due to unbalancing in transistor sizes.

NOR Gate: This particular circuit was realized with isolated TFTs. Fig. 4.6 shows both the schematic and the used transistors. The widths of the diode connected transistor (T3) and drivers (T1 and T2) are 40 μm and 480 μm, respectively.

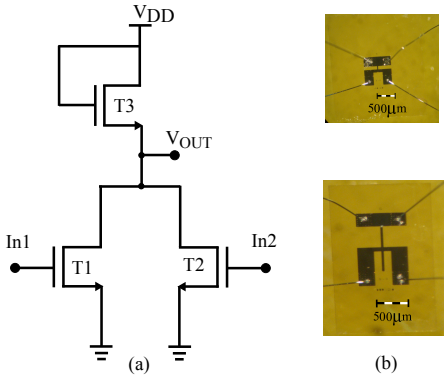


Figure 4.6: Two input NOR gate (a) Schematic (b) Micrograph of the isolated TFTs : dimensions - W = 40 μm and L = 20 μm and T3 dimensions - W = 480 μm and L = 20 μm.

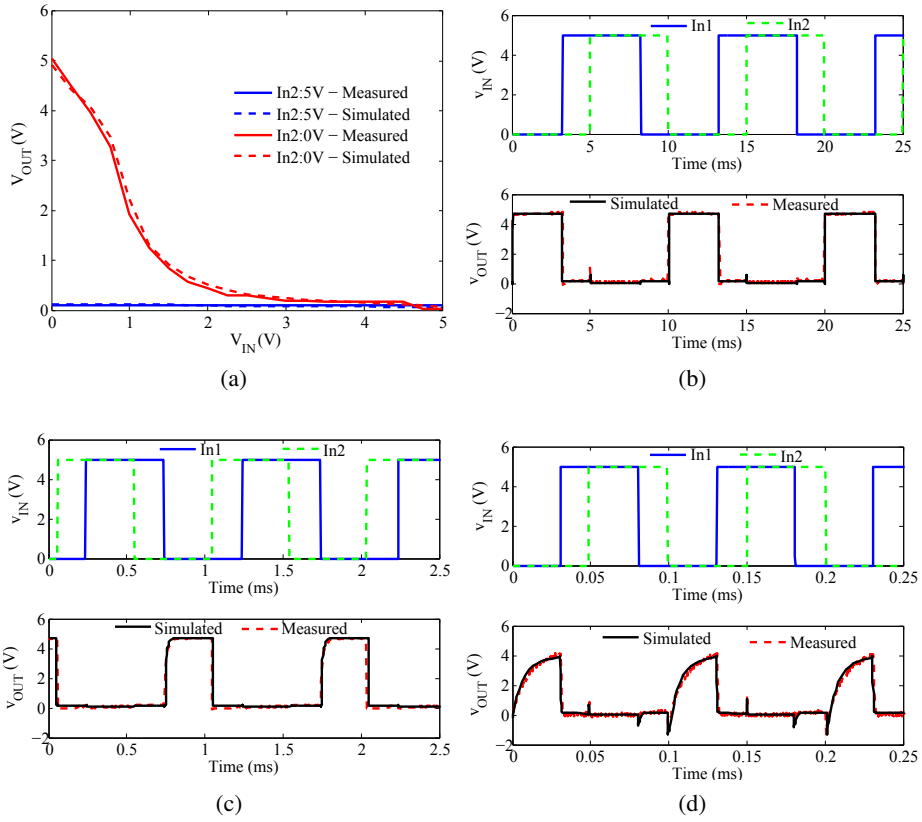
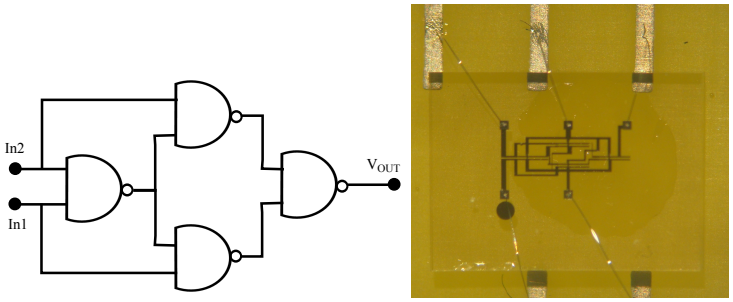


Figure 4.7: NOR static and dynamic response (a) VTC (b) input signal frequency: 100 Hz (c) input signal frequency:1 kHz (d) input signal frequency:10 kHz.

The NOR gate is a dual of the NAND, accordingly, the output is low if any of the inputs (In1 or In2) is set to logic '1', otherwise the output is high. The mechanisms for the voltage swing follows a similar explanation to that given for the previous gates. The expected behavior can be recognized from the analysis of Fig. 4.7, for dc as well as input signals with different frequencies (with a load of 4 pF and $V_{DD} = 5$ V). No surprisingly, spikes at higher frequencies and asymmetric transitions are again observed.

XOR Gate: Fig. 4.8a presents a two-input XOR gate built from two-input NAND gates. Its fabricated circuit with wire-bonding is shown in Fig. 4.8b. For the two-input XOR gate, when one of the inputs is at logic '1', then the expected output is the complemented version of the second input. This behavior can be noticed in Fig. 4.9 (with V_{DD} and the load set anew to 5 V and 4 pF).



(a) (b)

Figure 4.8: Two-input XOR (a) Schematic in terms of two-input NAND gate (b) Fabricated circuit with wire-bonding.

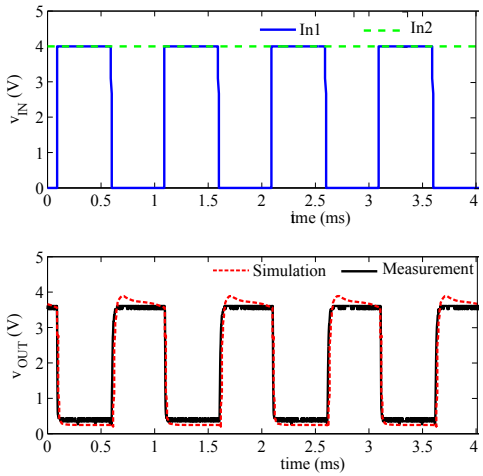


Figure 4.9: Two-input XOR response from simulations and measurements.

4.2.2 Half-Wave Rectifier and Peak Detector

The circuit shown in Fig. 4.10 acts either as a half-wave rectifier or a peak detector, depending if the load (R_L//C_L) is majorly defined by the resistance or else by the capacitor.

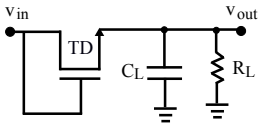


Figure 4.10: Half-wave rectifier or a peak detector.

The diode-connected transistor (TD – W = 70 μm and L = 20 μm) is used to realize a functional diode. During operation, the conductive channel is formed in the semiconductor layer when the gate to source voltage (v_{gs}) is greater than V_{TH}. Lets consider first $R_L \ll \left|\frac{1}{j\omega C_L}\right|$; as the input voltage increases, v_{gs} also increases. In fact, the circuit output (v_{out}) is equal to $v_{in} - v_{gs}$. This explains the lower output voltage in Fig. 4.11a during the positive half-cycle of the input. When the circuit is driven with the negative half-cycle of the input, the roles of the drain and source interchange and v_{gs} will become zero, cutting off the transistor. Therefore, the load is isolated and almost zero v_{out} can be noticed from Fig. 4.11a. Measurements were taken for R_L = 10 MΩ and C_L = 16 pF. In fact the original assumption of resistive load is not respected by the real load, because the capacitor impedance is comparable to that of the resistor (measurement probe), and thus some filtering is still visible at the lower end of the output signal, but not so pronounced at the beginning by virtue of the lower resistance presented by the diode connected transistor to a (practically) fully discharged capacitor. However, this experiment not only shows the rectifying ability of the device but also how the model is capable of capturing both switching and filtering. Nevertheless, the *on* resistance of the transistor is limited by the low mobility, but the behavior is similar to what would be expected from a PN junction diode under identical conditions.

Enforcing now a stronger capacitive load, the circuit becomes a peak detector. During the positive input ($> V_{TH}$), the load will charge to the input peak value, in an ideal case. If the input voltage drops, TD will be turned *off* and, apart from leakage current, C_L will hold the peak value that was previously impressed. For the present experiment, the load is formed by external passive components (R_L = 10 MΩ and $C_L \approx$ 200 pF). The Non-zero R_L causes a slight decay in the output (ripple), as noticed from Fig. 4.11b.

4.2.3 Current Mirrors

Fig. 4.12a and Fig. 4.12b present the schematics of the two-TFT and cascode current mirrors, respectively. Fig. 4.13 shows a picture of fabricated circuits with the two-TFT current mirrors, replicated twice with different current mirroring ratios (by changing the width of T2 – W = 40 μm, 80 μm, and 320 μm). A fingered layout was utilized for the wider transistors (when W $>$ 40 μm) in order to minimize the contact resistance and area. Fig. 4.14 shows the fabricated circuit of the transparent cascode current mirror. For this circuit, all TFTs (T1 to T4) were made with the same width (40 μm).

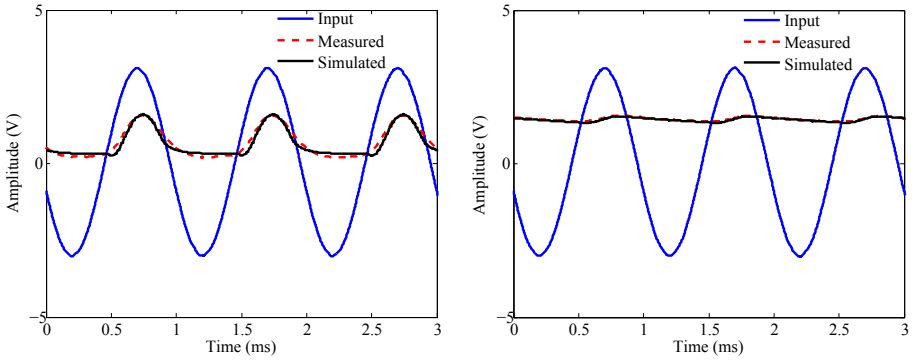


Figure 4.11: (a) Half-wave rectifier response (b) Peak detector response.

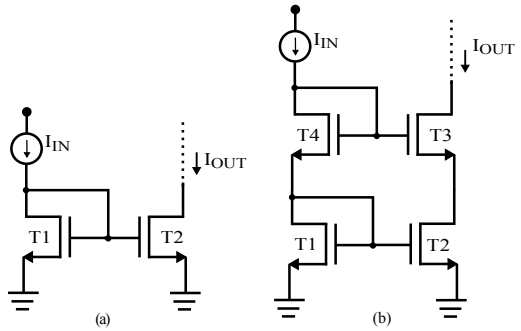


Figure 4.12: Current mirrors schematics (a) Using Two-TFTs (b) Cascode.

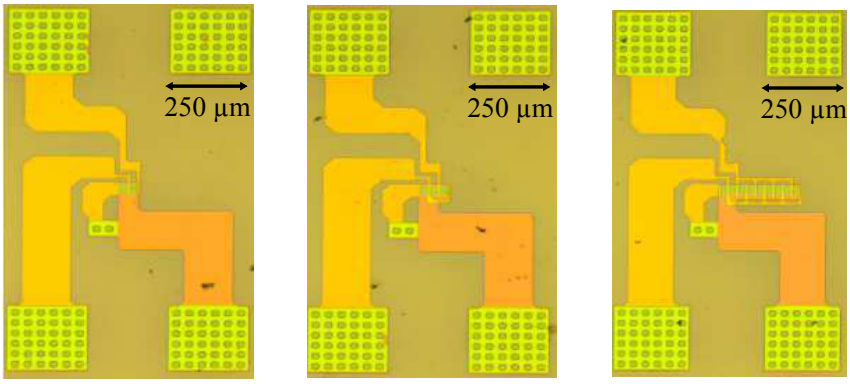


Figure 4.13: Micrographs of transparent two-TFT current mirrors based on a-GIZO TFTs with different widths for the output transistor (T2) in μm : (a) 40 (b) 80 (c) 320.

Ignoring channel-length modulation (λ), due to the long channel-length of the devices, and assuming good matching, the relation between input (I_{IN}) and mirrored (I_{OUT}) current can be expressed (for both topologies) as,

$$\frac{I_{OUT}}{I_{IN}} = \frac{W2(V_{GS}-V_{TH2})^2(1+\lambda V_{DS2})}{W1(V_{GS}-V_{TH1})^2(1+\lambda V_{DS1})} \approx \frac{W2}{W1}, \tag{4.1}$$

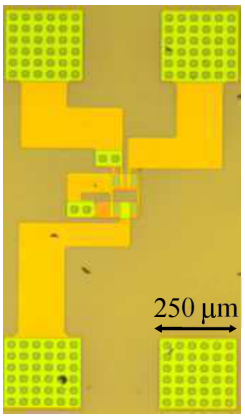


Figure 4.14: Micrograph of the transparent cascode current mirror based on a-GIZO TFTs with W/L = 40/20 μm.

where V_{TH1} and V_{TH2} are the threshold voltages of transistors T1 and T2. Fig. 4.15 shows the results for the two-TFT current mirrors with different mirroring ratios: simulation, expected, and measured responses are plotted (with mismatch removed by offsetting the simulation current). Similar results for the cascode current mirror, at different bias voltages, are shown in Fig. 4.16.

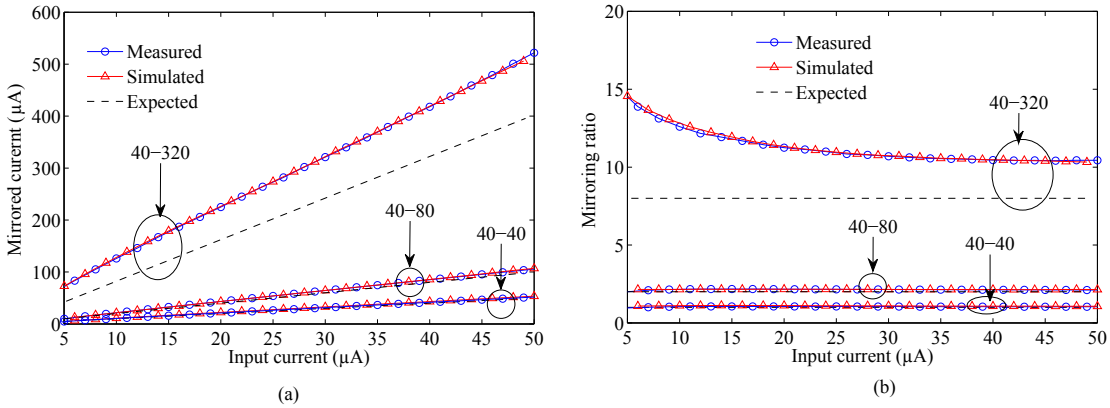


Figure 4.15: Two-TFT current mirror response: expected, from neural model simulation and measured response with fabricated circuits (a) Mirrored current (b) Mirroring ratio.

The average mirroring ratios of all the current mirrors are listed in Table 4.1. Results show good agreement between the metrics (expected, simulated and measured) at lower mirroring ratios, whereas, at higher ratios, a higher mirrored current is obtained. This is related to the output transistor layout. This transistor is designed with fingered layout, which establishes a lower threshold-voltage than would if designed in a direct layout fashion (as discussed in section 2.5 (Fig. 2.13)), meaning that for the same V_{GS}, it drives more current. Nevertheless, the simulator is able to properly capture this behavior. For the 40-320 current mirror, the negative slope in Fig. 4.15b is caused by a threshold-voltage mismatch between the input and output transistors.

The schematic and fabricated transparent two-TFT current mirrors, now with a passive load, are shown in Fig. 4.17 and Fig. 4.18. The resistor is implemented on chip with IZO material, and

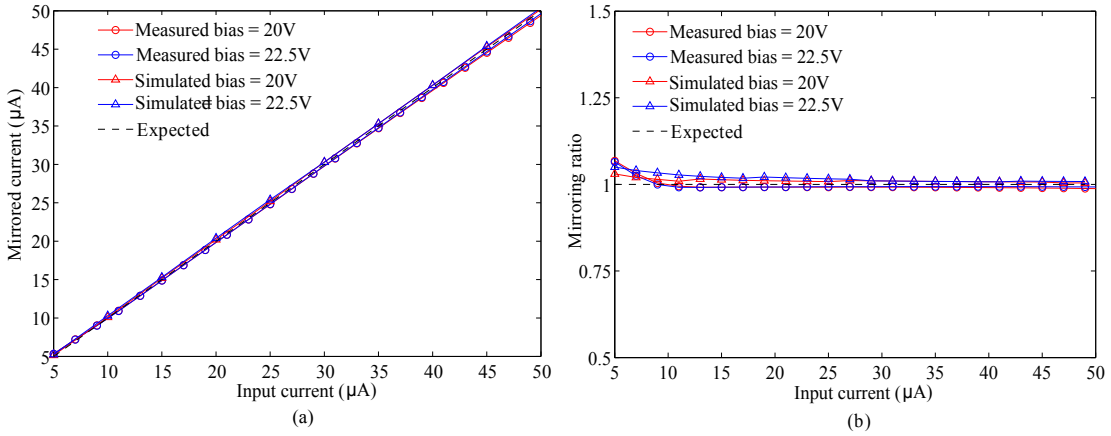


Figure 4.16: Cascode current mirror response at different bias voltages: expected, from neural model simulation and measured response with fabricated circuit (a) Mirrored current (b) Mirroring ratio.

Table 4.1: Mirroring Ratios

	40-40	40-80	40-320	Cas (20V)	Cas (22.5V)
Expected	1	2	8	1	1
Simulated	1.093	2.149	11.43	1.011	1.017
Measured	1.041	2.135	11.7	0.997	0.997

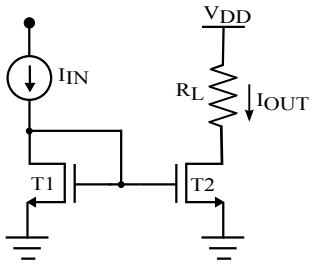
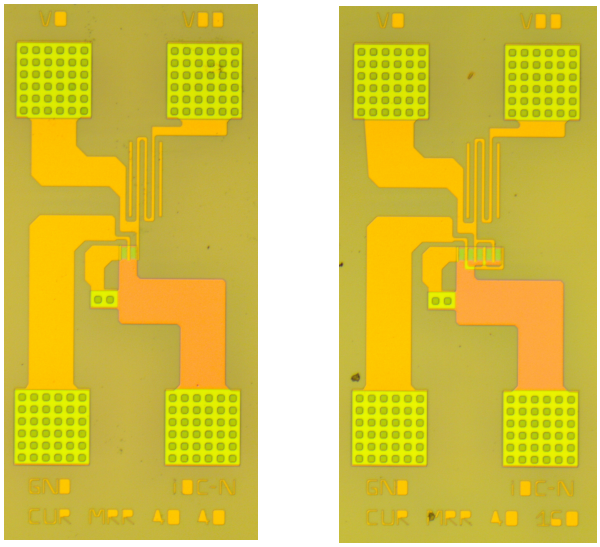


Figure 4.17: Schematic of current mirror with two TFTs and a passive load

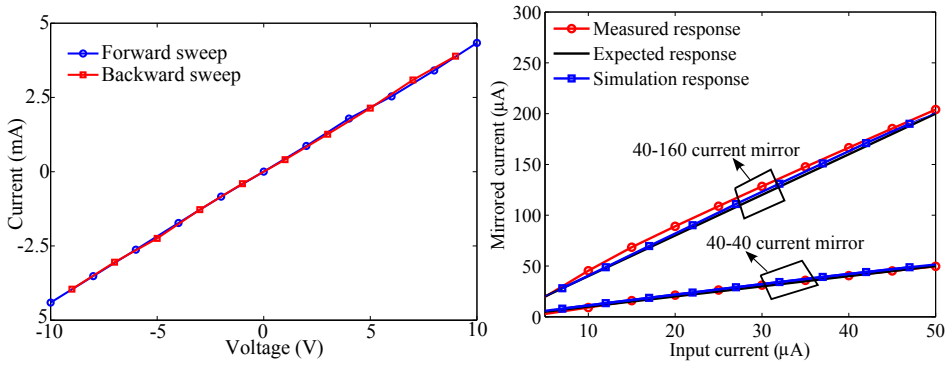
side by side, an isolated resistor was also fabricated for linearity characterization. In Fig. 4.18a, the current mirror is formed with transistors of the same width: $W_1 = W_2 = 40\,\mu$m, while in Fig. 4.18b T1 and T2 have different widths: $W_1 = 40\,\mu$m and $W_2 = 160\,\mu$m.

Fig. 4.19a shows that the designed resistor is extremely linear for a swept voltage between -10 to 10 V. The value for R_L can be found from the slope, and is 2.25 KΩ. In order to test the current mirror operation, the input current is swept from 1 to 50 μA at $V_{DD} = 10$ V, in both simulation and measurement setups. Fig. 4.19b shows the respective circuit responses. From these results, minor mismatches between the simulation, measured and expected behavior can be noticed. The probable causes are the modeling error, noise induced from the IZO contacts that corrupts the data used for the model development and the geometry of the actual device, which definitely is not the same as designed. However, the shift between the actual measurement and predicted by simulation does not exceed 5%.



(a) (b)

Figure 4.18: Fabricated current mirrors with two TFTs with (a) $W_2 = 40\,\mu$m (b) $W_2 = 160\,\mu$m



(a) (b)

Figure 4.19: (a) IZO based resistor characterization (b) Two-TFT current mirrors response with different mirroring ratios: from circuit simulations, measured and expected behavior.

4.2.4 Basic Amplifiers

In this subsection the basic amplifier topologies will be analyzed, namely the common-source (CS) and common-drain (CD) topologies.

Common Drain: The CD amplifier is useful in either shifting the dc level of a signal or as a buffer to drive circuits that have a low input impedance. The circuit schematic and its small signal equivalent are shown in Fig. 4.20.

The relation between v_x and v_1 is given by,

$$\frac{v_x}{v_1} = \frac{g_{m2}}{g_{m2} + g_{ds2} + g_{ds1}}, \tag{4.2}$$

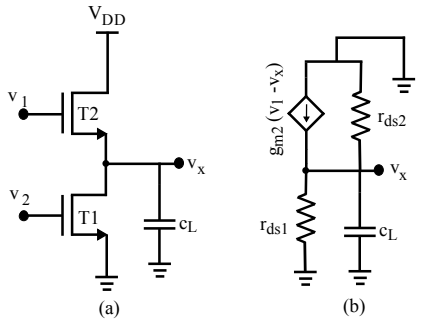


Figure 4.20: CD amplifier (a) Schematic (b) Small signal equivalent.

where g_m and g_{ds} represent the transconductance and output conductance of the transistor. The voltage gain can be made very close to one if $g_m >> g_{ds}$. In fact, this CD amplifier is characterized from Fig. 4.43a, by using a part of the circuit formed by the TFTs T1 and T2. The simulation results with TFT model and the measured circuit response are shown in Fig. 4.21. During the circuit simulation, the load impedance from the measuring cable and probes (10 MΩ resistor parallel with 16 pF capacitor) was also considered.

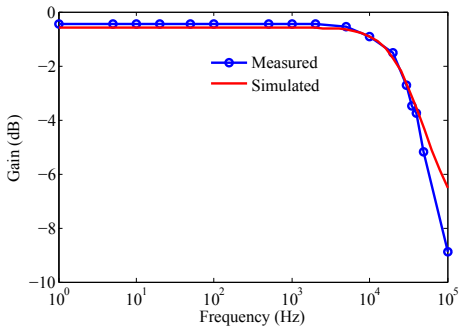


Figure 4.21: CD amplifier simulation and measured circuit response.

Along a multistage amplifier it is often necessary to change the levels of bias-voltages in conformity with the desired optimal operation-point. When a high dc level shift of a signal is needed, the dc-level shift that is accomplished by the circuit in Fig. 4.20 may not be sufficient (due to maximum ratings on V_{GS}). It may imply more voltage drops, which can be accomplished with the circuit shown in Fig. 4.22a. The corresponding fabricated picture with wire-bonding is shown in Fig. 4.22b. All the tansistors (T1-T4) have the same dimensions (W = 80 μm and L = 20 μm). The circuit transient and frequency responses are shown in Fig. 4.23, from simulations and measurement. Results are shown for an input given by 9.5 + 0.5sin(ωt), $V_B = 2$ V and $V_{DD} = 12$ V. The expected dc level shifting can be noticed from the transient response, similarly the expected gain (≈ 0 dB) can be observed from the frequency response.

Common-Source Amplifier: CS amplifiers are generally used to achieve high gain. They are important blocks in multi-stage amplifiers. Therefore, a simple CS amplifier with a diode connected transistor as the load is analyzed from Fig. 4.2. Its frequency response is presented in Fig. 4.24,

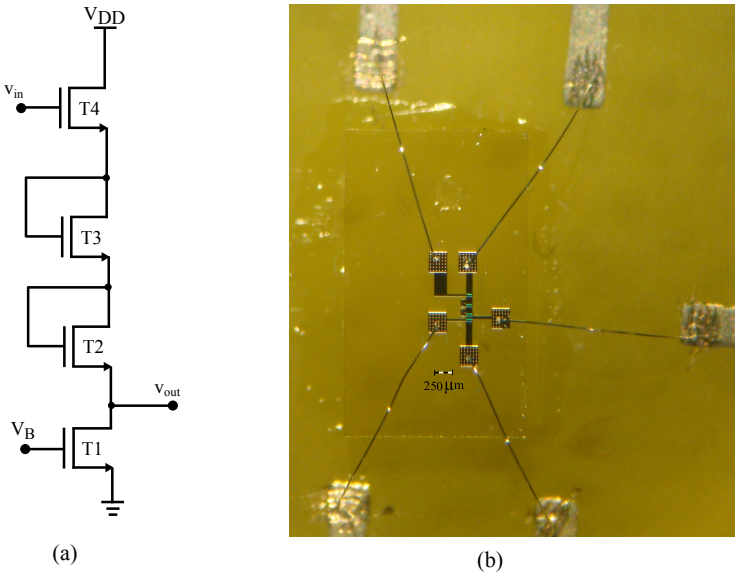


Figure 4.22: Level shifter (a) schematic (b) Fabricated circuit with wire-bonding.

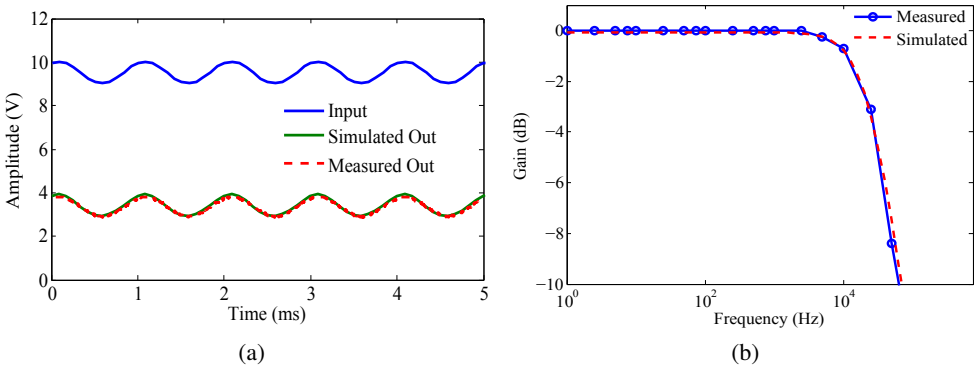


Figure 4.23: Level shifter response from simulations and measurements (a) Transient response (b) Frequency response

when it drives a capacitive load of 4 pF. As expected from $20\log(\sqrt{\frac{W_{T1}}{W_{T2}}})$, a gain of 12.5 dB is noticed.

Differential Amplifier: Differential amplifiers play a central role in analog circuits, as building blocks for a wide range of operations, from simple amplification to algebraic signal operation and filtering. Typically a differential amplifier comprises a transistor differential pair at the input stage to amplify the difference of two signals and to simultaneously attenuate the common-mode noise (present in both signals) in relation to the difference. In functional terms, the analysis of the non-linear behavior of the differential pair is fundamental to validate the usability of the technology for a broader range of applications in analog signal processing systems. The differential amplifier schematic and micrograph of the fabricated circuit with wire-bonding is shown in Fig. 4.25. During circuit characterization, external passive resistors (of value 1MΩ) are used as load. In this

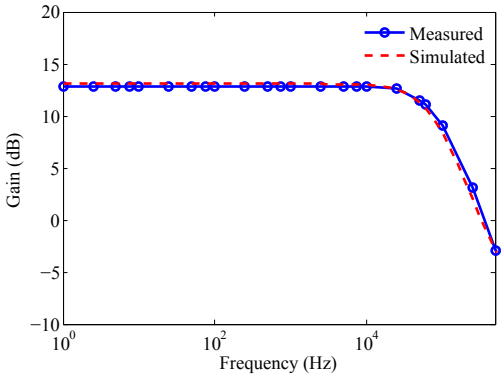
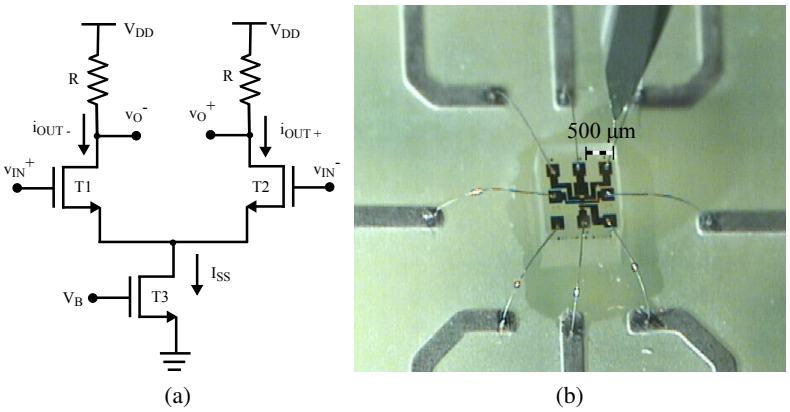


Figure 4.24: Frequency response of the amplifier (Fig. 4.2b) with 4 pf capacitive load.

circuit, T1 and T2 widths are 480 μm and T3 width is 160 μm. When all the transistors operate in the saturation, its small signal gain is given by (4.3).

$$A \approx -g_m(r_{ds}//R) \tag{4.3}$$



(a) (b)

Figure 4.25: Differential Amplifier (a) Schematic (b) Micrograph with wire-bonding

The differential output current (i_O) is given by

$$i_O = i_{OUT+} - i_{OUT-} = K v_{IN}\sqrt{\frac{2I_{SS}}{K} - v_{IN}^2}. \tag{4.4}$$

The above expression (4.4) is valid, as long as the input is limited to: $-\sqrt{\frac{I_{SS}}{K}} \leq v_{IN} \leq \sqrt{\frac{I_{SS}}{K}}$. Its linearity response (differential output current as a function of differential input voltage) is shown in Fig. 4.26a, when the differential input voltage is swept from -5 to 5 V, with a bias voltage V_B = 2.5 V. The circuit has almost a linear response in the range of $\pm$1.5 V, as predicted by $\pm\sqrt{I_{SS}/K}$. Its frequency response is shown in Fig. 4.26, which resulted in 10 kHz bandwidth, 21.2 dB gain and 114 μW power consumption. Amplifiers performance metrics are shown in Table. 4.2.

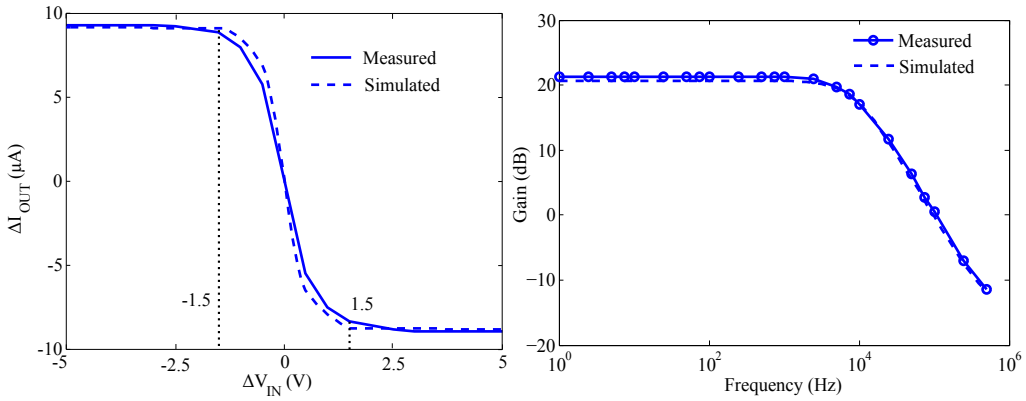


Figure 4.26: Differential amplifier characterization from simulations and measurements (a) Linearity response (b) Frequency response

Table 4.2: CS amplifiers performance

Circuit	No. of TFTs	Power (mW)	Bandwidth (KHz)	Mid-band gain (dB)	Load
CD (Fig. 4.22)	4	0.022	25	0	4 pF
CS (Fig. 4.2)	2	0.079	70	12.5	4 pF
Differential amplifier (Fig. 4.25)	3	0.114	10	21.2	10 MΩ//16 pF

4.2.5 Single Stage High-Gain Topologies

Some solutions have been suggested in the literature to boost the gain by using positive feedback when only single-type transistors are available. High gain can be obtained through a small-signal bootstrapping of the gate-source voltage in the load transistor, while keeping the transistor in saturation [124]. Fig. 4.27a illustrates the method. A similar procedure was successfully realized with a-Si:H TFTs in [24], and with a single-ended configuration in [5]. A high-gain stage using a bootstrapped inverter [125] is analyzed next. Based on this topology, a novel circuit is proposed to enhance the gain even further, without compromising power consumption.

Basic Capacitive Bootstrap Amplifier (Amp1): A basic high-gain amplifier topology using capacitive bootstrapping [125] is shown in Fig. 4.27b. This circuit is referred as Amp1 from here on. At dc, transistor T3 is in cutoff, hence, its effective *off* resistance is significantly high. Due to the transistor intrinsic capacitance, T3 can be viewed as parallel combination of a resistor and a capacitor as shown in Fig. 4.27(c). On the other hand, T1 and T2 should be in saturation, for the proper functionality of the amplifier. For high frequency signals, the capacitor (C) acts as a short circuit and the feedback factor (A_f) is supposedly one. However, A_f depends on the aspect ratio of

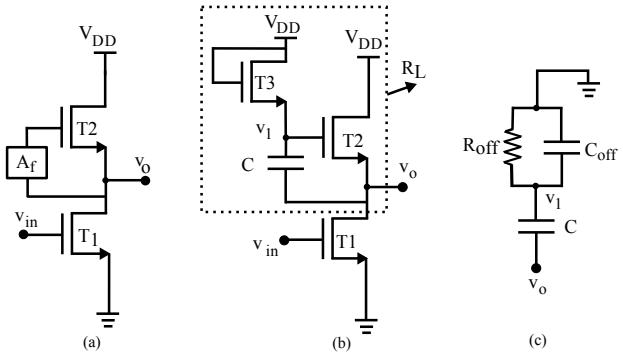


Figure 4.27: High gain amplifier employing positive feedback only with n-type enhancement transistors (a) Topology (b) Amplifier with capacitive bootstrapping (c) Positive feedback path with C and T3.

transistor T3 and C (C_{off} is a function of the transistor aspect ratio). From Fig. 4.27,

$$\begin{aligned} v_1 &= A_f v_0 \\ &= v_0 \frac{(R_{off} // \frac{1}{sC_{off}})}{\frac{1}{sC} + (R_{off} // \frac{1}{sC_{off}})} \\ &= v_0 \frac{1}{1 + \frac{1}{sC}(\frac{1}{R_{off}} + sC_{off})}, \end{aligned} \tag{4.5}$$

since R_{off} is very high, it can be simplified as

$$\begin{aligned} v_1 &= v_0 \frac{1}{1 + \frac{C_{off}}{C}}, \\ A_f &= \frac{v_1}{v_0} = \frac{1}{1 + \frac{C_{off}}{C}}. \end{aligned} \tag{4.6}$$

From (4.6), it is clear that as C_{off} increases, A_f decreases. This in turn will reduce the overall amplifier gain that can be computed with the aid of the small-signal model shown in Fig. 4.28.

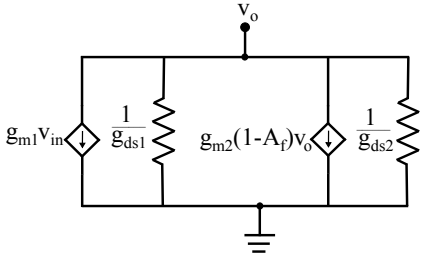


Figure 4.28: High gain amplifier small signal equivalent

By applying KCL at v_o in Fig. 4.28,

$$v_o(g_{ds1}+g_{ds2})+g_{m1}v_{in}+(1-A_f)g_{m2}v_o=0,$$
$$A=\frac{v_o}{v_{in}}=\frac{-g_{m1}}{(1-A_f)g_{m2}+g_{ds1}+g_{ds2}}. \tag{4.7}$$

If A_f is close to one, high gain can be obtained. However, in order to guarantee a stable behavior, A_f must always be less than unity.

In Fig. 4.27b the active load (R_L) is formed by T2, T3 and C, and can be represented by (4.8), which is very close to the transistor output resistance $\frac{1}{g_{ds2}}$.

$$R_L=\frac{1}{(1-A_f)g_{m2}+g_{ds2}} \tag{4.8}$$

DC Bootstrap Amplifier (Amp2): Another high-gain topology based on positive feedback using two delay stages is reported in [5]. The corresponding schematic is shown in Fig. 4.29. This circuit is referred as Amp2 from here on. This circuit can amplify dc signals, since, unlike Amp1, no high-pass action is present in the feedback network. However, this feedback circuit causes lower bandwidth and higher power consumption because of the extra power and delays added by the transistors. In this topology, the aspect-ratios of transistors T3 to T5 influence both the gain and bandwidth. Compared to Amp1, all transistors in Amp2 operate in saturation. In order to ensure a stable operation for Amp2, again the feedback loop gain must always be set to a value lower than one. For signal operation, Amp2 reduces to Fig. 4.27(a), so the same gain is obtained as in (4.7). Though this specific circuit was not characterized from measurements, it was used in a high-gain multiplier as an active load, but in a differential form, as can be seen in subsection 4.3.3.

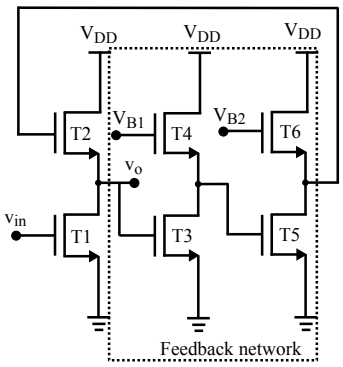


Figure 4.29: Amplifier topologies for high gain: Two stage inverting buffers (Amp2) [5]

Amp1 and Amp2 Comparison: In order to understand the advantages and drawbacks of the two high gain topologies (Amp1 and Amp2), they are compared from simulations. Their frequency responses are presented in Fig. 4.30, under no-load condition, and with the same input bias. Circuit component information, bandwidth and power consumption are listed in Table. 4.3. It can be

noticed that Amp2 shows dc amplification, higher power consumption and a lower bandwidth when compared to Amp1, as expected.

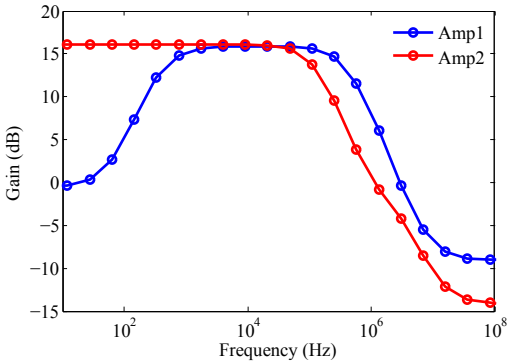


Figure 4.30: Amp1 and Amp2 frequency response from simulations.

Table 4.3: Circuit components information

Circuit	Transistors	Capacitors	BW (KHz)	Power (mW)
Amp1	T1,T2 : W = 160 μm, L =20 μm T3 : W = 40 μm, L =20 μm	C = 5 pF	435	0.2
Amp2	T1,T2 : W = 160 μm, L =20 μm T3,T5 : W = 75 μm, L =20 μm T4,T6 : W =80 μm, L =20 μm	-	127	0.21

Amp1 gain variation with respect to the C and T3 dimensions are demonstrated in Fig. 4.31. Higher value of C and small dimensions of T3 leads to higher gain as the feedback factor becomes closer to one. Fig. 4.32 presents the bandwidth variation of Amp1 with respect to C and T3 width.

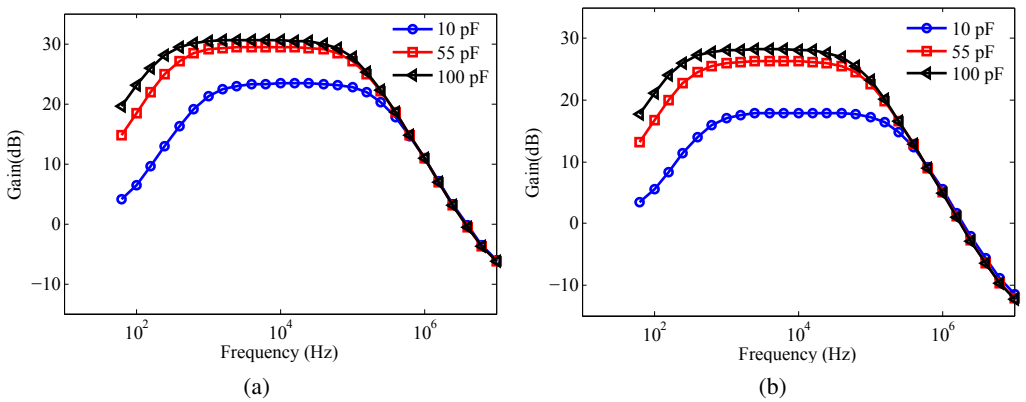
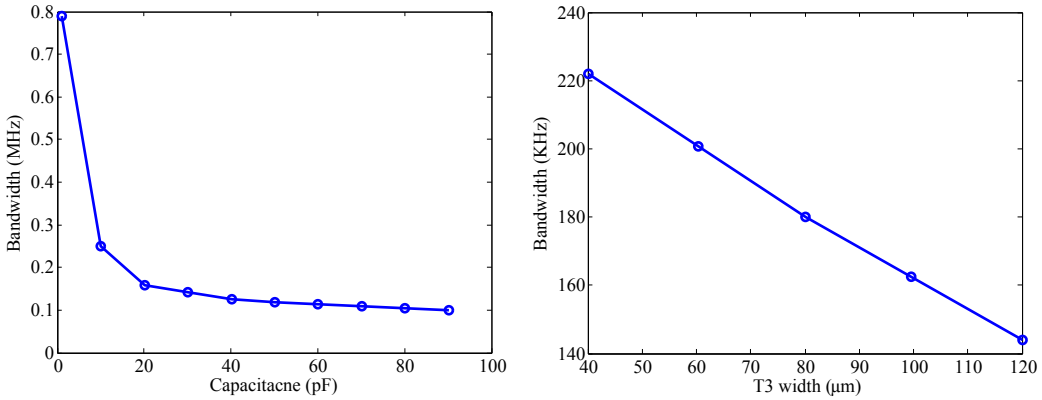
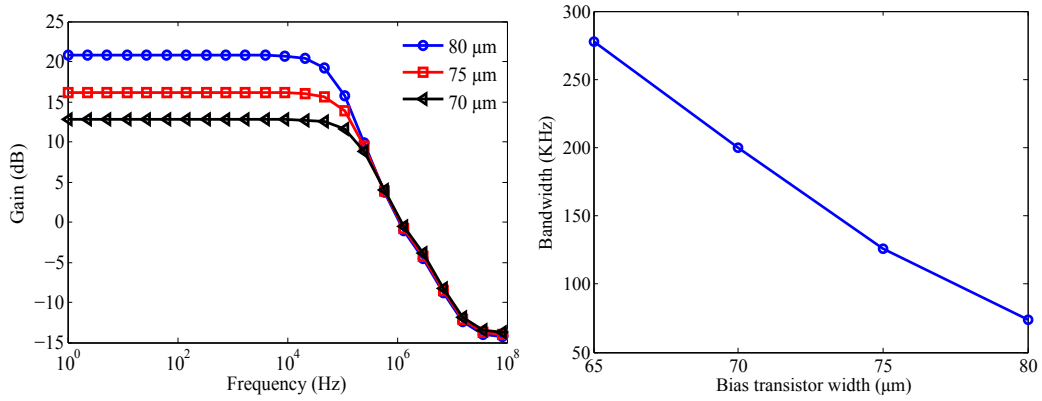


Figure 4.31: Impact of C value and T3 dimensions on Amp1 gain, from simulations using TFT models (a) W = 40 μm and L = 20 μm (b) W = 160 μm and L = 20 μm.



(a) (b)

Figure 4.32: Impact of C value and T3 dimensions on Amp1 bandwidth, from simulations using TFT models (a) T3 dimensions : W = 40 μm and L = 20 μm (b) C = 40 pF and T3: L = 20 μm.



(a) (b)

Figure 4.33: Impact T3 and T5 dimensions (width) on Amp2 gain and bandwidth, from simulations using TFT models (a) Gain variation (b) Bandwidth variation.

The gain and bandwidth variation of Amp2 with respect to T3 and T5 dimensions are presented in Fig. 4.33. It can be noticed that with higher values of T3 and T5 widths (close to T4 and T6 widths), higher gain is being achieved, as the feedback gain becomes closer to unity. As expected, the bandwidth is reduced with wider transistors.

Proposed High Gain Amplifier (Amp3): Based on Amp1 topology, a novel amplifier is proposed, to increase even further the gain. The circuit schematic is shown in Fig. 4.34, referred from now on as Amp3. For signal, the simplified load is shown in Fig. 4.35(b).

The load resistance (R_L), is given by

$$R_L = \frac{v_o}{i_o},$$

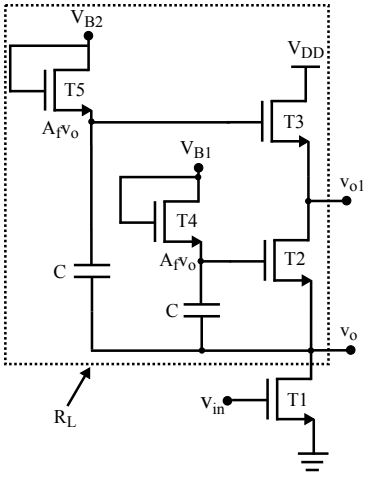


Figure 4.34: Proposed high gain amplifier (Amp3) only with n-type enhancement transistors

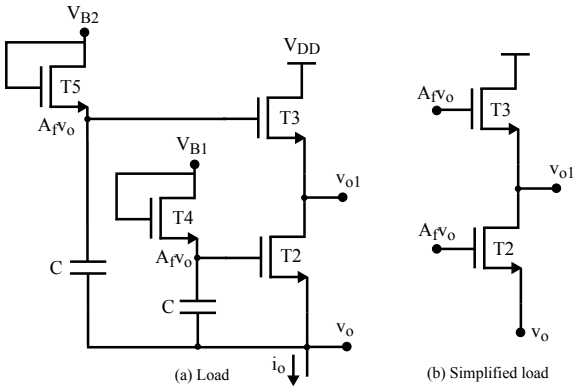


Figure 4.35: Active load

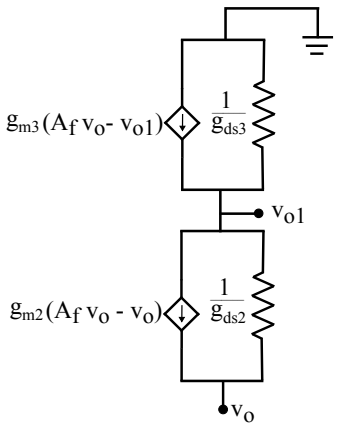


Figure 4.36: Small signal equivalent of R_L in Amp2

From Fig. 4.36, at node v_{o1},

$$\begin{aligned} -g_{m3}(A_f v_o - v_{o1}) + v_{o1} g_{ds3} + (v_{o1} - v_o) g_{ds2} + g_{m2}(A_f - 1) v_o &= 0 \\ v_{o1}(g_{m3} + g_{ds3} + g_{ds2}) - v_o(A_f g_{m3} + g_{ds2} + (1 - A_f) g_{m2}) &= 0 \end{aligned} \tag{4.9}$$

$$\begin{aligned} v_{o1} &= \frac{A_f g_{m3} + g_{ds2} + (1-A_f) g_{m2}}{(g_{m3} + g_{ds3} + g_{ds2})} v_o \\ i_o &= \left[1 - \frac{(A_f g_{m3} + g_{ds2} + (A_f - 1) g_{m2})}{(g_{m3} + g_{ds3} + g_{ds2})}\right] v_o g_{ds2} + g_{m2}(1-A_f) v_o \end{aligned} \tag{4.10}$$

Assuming A_f = 1, transistors T1-T3 with equal signal parameters and $g_m >> g_{ds}$

$$\begin{aligned} i_o &\approx \frac{g_{ds}^2}{g_m} v_o \\ R_L &= \frac{v_o}{i_o} \approx g_m r_{ds}^2 \end{aligned} \tag{4.11}$$

The gain of Amp3 is then given by (4.12), and considering equal feedback gains, the value is close to twice of that in Amp1 and Amp2 (4.7).

$$\frac{v_0}{v_{in}} = g_m (r_{ds} // g_m r_{ds}^2) \tag{4.12}$$

The gain variation of Amp3 with respect to the bias transistor dimensions (T5 and T6 width) and C are shown in Fig. 4.37. The gain comparison between Amp1, Amp2 and Amp3, from simulations, is shown in Fig. 4.38. As expected, Amp2 shows the lowest bandwidth and highest power consumption, while Amp3 shows the highest gain with the same power consumption as Amp1. It should be noted that Amp3 has two outputs, if a low impedance is demanded, then v_{o1} can be used instead (Fig. 4.34).

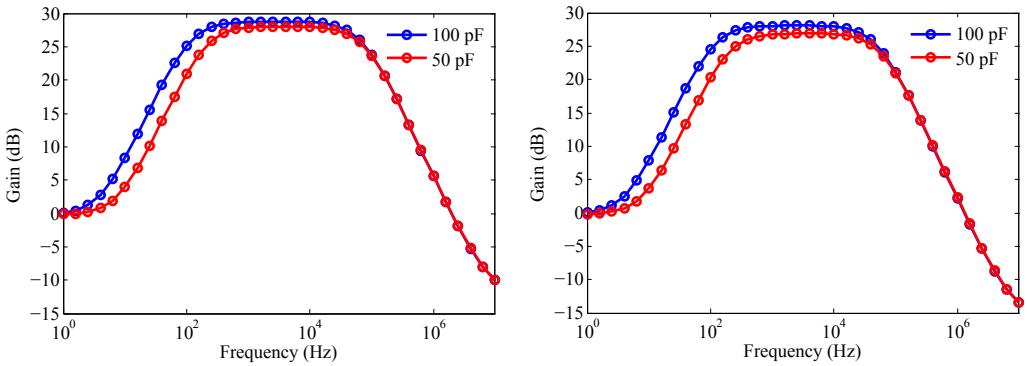


Figure 4.37: Impact of C and bias transistors (T4 and T5) widths on the gain and bandwidth of Amp3. Simulation results using TFT models (a) W = 40 μm (b) W = 80 μm

Measured Amplifier Response: Fig. 4.39 shows Amp1 fabricated circuit, with on-chip capacitor. In this circuit, T1 and T2 have the same aspect ratio (W = 160 μm and L = 20 μm) with fingered layout, whereas, T3 has a different aspect ratio (W = 40 μm and L = 20 μm) and is designed in direct layout. The width of the bias transistor (T3) is made smaller than T1 and T2 for achieving a

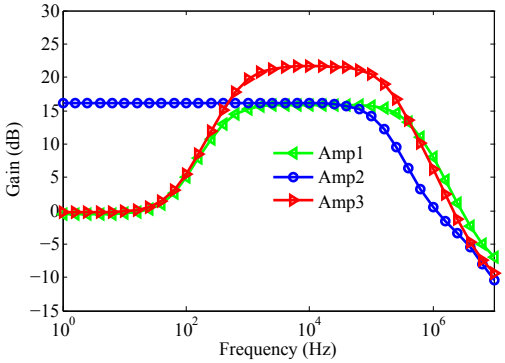


Figure 4.38: Amplifiers (Amp1 to Amp3) gain comparison from simulations.

high gain, as explained before for Amp1. The on-chip capacitance is 40 pF, a value taken from an actual measurement.

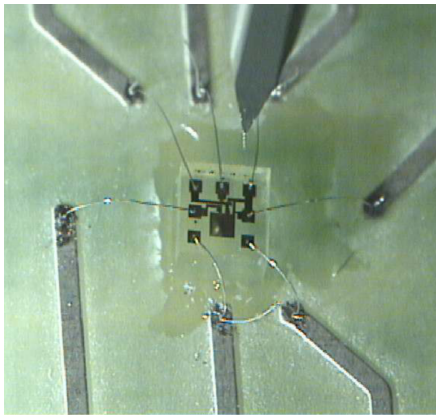


Figure 4.39: Amp1 fabricated circuits after dicing and wire-bonding

The bias transistors in the high-gain amplifiers (Amp1 or Amp3) should evince a very high impedance, since they operate in cutoff. However, because the precision of measurements at very small values of currents induces a relatively high error in modeling (very small bias voltages), the model result for the TFT in cutoff does not show such a high impedance, which resulted in a higher value for the lower cutoff frequency, as can be noticed in Fig. 4.38. To circumvent this problem, a large resistance was used in parallel with the overlap capacitance of the cutoff transistor for ac simulation purposes. Measured and simulation response is shown in Fig. 4.40, revealing that the cutoff resistance value stays in the order of 10 MΩ. This circuit has shown a mid-band gain of 10.4 dB.

For Amp3, two versions of the circuit were fabricated and wire-bonded as shown in Fig. 4.41: one with external capacitance and the other with on-chip capacitance. Transistors T1 to T3 were made with the same aspect ratios: W = 160 μm and L = 20 μm, whereas T4 and T5 were set to W = 10 μm and L = 20 μm. Again, on chip capacitance is measured to be 40 pF, similar to Amp1. In fact, when the external capacitor is added to the amplifier in Fig. 4.41a with a value of 40 pF the

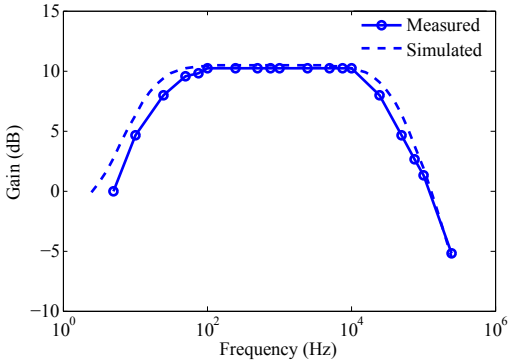
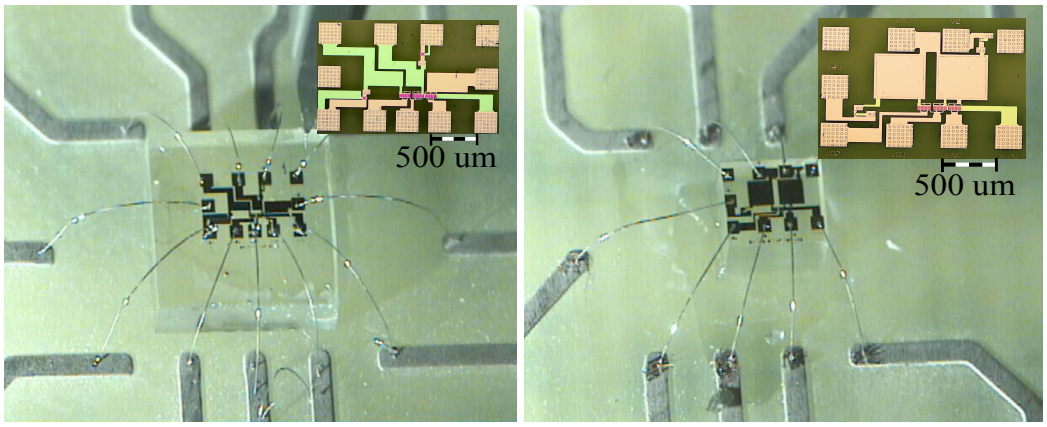


Figure 4.40: Amp1 simulation response validation using measured outcome

frequency response matches that of the amplifier with on-chip capacitors in Fig. 4.41b. Fig. 4.42 presents the frequency response of Amp3 with different values of capacitance (C) and a load (from the measuring cables) similar to Amp1. From Fig. 4.42, with higher value of C, an improvement in gain is observed, since the feedback factor becomes closer to unity, as explained before.



(a) (b)

Figure 4.41: Amp3 fabricated circuits after dicing and wire-bonding; corresponding micrographs of the circuits are shown in the inset (a) External capacitance (b) On-chip capacitance.

Table 4.4: Amp1 and Amp3 performance comparison

Circuit	No. of TFTs	C (pF)	Power (mW)	Bandwidth (KHz)	Gain (dB)	Load
Amp1	3	40	0.576	27	10.4	10 MΩ//16 pF
Amp3	5	40	0.576	20	22	10 MΩ//16 pF
Amp3	5	330	0.576	5	34	10 MΩ//16 pF
[30]	16	-	0.9	54	18.7	1 MΩ//2 pF

Table. 4.4 presents a brief summary of Amp1 and Amp3 performance in comparison with the literature. Up to the date, and to the best of our knowledge, Amp3 presents the highest gain

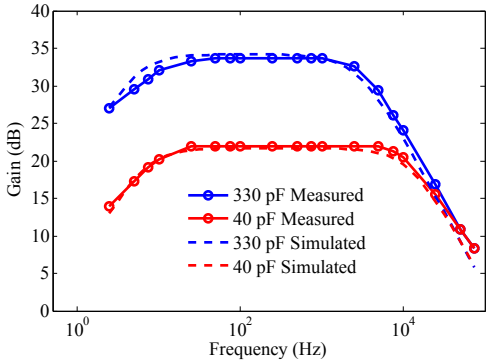


Figure 4.42: Amp3 frequency response

reported for a single stage amplifier with n-type enhancement a-GIZO TFTs. In fact, Amp3 is expected to give 6 dB higher gain than Amp1 under similar conditions (with same feedback gain). It can be noticed from Table. 4.4 that under similar bootstrapping capacitance value (C = 40 pF), Amp3 shows an even higher gain than the expected 6dB over Amp1 gain. However, Amp3 actually has a higher A_f than Amp1, which resulted from the smaller aspect ratio of its bias transistors (T4 and T5: W= 10 μm L = 20 μm in Amp3 and T3: W= 40 μm L = 20 μm in Amp1).

4.3 Signal Processing Blocks

In this section a few fundamental signal processing blocks will be analyzed, namely, adder, subtractor and different types of multipliers. First the functionality verification is made for the traditional adder and subtractor, which are characterized from both simulation and measurements. Then a novel circuit is proposed either to add or to perform the average of multiple signals. The discussion follows to the analysis of multipliers based on the Gilbert cell.

4.3.1 Adder-Subtractor

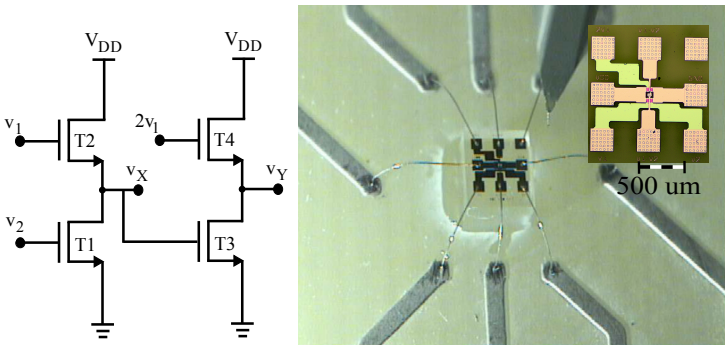
The adder/subtractor circuit schematic is shown in Fig. 4.43a, T1 and T2 TFTs form the subtractor, while T1 to T4, all together, constitute an adder [22]. Fig. 4.43b shows the correspondent fabricated circuit.

In order to attain the adding and subtraction operation, all the transistors have to operate in saturation. The drain current (I_D) is going to be approximately expressed as per level 1 MOSFET model (ignoring channel-length modulation),

$$I_D \approx K * (V_{GS} - V_{TH})^2. \tag{4.13}$$

The drain currents in T1 and T2 can then expressed as,

$$\begin{aligned} i_{D1} &\approx K\left[v_1 - v_X - V_{TH}\right]^2, \\ i_{D2} &\approx K\left[v_2 - V_{TH}\right]^2. \end{aligned} \tag{4.14}$$



(a) (b)

Figure 4.43: Adder subtractor circuit (a) Schematic (b) Fabricated circuit after dicing and wire-bonding; micrograph of the circuit is shown in the inset.

Equating i_{D1} and i_{D2} due to series connection of T1 and T2

$$\left[v_1 - v_X - V_{TH}\right]^2 = \left[v_2 - V_{TH}\right]^2, \tag{4.15}$$

results in

$$v_X = v_1 - v_2, \tag{4.16}$$

Applying the same analysis to T3 and T4, one gets

$$[2v_1 - v_Y - V_{TH}]^2 = [v_1 - v_2 - V_{TH}]^2, \tag{4.17}$$

which simplifies to,

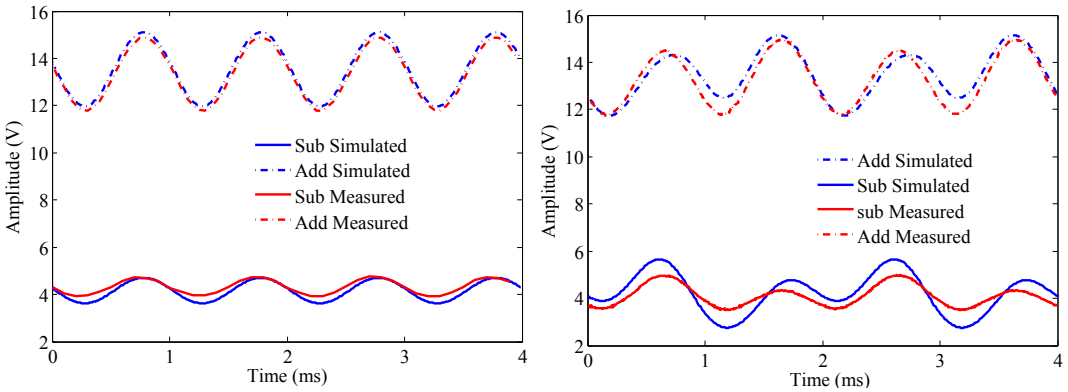
$$v_Y = v_1 + v_2. \tag{4.18}$$

Functional verification as subtractor and adder is made by applying the following stimulus,

$$\begin{aligned} v1 &= 9 + sin(2\pi f_1 t), \\ v2 &= 4.5 + 0.5 * sin(2\pi f_2 t). \end{aligned} \tag{4.19}$$

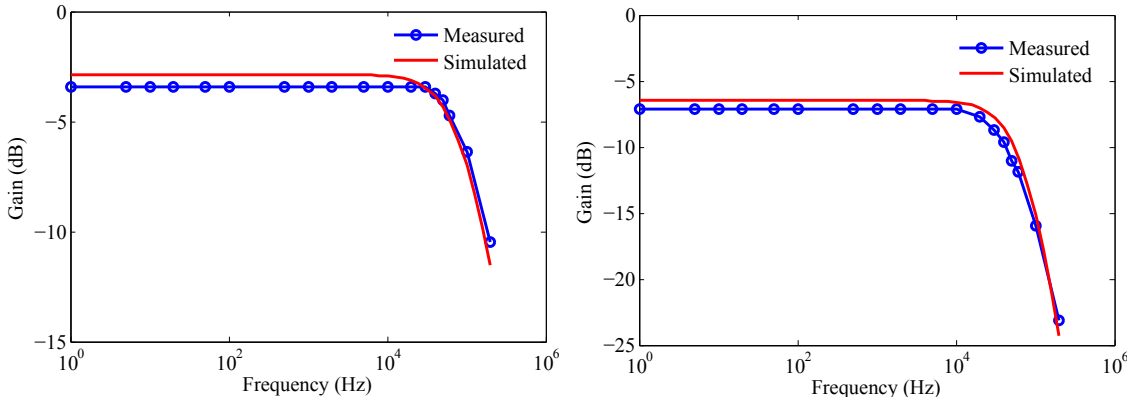
Testing was carried out using the two signals with the same frequency $f_1 = f_2 = 1\,KHz$, but also with different frequencies – $f_1 = 1\,KHz$ and $f_2 = 500\,Hz$. Since the ANN verilog-A model is not able to characterize the bias stress, a minor mismatch between the simulated and measured circuit response can be observed from Fig. 4.44. However, both simulation and measured responses follow the same trend.

Fig. 4.45 presents the simulation and measured frequency response of the circuit (v_x and v_y), including the load impedance from the measurment cable. Voltage v_1 is fixed to the bias voltage and v_2 is a signal. From Fig. 4.45, it can be noticed that the gain (A_1) from v_2 to v_x is slightly lower than one. Because of cascading, gain (A_2) from v_2 to v_y is reduced even further, as expected.



(a) Same frequency (b) Different frequency

Figure 4.44: Adder subtractor functional verification from simulation and measured circuit response



(a) (b)

Figure 4.45: Frequency response (a) v_x (b) v_y

4.3.2 Novel Adder/ Averaging Circuit

A novel circuit is proposed to either add or average multiple signals. This circuit is capable of adding an arbitrary number of signals and its schematic and micrograph are shown in Fig. 4.46. The fabricated circuit was designed to add up to four signals.

The small-signal equivalent circuit, formed by transistors T1 to Tn ,TB1 and TB2, is shown in Fig. 4.47. Assuming the same aspect ratios for all transistors, T1 to Tn, and under similar bias conditions, they will share the same small-signal transconductance value g_m, while the biasing transistors will be defined by g_{mb}. With the help of Fig. 4.47, the relationship between the output voltage and inputs can be expressed as in (4.21).

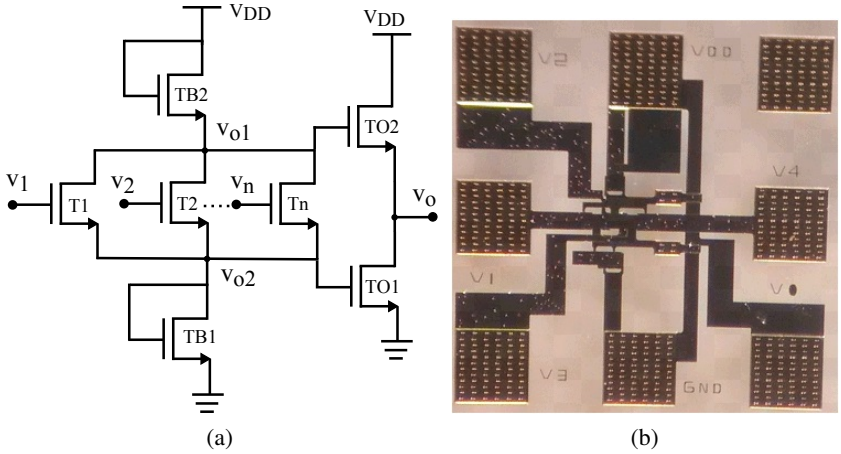


Figure 4.46: Novel adder (a) Schematic (b) Micrograph of the fabricated circuit.

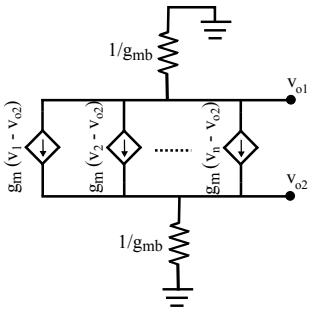


Figure 4.47: Small signal equivalent formed by the transistors T1 to T5

$$
\begin{aligned}
v_{o1} &= -v_{o2} \qquad (4.20)\\
v_{o2} &= \frac{1}{g_{mb}}\left[g_m(v_1 - v_{o2}) + g_m(v_2 - v_{o2}) + ... + g_m(v_n - v_{o2})\right]\\
v_{o2} &= \frac{g_m}{g_{mb}}\left[v_1 + v_2 + ... + v_n - nv_{o2}\right]\\
v_{o2} &= \frac{\frac{g_m}{g_{mb}}}{1 + \frac{ng_m}{g_{mb}}}\left[v_1 + v_2 + ... + v_n\right]\\
v_o &= v_{o1} - v_{o2}, \quad \text{hence}\\
v_o &\propto v_1 + v_2 + ... + v_n
\end{aligned}
$$

For the specific case, when $g_{mb} = ng_m$ i.e., $W_{(TB1/TB2)} = nW_{(T1,T2..Tn)}$, (4.20) can be reduced

to

$$\begin{aligned} v_{o2} &= \frac{1}{2n}[v_1 + v_2 + ... + v_n] \\ v_o &= \frac{1}{n}[v_1 + v_2 + ... + v_n] \end{aligned} \tag{4.21}$$

From (4.20), it can be noticed that this circuit can perform the summation of multiple signals. The average of the input signals can also be obtained as per (4.21). The normalized measured response, and simulation outcome of the circuit are compared and validated with the expected response as shown in Fig. 4.48, for a power supply of 12 V and f_1 = 250 Hz, f_2 = 500 Hz and f_3 = 1000 Hz. It should be said at this point that in principle TB1 (and TO1) could be removed. However, in doing so the inputs would be limited to lower values due to V_{GS} maximum ratings, but also adding both transistors augments the gain by two (for the same aspect ratios), and in principle is more linear because V_{GS} variation is smaller for the same input levels (simulated results show evidences for this claim).

$$\begin{aligned} x1 &= 5 + 0.25sin(2\pi f_1 t), \\ x2 &= 5 + 0.25sin(2\pi f_2 t), \\ x3 &= 5 + 0.25sin(2\pi f_3 t). \end{aligned} \tag{4.22}$$

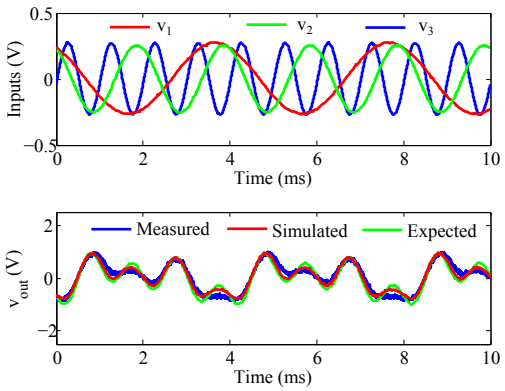


Figure 4.48: Novel adder characterization from simulated, measured and expected response

4.3.3 Multipliers

A multiplier based on Gilbert-type cell [126] is first attempted with a diode connected load. The circuit schematic and the micrograph are shown in Fig. 4.49. This circuit is referred as Mul1 from here on.

For analysis purposes, again, the I/V relationship for TFTs is roughly approximated by the well known FET expression. Having all transistors in saturation, the drain current is represented

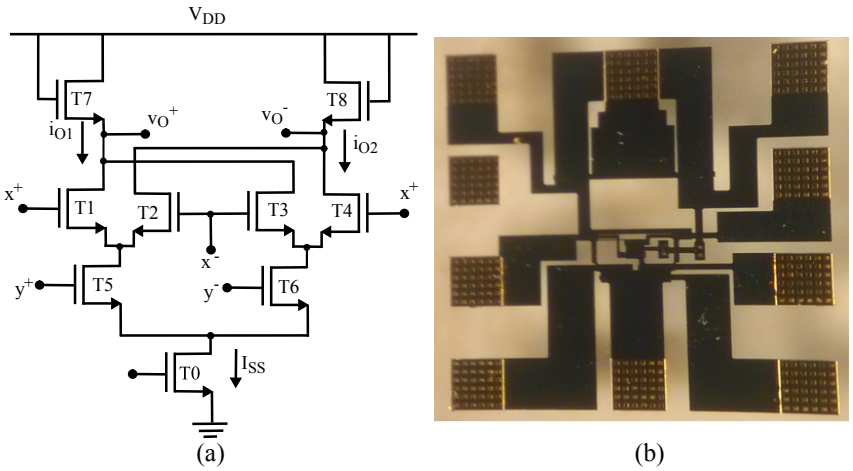


Figure 4.49: Gilbert cell with a-GIZO TFTs (Mul1) using a diode connected load (a) schematic (b) micrograph of the fabricated circuit.

by,

$$i_{DS} \approx \tfrac{1}{2}K(v_{GS} - V_{TH})^2. \tag{4.23}$$

By few manipulations, the differential output current of the multiplier can be found to be,

$$i_{OUT} \approx Kx\left(\sqrt{\left[\sqrt{\frac{I_{SS}}{K} - \frac{y^2}{2}} + \frac{y}{\sqrt{2}}\right]^2 - x^2} - \sqrt{\left[\sqrt{\frac{I_{SS}}{K} - \frac{y^2}{2}} - \frac{y}{\sqrt{2}}\right]^2 - x^2}\right), \tag{4.24}$$

where x and y are the differential input voltages. Assuming small x and y,

$$i_{OUT} \approx 2Kxy. \tag{4.25}$$

For testing purposes, the devices in Fig. 4.49 were set with the following sizes: W_{T0} = 320 μm, $W_{(T1\text{-}T4)}$ = 80 μm, $W_{(T5\text{-}T8)}$ = 160 μm. The circuit is tested with a power supply of 12 V. The following stimulus is applied to verify the linearity response of Mul1.

$$x = 9 \pm 2\,\text{V}, \quad y = 6 \pm 2\,\text{V}, \quad V_1 = 2\,\text{V} \tag{4.26}$$

Its linearity response from measurements is shown in Fig. 4.50a. These measurements are confronted with the expected ideal results in the normalized form, as shown in Fig. 4.50b. The expected multiplication operation is observed, but with a relatively low linearity of 10% for a 0.7 mW power consumption. This value, however, is measured at dy = 4 V and dx = -2 V, which is calculated by

$$\text{Linearity error}\Big|_{max} = \frac{(\text{Actual value - Obtained value})_{max}}{\text{Actual value}} \tag{4.27}$$

High-Gain Gilbert cell (Mul2): A novel high-gain multiplier is proposed based on Mul1, referred here as Mul2. This new multiplier uses positive feedback to achieve a high load impedance

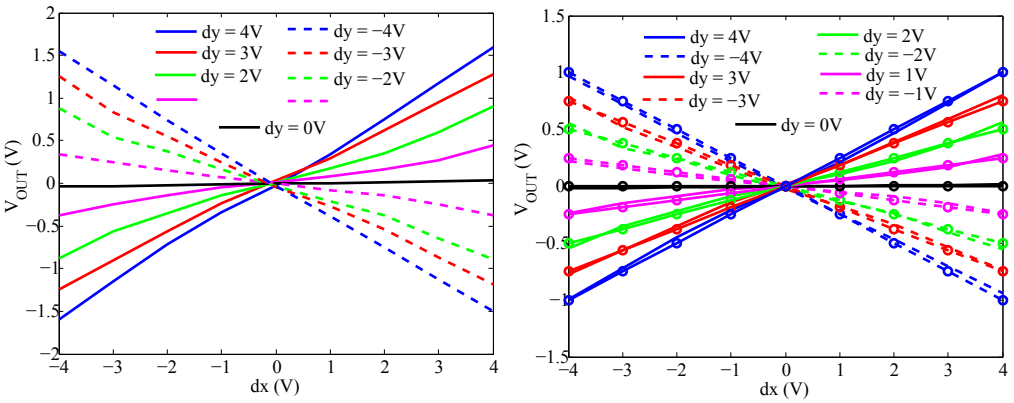


Figure 4.50: Mul1 measured linearity response (a) Actual value (b) Validation with the expected value in normalized form - line with circle represents the expected value.

as shown in Fig. 4.51, through a modification of the circuit in Fig. 4.29 for fully differential purposes. The high load impedance can be achieved as per Fig. 4.27, by making the same signal level at the gate and source of transistors (T7 and T8) with the help of a feedback network formed by T9 to T13.

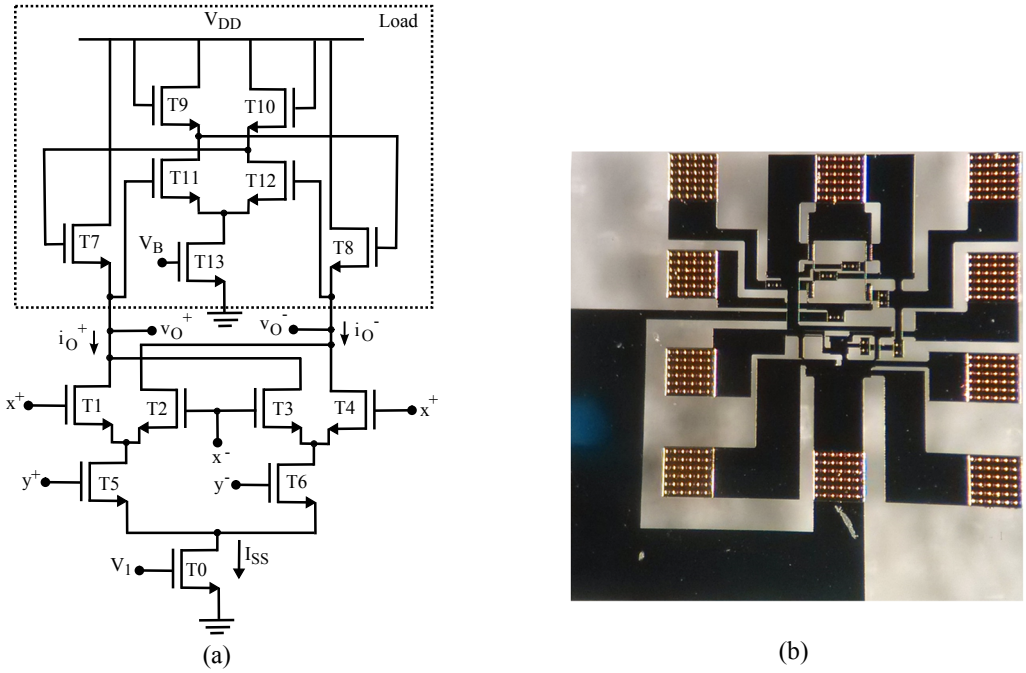


Figure 4.51: High gain multiplier (a) Schematic (b) Micrograph of the fabricated circuit.

The multiplier was designed with the following transistor sizes: $W_{(T0,\,T13)} = 320\,\mu$m, $W_{(T1\text{-}T4,\,T9\text{-}T10)} = 80\,\mu$m, $W_{(T5\text{-}T8)} = 160\,\mu$m, $W_{(T11\text{-}T12)} = 70\,\mu$m. The circuit is tested with a power supply of 16 V.

The following stimulus is applied for verification.

$$x = 6 \pm 2\,\mathrm{V}, \quad y = 4 \pm 2\,\mathrm{V}, \quad V_1 = V_B = 1.5\,\mathrm{V} \tag{4.28}$$

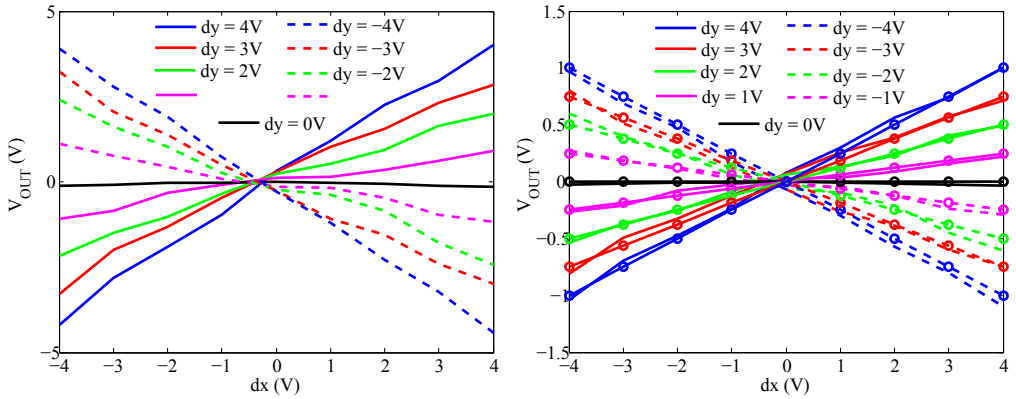


Figure 4.52: Mul2 measured linearity response (a) Actual value (b) Validation with the expected value in normalized form - line with circle represents the expected value.

Fig. 4.52a presents the linearity response of Mul2 taken from the measurements. This result is further confronted with the expected ideal response, in the normalized form, as shown in Fig. 4.52b. The circuit shows a 13% linearity (at dx = -3 V and dy = 3 V) with a 0.7 mW power consumption. A comparison of Mul1 and Mul2 performance and testing setup is presented in Table. 4.5. It has to be noted that Mul1 and Mul2 consumes the same power because of the different bias and supply voltages that were applied. In fact, under the same bias conditions and power supply, Mul2 is supposed to consume more power than Mul1 because of the positive feedback circuit (more current branches). In both circuits (Mul1 and Mul2) the linearity error can be explained in good extent by the mismatches between the transistors and also because in strong accumulation the Gilbert cell is approximated from a squared function. Mul2 has shown 8 dB gain improvement over Mul1. Again, under the same bias condition Mul2 was expected to show higher gain.

Table 4.5: Mul1 and Mul2 comparison

Circuit	No. of TFTs	V_{DD}	V_1	Power (mW)	Linearity error (%)	gain (dB)
Mul1	9	12	2	0.7	10	-20
Mul2	14	16	1.5	0.7	13	-12

4.4 Summary

The fundamental building blocks of complex electronic systems were addressed along the chapter. The lack of complementary devices, and low mobility are limiting factors that can be overcome, to some extent, applying non-convensional design schemes. The inclusion of positive feedback, as done in old technologies of the past, is effective in gain improvement. Also higher order signal processing operations, such as multiplication, can also be accomplished. The very fundamental building blocks of multistage amplifiers and signal processing were demonstrated, within the natural limits of the technology, in particular the bandwidth. From the analyzed techniques, it was possible to design a folding ADC, presented in the next chapter. In order to position the contribution of this chapter in the state of the art, a brief summary of the characterized circuits is presented in Table. 4.6 and compared with the circuits that are reported in the literature with AOS TFT technology. As referred earlier, all the circuits in this work were fabricated at room temperature, but annealed at temperatures lower than 200°C. Considering the low-temperature processing, the contributions show a significant improvement.

Table 4.6: Summary of characterized circuits and comparison with literature

Circuit	Literature	Current work
Logic gates	Fabricated at 600°C (Max. operating freq. 5 kHz) [121]	Max. operating freq. 10 kHz
Current mirrors	Fabricated at 400°C [123]	Expected behavior with low-temp. fabrication
Amplifier	Fabricated at 150°C, gain = 18.7 dB in [30]	gain = 34 dB
Signal processing blocks	-	Adder, novel circuit for averaging or summing, gilbert cell, high-gain novel multiplier

Chapter 5

Folding ADC with Resistive Interpolation

The analog to digital converter (ADC) is the ultimate block in a signal conditioning chain, where the analog continuous-time signals are converted for digital post-processing. Different types of ADCs have been reported in literature for TFT technologies. A few examples can be found, such as a four-bit counting type ADC [127], a six-bit SAR (the digital logic is implemented in FPGA) [27] with complementary organic TFTs, a five-bit flash ADC with n-type a-Si:H TFTs [26] or a delta-sigma ADC with p-type OTFTs [128]. Although a six-bit current steering digital to analog converter (DAC) has been reported with a-GIZO TFTs [29], apparently ADCs have not yet been addressed. The main focus of this chapter is then to design an ADC with a-GIZO TFTs. Having this done, the basic building blocks necessary to build a signal conversion chain are accomplished. It should be noted, however that the circuits presented below are limited to only simulations due to some unpredicted post-fabrication problems that prevented the experimental validation in the due time of this dissertation. A new batch has been fabricated with refined techniques and is almost ready for final testing. Nevertheless, the circuits are valuable and deserved to be reported, and having in mind that from previous testing the model has shown a good ability to predict the real circuit behaviour, it is an assurance that the circuits will function as expected with good probability.

The appropriate choice of an ADC architecture depends on many aspects, but mainly on the type of signal involved and resolution (number of bits). Nevertheless, technology limitations also play an important role. In the context of a-GIZO technology, the lack of a complementary (p-type) device and the relative low-intrinsic mobility need to be taken into account. In particular, the low-intrinsic mobility of devices restricts the intrinsic gain ($g_m r_{ds}$). Such limitation enforces the use of wider devices for gain improvement, which is essential in many practical situations. However, wider devices will impose limitations on the operating speed because of a consequent higher parasitic capacitance. If the devices are not self aligned (which is the present case) the extra needed overlap will surmount on the parasitic capacitors, restricting even more the bandwidth. With the bottom gate staggered TFT structure, another factor that limits speed is bigger contact

resistance, since the charge carriers from source to drain have to travel through the high-impedance path in the semiconductor as shown in Fig. 2.1c. It is important to consider these limitations while choosing the ADC architecture to attain a reasonable speed. Different ADC architectures have different characteristics with natural pros and cons. Table. 5.1 shows a brief summary of ADC architectures in relation to speed and accuracy (number of bits). The proper choice of an ADC is

Table 5.1: Comparison of ADCs

Speed	Accuracy	Example
Low to medium	High	Integrating
Medium	Medium	SAR, algorithmic
High speed	Medium to low	Flash, two-step, interpolating, folding, pipelined

application dependent. Notwithstanding, a major limitation of the technology is operating speed, for this reason the choice has fallen into an high-speed (flash type) ADC.

An n-bit flash ADC architecture with 2^n - 1 comparators is shown in Fig. 5.1. Each comparator uses a voltage reference, correspondent to one of the 2^n quantization levels, to signal if the input voltage is above its correspondent reference. The output of the comparators gives a known unary code of the input voltage that is finally converted to binary through a digital decoder. The conversion is parallel in nature, and so presents a good operating speed; however, not without its own limitations, as listed below:

- For an n-bit conversion the flash ADC needs (2^n - 1) comparators, properly matched. As the number of bits increase, the circuit complexity increases exponentially.
- Necessarily the area increases proportional to the complexity.
- The power consumption is high.
- In order to drive the input capacitance seen from the inputs of the (2^n - 1) comparators, a powerful driver is required.

Alternatively, a folding ADC architecture with resistive interpolation can overcome some of the drawbacks of a flash ADC, and at the same time retain some of its advantages, such as fast conversion speed. This technique has been previously employed in CMOS and BJT technologies [129, 130], and its effectiveness comes from the use of a folded version of the input signal for conversion, instead of its actual amplitude. An example of a typical folding characteristic is shown in Fig. 5.2 for a four bit conversion. The triangular shape represents the folded operation over the input signal. It can be observed that there are four folding edges and the amplitude of the each folded signal is reduced to one fourth of the original input signal. The folding edge, where the actual input amplitude falls, is determined by a coarse converter, which gives the information on the most significant bits (MSB), corresponding to one of the folding edges. As there are four edges, a two-bit coarse converter is required in this example. Further, a fine conversion is then

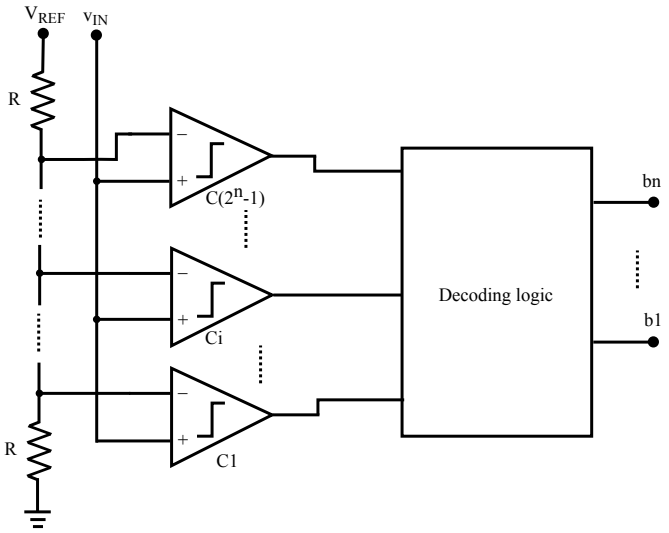


Figure 5.1: n-bit flash type ADC

required to convert the amplitude level in the corresponding folding edge, where the folding signal can be obtained through an analog signal processing block, which is explained further down in the text.

A four-bit folding ADC block diagram is shown in Fig. 5.3, which employs two-bit coarse and fine converters and the analog signal processing block. Both of the converters are flash type. This design needs a total of six comparators, three for fine conversion and another three for coarse. With the same resolution, a full flash architecture would need 15 comparators. Therefore, the folding ADC architecture minimizes circuit complexity, power consumption and area. In addition, it avoids the need for powerful drivers at the input as the number of comparators are significantly less than of a flash ADC.

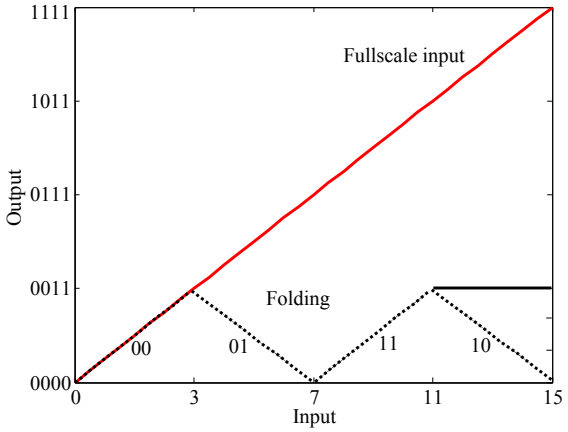


Figure 5.2: Folding operation

From Fig. 5.3, it can be noticed that the signal path for the least significant bits (LSB – b_1 and b_2) is slightly longer than the MSB (b_4 and b_3), caused by the analog signal processing block prop-

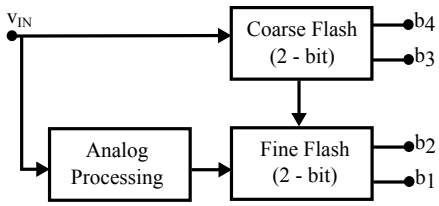


Figure 5.3: 4-bit folding type ADC.

agation time. Consequently, synchronization is required between these coarse and fine converter outputs. It can also be noticed that these fine and coarse conversion blocks operate it parallel, so it is possible to attain a high-speed conversion, very close to that of the flash ADC.

Some of the basic building blocks (digital logic gates, level shifter and amplifier) that are required for the 4-bit folding ADC with interpolation were presented in chapter. 4. This chapter focus on the other individual blocks in the ADC, namely, the comparator, which is essential for coarse and fine conversion and the folding circuit, which is part of analog signal processing block shown in Fig. 5.12, which will be explained later together with the circuit realization.

5.1 Comparator

As Fig. 5.1 shows, the comparator is the fundamental functional block in each of the coarse and fine flash-converters. The comparator can be treated as a single-bit ADC, whose symbol is shown in Fig. 5.4, and its operation can be defined as follows:

$$\text{Vo = high; when (V2 - V1)} > 0,$$
$$\text{Vo = low; when (V2 - V1)} \leq \text{V1}.$$

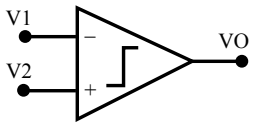


Figure 5.4: Comparator symbol

It is important to improve the gain in the comparator so that good level swings are accomplished from small input differences, i.e. the comparator presents a good sensitivity. A multistage pre-amplifier architecture, with three stages, shown in Fig. 5.5 was adopted for gain improvement, followed by a latch circuit for level adjustments.

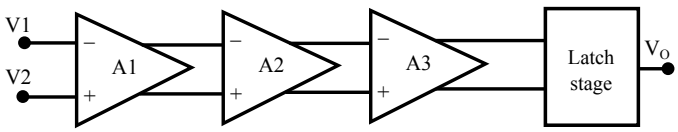


Figure 5.5: Comparator block diagram

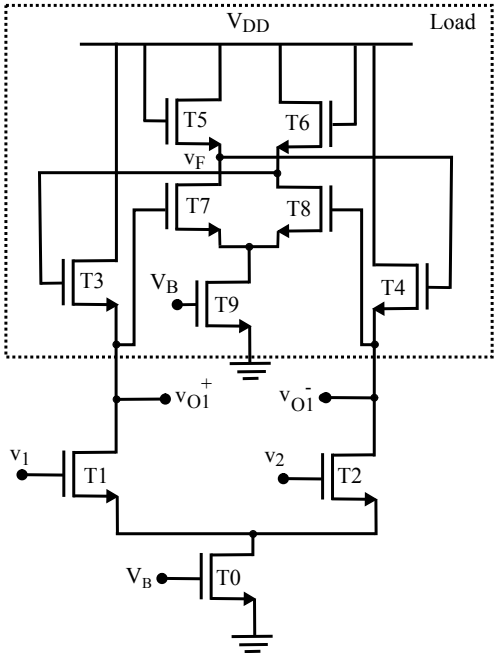


Figure 5.6: Amplifier stage in the comparator

Amplfier: Each single amplifier stage in Fig. 5.5 is made from a differential pair with a positive feedback load [124], as shown in Fig. 5.6. The stability to parametric variations in the positive feedback signal v_F, due to bias stress, depends on the aspect ratio of transistors T5, T6 and T9. To understand this dependency, a large signal analysis for these transistors in the feedback path is needed. Let us consider that all transistors have the same length, then,

$$\begin{aligned} \frac{1}{2} i_{D9} &= i_{D5}, \\ \frac{1}{2} W_{T9}(V_B - V_{T9})^2 &= W_{T5}(V_{DD} - v_F - V_{T5})^2, \\ \sqrt{\frac{W_{T9}}{2W_{T5}}}(V_B - V_{T9}) &= (V_{DD} - v_F - V_{T5}), \end{aligned} \tag{5.1}$$

just considering now the varying components we get,

$$\begin{aligned} \sqrt{\frac{W_{T9}}{2W_{T5}}}(-\Delta V_{T9}) &= (-\Delta v_F - \Delta V_{T5}), \\ \Delta v_F &= \sqrt{\frac{W_{T9}}{2W_{T5}}}(\Delta V_{T9}) - \Delta V_{T5}. \end{aligned} \tag{5.2}$$

Hence, when W_{T9} is double of W_{T5}, the feedback signal v_F is less sensitive to the threshold voltage variation [24]. In the current design, this constraint has been taken into account, to reduce bias stress impact. In fact, this amplifier is a differential form of Amp2 (Fig. 4.29) from the previous chapter, and so its gain is equal to Amp2, given by (4.7). Care has been taken to ensure a stable

operation by making the feedback gain less than one, as explained for Amp2. The amplifier frequency response is shown in Fig. 5.7 (from simulation). This circuit shows 14 dB gain and 55 kHz bandwidth, when driving a 4 pF load.

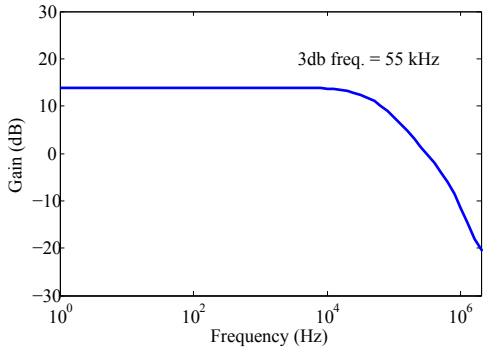


Figure 5.7: Amplifier frequency response

Latch: The schematic of the latch is shown in Fig. 5.8. It can be seen as a back to back connection of two inverters with positive feedback. This circuit senses the difference in the input signal (v^+_{O3} - v^-_{O3}) and amplify it in a regenerative manner to boost the gain. Its dc transfer characteristic

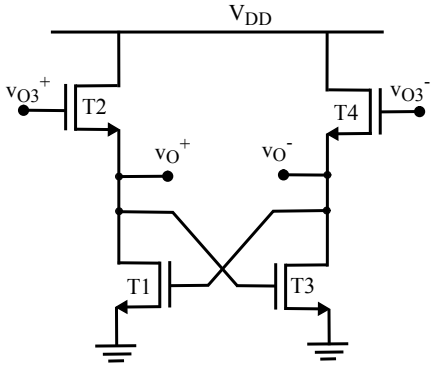


Figure 5.8: Latch schematic

i.e., differential output voltage versus differential input voltage is presented in Fig. 5.9, when the input voltage is swept from -0.5 V to 0.5 V. The gain around the mid point is 21.5 dB.

The resulting full comparator frequency response is then shown in Fig. 5.10, and its transient response is presented in Fig. 5.11 for a triangular and sine waves (one of the inputs is a fixed dc level of 10 V). The performance of the comparator is summarized in Table. 5.2. Although, an a-Si:H TFT based flash ADC is reported in [26], the comparator performance metrics are not referred explicitly, only the final ADC results were discussed. Hence, the information for that comparator is not presented in Table. 5.2. But even for the OTFT comparator the bandwidth is not reported, we could guess a bandwidth of at least 10 times that of the clock frequency. Since the proposed comparator does not use switching, solely the bandwidth is presented in the Table. 5.2.

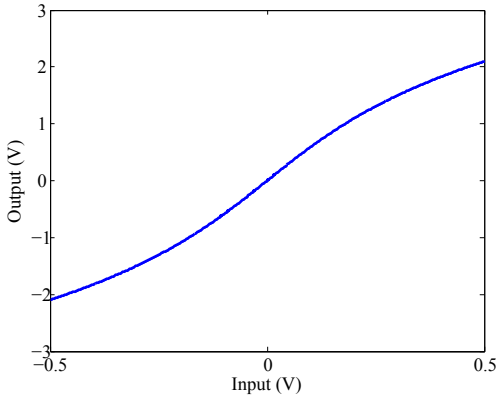


Figure 5.9: Latch dc voltage transfer characteristics

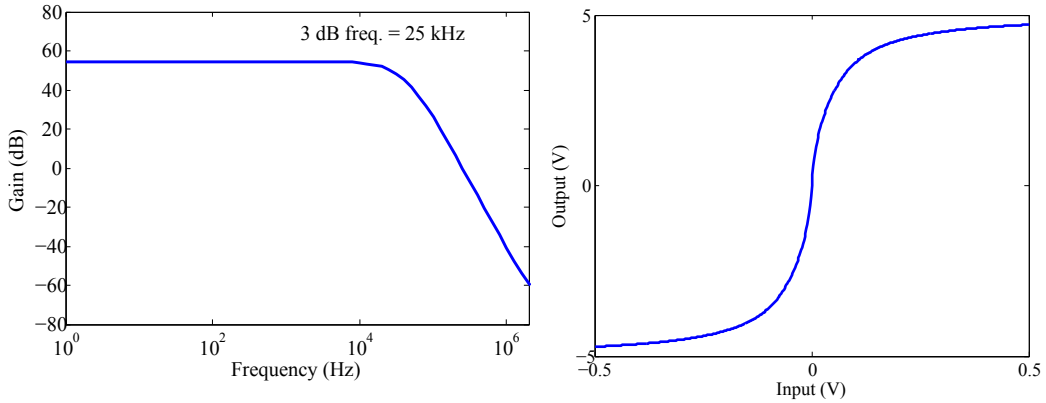
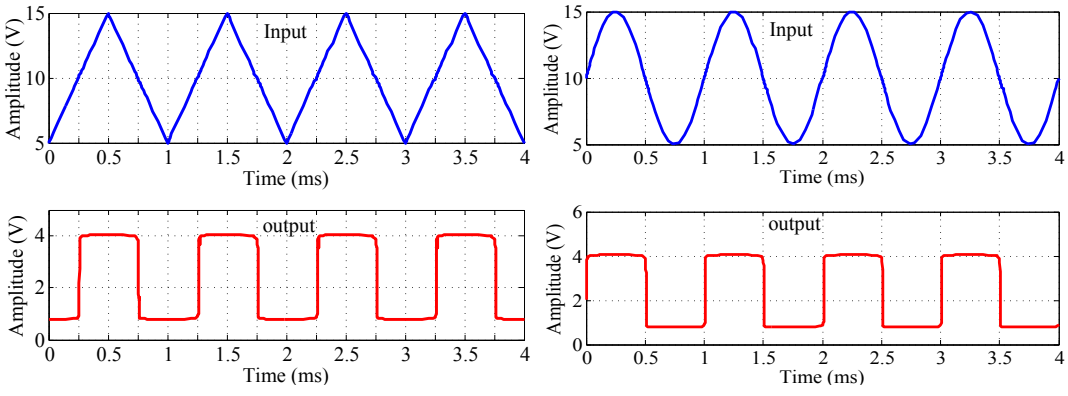


Figure 5.10: Comparator frequency response



(a) Triangular wave input

(b) Sine wave input

Figure 5.11: Comparator transient response, for 1 KHz input signals

Table 5.2: Comparators with different TFT technologies

Technology	Gain (dB)	Power (mW)	Clock (KHz)	Sensitivity (mV)	Ref.
OTFT	12	0.18	1	200	[25]
a-GIZO TFT	55	3.24	25 (Bandwidth)	32	Current work

5.2 Analog Signal Processing Block

The analog signal processing block is presented in Fig. 5.12. This has two folding blocks and an interpolation stage that, as seen bellow, is needed to generate the intermediate quantization levels within a given folded edge for the fine conversion. But let us start with the folding block that is realized by cross-coupled differential pairs [131], as shown in Fig. 5.13 using four pairs.

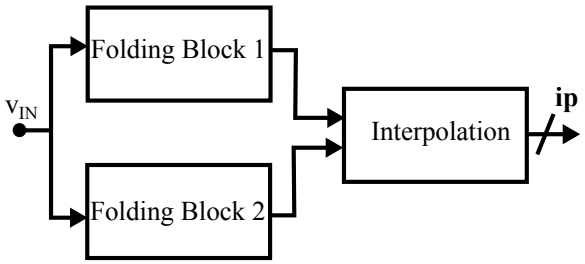


Figure 5.12: Analog processing block diagram

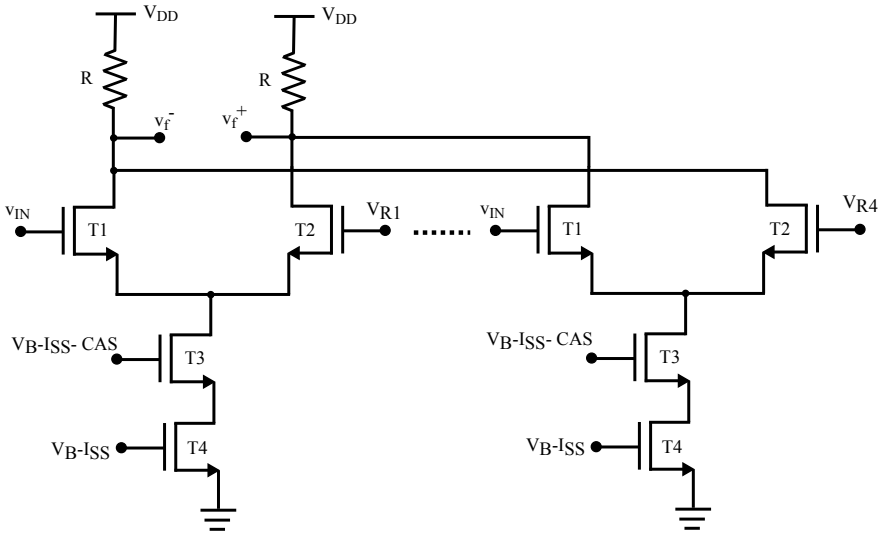


Figure 5.13: Folding block

In order to provide the bias-current for the differential pairs, a cascode configuration (formed by T3 and T4) is used to set a high output impedance for the current source. This topology then ensures a lesser sensitivity of the bias currents relatively to the common-mode voltages at the sources of all T1 and T2. If not done so, it would be much more difficult to match the currents in all differential pairs, because each common-mode voltage is different. Such mismatch leads to asymmetric folding characteristics, increasing the static nonlinearities of the final ADC. The signal v_{IN} is connected to one of the inputs of the differential pair, and the other input is connected to a reference voltage ladder. In an ideal folding case, as shown in Fig. 5.2, a full scale input signal should be folded with a triangular characteristic. In a practical case, the triangular edges

are rounded at the peaks. Fig. 5.14 shows the simulation result for the four cross-coupled folding circuit in Fig. 5.13. For a better understanding how the circuit works, the characteristic of two isolated differential pairs is plotted in Fig. 5.15, taken from opposite branches of the differential pairs. If those characteristics are added, the result is the first folding shape. The remaining shapes can be obtained by adding more differential pairs shifted in voltage, set by V_{R1} to V_{R4} in Fig. 5.13 and given by the weighting defined in (5.3).

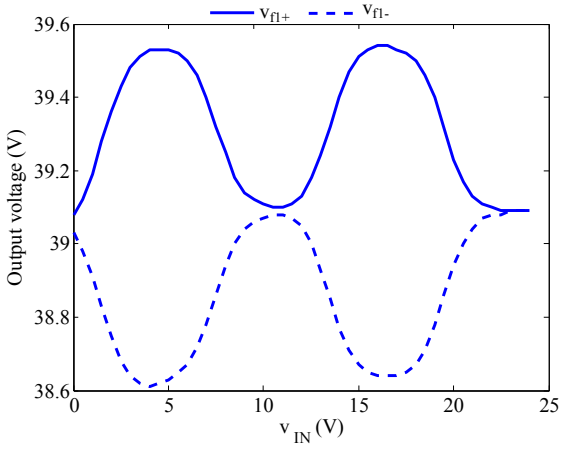


Figure 5.14: Folding block response

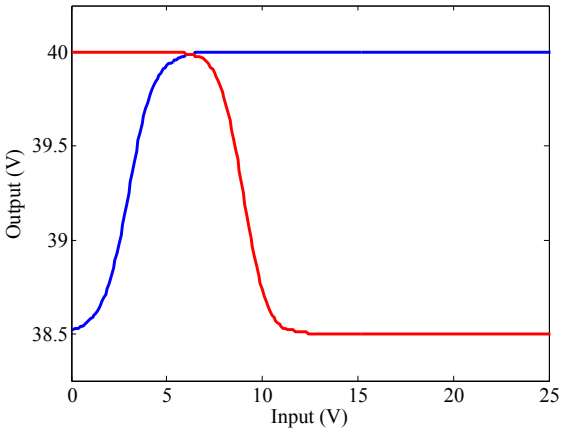


Figure 5.15: Characteristics of two isolated differential pairs for folding generation

$$V_{R1} = V_{FS} * \frac{1}{16}; V_{R2} = V_{FS} * \frac{5}{16}; V_{R3} = V_{FS} * \frac{9}{16}; V_{R4} = V_{FS} * \frac{13}{16}; \text{where } V_{FS} = 24V. \tag{5.3}$$

5.3 Folding ADC Characterization

The final designed ADC has 4 folding edges. The reason behind limiting to 4 has to do with the maximum operating voltage. As it can be noticed from Fig. 4.26, the differential amplifier has a linear range defined at the input by $\pm\sqrt{I_{SS}/K}$. Since the intrinsic mobility of the a-GIZO TFTs is

much smaller than crystalline silicon, K is also much smaller, then the linear region spreads over a wide input range. Hence, if many folding edges are added, the full scale of the ADC can get very high. In fact, the input full scale voltage, in this case, goes from 0 to 24 V, which is already too high, but expectedly it may become smaller as technology evolves. This means that the coarse conversion will be limited to two bits. The fine conversion was also set for two bits. This way the demand on the interpolation circuit will be relaxed (as will be seen next). If the final linearity results in an equivalent number of bits bigger than four, then one may conclude that probably a higher resolution ADC can actually be accomplished.

As referred earlier, the block diagram of the folding ADC is represented by Fig. 5.3. The final implementation contains a two-bit coarse and fine flash ADCs, which operate in parallel. The two-bit coarse/fine flash converter is shown in Fig. 5.16. The output bits are in gray code. An XOR operation over the MSBs – b4$\oplus$b3 – will then hold the information on the sign of the folding-edge slope where the input signal falls that is then used to assist the decoding of the LSBs.

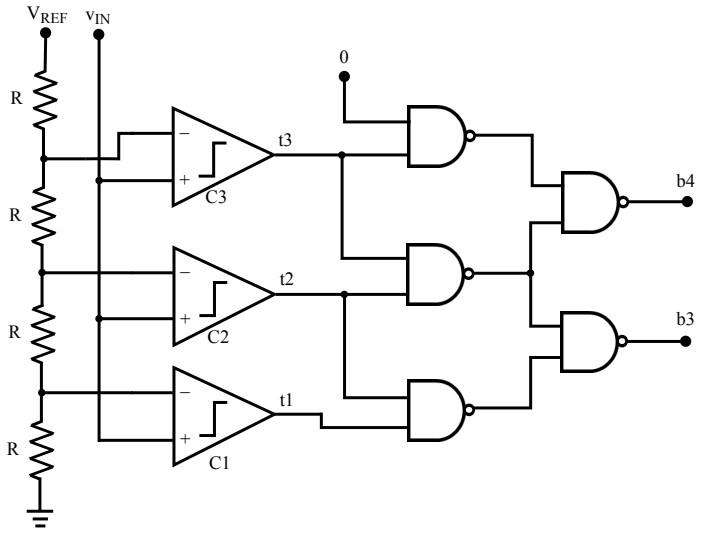


Figure 5.16: 2-bit flash converter for gray code

For the fine converter, the detected folding edge needs now to be quantized in a number of levels correspondent to the fine resolution. This can be accomplished by creating replicas of the folding characteristic, each separated by LSBs, in a number equal to the quantizing levels (minus one, assuming that the first level is zero), as represented in Fig. 5.17. It corresponds to a repetition of the folding circuit as many times as quantization levels (minus one). The output is applied to the two-bit flash converter that then will give the gray code correspondent to where the input lays in-between the zero crossings of the characteristic (zero crossing detection) in Fig. 5.17.

In order to minimize the complexity of the design, generically, less number of folding circuits can be used in conjunction with linear interpolators that synthesize the intermediate folding characteristics. This was the procedure adopted in the current design. Two folding circuits and an interpolator completes the analog-processing block in Fig. 5.12. The reference voltages for the folding blocks are given by (5.4), and the corresponding response shown in Fig. 5.18.

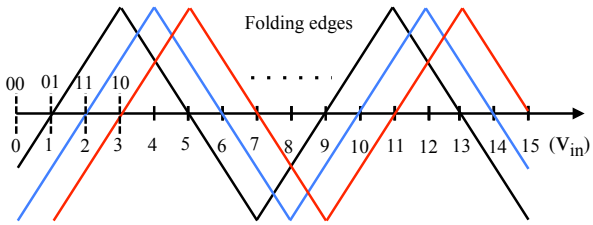


Figure 5.17: Folding signal showing different quantization levels (in gray code)

$$\begin{aligned} &\text{Folding block1: } V_{R1} = V_{FS} * \frac{1}{16}; V_{R2} = V_{FS} * \frac{5}{16}; V_{R3} = V_{FS} * \frac{9}{16}; V_{R4} = V_{FS} * \frac{13}{16}; \\ &\text{Folding block2: } V_{R1} = V_{FS} * \frac{3}{16}; V_{R2} = V_{FS} * \frac{7}{16}; V_{R3} = V_{FS} * \frac{11}{16}; V_{R4} = V_{FS} * \frac{15}{16}; \end{aligned} \tag{5.4}$$

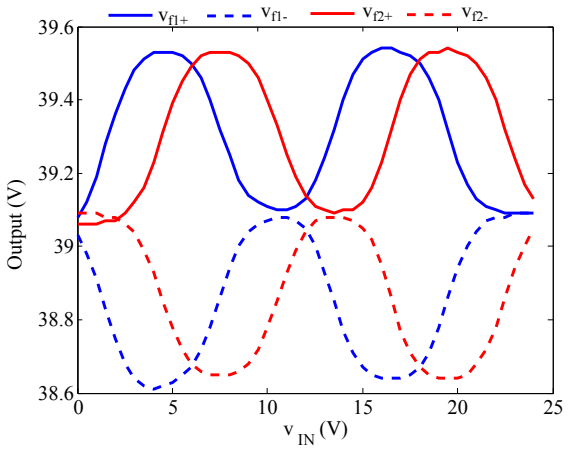


Figure 5.18: Folding blocks response

Fig. 5.19 shows the interpolation circuit made by a resistive ladder driven by a level shifter. The diode-connected transistors were placed to set each V_{GS} within safe limits (about seven Volts max). Fig. 5.20 presents the final folding characteristics with interpolation. It can be noticed that level shifter (and interpolator) causes distortion in the folding edges, nevertheless, to a good extent, the distance between zero crossings are preserved.

The complete ADC was simulated with the neural model. The response is found in Fig. 5.21, together with the ideal expected behavior. Differential non-linearity (DNL) and integral non-linearity errors are presented in Fig. 5.22. The maximum DNL and INL are -0.26 LSB and 0.31 LSB, respectively. The power consumption of the circuit is 24 mW. The ADC shows a 4.6 equivalent number of bits, revealed by the nonlinearities. The SNR (signal to noise ratio) and SINAD (signal to noise and distortion ratio) should also be characterized, however, such is only possible to be measured with an actual circuit, which is not yet available. Comparing the folding ADC with other related published results, listed in Table 5.3, the design could be said to be within the state of the art (with an expected high power consumption, typical of flash type converters).

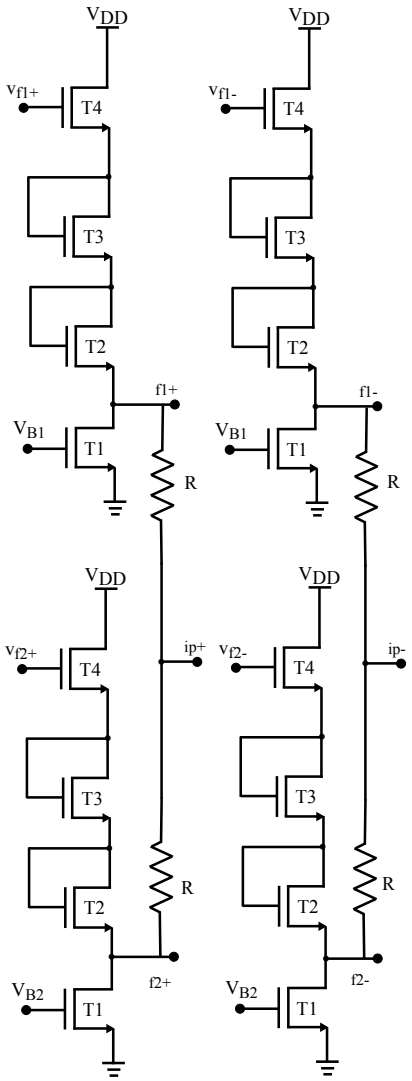


Figure 5.19: Resistive interpolation

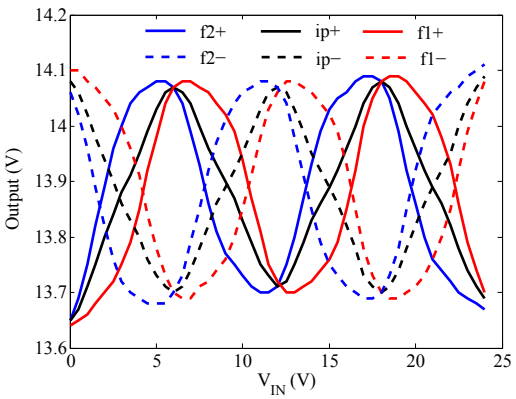


Figure 5.20: Folding characteristic with resistive interpolation

The conclusion on itself is not totally fair given the fact that all other reported results come from actual real measurements. Notwithstanding, it gives a good indication, with an acceptable degree of confidence supported on the results related to the model effectiveness, discussed in previous chapters.

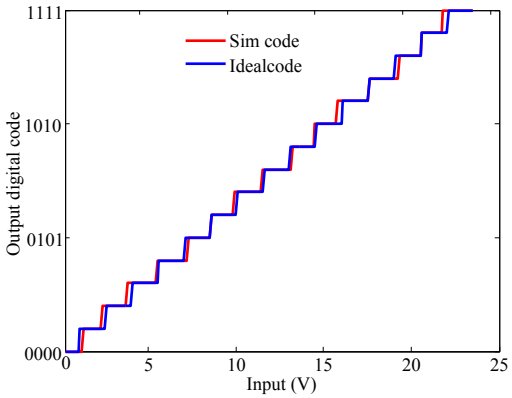
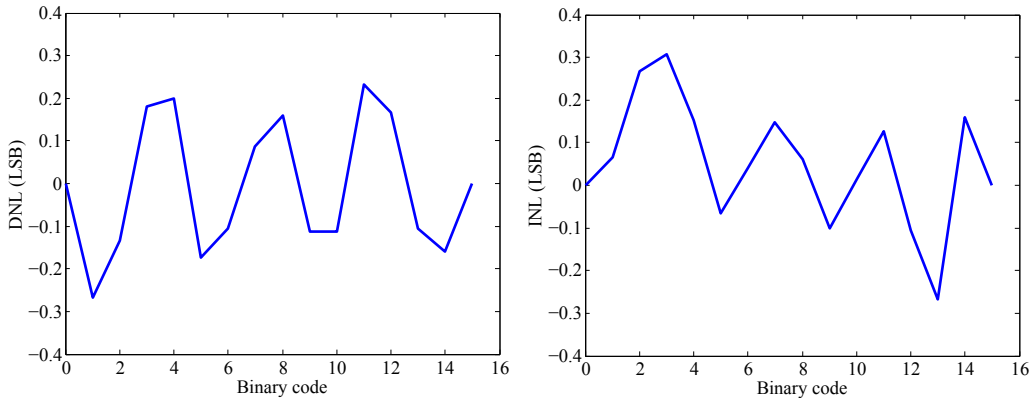


Figure 5.21: Comparison of ADC simulation response with the expected behavior



(a) DNL (b) INL

Figure 5.22: ADC performance from simulation

Table 5.3: ADC with different TFT technologies

Technology	Architecture	DNL (LSB)	INL (LSB)	Sampling frequency (Hz)	Power (mW)	Ref.
a-Si:H	Flash (5-bit)	± 1	± 1.8	2 K	13.6	[26]
OTFT	$\Delta\Sigma$	-	-	500	1.5	[28]
OTFT	Counting (4-bit)	0.24	0.42	4.17	0.5	[127]
OTFT	SAR (6-bit)	0.6	-0.6	10	0.0036 (excluding FPGA)	[27]
a-GIZO TFT	Folding with interpolation (4-bit)	-0.26	0.31	300	24	Current work

Chapter 6

Conclusions and Future Work

This chapter presents some conclusions and comments on the work developed for the PhD. dissertation, and some possible new directions to improve the effectiveness of circuit design with a-GIZO TFTs.

6.1 Conclusions

The major goal of this dissertation was the design of mixed-signal circuits with active devices based on AOS materials, more specifically a-GIZO, and to better understand its limitations and propose possible methods to circumvent them. The developed research contributes towards achieving an integrated system with single substrate, where the sensors and signal processing/conditioning circuits can be realized with the same technology. However, the technology in the present state still poses many challenges with respect to circuit design and development. To bring circuits into reality, accurate device models are required to predict not only static but also dynamic behavior of the devices, so that an effective circuit design-flow is accomplished. A compact model was then proposed to close this gap, developed from the measured characteristics of the device. If any changes are set in the fabrication process, a model can immediately be produced from the proposed platform, assisting a rapid electronics development as technology evolves. In this process, various types of neural modeling methods, such as MLP, RBF and LS-SVM, were experimented. The MLP network has shown the best balance in the trade-off between simplicity and complexity. The method was subsequently extended to a complete description that includes dynamics by means of an equivalent circuit model that brings dynamics through non-linear capacitors, and further implemented in Verilog-A for circuit simulation. Using the developed model to support the design, basic analog/digital circuits, namely, current mirrors, simple single-stage CS amplifiers, differential pair, adders, subtractor, level-shifter, logic gates, half-wave rectifier, were successfully characterized using a-GIZO TFTs. Different multiplier circuits were also simulated and then validated from actual measurements. A high-gain single stage amplifier, with single n-type enhancement transistors was described. The novel high-gain stage showed a 34 dB gain, when driving a load of 10 MΩ in parallel with 16 pF. To best of our knowledge, this is the highest gain reported so

far for an a-GIZO TFT single-stage amplifier. Finally, a 4-bit folding ADC with interpolation was designed. This ADC promises -0.26 LSB DNL and 0.31 LSB INL from simulations. Together, a multistage comparator was proposed. Simulations indicates that it may achieve a gain of 55 dB, with a sensitivity of 32 mV for an output swing of 3V, which is enough to trigger a digital logic gate.

6.2 Future directions

6.2.1 Modeling

The developed models can characterize the static and dynamic behavior of the device. However, during integrated circuit fabrication, mismatches between identically designed devices will impact on performance. Thus, corner and Monte-Carlo analyzis is also important to maximize circuit robustness to process variations and thus improve yield. The development of models to include statistical simulations will imply the inclusion of physical insight to the models, with some parameters having some explicit physical meaning. Probably the best choice would be a semi-empirical approach, where a balance between accuracy and simplicity is achieved. However, one should be aware that in a still emergent technology, building a standard model is not a very viable option. In addition, basic understanding of the noise sources and models are required for good analog circuit design. Thermal (white) and flicker (low-frequency or 1/f) noise are two important categories that influence the circuit figures of merit. Although, a significant progress was made in noise modeling and characterization of CMOS devices [132], for more than a half century, there is still little contribution towards characterization of a-GIZO TFTs [34, 133, 134].

6.2.2 Circuit Design

Compared to the other TFT technologies, namely, a-Si:H and OTFT, the maturity level of oxide based (a-GIZO) TFT technology, in terms of generic circuit design, is still quite limited. Nevertheless, as discussed earlier, a-GIZO devices present a set of features that beat many of other TFT electric characteristics. It is worthwhile investigate other means that may take advantage of such properties. Passive devices can be designed in AOS technologies. The realization of active filters, through means of switched capacitor techniques, can achieve well precise time constants and opens the opportunity for the design of switched amplifiers for power efficient, but more importantly, to reduce the bias stress in the amplifiers, prolonging the lifetime of the electronic systems in use. Such technique would open the window for the design oversampled converters, using Δ-Σ modulators to increase the bit resolution.

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Appendix A

Master thesis co-supervised

A.1 DC-DC converters

DC-DC converters for PV panels are one of potential applications of TCO based TFT technology. In this work, positive DC-DC converter has been developed with transparent a-GIZO TFTs. This work was mainly focused on inductor-less positive DC-DC converter, because of limitations associated with the technology in realizing inductors with near ideal behavior. Different types of DC-DC conversion techniques were studied and simulated with the TFT neural model, in order to design high performance DC-DC converter. The final design has 10 DC-DC converters working in parallel and a regulator to reduce the voltage ripple at the output. This novel design promised an output voltage of 27.8 V, when the input voltage 10 V. Whereas, a single DC-DC converter resulted an output voltage of 16.37 V, for the same input. The circuit also includes an amplifier with a voltage gain of 36.7 dB and 83.79^o phase margin. The regulator designed in the final circuit promises a decrease of 80% in voltage ripple from simulations.
Student : Romano Jorge de Sousa Torres

A.2 Analog Circuit Design with Transparent Electronics

A comparative study of single stage high-gain amplifiers, only with n-type enhancement transistors was carried out as a first step. Then, a novel high-gain stage is proposed that can amplify DC signals. This stage is employed in the fully differential operational amplifier (opamp). Other stages of the opamp were also designed in order to enhance gain further. Common-mode feedback was used to reduce gate bias stress impact. From simulations, a gain of 57.26 dB is noticed. Since the developed Opamp initially presented a negative phase margin, several compensation schemes were experimented to compensate the circuit. Final design after frequency compensation has shown a stable phase margin above 60^o. In order to reduce the bias stress further, the opamp developed from this work is used as switched operational amplifier, with pulsed biasing. In addition, the switch opamp is used to realize a sample and hold circuit.
Student : Bruno Filipe Guedes da Silva