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High-Efficiency Linear Transmitters for Mobile Communication Systems

by

Cândido Duarte

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of the requirements for the degree of

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– Declaration of Authorship –

I declare that this thesis and the work presented in it has not been previously submitted for a degree at the University of Porto or any other university and I further declare that the work embodied in it is my own, or else clearly attributed.

Cândido Duarte

Abstract

This thesis presents a new wireless transmitter architecture in which both Cartesian and polar topologies are merged into a single structure, herein termed "Cartesian-Polar (C-P) architecture." By exploiting the main advantages of both topologies, the proposed transmitter aims at linear and efficient amplification of signals with high peak-to-average power ratios. Switching-mode polar amplifiers are employed with bipolar envelope modulators targeting high efficiency. These power stages also operate as high-level quadrature modulators, where the I and Q baseband signals directly modulate the dynamic power-supply. Compared to the polar architecture, the now proposed C-P transmitter shows reduced bandwidth requirements for both the envelope amplifiers and PAs. The C-P also compares favorably to the LINC architecture in terms of power efficiency and spectrum regrowth due to impairments in the RF paths.

In the present research, the feasibility of implementation of the proposed arquitecture is addressed. Two circuits are studied, as distinct implementation solutions for the PA stages of the C-P architecture. The first circuit consists of a CMOS-PA topology operating in class E with bipolar envelope. A comprehensive analysis is presented, briefly addressing asymmetries of relevant parameters in the RF performance. In a second circuit proposal, an LDMOS topology is addressed. It consists of a switching-mode circuit operating either as an oscillator or amplifier, depending on the power supply. It allows the rejection of common-mode components of two dynamic power-supplies, while the differential mode is amplified. For each of the two topologies included in a C-P architecture, the efficiency is shown to be higher than a LINC transmitter for output signals considerably lower than the peak power.

Resumo

A presente tese apresenta uma nova arquitetura de transmissão RF onde as configurações cartesiana e polar são combinadas numa única, aqui denominada "transmissor Cartesiano-Polar (C-P)." Ao explorar as principais vantagens de cada uma das arquitecturas, o transmissor proposto visa a amplificação linear e eficiente de sinais com elevados rácios entre a potência de pico e a potência média. Para obter alta eficiência são utilizados amplificadores comutados em que a envolvente é bipolar. Estes andares de potência também funcionam como moduladores de quadratura de alto nível, onde a tensão de alimentação dinâmica dá-se pelos sinais IQ. Em comparação com o polar, o transmissor proposto mostra requisitos de largura de banda mais reduzidos, tanto para o amplificador de envolvente como para o PA. O C-P também se compara favoravelmente com o LINC em eficiência e resposta espectral devido a desigualdades nos caminhos RF.

Na presente investigação estuda-se a viabilidade de implementação da arquitetura proposta. São estudados dois circuitos distintos como possíveis soluções de implementação dos PAs no C-P. A primeira proposta é um circuito CMOS a operar em classe E com envolvente bipolar. É apresentada uma análise detalhada, abordando assimetrias de parâmetros relevantes no desempenho RF. O segundo circuito é uma configuração LDMOS. Trata-se de um circuito de comutação que opera como oscilador ou amplificador, dependendo da tensão de alimentação. O circuito permite a rejeição de componentes de modo comum de duas fontes de alimentação dinâmicas, sendo amplificado o modo diferencial. Em cada um dos dois circuitos, incluídos em arquiteturas C-P, mostra-se que a eficiência é superior à de um LINC com sinais de saída muito menores que a potência de pico.

In memory of my grandfather,

Alexandre Duarte

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Chapter 1

Introduction

On the lookout for new mobile applications, the telecommunication markets are continuously demanding for higher and higher data rates [1–3]. Conversely, the available frequency bandwidth is relatively limited. The regulated wireless spectrum is shared by numerous subscribers and different communication standards coexist in a wide variety. With such a crowded medium, improving transmission data rates requires spectral-efficient communication schemes, such as those adopted in latest wireless technologies.

Nowadays, advanced digital modulations are commonly employed with pulse-shaped data, e.g. using root or square-root raised cosine filtering. This prevents intersymbol interference (ISI) in detection, and also provides a nearly-rectangular format for the spectrum emission [4]. Modern communications may also comprise other techniques for reducing the sensitivity to multi-path fading and frequency-selective interferences. These are often combined with multi-carrier modulations, such as OFDM[1] used in WiFi IEEE 802.11 (a/g/n), WiMAX, DVB and DAB, along other recent technologies. However, such sophistication comes at a relatively high cost. It ensues a non-constant envelope in the radio frequency (RF) signals to be transmitted. That is, confining large amounts of data in the available channel bandwidths is possible, but requires proper amplitude modulation of

[1]For the sake of clarity, acronyms/abbreviated terms for modulation names and communication standards were not spelled out in its first use, because they tend to have very long terms. These are however included in a complete list provided in page 161.

PM/FM signals [5]. Hence, a time-varying envelope, as in typical OFDM systems, entails great linearity requirements in the transmitter (Tx) architecture. In fact, this implies that the transmitted power must not interfere with adjacent channels, otherwise the spectral efficiency would be adversely lowered. Additionally, the near-far problem also limits the channel capacity. To supress shadowing effects, all the mobile units are required to regulate their output powers. This way the interference with other similar mobile equipments is kept to a minimum [6]. The power control is actively applied within some sort of slow feedback. As a result, there is a significant variation of transmitted power levels, although in a time scale much larger than that from the envelope itself. Generally, this effect has no severe implications in terms of linearity, but it raises some efficiency concerns due to the need for a long-term regulation in power supply [7].

Energy efficiency is another factor that plays an important role in current days. In the case of wireless portable devices, in which the energy is already a scarce resource, an ever increasing number of software applications and multiple radio interfaces share the same battery as power supply. Extended operation or smaller battery sizes can only be attained by reducing the overall power dissipation. As a major concern, energy efficiency should be taken into consideration since the early phase of the architectural definition for the RF transmitter, i.e. having in mind the design of its constituent circuits. In fact, this is becoming a critical issue in new wireless products. The semiconductor industry foresees the reduction of one order of magnitude in power consumption as one of the most apprehensive challenges in forthcoming years [8]. Needless to say, any of these technological innovations must be accomplished without slowing down current data communication trends.

To a certain extent, high spectral and energy efficiencies depict contradictory scenarios in the performance of any wireless transmitter system. This is commonly known as the linearity-efficiency compromise [9]. Along the current dissertation, this kind of tradeoff is investigated from the

viewpoint of the transmitter architecture and respective circuits. A novel architecture is addressed, with circuits proposed for its practical implementation. The main goal is to obtain a feasible solution in which the tradeoff between linearity and efficiency can be further improved.

1.1 Linearity-Efficiency Compromise

Traditionally, in transmit mode, the power amplifier (PA) represents the most significant share of power budget in a wireless transmitter. The most conventional linear classes A, AB and B are quite common in amplification of time-varying envelope signals. However, the major drawback of these classes is their low efficiency. Notwithstanding the PAs operating in classes A or B achieve drain efficiencies up to 50 or 80 %, respectively, these theoretical values are solely valid at peak power. The drain efficiency rapidly drops when the transmission power is reduced to mid-range values [10]. This is strongly reflected on the average power usage-efficiency (η_{avg}), defined as the ratio between output and input average powers [11],

$$\eta_{\text{avg}} \triangleq \frac{\langle P_{\text{out}} \rangle}{\langle P_{\text{dc}} \rangle} = \frac{\int_0^{P_{\max}} P_{\text{out}} \cdot f(P_{\text{out}})\, \mathrm{d}P_{\text{out}}}{\int_0^{P_{\max}} P_{\text{dc}}(P_{\text{out}}) \cdot f(P_{\text{out}})\, \mathrm{d}P_{\text{out}}} \tag{1.1}$$

where $f(P_{\text{out}})$ is the probability density function (PDF) of the output power.

In the majority of sophisticated communication standards, most of the time it is required that the transmitter operates at a level well below the peak envelope power (PEP). As a practical example, Fig. 1.1 shows the PDF for the reverse link of an IS-95 CDMA transmission profile, from field measurements in an urban area [12]. The most probable power level is about 25 dB lower than the PEP of ∼0.5 W. Indeed, this implies a very high[2] peak-to-average power ratio (PAPR). It means that the PA must be

[2] About 6 dB are due to the O-QPSK modulation and pulse shaping, whereas the remainder are due to long-time regulated operation [13].

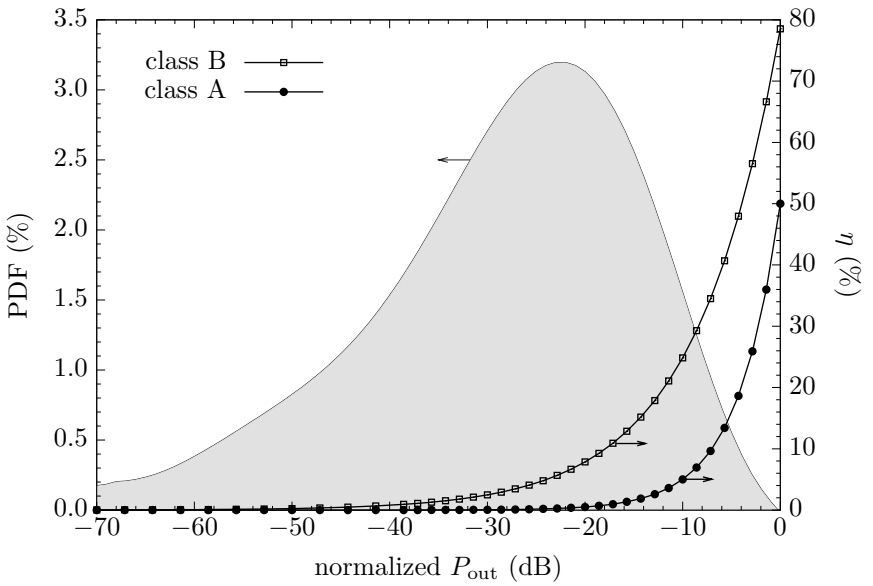


Figure 1.1: CDMA PDF [12] and efficiencies of classes A and B.

designed far from peak envelope operation to accomodate a wide dynamic range.

The back-off (B-O) level from the saturated power has direct impact on the overall efficiency. In Fig. 1.1, the power efficiency is also depicted for ideal classes A and B at different output power levels. Graphically, comparing the efficiency dependence on P_{out} with the CDMA PDF, an overall drain efficiency of solely 2 % comes at no surprise for the case of a typical class-AB PA operating in the present context [7, 14].

Reducing the output B-O leads to compression in the envelope. Although it improves the efficiency, also degrades the linearity. This compromise between power efficiency and linearity is quite noticeable in these conventional PA classes. It basically resides on the fact it is not possible to maintain a constant gain irrespective of the output power level. The efficiency in class A decreases with $P_{\text{out}}/P_{\text{max}}$, whereas in class B depends on $\sqrt{P_{\text{out}}/P_{\text{max}}}$. In practical terms, depending on the communication standards, the B-O can be slightly reduced by allowing some signal clipping that still meets the error vector magnitude (EVM) and packet error

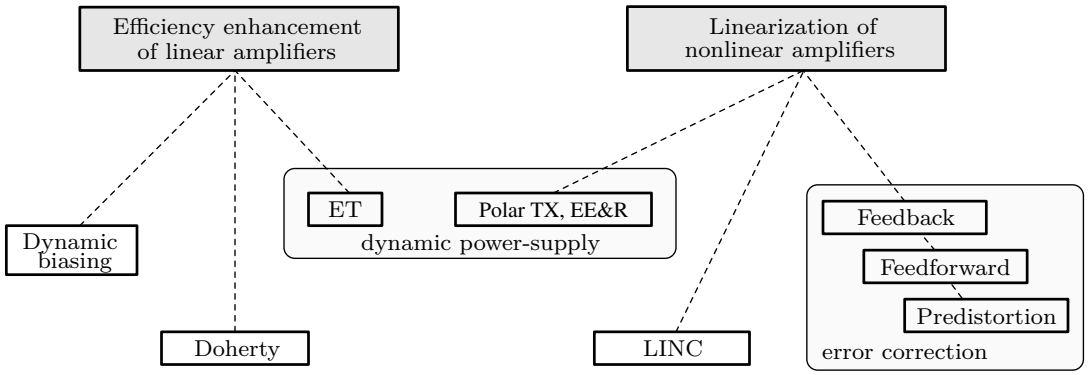


Figure 1.2: Existing techniques to overcome the linearity-efficiency tradeoff.

rate (PER) [15, 16]. However, this workaround is often not sufficient for satisfactory improvements on the linearity-efficiency compromise.

The energy efficiency is improved whenever the PA operates under strong nonlinear regimes. To the greatest degree, the transistor acts as an RF switch. In principle, high efficiencies can be attained using switching-mode PA (SMPA) classes, such as D, E, and F. This is possible because of the minimum overlapping between current and voltage across the switch. Theoretically, SMPAs offer the possibility to obtain drain efficiencies well above 80%, i.e. above the limit for ideal classes A to B. Nonetheless, as the power drawn from power-supply spreads over the frequency spectrum, the spectral efficiency is sacrificed. In fact, SMPA classes can only find a straightforward application in modulations for which the envelope is constant (e.g. GSM systems). For amplitude modulation, the switching-mode topology requires adequate modifications, which brings the linearity issues back into play.

In essence, there have been two distinct strategies on dealing with the linearity-efficiency tradeoff. One of those approaches relies on the efficiency enhancement of linear amplifiers, while the other consists of improving the linearity on efficient transmitters. As depicted in Fig. 1.2, numerous techniques can be divided between both approaches. Linearization techniques such as feedback, feedforward and predistortion are herein categorized as error correction methods. Such techniques are associated

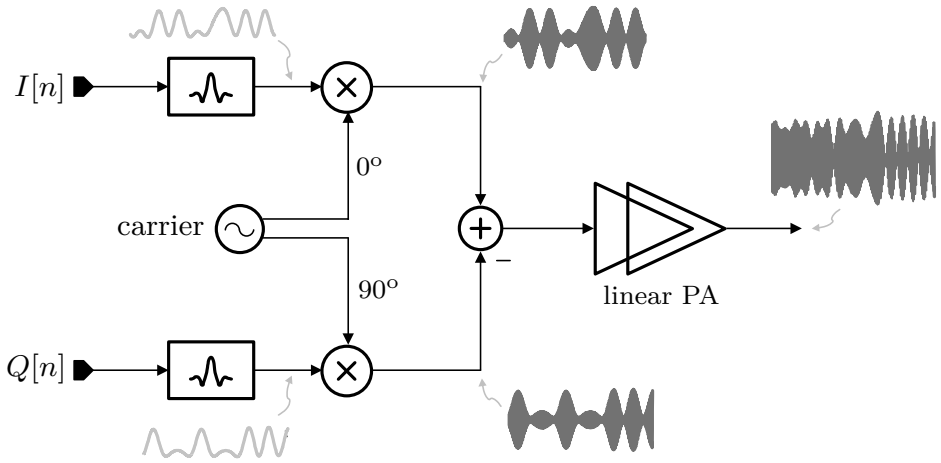


Figure 1.3: Cartesian (IQ) Tx.

to significant drawbacks [17]. For instance, RF feedback requires excessive loop-bandwidth to ensure stability. Since this is rather complex to achieve in practice, linearization at RF is performed at an intermediate frequency (IF) or baseband using down-conversion mixers within a feedback loop [18]. The feedforward linearization also meets pratical implementation difficulties, in particular due to misalignments between RF paths [19]. Predistortion is perhaps the most successful scheme in reducing effects of nonlinear distortion on the performance of some systems [20]. It can be applied digitally and in conjunction with other systems, e.g. Doherty amplifier [21], but its main drawback is the difficulty on obtaining the inverse transfer function of the PA. In envelope tracking [22] and dynamic biasing [14], the power supply and/or bias voltages are controlled so that the PA operates close to saturation. Instead, in the Doherty amplifier, the load is actively modulated to improve the efficiency [23–26].

Traditionally, most of the transmitter implementations are based on the Cartesian (or IQ) architecture, because it is well suitable for the amplification of non-constant amplitude signals. Fig. 1.3 shows a simple block-diagram representation of the Cartesian transmitter. The in-phase (I) and quadrature (Q) signals are combined resulting in an RF signal with time-varying envelope, which is then amplified using a linear PA. But, as men-

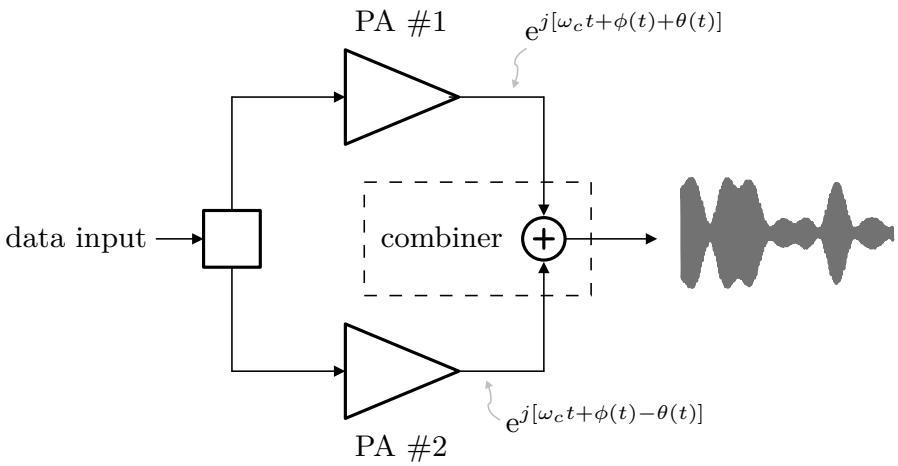


Figure 1.4: LINC Tx.

tioned, due to high PAPRs the required power B-O significantly lowers the overall efficiency. This makes the IQ transmitter less attractive for modern high data-rate systems.

Linearization of SMPAs mostly implies the modification of transmitters at an architectural level. Lately, this has driven research and industry into the renaissance of amplitude modulation architectures, some of which were proposed still in the early days of radio. The LINC (linear amplification using nonlinear components) is such an example [27]. Fig. 1.4 shows the representation of a LINC transmitter system. It is based on the outphasing principle [28], in which two phase-deviated signals with constant amplitudes are combined to generate non-constant envelope signals. Hence, high-efficiency SMPAs can be used.

Recently, this technique has received renewed interest because apparently the efficiency can actually improve without great impact on linearity [29, 30]. The linearity-efficiency problem has been universally focused onto the PA, but the LINC concept embraces a distinct approach. First, it requires that the input data is translated in a specific way to provide constant-envelope signals for the use of SMPAs. Then, the linearity-efficiency compromise is more constrained by the output combining of the two PAs than the PAs themselves [31–33].

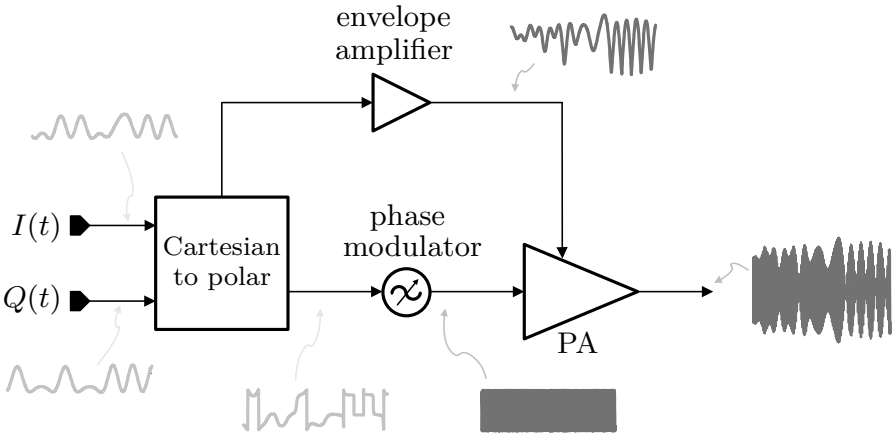


Figure 1.5: Polar Tx.

Power combining the two PAs of the LINC transmitter demands isolating and lossless passive networks. However, there is no theoretical possibility to meet these requirements simultaneously [34]. Therefore, one option is combining the PAs with lossy networks that isolate the outputs of each amplifier. In this case, the linearity should not be compromised, although the efficiency depends on the power combiner. The other solution is to use a non-isolated power combiner so that the efficiency can be improved, but at the expense of linearity. That is, each amplifier contributes to the impedance seen by the other (i.e., dynamic load modulation) and the gain is no longer preserved constant. As a result, nonlinearity is induced in the overall performance of the transmitter.

Fig. 1.5 depicts the polar transmitter, which is another promising alternative to Cartesian transmitter. As in the LINC, it also tackles the linearity-efficiency compromise by introducing modifications at the architectural level. That is, the IQ signals are converted into PM and AM signals. In the PM branch it is possible to use efficient PAs, whereas the linear amplification of the envelope is accomplished by drain modulation. As in the LINC, the net result from the combination of RF signals is a linear transmitter using a nonlinear PA.

Although the output waveforms at the load for any of these architectures

are the same (for the same data input), the signal characteristics of the analog paths are quite distinct. The digital data consists of I and Q symbols filtered at baseband. This is accomplished by pulse-shaping filters that limit the bandwidth occupied by data pulses. The bandwidth in the branches of the IQ modulator is imposed by the spectrum of pulse-shaped signals. However, as the conversion between Cartesian and polar coordinates takes place, the resulting signals are no longer limited in spectrum. As a result, in a polar transmitter the envelope $|A(t)|$

$$|A(t)| = \sqrt{I^2(t) + Q^2(t)} \tag{1.2}$$

and phase signals $\phi(t)$

$$\phi(t) = \tan^{-1}\left(\frac{Q(t)}{I(t)}\right) \tag{1.3}$$

are wider in spectrum than the input signal itself. The circuits in the two analog paths have to deal with incredible large bandwidths to drive the PA. The envelope modulator, which is often implemented with switching-mode topologies, demands excessive oversampling ratios [35–38]. As the sampling frequencies get higher, also the associated switching-losses increase. Moreover, any time misalignment between phase and envelope paths degrades linearity as it results in spectral regrowth.

Table 1.1 summarizes some of the characteristics of Cartesian and polar transmitters. There is a compromise between efficiency and demanded input bandwidth in both architectures. Nevertheless, balancing these characteristics is not straightforward. It requires structural modifications in the architectures to expand the degrees of freedom in the overall efficiency-linearity tradeoff.

Such classical tradeoff has always been a challenge in the RF research. The growing demand for increased data rates has been driving investigation into different solutions in wireless architectures. Most works attempt improving the RF performance of linear transmitters either introducing

Table 1.1: Pros "+" and Cons "−" of Cartesian and polar transmitters.

	Cartesian	**Polar**
Bandwidth	+ Narrow bandwidth in the I and Q baseband signals.	− Extensive bandwidth in typical $\|A(t)\|$ and $\phi(t)$ signals.
Efficiency	− Low-efficiency due to the mandatory use of conventional linear PAs at constant V_{DD}.	+ High-efficiency in the PA due to possible use of dynamic biasing in linear classes or drain modulation in switched-mode PAs.

digital control techniques, or modifying the architecture itself – or even both ways. To address likely divergences on the linearity and efficiency requirements, the present thesis addresses the complete structure of a new transmitter, which is based on slight modifications of the classical Cartesian architecture.

1.2 Cartesian-Polar Transmitter

The present thesis aims at studying the implementation feasibility of a novel transmitter architecture, herein termed "Cartesian-Polar (C-P) transmitter". As described next, the proposed architecture presupposes particular specifications, which require the investigation of circuit topologies suitable for a hardware realization.

Basically, this new transmitter scheme explores the benefits of polar and Cartesian architectures. As shown in Table 1.1, both offer distinct and interesting features, which motivated the current research work. The proposed solution is a combination of the two transmitter architectures. Without degrading efficiency, the proposed architecture aims at surpassing the typical drawbacks associated with the wide-bandwidth requirements in the analog paths of the conventional IQ transmitters.

In a polar architecture, one of the underlying causes for large band-

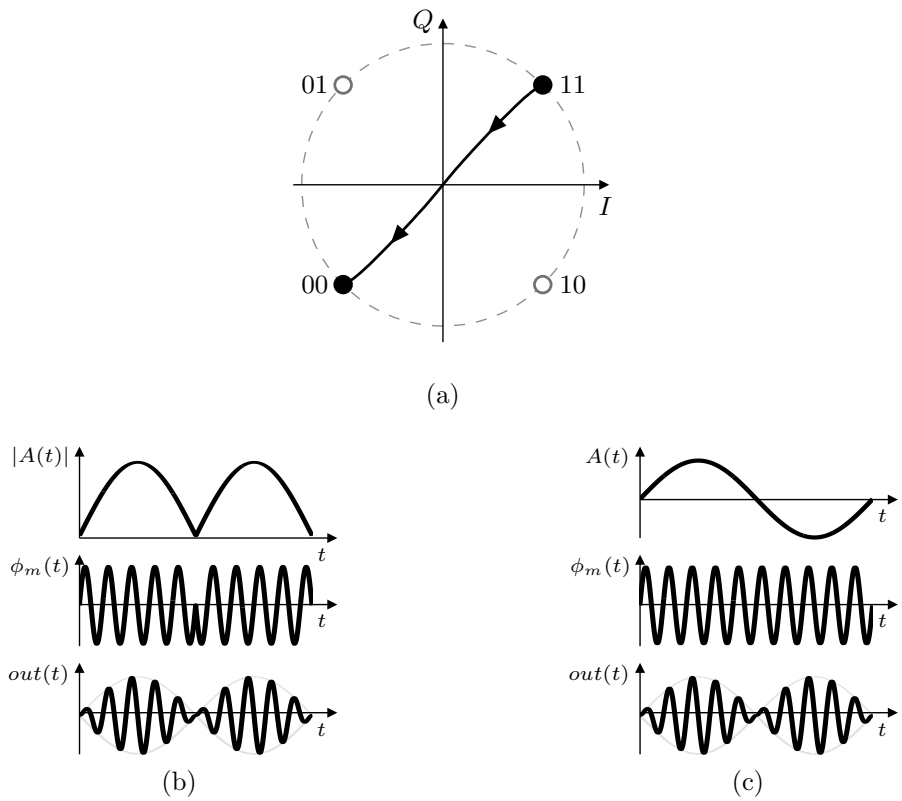


Figure 1.6: Representative waveforms for an (a) IQ zero-crossing in a (b) typical and (c) modified transmitter.

widths in phase and amplitude signals is the zero-crossing in an IQ diagram. Fig. 1.6(a) exemplifies such a case. In the conventional polar architecture, this leads to a phase reversal and an abrupt change in the envelope, as depicted in Fig. 1.6(b). To overcome this problem, it is proposed a different scheme in which the envelope is treated as a bipolar signal. Fig. 1.6(c) illustrates how such basic modification alleviates the bandwidth problems mentioned previously. Clearly, there are no abrupt changes in the signals. However, the generation of the required negative-valued envelope, and respective PM signal, cannot be obtained in a simple way. A slightly different approach and more adequate is therefore applied. Hence, if this type of amplifier is thought as a multiplier, an IQ transmitter can be actually implemented based upon the combination of two of these "bipolar transmitters". The most obvious advantage over the classical Cartesian[3]

[3]The terms "Cartesian" and "IQ" transmitters will be used interchangeably along the text.

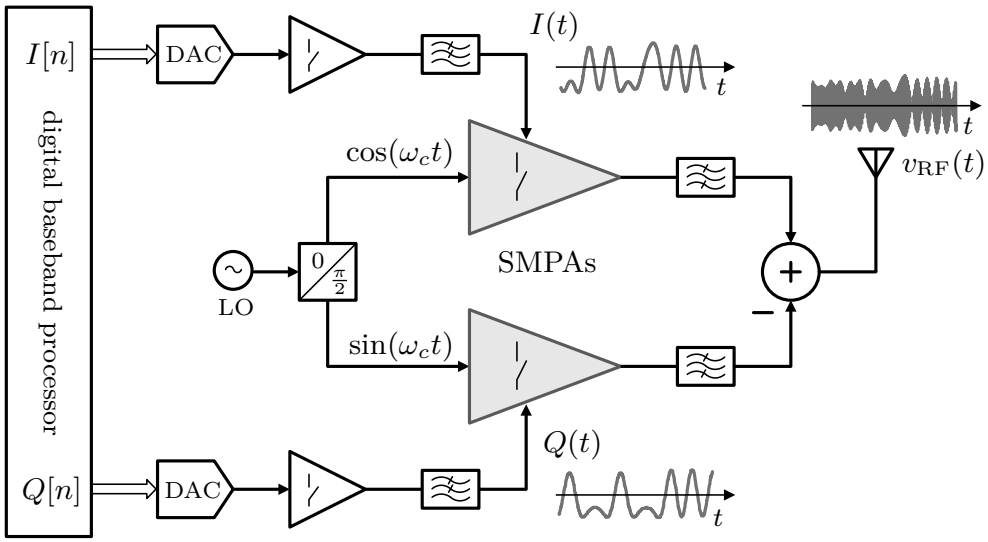


Figure 1.7: Proposed architecture.

transmitter is that now one can employ SMPAs to improve the overall efficiency.

Fig. 1.7 depicts the proposed topology for the C-P transmitter, wherein each bipolar transmitter is driven by single tones in quadrature. Hence, the amplifiers (or power mixers as we might call them) are driven by narrow-band signals. These signals have constant amplitude and thus allow the use of SMPA classes. Instead of an envelope signal, the I and Q signals modulate the power-supply of the bipolar amplifiers. This way, the drain modulation is performed by baseband signals that are limited in spectrum due to pulse shaping. As so, the bandwidth requirements of the envelope paths are much more relaxed than in the conventional polar transmitter, which allows an easier implementation of power supplies operating in switching mode. Hence, with this new architecture the bandwidth issues of the common polar transmitter are virtually solved, and low-efficiency of the IQ transmitters is also avoided. Compared to a LINC transmitter, as it will be demonstrated latter, the proposed C-P structure presents some benefits in terms of overall efficiency. It overcomes practical limitations of the LINC when dealing with signals having large PAPRs, an issue that has been restricting its use with modern communication standards.

1.3 Original Contributions

In this thesis, the proposed C-P architecture is analyzed at a system level and from a hardware design perspective as well. Two circuit topologies are proposed for the implementation of the C-P transmitter. In short, the main contributions of the present work are the following:

- introduction of a novel architecture, named "C-P transmitter". This architecture consists of a high-level multiplier and envelope modulator. It aims the use of efficient SMPAs, while avoiding typical bandwidth limitations in the envelope amplifiers.

- the structural analysis of the proposed architecture in terms of performance, e.g. efficiency (proven to be advantageous for high B-O), power recycling, and impairments sensitivity.

- proposal of a CMOS circuit for practical realization of the C-P transmitter, comprehensive study of its performance, validation through simulation and comparison against a LINC implemented in the same CMOS process.

- proposal of a new switching topology for the realization of a C-P transmitter for semiconductor technologies other than CMOS. The circuit provides up-conversion of the differential components of time-varying power supplies.

1.4 Outline

Following this introductory chapter, this thesis comprises other five chapters, which can be briefly described next.

- **Chapter 2** gives a brief reference on wireless systems and current trends for data improvement. It addresses the fundamental aspects

as well as the latest developments in transmitter technologies and architectures.

- **Chapter 3** presents the proposed transmitter architecture on a system level perspective. The system is studied in terms of bandwidth, efficiency and linearity. These characteristics are further compared to the LINC and polar transmitters.

- **Chapter 4** describes a circuit topology for implementation of the proposed transmitter architecture using CMOS processes for the active devices. A comprehensive analysis of the circuit is presented, describing the impact of different parameters in the asymmetric performance of the C-P transmitter.

- **Chapter 5** presents the study of another circuit for the implementation of the C-P transmitter. The analysis of the circuit includes the derivation of waveforms equations and computation of the electronic components for the circuit. An LDMOS implementation is addressed for its conceptual validation.

- **Chapter 6** concludes this thesis with final remarks on the presented research work and a discussion on future work.

Chapter 2

Transmitter Architectures

Wireless communication is perhaps the best example of a technology having fast global spreading and development. Today's systems encompass a wide range of easy-to-use RF technologies and services – from GPS and Bluetooth to WiFi and DVB. Numerous developments point towards ubiquitous wireless accesses in future, with device interfaces operating at much higher data-rates. This high-speed communication trend is crucial to achieve real-time responsiveness in wireless services. However, such demands push the linearity requirements to the limits of performance of AM transmitters.

The improvements on the spectral efficiency of wireless communications are dependent on the technical progress at successive levels, i.e. from the RF network system, to the transmitter and receiver architectures, and respective hardware implementations. Briefly, the present chapter focuses on the fundamental aspects related with RF transmitters, in terms of architecture and circuit implementation. It departs from the most conventional transmitter structure, i.e. the IQ transmitter. It then describes other transmitters that, despite being considered as classical architectures (from a historical perspective), they recently gained momentum with the need for high-performance AM systems. A few ways for improving the transmitter front-ends are also described, such as RF circuits for the synthesis of AM signals, as well as the use of digital control on the PA stage.

2.1 IQ Transmitters

Most transmitters are based on Cartesian coordinates to transmit digital information. In-phase and quadrature data paths are combined and then amplified by a PA at the end of the transmitter chain. In an IQ transmitter, the RF signal can be described by band-limited I and Q components as

$$x_{\mathrm{RF}}(t) = \mathrm{Re}\left\{[I(t) + jQ(t)] \cdot \mathrm{e}^{j\omega_c t}\right\} \tag{2.1}$$

$$= I(t)\cos(\omega_c t) - Q(t)\sin(\omega_c t) \tag{2.2}$$

For non-constant envelope signals, the combination of I and Q components needs to be amplified by linear PAs. However, in conventional transconductance-mode classes (such as A, AB and B) the efficiency strongly depends on the PAPR. That is, the PA must be designed with reasonable B-O from its maximum output power to ensure that the peak power can be achieved within a linear operation range.

Typically, the maximum drain efficiency will most likely occur at maximum output power. However, since most of time the PA operates at power levels much lower than its maximum, high-PAPR values lead to very reduced power efficiencies. Typical PAPR values for commercial standards are in the order of 3.4 dB for EDGE, 3.1–6.5 dB in W-CDMA, and more than 10 dB for systems using OFDM. When highly-linear PAs are used, the power-added efficiency (PAE) values are below 30–40 % [39, 40].

For a long time, the Cartesian architecture has been the standard technology for RF transmitters. Indeed, even CMOS implementations have adopted the Cartesian transmitter in null-PAPR systems. In such cases, the PA operates in class C or in a saturated AB/B mode. In [41], a fully-integrated solution for GSM (DCS-1800) is presented in a 0.35 μm CMOS process, using a differential cascode configuration operating in class C. The PA uses two pairs of very large transistors (9 and 18 mm widths each), to

provide 25 dBm of output power. Another version of the same implementation reaches over 30 dBm of peak output power using off-chip inductors. Other examples can be found in Bluetooth systems with GFSK, for which a linear envelope amplification is not required, but saturated PAs are employed in an IQ transmitter for maximizing the efficiency [42–45].

2.1.1 Doherty Technique

With the increased interest in AM formats, the Doherty technique has been lately revisited. It is perhaps one of the most promising techniques to improve the efficiency in actual IQ transmitters without degrading the linearity. The Doherty technique improves the efficiency of a linear amplifier by adding an auxiliary amplifier to the transmitter. The concept dates back to 1936 [23]. The operation relies on a very interesting principle, which is "load modulation" (or "active load-pull" [46]). Fig. 2.1 shows the classical Doherty topology with two PAs. One is commonly termed as "main amplifier" (or "carrier amplifier") and the other "auxiliar amplifier" (also known as "peak amplifier"). The auxiliar amplifier is normally a class-C amplifier biased at a given voltage below threshold so that only turns on for a specific input level, i.e. the transition point. Depending on the transition point,

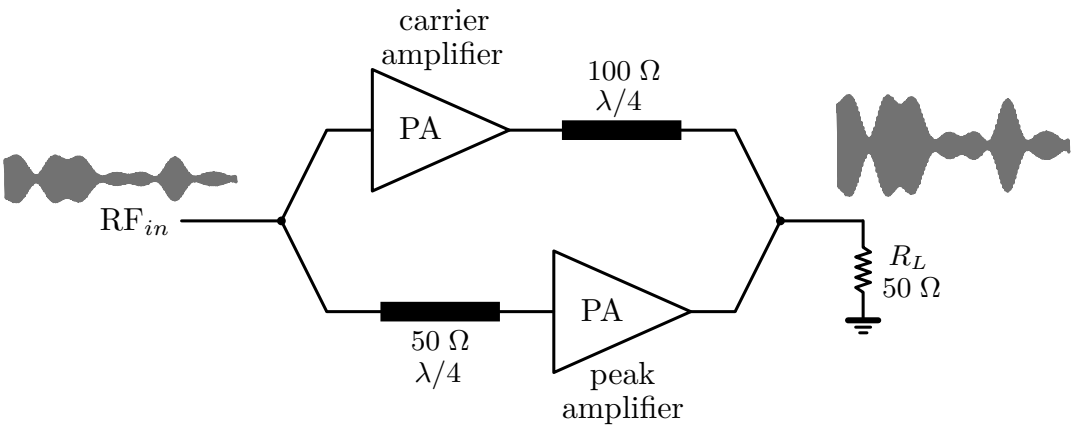


Figure 2.1: Doherty amplifier.

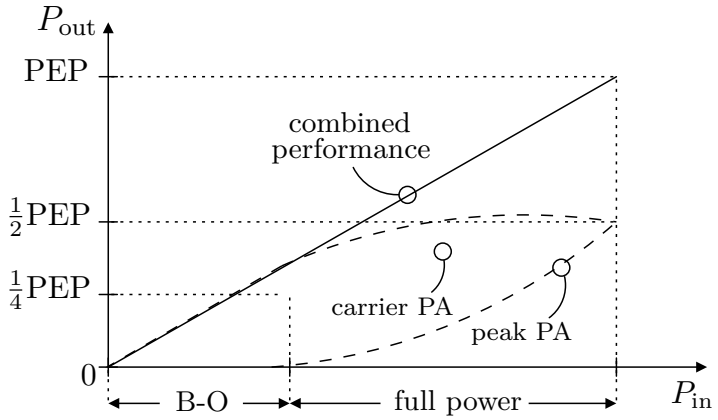


Figure 2.2: Operation regions in the Doherty PA.

two operation regimes are defined: full power and B-O. Fig. 2.2 gives a simplified representation of this type of operation. For a classical Doherty, the main amplifier begins to saturate at 1/4 of the PEP, which means 6 dB of B-O. The value of the transition point also dictates the load network characteristics.

The classical Doherty is capable of obtaining significant improvements in the overall efficiency for signals with PAPRs up to ~ 6 dB. Below the transition point, for higher PAPRs, the efficiency drops abruptly. Nonetheless, the efficiency boost along other PAPR ranges is possible by design, arbitrating the turn-on voltage of the auxiliary PA close to the required B-O.

At 10 dB B-O, Iwamoto *et al.* demonstrated an improvement of 2.6 times over the class B, maintaining the PAE above 39 % within the B-O range [24]. The efficiency enhancement is in fact significant over a simple class-B version. If more than two amplifier stages are used, in spite of the additional complexity there are still meaningful improvements. In the case of a three stage Doherty, with transition points at 1/4 and 1/2 of the PEP, it has been demonstrated an efficiency improvement in the order of 7 times the class B, at a B-O of 12 dB [25].

2.2 Envelope Tracking

In a linear PA (classes A/AB/B), if the power delivered to the PA is somehow controlled according to the signal to be transmitted, the efficiency can be properly optimized. Fig. 2.3(a) shows an example[1] in which it is clear how the fixed power-supply can have a great impact on power consumption. As shown in figure, the power dissipated is highly dependent on the input signal magnitude and sometimes can be even higher than the output power. Evidently, the power consumption is elevated because the power supply is fixed regardless the output power required. Therefore, when very low-power signals are to be transmitted, the PA has to dissipate all the power that the load does not demand.

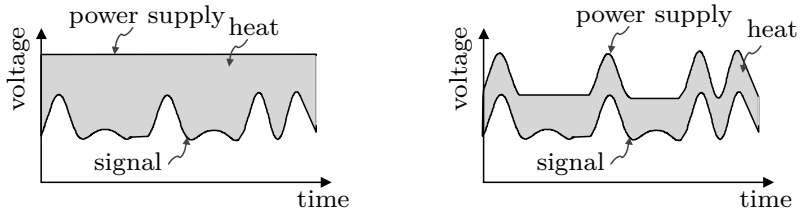


Figure 2.3: Illustrative example on ET. (a) High power dissipated due to fixed power supply; (b) Lowering power consumption is achieved by ET.

If the power supply follows a long-term envelope, as it is illustrated in Fig. 2.3(b), then the power consumption can be fairly reduced at the PA. This can be seen as moving the PA gain compression always closer to the output power level. Such technique is commonly known as envelope tracking (ET), or envelope following. It requires a dynamic power-supply (i.e., an envelope amplifier) with its output defined by a slow variation of the envelope, e.g. the average power [13, 52] or other shaping function for the drain voltage [51]. This results in a time-varying load for the envelope amplifier, which must be carefully designed to account for any resultant

[1]The example given here is merely illustrative. It is not intended to represent any realistic time relationships.

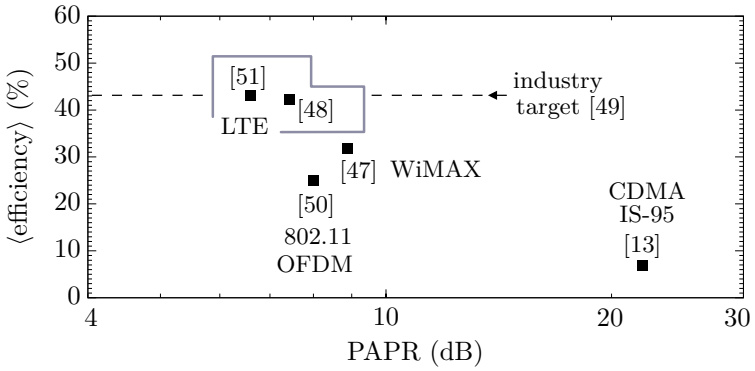


Figure 2.4: ET implementations.

nonlinearity. Fig. 2.4 shows average efficiencies for transmitter implementations in different applications using ET[2]. State-of-the-art performances are in the 30 to 45 % range, decreasing with the PAPR. Here, the PAPR denotes the loading conditions, meaning that a high PAPR implies wide load variations for the envelope amplifier.

To avoid efficiency degradation, almost every ET implementation makes use of a switching-mode configuration as its dynamic power-supply. Compared to a stand-alone PA, the efficiency enhancement due to the ET is in the typical range of 5 to 8 % [48, 51]. The way the envelope is tracked makes some influence on the results. Instead of an average (slow) tracking, some works employed an ET system with a wide-bandwidth configuration in the envelope amplifier, e.g. [51] and [53]. This implies a fast tracking that almost results in following the envelope instantaneously. In literature, such schemes are usually referred to as wideband ET (WBET) or envelope following [13]. However, the usage of such approach in ET is not always possible. When the signal has a considerable PAPR, it gets difficult to switch between high power values. Hence, to mitigate the efficiency degradation, the power supply has to be adjusted in steps [54]. This results in a very-slow tracking of the envelope, being only suitable for implementations in which the PAPR is in the order of 10 dB or more [53].

[2]These results account for the power losses in envelope amplifier and PA as well.

However, ET can be used in conjunction with other approaches. For instance, ET has been implemented with the regulation of the gate voltage (of the PA) according to supply voltage, to optimize the overall efficiency instead of the PA efficiency itself [55]. It turns out that both the envelope shaping function and linearity get improved. Furthermore, in a quite distinct approach, [47], the inclusion of ET in a Doherty amplifier allowed to improve not the efficiency, but the linearity measured by the EVM. In fact, the linearity enhancement by means of an ET approach has been demonstrated using a proper shaping function for the envelope modulator. Based on sweet spots [56, 57], the work in [48] uses ET to lower the power-supply level, targeting an optimum IMD_3 for each power level. As a result, for W-CDMA/LTE at PEP, both efficiency and EVM are slightly better than a stand-alone PA solution.

2.3 Polar Transmitter

Polar transmitters are the present renaissance of an amplification method from the 1950s[3], namely the envelope elimination and restoration (EER) or Kahn technique [59]. With the ever-increasing data-rate in communication standards, the polar transmitters are also receiving increased attention. The possibility to use saturated RF PAs together with non-constant envelope signals makes them suitable for such applications. Using nonlinear PAs, the power efficiency is significantly higher than conventional linear classes used in IQ transmitters.

In polar and EER transmitters, instead of tracking the envelope, the drain is modulated precisely with the amplitude signal. As so, the PA can be used in switching-mode improving its efficiency. In an EER transmitter, the signals are not promptly generated, but require intermediate stages to obtain them. Fig. 2.5 depicts a simple representation for both types of

[3]It is not generally known but polar modulation techniques had already been proposed in 1915 [58].

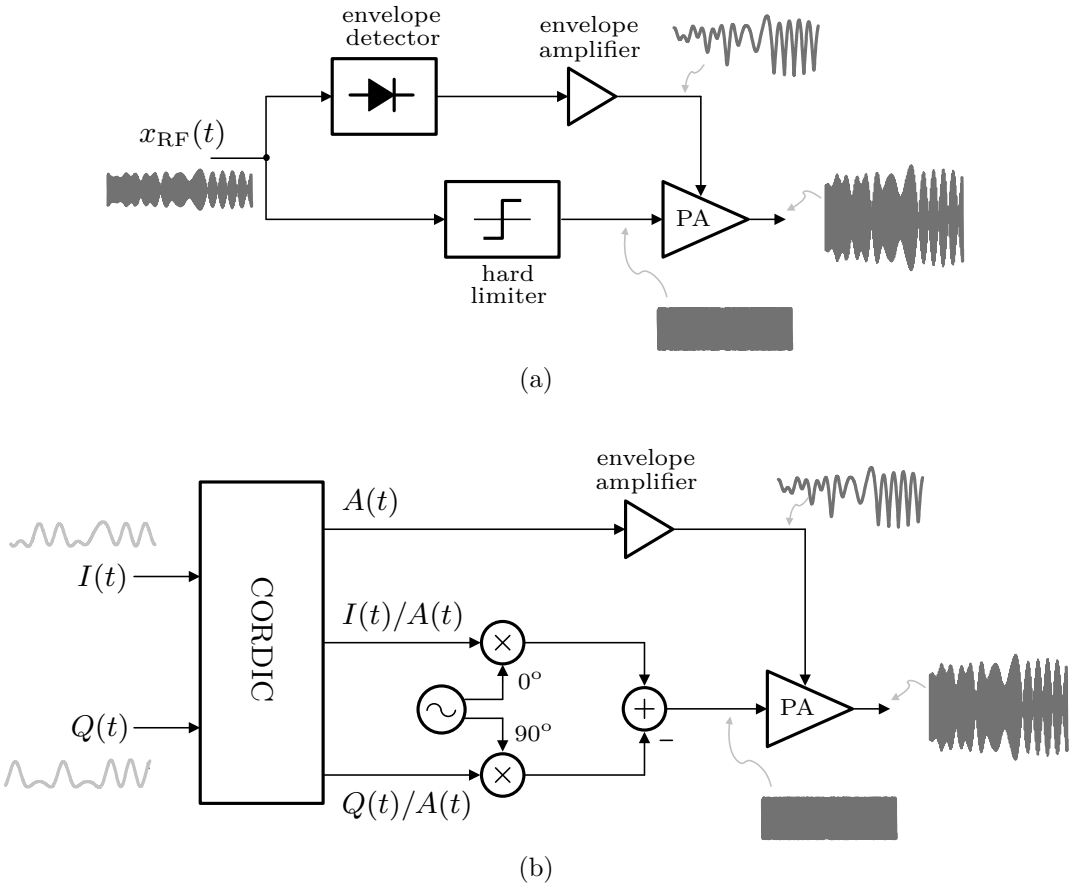


Figure 2.5: (a) EER and (b) polar transmitters.

polar transmitters. In the EER architecture the IQ data is decomposed in amplitude and phase signals by employing a envelope detector and a limiter, respectively. A delay line can also be included in the phase path to synchronize envelope and phase. The signal is then restored and amplified in the PA.

The polar transmitter is a modern version of the EER architecture, in which the IQ data is pulse shaped firstly by digital baseband filters and then transformed into polar form by means of rectangular-to-polar CORDIC algorithms [60]. Fig. 2.5(b) shows the basic diagram of a polar transmitter. Since the PA efficiency is unaffected by the power-supply level, the PAPR impact is mitigated. Currently, the envelope amplifiers are the hot-topic

research for polar transmitters. Note that the overall efficiency is given by

$$\eta_{\text{ovr}} = \eta_{\text{env}} \times \eta_{\text{PA}} \tag{2.3}$$

where η_{env} is the efficiency of the envelope amplifier and η_{PA} is the drain efficiency of the PA. Since the PA itself has the same structure used in constant-amplitude amplification, the drain efficiency should remain nearly unchanged. Consequently, the most important characteristic that dictates the overall efficiency in state-of-the-art implementations is the performance of the envelope amplifier.

2.3.1 Envelope amplifier

Several approaches have been reported on the design of envelope amplifiers [35, 37, 53, 61–68]. Fig. 2.6(a) depicts a basic circuit used in the envelope amplification, namely the low-dropout (LDO). LDOs are linear regulators with low power-efficiency. Characteristically, an LDO provides wide bandwidth, low-output impedance and high-current driving capability [61]. A CMOS-LDO fully-integrated on a chip (with the PA) has been proposed by Reynaert *et al.* [37] as an envelope modulator for a polar transmitter. The target of this application is the EDGE (class E3) standard. At the peak power of 27 dBm, using a constant envelope, the efficiency is 30 % for the transmitter system comprised of a class-E PA, its driver and envelope modulator. Nonetheless, this is fairly low compared to some state-of-the-art approaches avoiding the usage of LDOs, e.g. 45.3 % peak PAE at 27.8 dBm in [62] based on a switching-mode topology.

Alternatively, dc-dc converters based on switching-mode power supply (SMPS) regulators are much more efficient over a wide range of amplitudes. Fig. 2.6(b) shows a very common SMPS, usually known as synchronous buck-converter. The downside of such converter is its limited operation speed. When the SMPS is not sufficiently fast, the elimination of switching noise by the reconstruction filter requires very large values for L and C,

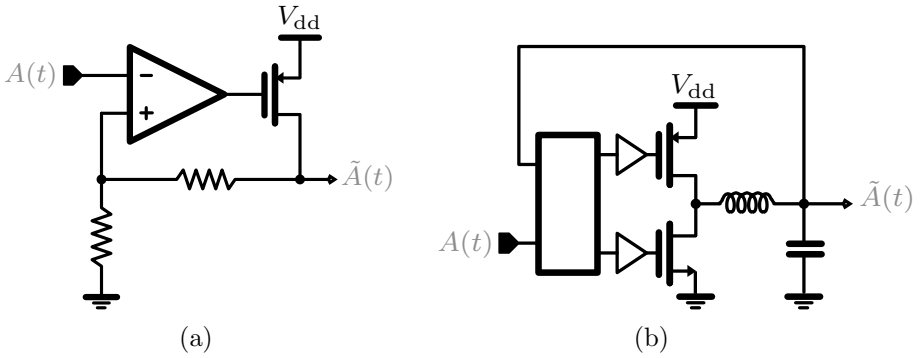


Figure 2.6: Envelope modulators for the polar Tx – (a) LDO [37], (b) synchronous-buck converter.

typically in the order of μH and μF. This greatly increases the delay in amplitude path, which can lead to time misalignment between RF paths leading to spectral re-growth.

When pulse-width modulation (PWM) is used in SMPS, high-sampling rates are required. This leads to increased switching losses and difficulties in driving circuitry. Moreover, EM interference (EMI) can be a problem when PWM is used in buck converters with inductor and free-wheeling diode [35]. Instead, PWM can find its use with envelope signals having reduced bandwidths, such as those in ET transmitters [53]. However, pure ET systems require linear PAs, which then leads to an efficiency tradeoff between PWM-SMPS and linear PAs.

There are alternative approaches in which both fundamental types of converters are used as some kind of mixed topology. Linear-assisted SMPSs employing delta modulation have been reported in [63] and [64]. Delta modulation reduces the number of switching transitions within a given sampling rate when compared to PWM. In [63], a delta-modulated synchronous buck-converter controls the power supply of an LDO, compensated through feedback. A similar scheme is presented in [64], demonstrating its ability to reduce quantization noise due to delta modulation.

More complex circuits, suitable for wide-band signals, have been implemented using hybrid-switching amplifiers [53, 61, 62, 65]. The concept is

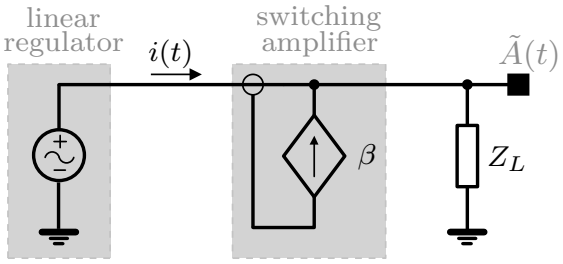


Figure 2.7: Hybrid-switching concept [53, 61, 65].

illustrated in Fig. 2.7. Basically, it uses a SMPS regulated by a linear amplifier. The technique has been used in audio to improve fidelity in class-D amplifiers. In hybrid-SMPSs, feedback of a hysteresis current seems to be the most promising control technique [53, 62, 67].

Table 2.1 summarizes the results of some more reported works. The envelope amplifier recently published by Choi *et al.* in [62] can be used for EDGE, W-CDMA and WiMAX. Remarkably, in any of these standards the peak efficiency of the envelope modulator is above 75 %, and the transmitter average efficiency is always higher than 34 %. Although the amplitude modulator is built in CMOS 130 nm, the PA is implemented in a different semiconductor technology (InGaP/GaAs HBT). In [67], a hybrid envelope modulator in a 65 nm CMOS process is proposed for a WLAN transmitter. Due to such reduced lengths of the transistors, the envelope modulator is capable of maintaining high-speed switching operation and, as a result, it improves its efficiency about 20 % at 10 dB when compared to a stand-alone AB amplifier. Nonetheless, for the efficiency measurements, the RF-PA has been characterized by a 5.3 Ω load, hence it admits a perfectly isolated RF-PA with fixed load (which differs considerably from a practical case). For a class-E1 EDGE, about 4 W has been achieved for using a standard CMOS process [65]. For the current-sensing feedback, sample-and-hold circuits are used at 40 MHz. To achieve such high output power, the hybrid envelope modulator has been divided into a master-slave configuration.

Envelope modulation using digital techniques are valid alternatives to

Table 2.1: Performance summary of some envelope amplifiers reported in literature for different wireless technologies

ref	peak efficiency	peak (dBm)	target application nomenclature	Δf	f_c	year
[7]	74 %	30	CDMA IS-95	1.22 MHz	950 MHz	1999
[61]	88 %	34	EDGE	384 kHz	1.88 GHz	2007
[63]	76 %	31	–	4 MHz	900 MHz	2007
[66]	89 %	33	W-CDMA	3.84 MHz	1.88 GHz	2010
[67]	88 %	23	802.11g WLAN	20 MHz	2.45 GHz	2009
[62]	75 %	29	WiMAX	5 MHz	–	2009

typical dc-dc converters. These schemes have gained particular interest in recent publications. One remarkable approach has been introduced by Shameli *et al.* in [68]. It relies on a new scheme based on two-point modulation, with the envelope data injected at two different PA inputs. The amplitude signal is applied by means of a digital 7 bit word that controls the current of a differential switched amplifier. The power supply is modulated with a 95 % efficiency dc-dc converter, which uses a second-order $\Delta\Sigma$ modulator. Another interesting approach is the interleaving version of delta-modulation introduced in [35]. An array of modulators acts in parallel with phase-shifted clocks, but all at the same frequency. Therefore, narrow streams of driving pulses are treated as parallel contributions of wider pulses, which alleviates the hardware speed requirements.

2.3.2 Main drawbacks of polar transmitters

While in Cartesian modulators the I and Q are band-limited signals, in the polar form the magnitude and phase signals are (theoretically) unlimited in spectrum. The polar representation can be written as follows

$$x_{\mathrm{RF}}(t) = \mathrm{Re}\left\{\mathrm{A}(t)\cdot \mathrm{e}^{j[\omega_c t+\phi(t)]}\right\} \tag{2.4}$$

$$= \sqrt{I^2(t)+Q^2(t)}\cdot\cos\left[\omega_c t+\phi(t)\right] \tag{2.5}$$

where $A(t)$ is the time-varying amplitude of the RF signal, and $\phi(t)$ the

phase given by (1.3), where

$$I(t) = A(t)\cos[\phi(t)] \tag{2.6}$$

$$Q(t) = A(t)\sin[\phi(t)] \tag{2.7}$$

In a polar transmitter the spectra of amplitude and phase signals are wider when taken separately than the original complex form [35, 69, 70]. The non-limited bandwidth poses serious challenges in the design of phase and amplitude signal paths, and is considered one of the major bottlenecks of present designs. Since both signal paths can be regarded as separate systems, time misalignment contributes to spectral re-growth [36]. As a rule of thumb, the maximum differential delay is in the order of ± 20 ns per MHz of RF bandwidth. For instance, in 200 kHz EDGE signals a ± 100 ns delay is tolerable [35, 37].

For signals with zero-crossing trajectories in IQ constellations, such as pulse-shaped W-CDMA signals, a great design effort is required to fulfill the spectrum emission mask. In particular, HSDPA and HSUPA include constellation data points at the IQ origin [40]. Due to the limited bandwidth of practical circuits, the IQ diagram can present a hole since envelope trajectories cannot reach null voltages, thus degrading the EVM [40, 71]. This is a growing problem for emerging technologies, such as UTRA-LTE [72] and UWB [38]. For instance, in order to satisfy the EVM required for multi-band OFDM of an UWB system, [38] reports that, while amplitude suffices at least 1.1 times, phase bandwidth of a polar transmitter needs to be 7.1 times higher than the bandwidth in an IQ transmitter. About 5 times the RF bandwidth is indicated in [35], assuming perfect synchronization of phase and amplitude signals.

Other contributions to non-ideal performance of polar transmitters include AM-to-AM and AM-to-PM nonlinear behaviors. The analysis of the distortion mechanisms in polar amplifiers has been presented by J. C. Pedro *et al.* in [73]. It has been shown that: AM-to-AM distortion is mainly

caused by the nonlinear characteristic of the envelope modulator; AM-to-PM distortion is a result of residual output carrier modulation due to low power-supply values; and this low-voltage region is quite susceptible to carrier feedthrough. For null amplitude values, corresponding to the IQ origin, the amplifier must present null output. However, some configurations may be less immune to null-supply values and produce undesired output power, lowering efficiency. This kind of leakage is hardly removed since it contains in-band frequency components.

The feedforward is established through C_{gd}, resulting in adverse effects. In very large transistors, when the AM signal is relatively low, the feedforward currents flowing through C_{gd} are converted into a voltage level comparable to the envelope signal. Since the phase signal is broadband in frequency, the spectral emission mask is affected [37]. At low-supply modes, AM-to-PM dominates over AM-to-AM distortion, while for high power-supply levels the AM-to-AM distortion can be predominant [73].

The AM-to-AM and AM-to-PM distortion effects require always proper compensation to meet spectrum emission masks. In linear amplifiers, AM-to-PM distortion can be compensated through gate capacitance modulation [74]. But in switching-mode PAs, AM-to-PM distortion requires much more complex compensation mechanisms. On one hand, feedback effectively improves the linearity. The main challenge, for instance in case of polar-loop (with the RF feedback of phase/magnitude signals), is the design of a precision receiver capable to operate with wide-bandwidth signals. [75]. Even though, Sowlati *et al.* [76] implemented a complete polar modulator with excellent results for EVM in GSM/GPRS/EDGE using a $0.35\,\mu$m BiCMOS process. Another common technique used for linearization is predistortion, but it requires accurate modeling of the PA nonlinear behavior. Recent works have described predistortion studies for EDGE [77,78] including memory effects [70], W-CDMA [79] and multi-mode standards [80]. The main advantage of digital predistortion (DPD) is its implementation in digital baseband processing, which avoids an increased complexity at the RF

circuitry. Due to so many implementation difficulties in hardware, one can say that every transmitter requires DPD to comply with linearity standards of current standards. This is not limited to the polar transmitter, but it is in fact applicable to any other RF architecture.

2.4 LINC

The concept of "outphasing" has been originally conceived in 1935. This technique has been introduced by H. Chireix [28] as a high-efficient modulation system, when power expenses started to be a major concern in operating costs of base stations. Chireix proposed this technique to avoid two typical problems at that time. One problem was the relatively low efficiency of power tubes, when used under linear amplification. The other problem was the alternative itself. That is, anode modulation was challenging because of the low efficiency of time-varying power-supplies. Curiously, inasmuch as radio evolved, some problems remain nearly the same almost eight decades later.

In the outphasing technique, two phase-deviated signals with constant amplitudes are combined to generate AM signals. Fig. 2.8(a) shows the basic representation of a LINC transmitter. Let us admit the generic data signal $s_i(t)$, modulated both in amplitude $A(t)$ and phase $\theta(t)$ as

$$s_i(t) = A(t) \cdot \cos\left[\omega_c t + \theta(t)\right], \qquad 0 \leq A(t) \leq A_{\max} \tag{2.8}$$

In a LINC transmitter, this input signal is then split by a signal component separator (SCS) into two constant-envelope signals,

$$s_1(t) = s_i(t) + e(t) \tag{2.9}$$

$$= A_{\max} \cdot \cos\left[\omega_c t + \theta(t) + \phi(t)\right] \tag{2.10}$$

and

$$s_2(t) = s_i(t) - e(t) \tag{2.11}$$

$$= A_{\max} \cdot \cos\left[\omega_c t + \theta(t) - \phi(t)\right] \tag{2.12}$$

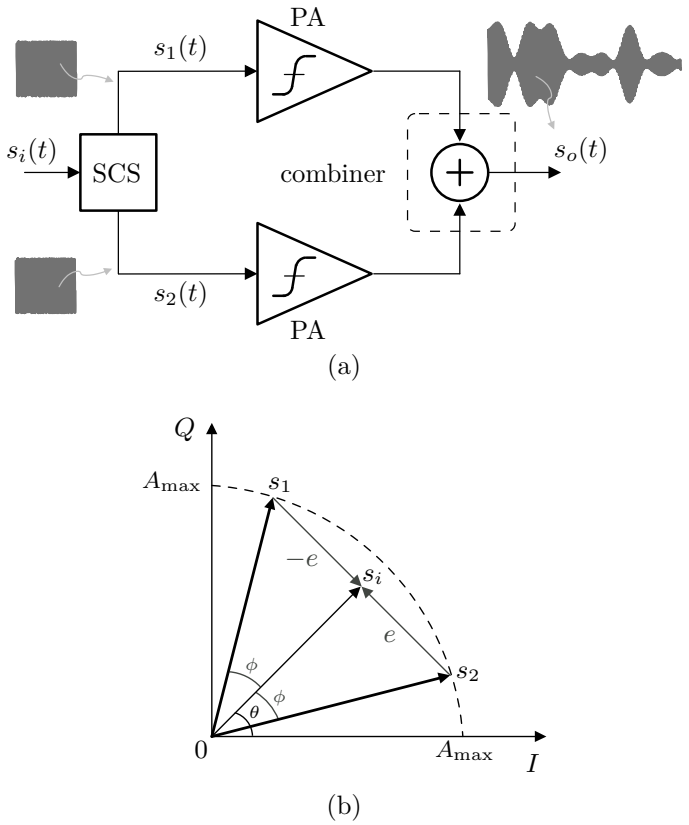


Figure 2.8: (a) LINC transmitter and (b) phasor representation of its signals.

where $s_1(t) + s_2(t) = 2 \cdot s_i(t)$. The phase $\phi(t)$ can be written as

$$\phi(t) = \cos^{-1}\left[\frac{A(t)}{A_{\max}}\right], \qquad 0 \leq \phi(t) \leq \pi \tag{2.13}$$

and $\theta(t)$ refers to the four-quadrant inverse tangent

$$\theta(t) = \tan^{-1}\left(\frac{Q(t)}{I(t)}\right), \qquad |\theta(t)| \leq \pi \tag{2.14}$$

Fig. 2.8(b) shows $e(t)$, which is the quadrature signal used in equations (2.9) and (2.11) to express the outphased signals. This signal can be written as follows

$$e(t) = j \cdot s_i(t) \cdot \sqrt{\frac{A_{\max}^2}{|s_i(t)|^2} - 1} \tag{2.15}$$

Since the introduction of the LINC concept, the practical reason preventing its wide-spread use was the implementation of the SCS. Only with

an accurate SCS would be possible to generate the correct phase for the signals. In the seventies, D. Cox brought to life the outphasing technique under the name of LINC [27]. Any signal applied to the SCS could generate the two constant-envelope signals needed to drive the two output amplifiers with the appropriate phases. This further extended the concept of outphasing to generalized schemes with quadrature modulation.

2.4.1 Generation of outphasing signals

The LINC transmitter is generally seen as a promising candidate for highly-linear highly-efficient transmitters. However, in practice, the LINC transmitter still finds stringent constraints in its application. The SCS remains one of such problems. Note that, the system required to obtain $s_1(t)$ and $s_2(t)$ signals represents a process that must be capable of performing very precise AM-to-AM and AM-to-PM distortions.

Two basic approaches exist for implementation of the SCS, namely: *i)* the phase-modulation method, and *ii)* in-phase/quadrature method. Alternatives to these two exist in literature, but are less abundant and require complex circuits [81, 82] – although with the advantage of not requiring phase modulators.

Earlier versions of the phase-modulation method were entirely analog [27, 83]. These basically consisted of arc-cosine (or arc-sine) phase-modulators operating at an intermediate frequency or RF. The digital version of an SCS is preferred instead. In fact, the great advances on digital computation are responsible for reviving the actual interest on an ancient technique used for AM broadcasting. Digital processing presently available allows cost-effective implementations in communication systems with flexible compensation performed in real time [84]. As so, digital implementations of the phase-modulation method are already feasible for W-CDMA signals, both in field-programmable gate arrays (FPGAs) [85,86] and digital signal processors (DSPs) [86].

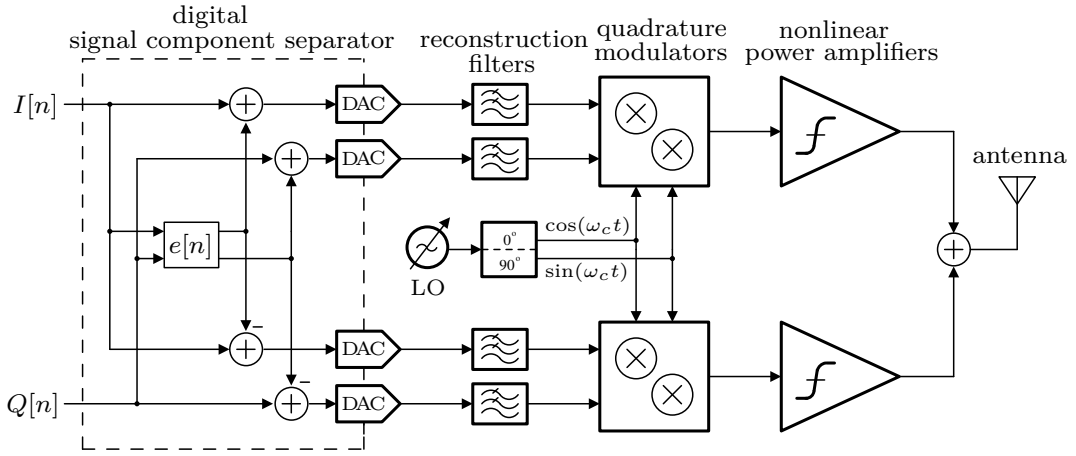


Figure 2.9: LINC with digital SCS implemented by in-phase/quadrature method.

The in-phase/quadrature approach for the SCS is based on generating the quadrature signal $e(t)$ – Fig. 2.8(b). Throughout the quadrature signal and the input signal itself, the required out-phased signals can be produced – Fig. 2.9. Several nonlinear operations are required to compute $e(t)$. Some systems rely on baseband digital processing implemented in a DSP, assisted by look-up tables (LUTs) to minimize division and square-root operations [87, 88]. The LUT is used to store values of a limited number of quadrature signals. The main drawbacks associated with a true-digital implementation are related to high-oversampling rates, which impose the level of power consumption and required bandwidth. The SCS digital signals, generated at baseband, are followed by digital-to-analog converters (DACs), reconstruction filters and then by quadrature up-converters. Mismatches on these components also limit the overall performance of a digital-based solution.

Several analog implementations of the in-phase/quadrature method exist in literature [89–91]. The major limitation in these analog approaches is the accuracy needed to deal with less-relaxed linearity requirements. For instance, a potential problem for the envelope signal crossing the origin (of the IQ constellation) is due to the difficulties in generating the quadrature signal $e(t)$ [92]. The signal $e(t)$ is typically obtained through implemen-

tation of a variable-gain amplifier (VGA), and when $|s_i(t)| \rightarrow 0$ in (2.15), the gain of the VGA should be infinite, which is not feasible in practice. This also explains why some implementations were validated through $\pi/4$-shifted DQPSK, which are modulation schemes designed to avoid IQ zero crossings [90], or simply by preventing the signal to have the null value as minimum magnitude [89, 93].

2.4.2 Effect of path impairments

Ideally, in the LINC transmitter, the outphased signals cancel out any nonlinearity at the output. That is, the quadrature signal $e(t)$ in each branch is supposedly eliminated at power combining. Consider the gain imbalance Δg and phase imbalance $\Delta\phi$ at one of the branches. After combining both signals, the output is given by

$$\begin{aligned} s_o(t) = s_1(t) + s_2(t) &= s_i(t) \cdot (2 + \Delta g) \cdot \mathrm{e}^{j\Delta\phi} \\ &+ e(t) \cdot \left[(1 + \Delta g)\mathrm{e}^{j\Delta\phi} - 1\right] \end{aligned} \tag{2.16}$$

It can be concluded from (2.16) that inherent imbalances between the two RF branches lead to distortion in a LINC transmitter [94, 95]. This distortion widens the radiated power along the frequency spectrum, increasing the adjacent channel interference (ACI) [96]. Particularly in the case of systems with high-spectral efficiencies, such as 64-QAM or other high-order modulations, it has been shown that the LINC is very sensitive to path imbalances [97].

Different nonlinear behaviors of the pair of amplifiers can affect distortion at the output. If similar highly-nonlinear PAs are used, the overall performance is not significantly affected. But, if less similar PAs are available, then linear PA regimes are preferable over SMPSs [95], hence directly affecting the overall efficiency. The digital SCS can also be responsible for ACI degradation due to quantization. Nonetheless, small words are required for

the SCS to meet with reasonable low-levels of ACI [98]. Other sources of ACI degradation created by the digital SCS architecture include the reconstruction filters. These filters are used to eliminate the sampling images. However, its effect is seen in the ripple produced in the driving signals of the PA, when such signals are supposed to be constant [99]. The ACI can also be degraded due to non-ideal quadrature modulators [100, 101]. These effects are difficult to compensate, demanding quite complex systems [102].

Gain and phase matching for typical applications are in the order of 0.1 to 0.5 dB and 0.4 to 2.0 degrees, respectively, which is hardly attainable in practice without any calibration scheme [101]. Correction techniques can be implemented to reduce gain and phase mismatches between both branches, as well as to compensate for changes due to thermal drifting variations, bias, and component aging when adaptive correction is considered. Some works demonstrated that relatively accurate cancellation can still be achieved, within some degree of path imbalances, by using baseband processing in several ways. However, these can suffer from practical implementation limitations.

A solution based solely on phase corrections has been proposed in [103]. Other methods rely on the correction of both imbalances, i.e. gain and phase. Sundström describes, in [96], a direct-search algorithm based on the simplex method, measuring out-of-band produced signals. This scheme requires considerable time for effective correction due to the high amount of data that has to deal with. In [104], the authors also avoided computation of derivatives by employing direct search for compensating imbalances in phase and gain due to the effects of AM-to-PM distortion. In the proposed architecture, the comparison between the low-pass filtered output and the input signal represents a critical issue in terms of correction performance. Algorithms based on the computation of the minimum mean-squared error have been investigated in [105–107]. Genetic algorithms have also been studied by García-Dúcar *et al.* in [108], but the heavy computation required represents a limiting factor difficult to circumvent. Most methods

rely on digital processing, because avoiding algorithms to perform calibration would rather require analog circuitry that may be difficult to implement [109]. Although such correction techniques seem promising, some of the works lack real implementation results.

Simpler calibration schemes are also possible, e.g. obtaining measurements of the signals at different points [110]. A method sharing a similar basis is presented by Zhang *et al.* in [111], with analysis and algorithm details. However, the usefulness of any of these two schemes is restricted to off-line operation, since some reference signals must be generated prior to the compensation procedure. On-line calibration has been proposed in [101] with practical implementation results demonstrated for CDMA IS-95.

2.4.3 Efficiency of the LINC transmitter

The combiner can also have great impact in the linearity of a LINC system. There are two types of power combination that can be applied. The most common is a lossless combiner, with non-isolated and unmatched ports, such as the Chireix combiner. The other is lossy, with matched and isolated ports. In the case of the latter, phase and gain imbalances are the only causes for linearity degradation [112]. Its efficiency is given by

$$\eta = \cos^2[\phi(t)] \tag{2.17}$$

which is unitary only at PEP. When using a lossless tee as output combiner in the form of a Wilkinson combiner without isolation resistor (the same as the Chireix combiner without reactive terminations), the coupling between the two amplifiers also leads to distortion [113]. With a Chireix combiner, analytical expressions have been derived in [114], for efficiency and voltage waveforms. It has been shown that depending on the reactance, efficiency varies but the performance can be optimized for a given PEP. Explicit forms are given in [115] and [116] for optimization in terms of the signal PDF. Nonetheless, these results did not take into account the distortion

due to the power combining. In [117], it is also introduced the effect of reflection coefficient due to impedance mismatches seen by each amplifier in the voltage waveforms. It is shown that even without any imbalance between the RF paths connecting to the Chireix combiner, the linearity is affected due to the mismatched combiner.

The linearity-efficiency compromise is mostly focused at the combiner of the LINC. The efficiency on a LINC is improved with a Chireix combiner due to the gain and phase imbalances introduced by the reactive termination of the combiner. This comes at the expense of linearity. On the other hand, for predistortion in phase for a LINC with a lossless combiner, it is shown in [118, 119] that the efficiency drops as linearity is increased. The maximum linearity leads to an efficiency value close to that of a LINC with a matched combiner.

2.5 Digital RF Transmitters

Deep-submicron CMOS has been the dominating technology for almost every application in which an electronic circuit requires some sort of digital processing. Due to large scale of integration, costs of masks, time-to-market and high-yield in mass production, it is natural that if the analog/RF functionalities can migrate to the digital domain, downscaling brings several benefits to the performance of wireless transmitters.

Owing to CMOS downscaling, better resolution is currently achieved in time-domain transitions than in the voltage level [120]. This perception encourages the study of novel RF architectures based on fully-digital approaches. For instance, in [121] the complete RF signal generation is performed through the so called “digital-to-RF converters”. It basically consists of switched-mode Gilbert cells grouped in parallel to accomplish the RF modulation of AM signals. Consequently, the analog baseband is omitted, which improves the transmitter flexibility to deal with multiple

standards (EDGE, W-CDMA and wireless LAN). Some works reported by Staszewski *et al.* also addressed new digital-RF techniques to handle specific analog-RF functions [120, 122]. The single-chip radio for Bluetooth reported in [122] has been implemented in a standard 130 nm CMOS process, using only digital circuits. It comprises a digitally-controlled oscillator (DCO) within an all-digital phase-locked loop (ADPLL). These circuits are responsible for the synthesis of Bluetooth signals, being followed by a PA operating close to class-E amplification. For standards having signals with non-constant envelope, this transmitter system has been employed in a polar version [120]. The proposed transmitter has been fabricated in a 90 nm digital CMOS process, targeting dual-mode communication, i.e. GSM and EDGE. Fig. 2.10(a) depicts the circuit used in the transmitter front-end. The AM signals are obtained based on the digital word $d_n \ldots d_1$ (the LDO just provides a stable voltage). An alternative approach to modulate the envelope has been introduced in [123]. The circuit is depicted in Fig. 2.10(b). Similarly to a DAC system, it binary weights the power supply applying the thermometer-coded envelope as an 8 bit word. Although these approaches reduce the number of analog blocks, they are only able to perform RF synthesis. An external amplifier is always required at the output, i.e. an actual PA, operating in linear mode for AM signals. Hence, in spite of the supposed advantages, there is no real advantage in terms of efficiency.

Extending the digital processing beyond the transmitter baseband has been explored in several scientific works. This is the main goal of RF-PWM[4] addressed in [125] and [126]. The concept is quite attractive, since it can employ digital circuitry and nonlinear PAs to generate AM signals at constant V_{dd}. The PWM signal is directly applied to the gate of a class-E PA and the time-varying envelope is acquired at the antenna, due to a reconstruction filter (BPF) at the PA output. This approach achieves

[4]Surprisingly, the concept was patented still in the late sixties [124].

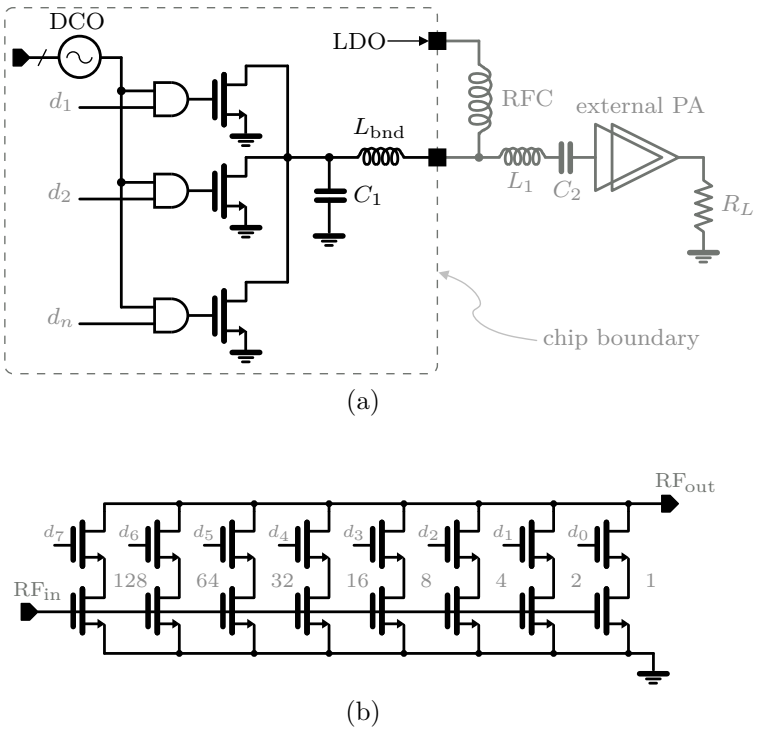


Figure 2.10: Digital controlled PA structures with amplitude modulation – (a) digital PA as proposed in [120]; and (b) binary-weighted envelope DAC from [123].

a reasonable efficiency (PAE $\simeq 28.5\,\%$ in [125]) but at the cost of an extensive bandwidth of the driving signals of the PA. RF-PWM requires a slicing frequency about ten times higher than the input (carrier) bandwidth for proper conversion. An alternative is the use bandpass $\Delta\Sigma$ signals, which allows a slightly lower sampling frequency. Nonetheless, it requires four times of oversampling [127, 128], which is still excessive for wireless communications in the GHz range.

Chapter 3

The Cartesian-Polar Architecture

This chapter is devoted to the description of the proposed architecture, that is, the C-P transmitter. First, the proposed system structure is addressed on a functional basis. The following sections introduce several performance analyses and comparison with other transmitter technologies. The analyses covered along this chapter include the transmitter performance in terms of bandwidth, energy efficiency, and efficiency improvement using power recycling. Finally, since in principle the C-P architecture relies on symmetry, the impact of possible impairments in system performance is also addressed.

3.1 System Description

The proposed transmitter is devised from the Cartesian architecture, including adequate topology modifications based on the polar transmitter as depicted in Fig. 3.1. In the conventional Cartesian transmitter, the RF signal acquires its time-varying amplitude in the frequency up conversion in the IQ modulator – Fig. 3.1(a). As previously referred, this implies that the following stage comprises a PA performing linear amplification, which is typically inefficient under high-PAPR regimes. To accommodate for large variations in signal envelope without degrading the average efficiency, the polar transmitter is a preferable approach – Fig. 3.1(b). The PA can

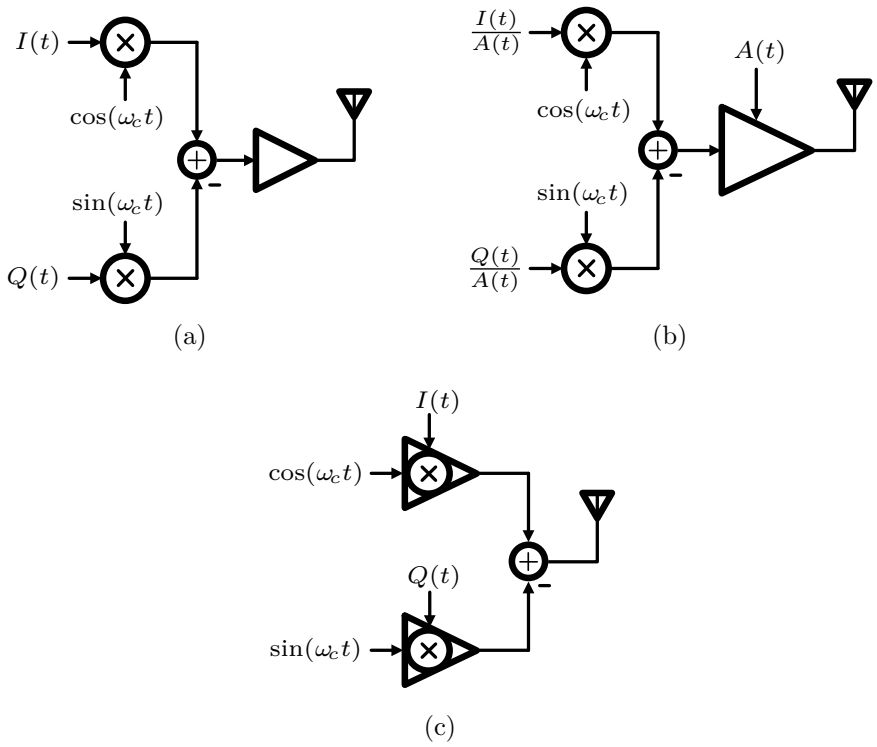


Figure 3.1: Build up of the C-P transmitter starting with (a) the typical Cartesian architecture and (b) polar transmitter, and then introducing architectural modifications, e.g. replacing mixers by SMPAs, ending up with (c) the C-P transmitter.

operate efficiently in switching mode, driven by a constant amplitude signal, while the dc power-supply varies accordingly with signal envelope so that, ideally, the PA produces solely the demanded power. Furthermore, the polar amplifier can also be regarded as a high-level amplitude modulator or multiplier, which is the case of the C-P transmitter conceptually depicted in Fig. 3.1(c). This modification is possible because the input of each amplifier is driven by constant amplitude signals, i.e. the in-phase and quadrature versions of the RF carrier. Here it was adopted power-supply modulation directly from IQ signals instead of their absolute values, since the latter option would imply higher bandwidth requirements than the envelope signal in conventional polar transmitters.

The proposed architecture can be seen in greater detail in Fig. 3.2. Both baseband signals I and Q are generated at the digital processor unit, and

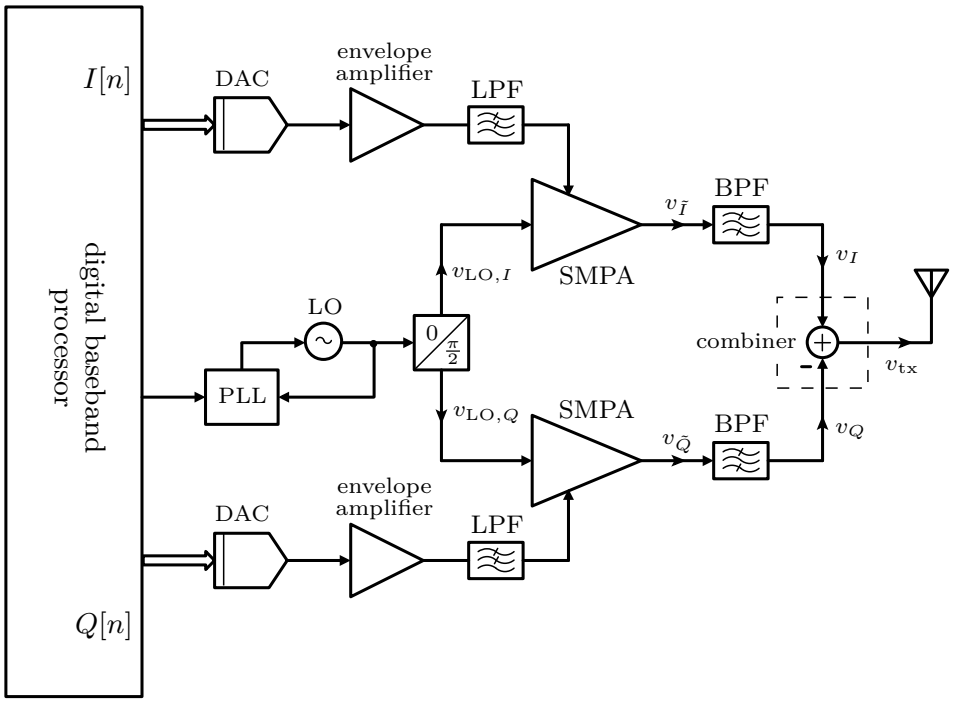


Figure 3.2: Block diagram of the C-P transmitter architecture.

then converted into the analog domain. DACs are employed to obtain the formats $I(t)$ and $Q(t)$ as required. The following envelope amplifiers are used to further amplify these baseband signals, which can be done either through linear regulators [129] or SMPS techniques [7], e.g. using $\Delta\Sigma$ or PWM techniques in the latter. The reconstruction filter is represented by the low-pass filter (LPF), required to attenuate spectrum replicas due to switching, and prevent aliasing in the following circuits that operate as multipliers.

Frequency up-conversion takes place at the polar amplifiers employed as bipolar SMPAs with quadrature carriers at their inputs. The phase-locked loop (PLL) generates the local oscillator (LO) signal at the carrier frequency, then decomposed into quadrature signals, e.g. by a polyphase filter, hence resulting in fixed tones

$$v_{\mathrm{LO},I}(t) \propto \cos(\omega_c t) \tag{3.1}$$

$$v_{\mathrm{LO},Q}(t) \propto \sin(\omega_c t) \tag{3.2}$$

In the proposed architecture, no wide-band phase-modulation scheme is demanded as it happens in driving of polar transmitters. Besides the constant quadrature, the only restriction imposed on these signals is that the amplitudes are kept high enough to prevent drain-efficiency degradation. Under ideal conditions, the voltage at the output of the polar amplifiers can be described as

$$v_{\tilde{I}}(t) \;\propto\; I(t)\cdot \mathrm{sgn}[\cos(\omega_c t)] \tag{3.3}$$

$$v_{\tilde{Q}}(t) \;\propto\; Q(t)\cdot \mathrm{sgn}[\sin(\omega_c t)] \tag{3.4}$$

To achieve the desired combining integrity, the signals at the output of each polar amplifier are filtered by a band-pass filter (BPF) to remove higher-order frequency components due to switching. The modulated signals need now to be combined to obtain the RF output. Simple structures of power combiners, such as the Wilkinson or matched-hybrid combiners, present typical fractional bandwidths in the order of 20% [130], which is fairly enough for the RF signals in modern standards. The output due to filtering and combining of (3.3)–(3.4) is then

$$v_{\mathrm{tx}}(t) \;=\; v_I(t) - v_Q(t) \;\propto\; \mathrm{BPF}\{v_{\tilde{I}}(t)\} - \mathrm{BPF}\{v_{\tilde{Q}}(t)\} \tag{3.5}$$

$$\propto\; I(t)\cos(\omega_c t) - Q(t)\sin(\omega_c t) \tag{3.6}$$

Under perfect isolating conditions, the load seen by each polar amplifier is kept constant, independently of the output power level. As a consequence, the linearity of the individual polar amplifiers can be preserved, at the expense of some efficiency degradation. But, as we will show later, this degradation is smaller than what is observed in the LINC based in a similar combiner. Beyond this, the linear performance in the C-P transmitter is dictated by the linearity of the envelope amplifiers. In fact, this resembles the typical limitation in terms of linear performance of polar transmitter. However, as described next, the structure of the C-P architecture presents some inherent advantages to alleviate this problem.

3.2 Bandwidth

In the polar architecture, the bandwidth of both phase and envelope signals impose critical limitations in terms of performance. This is because the conversion from IQ baseband into amplitude- and phase-modulated signals widens their spectra significantly. As an example, Fig. 3.3 shows the power spectrum density (PSD) of a 16-QAM signal for 10^4 random symbols applied to FIR pulse-shaping filters with 0.35 roll-off factor and order 10, sampled at 16 times the baseband data f_{BB}. Both the envelope $A(f/f_{\mathrm{BB}})$ and phase $\phi(f/f_{\mathrm{BB}})$ show that their spectra noticeably widens when comparing to the original I and Q signals.

As a result, not only the wide bandwidth of the carrier (with constant envelope and modulated in phase) reduces the efficiency of a typical narrow-band RF-PA operating in class E or F, as the wide bandwidth of the envelope signal increases the switching-losses of the envelope amplifier. Hence, the extended bandwidths in the polar architecture potentially degrades the overall transmitter efficiency.

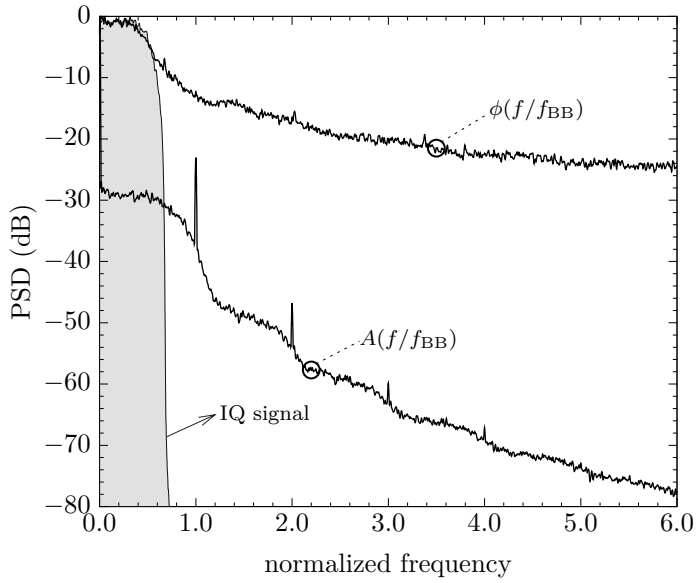


Figure 3.3: Complex baseband PSD of a 16-QAM signal (magnitudes normalized to individual PSD peaks).

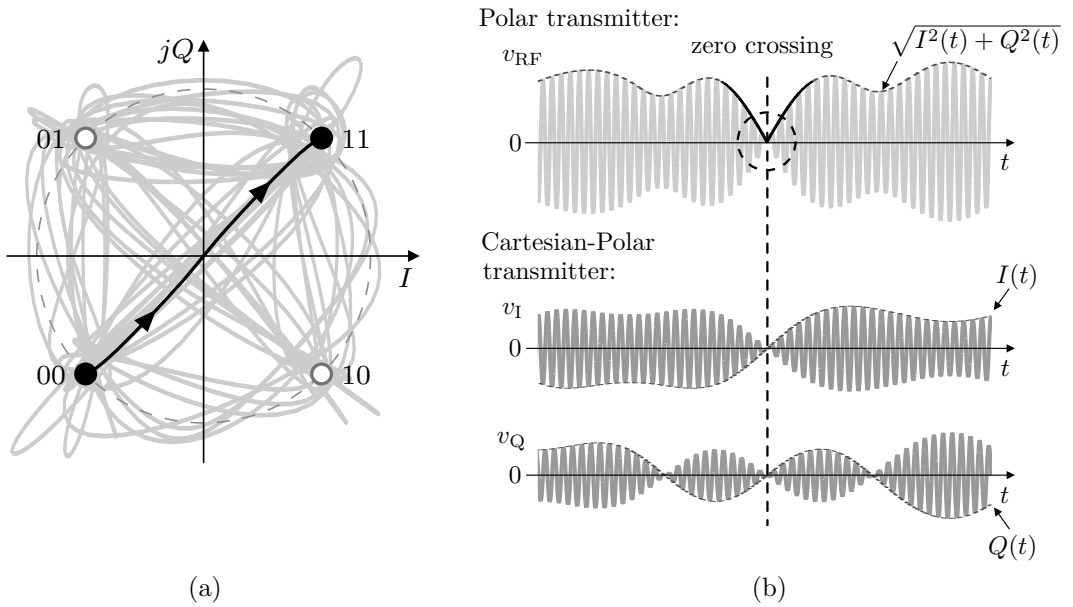


Figure 3.4: Zero-crossings example in polar and C-P Txs in (a) the IQ constellation; and (b) respective time waveforms in both architectures.

Additionally, as demonstrated in [73], the finite bandwidth of the envelope amplifier acts as a linearity degradation mechanism in the polar architecture. In the proposed C-P transmitter, the envelope signals are the I and Q signals directly modulating the power supplies of the PAs. Since in practice these signals are typically provided by pulse-shaping filters and therefore are band limited, its impact on linearity is much more relaxed than in the case of a polar transmitter. This is due to bipolarity of the I and Q signals, which avoids any conversion requirement to obtain only positive voltages for the drain modulation.

The most explicit example in which this has a significant advantage is the case of a zero crossing in the IQ constellation, as illustrated in Fig. 3.4(a). These type of trajectories substantially widen the spectrum at the output and require complex techniques to reduce their impact, e.g. [131]. Fig. 3.4(b) depicts the envelope signals for the polar and C-P transmitters for the same output. As shown, an abrupt change in the derivative of the envelope in the polar transmitter can be avoided by the bipolarity on the IQ signals with the C-P approach.

Let us consider the hybrid switching amplifier for the envelope modulation, which lately has become quite popular in the research of polar transmitters. Fig. 3.5 shows the most typical circuit representation for the amplifier. Several modulation schemes were used to generate signals $I(t)$, $Q(t)$ and respective $A(t)$, with distinct roll-off factors in the square-root raised-cosine filter, to provide some diversity on the PAPR. Around 10,000 symbols were randomly generated during $T_N \sim 10\,\mathrm{ms}$, fitting a maximum bandwidth of 1 MHz. These signals were used in Cadence Virtuoso environment with the blocks from the envelope amplifier implemented in Verilog-A language. Let us define the power absorbed by the linear amplifier as $P_{\mathrm{lin}}^{-} = \frac{1}{T_N}\int v_{\mathrm{env}}(t)\, i_{\mathrm{lin}}^{-}(t)\,\mathrm{d}t$, where $i_{\mathrm{lin}}^{-}(t)$ is the negative part of $i_{\mathrm{lin}}(t)$, being zero otherwise. On the other hand, the power provided by the linear amplifier can be defined similarly as $P_{\mathrm{lin}}^{+} = \frac{1}{T_N}\int v_{\mathrm{env}}(t)\, i_{\mathrm{lin}}^{+}(t)\,\mathrm{d}t$ with $i_{\mathrm{lin}}^{+}(t)$ as the positive part of $i_{\mathrm{lin}}(t)$ – with zero otherwise, as well. The average power provided by the switching amplifier is denoted as P_{sw}. Let us also normalize these quantities to the average power consumption at the load (i.e. the PA), P_{PA}, as

$$\widetilde{p}_{\mathrm{lin}}^{-} = P_{\mathrm{lin}}^{-}/P_{\mathrm{PA}}, \quad \widetilde{p}_{\mathrm{lin}}^{+} = P_{\mathrm{lin}}^{+}/P_{\mathrm{PA}}, \quad \widetilde{p}_{\mathrm{sw}} = P_{\mathrm{sw}}^{+}/P_{\mathrm{PA}} \tag{3.7}$$

The simulation results are presented in Table 3.1 including the calculated average switching frequency $\langle f_{\mathrm{sw}} \rangle$, which by itself is not sufficient for a performance analysis. Instead, the amount of power provided by each block is considered. The power provided by the linear amplifier is diminished with larger PAPRs. Generally, this situation occurs near zero, when the required power is also minimum. On the other hand, with the increase of PAPR, the filtering action for the switching signals becomes demanding. In fact, this is performed by the linear amplifier, whereas the relative amount of power absorbed is given by $\widetilde{p}_{\mathrm{lin}}^{-}$. This is only noticeable in the amplitude signal $A(t)$. Therefore, the hybrid switching envelope amplifier is sensitive to large PAPRs, but in particular for the $A(t)$ signals. In contrast, the $I(t)$ and $Q(t)$ signals are almost unresponsive to the PAPR increase.

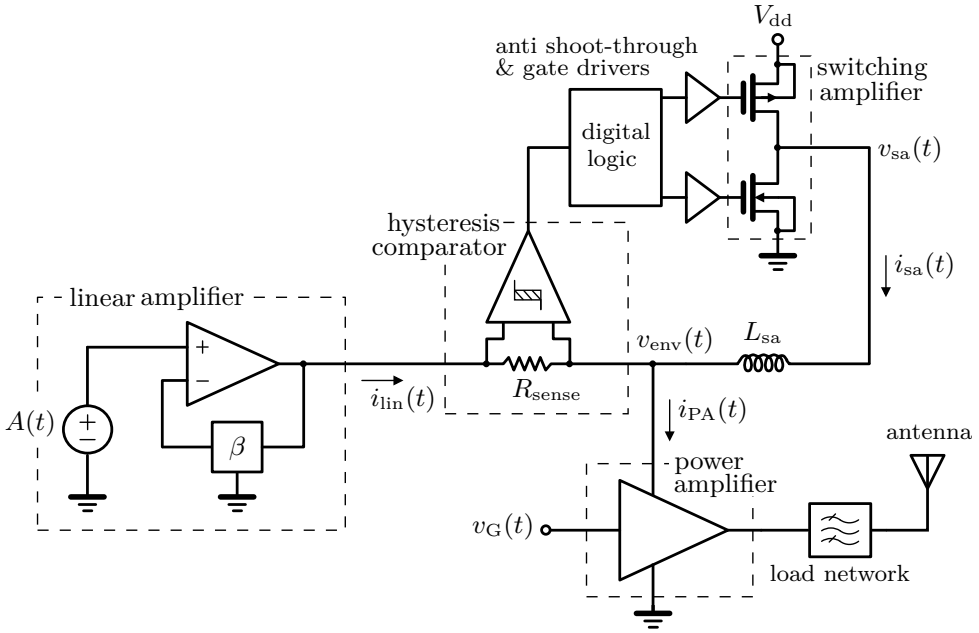


Figure 3.5: Conventional hybrid-switching envelope amplifier.

Table 3.1: Influence of the PAPR in the performance of the hybrid switching amplifier.

mod. format	PAPR (dB)	$\langle f_{sw}\rangle$(kHz)			$\widetilde{p}^{-}_{lin}$(%)			$\widetilde{p}^{+}_{lin}$(%)			$\widetilde{p}_{sw}-\widetilde{p}^{-}_{lin}$(%)		
		I	Q	A	I	Q	A	I	Q	A	I	Q	A
O-QPSK	2	260	258	590	35	35	28	26	26	14	74	74	86
8-PSK	4	557	561	680	37	36	37	12	12	15	88	88	85
	5	607	603	700	36	37	42	9	10	12	91	90	88
	6	650	682	709	36	37	47	8	7	11	92	93	89
16-PSK	4	556	547	681	37	37	37	12	13	15	88	87	85
	5	590	600	704	36	38	42	10	10	12	90	90	88
	6	633	669	709	37	38	47	9	7	11	91	93	89
	7	667	701	718	37	36	52	7	7	9	93	93	91
16-QAM	6	521	520	588	37	37	47	15	15	15	85	85	85
	7	582	584	593	37	37	52	11	11	12	89	89	88
	8	721	684	585	37	37	56	6	7	10	94	93	90
64-QAM	7	595	608	612	36	37	52	12	11	13	88	89	87
	8	674	680	593	36	38	56	8	8	10	92	92	90
	9	719	749	583	37	39	61	7	6	9	93	94	91
OFDM	12	859	845	645	40	39	75	8	8	11	92	92	89

3.2.1 Impact of finite bandwidth of dynamic power-supply

Since the polar and C-P architectures work with different driving signals, let us now address the impact of the finite bandwidth of the envelope modulator, and also due to possible time misalignments. Consider the Fig. 3.6 in which the C-P transmitter has an LPF in the I and Q paths, as well as a time delay of τ seconds in one of the branches. Only one branch is considered for misalignments, because equal delays are easily compensated by proper synchronization in the receiver. Hence, only the differential delay is admitted. For the case of the polar transmitter, a similar structure is assumed in the envelope path.

For simplicity, a first-order filter is applied. The cut-off frequency of the filter $f_{3\text{dB}}$ is swept and its influence is studied by means of the resultant EVM. The same QAM signal previously presented in Fig. 3.3 has been used. An ideal receiver is employed with ideal LPFs followed by square-root cosine pulse shaping as matched filters to recover the symbols.

Fig. 3.7 shows the EVM with frequency normalized as $f_{3\text{dB}}/f_{\text{BB}}$. The results are plotted for different time delays in terms of the bandwidth, i.e. $\tau = [\,0, \frac{1}{16}/f_{\text{bb}}, \frac{2}{16}/f_{\text{bb}}\,]$. The results are not obvious, i.e. the polar transmitter is less sensitive to both nonidealities. This seems to go against

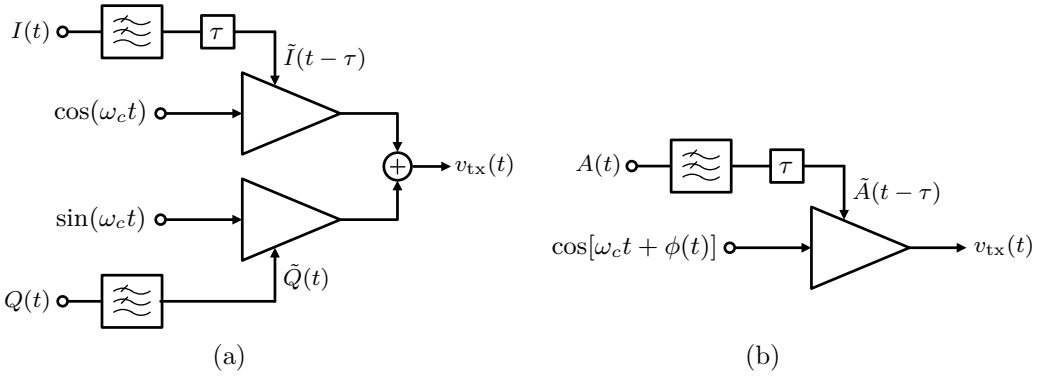


Figure 3.6: System models for study of the impact of finite bandwidth and time delays in signal paths of the (a) C-P and (b) polar architectures.

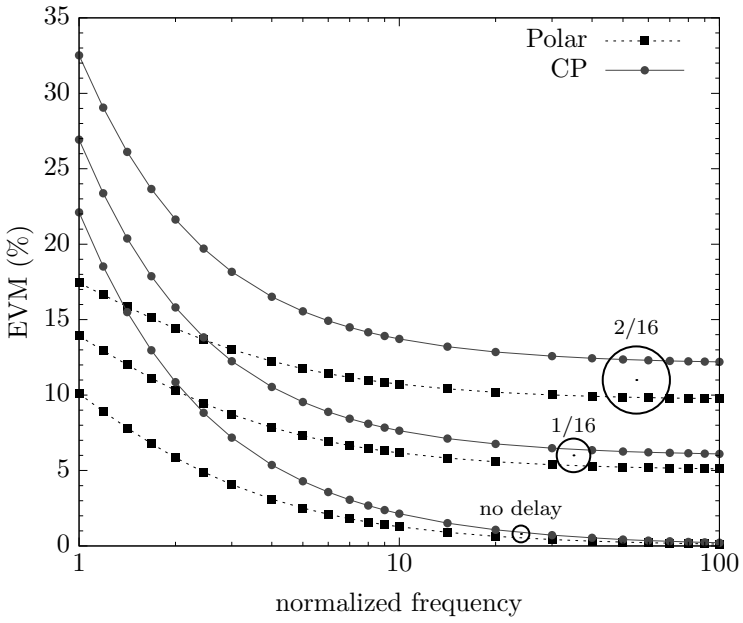


Figure 3.7: Impact of time misalignments in the output spectrum of polar and C-P architectures.

what might be expected. It should be reminded, however, that the EVM addresses in-band distortion and is not influenced by spectral regrowth. For the same parameter values let us also analyze the resultant spectrum.

Fig. 3.8 shows the PSD for the signals comprising different values of $\tau = [\frac{1}{16}, \frac{1}{8}, \frac{3}{16}, \frac{1}{4}, \frac{5}{16}]/f_{\mathrm{bb}}$. The delay value has no significant impact in adjacent channels for the C-P system, since it remains nearly the same as the original signal. However, the sensitivity to any time misalignment in the polar transmitter is quite noticeable, thereby increasing the adjacent-channel power ratio (ACPR).

3.3 Efficiency Analysis

In polar transmitters, most of the high-efficiency envelope amplifiers consist of switching-mode topologies [67, 132–134]. The efficiency of those amplifiers is strongly affected by the operating frequency, i.e. it tends

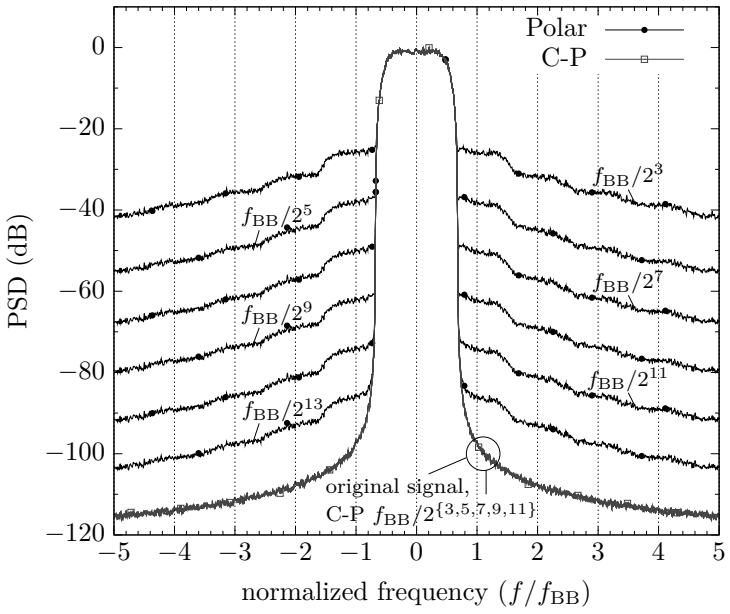


Figure 3.8: Impact of finite bandwidth of the envelope modulator in EVM of polar and C-P architectures.

to decrease significantly for signal with wide bandwidth signals since the required sampling frequency is higher with higher inherent switching losses. Nonetheless, as previously mentioned, the envelope bandwidth required in the C-P transmitter is fairly reduced when compared with other polar architectures. Therefore, it is expected higher envelope efficiencies attained with the proposed architecture.

The output of the proposed C-P transmitter consists of a matched-hybrid combiner at the end of the I and Q branches (Fig. 3.2). This is similar to a LINC transmitter with isolated combiner. In such a case, if one assumes equal phases at the combiner inputs, no power consumption takes place at the isolating port. That is, transmitting at PEP results in the maximum efficiency for the LINC [113]. The important difference to the proposed architecture is that the efficiency does not depend on the output power level. One should note that I and Q signals can independently vary their amplitudes. This means some power is dissipated at the isolating port. But, as illustrated in Fig. 3.9, summing and subtracting

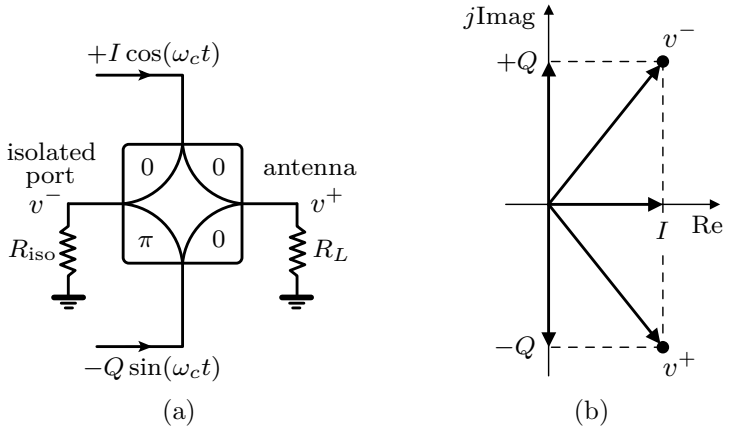


Figure 3.9: Signal decomposition at the output combiner of the C-P Tx architecture – (a) symbol and (b) vector representations.

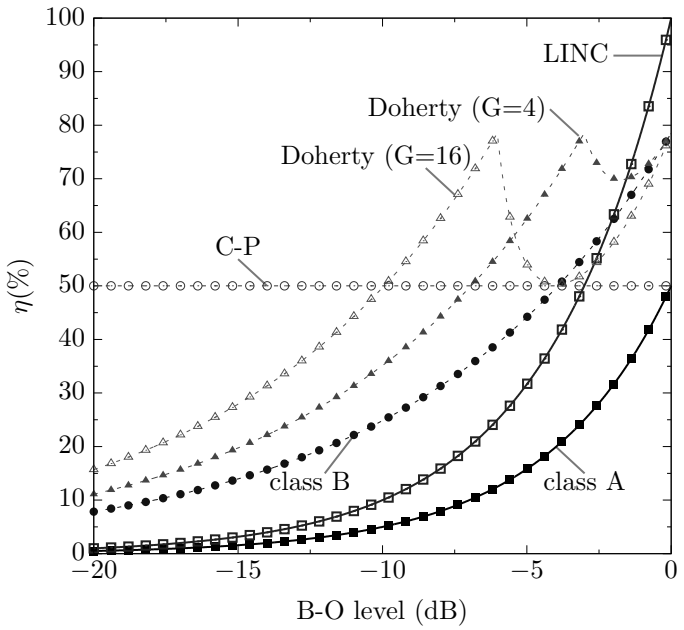


Figure 3.10: Drain efficiencies in terms of B-O values for different wireless transmitter systems.

the inputs leads to the same power level due to the orthogonality of the signals. Therefore, the power is equally split between the antenna and the isolated port of the output combiner. It can be concluded that the efficiency of the C-P is 50 % irrespective of the B-O level. Fig. 3.10 shows a comparison between drain efficiencies of different linear transmitter systems. The efficiency of C-P architecture is compared against classes A and

B, LINC transmitter comprising a matched-hybrid combiner, and conventional and asymmetrical Doherty amplifier ($G = P_{\max}/P_{\mathrm{t}} = 4$ and $G = 16$, respectively, where P_{t} is the peak-amplifier turn-on point). The efficiencies of the Doherty amplifiers are noticeably higher than the C-P transmitter for PAPR values in the vicinity of $P_{\max}/P_{\mathrm{t}}$. However, regarding multiple wireless standards with different B-O levels, the Doherty topology requires peak efficiency optimization. This would require physical changes in the characteristic impedance of the transmission lines according to the power B-O level [25], which poses a reconfigurability limitation in wireless communication for multiple network standards within the same RF band. As for the LINC transmitter, whenever the power B-O is higher than 3 dB, the C-P architecture presents much higher efficiencies. One should note that this PAPR value is fairly reduced. As examples, EDGE has a PAPR relatively constant in the order of 3.4 dB, whereas wireless LAN 802.11g has PAPRs ranging from 6 to 17 dB. In the latter case, a constant efficiency as the C-P would bring significant advantages over the LINC transmitter.

3.4 Effect of Power Recycling

To improve the efficiency performance, the concept of power recycling has been applied together with matched-hybrid combiners in LINC systems in [31–33]. Due to the similarities at the output power-combining scheme, the same concept can be extended to the now proposed C-P architecture.

Fig. 3.11 shows a representative diagram of a transmitter comprising a power-recycling mechanism. The RF power is obtained from a combination of the outputs of the power amplifiers, whereas the differential power component flows into the isolated port and the remaining part into the antenna. To perform RF-to-dc conversion, the load at the isolated port is replaced by a recycling network. Consequently, the power that would be wasted at the isolation load is recovered back to the power-supply of the amplifiers, enhancing the overall efficiency of the transmitter.

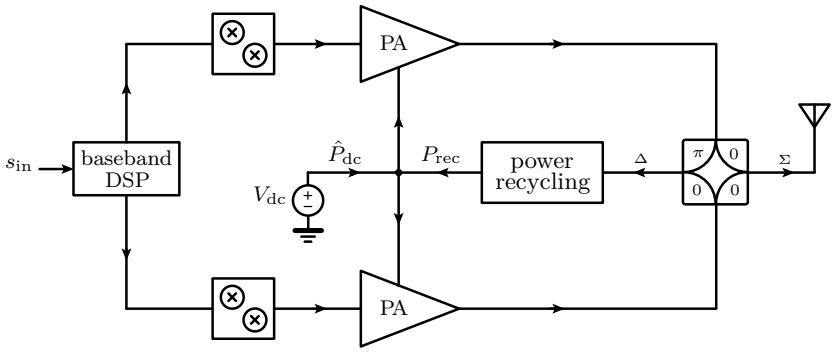


Figure 3.11: RF Tx with power recycling.

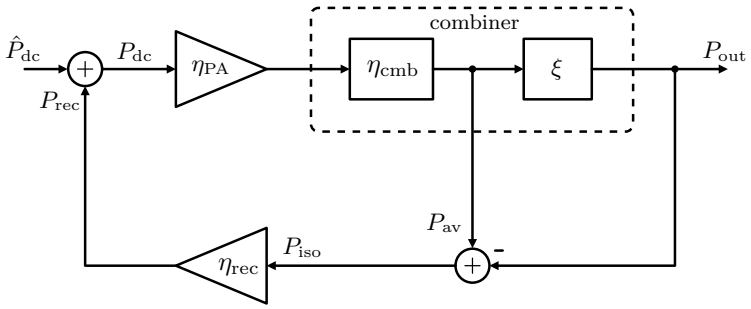


Figure 3.12: Power-flow diagram of power-recycling Txs.

Fig. 3.12 shows a representation of the power flow that takes place on a typical power-recycling mechanism. Based on the diagram representation, the overall efficiency of the transmitter system, including the recovered power, is given by

$$\eta(P_{\text{out}}) = \frac{P_{\text{out}}}{\widehat{P}_{\text{dc}}} = \frac{P_{\text{out}}}{P_{\text{dc}} - P_{\text{rec}}} \tag{3.8}$$

$$= \frac{\xi(P_{\text{out}}) \cdot \eta_{\text{PA}} \cdot \eta_{\text{cmb}}}{1 - \eta_{\text{rec}} \cdot \eta_{\text{PA}} \cdot \eta_{\text{cmb}} \cdot [1 - \xi(P_{\text{out}})]} \tag{3.9}$$

which coincides with the result derived by Godoy *et al.* [33]. The parameters η_{PA}, η_{cmb} and η_{rec} are, respectively, the efficiencies of the PA, combiner and recycling network. The parameter ξ is defined as the ratio between output power and the power available at the combiner inputs, $\xi = P_{\text{out}}/P_{\text{av}}$. This is related to the type of signals applied at the combiner, thus determined by the transmitter architecture. For the case of the LINC transmitter, P_{av} represents the maximum power. Hence, ξ is maximum

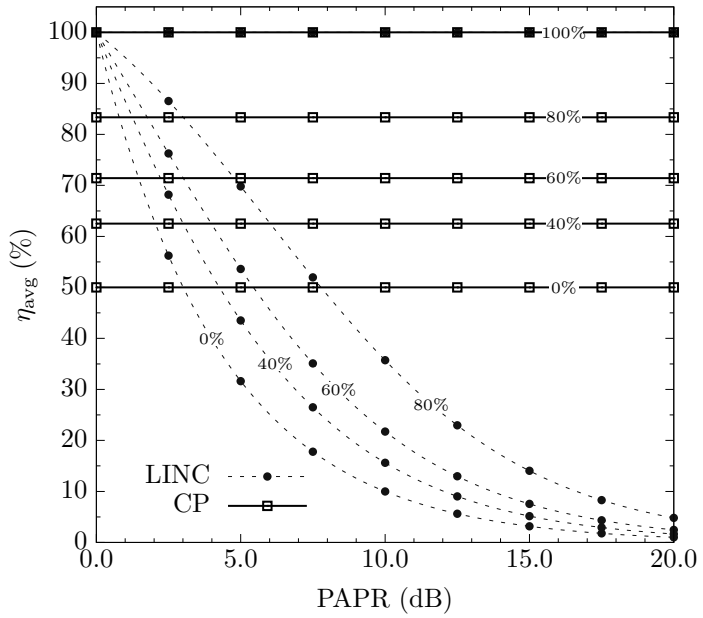


Figure 3.13: Average efficiencies with recycling systems in LINC with isolated combiner, and the C-P Tx ($\eta_{PA} = \eta_{cmb} = 100\%$).

solely when the outphasing angle is null. In the C-P transmitter, there is a constant relationship between the power delivered to the antenna and the power flowing into the isolated port, which is 50 %. Applying this result in (3.9), the efficiency for the C-P transmitter with power recycling can be written as

$$\eta(\eta_{rec}) = \frac{\eta_{PA} \cdot \eta_{cmb}}{2 - \eta_{rec} \cdot \eta_{PA} \cdot \eta_{cmb}} \tag{3.10}$$

Fig. 3.13 and Fig. 3.14 show the average efficiencies for the C-P architecture with power recycling included. In Fig. 3.13 the LINC with isolated combiner is also shown so that it can be compared with the C-P transmitter for different PAPR values. As shown, with the same recycling efficiency, the C-P architecture achieves much higher average efficiency. Some studies have reported efficiencies on RF-to-dc conversion η_{rec} up to 76 % at 5.8 GHz [135]. From Fig. 3.14 one can conclude that, ideally, the same recycling efficiency would be sufficient to increase the overall efficiency to about 80 % in a C-P architecture.

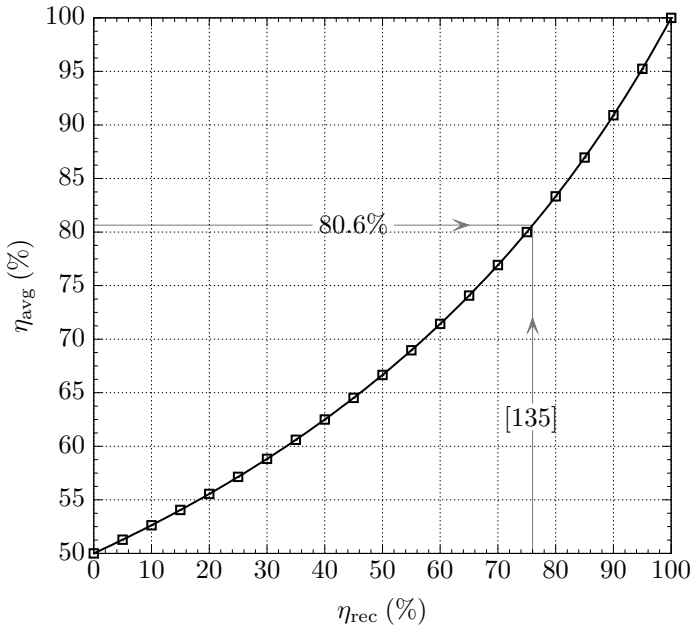


Figure 3.14: Average efficiency of the C-P Tx for different recycling-network efficiencies.

3.5 Sensitivity to Structural Impairments

As the C-P architecture relies on a symmetric operation, this section will address the impact of system parameter mismatches on the overall performance. As in any other transmitter system, the signal integrity in the C-P architecture is affected by different impairments, specifically due to gain and phase mismatches and dc offsets. The EVM will be firstly used to characterize the performance of the C-P transmitter and, in the end of the section, the spectral regrowth will also be addressed. In order to establish a performance comparison metric between the the C-P transmitter and another linear transmitter architecture under the same operating conditions, an analytical formulation for the EVM is derived for the LINC transmitter with isolated combiner.

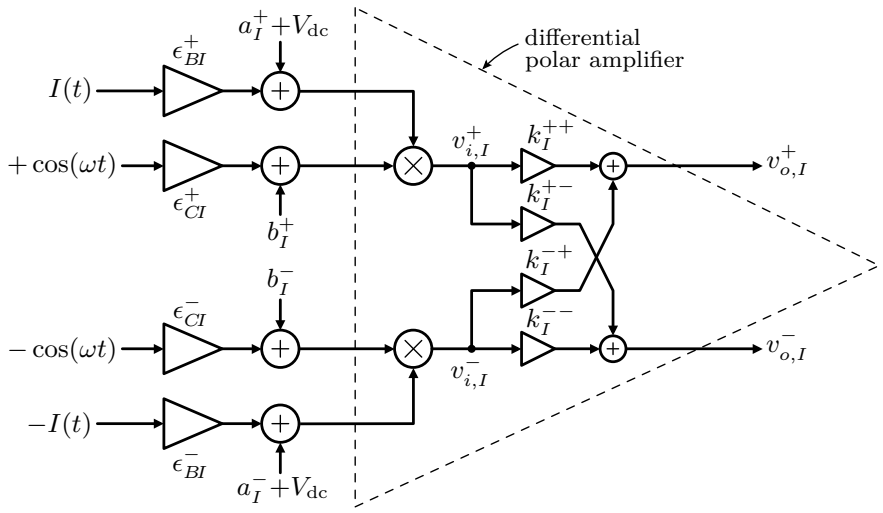


Figure 3.15: Block diagram for study of impairments in the I branch of the C-P Tx.

Let us consider the system impairments depicted in Fig. 3.15. Although, for simplicity, only the I branch is depicted there, an equivalent representation is assumed for the quadrature counterpart. Each carrier differential-signal is affected by constant gain (ϵ_{CI}) and dc-offset (b_I) impairments. Under ideal operation, the gain parameters are unitary while the dc-offset terms are null. In the baseband circuitry, similar mismatches are also included, i.e. ϵ_{BI} and a_I, respectively. Each gain impairment comprises magnitude and phase mismatches.

From Fig. 3.15, the signals at the multipliers can be expressed as $\mathbf{v_{i,I}} = [v_{i,I}^{+}, v_{i,I}^{-}]^T$, with "$T$" denoting transpose operation. In this way, the signals at both branches are given by

$$\mathbf{v_{i,I}}(t) = \begin{bmatrix} \Big(a_I^{+} + V_{\rm dc} + \epsilon_{BI}^{+}\ I(t)\Big) \cdot \Big(b_I^{+} + \epsilon_{CI}^{+}\cos(\omega t)\Big) \\ \Big(a_I^{-} + V_{\rm dc} - \epsilon_{BI}^{-}\ I(t)\Big) \cdot \Big(b_I^{-} - \epsilon_{CI}^{-}\cos(\omega t)\Big) \end{bmatrix} \tag{3.11}$$

$$\mathbf{v_{i,Q}}(t) = \begin{bmatrix} \Big(a_Q^{+} + V_{\rm dc} + \epsilon_{BQ}^{-}Q(t)\Big) \cdot \Big(b_Q^{+} - \epsilon_{CQ}^{+}\sin(\omega t)\Big) \\ \Big(a_Q^{-} + V_{\rm dc} - \epsilon_{BQ}^{+}Q(t)\Big) \cdot \Big(b_Q^{-} + \epsilon_{CQ}^{-}\sin(\omega t)\Big) \end{bmatrix} \tag{3.12}$$

Taking the in-phase counterpart to describe the analysis procedure, at the differential outputs of the in-phase amplifier, $\mathbf{v_{o,I}} = [v_{o,I}^{+}\ ,\ v_{o,I}^{-}]^T$ can be written in terms of (3.11) as follows

$$\mathbf{v_{o,I}}(t) = \begin{bmatrix} k_I^{++} & k_I^{-+} \\ k_I^{+-} & k_I^{--} \end{bmatrix} \cdot \mathbf{v_{i,I}}(t) \tag{3.13}$$

The combined signals comprise several terms grouped into four functions differing in their spectral properties

$$v_I(t) = v_{o,I}^{+}(t) + v_{o,I}^{-}(t) \tag{3.14}$$

$$= f_{\mathrm{dc}_I} + f_{BB_I}[I(t)] + f_{CI}[\cos(\omega t)] + f_{RF_I}[I(t), \cos(\omega t)] \tag{3.15}$$

where f_{dc_I} comprises the dc terms, f_{BB_I} and f_{CI} groups the baseband and carrier constant-leakage components, respectively, and f_{RF} comprises the carrier-modulated signals. The first two terms consist of dc and baseband signals that can be discarded due to RF filtering at the combiner (see Fig. 3.2). Furthermore, the function f_{CI} represents a systematic IQ-origin deviation that is compensated assuming proper correction techniques at the receiver. In this sense, one can consider only f_{RF} in both branches for the EVM analysis, given by

$$f_{RF_I}[I(t), \cos(\omega t)] = I(t) \cdot \cos(\omega t) \cdot \Big(\left(k_I^{++} + k_I^{+-}\right) \cdot \epsilon_{BI}^{+} \cdot \epsilon_{CI}^{+} + \left(k_I^{-+} + k_I^{--}\right) \cdot \epsilon_{BI}^{-} \cdot \epsilon_{CI}^{-} \Big) \tag{3.16}$$

$$f_{RF_Q}[Q(t), \sin(\omega t)] = -Q(t) \cdot \sin(\omega t) \cdot \Big(\left(k_Q^{++} + k_Q^{+-}\right) \cdot \epsilon_{BQ}^{+} \cdot \epsilon_{CQ}^{+} - \left(k_Q^{-+} + k_Q^{--}\right) \cdot \epsilon_{BQ}^{-} \cdot \epsilon_{CQ}^{-} \Big) \tag{3.17}$$

This indicates that, in terms of system impairments, the C-P performance is equivalent to a Cartesian transmitter with imperfect quadrature between the I and Q branches. Let us now define the gain and phase impairments respectively as g and $\Delta\phi$. The output signal can be written as an RF signal

with phase and gain impairments as depicted in Figure 3.16(a)

$$\hat{v}_I(t) = g_I \cdot e^{j\Delta\phi_I} \cdot I(t) \cdot \cos(\omega t) \tag{3.18}$$

$$\hat{v}_Q(t) = -g_Q \cdot e^{j\Delta\phi_Q} \cdot Q(t) \cdot \sin(\omega t) \tag{3.19}$$

In order to compute the modulation accuracy, let us use the EVM of an m-ary modulation, defined by its rms for N transmitted symbols as in [136–139],

$$\mathrm{EVM}^2_{\mathrm{rms}} \triangleq \frac{\sum_{k=1}^{N} |\mathbf{s}_n[m] - \hat{\mathbf{s}}_n[m]|^2}{\sum_{k=1}^{N} |\mathbf{s}_n[m]|^2} \tag{3.20}$$

with $\mathbf{s}$ being the ideal coordinate of the symbol, and $\hat{\mathbf{s}}$ the obtained symbol. Let us assume symmetric impairments [140], with

$$g = \frac{g_I}{g_Q}\,, \qquad g_Q = \sqrt{\frac{2}{1+g^2}} \tag{3.21}$$

and for the phase mismatches

$$\Delta\phi_I = -\Delta\phi_Q = \frac{\Delta\phi}{2} \tag{3.22}$$

This way, one can analytically express the EVM similarly to that derived in [141]

$$\mathrm{EVM}_{\mathrm{rms}} = 100\% \cdot \left[2 - \left(2 + \frac{4 \cdot g}{1+g^2} \right)^{1/2} \cdot \cos\left(\frac{\Delta\phi}{2} \right) \right]^{1/2} \tag{3.23}$$

The symmetric impairment approach admits perfect phase-rotation compensation at the receiver so that the EVM can be kept to a minimum level[1]. The LINC transmitter with isolated combiner can be used for performance comparison under the same considerations – Fig. 3.16(b). Gain mismatches are considered due to impairments on the two RF paths and saturated gains of the switching-mode amplifiers, as well as phase mismatches

$$\hat{s}_1(t) = s_1(t) \cdot g_1 \cdot e^{+j\frac{\Delta\phi}{2}} \tag{3.24}$$

$$\hat{s}_2(t) = s_2(t) \cdot g_2 \cdot e^{-j\frac{\Delta\phi}{2}} \tag{3.25}$$

[1]This differs from other EVM analysis in literature where asymmetric impairments lead to higher values for the (not compensated) EVM, e.g. [142].

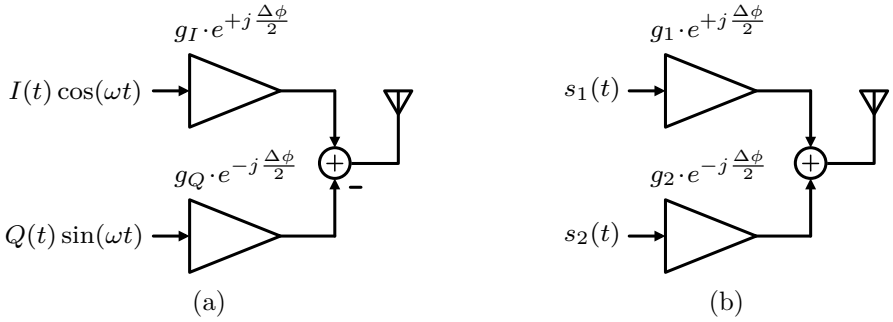


Figure 3.16: Block diagrams with RF path impairments included for analysis in the (a) Cartesian/C-P and (b) LINC transmitters.

whereas g_1 and g_2 are respectively equivalent to g_I and q_Q as given in (3.21). In [143], the authors present an approximation for small angles that simplifies the calculation of the EVM. In order to establish a fair comparison, the EVM described herein follow an exact analysis. The resultant error signal is defined as

$$e(t) = s_1(t) - \hat{s}_1(t) + s_2(t) - \hat{s}_2(t) \tag{3.26}$$

Using the complex envelope notation, the squared magnitude of the error is given by

$$\begin{aligned} \frac{|e|^2}{\mathrm{A}_{\max}^2} &= \left[\cos(\phi) - \frac{g_1+g_2}{2}\cdot\cos\left(\phi+\frac{\Delta\phi}{2}\right)\right]^2 \\ &\quad + \left(\frac{g_1-g_2}{2}\right)^2\cdot\sin^2\left(\phi+\frac{\Delta\phi}{2}\right) \end{aligned} \tag{3.27}$$

The result in (3.27) can be further developed to be used in the EVM computation as follows

$$\begin{aligned} \frac{\mathrm{EVM_{rms}}}{\mathrm{A_{max}}} &= 100\%\cdot\left(\tfrac{1}{\mathrm{M}}\cdot\sum_{k=1}^{\mathrm{M}}\left[\frac{1}{2}+\frac{g}{1+g^2}\cdot\cos(2\phi+\Delta\phi)\right.\right. \\ &\quad -(g+1)\cdot\sqrt{\frac{2}{1+g^2}}\cdot\cos(\phi)\cdot\cos\left(\phi+\frac{\Delta}{2}\right) \\ &\quad \left.\left.+\cos^2(\phi)\right]\right)^{1/2}\Big/\left(\tfrac{1}{\mathrm{M}}\cdot\sum_{k=1}^{\mathrm{M}}|s_{1_k}+s_{2_k}|^2\right)^{1/2} \end{aligned} \tag{3.28}$$

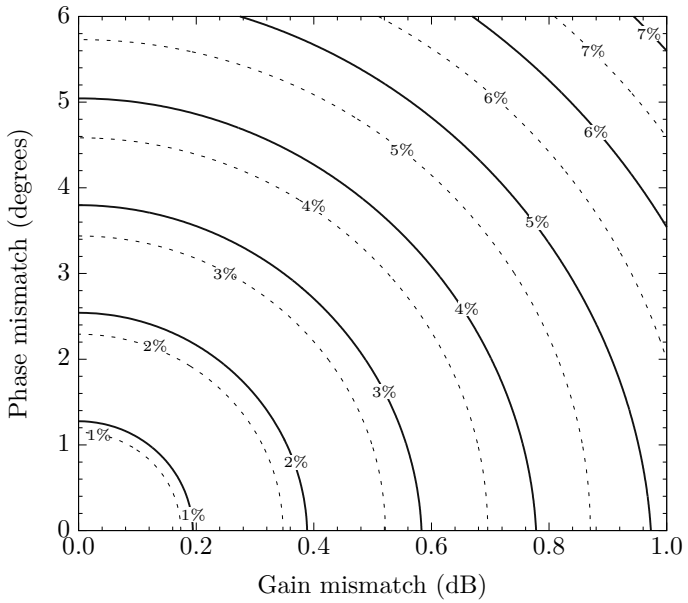


Figure 3.17: 16-QAM EVM comparison between Cartesian/C-P (solid lines) and LINC (dashed lines) architectures.

Contrary to the case of the C-P transmitter, the EVM for the LINC is strongly dependent on the modulation format. In order to compare both architectures, we will use a 16-QAM modulation. This allows us to relate the ϕ_k terms with $\mathrm{A_{max}}$ in any given k-symbol of the 16-point constellation, resulting in

$$\begin{aligned} \mathrm{EVM_{rms}} \;=\; 100\% \cdot \Bigg(& \frac{1}{5} \cdot \frac{g}{1+g^2} \cdot \Big[\cos(\Delta\phi) \\ & - \sqrt{2} \cdot \left(1+\sqrt{10}\right) \cdot \sin(\Delta\phi) \Big] \\ & - (g+1) \cdot \sqrt{\frac{2}{1+g^2}} \cdot \left[\cos\left(\frac{\Delta\phi}{2}\right) \right. \\ & \left. - \sqrt{2} \cdot \frac{1+\sqrt{10}}{10} \cdot \sin\left(\frac{\Delta\phi}{2}\right) \right] + 1.9 \Bigg)^{1/2} \end{aligned} \tag{3.29}$$

Fig. 3.17 shows constant EVM curves for the Cartesian/C-P and LINC architectures assuming an ideal receiver. As shown, the LINC is much more

prone to parameter impairments than the Cartesian topologies. This tends to increase significantly for larger values of gain and phase mismatches.

One main drawback of the C-P transmitter is the potential carrier leakage. It mainly affects the power efficiency of the transmitter. Although this effect is mitigated in the LINC, there are other linearity aspects to be considered. Due to imprecise cancellation in the LINC output combiner, the spectrum of the transmitted signal is significantly increased [144]. This is a consequence of the nonlinear signal conversions required by the LINC architecture. On the other hand, it can be seen that having the same output combiner structure, the linearity can be preserved in the C-P transmitter. Fig. 3.18 shows numerical results for the PSD obtained for both architectures operating under the same system impairments. A 16-QAM modulation is used with square-root raised cosine filters having 0.35 roll-off and 16 up-sampling factors. As shown in the PSD, the system impairments have a noticeably higher interference in the adjacent channels in the LINC transmitter.

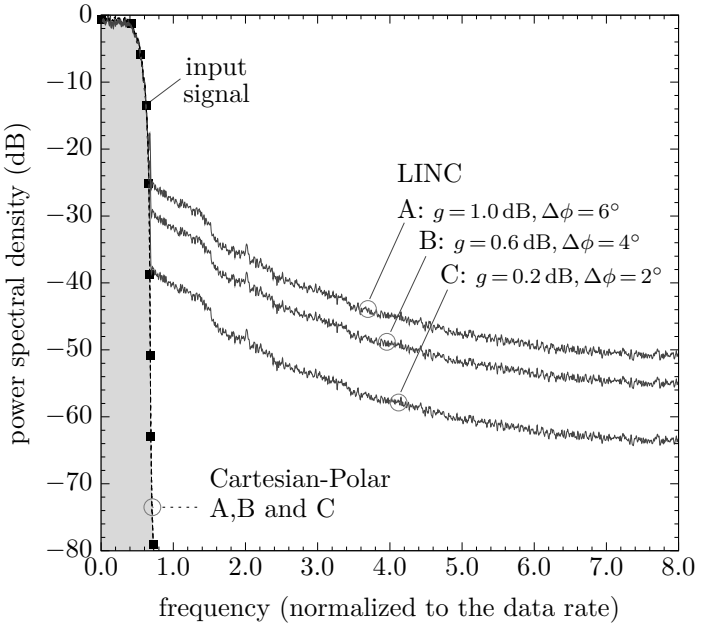


Figure 3.18: Output spectra for C-P and LINC transmitters with several phase and gain impairments.

Chapter 4

C-P Transmitter based on a Symmetric PA Topology

This chapter details a circuit topology for the hardware realization of a C-P transmitter in CMOS technologies. A class E using a CMOS technology is chosen as PA topology. Slight modifications are proposed to attain the required bipolarity for the signals. To prevent forward biasing of junction diodes of the transistor, the bulk is connected to a negative potential. This implies that, according to the envelope polarity, the drain and source may be interchanged. A comprehensive analysis for this four-quadrant PA is herein presented. It briefly addresses possible asymmetric behaviors in performance due to some relevant parameters. In particular, the proposed circuit topology is studied in terms of asymmetric current-to-voltage (I-V) characteristics, gate to source/drain capacitive behavior, influence of non-grounded bulk, input impedance and matching. Other general issues, such as gate driving, relationship between output power and efficiency, and reliability details are also included in the analysis. Simulation results for the proposed C-P transmitter are presented at the end of the chapter. Along the text, all the simulation data shown is based on a BSIM3v3 model of a RF-CMOS process for thick-gate devices with minimum length of 0.34 μm.

An implementation for the proposed transmitter cannot be held in a simple and straightforward approach. The combination of I and Q modulated signals implies some concerns on efficiency and isolation and will be firstly

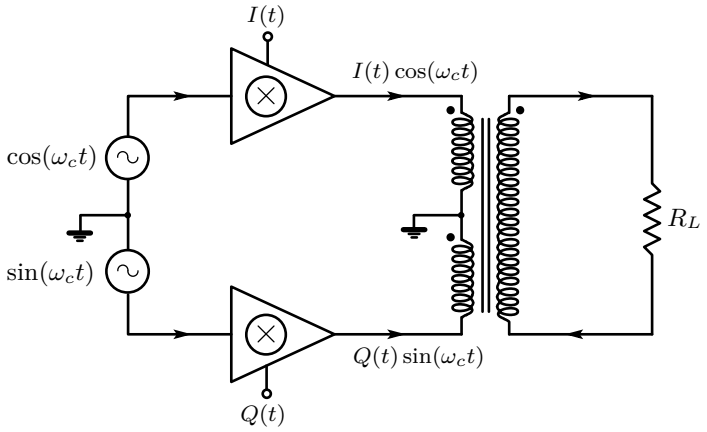


Figure 4.1: Simplified representation for a C-P architecture (non-isolated).

addressed. The representation in Fig. 4.1 can be seen as an RF transmitter based on the C-P architecture (or even the Cartesian architecture, itself). It relies on two high-level multipliers to obtain the in-phase and quadrature modulate signals, respectively $I(t)\cos(\omega_c t)$ and $Q(t)\sin(\omega_c t)$, generated by voltage (or current sources) with some finite output impedance. Both signals are added at the secondary winding of the centered-tapped transformer, to achieve the RF output at the antenna R_L.

Such oversimplified version of the C-P architecture is used here to emphasize a specific concern: the output power combination. It can be noticed that each primary winding is influenced by the other, due to loading effects from the secondary side into the primary sides. Hence, the voltage (or current) at each input will exhibit some influence on the magnitude and phase of its quadrature counterpart. Only when the two signals to be combined present equal or perfectly symmetric values at all time, the RF combiner (transformer) can be used efficiently without degrading isolation. However, in any IQ constellation, such condition is unlikely to occur (at all time), since I and Q modulated signals are provided by independent data sources.

Unless the transformer uses a specific center-tapped resistor, as in [33] or [145], the isolation between primary windings is seriously compromised. In other words, incorporating a dissipative element is required to provide port isolation. Otherwise, an immediate consequence is that both I and Q

signals mutually influence each other by means of load modulation, which is translated into nonlinear-distorted signals at the amplifier outputs and antenna.

The aforementioned approach conveys the idea that a certain degree of power dissipation is mandatory to ensure port isolation and, consequently, the required linearity. Furthermore, it implies that the transformer is converted into a three-port network so the resistive termination is properly included. In the absence of such a "dummy" load, the signal integrity is likely to deteriorate. The underlying reason for this is due to an interesting property of three-port time-invariant networks. That property states it is theoretically impossible for a three-port network to be simultaneously: *i)* lossless, *ii)* reciprocal, and *iii)* matched at all ports [34].

If the combiner is represented by the scattering matrix $[\,\mathrm{S}\,]$, then each of the three conditions is described as

- **lossless:** $[\,\mathrm{S}\,]$ must be unitary, i.e. $[\,\mathrm{S}\,][\,\mathrm{S}^*]^t = [\,\mathrm{S}^*]^t[\,\mathrm{S}\,] = [\,\mathrm{I}\,]$;
- **reciprocal:** $[\,\mathrm{S}\,]$ must be symmetric, i.e. $S_{ij} = S_{ji}$, $i \neq j$;
- **completely matched:** $S_{ii} = 0, \forall i$;

where $[\,\mathrm{S}^*]^t$ denotes the conjugate transpose of the scattering matrix, and $[\,\mathrm{I}\,]$ the identity matrix.

In fact, developing the relationships above allows to conclude that the only three-port network completely matched and lossless is the ideal circulator, but at the expense of reciprocity. Loosen the specifications by mismatching one port leads to an impossibility of signal flowing between the mismatched port and the other, hence useless. On the other hand, lossless combiners have a hardly predictable impact on nonlinearity of practical systems [113]. Some examples are either lossless "tee" networks or Chireix combiners employed at the output of the LINC transmitter. Since the present architecture targets a highly-linear solution, lossless combiners are discarded. A lossy combiner is here preferred as the best implementation candidate for the output combination of the quadrature-modulated signals.

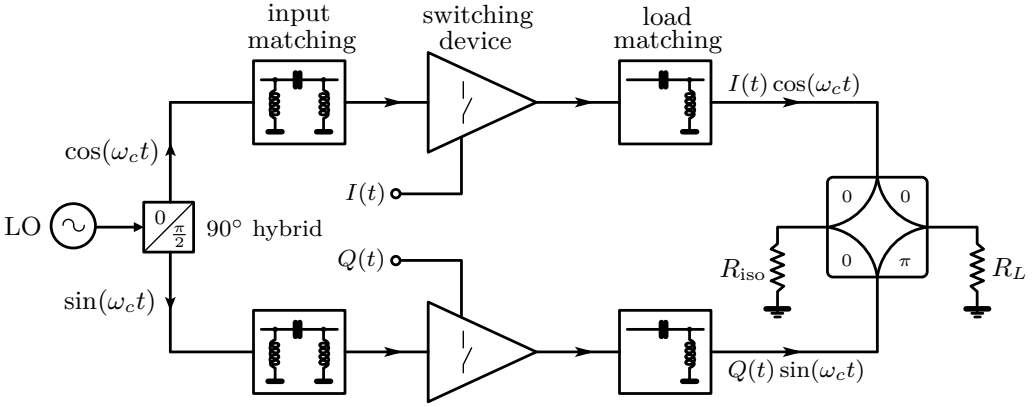


Figure 4.2: Proposed front-end for the C-P architecture (isolated).

Despite the transformer has been used so far, on an illustrative basis for signal combining (due to conceptual simplicity), it will not be considered as an actual implementation option for the proposed transmitter. Instead, for the present work, the proposed combiner consists of a four-port network, i.e. the π-hybrid combiner[1], which provides full isolation between the two inputs (under ideal circumstances) [146].

Fig. 4.2 shows the proposed front-end for the C-P transmitter with a π-hybrid combiner at the antenna interface. The quadrature-modulated signals drive the two inputs of the combiner and an isolating resistor R_{iso} is used at the dummy port ($R_{\text{iso}} = R_L$). As the carrier-modulated signals are obtained through switched-mode amplifiers, the high-frequency terms resultant from switching must be eliminated by the bandpass filters, previously to combination of the I and Q branches. It is worth noting that this represents a great difference from the LINC architecture. In the LINC, the precise cancellation of signal harmonics is demanded to build the RF signal at the output. Hence, in the LINC a large bandwidth is demanded at the combiner, whereas at the C-P the signals just require the original bandwidth. Moreover, the inexact cancellation decreases the efficiency of the LINC, since the non-transmitted power is wasted at the dummy load. In the case of a non-isolated output, out-of-band emission would occur.

[1]In theory, a π-hybrid combiner may also be treated as a transformer.

4.1 Output Combiner

In microwave circuits, the π-hybrid combiner is most commonly found in the form of rat-race structure [146]. It typically comprises an inner ring with $1.5\,\lambda$ length and $\sqrt{2}\,\mathrm{Z}_0$ characteristic impedance, with two outputs: a summing ($\sum$) and a difference port (Δ). The conventional circular structure is quite large, but it can be changed to significantly reduce its footprint. Some miniaturization techniques allow more than 70 % reduction [147], e.g. using folding sections [148], coupled-line sections [149], or using phase inverters to perform the complete phase shifting [150–152]. Typically, the isolation between inputs is about 20 dB, the return losses are less than 15 dB, and the coupling is in the order of 3 to 6 dB. In terms of bandwidth, more than 20 % can be easily achieved without compromising any other parameters in design [152, 153]. Another alternative to reduce the overall area of a π-hybrid combiner is the use of a lumped-element version [154]. For relatively low frequencies, due to inherent large areas required, such approach may be unavoidable. The components can be derived from the transmission-line model [130]. Each $\lambda/4$ section is replaced by a π low-pass equivalent circuit, whereas the high-pass T equivalent can replace the $3\lambda/4$ section. Fig 4.3 shows the resultant lumped-model circuit. The component values are determined by

$$L_1 = L_2 = L_3 = L_4 = \frac{\sqrt{2}}{\omega_c} Z_0 \tag{4.1}$$

$$C_1 = \tfrac{1}{2}C_2 = \tfrac{1}{2}C_3 = C_4 = \frac{1}{\sqrt{2}\,\omega_c Z_0} \tag{4.2}$$

where Z_0 is the characteristic impedance. Defining $Z_0 = 50\,\Omega$, the inductors are 11.25 nH/GHz and C_1 is about 2.25 pF/GHz. In both types of components, these values can be integrated on a chip in the GHz range. Another possible solution is the use of a transformer as a combiner. For an integrated circuit (IC) implementation, the design of such a device is not straightforward because neither is typically offered as an RF component

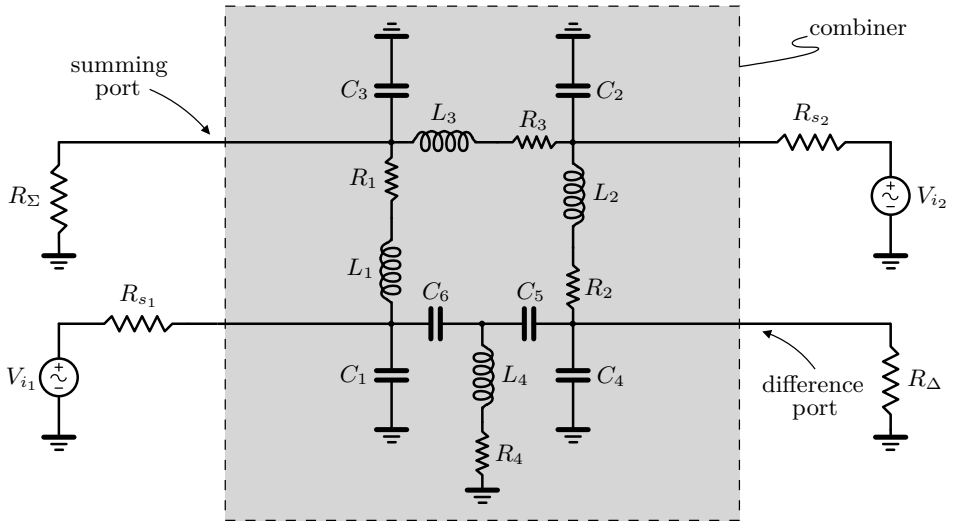


Figure 4.3: Lumped-model representation for the π-hybrid combiner.

by foundries, nor the IC design tools provide accurate means to extract and simulate its parameters. As for a transformer as a commercial off-the-shelf component, the available devices depend much on the frequency of operation [155], but should be easy to implement in the C-P design once properly modeled.

For the present study let us admit the lumped version of a matched-hybrid combiner. In Fig 4.3 each inductor has associated an equivalent series resistance (ESR). This is due to a finite unloaded quality factor (Q_u). On the other hand, in terms of parasitic capacitances, note that it can be practically absorbed into nearby capacitances (see Fig 4.3). Hence, to address the influence of other nonidealities in the combiner performance, let us just consider the finite Q_u of inductors. At least for integrated circuit technologies, such as CMOS, the value of Q_u is the greatest limitation at RF operation [156]. Fig. 4.4 shows parametric simulations performed with the same Q_u for each inductor. Since all the inductors have the same size, this implies their ESRs have the same value, $R_i = \omega L_i/Q_u, \forall i$. For this study, the series resistances have been varied according to Q_u. The inputs have the same magnitude and opposite phases in one case (power is maximized at the Δ port), and quadrature in another test. Moreover,

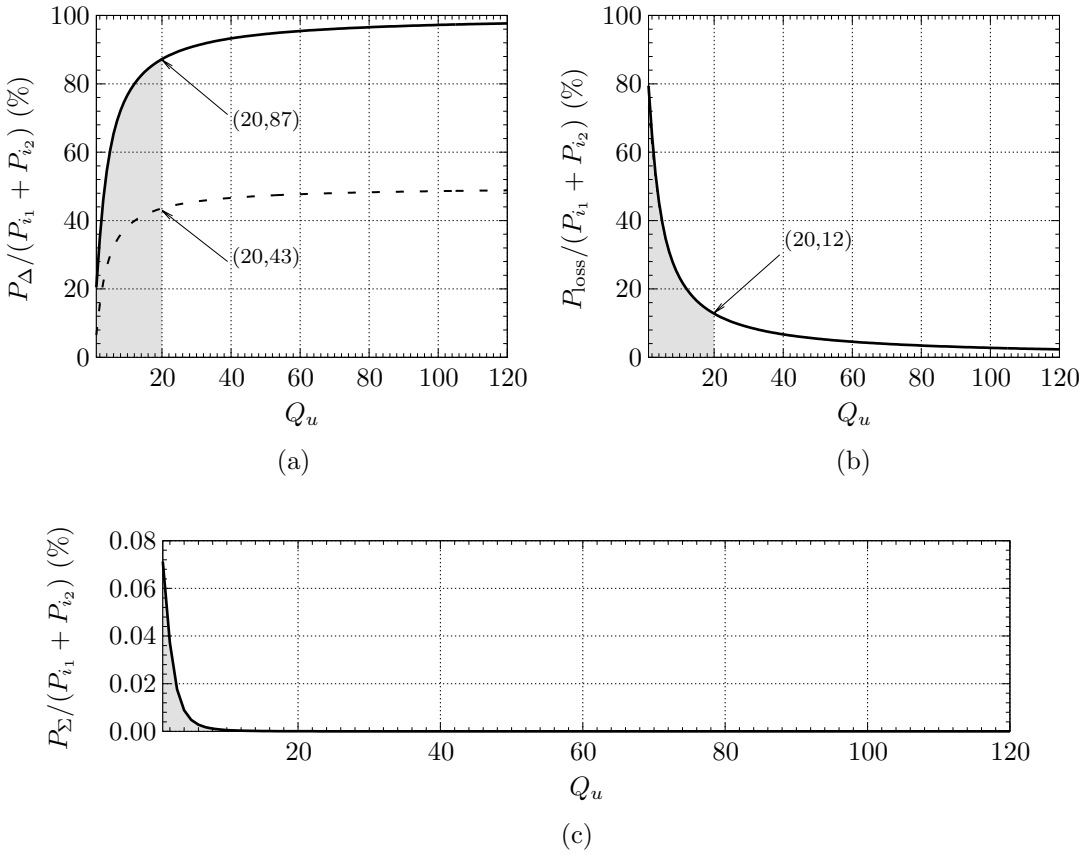


Figure 4.4: Efficiencies in a matched-hybrid combiner in terms of unloaded Q, assumed equal for all the inductors. The shaded areas represent $Q_u < 20$ (see text). The solid lines correspond to 180-degrees out-of-phase input, and dashed lines correspond to inputs in quadrature. In (b), where $P_{\text{loss}} = P_{i_1} + P_{i_2} - P_\Delta - P_\Sigma$. both lines overlap. In (c) the shaded line is not plotted as it coincides with its own representation in (a).

the inputs are properly matched, i.e. the source resistances are chosen as $R_{s_1} = R_{s_2} = 50\,\Omega$.

Fig. 4.4(a) shows the most important result, which is the efficiency on delivering the input power to the output load R_Δ, for in-phase and quadrature inputs. The shaded areas represent the range of values for typical quality factors of spiral inductors in silicon ICs. At the limit, $Q_u = 20$, which means the maximum efficiency is around 43% (for inputs in quadrature). If we consider discrete devices in surface-mount technology (SMT), the Q_u is typically maximized for frequencies $\sim 1\,\text{GHz}$, near the

GSM bands. One can generalize $Q_u > 40$ for film non-magnetic inductors. In these conditions, discrete solutions would have about 46% minimum efficiency, also for quadrature inputs, and should be preferred since its performance is less prone to Q_u variations.

Having addressed the transmitter front-end, the following step on the circuit design is the topology for the PA. Perfect isolation at the output and a constant R_L is assumed for both I and Q branches. For simplicity, in the next developments only one branch is considered, i.e. the in-phase branch that provides the output $I(t)\cos(\omega_c t)$.

4.2 Class-E Power Amplifier

Due to bipolar signal characteristics of baseband $I(t)$ or $Q(t)$, the proposed class-E PA must be able to accommodate a bipolar power-supply as the envelope modulator. This differs from conventional unipolar power-supply modulation in polar transmitters, where the envelope is obtained as $A(t) = \sqrt{I(t)^2 + Q(t)^2} \geq 0, \forall t$. Therefore, the proposed architecture requires bidirectional switches implemented as SMPAs. The bipolar-driven PA herein proposed is comprised of a switching device with its body connected to a negative voltage $-V_{\mathrm{B}}$. This allows the drain and source terminals to be interchanged along time. The circuit can be designed to meet typical class-E conditions, i.e. both zero-voltage switching (ZVS) and zero-voltage derivative switching (ZVDS) at turn-on time instant.

The topology for the class-E PA proposed is depicted in Fig. 4.5. The time varying power-supply is denoted as $A(t)$. As mentioned above, $A(t)$ is allowed to have both positive and negative voltages along time. Fig. 4.5 represents either the I or Q-channel stage, since an identical structure is assumed for both. Hence, $A(t)$ hereafter may represent $I(t)$ or $Q(t)$.

To meet class-E conditions, the component values can be determined as in classical class-E designs [157–162]. The shunt capacitance C_s can include

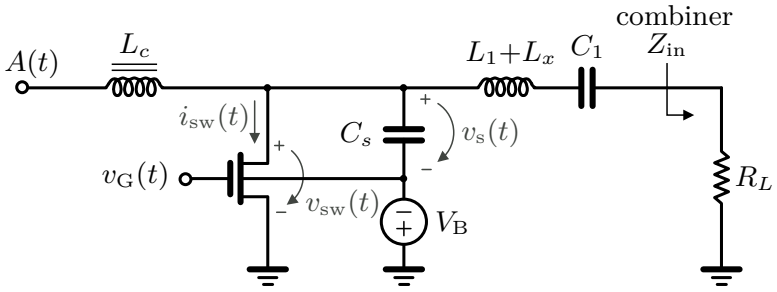


Figure 4.5: Class-E bipolar-driven PA.

the parasitic capacitance of the transistor, determined by

$$C_s = \frac{0.1836}{\omega_c R_L} \tag{4.3}$$

The inductor L_{c} is intended to act as an RF choke. It is designed to have its reactance much higher than the shunt capacitance C_s. A common practice is defining it ten times larger [162, 163]

$$L_c \geq \frac{10}{\omega_c^2 C_s} \tag{4.4}$$

The output load network is comprised by the LC tank, $L_1 + L_x$ and C_1, with $\omega_c^2 = 1/(L_1 C_1)$. The resonance is defined slightly deviated from ω_c. If one takes into consideration a finite Q_L, given by [158]

$$Q_L \triangleq \frac{\omega_c (L_1 + L_x)}{R_L} \tag{4.5}$$

then, the following relationship may be established [164]

$$C_1 \simeq \frac{1}{\omega_c R_L Q_L} \left(1 + \frac{1.11}{Q_L - 1.7879}\right) \tag{4.6}$$

A possible design guideline is as follows. First, the resistive load seen from the drain (R_L) is arbitrated, so that a predefined output power can be achieved. The load and output power at the fundamental frequency are related by [165]

$$P_{\text{out}} = \frac{2}{1 + \pi^2/4} \frac{V_{\text{dd}}^2}{R_L} \simeq \frac{1}{2R_L} (1.07 V_{\text{dd}})^2 \tag{4.7}$$

The Q_L must also be defined, targeting a given communication bandwidth and parameter insensitivity. Upon the definition of such parameters (R_L and Q_L), the remaining components can be determined using the relationships from (4.3) to (4.6).

In essence, the present configuration can be seen as a *bipolar polar transmitter*, since the MOSFET can source and sink current, from the power supply or to the ground, respectively. The polarity of $A(t)$ automatically establishes the current direction, therefore, it defines which terminals are the source and drain. In this topology, the bulk is tied to $-V_{\mathrm{B}}$ to prevent forward biasing of junction diodes. As such, it is important to ensure the condition $\max\{|v_{\mathrm{sw}}(t)|\} \leq V_{\mathrm{B}}$ at all time, where v_{sw} is the switch voltage as depicted in Fig. 4.5. Along the present work, $I(t)$ and $Q(t)$ are assumed to be signals with similar peak levels in their positive and negative counterparts, i.e. $\max\{A(t)\} = -\min\{A(t)\}$. Fig. 4.6 depicts the illustrative waveforms for the voltage and current at the switch of the proposed class-E PA, for different values of power supply (both positive and negative). The waveforms are almost symmetrical, which show the capability of the proposed class-E PA to act as a bipolar PA.

As the proposed SMPA operates in class E, the peak voltage at the switch can theoretically achieve $3.56 \cdot \max\{|A(t)|\}$. The bulk should be biased below this limit, or equivalently,

$$|A(t)| \leq 0.28 V_{\mathrm{B}} \tag{4.8}$$

The driving voltage should be large enough to turn on and off the transistor effectively. This must be ensured for both operation regimes $A(t) > 0$ and $A(t) < 0$. At first sight, turning on the NMOS transistor should be harder, since it requires the minimum driving $v^{\mathrm{on}}_{\mathrm{G,min}}(t) = v_{\mathrm{sw}}(t) + V_{\mathrm{th}}$, i.e. higher than v_{sw}. Note that $v^{\mathrm{on}}_{\mathrm{G,min}}(t)$ is entirely dependent on the time varying $A(t)$, but the C-P topology makes use of a data-independent signal at each driver. As a result, the driver amplitude must be fixed at the worst case, i.e. $V_{\mathrm{B}} + V_{\mathrm{th}}$. On the other hand, turning off the transistor faces the same

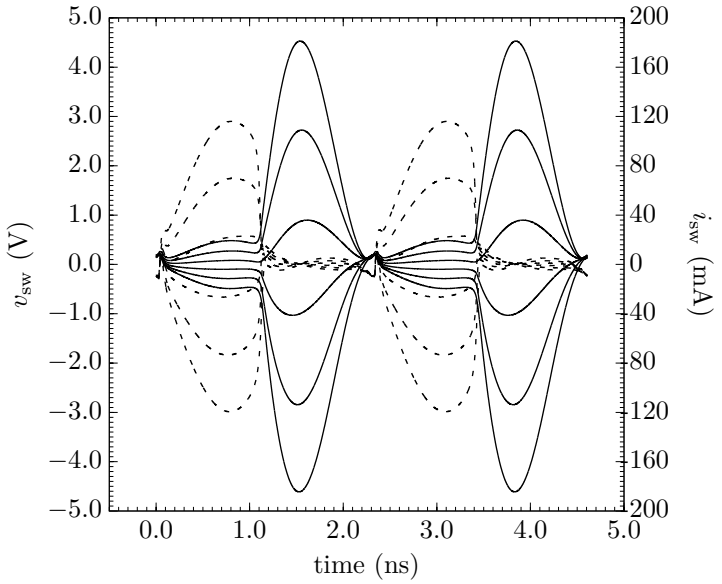


Figure 4.6: Voltage (solid lines) and current (dashed lines) waveforms at the switch for a bipolar class E for different supply voltages.

problem. If $v^{\text{off}}_{\text{G,max}}(t)$ does not differ by V_{th} from v_{sw}, the transistor operates in saturation. The minimum voltage at the gate should be $-V_{\text{B}} - V_{\text{th}}$ to impose cut-off. The driver limits $V_{\text{B}} \pm V_{\text{th}}$ are obtained for maximum excursion on v_{sw}. Generically, one can specify the driving signal limits by $\pm\max\{|v_{\text{sw}}(t)|\} \pm V_{\text{th}}$.

Both the gate drive and the envelope signals assume positive and negative values. The transistor acts as a bidirectional switch, that is, its terminals interchange along time depending on the envelope $A(t)$. Whenever the envelope signal is negative, the terminal tied to ground becomes the drain and current is drawn from the ground. Fig. 4.7 shows the I-V characteristic for a transistor array[2] with equivalent size W/L of $420\,\mu\text{m}/0.34\,\mu\text{m}$ and its body tied to $-4.5\,\text{V}$. The R_{on} is nearly the same for first and third quadrants, although the negative v_{sw} seems to offer higher current capability (this is addressed in the next section). Some asymmetric behavior can be tolerated since predistortion can be still applied to compensate these issues. In a general case, a first-order model of the switch (R_{on}) should

[2]This section has only explanatory purposes; process and design details will be given later.

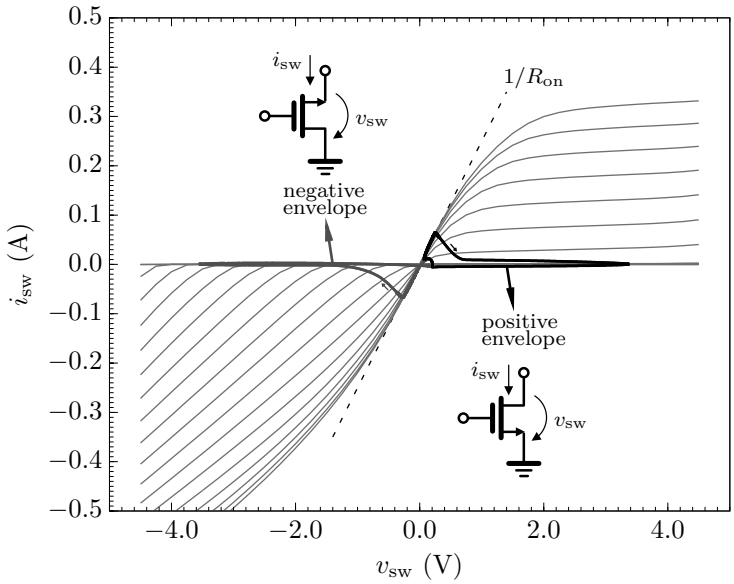


Figure 4.7: Illustrative load lines for the class-E PA with the bipolar current.

suffice for the study of a switching topology. But as the bi-directionality is not common for the switch current in PA topologies, the underlying causes for the assymetries must be well known first. Additional details are to be addressed along the analysis that follows, which is mostly focused on the performance for negative $v_{\rm sw}$. As such, next section includes several performance analyses, e.g. concerning relevant assymetries in the dc characteristic, capacitance, input matching, efficiency among other issues.

4.3 Topology Analysis

4.3.1 Asymmetric current-voltage characteristic

The equal-valued conduction resistance for both polarities is not an obvious result. As we are dealing with sub-micron devices, a short-channel model is much more accurate for the analysis of switch behavior, instead of the usage of long-channel equations with the classical quadratic model [166]. The short-channel MOSFET approach allows for the inclusion of velocity saturation, which is relevant for proper definition of the triode region. Thus,

considering the same nomenclature used in Fig. 4.5 regarding i_{sw} and v_{sw}, let us assume the short-channel model based on Appendix A, such as given by (A.7). When v_{sw} is positive, and $v_{\mathrm{sw}} > v_{\mathrm{G}} - V_{\mathrm{th}}$, the current i_{sw} depicted in Fig. 4.5 is given by

$$i_{\mathrm{sw}} = \begin{cases} K[v_{\mathrm{G}} - V_{\mathrm{th}} - \frac{1}{2}v_{\mathrm{sw}}][v_{\mathrm{sw}}||E_c L][1 + \lambda v_{\mathrm{sw}}], & \text{for } v_{\mathrm{sw}} < v_{\mathrm{sat}}^{+} \quad (4.9\mathrm{a}) \\ \frac{1}{2}K[v_{\mathrm{G}} - V_{\mathrm{th}}][(v_{\mathrm{G}} - V_{\mathrm{th}})||E_c L][1 + \lambda v_{\mathrm{sw}}], & \text{for } v_{\mathrm{sw}} \geq v_{\mathrm{sat}}^{+} \quad (4.9\mathrm{b}) \end{cases}$$

where $v_{\mathrm{sat}}^{+} = (v_{\mathrm{G}} - V_{\mathrm{th}})||LE_c$, with λ as channel-length modulation, K the intrinsic transconductance, and E_c the critical electric field. The weak-inversion region is herein neglected; due to relatively small currents it is considered as cut off ($i_{\mathrm{sw}} = 0$).

In the opposite case, that is for negative v_{sw}, the source terminal of the transistor becomes connected to the node v_{sw}. As a result, the on resistance becomes modulated by the envelope signal. The current for which $v_{\mathrm{sw}} < 0$ and $v_{\mathrm{G}} - v_{\mathrm{sw}} > V_{\mathrm{th}}$ is given by

$$i_{\mathrm{sw}} = \begin{cases} -K[v_{\mathrm{G}} - V_{\mathrm{th}} - \frac{1}{2}v_{\mathrm{sw}}][-v_{\mathrm{sw}}||E_c L][1 - \lambda v_{\mathrm{sw}}], & \text{for } v_{\mathrm{sw}} > v_{\mathrm{sat}}^{-} \, (4.10\mathrm{a}) \\ -\frac{1}{2}K[v_{\mathrm{G}} - v_{\mathrm{sw}} - V_{\mathrm{th}}][(v_{\mathrm{G}} - v_{\mathrm{sw}} - V_{\mathrm{th}}) & \\ \qquad\qquad ||E_c L][1 - \lambda v_{\mathrm{sw}}], & \text{for } v_{\mathrm{sw}} \leq v_{\mathrm{sat}}^{-} (4.10\mathrm{b}) \end{cases}$$

and null current is assumed for the remaining cases, when $v_{\mathrm{G}} - v_{\mathrm{sw}} \leq V_{\mathrm{th}}$. The negative saturation voltage is given by $v_{\mathrm{sat}}^{-} = -(v_{\mathrm{G}} - v_{\mathrm{sw}} - V_{\mathrm{th}})||LE_c$.

Let us consider the triode regime of the transistor, i.e admitting large gate voltage. Let us also admit the simplification $v_{\mathrm{sw}} \ll 1/\lambda$, which is a reasonable approximation since the influence of Early voltage is much more evident when there is a large potential between drain and source terminals. Differentiating both (4.9a) and (4.10a) in respect to v_{sw}, for constant v_{G}, one obtains

$$\frac{\partial i_{\mathrm{sw\ (4.9a),(4.10a)}}}{\partial v_{\mathrm{sw}}} = KE_c L \frac{(v_{\mathrm{G}} - v_{\mathrm{sw}} - V_{\mathrm{th}})E_c L \mp \frac{1}{2}v_{\mathrm{sw}}^2}{(E_c L \pm v_{\mathrm{sw}})^2} \qquad (4.11)$$

For small v_{sw}, (4.11) results in equal values for $1/R_{\mathrm{on}}$ regarding (4.9a) and (4.10a), i.e. $v_{\mathrm{sat}}^{-} < v_{\mathrm{sw}} < v_{\mathrm{sat}}^{+}$. Close to the I-V origin, (4.11) leads to

$K(v_{\mathrm{G}} - V_{\mathrm{th}})$, thereby coincident with the ON conductance in the case of a long-channel model.

Despite the similar behavior along with the triode region for both polarities, the regions $v_{\mathrm{sw}} \leq v_{\mathrm{sat}}^{-}$ and $v_{\mathrm{sw}} \geq v_{\mathrm{sat}}^{+}$ differ considerably. For a non-ideal MOSFET device, the load lines include such regions, even though transitionally, from triode into cut-off. This is because the finite R_{on} imposes a non-null voltage across the switch, which comes as the initial voltage when the transistor turns off. Conversely, from cut-off into triode, there is the class-E principle of discharging the shunt capacitance, so the transition into the regions $v_{\mathrm{sw}} \leq v_{\mathrm{sat}}^{-}$ and $v_{\mathrm{sw}} \geq v_{\mathrm{sat}}^{+}$ are not such noticeable. Nonetheless, referring to the triode/cut-off transition, the evident I-V discrepancies in Fig. 4.7 impose the load-line differences. For positive v_{sw} the strong inversion leads to a current source behavior, whereas for negative v_{sw} the I-V lines are no longer parallel to the v_{sw} axis, which means the current source behavior is highly affected by a very reduced output resistance. Such higher conductance can effectively unbalance both efficiency and output power if a weak drive is applied.

In fact, in the $v_{\mathrm{sw}} < 0$ side, triode and strong inversion are almost indistinguishably, at least visually in an I-V representation. This can be demonstrated using (4.10a–4.10b) and the respective slopes. Differentiating (4.10b) results

$$\frac{\partial i_{\mathrm{sw}}}{\partial v_{\mathrm{sw}}} = \tfrac{1}{2} K E_c L \left(1 - \frac{E_c^2 L^2}{(E_c L + v_{\mathrm{G}} - v_{\mathrm{sw}} - V_{\mathrm{th}})^2}\right) \tag{4.12}$$

When v_{sw} gets more negative, the approximation $v_{\mathrm{sw}} \ll -(v_{\mathrm{G}} - V_{\mathrm{th}})$ can be applied to conclude

$$\frac{\partial i_{\mathrm{sw}}}{\partial v_{\mathrm{sw}}} \simeq \tfrac{1}{2} v_{\mathrm{sw}} K E_c L \frac{v_{\mathrm{sw}} - 2E_c L}{(E_c L - v_{\mathrm{sw}})^2} \tag{4.13}$$

With the same approximation in (4.11) for $v_{\mathrm{sw}} > v_{\mathrm{sat}}^{-}$ one gets the same result. The expression $\frac{1}{2} K E_c L$ may be seen as an asymptote ($v_{\mathrm{sw}} \to -\infty$) for the output resistance. It reflects its weak dependence on v_{G} and v_{sw}, when $v_{\mathrm{sw}} < v_{\mathrm{sat}}^{-}$.

4.3.2 Body effect

The way the bulk is electrically connected denotes a peculiarity of the present topology. As the source terminal changes along time, it cannot be short-circuited to bulk. Hence, the non-null value of source-bulk potential affects the MOSFET threshold voltage (V_{th}).

This bulk (or body) effect is directly reflected into gate driving demands. That is, if somehow V_{th} presents some relationship with the envelope voltage, the driving signal v_{G} has to follow exactly the same dependence if the same switching conditions are to be established (i.e. to keep $v_{\mathrm{G}} - V_{\mathrm{th}}$ constant). However, in the present topology the gate driving has fixed amplitude and frequency. If the drive level is sufficient higher/lower than V_{th}, the on/off regimes can be attained with less sensitivity of V_{th}. Still, the impact of v_{sw} on V_{th} should be properly addressed, so that V_{th} asymmetries can be understood and identified.

When $v_{\mathrm{sw}} > 0$, the source terminal is fixed at a null voltage. Hence, the source-bulk potential remains fixed at $-V_{\mathrm{B}}$. The V_{th} is increased above V_{th0}, although the short-channel effects due to v_{sw} tend to counteract such behavior. The threshold voltage can be approximated by

$$V_{\mathrm{th}} = V_{\mathrm{th0}} + \gamma \left[\sqrt{V_{\mathrm{B}} - 2\phi_{\mathrm{F}}} - \sqrt{|2\phi_{\mathrm{F}}|} \right] - \eta(v_{\mathrm{sw}}, V_{\mathrm{B}}, L), \quad v_{\mathrm{sw}} > 0 \quad (4.14)$$

In the relationship above, ϕ_{F} represents the Fermi potential, γ the body-effect parameter, and V_{th0} the threshold voltage when source and bulk are tied together. Although not dominated by drain induced barrier lowering (DIBL), the threshold voltage in short-channel devices is affected by this phenomena [167]. In (4.14), η is the DIBL factor, being determined by the device dimensions, drain-source and source-bulk potentials [168]. These parameters are respectively affected by η_L, η_a and η_b as given below

$$\eta(v_{\mathrm{sw}}, V_{\mathrm{B}}, L) = [\, \eta_a - \eta_b V_{\mathrm{B}} \,]\, v_{\mathrm{sw}} + \eta_L \quad (4.15)$$

The function η determines the only influence of v_{sw} in V_{th}. If the DIBL effect is neglected, then V_{th} is constant and easily compensated by increasing the potential v_{G} by the same amount. Unfortunately, that is not the case. In the interval $0 < v_{\mathrm{sw}} < \max\{v_{\mathrm{sw}}\}$, V_{th} is significantly higher than V_{th0}. However, it is less sensitive to v_{sw} than in $v_{\mathrm{sw}} < 0$. This can be verified in Fig. 4.8, which compares the relationships derived herein with Cadence Spectre simulations using the BSIM model of a large thick-gate NMOS device. When v_{sw} turns negative, it directly imposes the potential source-bulk potential. In this case, the threshold voltage is given by

$$V_{\mathrm{th}} = V_{\mathrm{th0}} + \gamma \left[\sqrt{v_{\mathrm{sw}} - v_{\mathrm{B}} - 2\phi_{\mathrm{F}}} - \sqrt{|2\phi_{\mathrm{F}}|} \right] + \left[\eta_a - \eta_b (V_{\mathrm{B}} + v_{\mathrm{sw}}) \right] v_{\mathrm{sw}} - \eta_L, \quad v_{\mathrm{sw}} < 0 \tag{4.16}$$

Regarding the I-V characteristic, previous results (4.11)–(4.13) did not included the dependence of V_{th} on v_{sw}, since it shows no impact on the I-V slope. Nevertheless, this dependence has to be considered to fully characterize the dynamic behavior of the PA. The switching point is affected by V_{th} and the gate bias has to be properly chosen to minimize its influence. Another parameter to be studied in the switching context is the parasitic junction capacitances.

4.3.3 Parasitic capacitances

As the envelope varies, the potential at the reverse-biased junction of the drain (or source) changes accordingly. The *pn*-junction capacitance follows a nonlinear behavior with v_{sw}, which is defined as [169, 170]

$$C_j(v_{\mathrm{sw}}) = C_{j_0} \left(1 + \frac{v_{\mathrm{sw}} - v_{\mathrm{B}}}{V_{\mathrm{bi}}} \right)^{-m_j} \tag{4.17}$$

where m_j is the grading coefficient, V_{bi} is the built-in potential, and C_{j_0} is the bottom-plate capacitance when v_{sw} has the same potential as the bulk.

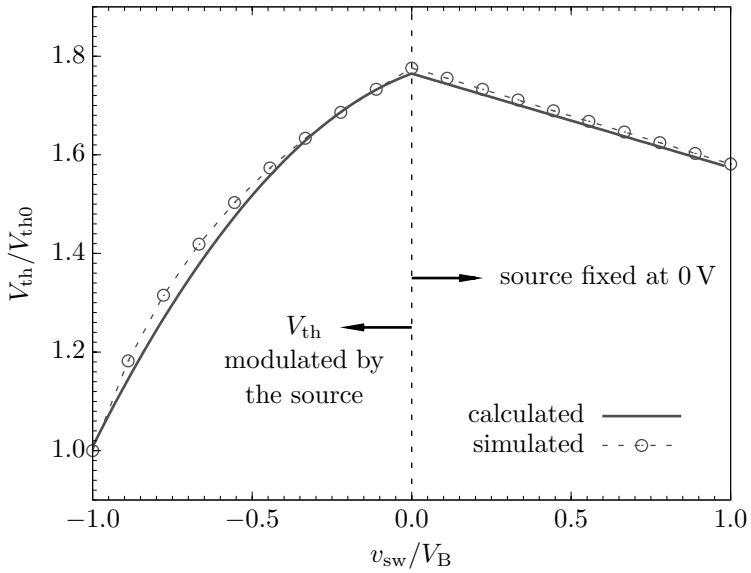


Figure 4.8: Asymmetries in threshold voltage.

Most literature presents $m_j = 0.5$ to characterize a gradual junction and less for abrupt junctions, which is often the case (around 0.33).

Fig. 4.9 shows the junction capacitance normalized to C_{j0}, with $V_{\rm bi}$ about 0.7 V and the bulk biased at -4.5 V. The result is compared with

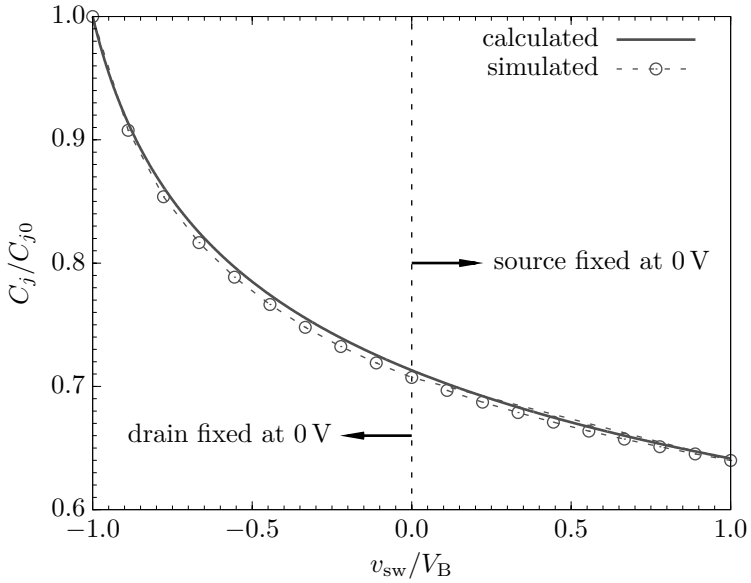


Figure 4.9: Normalized junction capacitance due to the switch voltage.

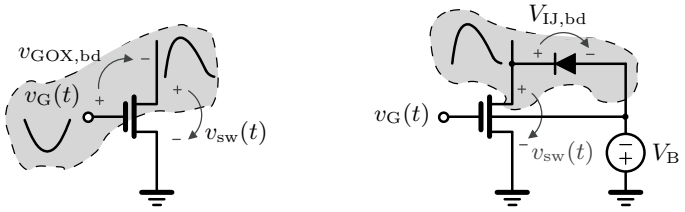
a Spectre simulation for a BSIM-modeled transistor, which agrees for the whole range of v_{sw}. The value of C_j can vary significantly for negative envelope values. Along the normalized v_{sw} axis, the asymmetric behavior is quite noticeable. One should however refer that the results from simulation in Fig. 4.9 are in fact due to several capacitances, such those referring to sidewall and drain area capacitances. Nonetheless, as shown, those can be approximated by a single expression as in (4.17).

For the channel-bulk capacitance, more specifically at the drain region for $v_{\mathrm{sw}} > 0$, and source when $v_{\mathrm{sw}} > 0$, the transistor is assumed to be in triode. This way a constant charge distribution can be assumed for the channel for any v_{sw}. Simulation results with BSIM3v3 modeling have demonstrated the validity of the assumption, ensuring at all time v_{G} slightly above $v_{\mathrm{sw}} + V_{\mathrm{th0}}$. As for the feedback capacitance C_{gd}, its contribution for the nonlinear performance can be approximated to a loading effect at the drain. This can be seen as given in [171], adapted to the present topology, i.e. $C_{\mathrm{gd}} + C_{\mathrm{gd}}\, v_{\mathrm{GS,max}}/v_{\mathrm{sw,max}}$. Nevertheless, the loading effect at the drain/source terminals is dominated by *pn*-junction capacitance C_j.

4.3.4 Reliability issues

The maximum value for $i_{\mathrm{sw}}(t)$ is dictated by the operation temperature and electromigration rules, which impose the minimum channel width of the transistor, contact and via dimensions, and metal trace widths. For the present case, as the transistor is switched on and off alternately, the maximum current per device finger is reduced by about π, compared to more restrictive dc design rules.

On the other hand, the typical high-voltage stresses in SMPAs impose reliability concerns. This is particularly severe for CMOS technologies, which typically have reduced breakdown voltages [172]. At radio frequencies, the device degradation can be due to hot carriers (HC) and gate



(a) (b)

Figure 4.10: Illustrative schematic on most susceptible types of breakdown in the proposed CMOS PA – (a) oxide and (b) junction breakdown.

oxide breakdown (BD) [173–176]. For the typical class-E, the peak voltage at the drain occurs with the transistor while in cut-off. As long as current and voltage overlap is minimized, hot-carrier stress is minimized. Due to elevated potential across gate-drain overlapping, Fowler-Nordheim (F-N) injection is much likely to occur in a class-E PA [177].

As safety voltage to prevent the oxide BD, twice the nominal supply is recommended as the maximum voltage between the device terminals ($V_{\mathrm{GOX,bd}}$) [164]. This considers the electrical field critical at 10 V/Å [164]. However, this is not widely consensual. Other works suggest less conservative limits [178]. Even assuming partly defective oxides (as high as $\sim 30\,\%$), about 50 to 60 V/Å is estimated for time-dependent dielectric breakdown (TDDB) extrapolated to 20 years operation [179]. TDDB is based on quasi-static experiments, thereby distinct from the cyclic stress at RF. F-N stress has been demonstrated to be overrated if considering wear-out limits based on quasi-static analysis [180]. Recently, tolerable operation has been demonstrated experimentally at 20 V/Å gate oxide field [181], without any noticeable impact in the class-E performance. In the present CMOS process, thick-oxide devices are used, having oxide breakdown of $V_{\mathrm{GOX,bd}} = 9.1\,\mathrm{V}$ and 70 Å gate thickness. Based on the last reference, about 14 V would be allowed between gate and switch terminals.

Another reliability limitation is due to the *pn*-junction diodes between drain/bulk and source/bulk. For the current CMOS process, the reverse voltage breakdown for the junction ($V_{\mathrm{J,bd}}$) is around 9 V. Therefore, high-

voltage stress at the drain side can induce this kind of breakdown prior to oxide damage. As the bulk is to be negatively biased, special care should be taken when choosing V_{B}. For the proposed design, half the minimum breakdown voltage is adopted, hence $V_{\mathrm{B}} = 4.5\,\mathrm{V}$. The most aggressive conditions occur when v_{sw} is high, maximum at $v_{\mathrm{sw}} = V_{\mathrm{B}}$, when $2V_{\mathrm{B}} = V_{\mathrm{IJ,bd}}$.

4.3.5 Maximum-power and efficiency dependence

Since the efficiency of the PA represents a key role in the transmitter performance, it is worth studying in detail. Let us start with a simplified analysis, by considering R_{on} as the unique degradation source in efficiency. Additionally, let us admit its finite value does not change significantly the wave shape of switch current during the activated state. Under such conditions, the drain efficiency on a class E can be approximated as in [182],

$$\eta\,(r, g) \simeq \frac{1}{1 + \frac{g^2+6}{2g^2} \cdot r} \tag{4.18}$$

where $r = R_{\mathrm{on}}/R_L$, which equals to $\eta\,(r) \simeq 1/(1 + 1.365 \cdot r)$. In this result, the parameter g has been used as defined in [157], with the value of 1.862, which corresponds to a 50 % duty ratio. Fig. 4.11 depicts the drain efficiency with (4.18) and simulation results. To force the required duty-cycle, a square waveform was applied at the gate. For the CMOS process used in this work, the estimated R_{on} is in the order of $1.7\,\Omega \cdot \mathrm{mm}$. The value of R_{on} has been changed by modifying the gate dimensions of the active device (widths shown in Fig. 4.11), keeping the minimum length. As previously mentioned, the conduction resistance is almost the same for positive and negative supply operation, as long as the gate driving is high. But it is important to point out that when R_{on} is decreased, the conventional design expressions cannot be assured anymore, and the shunt capacitance and also the load network have to be slightly re-tuned to attain class-E conditions. The adjustments are solely in the order of 5 % in the

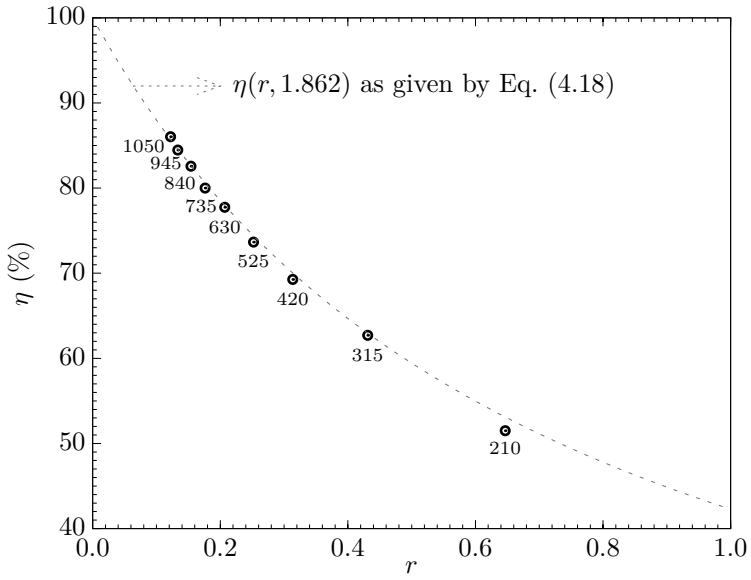


Figure 4.11: Drain efficiency versus device on resistance in the C-P transmitter (transistor widths shown in μm).

load inductance (choke with 10 times the ideal reactance of C_s) for a Q_L of 10, and C_s adjustments up to 25 %. The resultant drain efficiency is slightly reduced when compared to the approximation in (4.18). In this analysis, all the inductors are considered ideal.

As some power is dissipated in R_{on}, the peak voltage at the switch is lower than the ideal 3.56 times the power supply. Considering that the current and voltage shapes do not suffer significant changes, the average output power can be written as

$$P_{\text{out}} = \frac{g^2 R_L}{2R_{\text{dc}}^2} V_{\text{eff}}^2 \tag{4.19}$$

$$= \frac{2}{g^2 R_L} [\eta(r) V_{\text{dd}}]^2 \tag{4.20}$$

with $R_{\text{dc}} = g^2 R_L/2$ and $V_{\text{eff}} = \eta(r) V_{\text{dd}}$ [182]. Fig. 4.12 shows the normalized output power for different power-supply values kept constant, varying R_{on}/R_L. As the output power is limited by the peak voltage at the switch (always less than V_{B}), the maximum V_{dd} should be also estimated. From ideal class-E waveforms, the voltage across the active device can be de-

scribed as in [165] by

$$v_{\mathrm{sw}}(\theta) \simeq 2.9250\,\theta\,V_o + 5.4466 V_o \cos(\theta - 0.1804\pi) - 4.5945 V_o \qquad (4.21)$$

for which the peak is achieved at $\theta_{\mathrm{pk}} \simeq 0.36\pi$, i.e. $V_{\mathrm{peak}} \simeq 1.055\pi V_o$, where V_o is the voltage at the output. It is difficult to predict the waveform $v_{\mathrm{sw}}(\theta)$ for efficiency values other than 100 %. As such, let us proceed with such assumption. Writing V_o in terms of output power, $V_o = \sqrt{2R_L P_{\mathrm{out}}}$, and using (4.20) results in $V_o = 2V_{\mathrm{dd}}/g$, allows us to derive the peak voltage in terms of efficiency as $V_{\mathrm{peak}}/V_{\mathrm{dd}} = 2.11\pi/g$. As the dc voltage at the switch is imposed by the choke, this last relation must be decomposed as

$$V_{\mathrm{peak}} = V_{\mathrm{dd}} + V_{\mathrm{dd}}(2.11\pi/g - 1) \qquad (4.22)$$

The reason why (4.22) is written with V_{dd} set apart is that now we can affect the remainder part by $\eta(r)$. The resultant maximum V_{dd} is then

$$V_{\mathrm{dd,max}} = \frac{V_{\mathrm{peak}}}{a + 2.56 \cdot b \cdot \eta(r)} \qquad (4.23)$$

coinciding with the result in the works [182–184] when $a = b = 1$. As the unitary value for a and b results in rough approximations for less ideal conditions, such factors are proposed as fitting parameters determined empirically. Simulation data shows that accurate results in the range of 50 to 85 % should use $a \simeq 1.4$ and $b \simeq 0.9$. Eq. (4.23) provides useful guidance for the envelope modulator design, which for instance admiting $\eta \simeq 0.60$ should accomodate at maximum $V_{\mathrm{dd}}/V_{\mathrm{B}} \simeq 0.36$. The maximum power is derived using $V_{\mathrm{peak}} = V_{\mathrm{B}}$, which yields

$$P_{\mathrm{out,max}} \simeq \frac{0.55}{R_L}\left[\frac{V_{\mathrm{B}}}{g} \cdot \frac{1}{r + 1.95}\right]^2 \qquad (4.24)$$

In Fig. 4.12, the solid line labeled $P_{\mathrm{out,max}}$ represents (4.24). Each data point represented as a symbol "□" was obtained choosing a different V_{dd}. The chosen value allowed to achieve a peak at V_{B} in the voltage waveform.

In the present analysis, only positive values for V_{dd} were illustratively applied. Its validity is extended to negative regimes provided that R_{on}

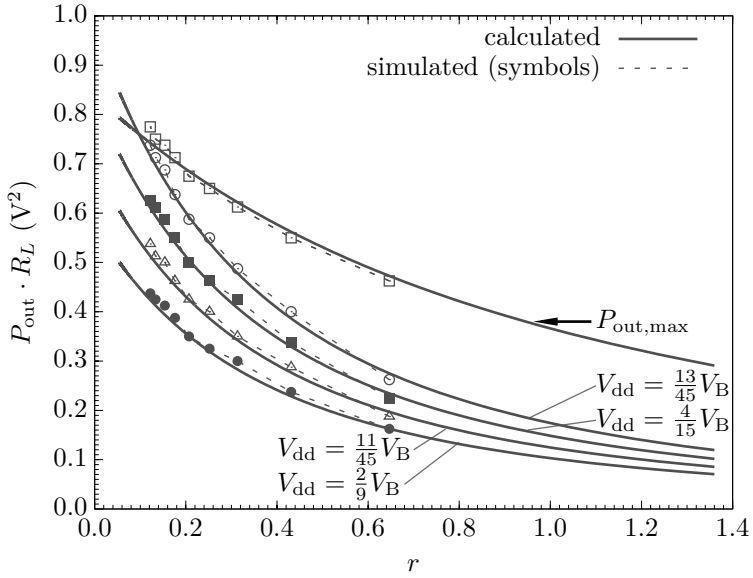


Figure 4.12: Output power for different power-supply values and estimated limits.

should be kept unchanged. Nonetheless, second-order effects may exist due to the nature of signals applied at the gate, with some impact on the drain efficiency. In the present analysis, only square waveforms were considered for the driver. The next section will provide additional insights regarding more realistic driving signals.

4.3.6 Gate driving

To impose the ideal class-E conditions, the active device is considered either closed or opened, switching almost instantaneously between these states. To acquire such behavior, the gate voltage should be a square wave to attain half duty-ratio and maximum power capability. If a class-D amplifier is chosen as a gate driver for the class-E PA, the power needed for driving is about $fC_{\text{NMOS}}V_{\text{dd}}^2/2$ [37], with C_{NMOS} as the PA input capacitance and the operating frequency f_c. This last parameter reveals a reasonable impact on efficiency and may even turn unfeasible a class-D driving. Also due to bandwidth limitations, a sine or saturated sine waveform can be applied within the same purpose (around the V_{th} of the transistor). For

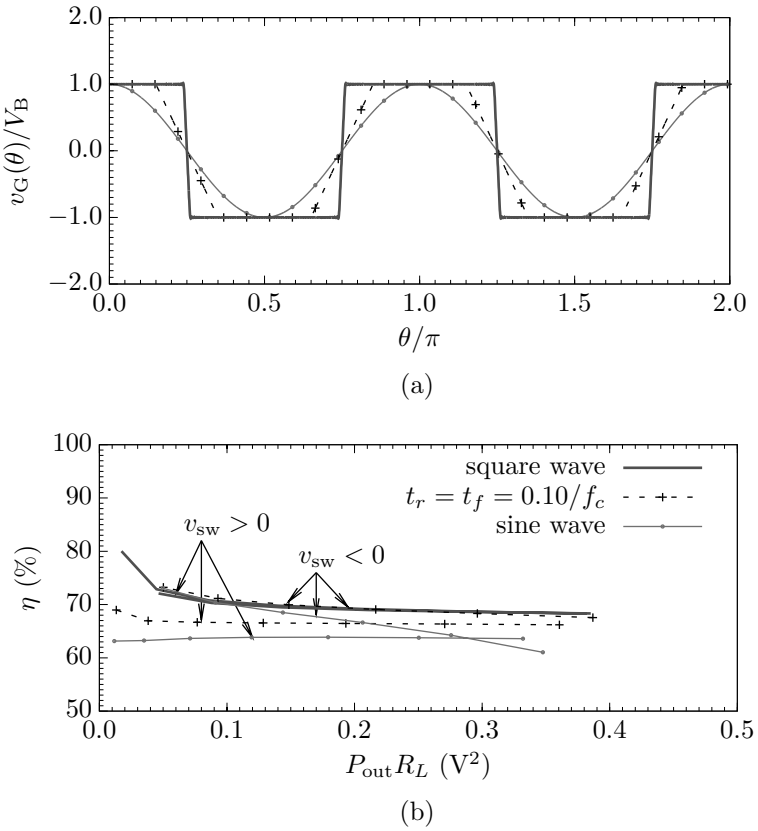


Figure 4.13: Impact of gate signal on efficiency in terms of output power. (a) Driving waveforms, and (b) efficiency versus output power.

a conventional class-E PA, the impact in performance is not drastic as long as the transitions between on and off states have a reasonable slope. In that case, a common practice is sweep the input power to establish the driving amplitude, which basically works as PAE optimization.

In the present C-P proposal, if any signal different from a square waveform is applied at the gate, the I-V asymmetric behavior is slightly emphasized. The finite rise/fall times of the square signal have a noticeable impact because of the V_{th} dependence on v_{sw}. To have a better insight on this, let us assume three separated cases: the gate terminal driven by an ideal square waveform, a pulsed waveform with finite rise/fall times (in the order of 20 %), and a sinusoidal signal. All the signals have the same peak values, as depicted in Fig. 4.13(a). Simulations using Agilent ADS were

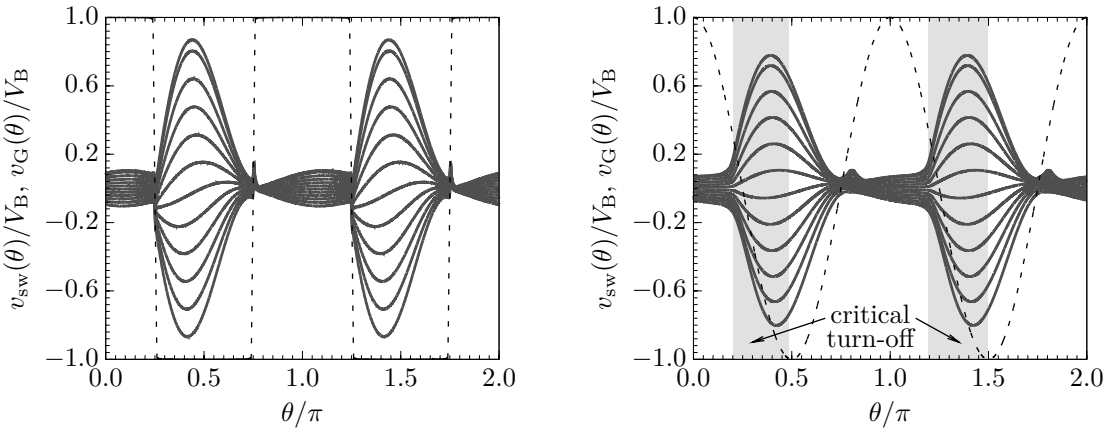


Figure 4.14: Voltage waveforms at the switch for (a) square wave and (b) sinusoidal driving.

performed sweeping the power supply for several V_{dd} values, negative and positive, with the gate signals depicted in Fig. 4.13(a). It turns out that an efficiency asymmetry results from different gate driving signals. For the ideal driving with the square wave, the efficiency is almost the same from negative, up to positive v_{sw}. This is depicted in Fig. 4.13 as two solid lines practically superimposed, above 70 % in drain efficiency. With a finite transition between states at the gate, the efficiency for positive v_{sw} remains nearly the same as the ideal case. As illustrated, the efficiency for $v_{sw} < 0$ lowers, despite being relatively constant along P_{out}. When a sine waveform is applied, the assymetries become remarkable. For $v_{sw} > 0$ the efficiency reduces, but it does not loose its flatness. As P_{out} increases in the $v_{sw} < 0$ counterpart, the efficiency is dramatically reduced to values below those in the $v_{sw} > 0$ range.

The main difficulty in sine waveform excitation is the device cut-off. Since $v_G(\theta)$ is fixed in amplitude and $v_{sw}(\theta)$ is not, when $v_{sw}(\theta) \ll 0$ and close to the gate peak voltage, the duty ratio is increased. The value of V_{th} gets lowered when v_{sw} is too negative and the transistor is activated earlier. The transistor has a longer time operation in transconductance mode. As a result, the power dissipated within this operating region de-

creases the PA efficiency. Fig. 4.14 illustrates a comparison between two driving approaches. At any time, the gate voltage in Fig 4.14(a) is either well above $v_{\rm sw}(\theta)+V_{\rm th}$ (defining the on state), or below $V_{\rm th}-v_{\rm sw}(\theta)$. As for gate driving with a sine waveform, this is not always the case. Activating the device is easier than turning it off.

The shaded area in Fig. 4.14(b) represents operating regions wherein potentially the device will act as a voltage-controlled current source. To cut-off when $V_{\rm dd} > 0$, the gate voltage is only required to be fairly below $V_{\rm th}$ (relatively high for $v_{\rm sw} > 0$). But for negative values in the power-supply, the required gate voltage to cut-off the MOSFET is $v_{\rm sw}(\theta) + V_{\rm th}$, or less. If the PA is subject to work at its full power range, up to its power limits, cutting off the device is only possible during some time, depending on the negative power-supply levels. Nonetheless, building a driver for sine waveform excitation is significantly easier than flattening a sine waveform. This motivates a straightforward application, which will be addressed in the present work.

4.3.7 Input impedance

It has been seen that, depending on the drain supply of the transistor, the resistance seen into $C_{\rm gd}$ can assume negative values [185]. In most cases, the positive gate resistance compensates this effect, but such compensation is sensitive to gate-drain voltage ratios. As a consequence, the design of a proper input matching network may definitely be a challenge. To get a clearer idea on how such a phenomenon has its implications, let us admit the drain voltage given as (4.21) and its respective gate driving here assumed as a sinusoidal waveform. In practical realizations, the most common form of driving is $v_{\rm DRV}(t) = V_{\rm th} - V_{\rm dd,DRV}\sin(\omega t)$, as shown in Fig. 4.15. When the transistor is closed, if $R_{\rm on}$ is reasonably low, the feedback current is sinusoidal due to the gate driving signal. When the switch is in the off

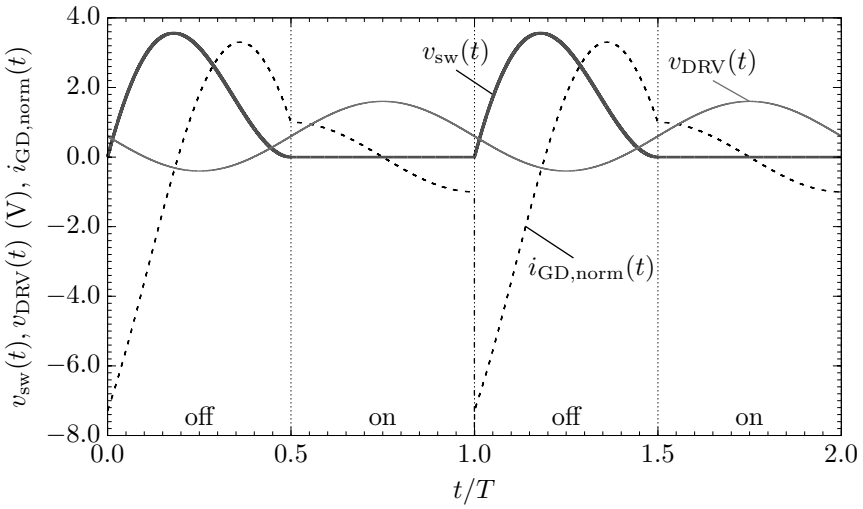


Figure 4.15: Drain signal, gate driving and current through $C_{\rm gd}$ in a class-E PA.

state, the resultant waveform is much more complex

$$\frac{i_{\rm GD,off}}{\omega\, C_{\rm gd} V_{\rm dd,DRV}} \simeq 5.85\,\zeta \sin(\omega t - 0.1804\pi) - \pi\,\zeta - \cos(\omega t) \tag{4.25}$$

where ζ is the ratio between power-supplies of the PA and driver, i.e. $\zeta = V_{\rm dd,PA}/V_{\rm dd,DRV}$. Fig. 4.15 shows the normalized gate-drain current, $i_{\rm GD,norm} = i_{\rm GD}/(\omega\, C_{\rm gd} V_{\rm dd,DRV})$. An unitary ζ was considered for the illustration purposes. In the representation, a noticeable discontinuity occurs in the waveform of the feedback current when turning off the transistor. Naturally, in an actual implementation this behavior should be smoothed, due to inevitable bandwidth limitations.

Due to the Miller effect, it follows that the impedance seen into $C_{\rm gd}$, herein denoted as $Z_{\rm fb}$, is influenced by the power supply of driver and PA stages, owing to

$$R_{\rm in,fb} = \text{real}\left\{ \frac{j V_{\rm dd,DRV}}{\frac{2}{T}\int_T i_{\rm GD}(t)[\cos(\omega t) - j\sin(\omega t)]\,{\rm d}t} \right\} \tag{4.26}$$

$$\simeq -\frac{1}{\omega C_{\rm gd}} \cdot \frac{0.4675\,\zeta}{1 + \pi\,\zeta + 2.6844\,\zeta^2} \tag{4.27}$$

For the C-P transmitter, one should reinforce that a minimum gate voltage is required to effectively turn off the transistor in the whole range

of the envelope. This minimum value is ideally $-3.56V_{\mathrm{dd,PA}} - V_{\mathrm{th}}$. Hence, in the proposed C-P topology, if the driving waveform is sinusoidal and centered at 0 V, then ζ is lower bounded by $-1/3.56$ ($\simeq -0.28$).

At the gate terminal, the gate-to-source capacitance reduces the absolute value of the feedback resistance

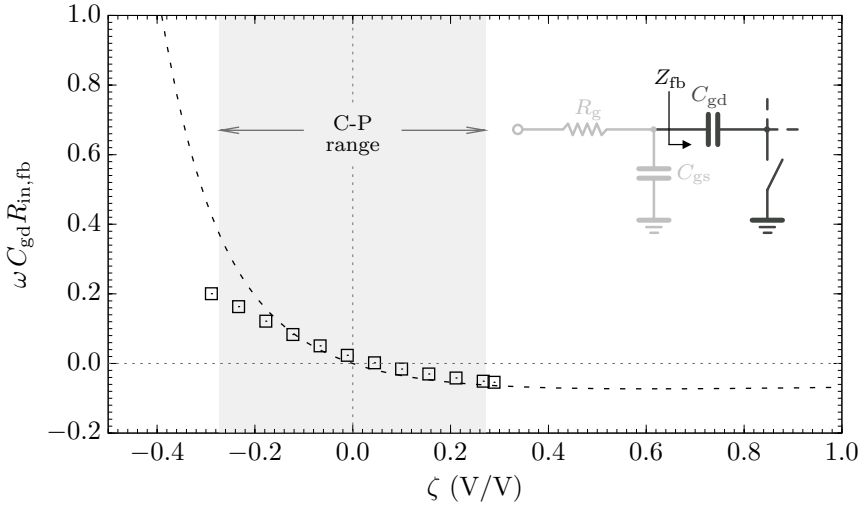
$$R_{\mathrm{in,g}} = \mathrm{real}\Big\{[R_{\mathrm{in,fb}} - j/(\omega C_{\mathrm{in,fb}})] \,||\, [-j/(\omega C_{\mathrm{gs}})]\Big\} \tag{4.28}$$

in which C_{gs} and C_{gd} can be assumed to have approximately the same value (in triode). The effect is represented in Fig. 4.16.

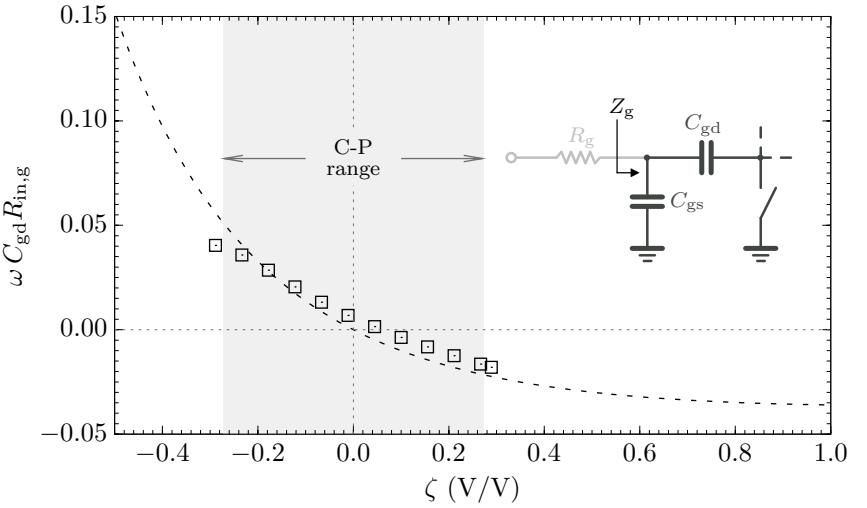
Fig. 4.16 shows that the feedback resistance $R_{\mathrm{in,fb}}$ changes its sign in accordance with the polarity of the power supply. Simulation data with BSIM models is also included, to validate the analytical results. A high-efficiency circuit has been used to attest the proposed analysis, because in this case the switch voltage given by (4.21) does not need to include any efficiency dependence. As ζ approximates its negative limit inherent to the proposed C-P topology, due to the greater difficulty on turning off the transistor, the simulation behavior starts to deviate from predicted results. On the other hand, when the PA is supplied by positive voltages, a positive value of resistance may only be obtained if the gate resistance R_g (shown in figure) is higher than $R_{\mathrm{in,g}}$. The resistance R_g represents the distributed resistance of the gate electrode and also models non-quasi static (NQS) effects [186]. As for the imaginary component, the way the input capacitance is affected is consistent with the Miller effect.

4.3.8 Matching considerations

When the gate resistance R_g is still low to compensate for the negative input resistance, the resultant stability issues must be carefully addressed. To prevent instability at the range of operating frequencies, a positive input resistance must be ensured. Fig. 4.17 shows a matching topology proposed



(a)



(b)

Figure 4.16: Influence of the feedback capacitance due to power supply ("□" denotes simulation points, whereas the dashed line represents the expression derived).

for the C-P topology. It avoids the negative resistance by including a low positive resistance within the matching network.

In the topology of Fig. 4.17, $-r_i$ and c_i represent, respectively, the negative input resistance and input capacitance looking to the feedback network of the transistor. In this network, to achieve a $50\,\Omega$ input, the capacitor $C_{\mathrm{m_2}}$ decreases the negative component due to $-r_i$. Then, $R_{\mathrm{m_2}}$ allows for some

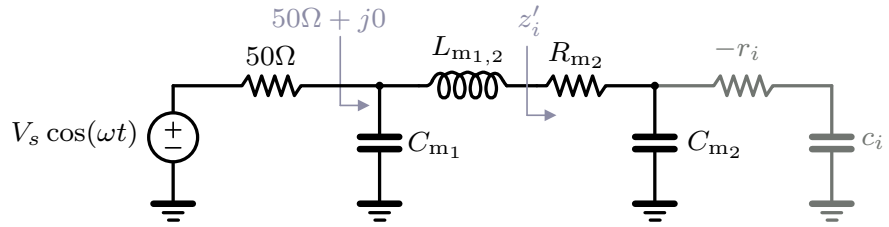


Figure 4.17: Input matching network.

compensation, by converting it into a positive resistance ($r_i' = \text{real}\{z_i'\}$, see Fig. 4.17), which can also incorporate R_g,

$$r_i' = R_{m_2} - \frac{r_i}{(\omega_c C_{m_2} r_i)^2 + (1 + C_{m_2}/c_i)^2} \tag{4.29}$$

In this network topology, a large C_{m_2} reduces the matching sensitivity to r_i, as well as due to input capacitance of the transistor. This is even advisable when the input capacitance is strongly dominated by parasitic capacitances. Still regarding the notation used in Fig. 4.17, assuming $L_{m_{1,2}}$ comprised by $L_{m_1} + L_{m_2}$, nulling the reactive component would imply to have, for instance

$$L_{m_2} = \frac{1}{C_{m_2}} \cdot \frac{r_i^2 + \dfrac{1}{\omega_c^2 c_i}\left(1/c_i + 1/C_{m_2}\right)}{(\omega_c r_i)^2 + (1/c_i + 1/C_{m_2})^2} \tag{4.30}$$

Once these components have been arbitrated, only L_{m_1} and C_{m_1} must be determined to attain $50\,\Omega + j0$ at the input. As part of $L_{m_{1,2}}$ resonates with the input capacitance, the remaining together with C_{m_1} works as an L-matching network. That is, the imaginary component is decreased towards zero, at the same time the input resistance is tuned at $50\,\Omega$ as desired. This last procedure is pretty straightforward. The component values are determined by

$$C_{m_1} = \frac{1}{50\,\omega_c}\sqrt{\frac{50}{r_i'} - 1} \tag{4.31}$$

$$L_{m_1} = 50\,r_i' C_{m_1} \tag{4.32}$$

4.4 Performance Overview

To further validate some of the considerations made in previous sections, and also gain a better perspective on the performance of the proposed CMOS transmitter, let us admit the circuit depicted in Fig. 4.18. Besides the inductor L_{chk} that is an RF choke, the circuit comprises the passive devices that must be designed to meet class-E conditions: the capacitance C_s, which together with the junction capacitance C_j form the total shunt capacitance; and the load network comprising L, C and R_L, all these designed to meet ZVS and ZVDS. The circuit inside the shaded region represented in Fig. 4.18 corresponds to the bidirectional switching device. As shown, the bulk is connected to a power-supply valued $-V_{\text{B}}$, being mandatory to have V_{B} positive.

Since the junction capacitance has some asymmetric behavior due to the bipolar power-supply, the proposed device model also includes it. The junction capacitance is implemented as a nonlinear component given by (4.17). The bipolar current is denoted as i_{sw} and described by relationships (4.9a)–(4.9b) for $v_{\text{sw}} > 0$, and (4.10a)–(4.10b) when $v_{\text{sw}} < 0$. Another asymmetry

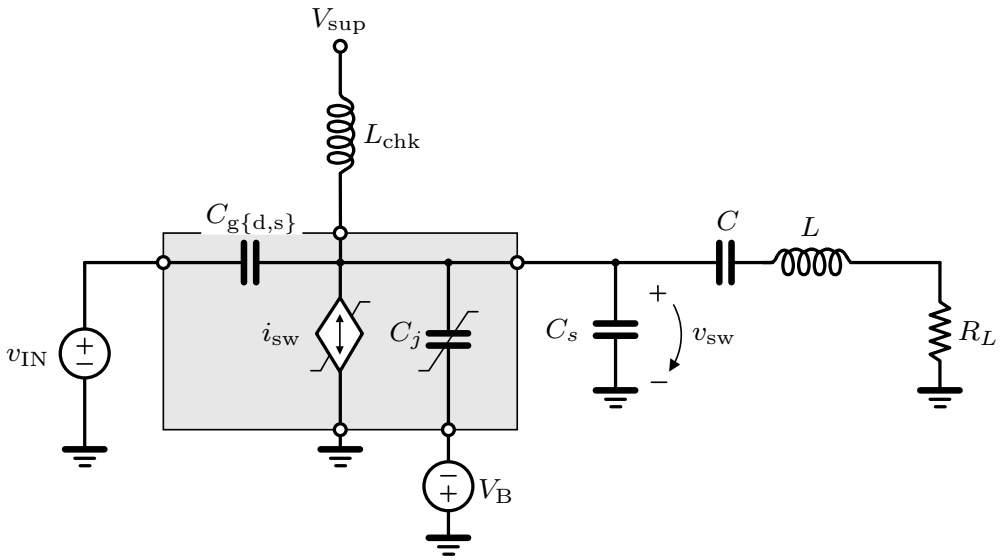


Figure 4.18: Circuit for the CMOS C-P performance overview.

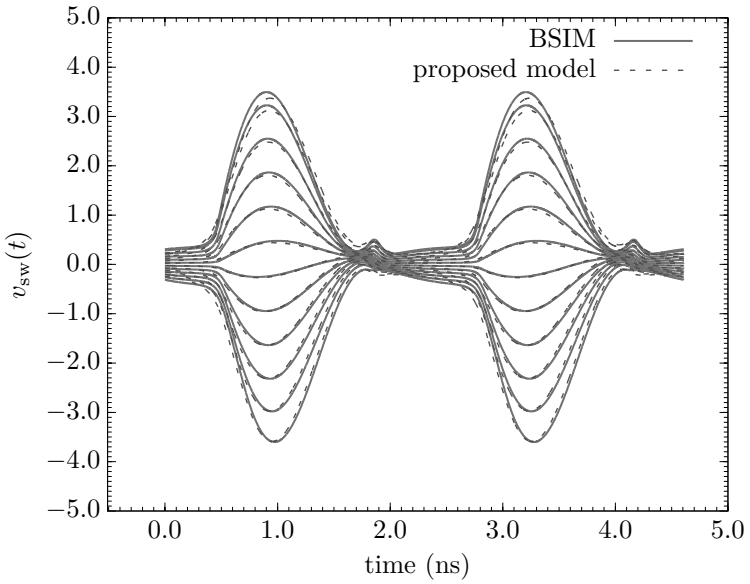


Figure 4.19: Switch time-waveforms with BSIM and proposed model.

previously considered is due to the V_{th} variation. The body effect is incorporated through (4.14) and (4.16), depending on the polarity of v_{sw}. Additionally, a linear capacitance $C_{\text{g\{d,s\}}}$ is included between input and one of the switch terminals. Although a nonlinear behavior should be expected, a linear approximation is adopted for the sake of simplicity. A second capacitance exists between the input and the remaining switch terminal, $C_{\text{g\{s,d\}}}$, but it is neglected here as no driver is assumed for the present analysis. In such a case, R_g would be also of relative importance[3]. The active device is implemented with Verilog-A, and the complete class-E circuit is simulated with Agilent ADS. Fig. 4.19 shows the time waveforms at the switch, obtained from simulations for different power-supply values (both negative and positive). The bulk has been biased at -4.5 V, and a sinusoidal signal has been applied as the gate drive, with null offset. The simulation data is compared in the same figure against other simulation results with BSIM models. The two types of models do not differ much, which demonstrate the validity of the proposed modeling approach for the time domain.

[3]The driving issues are considered later. At this stage, it is preferable to try isolating all the possible effects (e.g. Miller effect) for better understanding of the performance of the amplifier.

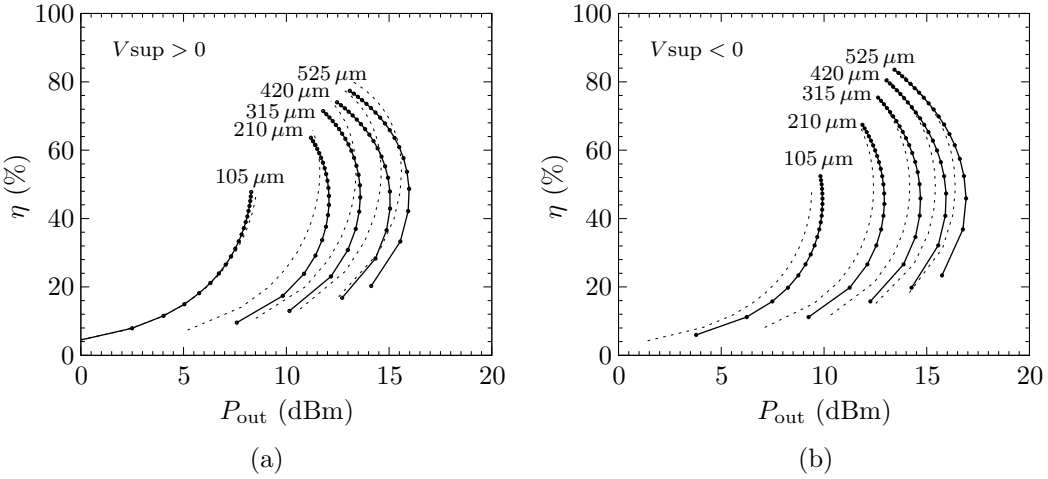


Figure 4.20: Class-E PA efficiency for different load values and switch sizes for (a) positive and (b) negative envelope.

Still as an overview of the present topology let us consider now the power-efficiency compromise. Fig. 4.20 shows results of simulations addressing the efficiency for different transistor dimensions. Each point plotted in the solid lines corresponds to a different load (R_L). The power supply is fixed at $\pm 1.3\,\mathrm{V}$. The solid lines correspond to the model shown in Fig. 4.18, whereas the dashed lines are resultant from simulations with BSIM models. All the passive elements are tuned for each transistor size according to the class-E conditions. The shunt capacitor is adjusted to account for the transistor output parasitic capacitance, which is different for each size but kept unchanged for both values of V_{sup}. In the present CMOS process, the thick-gate-oxide transistors have featured sizes of $0.34\,\mu$m. The transistor length is kept at this minimum value, and the widths are swept to $525\,\mu$m, in $105\,\mu$m steps. Additionally, to include more realistic effects, the RF pad models are also taken into account, as well as a finite Q_u of 70 for the inductor, and a sinusoidal driving signal. The efficiency η is given as $P_{\mathrm{out}}/P_{\mathrm{dc}}$, where P_{dc} is the power driven by the envelope modulator, i.e. the bipolar signals $I(t)$ or $Q(t)$ that are fixed at $\pm 1.3\,\mathrm{V}$ for the present simulation purposes.

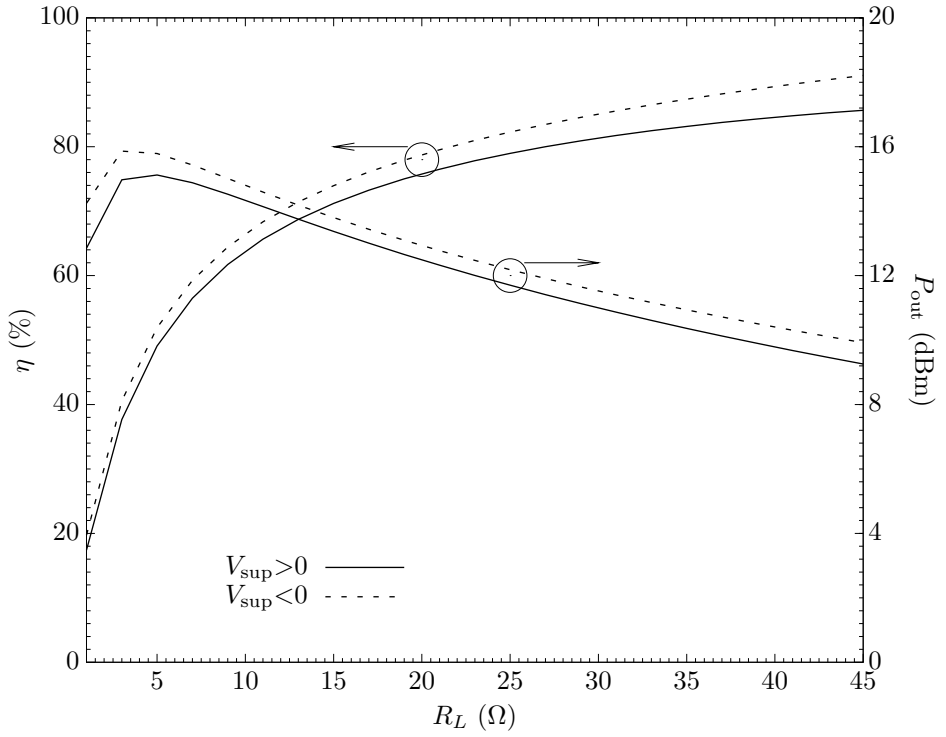


Figure 4.21: Efficiency and output power in terms of load resistance for a $420\,\mu$m/$0.34\,\mu$m transistor in the C-P class-E.

Comparing Figs. 4.20(a) and 4.20(b) one can conclude that a negative envelope allows higher efficiency and output power. This is due to the slightly lower conduction resistance for $v_{\rm sw} < 0$. In both cases, a compromise between transistor dimensions, output power and efficiency is evident. The efficiency is improved with larger transistors, as $R_{\rm on}$ is decreased. The efficiency decreases with the output power (lowering R_L) because both $R_{\rm on}$ and the ESR of the inductor become significant comparing with R_L. A reasonably good tradeoff seems attained for $420\,\mu$m widths[4], at an efficiency above $60\,\%$ with R_L between 10 and $15\,\Omega$, which provides about 14 to 15 dBm of output power. The tradeoff just mentioned is further exemplified in Fig. 4.21, with curves for positive and negative power-supply values, for the transistor dimensions of $W/L = 420\,\mu$m/$0.34\,\mu$m.

[4]Another reason for choosing such size was the existence of silicon dies in the lab, having MOSFETs with an accessible body terminal and widths of $210\,\mu$m. This allows a future implementation of the C-P Tx with four ICs (a larger number increases too much the complexity of assembly).

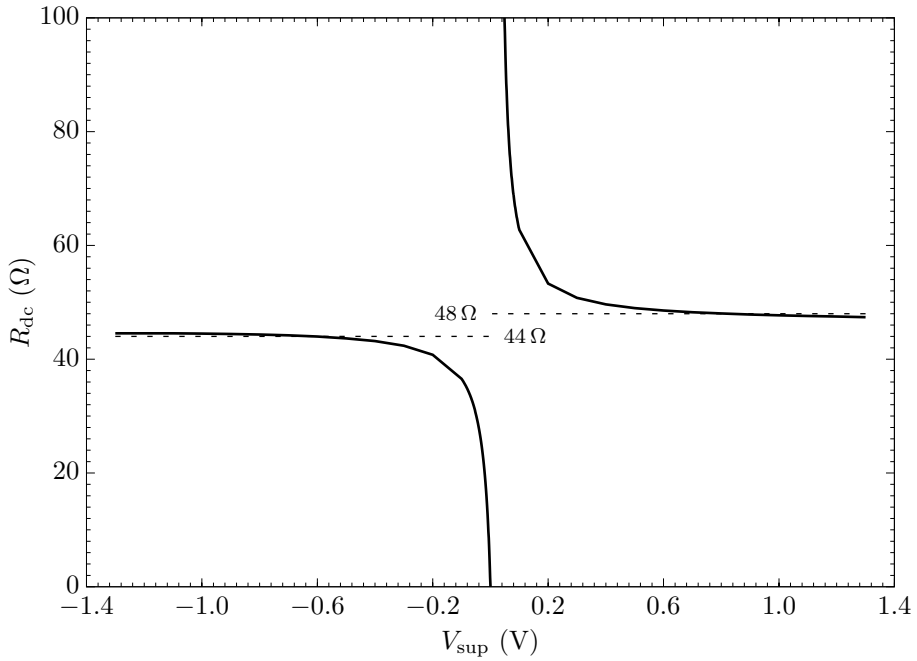


Figure 4.22: R_{dc} in terms of supply voltage.

An interesting parameter to take into account in design is the dc resistance seen from the RF choke, i.e. R_{dc} given as $V_{sup}/<i_{sup}>$. This gives an idea about the driving load for the envelope modulator. Fig. 4.22 shows simulation results from the proposed model, indicating how R_{dc} changes in value for positive and negative envelopes ($\sim 9\,\%$). Moreover, as the envelope has a finite bandwidth, R_{dc} is also useful in the design of low-pass filtering in case of a bidirectional SMPS is to be employed.

It should be noted that the active device includes a Miller capacitance, $C_{g\{d,s\}}$, as a linear component. This has some impact on the power efficiency. In particular, $C_{g\{d,s\}}$ is responsible for some asymmetric behavior in power consumption. Fig. 4.23 shows this effect, and compares it with simulations using BSIM models. In figure, one can also notice that the maximum power at the output is influenced differently due to $C_{g\{d,s\}}$. It can be concluded that an accurate prediction for the efficiency should not neglect this capacitance, although a linear approximation should suffice.

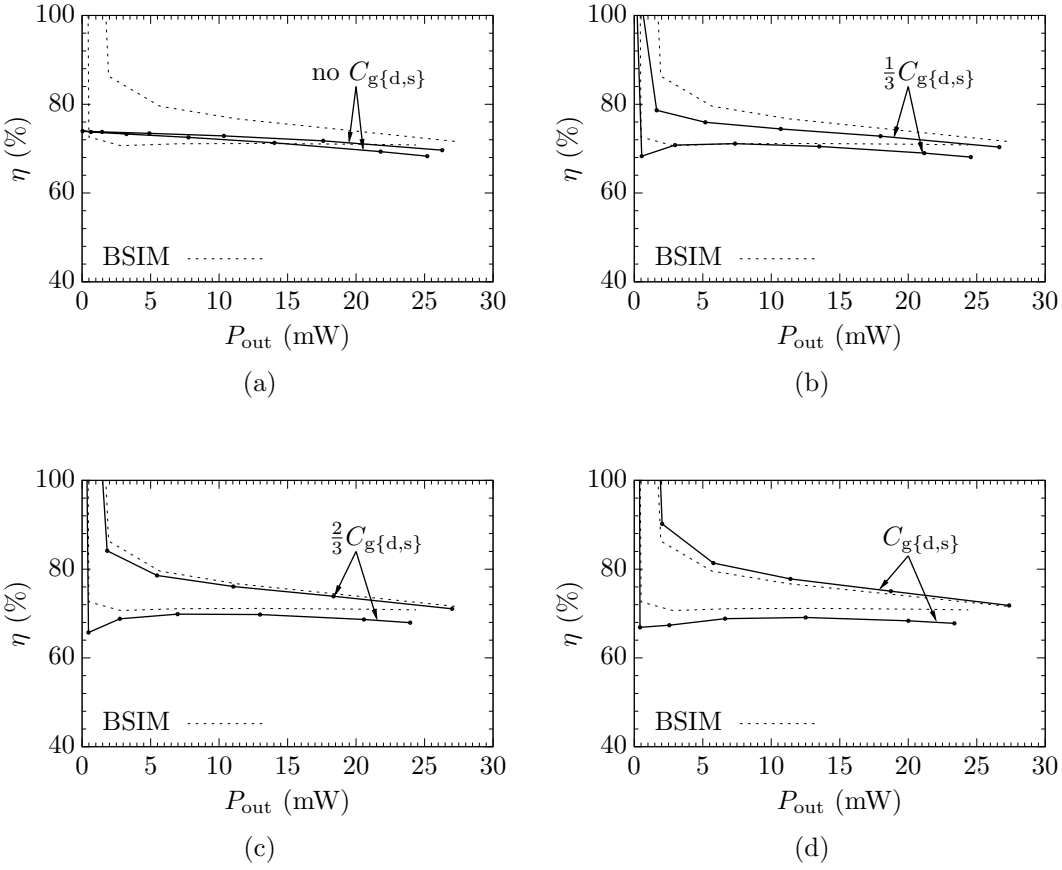


Figure 4.23: Influence of $C_{g\{d,s\}}$ in efficiency.

4.5 Simulation Results

The circuit proposed in this chapter has been implemented in the Agilent ADS environment using the CMOS process already referred along the text. In short, it consist of a process with RF option, providing 340 μm length transistors with thick-gate oxide devices and BSIM 3v3 as simulation models. The CMOS C-P transmitter has been designed with Murata models of SMT devices for the inductors and capacitors. The design follows the values referred in earlier sections, that is, the transistor dimensions are those earlier established, as well as the load value and power supply. At the input is applied an L matching network similar to the one depicted in Fig. 4.17, but with C_{m_2} omitted to minimize the power needed for driving

purposes (note that about 4.5 V are required in magnitude). The drawback is that the impedance seen into the gate of the amplifier improves its sensitivity due to the drain voltage, which is relevant in terms of linearity-efficiency tradeoff. As for the gate bias, an RF choke is applied at the PA to force the dc gate voltage $V_{\text{th0}} = 0.6\,\text{V}$. The C-P transmitter has been built using two of these amplifiers and a 180-degree hybrid combiner using SMT devices. A 90-degree hybrid combiner has been used with a single voltage reference at the fundamental frequency with 1 V at its input of the matching network. The voltage supply has been swept between $-1.3\,\text{V}$ and $+1.3\,\text{V}$ simultaneously in both sides, i.e. with $I = Q$, to achieve the maximum power of 13.5 dBm.

In order to establish a performance reference, a LINC transmitter has been designed with the same semiconductor process as in the C-P transmitter. Due to architectural similarities, the same output combiner is employed at both designs. Moreover, a class-E PA has been also applied in the LINC transmitter, which allows the use of a the same PA components. However, the major differences in the LINC design are worth mentioning. As the bulk is connected to ground in the LINC PAs, for the same drain voltage the junction stress can be reduced in half when comparing to the C-P counterpart. About 6 dB improvement in output power should be expected if doubling the maximum voltage of the power-supply. However, due to the limits for gate-oxide integrity, there is less room for such improvement. While in the C-P transmitter the gate driver must be lower than the drain peak voltage, in LINC there is an additional degree of freedom. That is, the driving level can be reduced. Hence, the maximum power-supply for the PA and gate driving should be constrained to

$$3.56\,V_{\text{dd}} + V_{\text{G}} < V_{\text{GOX,bd}} + V_{\text{th0}} \tag{4.33}$$

This relationship assumes the gate biased at V_{th0} and superimposed to a single tone $V_{\text{G}}\cos(\omega_c t)$. Furthermore, the term 3.56 at the power supply may be lowered when dealing with reduced efficiencies. For the present

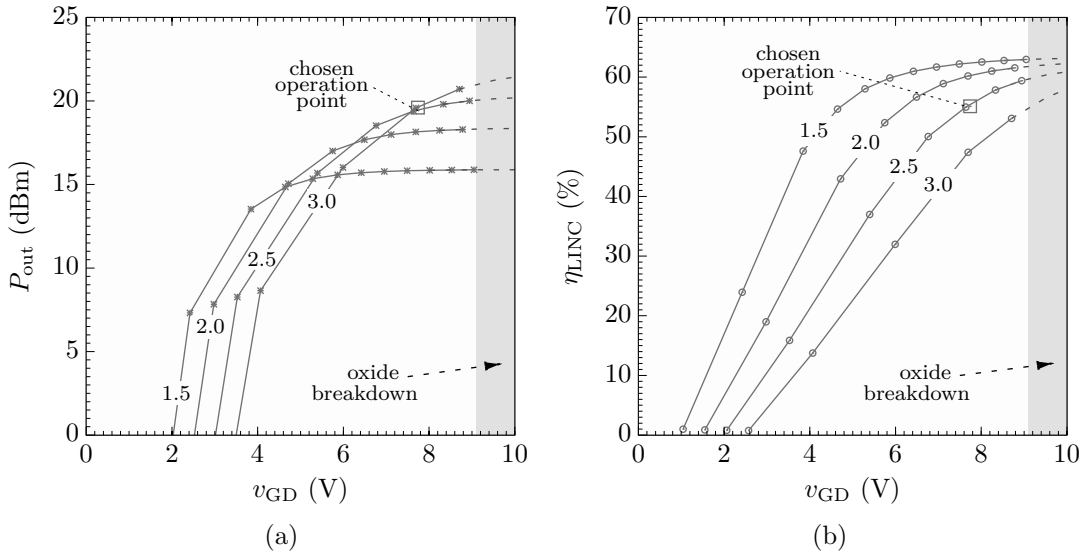


Figure 4.24: LINC efficiency and output power in terms of v_{GD} for different power-supply levels (each curve corresponds to a constant power supply value).

design, if one chooses V_{dd} too high, although the respective output power may be maximized, the driving level is in effect constrained. As a result, the efficiency drops significantly. On the other hand, improving the driver amplitude has the effect of reducing the output power. To better obtain an idea about a reasonable performance, several simulations were performed sweeping both V_{dd} and V_{G}, with $V_{\text{th0}} \simeq 0.6\,\text{V}$ and the passive elements properly tuned for each pair of inputs. Figs. 4.24(a)–4.24(b) shows the data resultant from the simulations. The tradeoff between efficiency and output power is evident in the two figures. Nonetheless, one should emphasize the fact that the LINC PAs operate producing the maximum output power at all time. While in the C-P alternative the stress decreases with higher PAPR values, in the LINC the RF stress at the gate oxide is always constant and at its maximum. For the present LINC design, the voltage amplitude chosen for the gate driver is 2.0 V, and the power supply is fixed at 2.5 V. At the input, a network similar to the C-P transmitter is employed to provide a $50\,\Omega$ matching. To achieve the required voltage amplitude at the gate terminals, the input is driven by a 300 mV sine wave. The target

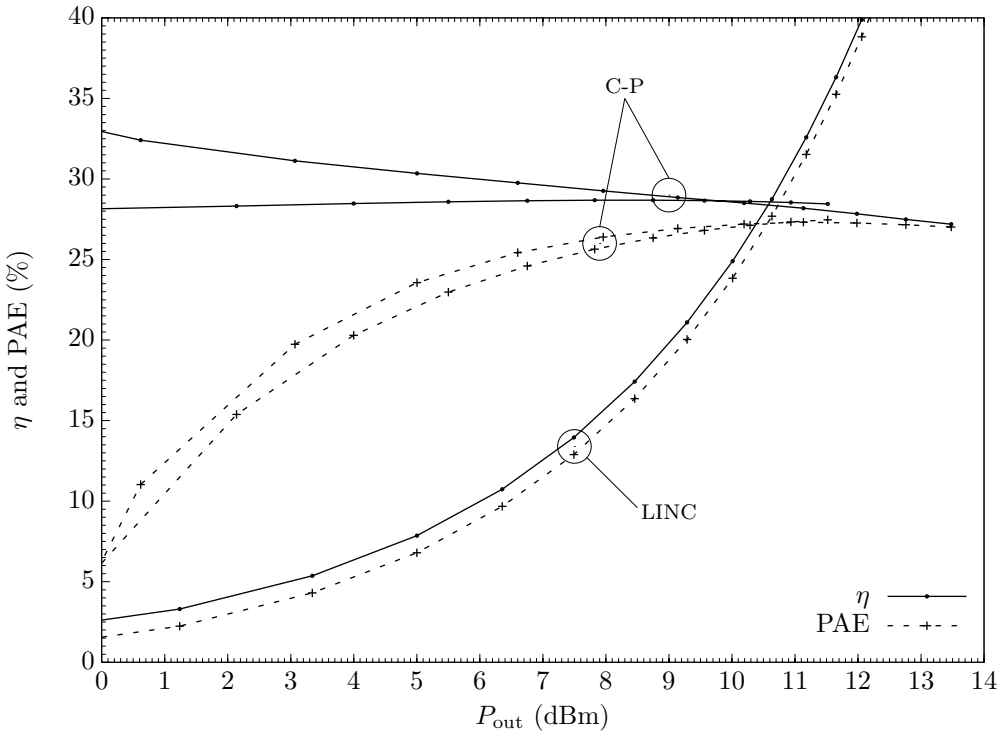
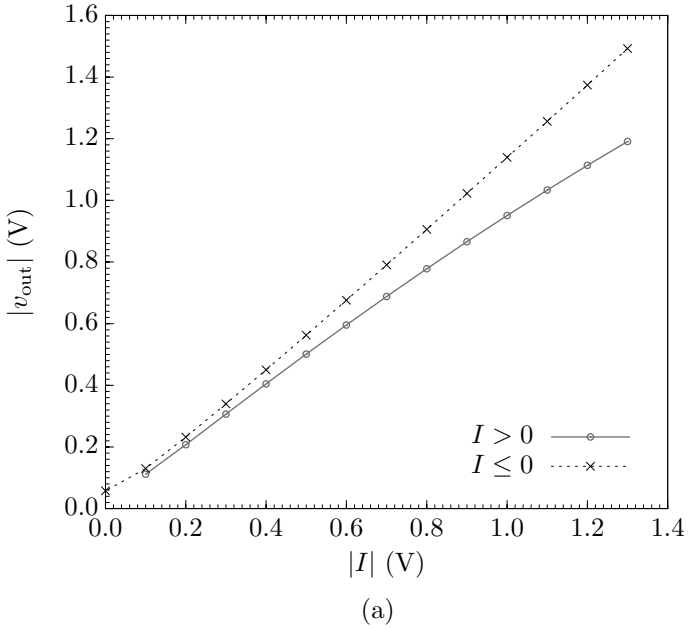


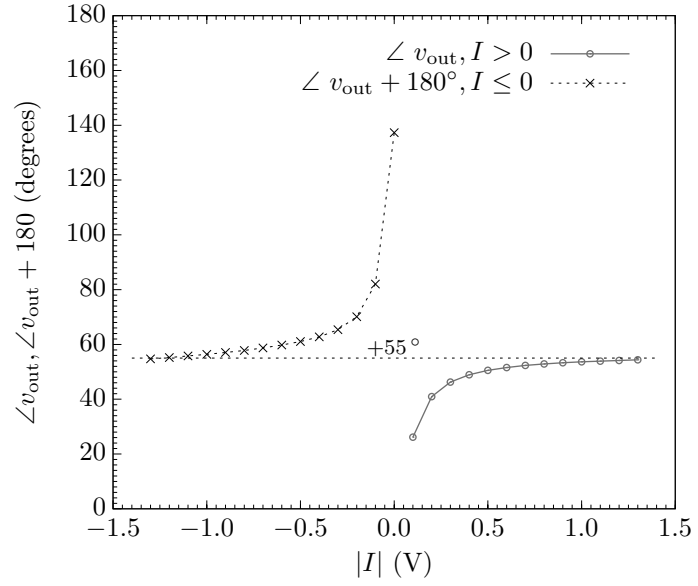
Figure 4.25: Efficiencies C-P *vs.* LINC in CMOS designs.

chosen for the output power is established at 19 dBm, corresponding to an efficiency value close to $\simeq 55\,\%$. For comparison purposes the peak power of the LINC is normalized to the maximum obtained with the proposed C-P architecture.

Fig. 4.25 depicts simulation results for the C-P and LINC transmitters obtained with the Agilent-ADS using harmonic balance (HB). For the LINC transmitter, the outphasing angle has been varied from 0 to 90° to obtain the complete power range. As predicted, the drain efficiency of the C-P transmitter is higher than in the LINC for signals above the 3 dB of power B-O. The magnitude and phase of the output signals of the C-P transmitter are represented in Fig. 4.26. At least for the magnitude, the asymmetries in positive and negative voltage supplies are noticeable. This can be tackled by means of digital predistortion or increasing the power in the gate drive. The same applies to the phase, whereas the asymptotes in Fig. 4.26(b) represent the 180° phase difference.



(a)



(b)

Figure 4.26: Simulation results for CMOS C-P magnitude and phase of the output signal. For easier comparison, for $I \leq 0$, the phase has been shifted up 180°.

The present results denote the feasibility of the proposed circuit as a possible CMOS version for the C-P transmitter. An obvious limitation is the power output, which is due to reliability issues and are strictly process

dependent. Nonetheless, concerning low-power applications for which the CMOS technology is typically employed, the C-P architecture shows to be a viable option for a relatively large range of B-O levels. The body terminal needs to be accessible, which is only relatively easy to attain with CMOS technologies. This issue will be addressed in detail in the next chapter with a new circuit proposed to be used with other types of semiconductor devices.

Chapter 5

C-P Transmitter based on a Differential PA Topology

In chapter 4, the proposed C-P version addressed technologies in which the bulk terminal is electrically accessible and not short-circuited to the source terminal. The circuit allowed bidirectional currents in the transistor by means of a negatively-biased bulk, as well as a nearly-symmetric structure of the NMOS transistor. However, this is only feasible with CMOS implementations due to its full-custom capabilities. Since such technologies are rarely a suitable option for Watt-level applications (due to typical low-voltage breakdowns), the present chapter addresses an alternative solution for a C-P transmitter in semiconductor processes other than CMOS.

In most common power devices available off the shelf, like silicon LDMOS or standard III-V devices (GaAs, GaN, etc), the source/emitter terminal is always connected to the heat sink, coinciding with the electrical ground. As such, the asymmetric structure prevents the usage of these devices within the previous C-P topology. In the circuit proposed now, the bulk is connected to the source terminal. Consequently, an adequate approach is required to ensure that only positive voltages occur at the drain. If this is not the case, some risks remain on reverse biasing the bulk-drain junction. Hence, to overcome this issue, a positive offset is introduced at the drain voltage. Fig. 5.1 depicts a representation of the proposed approach. The carrier consists of two balanced signals with equal frequencies,

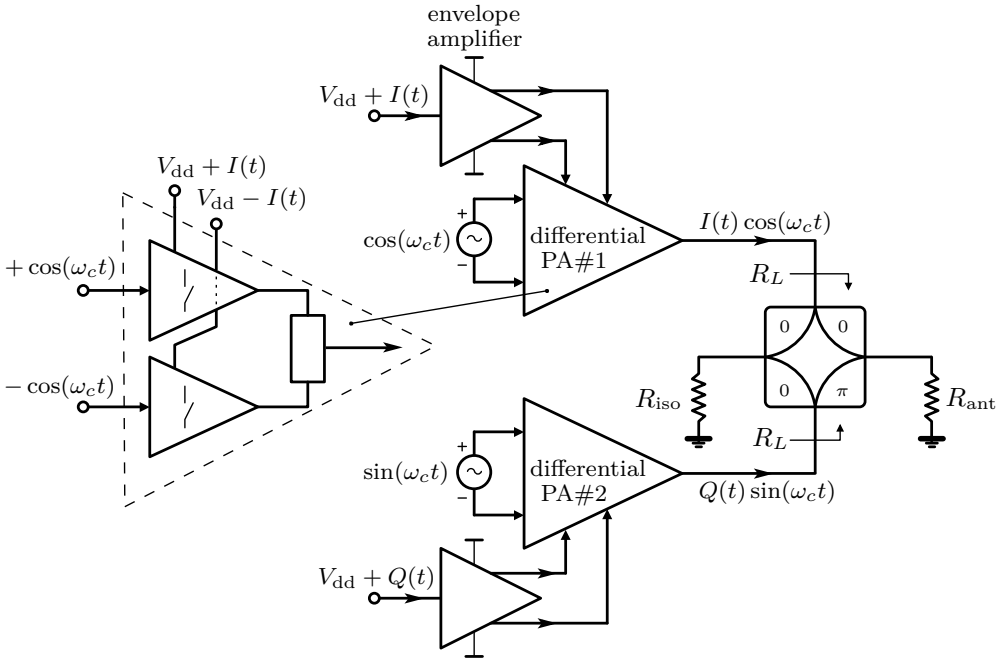


Figure 5.1: Block diagram of the LDMOS topology for the C-P transmitter.

fixed magnitudes and constant 90-degree phase differences: $\pm\sin(\omega_c t)$ and $\pm\cos(\omega_c t)$. These can be easily obtained from a stable frequency source applied to a 90-degree hybrid combiner, followed by RF transformers implemented as baluns. At the output, the proposed structure is exactly the same as previously: a 180-degree hybrid combiner to couple the modulated signals from the amplifiers to the antenna. In contrast to the previous approach, the major modification in the block diagram representation relies on the way the envelope signals are applied at each quadrature branch: $I(t)$ and $Q(t)$ are now two differential signals. This pair of differential signals has a dc voltage as the common-mode voltage, i.e. $V_{\rm dd}$. Therefore, the envelope amplifiers provide at their outputs $V_{\rm dd} \pm I(t)$ and $V_{\rm dd} \pm Q(t)$.

The proposed circuit for the differential PAs must selectively operate between two distinct behaviors: the common and differential modes. In essence, what is being proposed here is that the two differential PAs operate as amplifiers only at the differential mode. The common-mode components should be rejected by an adequate circuit topology avoiding current paths

through the load. Moreover, it should be noted that the fundamental purposes of using bipolar signals within the C-P transmitter are maintained in the proposed concept. That is, the relaxed bandwidth requirements for the SMPSs are kept unchanged because there is no need for any rectification of $I(t)$ or $Q(t)$ signals. As such, each envelope amplifier depicted in Fig. 5.1 can be implemented as efficient switching amplifiers without stringent speed requirements.

In the next section, the differential PA will be analyzed separately from the C-P structure. The main issues in the differential topology are firstly identified and a circuit is proposed for its practical realization. In a following section, a design example is presented using LDMOS transistors. The efficiency comparison will be established using the differential PAs in a C-P architecture, against a LINC transmitter using the same active devices.

5.1 Proposed Topology

Concerning the definition of the C-P transmitter with differential PAs, let us draw the attention to some key aspects first. An adequate topology for the differential PA should take into account the following list of attributes:

i. for an efficient solution, the proposed circuit needs to be operated in switching mode;
ii. the time-varying signals $\pm I(t)$ and $\pm Q(t)$ are assumed to have an LPF behavior, with bandwidths much lower than the switching frequency;
iii. when the data input is null, i.e. $\pm I(t) = 0$ or $\pm Q(t) = 0$, the power dissipation at the respective amplifier and its load should both tend to zero; this must hold disregarding the values of V_{dd};
iv. for high efficiency, the power derived from the generation of $\pm I(t)$ or $\pm Q(t)$ signals should be totally consumed by the load;

v. regardless of the values of V_{dd} and $I(t)$ or $Q(t)$, the ZVS condition must be ensured to prevent switching losses due to parasitic shunt capacitances;

vi. the drain voltage must be either positive or null at any time instant.

Given the major obstacle of 50 % of the power lost in the combination of the I and Q signals, there are still some concerns related with the efficiency, given as the two following additional requirements:

vii. the proposed circuit should include a power-recycling mechanism, which is assured if the four-port combiner is maintained at the output as depicted in Fig. 5.1;

viii. as the circuit requires reduced sensibility to V_{dd}, this characteristic should be explored to compensate for any efficiency degradation due to zero or very low envelope levels, e.g. introducing a time varying V_{dd} to reduce the energy in common-mode operation.

The operation principle of the differential topology should attempt to meet all the conditions just described. However, the simultaneity of those requirements denote several practical difficulties. For instance, the rejection of common-mode components implies that no current should flow through R_L due to a common-mode stimulus – hence, the load should behave as an infinite impedance. On the other hand, the amplification of the differential mode needs the load to be *actually seen* by the circuit, as a finite load, to absorb the power provided by $\pm I(t)$ and $\pm Q(t)$. To accommodate these and the other requirements, it is proposed the differential PA depicted in Fig. 5.2. Each differential PA in Fig. 5.1 corresponds to the circuit shown in Fig. 5.2. The proposed topology is built from two switching devices connected by a complex network of passive components. The gate signals v_{G_1} and v_{G_2} consist of signals in opposite phases, either $V_{\mathrm{G}} \pm V_{\mathrm{g}} \cos(\omega_c t)$ or $V_{\mathrm{G}} \pm V_{\mathrm{g}} \sin(\omega_c t)$, whereas the signals $\pm V_i$ represent $\pm I(t)$ or $\pm Q(t)$. For establishing the switching operation, the gate drive must present a sufficiently high amplitude, V_{g}, to force the active devices into deep cut-off and triode regions. The bias V_{G} coincides with the V_{th} of the transistor.

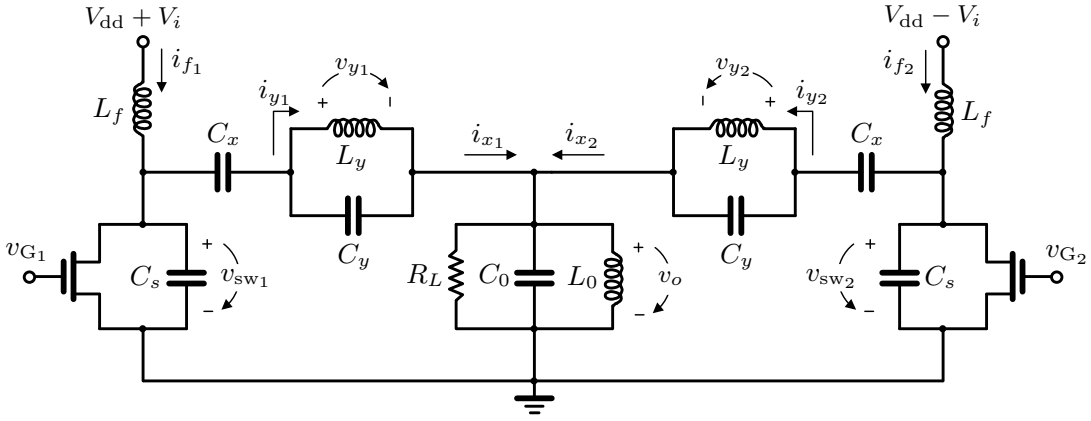


Figure 5.2: Schematic of the proposed differential power amplifier.

At the drain of each transistor, an inductor L_f is used as a finite dc-feed. This imposes the average values $V_{\rm dd}+V_i(t)$ or $V_{\rm dd}-V_i(t)$ for the drain voltages. The shunt capacitances C_s include the drain-source capacitance of each transistor, such as in typical class-E PAs. The capacitors C_x are included to avoid a dc short and, in conjuction with the L_yC_y networks, also ensure there are enough degrees of freedom for the present design purposes. In Fig. 5.2 (and Fig. 5.1, also), the resistance R_L represents the resistance seen at the input ports of the power combiner (typically $50\,\Omega$), whereas the parallel connection of the tank L_0C_0, tuned at the fundamental frequency $\omega_c = 1/\sqrt{L_0C_0}$, provides a short circuit for all out-of-band components. The currents $i_{x_{1,2}}(t)$, shown in the figure, comprise both common- and differential-mode components due to $V_{\rm dd}$ and $\pm V_i(t)$, respectively. Only the fundamental components of $i_{x_{1,2}}(t)$ flow through R_L, whereas the remaining harmonics have a current path through L_0 and C_0. Any non-null reactive component of the input impedance of the combiner can be absorbed into the values of the tank components, which allows an additional design flexibility. Conversely, the remaining passive components require a specific design to satisfy the objectives previously mentioned. Consider for instance the common-mode operation. Let us admit the case of null $V_i(t)$, that is, the circuit is powered solely by $V_{\rm dd}$. No energy losses can occur during this phase, particularly due to switching losses, which are quite

often associated with the dominating loss mechanisms at RF operation. Hence, if the ZVS condition is satisfied when $V_i(t) = 0$, then one might ask what happens to the common-mode components in terms of energy flow. If no power can be wasted, then the circuit must behave as an oscillator as response to V_{dd} as the voltage stimulus. Therefore, the energy required by the common-mode operation should be delivered by V_{dd} and returned back to the same power supply during each RF cycle. In essence, the dc power-supply only introduces a fixed amount of energy at the initial state. Then, the high-frequency currents flow back and forth in the switched circuit, that is, as long as ZVS occurs and the conduction losses are negligible.

On the other hand, when a non-null time-varying symmetric $\pm V_i(t)$ is added to V_{dd}, the circuit has to respond differently. Due to the differential voltage excitation, R_L should be seen as a finite part of the load network. Additionally, no power should be wasted on switching. Hence, ZVS is demanded again because, at any $V_i(t)$ value, its sum or difference with V_{dd} must not deteriorate the common-mode rejection. Besides this, another aspect to take into consideration is that V_{dd} should be kept sufficiently high to avoid negative drain voltages due to $\pm V_i(t)$. As a conclusion, the circuit responds to the differential envelope input excitation as a differential PA (disregarding V_{dd}), and to common-mode components as a switched oscillator (disregarding V_i). To the best knowledge of the author, there are no similar circuit structures existent in literature to accomplish the twofold requirements with the same circuit. Only passive combiners are usually employed for such purposes.

5.1.1 Circuit waveforms

The circuit equations are still required for design purposes. As such, an analytical model is developed in this section, enabling the derivation of approximate expressions needed for the design. Since the present topology consists of a nonlinear system, superposition is generally not applicable.

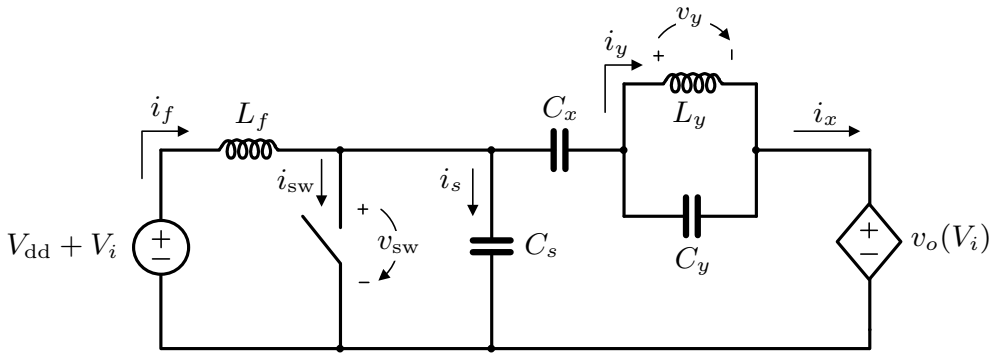


Figure 5.3: Proposed simplification for the analysis of the differential PA.

However, without any further simplification, studying the performance of this circuit becomes excessively laborious. To derive a set of approximate equations, the system will be treated as linear time variant (LTV) with on and off states imposed by an RF source assumed as "internal" in such an LTV system (similarly to the analysis of mixers or sampling circuits). The adopted approach consists on separately addressing the common and differential modes of the system under the specific circumstances that allow the superposition of both modes. The inputs $\pm V_i(t)$ are considered constant, the transistors are assumed ideal switches ($R_{\rm on} = C_{\rm ds} = 0$), and ZVS is imposed during off-on transitions. Fig. 5.3 shows the simplified version of the topology used in the present analysis. Such simplification reduces considerably the number of circuit nodes and branches, hence also the number of equations. At each component terminals, the voltage $v(t)$ will be decomposed into a common-mode component $\overline{v}(t, V_{\rm dd})$ and a differential-mode component $\widetilde{v}(t, V_i)$ so that $v(t) = \overline{v}(t, V_{\rm dd}) + \widetilde{v}(t, V_i)$. The same approach is applied to circuit currents. The analysis is carried out first considering $V_i(t) = 0$, that is, studying only the waveforms $\overline{v}(t, V_{\rm dd})$ and $\overline{i}(t, V_{\rm dd})$; and then considering $V_i(t) \neq 0$ to obtain also $\widetilde{v}(t, V_i)$ and $\widetilde{i}(t, V_i)$.

Null input waveforms

For the first case, in which $V_i = 0$, let us consider that infinite common-mode rejection is assured. Under such circumstances, the voltage across R_L is null, which implies $v_o = 0$ in the equivalent circuit of Fig. 5.3. While the transistor is deactivated, arbitrarily during $0 \leq \omega_c t \leq \pi$, applying nodal analysis leads to the following KCL equations

$$\frac{1}{L_f}\int_0^t \left[\overline{v}_{\rm sw}(t,V_{\rm dd}) - V_{\rm dd}\right] {\rm d}t + \bar{i}_f(0,V_{\rm dd}) + \left[C_s + C_x\right]\frac{{\rm d}\overline{v}_{\rm sw}(t,V_{\rm dd})}{{\rm d}t} - C_x\frac{{\rm d}\overline{v}_y(t,V_{\rm dd})}{{\rm d}t} = 0 \tag{5.1}$$

and

$$C_x\left[\frac{{\rm d}\overline{v}_y(t,V_{\rm dd})}{{\rm d}t} - \frac{{\rm d}\overline{v}_{\rm sw}(t,V_{\rm dd})}{{\rm d}t}\right] + C_y\frac{{\rm d}\overline{v}_y(t,V_{\rm dd})}{{\rm d}t} + \frac{1}{L_y}\int_0^t \overline{v}_y(t,V_{\rm dd})\,{\rm d}t + \bar{i}_y(0,V_{\rm dd}) = 0 \tag{5.2}$$

Applying the time derivative to both expressions (5.1) and (5.2), and working out the interdependence results

$$\frac{{\rm d}^2\overline{v}_{\rm sw}(t,V_{\rm dd})}{{\rm d}t^2} + \omega_f^2\overline{v}_{\rm sw}(t,V_{\rm dd}) = -\frac{1}{1+C_s/C_x}\omega_y^2\overline{v}_y(t,V_{\rm dd}) + \omega_f^2 V_{\rm dd} \tag{5.3}$$

and

$$\frac{{\rm d}^2\overline{v}_y(t,V_{\rm dd})}{{\rm d}t^2} + \omega_y^2\overline{v}_y(t,V_{\rm dd}) = -\frac{1}{1+C_y/C_x}\omega_f^2\left[\overline{v}_{\rm sw}(t,V_{\rm dd}) - V_{\rm dd}\right] \tag{5.4}$$

with $\omega_f^2 = 1/[L_f(C_s + C_x||C_y)]$ and $\omega_y^2 = 1/[L_y(C_y + C_x||C_s)]$, where $C_a||C_b = C_aC_b/[C_a + C_b]$. Based on (5.3), one obtains

$$\omega_y^2\overline{v}_y(t,V_{\rm dd}) = \left[1 + \frac{C_s}{C_x}\right]\left[\omega_f^2 V_{\rm dd} - \frac{{\rm d}^2\overline{v}_{\rm sw}(t,V_{\rm dd})}{{\rm d}t^2} - \omega_f^2\overline{v}_{\rm sw}(t,V_{\rm dd})\right] \tag{5.5}$$

and, applying twice the differentiation with respect to time,

$$\frac{{\rm d}^2\overline{v}_y(t,V_{\rm dd})}{{\rm d}t^2} = -\left[1 + \frac{C_s}{C_x}\right]\left[\frac{1}{\omega_y^2}\frac{{\rm d}^4\overline{v}_{\rm sw}(t,V_{\rm dd})}{{\rm d}t^2} + \frac{\omega_f^2}{\omega_y^2}\frac{{\rm d}^2\overline{v}_{\rm sw}(t,V_{\rm dd})}{{\rm d}t^2}\right] \tag{5.6}$$

Substituting (5.5) and (5.6) into (5.4) leads to a single differential equation, although with higher order

$$\frac{\mathrm{d}^4\overline{v}_{\mathrm{sw}}(t,V_{\mathrm{dd}})}{\mathrm{d}t^4}+\left[\,\omega_f^2+\omega_y^2\,\right]\frac{\mathrm{d}^2\overline{v}_{\mathrm{sw}}(t,V_{\mathrm{dd}})}{\mathrm{d}t^2}+\omega_z^4\,\overline{v}_{\mathrm{sw}}(t,V_{\mathrm{dd}})=\omega_z^4 V_{\mathrm{dd}} \tag{5.7}$$

with $\omega_z^4 = 1/(L_f L_y[\,C_sC_x + C_yC_x + C_sC_y\,])$. Formally defining $\Lambda \subseteq \mathbb{R}^6$ as a design set $\Lambda = \left\{(C_s, C_x, C_y, L_y, L_f, R_L)\,|\,C_s, C_x, C_y, L_y, L_f, R_L \in \mathbb{R}^+\right\}$, the solution to the differential equation in (5.7) is

$$\overline{v}_{\mathrm{sw}}(t,V_{\mathrm{dd}}) = V_{\mathrm{dd}}+\alpha_1\sin(\omega_a t)+\alpha_2\cos(\omega_a t)+\alpha_3\sin(\omega_b t)+\alpha_4\cos(\omega_b t) \tag{5.8}$$

where the coefficients $\alpha_1, \ldots, \alpha_4$ are all functions of $\lambda \in \Lambda$ with no other time or input dependencies. As for the frequencies ω_a and ω_b, these are given by the solution of the bi-quadratic form of the characteristic equation,

$$\omega_a^2 = \tfrac{1}{2}\omega_f^2 + \tfrac{1}{2}\omega_y^2 + \tfrac{1}{2}\sqrt{(\omega_f^2+\omega_y^2)^2 - 4\omega_z^4} \tag{5.9}$$

$$\omega_b^2 = \tfrac{1}{2}\omega_f^2 + \tfrac{1}{2}\omega_y^2 - \tfrac{1}{2}\sqrt{(\omega_f^2+\omega_y^2)^2 - 4\omega_z^4} \tag{5.10}$$

The purely imaginary roots allow such simple result due to the nonexistence of any resistive element in the present circuit form. Otherwise, the quartic equation would give longer solutions (still analytical). Here, the imaginary roots are ensured by $\omega_f^2+\omega_y^2 \geq 2\,\omega_z^2$ with the capacitances and inductances as real positive quantities.

On the remaining phase, when the transistor is activated, it results in an undriven LC circuit

$$\frac{\mathrm{d}^2\overline{v}_y(t,V_{\mathrm{dd}})}{\mathrm{d}t^2}+\omega_{xy}^2\,\overline{v}_y(t,V_{\mathrm{dd}})=0 \tag{5.11}$$

with natural frequency $\omega_{xy} = 1/\sqrt{L_y(C_x+C_y)}$ and homogeneous solution

$$\overline{v}_y(t,V_{\mathrm{dd}}) = \beta_1\sin(\omega_{xy}[t-\pi/\omega_c]) + \beta_2\cos(\omega_{xy}[t-\pi/\omega_c]) \tag{5.12}$$

whereas $\overline{v}_x(t,V_{\mathrm{dd}}) = -\overline{v}_y(t,V_{\mathrm{dd}})$ during this time interval, $\pi < \omega_c t \leq 2\pi$. For the remaining time of the fundamental period, the voltage at L_y can

be determined by replacing (5.8) in (5.5), resulting in

$$\overline{v}_y(t,V_{\rm dd}) = \frac{1}{\omega_y^2}\left[1+\frac{C_s}{C_x}\right]\Big[\left[\,\omega_a^2-\omega_f^2\,\right]\left[\alpha_1\sin(\omega_a t)+\alpha_2\cos(\omega_a t)\,\right] + \left[\,\omega_b^2-\omega_f^2\,\right]\left[\,\alpha_3\sin(\omega_b t)+\alpha_4\cos(\omega_b t)\,\right]\Big] \quad (5.13)$$

Two important conditions should be established to determine β_1 and β_2. One is that the dc voltage across L_y must be null, and the other is due to C_y for which the dc current should be null as well. This allows us to summarize the following

$$\int_0^{2\pi/\omega_c} \overline{v}_y(t,V_{\rm dd})\,{\rm d}t = 0 \quad (5.14)$$

$$\int_0^{2\pi/\omega_c} \frac{{\rm d}\overline{v}_y(t,V_{\rm dd})}{{\rm d}t}\,{\rm d}t = 0 \quad (5.15)$$

Applying (5.14)–(5.15) to (5.12) and (5.13) leads to β_1 and β_2.

Let us proceed now by taking into consideration the ZVS conditions and dc short across L_f,

$$\overline{v}_{\rm sw}(0,V_{\rm dd}) = 0 \quad (5.16)$$

$$\overline{v}_{\rm sw}(\pi/\omega_c,V_{\rm dd}) = 0 \quad (5.17)$$

$$\int_0^{\pi/\omega_c} \overline{v}_{\rm sw}(t,V_{\rm dd})\,{\rm d}t = \frac{2\pi}{\omega_c}\,V_{\rm dd} \quad (5.18)$$

Three out of four constants can be determined from (5.16)–(5.18). As for the last one, charge conservation can be applied as follows

$$\int_0^{\pi/\omega_c}\left[\bar{i}_f(t,V_{\rm dd})+\bar{i}_y(t,V_{\rm dd})\right]{\rm d}t + \int_0^{\pi/\omega_c} C_x\frac{{\rm d}\overline{v}_x(t,V_{\rm dd})}{{\rm d}t}\,{\rm d}t + \int_0^{\pi/\omega_c} C_y\frac{{\rm d}\overline{v}_y(t,V_{\rm dd})}{{\rm d}t}\,{\rm d}t = \int_{\pi/\omega_c}^{2\pi/\omega_c}\left[\bar{i}_f(t,V_{\rm dd})+\bar{i}_y(t,V_{\rm dd})\right]{\rm d}t + \int_{\pi/\omega_c}^{2\pi/\omega_c} C_x\frac{{\rm d}\overline{v}_x(t,V_{\rm dd})}{{\rm d}t}\,{\rm d}t + \int_{\pi/\omega_c}^{2\pi/\omega_c} C_y\frac{{\rm d}\overline{v}_y(t,V_{\rm dd})}{{\rm d}t}\,{\rm d}t \quad (5.19)$$

leading to

$$\overline{v}_y(0^+,V_{\rm dd}) - \overline{v}_y(\pi/\omega_c^-,V_{\rm dd}) + \overline{v}_y(2\pi/\omega_c^-,V_{\rm dd}) - \overline{v}_y(\pi/\omega_c^+,V_{\rm dd}) + \frac{1}{2}\frac{\pi^2}{\omega_c^2}\frac{V_{\rm dd}}{C_x} - \frac{1}{2}\frac{1}{L_f C_x}\int_0^{\pi/\omega_c}\int_0^t \overline{v}_{\rm sw}(t,V_{\rm dd})\,{\rm d}t^2 = 0 \quad (5.20)$$

As for the current through the inductor L_f, one can write the following equations for both states of the switch

$$\bar{i}_f(t,V_{\rm dd})=\begin{cases}\dfrac{t}{L_f}V_{\rm dd}-\dfrac{1}{L_f}\displaystyle\int_0^t\overline{v}_{\rm sw}(t,V_{\rm dd})\,{\rm d}t+\bar{i}_f(0,V_{\rm dd}), \text{for } 0\le\omega_c t\le\pi & (5.21)\\ \dfrac{1}{L_f}V_{\rm dd}\big[\,t-\pi/\omega_c\,\big]+\bar{i}_f(\pi/\omega_c,V_{\rm dd}), \qquad \text{for } \pi<\omega_c t\le 2\pi & (5.22)\end{cases}$$

Taking into account $\bar{i}_f(0,V_{\rm dd})=\bar{i}_f(2\pi/\omega_c,V_{\rm dd})$ and (5.18) in (5.21), the initial condition for (5.22) can be determined as

$$\bar{i}_f(\pi/\omega_c,V_{\rm dd})=\bar{i}_f(0,V_{\rm dd})-\frac{\pi}{\omega_c}\,\frac{V_{\rm dd}}{L_f} \tag{5.23}$$

To prevent the power from being delivered to the load when the power supply is $V_{\rm dd}$, in a fundamental period the average current flowing through the inductor L_f must be zero, i.e.

$$\frac{\omega_c}{2\pi}V_{\rm dd}\int_0^{2\pi/\omega_c}\bar{i}_f(t,V_{\rm dd})\,{\rm d}t=0 \tag{5.24}$$

This provides an interesting condition for the voltage $\overline{v}_{\rm sw}(t,V_{\rm dd})$. Integrating $\bar{i}_f(t,V_{\rm dd})$ in (5.21)–(5.22) leads to

$$\frac{1}{L_f}\iint_{2\pi/\omega_c}\overline{v}_{\rm sw}(t,V_{\rm dd})\,{\rm d}t^2=\frac{2\pi}{\omega_c}\bar{i}_f(0,V_{\rm dd}) \tag{5.25}$$

Therefore,

$$\begin{aligned}\frac{2\pi}{\omega_c}\,L_f\,\bar{i}_f(0,V_{\rm dd})=&\frac{\alpha_1}{\omega_a}\left[\frac{2\pi}{\omega_c}-\frac{1}{\omega_a}\sin(2\pi\omega_a/\omega_c)\right]+2\frac{\alpha_2}{\omega_a^2}\sin^2(\pi\omega_a/\omega_c)\\&+\frac{\alpha_3}{\omega_b}\left[\frac{2\pi}{\omega_c}-\frac{1}{\omega_b}\sin(2\pi\omega_b/\omega_c)\right]+2\frac{\alpha_4}{\omega_b^2}\sin^2(\pi\omega_b/\omega_c)\end{aligned} \tag{5.26}$$

Non-null input waveforms

When a non-null differential signal $\pm V_i$ is applied at the input terminals, the power at the fundamental frequency flowing into the load R_L should be non null as well. Despite the power-suppy values being symmetric,

due to switching at opposite phases, the currents through the load at such frequency need to be in phase and with an identical magnitude. The circuit in Fig. 5.3 is used here to simplify the analysis and the voltage at the load is assumed sinusoidal

$$v_o(t) = \widetilde{v}_o(t, V_i) = V_a \sin(\omega_c t) + V_b \cos(\omega_c t) \tag{5.27}$$

If this is not the case, then the energy efficiency due to V_i will never be 100 %. Hence, we will admit this hypothesis as long as no other finding contradicts it. Applying KCL to the remaining nodes of the circuit, for $0 \leq \omega_c t \leq \pi$ one obtains

$$\begin{aligned} \frac{\mathrm{d}^2 v_y(t, V_i)}{\mathrm{d}t^2} + \omega_{xy}^2 v_y(t, V_i) - \frac{1}{1 + C_y/C_x} \frac{\mathrm{d}^2 v_{\mathrm{sw}}(t, V_i)}{\mathrm{d}t^2} \\ = -\frac{1}{1 + C_y/C_x} \frac{\mathrm{d}^2 v_o(t, V_i)}{\mathrm{d}t^2} \end{aligned} \tag{5.28}$$

and

$$\begin{aligned} \frac{\mathrm{d}^2 v_{\mathrm{sw}}(t, V_i)}{\mathrm{d}t^2} + \omega_{fx}^2 v_{\mathrm{sw}}(t, V_i) - \frac{1}{1 + C_s/C_x} \frac{\mathrm{d}^2 v_y(t, V_i)}{\mathrm{d}t^2} \\ = \omega_{fx}^2 V_i + \frac{1}{1 + C_s/C_x} \frac{\mathrm{d}^2 v_o(t, V_i)}{\mathrm{d}t^2} \end{aligned} \tag{5.29}$$

with $\omega_{fx} = \omega_f \, \omega_{xy}/\omega_y = 1/\sqrt{L_f(C_s + C_x)}$. First, (5.28) is solved in respect to the term $\widetilde{v}_y(t, V_i)$, whereas (5.29) is solved due to $\mathrm{d}^2\widetilde{v}_y(t, V_i)/\mathrm{d}t^2$. The latter is replaced in the former, and then differentiated twice with respect to time. Both second derivatives are compared, using the equality to obtain a fourth-order differential equation in $\widetilde{v}_{\mathrm{sw}}(t, V_i)$, such as follows

$$\begin{aligned} \frac{\mathrm{d}^4 \widetilde{v}_{\mathrm{sw}}(t, V_i)}{\mathrm{d}t^4} + \left[\omega_f^2 + \omega_y^2\right] \frac{\mathrm{d}^2 \widetilde{v}_{\mathrm{sw}}(t, V_i)}{\mathrm{d}t^2} + \omega_z^4 \widetilde{v}_{\mathrm{sw}}(t, V_i) = \\ \frac{1}{1 + C_s/C_x + C_s/C_y} \frac{\mathrm{d}^4 \widetilde{v}_o(t, V_i)}{\mathrm{d}t^4} + \frac{\omega_y^2}{1 + C_s/C_x} \frac{\mathrm{d}\widetilde{v}_o^2(t, V_i)}{\mathrm{d}t^2} + \omega_z^4 V_i \end{aligned} \tag{5.30}$$

Admitting $\widetilde{v}_o(t, V_i)$ defined as in (5.27), the solution to (5.30) is

$$\begin{aligned} \widetilde{v}_{\mathrm{sw}}(t, V_i) = \gamma_1 \sin(\omega_a t) + \gamma_2 \cos(\omega_a t) \\ + \gamma_3 \sin(\omega_b t) + \gamma_4 \cos(\omega_b t) + V_i + \varpi \, \widetilde{v}_o(t, V_i), \quad 0 \leq \omega_c t \leq \pi \end{aligned} \tag{5.31}$$

with $\gamma_j = \Gamma_j(\lambda)$, $\lambda \in \Lambda$ and $j \in \{1, \ldots, 4\}$. The coefficient ϖ has been defined as

$$\varpi = \frac{\omega_c^2}{\omega_c^4 - \omega_c^2[\omega_f^2 + \omega_y^2] + \omega_z^4}\left[\frac{\omega_c^2}{1 + C_s/C_x + C_s/C_y} - \frac{\omega_y^2}{1 + C_s/C_x}\right] \quad (5.32)$$

During the remaining time $\widetilde{v}_{\rm sw}(t, V_i)$ is null, because of the switch activation. It should be emphasized the fact that the roots of the characteristic equation are the same as before for the null-input amplitude case. This implies that there are no exponential (decaying) terms in the homogeneous solution. Moreover an explicit term is found due to the load voltage, $\widetilde{v}_o(t, V_i)$. As for the voltage $\widetilde{v}_y(t, V_i)$, from the earlier development in (5.28)–(5.29), besides leading to (5.30) it also provides the following relationship

$$\begin{aligned}\widetilde{v}_y(t, V_i) = \frac{1}{\omega_{xy}^2}\left[\frac{C_x}{C_x + C_y} - \frac{C_x + C_s}{C_x}\right]\frac{\mathrm{d}^2\widetilde{v}_{\rm sw}(t, V_i)}{\mathrm{d}t^2} \\ + \frac{\omega_{fx}^2}{\omega_{xy}^2}\left[1 + \frac{C_s}{C_x}\right]\left[V_i - \widetilde{v}_{\rm sw}(t, V_i)\right] \\ + \frac{1}{\omega_{xy}^2}\frac{1}{1 + C_x/C_y}\frac{\mathrm{d}^2\widetilde{v}_o(t, V_i)}{\mathrm{d}t^2}, \quad 0 \le \omega_c t \le \pi \end{aligned} \quad (5.33)$$

Using (5.31) in (5.33) leads to

$$\begin{aligned}\widetilde{v}_y(t, V_i) = \delta_1\gamma_1 \sin(\omega_a t) + \delta_2\gamma_2 \cos(\omega_a t) + \delta_3\gamma_3 \sin(\omega_b t) \\ + \delta_4\gamma_4 \cos(\omega_b t) + \delta_a V_a \sin(\omega_c t) + \delta_b V_b \cos(\omega_c t), \quad 0 \le \omega_c t \le \pi \end{aligned} \quad (5.34)$$

with $\delta_1, \delta_2, \ldots, \delta_a, \delta_b$ as functions of $\lambda \in \Lambda$.

During a second switching phase, $\pi < \omega_c t \le 2\pi$, one can write

$$\begin{aligned}C_x\left[\frac{\mathrm{d}\widetilde{v}_o(t, V_i)}{\mathrm{d}t} + \frac{\mathrm{d}\widetilde{v}_y(t, V_i)}{\mathrm{d}t}\right] + \frac{1}{L_y}\int_{\pi/\omega_c}^{t} \widetilde{v}_y(t, V_i)\,\mathrm{d}t \\ + \widetilde{i}_y(\pi/\omega_c, V_i) + C_y\frac{\mathrm{d}\widetilde{v}_y(t, V_i)}{\mathrm{d}t} = 0 \end{aligned} \quad (5.35)$$

from which, following some basic manipulation, results in

$$\frac{\mathrm{d}^2\widetilde{v}_y(t, V_i)}{\mathrm{d}t^2} + \omega_{xy}^2\widetilde{v}_y(t, V_i) + \frac{1}{1 + C_y/C_x}\frac{\mathrm{d}^2\widetilde{v}_o(t, V_i)}{\mathrm{d}t^2} = 0 \quad (5.36)$$

with solution

$$\widetilde{v}_y(t,V_i) = \nu_1 \sin(\omega_{xy}[t-\pi/\omega_c]) + \nu_2 \cos(\omega_{xy}[t-\pi/\omega_c]) \\ - \frac{1}{1-\omega_{xy}^2/\omega^2}\frac{1}{1+C_y/C_x}\widetilde{v}_o(t,V_i), \quad \pi < \omega_c t \leq 2\pi \quad (5.37)$$

The current through the load can be obtained knowing the current flowing through C_x. At any time instant,

$$\frac{1}{C_x}\widetilde{i}_x(t,V_i) = \frac{\mathrm{d}\widetilde{v}_{\mathrm{sw}}(t,V_i)}{\mathrm{d}t} - \frac{\mathrm{d}\widetilde{v}_y(t,V_i)}{\mathrm{d}t} - \frac{\mathrm{d}\widetilde{v}_o(t,V_i)}{\mathrm{d}t} \quad (5.38)$$

One obvious restriction is that the dc voltage across the two inductors must be null. Hence, the average voltage is obtained as

$$\int_0^{2\pi/\omega_c} \widetilde{v}_y(t,V_i)\,\mathrm{d}t = 0 \quad (5.39)$$

Moreover, the inductors are in parallel with capacitors at both switching phases. As such, since by definition no dc currents can flow through C_y, the average value of the derivative of $\widetilde{v}_y$ is zero, i.e.

$$\int_0^{2\pi/\omega_c} \frac{\mathrm{d}\widetilde{v}_y(t,V_i)}{\mathrm{d}t}\,\mathrm{d}t = 0 \quad (5.40)$$

The unknowns ν_1 and ν_2 in (5.37) are derived using (5.27), (5.31), (5.34) and (5.37) in (5.38), and applying the two conditions above, namely (5.39) and (5.40). The following short notation is used here for the result

$$\nu_1 = \widehat{\nu}_{11}\gamma_1 + \widehat{\nu}_{12}\gamma_2 + \widehat{\nu}_{13}\gamma_3 + \widehat{\nu}_{14}\gamma_4 + \widehat{\nu}_{1a}V_a + \widehat{\nu}_{1b}V_b \quad (5.41)$$

$$\nu_2 = \widehat{\nu}_{21}\gamma_1 + \widehat{\nu}_{22}\gamma_2 + \widehat{\nu}_{23}\gamma_3 + \widehat{\nu}_{24}\gamma_4 + \widehat{\nu}_{2a}V_a + \widehat{\nu}_{2b}V_b \quad (5.42)$$

These can be used back in (5.37) to write the current $\widetilde{i}_x(t,V_i)$ with a short format. For the on state, the terms in (5.37) can be rearranged and rewritten as follows

$$\widetilde{i}_x(t,V_i) = \{q_{11}\gamma_1 + q_{12}\gamma_2 + q_{13}\gamma_3 + q_{14}\gamma_4 + q_{1a}V_a + q_{1b}V_b\}\sin[\omega_{xy}(t-\pi/\omega_c)] \\ + \{q_{21}\gamma_1 + q_{22}\gamma_2 + q_{23}\gamma_3 + q_{24}\gamma_4 + q_{2a}V_a + q_{2b}V_b\}\cos[\omega_{xy}(t-\pi/\omega_c)] \\ + q_aV_a\cos(\omega_c t) + q_bV_b\sin(\omega_c t), \qquad \pi < \omega_c t \leq 2\pi \quad (5.43)$$

in which a straightforward relationship has been established between q_k and $\widehat{\nu}_k$, $\forall k$. As for the off state, similarly,

$$\widetilde{i}_x(t,V_i) = p_1\gamma_1\cos(\omega_a t) + p_2\gamma_2\sin(\omega_a t) + p_3\gamma_3\cos(\omega_b t) + p_4\gamma_4\sin(\omega_b t) + p_a V_a\cos(\omega_c t) + p_b V_b\sin(\omega_c t), \quad 0 \le \omega_c t \le \pi \tag{5.44}$$

As only the fundamental component of $\widetilde{i}_x(t,V_i)$ flows through the load resistance, one can impose[1]

$$\frac{\omega_c}{\pi}\int_0^{2\pi/\omega_c}\widetilde{i}_x(t,V_i)\sin(\omega_c t)\,\mathrm{d}t = \frac{V_a}{2R_L} \tag{5.45}$$

$$\frac{\omega_c}{\pi}\int_0^{2\pi/\omega_c}\widetilde{i}_x(t,V_i)\cos(\omega_c t)\,\mathrm{d}t = \frac{V_b}{2R_L} \tag{5.46}$$

From the conditions above, the magnitudes V_a and V_b can be derived and expressed in terms of $\gamma_1,\ldots,\gamma_4$ as the only unknowns,

$$V_a = a_1\gamma_1 + a_2\gamma_2 + a_3\gamma_3 + a_4\gamma_4 \tag{5.47}$$

$$V_b = b_1\gamma_1 + b_2\gamma_2 + b_3\gamma_3 + b_4\gamma_4 \tag{5.48}$$

The relationships above are replaced in (5.31) to denote an explicit dependence on $\gamma_1,\ldots,\gamma_4$. Similar boundary conditions to the previous case can be applied now, i.e. due to ZVS and taking into consideration the average voltage value at the switching nodes

$$\widetilde{v}_{\mathrm{sw}}(0,V_i) = 0 \tag{5.49}$$

$$\widetilde{v}_{\mathrm{sw}}(\pi/\omega_c,V_i) = 0 \tag{5.50}$$

$$\int_0^{\pi/\omega_c}\widetilde{v}_{\mathrm{sw}}(t,V_i)\,\mathrm{d}t = 2\pi V_i/\omega_c \tag{5.51}$$

resulting in the following three equations

$$\gamma_1 = \gamma_{14}\gamma_4 + \gamma_{1i}V_i \tag{5.52}$$

$$\gamma_2 = \gamma_{24}\gamma_4 + \gamma_{2i}V_i \tag{5.53}$$

$$\gamma_3 = \gamma_{34}\gamma_4 + \gamma_{3i}V_i \tag{5.54}$$

[1] An equivalent load of $2R_L$ is used here because just one side of the differential PA is actually being considered in the analysis; in other words, $i_x(t)$ is half of the total current $i_{x_1}(t) + i_{x_2}(t)$, and the same applies to the respective fundamental components (see Fig. 5.3).

The relationships above are replaced in (5.34) and (5.37) after ν_1, ν_2, V_a and V_b being replaced as functions of $\gamma_1, \ldots, \gamma_4$. This will provide a way to obtain γ_4. Since at steady state, due to the continuity on the voltage when transiting between off and on switch states (with the capacitor loop), the following additional condition must be satisfied

$$\widetilde{v}_y(\pi/\omega_c^-, V_i) = \widetilde{v}_y(\pi/\omega_c^+, V_i) \tag{5.55}$$

As such, the voltages $\widetilde{v}_{\text{sw}}(t, V_i)$ and $\widetilde{v}_y(t, V_i)$ can now be rewritten in terms of an only unknown, γ_4. When the switch is deactivated

$$\begin{aligned}\widetilde{v}_{\text{sw}}(t, V_i) = &\Big\{[a_4{+}a_1\gamma_{14}{+}a_2\gamma_{24}{+}a_3\gamma_{34}]\gamma_4 + [a_1\gamma_{1i}{+}a_2\gamma_{2i}{+}a_3\gamma_{3i}]V_i\Big\}\varpi\sin(\omega_c t)\\ &+ \Big\{[b_4{+}b_1\gamma_{14}{+}b_2\gamma_{24}{+}b_3\gamma_{34}]\gamma_4 + [b_1\gamma_{1i}{+}b_2\gamma_{2i}{+}b_3\gamma_{3i}]V_i\Big\}\varpi\cos(\omega_c t)\\ &+ V_i + \Big\{\gamma_{14}\gamma_4 + \gamma_{1i}V_i\Big\}\sin(\omega_a t) + \Big\{\gamma_{24}\gamma_4 + \gamma_{2i}V_i\Big\}\cos(\omega_a t)\\ &+ \Big\{\gamma_{34}\gamma_4 + \gamma_{3i}V_i\Big\}\sin(\omega_b t) + \gamma_4\cos(\omega_b t), \qquad 0 \le \omega_c t \le \pi\end{aligned} \tag{5.56}$$

and

$$\begin{aligned}\widetilde{v}_y(t, V_i) = &\,\delta_a\Big\{[a_4{+}a_1\gamma_{14}{+}a_2\gamma_{24}{+}a_3\gamma_{34}]\gamma_4 + [a_1\gamma_{1i}{+}a_2\gamma_{2i}{+}a_3\gamma_{3i}]V_i\Big\}\sin(\omega_c t)\\ &+ \delta_a\Big\{[b_4{+}b_1\gamma_{14}{+}b_2\gamma_{24}{+}b_3\gamma_{34}]\gamma_4 + [b_1\gamma_{1i}{+}b_2\gamma_{2i}{+}b_3\gamma_{3i}]V_i\Big\}\cos(\omega_c t)\\ &+ \delta_1\Big\{\gamma_{14}\gamma_4 + \gamma_{1i}V_i\Big\}\sin(\omega_a t) + \delta_2\Big\{\gamma_{24}\gamma_4 + \gamma_{2i}V_i\Big\}\cos(\omega_a t)\\ &+ \delta_3\Big\{\gamma_{34}\gamma_4 + \gamma_{3i}V_i\Big\}\sin(\omega_b t) + \delta_4\gamma_4\cos(\omega_b t), \quad 0 \le \omega_c t \le \pi\end{aligned} \tag{5.57}$$

When the switch is on, $\widetilde{v}_{\text{sw}}(t, V_i)$ is null, and

$$\begin{aligned}\widetilde{v}_y(t, V_i) = &\,[\mu_a\nu_{1a} + \mu_b\nu_{1b} + \mu_{1i}]\sin(\omega_{xy}[t - \pi/\omega_c])\\ &+ [\mu_a\nu_{2a} + \mu_b\nu_{2b} + \mu_{2i}]\cos(\omega_{xy}[t - \pi/\omega_c])\\ &- \frac{C_x}{C_x + C_y}\frac{\omega_c^2}{\omega_c^2 - \omega_{xy}^2}\widetilde{v}_o(t, V_i), \quad \pi < \omega_c t \le 2\pi\end{aligned} \tag{5.58}$$

with

$$\mu_a = a_1(\gamma_{14}\gamma_4{+}\gamma_{1i}V_i) + a_2(\gamma_{24}\gamma_4{+}\gamma_{2i}V_i) + a_3(\gamma_{34}\gamma_4{+}\gamma_{3i}V_i) + a_4\gamma_4 \tag{5.59}$$

$$\mu_b = b_1(\gamma_{14}\gamma_4{+}\gamma_{1i}V_i) + b_2(\gamma_{24}\gamma_4{+}\gamma_{2i}V_i) + b_3(\gamma_{34}\gamma_4{+}\gamma_{3i}V_i) + b_4\gamma_4 \tag{5.60}$$

and, for $k \in \{1, 2\}$,

$$\mu_{ki} = \nu_{k1}(\gamma_{14}\gamma_4+\gamma_{1i}V_i)+\nu_{k2}(\gamma_{24}\gamma_4+\gamma_{2i}V_i)+\nu_{k3}(\gamma_{34}\gamma_4+\gamma_{3i}V_i)+\nu_{k4}\gamma_4 \quad (5.61)$$

For the output voltage, $\forall t$ we have the following expression

$$\widetilde{v}_o(t, V_i) = \rho(a)\sin(\omega_c t) + \rho(b)\cos(\omega_c t) \quad (5.62)$$

where $\rho(a)$ and $\rho(b)$ are given by

$$\rho(r) = r_1(\gamma_{14}\gamma_4+\gamma_{1i}V_i)+ r_2(\gamma_{24}\gamma_4+\gamma_{2i}V_i)+r_3(\gamma_{34}\gamma_4+\gamma_{3i}V_i)+r_4\gamma_4 \quad (5.63)$$

with $r \in \{a, b\}$. Let us now focus our attention on the current $\widetilde{i}_f(t, V_i)$, i.e.

$$\begin{aligned}\widetilde{i}_f(t, V_i) = {} & \frac{\gamma_1}{\omega_a L_f}\cos(\omega_a t) - \frac{\gamma_2}{\omega_a L_f}\sin(\omega_a t) + \frac{\gamma_3}{\omega_b L_f}\cos(\omega_b t) - \frac{\gamma_4}{\omega_b L_f}\sin(\omega_b t) \\ & + \frac{\varpi}{\omega_c L_f}\Big[V_a\cos(\omega_c t) - V_b\sin(\omega_c t)\Big] + \varepsilon_1, \qquad 0 \le \omega_c t \le \pi \quad (5.64)\end{aligned}$$

in which (5.31) has been applied within the integration in time, hence resulting in the constant ε_1. During the closed state of the switch one can find $\widetilde{i}_f(t, V_i)$ as

$$\widetilde{i}_f(t, V_i) = V_i\frac{t - \pi/\omega_c}{L_f} + \varepsilon_2, \quad \pi < \omega_c t \le 2\pi \quad (5.65)$$

From the continuity of current, $\widetilde{i}_f(0, V_i) = \widetilde{i}_f(2\pi/\omega_c, V_i)$,

$$[\varepsilon_2 - \varepsilon_1]L_f = \frac{\gamma_1}{\omega_a} + \frac{\gamma_3}{\omega_b} + \frac{\varpi}{\omega_c}V_a - \frac{\pi}{\omega_c}V_i \quad (5.66)$$

An one-hundred percent efficiency implies that all power due to a non-null voltage V_i to be delivered to $2R_L$, that is, $P_{\text{in}} = P_{\text{out}}$, where

$$P_{\text{in}} = \frac{\omega_c}{\pi}V_i\int_0^{2\pi/\omega_c}\widetilde{i}_f(t, V_i)\,\mathrm{d}t \quad (5.67)$$

where the dc current provided by the power supply considers symmetry and that only the phases differ, $\widetilde{i}_{f_1}(t) = -\widetilde{i}_{f_2}(t - \pi/\omega_c) = \widetilde{i}_f(t)$, and

$$P_{\text{out}} = \frac{1}{2}\frac{V_a^2 + V_b^2}{2R_L} \quad (5.68)$$

leading to ϵ_1 defined as follows

$$\epsilon_1 = \frac{1}{2\pi\omega_c L_f \omega_a^2 \omega_b^2}\left\{u_i V_i + u_a V_a + u_b V_b + 2\sum_{k=1}^{4}(-1)^k u_k \gamma_k\right\} + \frac{2P_{\text{out}}}{V_i} \quad (5.69)$$

where

$$\begin{cases} u_i = \pi^2 \omega_a^2 \omega_b^2 \\ u_a = -2\pi\omega_a^2 \omega_b^2 \varpi \\ u_b = 4\omega_a^2 \omega_b^2 \varpi \end{cases} \quad (5.70)$$

and

$$\begin{cases} u_1 = \omega_c \omega_b^2 \left[\pi\omega_a + \omega_c \sin(\pi\omega_a/\omega_c)\right] \\ u_2 = \omega_c^2 \omega_b^2 \left[1 - \cos(\pi\omega_a/\omega_c)\right] \\ u_3 = \omega_c \omega_a^2 \left[\pi\omega_b + \omega_c \sin(\pi\omega_b/\omega_c)\right] \\ u_4 = \omega_c^2 \omega_a^2 \left[1 - \cos(\pi\omega_b/\omega_c)\right] \end{cases} \quad (5.71)$$

These and the remaining functions derived in this section have been verified with Mathematica (Wolfram Research),with the scripts provided in Appendix B.

Computation of the device values

As previously referred, the design of the proposed circuit involves multiple objectives, such as ZVS, null power consumption at $V_i = 0$, etc. These and other criteria have been applied to determine the solution of the fourth-order differential equation that characterizes the switch voltages. Nonetheless, the design space is not reduced to a single point. To compute the component values, an optimization methodology is required, that is, an optimization approach able to solve multi-objective problems with multiple variables. Genetic algorithms using Matlab (MathWorks) tools have been chosen to find a Pareto set providing the component values. For the present optimization, let us recall the design set λ formerly specified. Moreover, one defines $\vec{F} : \Lambda \to \mathbb{R}^{4\times 1}$, $\lambda \mapsto [f_1(\lambda), f_2(\lambda), f_3(\lambda), f_4(\lambda)]^T$. Using a genetic algorithm, one aims to find

$$\min_{\lambda \in \Lambda} \vec{F}(\lambda) \quad (5.72)$$

subject to positive-valued components, which is already contemplated in the definition of the design set Λ. The fitness function $\vec{F}(\lambda)$ comprises the following sub-functions

$$f_1(\lambda) = \int_{2\pi/\omega_c}^{0} \frac{\min\{\overline{v}_{\rm sw}(t, V_{\rm dd}), 0\}}{|\overline{v}_{\rm sw}(t, V_{\rm dd})|}\, {\rm d}t \tag{5.73}$$

$$f_2(\lambda) = \left| \overline{v}_y(\pi/\omega_c^+, V_{\rm dd}) - \overline{v}_y(\pi/\omega_c^-, V_{\rm dd}) \right| \tag{5.74}$$

$$f_3(\lambda) = \int_{2\pi/\omega_c}^{0} \frac{\min\{\widetilde{v}_{\rm sw}(t, V_i), 0\}}{|\widetilde{v}_{\rm sw}(t, V_i)|}\, {\rm d}t \tag{5.75}$$

$$f_4(\lambda) = 1 - P_{\rm out}(V_i)/P_{\rm in}(V_i) \tag{5.76}$$

Both the conditions (5.73) and (5.75) denote the ratio between negative and positive portions of the voltage waves $\overline{v}_{\rm sw}(t, V_{\rm dd})$ and $\widetilde{v}_{\rm sw}(t, V_i)$, respectively. Hence, at an optimum point λ^*, there will be no negative values for these waveforms, i.e. null for both: $f_1(\lambda^*) \approx 0$ and $f_3(\lambda^*) \approx 0$. As for the second function, $f_2(\lambda)$ denotes the continuity of $v_y(t)$ during off-on transition. One should note that this has not been explicitly used as a boundary condition in the previous analysis. Finally, in (5.76) the losses are represented through the use of $P_{\rm in}(V_i)$ and $P_{\rm out}(V_i)$ as given in (5.67) and (5.68), respectively.

The fundamental purpose here is to demonstrate the validity of the proposed topology within the C-P architecture. Hence, the value of R_L has been fixed at $50\,\Omega$, which avoids additional impedance matching networks and also reduces the number of decision variables (to 5). In fact, for a given load, there are several possible solutions that differ in the fundamental current through the load. That is, even though the problem restrictions are satisfied, different solutions provide different gains $V_{\rm out}/V_i$. To validate the proposed topology, one will just focus on one of those possible solutions (with $50\,\Omega$ as the load, for simplicity). Table 5.1 shows a set of component values obtained after running the genetic algorithms in Matlab with the conditions (5.73)–(5.76). Some additional circuit parameters are listed in Table 5.2.

Table 5.1: Component values for a design example (normalized to 1 MHz).

R_L	40	50	60	70	Ω
C_s	1,190	1,206	1,192	1,193	pF
C_x	508	526	535	549	
C_y	1,081	1,089	1,093	1,086	
C_0†	39,789	31,831	26,526	22,736	
L_y	6,356	6,374	6,395	6,420	nH
L_f	9,927	9,816	9,963	10,042	
L_0†	637	796	955	1,114	

†used in simulation only: $Q_L = \omega_c R_L C_0 = R_L/(\omega_c L_0) = 10$;

Table 5.2: Parameter values for the design example using the values listed in Table 5.1.

$R_L\,(\Omega)$	40	50	60	70
ω_f/ω_c	1.29	1.29	1.28	1.28
ω_y/ω_c	1.67	1.65	1.65	1.65
ω_z^2/ω_c^2	2.04	2.02	2.00	2.00
ω_a/ω_c	1.76	1.75	1.74	1.74
ω_b/ω_c	1.62	1.15	1.15	1.15
ω_{xy}/ω_c	1.58	1.57	1.56	1.56
ω_{fx}/ω_c	1.22	1.22	1.21	1.21
ϖ	-0.83	-0.88	-0.95	-1.05
P_{out} (mW)†	0.69	0.88	1.03	1.17

†$V_{\text{dd}} = 1.0\,\text{V}, V_i = 0.5\,\text{V}$;

5.2 Simulation Results

The values listed in Table 5.1 have been used in the circuit of Fig. 5.2, designed with ideal components using Cadence Virtuoso software. Simulations were performed using Spectre RF with PSS analysis. Fig. 5.4 shows some relevant results for the voltage and current waveforms with fixed $V_i = 0$. Reasonable matching is obtained between the analysis and simulation results.

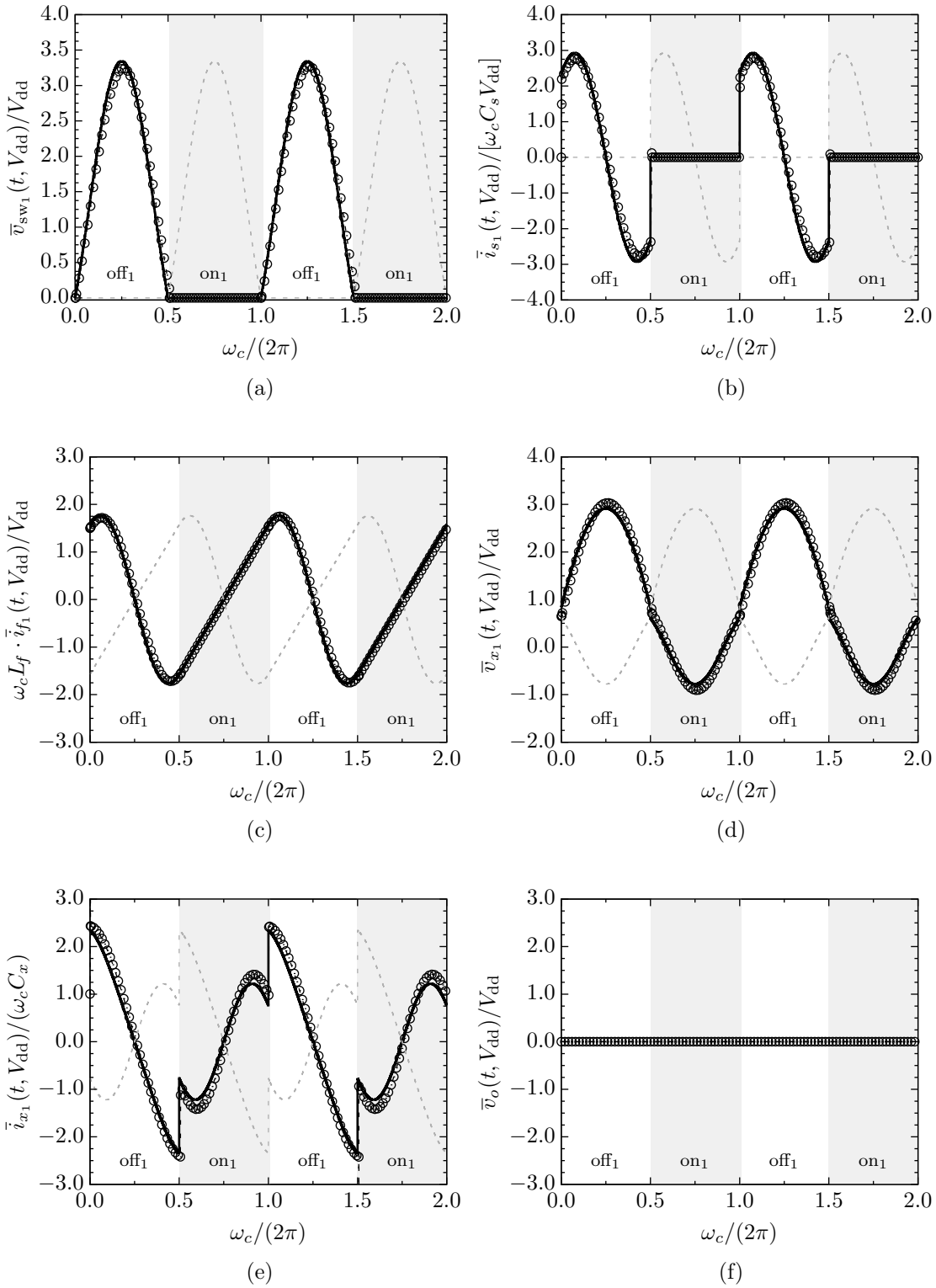
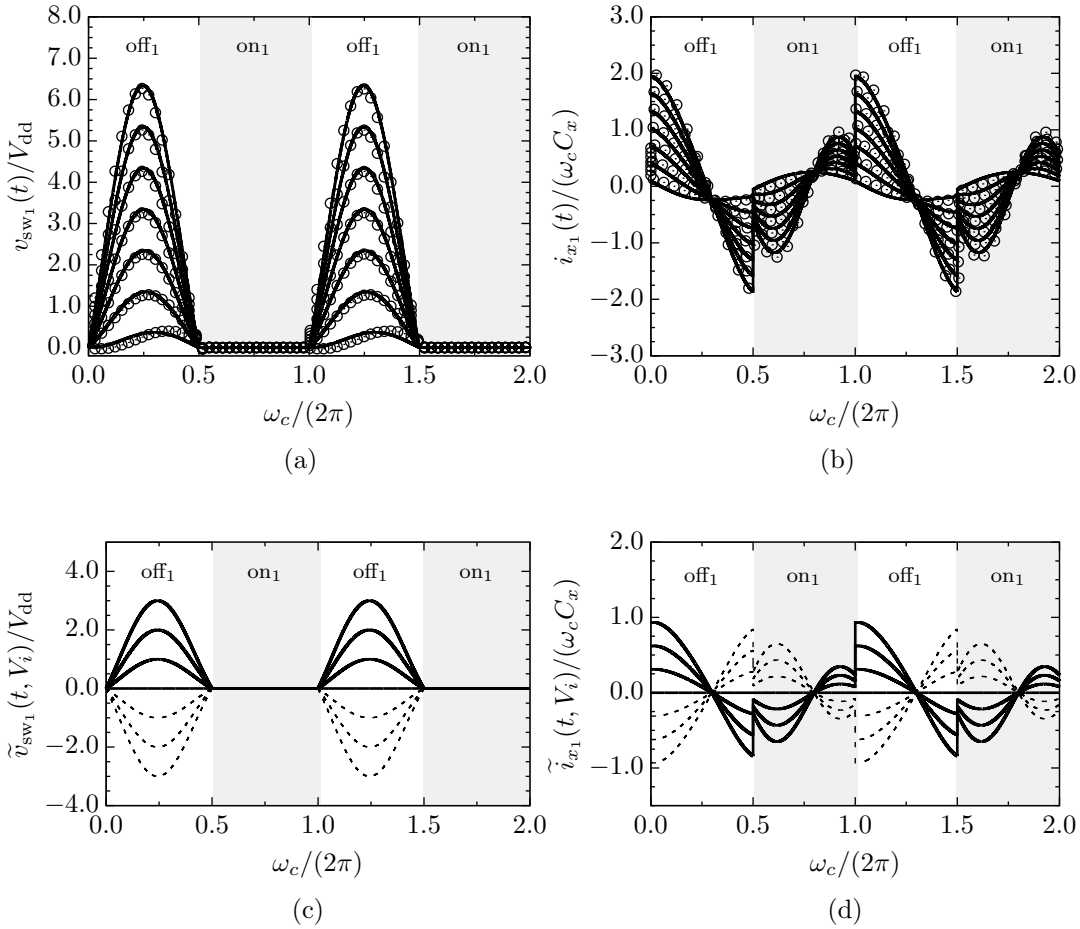
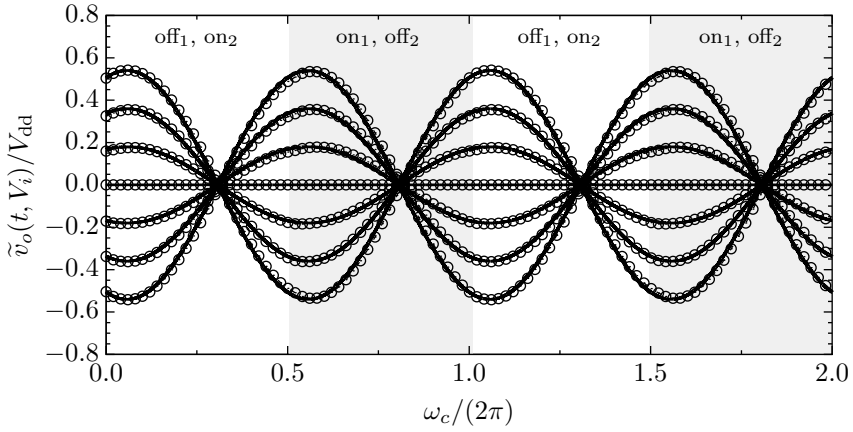


Figure 5.4: Voltage and current waveforms when $V_i = 0$. The solid line represents the analysis results and, for easier comparison, the dashed line represents the analytical result during the opposite phase (at the other drain terminal). The points "∘" represent simulation data.

It is interesting to note that, although $v_{\mathrm{sw}}(t)$ is formed by two resonance frequencies relatively distant (1.75 and 1.15 related to ω_c, as given in Table 5.2), the resultant waveforms at the drains are nearly sinusoidal with half rectification. As such, the peak voltage at each drain is considerably high, i.e. about three times ($\sim \pi \times V_{\mathrm{dd}}$) as in other SMPAs. However, there is no relationship with other PA classes, since for common-mode operation no power flows to the load – Fig. 5.4(f). A finite amount of energy just flows from one side to the other and is kept constant due to ZVS.

Let us consider the differential-mode operation, hence, admitting now $V_i \neq 0$. Fig. 5.5 shows some simulation results together with plots of some functions obtained along the analysis. The voltage V_i has been swept from $-0.9/V_{\mathrm{dd}}$ to $+0.9/V_{\mathrm{dd}}$, in $0.3/V_{\mathrm{dd}}$ steps.





(e)

Figure 5.5: Voltage and current waveforms when $V_i \neq 0$. Similarly to the previous figure, the solid line represents the analysis results and the points "∘" represent simulation data. The analysis results with null $V_{\rm dd}$ are also included, in which the dashed lines represent the negative V_i sweep.

In Figs. 5.5(a) and 5.5(b), the analysis results for the differential mode have been added to the common mode, with the latter previously represented in Figs. 5.4(a) and 5.4(e). The respective analysis results for the isolated differential mode are seen in Figs. 5.5(c) and 5.5(d). As shown, one of the first assumptions is verified, that is $v_{\rm sw_1}(t) = \overline{v}_{\rm sw_1}(t, V_{\rm dd}) + \widetilde{v}_{\rm sw_1}(t, V_i)$ and, similarly, this superposition is also valid for the current $i_{x_1}(t)$.

With all the circuit conditions assumed ideal, one should verify if the response to V_i and $V_{\rm dd}$ variations are not just narrow in frequency, due to infinite quality factors of the components. In typical conditions, it is desired that V_i has a low-pass characteristic and there is not just a narrow band where the common-mode is rejected. To verify the frequency behavior of the proposed circuit, the components are still assumed ideal and a periodic AC (PAC) analysis is performed – which is a small signal analysis with the circuit linearized about an operation point that varies at fundamental frequency [187]. Both $V_{\rm dd}$ and V_i have been swept in frequency, but independently. The results are shown in Fig. 5.6, where it is evident that the $V_{\rm dd}$ excitation is rejected ($\sim 38\,\text{dB}$) along a large frequency range,

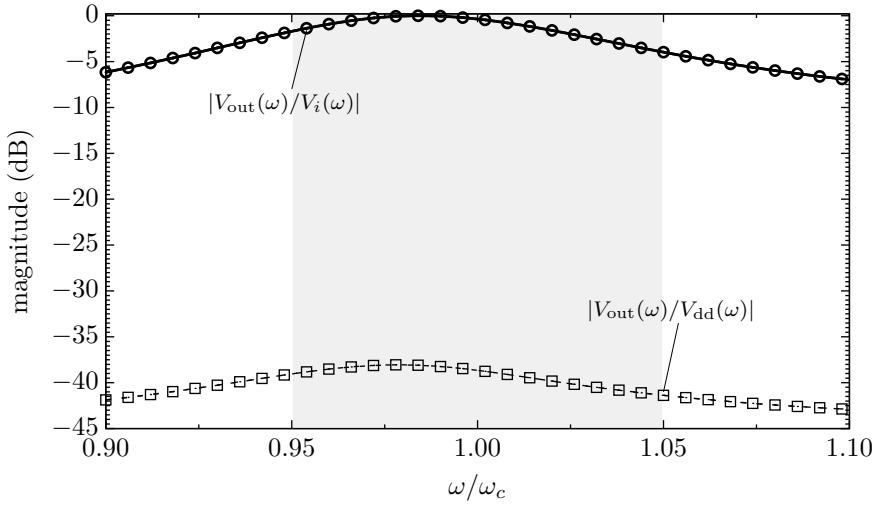
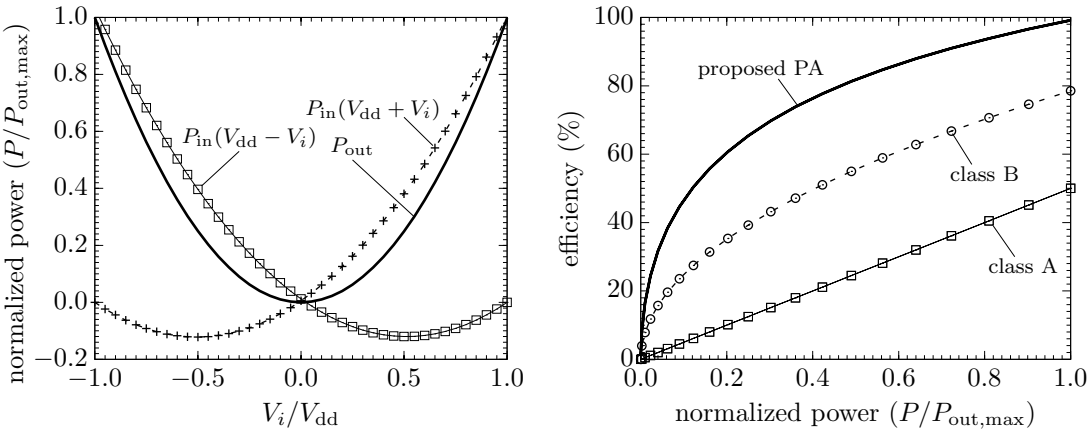


Figure 5.6: Frequency response to common and differential modes (normalized to the peak of V_i).

as well as the differential mode amplified in a bandwidth similar to that defined by the LC filter at the output – the shadowed region in Fig. 5.6 represents the frequency within the bandwidth defined by $\omega_c/(2\pi Q_L)$.

So far, the derived equations characterizing the circuit behavior have been demonstrated. Figs. 5.4 and 5.5 show that some of the items from the wish list in page 105 are accomplished. Specifically, it should be clear that, in the proposed switching-mode PA: the voltages at any of the two drain terminals are always non-negative (if assuming an adequate V_{dd}, i.e. $V_{\text{dd}} > V_i$); and ZVS can be ensured regardless of the V_i level. However, some issues related with the power efficiency are yet to be verified. Based also in simulation results, one can verify that (ideally) the power consumption at null V_i is zero. However, when the input is non-null, the efficiency might be subject to two possible interpretations. This is because one of the voltage sources receives power from the other. As such, there are implications on the value determined for the efficiency. For instance, if one considers two batteries, with different voltages, one charges the other. In fact, simulation results have shown that the efficiency is close to 1.0, with a vertical asymptote at $V_i = 0$. Although such might be seem interesting for physical reasons, quite often this is not the case because only one power



(a) (b)

Figure 5.7: Theoretical efficiency of the proposed differential PA – (a) power delivered to the load, and power flowing into L_f (see Fig. 5.2); (b) energy efficiency and comparison with other PAs for reference.

source supplies the complete circuit. Thus, the power through the terminal with less voltage will be associated to a power loss. In this case, adopting the current and voltage notations applied in the circuit of Fig. 5.2, the efficiency is given by

$$\tilde{\eta}(V_i) = \frac{P_{\text{out}}}{P_1 + P_2} \tag{5.77}$$

where

$$P_1 = \frac{2\pi}{\omega_c} \int_0^{2\pi/\omega_c} (V_{\text{dd}} + V_i)\, i_{f_1}\, \mathrm{d}t \quad \Leftarrow \quad P_1 \geq 0 \tag{5.78}$$

$$P_2 = \frac{2\pi}{\omega_c} \int_0^{2\pi/\omega_c} (V_{\text{dd}} - V_i)\, i_{f_2}\, \mathrm{d}t, \quad \Leftarrow \quad P_2 \geq 0 \tag{5.79}$$

and $P_1 = 0$ or $P_2 = 0$, respectively if any of the expressions above lead to a negative result.

Fig. 5.7 shows simulation results from the sweep of V_i from $-V_{\text{dd}}$ up to $+V_{\text{dd}}$. In Fig. 5.7(a), it is evident that while one side is providing all the power, the other one behaves as a load (since its power is negative). The worst case is at mid scale when $V_i = \pm V_{\text{dd}}/2$ and, on the other hand, at peak power one of the two sides has a null potential and wastes no power at all – thus, leading to the maximum efficiency. In Fig. 5.7(b), (5.77) is plotted based on the simulation values. The results are quite favorable to

the differential PA, with relatively higher energy efficiency along all the power range.

All the previous analysis assumed perfect matching between the devices. In practice, that is rarely the case; for instance: common tolerances for SMT passive devices are in the order of $\pm 1\,\%$ to $\pm 5\,\%$. For a more realistic scenario, let us assume a normal distribution for each of the passive devices depicted in Fig. 5.2, as well as for R_{on} of the switching devices. Each of the fifteen devices admits a normal PDF centered at the nominal values shown in Table 5.1, whereas for R_{on} about $100\,\text{m}\Omega$ is assumed as the central value. Each device value is spread out according to a common target in quality control, which is the tolerance associated with the $\pm 6\,\sigma$ limits [188, 189]. For the present demonstration purposes, the tolerance is set at $\pm 5\,\%$ for all the components, and 256 values are generated for each device according to their normal PDFs. Using Ocean/SKILL scripting with Cadence Virtuoso, 256 simulations have been performed. Fig. 5.8 shows the complementary cumulative PDFs for the efficiency when V_i is $+V_{\text{dd}}$ and $-V_{\text{dd}}$, as well as P_{out} (normalized to the typical) for both cases. The results reveal that $\sim 80\,\%$ of the samples have more than $94\,\%$ efficiency, and P_{out} is less sensitive to the bipolarity of V_i than the efficiency.

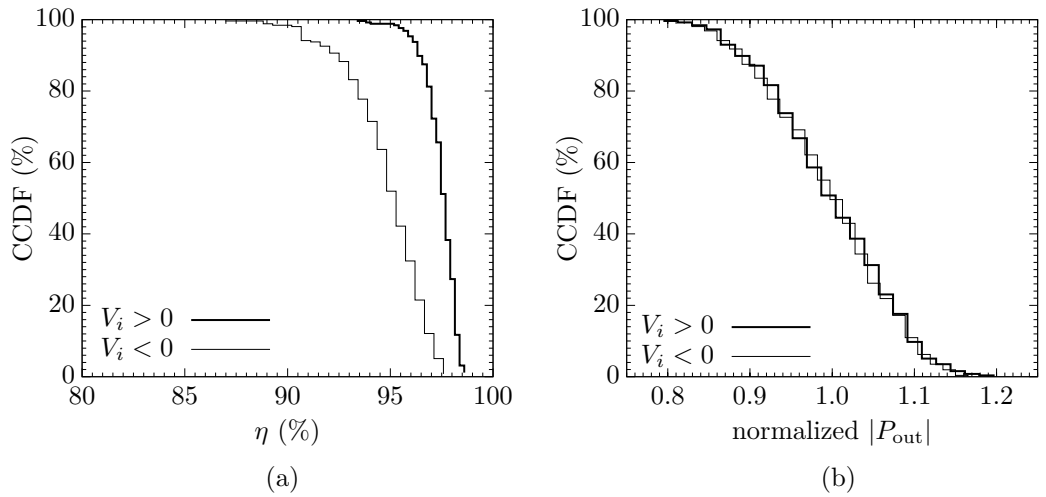


Figure 5.8: CCDF for the efficiency of the differential PA due to asymmetries.

5.2.1 Design example

As an illustrative example, this section presents the design of a differential PA and a C-P transmitter, using the proposed topology with simulation models of commercial-grade devices. The RF transistor used in this example consists of an LDMOS device from Freescale Semiconductor, which is the MRF6V2010N – an N-channel enhancement-mode transistor for operation up to frequencies of 450 MHz and 10 W peak output power. The nonlinear model MET [190], provided by Freescale, has been used within the Agilent-ADS environment (2009-U1) to design a transmitter for 220 MHz operation frequency. Such value nearly coincides with the frequency limit for which the capacitor C_s is fully replaced by the shunt capacitor of the transistor ($\sim 5.5\,\text{pF}$) assuming the load as $50\,\Omega$. Fig. 5.9 shows the complete setup of the proposed circuit. A combiner with lumped elements has been designed as in section 4.1, with the devices defined by (4.1)–(4.2), now at the central frequency of 220 MHz. All the remaining passive devices depicted in Fig. 5.9 are described in Table 5.3 with the respective value chosen for this design.

Table 5.3: Nominal values for the devices in the design of the differential PA operating at 220 MHz.

system component	device		units	manufacturer/reference
differential PA	L_f	47	nH	Coilcraft/1515SQ
	L_y	30		Coilcraft/1111SQ
	C_x	2.4	pF	ATC/CDR11-D
	C_y	5.1		
input matching	L_m	39	nH	Coilcraft/1008HQ
	L_b	1.2	μH	
	C_m	27	pF	ATC/CDR11-F
	C_c	100		
LC output	L_0	9	nH	Coilcraft/1508
	C_0	51	pF	ATC/CDR11D
output combiner	C_1	10	pF	ATC/CDR11-F
	C_2	20		
	L_1	51	nH	Coilcraft/0805HQ
	R_Δ	49.9	Ω	AVX/CR21-1%

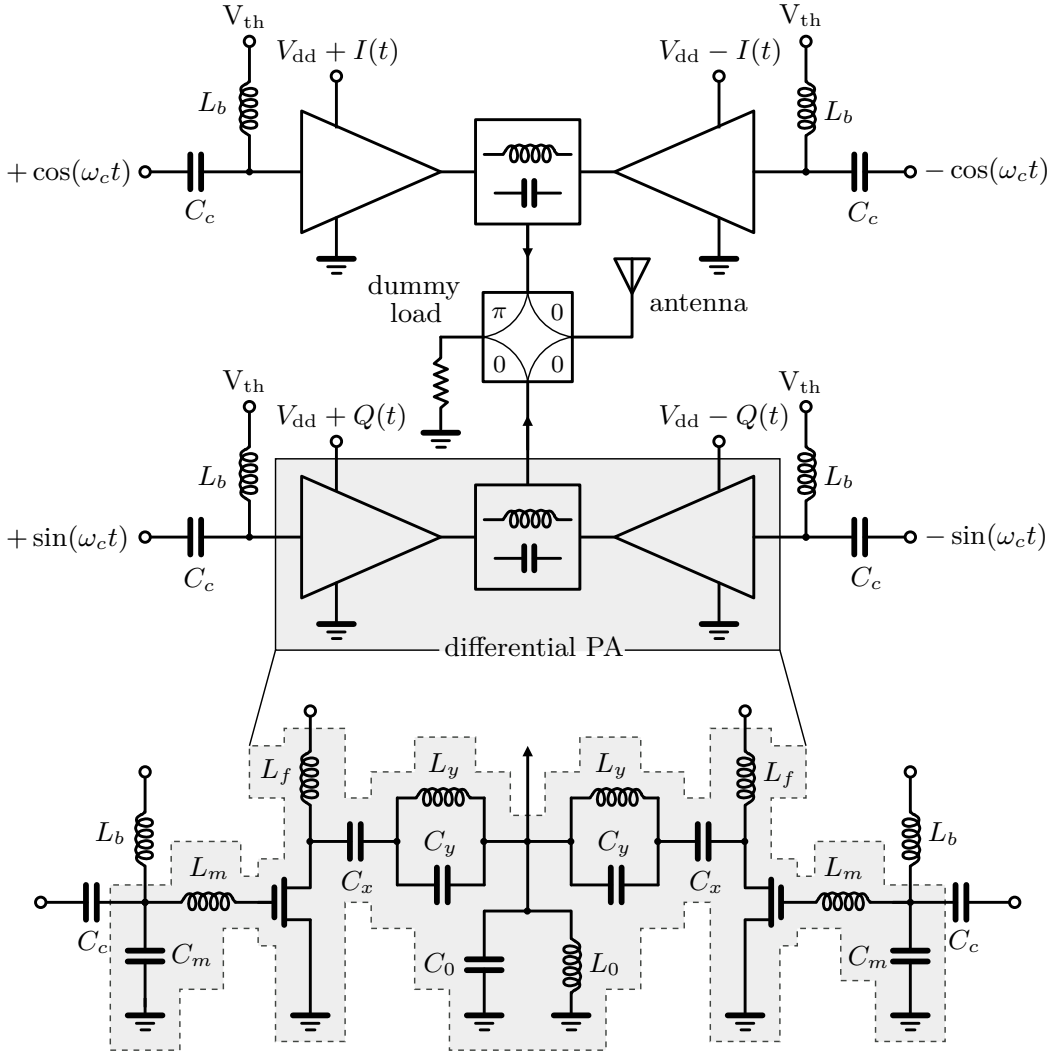


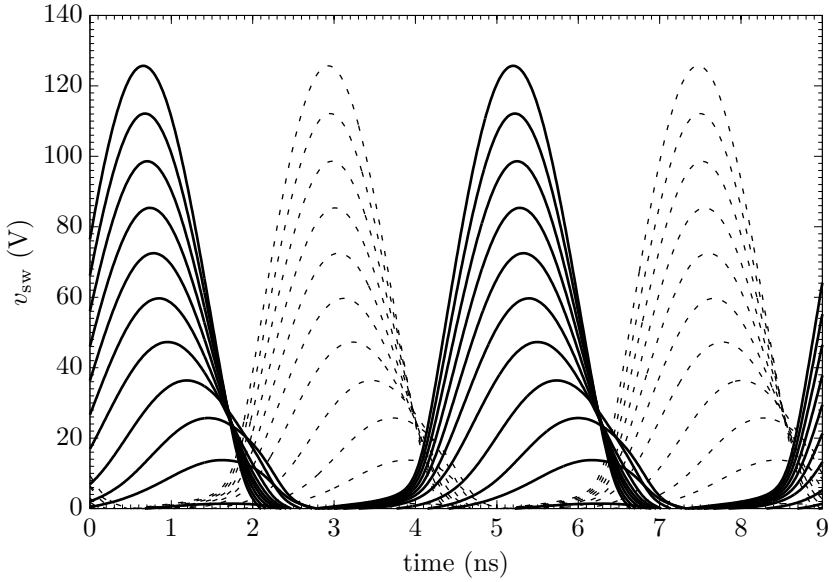
Figure 5.9: Schematic of the full CP transmitter with differential PAs.

The design is based on the component values presented in Table 5.1, with 50 Ω as the chosen load to avoid additional matching networks. The capacitors are porcelain multilayer devices from American Technical Ceramics Corp. (100A series, 250 V dc rating), whereas the inductors are from several series from Coilcraft, selected according to their quality factor, self resonance frequency and current rating required for the circuit. At the input, the transistors have been matched to $50\,\Omega + j0$ (at $V_i = 0\,\mathrm{V}$) with an L network (upward) formed by C_m and L_m – the latter also absorbs the negative reactance seen into the gate of the transistor. The transistors are

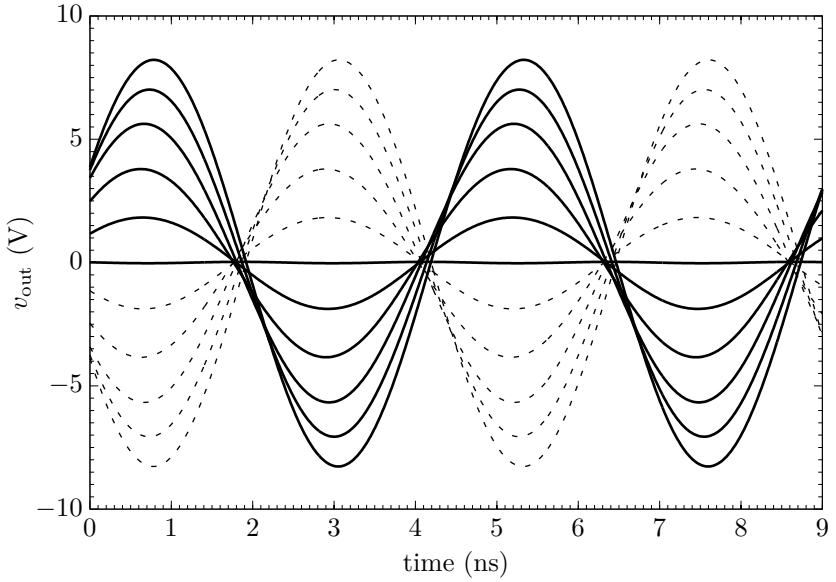
biased at their threshold voltage (1.68 V) to provide 50 % switching ratios. The mid-range power supply has been fixed to $V_{\mathrm{dd}} = 21\,\mathrm{V}$. This imposes the maximum voltage swing[2], i.e. each differential signal can go from -21 up to 21 V. The peak power at each differential-PA output is 31.5 dBm, which should be almost the same as the output power level because half of the power is dissipated at the dummy load. The input signals are provided by two 180-degree hybrid couplers (to obtain the antipodal signals), driven by a 90-degree coupler with a single voltage source operating at 220 MHz. For clarity of representation of the remaining system, these elements are omitted in the circuit of Fig. 5.9. As for the output, due to the band-pass frequency response inherent to the combiner, the output LC network can be relaxed in terms of Q_L, which has been designed as ~ 4.

The differential PA has been simulated with the combiner as a load, using the harmonic balance simulator from Agilent ADS. Fig. 5.10(a) depicts the drain voltage waveforms obtained at the differential PA. Each plotted line corresponds to a different V_i level, obtained sweeping $\pm V_i$ as a dc voltage source superimposed to a fixed value of V_{dd}. The solid lines correspond to a drain terminal with power-supply $V_{\mathrm{dd}} + V_i$, whereas the dashed lines correspond to the other drain terminal with a symmetrical V_i, i.e. $V_{\mathrm{dd}} - V_i$. As such, for the solid lines the peak voltage increases with V_i, whereas in the dashed counterpart the peak increases with $-V_i$. This means that, at the limit, the outermost lines correspond to the power-supply voltages of $2V_{\mathrm{dd}}$ and 0 V. Fig. 5.10(b) depicts the time-domain waveforms at the summing port of the output combiner. For the present example, both PAs used the same power supply, which means that $V_i = I = Q$. The solid lines correspond to a positive V_i, whereas the dashed lines are associated with negative values. The difference port presents identical waveforms (not shown), but with $\pi/2$ phase difference.

[2]It is worth mentioning that due to the bipolarity of V_i, the power-supply range has to accommodate both positive and negative parts of the signal, thus, the voltage range is virtually reduced to a half – as a result, it also restricts the output power to a quarter of its maximum.



(a)



(b)

Figure 5.10: Time domain waveforms – (a) drain voltage for the differential PA in the in-phase path; (b) output waveforms at the summing terminal.

An immediate consequence from the usage of nonideal devices is that the power generated at null V_i is no longer zero (although P_{out} still being null). This produces a shift in the power behavior of the dynamic power

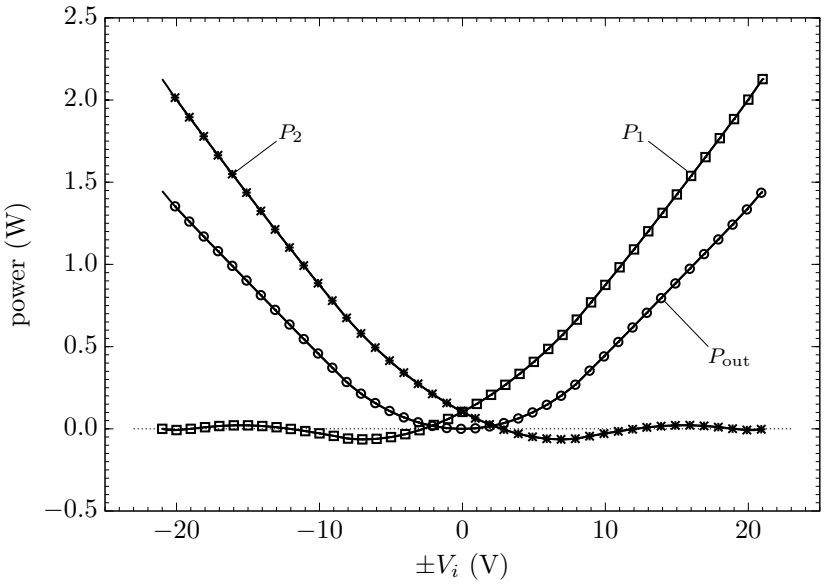


Figure 5.11: Power generated (P_1 and P_2) in the I side, and power at the output (P_{out}).

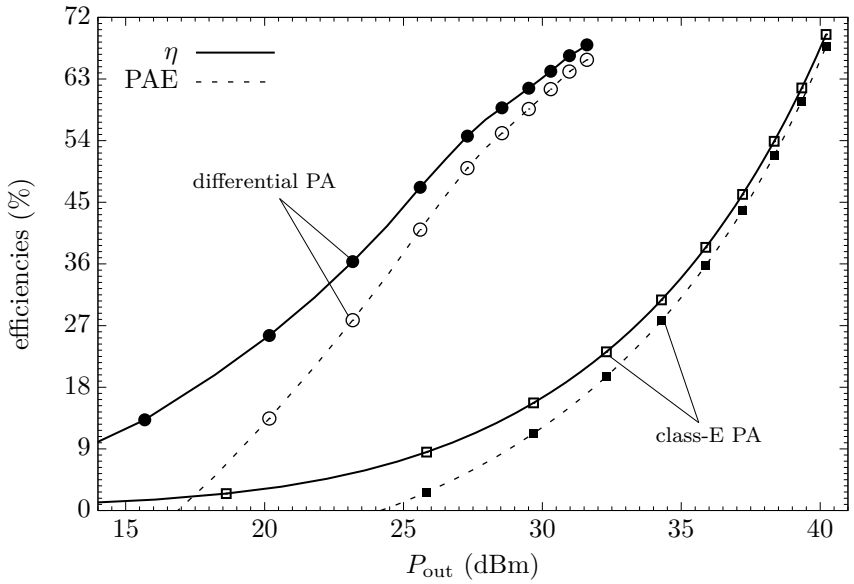


Figure 5.12: Efficiencies of the differential PA and LINC.

supply, i.e. the waveforms in Fig. 5.7(a) are changed to those of Fig. 5.11, with less negative components but increased power consumption. Fig. 5.12 shows the efficiency of the differential PA with the combiner as its load, and the output power obtained at the combiner input. This is compared with the efficiency performance of a class-E PA, designed with the same active

device, also at the frequency of operation 220 MHz. In the present case, the class E is less restrictive in terms of output power – it has been designed to achieve 40 dBm using the power supply of 48 V and 38 Ω as optimum load, matched to 50 Ω by means of an impedance matching network. In the case of the differential PA, no power output maximization has been performed previously with genetic algorithms. Hence, the peak output powers in both PAs still differ in about 8.5 dB, although denoting similar peak efficiencies (close to $\sim$ 70 %). It is also worth mentioning that in the LINC transmitter the class-E PA operates always at its peak power, whereas the differential PA suffers from an efficiency decline with higher B-O levels. In both cases, the most significant power loss is the LDMOS transistor itself, and in the differential PA only, a secondary potential loss mechanism is at the inductor L_f that must be chosen very carefully to prevent excessive power dissipation (even when $V_i = 0$) due to a high ESR.

Let us now take into consideration both the magnitude and phase, at the fundamental frequency at the output of the combiner. For a voltage sweep along the line $V_i = I = Q$ with V_i admitting values from $-V_{\mathrm{dd}}$ up to $+V_{\mathrm{dd}}$, Figs. 5.13(a) and 5.13(b) show, respectively, the magnitude and phase for the signal obtained at the summing port. The phase has been intentionally shifted up 180° for easier inspection on the nonlinearity. Further improvements can be achieved introducing digital predistortion, such as in other architectures for wireless standards with stringent linearity demands – e.g. [22, 50, 53].

Fig. 5.14 shows the comparison between the efficiency of the C-P transmitter using a differential PA and the LINC, with the output power of the LINC normalized to the peak power of the C-P transmitter. To represent all the possible power levels at the output, the power supply of the C-P transmitter has been swept as previously, between $V_i = -V_{\mathrm{dd}}$ and $V_i = +V_{\mathrm{dd}}$ based on $I = Q$, and for the LINC the outphasing angle has been varied between 0 and $\pi/2$. Along the sweep of V_i with V_{dd} fixed to 21 V, the efficiency of the C-P architecture is only superior to the LINC

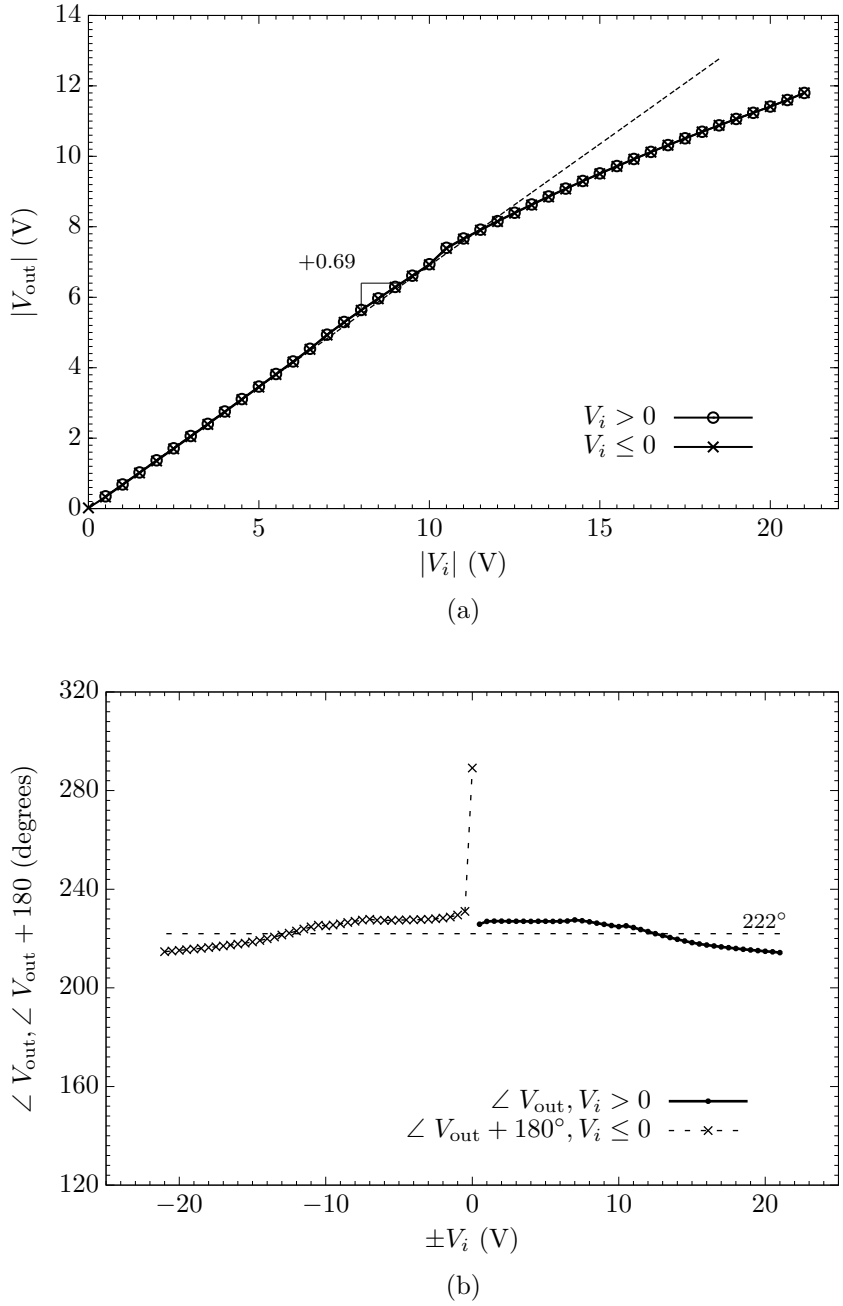


Figure 5.13: Voltage magnitude and phase for the proposed differential PA.

transmitter from minimum output levels to about 4 dB in the B-O from peak power. However, within this interval the difference is just a bit more than residual. In fact, this is a consequence of the 50 % of power being wasted in power combination of the signals in quadrature, which is signifi-

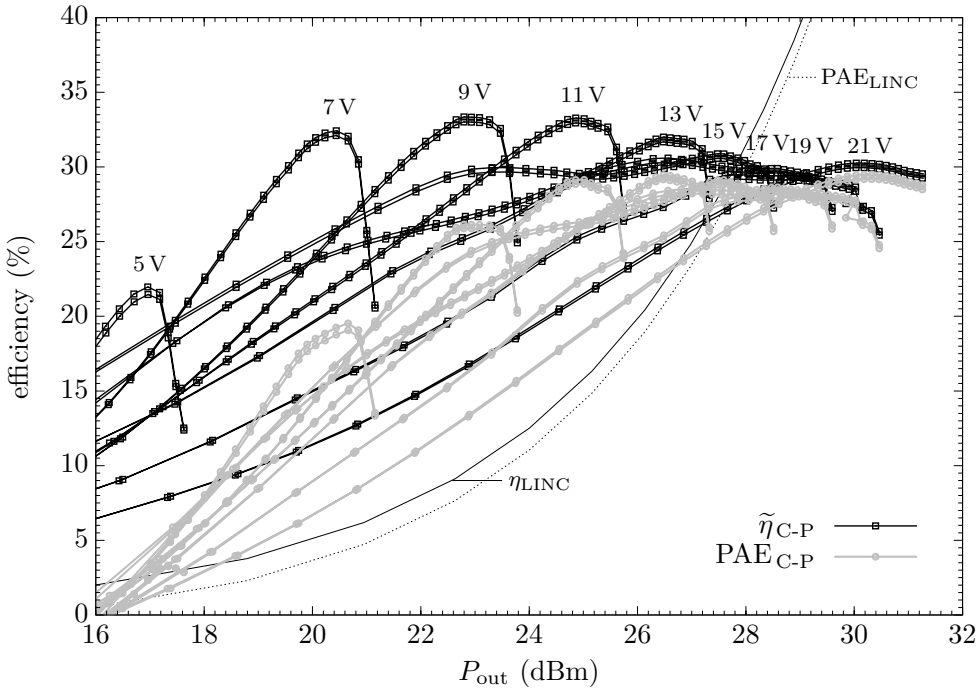


Figure 5.14: Simulation results for the efficiency.

cant. As such, it implies the usage of power recycling techniques to really take significant advantage of the differential topology. Additionally, since one of the most relevant features of the proposed PA is the rejection of common-mode components of the power supply, some V_{dd} reduction can be applied depending on the envelope levels. This has been referred earlier as one of the items from the initial list of requirements. It consists on imposing a time-varying V_{dd} similarly to an ET system but for baseband signals or, to be precise, two of those systems with one for the I and the other for the Q counterparts. Despite of an increased complexity, tracking $I(t)$ and $Q(t)$ results in quite significant improvements on the drain and power-added efficiencies. The value of V_{dd} has been swept in accordance to the value of V_i, that is: for each common-mode voltage V_{dd} fixed between 5 and 21 V in steps of 2 V, the value of V_i has been swept from zero to slightly above each V_{dd} value. In Fig. 5.14 the efficiencies are plotted for the differential PA against the LINC (with its power normalized). Clearly,

close to the PEP the LINC transmitter depicts much higher efficiency than the C-P transmitter (up to $\sim 4\,\mathrm{dB}$ of B-O). However, along a wide range of power output levels, in the C-P transmitter the drain efficiency is kept high (over almost $15\,\mathrm{dB}$), while the power losses in the LINC architecture increase substantially. Nevertheless, the average efficiency for one or the other architecture still depends on the characteristics of the baseband signals that, presently, have the general tendency to higher PAPRs.

Chapter 6

Conclusion

A new RF transmitter architecture has been presented in this dissertation, entitled "Cartesian-Polar (C-P) transmitter". The main purpose of the proposed architecture is to obtain high energy efficiency with switching-mode PAs, as in a typical polar transmitter, but without sacrificing the signal bandwidths in the envelope amplifiers. To circumvent this limitation, a structure inspired in the Cartesian architecture has been adopted, operating with $I(t)$ and $Q(t)$ as bipolar signals at the outputs of the envelope amplifiers. Consequently, the bandwidth requirements for these amplifiers are much more relaxed than in typical architectures operating with unipolar signals. One particular feature of this new transmitter is that its overall efficiency is ideally preserved at 50 % regardless of the B-O level. This means that, whenever the signals are lower than one half of the peak power at the output, the ideal C-P transmitter tends to superior performances in efficiency when compared to the conventional LINC transmitter.

In the present work, two C-P circuits have been proposed for the implementation of the C-P transmitter. One of the circuits consists of a CMOS topology suitable for low-power portable devices. The proposed topology for the CMOS PA relies on the negative bias of the body, to allow the negative excursion of the signals at the drain/source terminals. This, however, denotes some power limitations due to reliability issues related with excessive potential between gate and channel or across the *pn* junctions.

The second circuit is less confined in technology and application, as it can make use of any RF semiconductor with source and body interconnected. In this topology, the envelope is applied as a differential signal with some positive offset imposing the common-mode voltage. Such common mode ensures a positive drain voltage with null contribution to the output and, still, the ZVS condition occurs at any power-supply level, with relatively high efficiency at the differential mode.

In this dissertation, the two topologies have been validated as switching-mode solutions for the proposed C-P architecture. The present work is a contribution to the development of efficient transmitters in high-PAPR regimes. The C-P transmitter is a promising solution for communication standards where the LINC is unlikely to be employed. For instance, LINC applications are often limited to low-PAPR modulations, which avoid zero crossings in the IQ constellation, e.g. $\pi/4$-DQPSK. In contrast, in the proposed transmitter the trajectory through zero is less problematic. Both large PAPR signals and instantaneous null magnitudes can be handled without additional restrictions. As such, the characteristics of the proposed C-P architecture are in accordance with the properties of common RF signals found in actual and emerging modulation schemes.

6.1 Recommendations for Future Work

The first recommendation emphasis a potential interest for the investigation of power-recycling circuits for the proposed architecture. It has been shown that the C-P architecture benefits more from power recycling than a LINC transmitter using the same mechanism. However, in spite of the resemblances in output structure, the power recycling in the C-P transmitter is a lot more ambitious. Besides requiring two rectifiers, one for each quadrature branch, the recycling scheme must be bidirectional. As an example, when $I(t)$ is negative the only way to recover some energy is

to source current from the power-supply, whereas when $I(t)$ is positive the power-supply must sink current from the power combiner. Additionally, the rectification circuits must provide the input impedance of $50\,\Omega + j0$ at any power level. Nonetheless, the research work in this topic is justified by the theoretical improvements in efficiency above the ideal 50% with an adequate power-recycling scheme.

Another possible research direction is to explore a middle ground solution, with a bidirectional polar amplifier. When used as a standalone amplifier, the proposed differential PA denotes a relatively high performance in efficiency – see Fig. 5.7(b). An interesting possibility is then to explore the PA topology as a polar transmitter, where the gate signals are $\pm\cos[\omega_c t \pm \phi'(t)]$ and, as drain modulation, the differential signal $V_{\mathrm{dd}} \pm A'(t)$. This way, comparing to the proposed C-P transmitter, the efficiency is no longer reduced to a half. The signals $\phi'(t)$ and $A'(t)$ need to be related accordingly to phase reversals, but this alleviates the problem of spectral regrowth due to the phase/envelope delay mismatching that is typical in the polar transmitter. With this new scheme such problem should be less pronounced because of the V_{dd} offset, which eases the zero crossings. Additionally, the tracking of the envelope with a time varying offset, as proposed in this dissertation, can still be used with the same purpose, which provides the efficiency improvement at lower power output requirements.

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Acronyms and Abbreviations

ACI Adjacent Channel Interference

ACPR Adjacent-Channel Power Ratio

ADPLL All-Digital PLL

ADS Advanced Design System

AM Amplitude Modulation

B-O Back-Off

BD BreakDown

BiCMOS Bipolar-CMOS co-integration

BPF Band-Pass Filter

BSIM Berkeley Short-channel IGFET Model

C-P Cartesian-Polar

CCDF Complementary Cumulative Distribution Function

CDMA Code-Division Multiple Access

CMOS Complementary Metal-Oxide Semiconductor

CORDIC COordinate Rotation DIgital Computer

DAC Digital-to-Analog Converter

DCO Digitally-Controlled Oscillator

DAB Digital Audio Broadcasting

dc Direct Current

DCS Digital Cellular System

DIBL Drain Induced Barrier Lowering

DPD Digital PreDistortion

DQPSK Differential QPSK

DSP Digital Signal Processor

DVB Digital Video Broadcasting

EDGE Enhanced Data rates for GSM Evolution

EER Envelope Elimination and Restoration

EM ElectroMagnetic

EMI EM Interference

ESR Equivalent Series Resistance

ET Envelope Tracking

EVM Error Vector Magnitude

FIR Finite Impulse Response

FM Frequency Modulation

F-N Fowler-Nordheim

FPGA Field-Programmable Gate Array

FSK Frequency-Shift Keying

GaAs Gallium Arsenide

GaN Gallium Nitride

GFSK Gaussian FSK

GPRS General Packet Radio Service

GPS Global Positioning System

GSM Global System for Mobile communications

HB Harmonic Balance

HBT Heterojunction Bipolar Transistor

HC Hot Carriers

HSDPA High-Speed Downlink Packet Access

HSUPA High-Speed Uplink Packet Access

I In-phase

I-V Current-to-voltage

IC Integrated Circuit

IEEE Institute of Electrical and Electronics Engineers

IF Intermediate Frequency

IGFET Insulated Gate Field Effect Transistor

IMD$_3$ InterModulation Distortion of 3$^{\text{rd}}$ order

IQ Cartesian

IS-95 Interim Standard 95

ISI Intersymbol Interference

KCL Kirchhoff's Circuit Laws

LAN Local Area Network

LDMOS Laterally Diffused MOS

LDO Low-DropOut

LINC Linear Amplification using Nonlinear Components

LO Local Oscillator

LPF Low-Pass Filter

LTE Long Term Evolution

LTV Linear Time Variant

LUT Look-up Table

MET Motorola Eletro Thermal model

MOS Metal-Oxide Semiconductor

MOSFET MOS Field-Effect Transistor

NMOS N-channel MOS

NQS Non-Quasi Static

O-QPSK Offset QPSK

OFDM Orthogonal Frequency Division Multiplexing

PA Power Amplifier

PAC Periodic AC

PAE Power-Added Efficiency

PAPR Peak-to-Average Power Ratio

PDF Probability Density Function

PEP Peak Envelope Power

PER Packet Error Rate

PLL Phase-Locked Loop

PM Phase Modulation

PMOS P-channel MOS

PSD Power Spectrum Density

PSK Phase-Shift Keying

PSS Periodic Steady State (simulation analysis)

PWM Pulse-Width Modulation

Q Quadrature

QAM Quadrature Amplitude Modulation

QPSK Quadrature PSK

rms Root Mean Square

RF Radio Frequency

SCS Signal Component Separator

SMPA Switching-Mode PA

SMPS Switching-Mode Power Supply

SMT Surface-Mount Technology

TDDB Time-Dependent Dielectric Breakdown

Tx Transmitter

UMTS Universal Mobile Telecommunications System

UTRA UMTS Terrestrial Radio Access

UWB Ultra-Wide Bandwidth

VGA Variable-Gain Amplifier

W-CDMA Wide-band CDMA

WBET WideBand ET

WiFi Wi-Fi Alliance trademark

WiMAX Worldwide Interoperability for Microwave Access

ZVDS Zero-Voltage Derivative Switching

ZVS Zero-Voltage Switching

Appendix A

I-V Model for MOSFET devices including Short-Channel Effects

In the strong inversion regime, the well-know expression for the drain current of a long-channel NMOS device is given by the Shichman and Hodges model [166], that is

$$i_{\mathrm{DS}} = \tfrac{1}{2}\,\mu_{\mathrm{eff}}\,C_{\mathrm{ox}}\tfrac{W}{L}\,(v_{\mathrm{GS}} - V_{\mathrm{th}})\,v_{\mathrm{DS,sat}} \tag{A.1}$$

where v_{GS} is the gate-to-source voltage, and V_{th} is the threshold voltage. The term $v_{\mathrm{DS,sat}}$ is the pinch-off voltage, i.e. $v_{\mathrm{DS,sat}} = v_{\mathrm{GS}} - V_{\mathrm{th}}$, which leads to the typical quadratic behavior in long-channel devices. The other parameters correspond to the width and effective length of the gate, respectively W and L, electron mobility μ_{eff} at low-field inversion layer ($\approx 0.06\,\mathrm{m}^2/\mathrm{V/s}$), and gate capacitance per unit area C_{ox}, which is given by $C_{\mathrm{ox}} = \epsilon_0\epsilon_r/t_{\mathrm{ox}}$ with $\epsilon_0 = 8.854 \times 10^{-12}\,\mathrm{F/m}$ and $\epsilon_r = 3.9$ for $\mathtt{SiO_2}$, and t_{ox} the gate-oxide thickness that is technology dependent.

Among other effects, the operation of short-channel MOS devices is subject to velocity saturation. The mobility of electrons (in NMOS, or holes in PMOS devices) is degraded with stronger electric fields applied to the channel[1]. These effects cannot be ignored in present MOS technologies,

[1] "Short-channel effects" are not strictly related with channel length. In true, these are due to high electric fields on the channel, which can also be due to either reduced t_{ox}, or high supply voltage. Obviously, with present scaling trends, the term "short-channel effects" makes sense.

i.e. Eq. (A.1) is no longer valid as the I-V relationship looses its quadratic behavior. Instead, the dc current reveals a linear dependence on the gate overdrive. Hence, for $v_{\rm DS} > v_{\rm DS,sat}$, the static current can be written as [167, 191, 192]

$$i_{\rm DS} = \nu_{\rm sat} C_{\rm ox} W \left(V_{\rm GS} - V_{\rm th} - v_{\rm DS,sat}\right) \tag{A.2}$$

where $\nu_{\rm sat}$ is the velocity saturation. Here the term $v_{\rm DS,sat}$ is no longer the pinch-off voltage. In short-channel devices, $v_{\rm DS,sat}$ is related with the voltage at which the carriers saturate their mobility. This can be written shortly as

$$v_{\rm DS,sat} = \left(v_{\rm GS} - V_{\rm th}\right) \| E_c L \tag{A.3}$$

where E_c represents the critical electric field for which the carriers drop to half of their mobility, i.e. obtained from [193]

$$\nu = \begin{cases} \frac{\mu_{\rm eff} E}{1+E/E_c} & \Leftarrow \quad E \leq E_c \\ \nu_{\rm sat} & \Leftarrow \quad E \geq E_c \end{cases} \tag{A.4}$$

Typical values for E_c are around 4 and $12\,{\rm V}/\mu{\rm m}$ for NMOS and PMOS, respectivelly [194]. Applying (A.3) in (A.2), and $E_c = 2\,\nu_{\rm sat}/\mu_{\rm eff}$, results after some manipulation

$$\begin{aligned} i_{\rm DS} &= \nu_{\rm sat} C_{\rm ox} W \frac{\left(V_{\rm GS} - V_{\rm th}\right)^2}{V_{\rm GS} - V_{\rm th} + E_c L} \\ &= \tfrac{1}{2} \mu_{\rm eff} C_{\rm ox} \frac{W}{L} \frac{\left(V_{\rm GS} - V_{\rm th}\right)^2}{1 + \left(V_{\rm GS} - V_{\rm th}\right)/(E_c L)}, \qquad v_{\rm DS} > v_{\rm DS,sat} \end{aligned} \tag{A.5}$$

As for the triode region, one can write the drain current as [167]

$$i_{\rm DS} = K \frac{\left(v_{\rm od} - v_{\rm DS}/2\right) v_{\rm DS}}{1 + v_{\rm DS}/(E_c L)}, \qquad v_{\rm DS} < v_{\rm DS,sat} \tag{A.6}$$

In (A.6), the term $v_{\rm od}$ represents the overdrive voltage, $v_{\rm od} = v_{\rm GS} - V_{\rm th}$, and $K = \mu_n C_{\rm ox} W/L$ is the device transconductance. This can still be written in a much simpler form for both triode and strong inversion regions, such as follows

$$i_{\rm DS} = \begin{cases} K \left(v_{\rm od} - \frac{1}{2} v_{\rm DS}\right) \left(v_{\rm DS} \| E_c L\right) \left(1 + \lambda v_{\rm DS}\right) & \Leftarrow \quad v_{\rm DS} < v_{\rm DS,sat} \\ \frac{1}{2}\, K\, v_{\rm od} \left(v_{\rm od} \| E_c L\right) \left(1 + \lambda v_{\rm DS}\right) & \Leftarrow \quad \text{otherwise} \end{cases} \tag{A.7}$$

The relationships in (A.7) already include channel-length modulation, λ. Moreover, the relationships above are valid for $v_{\mathrm{od}} \geq 0$. For $v_{\mathrm{GS}} < V_{\mathrm{th}}$, the current i_{DS} is assumed to be null (i.e., weak inversion is herein neglected).

Other effects to account for are due to vertical mobility reduction, typically denoted as θ, which is inversely proportional to t_{ox}. The value of θ ranges from 0.1 to $0.4\,\mathrm{V}^{-1}$ for $t_{\mathrm{ox}} \approx 100\,\text{Å}$ [195]. If included, it would be as affecting the mobility similar to velocity saturation. The reduction can be written as [194]

$$\mu_{\mathrm{eff}} = \frac{\mu_n}{1 + \theta\left[v_{\mathrm{GS}} - V_{\mathrm{th}}\right]} \tag{A.8}$$

It is actually noticeable how the short-channel effects are incompatible with the formulation used for long-channel devices. Indeed, some simulations with such a model have shown how relevant was the inclusion of the velocity saturation to properly represent the triode region, and consequently the transition into strong inversion as well. However, in the present model, both the moderate and weak inversion regions were not properly modeled, due to simplicity issues. Furthermore, it should be noted that the current model also does not take into account an eventual body effect. As for a long-channel device, the threshold voltage can be related as

$$V_{\mathrm{th}} = V_{\mathrm{th0}} + \gamma\left(\sqrt{|v_{\mathrm{SB}} - 2\phi_{\mathrm{F}}|} - \sqrt{|2\phi_{\mathrm{F}}|}\right) \tag{A.9}$$

with ϕ_{F} as the Fermi potential, v_{SB} the source-to-bulk potential, γ the body effect parameter, and V_{th0} the threshold voltage with source and bulk tied together, i.e. $v_{\mathrm{SB}} = 0$. Nevertheless, when improved accuracy is demanded for the value of V_{th}, particularly in the case of short-channel devices, one should also consider the influence of W, L, as well as v_{DS} due to DIBL. In the present work the compactness of (A.9) suffices, due to minor impact of V_{th} in the performance of the proposed circuit topologies.

Appendix B

Scripts for the Derivation of the Differential-PA Waveforms

This section provides two Mathematica scripts (version 6.0) to assist the derivation of the waveforms in the differential circuit proposed in Chapter 5, both for common and differential modes.

B.1 Common Mode

```
ClearAll[Global`*]
vswt=Vdd+A1 Sin[wa t]+A2 Cos[wa t]+A3 Sin[wb t]+A4 Cos[wb t];
vswt0=vswt/.t→0;
vswtT=vswt/.t→π/w;
vswtD=∫_0^(π/w) vswt dt;
S1=Collect[Flatten[FullSimplify[Solve[{vswt0==0,vswtT==0,vswtD==2πVdd/w},
   {A1,A2,A3}]]],A4];
vlyon=B1 Sin[wxy(t−π/w)]+B2 Cos[wxy(t−π/w)];
vlyoff=1/wy^2 (1+Csh/Cx)(wf^2 Vdd−∂t ∂t vswt−wf^2 vswt);
vxtoff=vswt−vlyoff;
vxon=−vlyon;
idvly=(vlyoff/.t→π/w)−(vlyoff/.t→π/w)+(vlyon/.t→2π/w)−(vlyon/.t→π/w);
ivly=∫_0^(π/w) vlyoff dt+∫_(π/w)^(2π/w) vlyon dt;
S2=Flatten[FullSimplify[Solve[{idvly==0,ivly==0},{B1,B2}]]];
vloffs=vlyoff/.S1;
vlyons=vlyon/.S2;
vlyofft0=vlyoffs/.t→0;
```

vlyofft2=vlyoffs/.t→$\frac{\pi}{w}$;

vlyont=vlyons/.t→$\frac{2\pi}{w}$;

vlyont2=vlyons/.t→$\frac{\pi}{w}$;

Q=$\frac{Vdd(2\pi/w)^2}{4Lf}-\frac{1}{Lf}\int_0^{\frac{\pi}{w}}\left(\int_0^t(vswt/.S1)\,dt\right)dt+2*Cx(vlyofft0-vlyofft2+vlyont-vlyont2)$;

S3=FullSimplify[Solve[Q==0,A4]]

isoff=Csh ∂_tvswt;

ixoff=Cx ∂_tvxtoff;

ixon=Cx ∂_tvxon;

iloff=ixoff+isoff;

ilofft2=iloff/.t→$\frac{\pi}{w}$;

ilon=$\frac{Vdd\,t}{Lf}$+ilofft2-$\frac{Vdd\,\pi}{w\,Lf}$;

vlyon0=vlyon/.t→ton;

vlyoff0=vlyoff/.t→toff;

vswoff0=vswt/.t→toff;

vcxon0=-vlyon0;

vcxoff0=vswoff0-vlyoff0;

isoff0=isoff/.t→toff;

ixoff0=ixoff/.t→toff;

ixon0=ixon/.t→ton;

iloff0=iloff/.t→toff;

ilon0=ilon/.t→ton;

B.2 Differential Mode

ClearAll[Global`*]

vo=Va Sin[w t]+Vb Cos[wt];

vswoff=G1 Sin[wa t]+G2 Cos[wa t]+G3 Sin[wb t]+G4 Cos[wb t]+Vi+wv vo;

vswoff0=vswoff/.t→toff;

vyoff=$\frac{1}{wxy^2}\left(\frac{Cx}{Cx+Cy}-\frac{Cx+Csh}{Cx}\right)\partial_t\partial_t$vswoff+$\frac{wfx^2}{wxy^2}\left(1+\frac{Csh}{Cx}\right)$(Vi-vswoff)+$\frac{1}{wxy^2}\frac{Cy}{Cy+Cx}\partial_t\partial_t$vo;

(* collect terms *);

vyoffCollect=Collect[vyoff,{Sin[t w],Cos[t w],Sin[t wa],Cos[t wa],Sin[t wb],Cos[t wb]}];

vyoffSinwt=Coefficient[vyoffCollect,Sin[t w]];

vyoffCoswt=Coefficient[vyoffCollect,Cos[t w]];

vyoffSinwat=Coefficient[vyoffCollect,Sin[t wa]];

vyoffCoswat=Coefficient[vyoffCollect,Cos[t wa]];

```
vyoffSinwbt=Coefficient[vyoffCollect,Sin[t wb]];
vyoffCoswbt=Coefficient[vyoffCollect,Cos[t wb]];
(* collect subterms *)
deltaVa=Coefficient[vyoffSinwt,Va];
deltaVb=Coefficient[vyoffCoswt,Vb];
deltaG1=Coefficient[vyoffSinwat,G1];
deltaG2=Coefficient[vyoffCoswat,G2];
deltaG3=Coefficient[vyoffSinwbt,G3];
deltaG4=Coefficient[vyoffCoswbt,G4];
vyoffk=Va deltaVa0 Sin[w t]+Vb deltaVb0 Cos[w t]+G1 deltaG10 Sin[wa t]
    +G2 deltaG20 Cos[wa t]+G3 deltaG30 Sin[wb t]+G4 deltaG40 Cos[wb t];
vyoff0=vyoffk/.t→toff;
vyon=Nu1 Sin[wxy(t-π/w)]+Nu2 Cos[wxy(t-π/w)]-w^2/(w^2-wxy^2) Cx/(Cx+Cy) vo;
icxoff=Cx ∂t(vswoff-vyoffk-vo);
icxon=-Cx ∂t(vyon+vo);
Nux=Flatten[Solve[{∫0^(π/w) vyoffk dt+∫(π/w)^(2π/w) vyon dt==0,∫0^(π/w) icxoff dt+∫(π/w)^(2π/w) icxon dt==0},
    {Nu1,Nu2}]];
NuxCollect=Collect[Nux,{G1,G2,G3,G4,Va,Vb},Simplify];
Nu11=Coefficient[{Nu1/.NuxCollect},G1];
Nu21=Coefficient[{Nu2/.NuxCollect},G1];
Nu12=Coefficient[{Nu1/.NuxCollect},G2];
Nu22=Coefficient[{Nu2/.NuxCollect},G2];
Nu13=Coefficient[{Nu1/.NuxCollect},G3];
Nu23=Coefficient[{Nu2/.NuxCollect},G3];
Nu14=Coefficient[{Nu1/.NuxCollect},G4];
Nu24=Coefficient[{Nu2/.NuxCollect},G4];
Nu1a=Coefficient[{Nu1/.NuxCollect},Va];
Nu2a=Coefficient[{Nu2/.NuxCollect},Va];
Nu1b=Coefficient[{Nu1/.NuxCollect},Vb];
Nu2b=Coefficient[{Nu2/.NuxCollect},Vb];
Nu10=G1 Nu110+G2 Nu120+G3 Nu130+G4 Nu140+Va Nu1a0+Vb Nu1b0;
Nu20=G1 Nu210+G2 Nu220+G3 Nu230+G4 Nu240+Va Nu2a0+Vb Nu2b0;
icxoffg=icxoff;
icxong=icxon/.Nu1→Nu10, Nu2→Nu20;
icxoffCollect=Collect[icxoffg,Sin[t w],Cos[t w],Sin[t wa],Cos[t wa],Sin[t wb],Cos[t wb]];
icxoffSinwt=Coefficient[icxoffCollect,Sin[t w]];
icxoffCoswt=Coefficient[icxoffCollect,Cos[t w]];
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```
icxoffSinwat=Coefficient[icxoffCollect,Sin[t wa]];
icxoffCoswat=Coefficient[icxoffCollect,Cos[t wa]];
icxoffSinwbt=Coefficient[icxoffCollect,Sin[t wb]];
icxoffCoswbt=Coefficient[icxoffCollect,Cos[t wb]];
pb=Coefficient[icxoffSinwt,Vb];
pa=Coefficient[icxoffCoswt,Va];
p2=Coefficient[icxoffSinwat,G2];
p1=Coefficient[icxoffCoswat,G1];
p4=Coefficient[icxoffSinwbt,G4];
p3=Coefficient[icxoffCoswbt,G3];
icxoff0=Vb pb0 Sin[w t]+Va pa0 Cos[w t]+G2 p20 Sin[wa t]+G1 p10 Cos[wa t]
        +G4 p40 Sin[wb t]+G3 p30 Cos[wb t];
icxonCollect=Collect[icxong,{Sin[t w],Cos[t w],Sin[(t-π/w)wxy],Cos[(t-π/w)wxy]}];
icxonSinwt=Coefficient[icxonCollect,Sin[w t]];
icxonCoswt=Coefficient[icxonCollect,Cos[w t]];
icxonSinwxyt=Coefficient[icxonCollect,Sin[(t-π/w)wxy]];
icxonCoswxyt=Coefficient[icxonCollect,Cos[(t-π/w)wxy]];
qb=Coefficient[icxonSinwt,Vb];
qa=Coefficient[icxonCoswt,Va];
q11=Coefficient[icxonSinwxyt,G1];
q12=Coefficient[icxonSinwxyt,G2];
q13=Coefficient[icxonSinwxyt,G3];
q14=Coefficient[icxonSinwxyt,G4];
q1a=Coefficient[icxonSinwxyt,Va];
q1b=Coefficient[icxonSinwxyt,Vb];
q21=Coefficient[icxonCoswxyt,G1];
q22=Coefficient[icxonCoswxyt,G2];
q23=Coefficient[icxonCoswxyt,G3];
q24=Coefficient[icxonCoswxyt,G4];
q2a=Coefficient[icxonCoswxyt,Va];
q2b=Coefficient[icxonCoswxyt,Vb];
icxon0=(G1 q110+G2 q120+G3 q130+G4 q140+Va q1a0+Vb q1b0)Sin[(t-π/w)wxy]
       +(G1 q210+G2 q220+G3 q230+G4 q240+Va q2a0+Vb q2b0)Cos[(t-π/w)wxy]
       +Vb qb0 Sin[t w]+Va qa0 Cos[t w];
Vux=Flatten[Solve[{w/π ∫_0^(π/w) icxoff0 Sin[w t]dt+w/π ∫_(π/w)^(2π/w) icxon0 Sin[w t]dt==Va/2RL,
       w/π ∫_0^(π/w) icxoff0 Cos[w t]dt+w/π ∫_(π/w)^(2π/w) icxon0 Cos[w t]dt==Vb/2RL},{Va,Vb}]];
VuxVaCollect=Collect[Va/.Vux,{G1,G2,G3,G4},Simplify];
```

```
a1=FullSimplify[Coefficient[VuxVaCollect,G1]];
a2=FullSimplify[Coefficient[VuxVaCollect,G2]];
a3=FullSimplify[Coefficient[VuxVaCollect,G3]];
a4=FullSimplify[Coefficient[VuxVaCollect,G4]];
Va0=G1 a10+G2 a20+G3 a30+G4 a40;
VuxVbCollect=Collect[Vb/.Vux,{G1,G2,G3,G4},Simplify];
b1=FullSimplify[Coefficient[VuxVbCollect,G1]];
b2=FullSimplify[Coefficient[VuxVbCollect,G2]];
b3=FullSimplify[Coefficient[VuxVbCollect,G3]];
b4=FullSimplify[Coefficient[VuxVbCollect,G4]];
Vb0=G1 b10+G2 b20+G3 b30+G4 b40;
vswoffp=Collect[vswoff/.{Va→Va0,Vb→Vb0},{G1,G2,G3,G4},Simplify];
vswoff0p=vswoffp/.t→toff;
vswoffs0=vswoffp/.t→0; vswoffs1=vswoffp/.t→π/w; vswoffs2=w/(2π) ∫_0^(π/w) vswoffp dt;
Gux123=Flatten[Solve[{vswoffs0==0,vswoffs1==0,vswoffs2==Vi},{G1,G2,G3}]];
G1x=G1/.Collect[Gux123,{G4,Vi},Simplify];
G14=Coefficient[G1x,G4]; G1i=Coefficient[G1x,Vi]; G10=G4 G140+Vi G1i0;
G2x=G2/.Collect[Gux123,{G4,Vi},Simplify]; G24=Coefficient[G2x,G4];
G2i=Coefficient[G2x,Vi]; G20=G4 G240+Vi G2i0;
G3x=G3/.Collect[Gux123,{G4,Vi},Simplify]; G34=Coefficient[G3x,G4];
G3i=Coefficient[G3x,Vi];G30=G4 G340+Vi G3i0;
vswoffpx=Collect[vswoffp/.{G1→G10,G2→G20,G3→G30},
        {Sin[t w],Cos[t w],Sin[t wa],Cos[t wa],Sin[t wb],Cos[t wb]},Simplify];
vyoffk1=vyoffk/.{Va→Va0,Vb→Vb0};
vyoffk2=vyoffk1/.{G1→G10,G2→G20,G3→G30};
vyonk1=vyon/.{Nu1→Nu10,Nu2→Nu20};
vyonk2=vyonk1/.{Va→Va0,Vb→Vb0};
vyonk3=vyonk2/.{G1→G10,G2→G20,G3→G30};
vyoffkt0=vyoffk2/.t→π/w;
vyonk2pi=vyonk3/.t→π/w;
G4m=Solve[vyoffkt0==vyonk2pi,G4];
G4x=Collect[G4m,Vi];
```