FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

CMOS RF Sigma-Delta Converter

Luís Filipe Brochado Reis

Master in Electrical and Computers Engineering

Supervisor: Vítor Manuel Grade Tavares, PhD

Second Supervisor: Terry Sai Weng Sin, PhD

July 28, 2017

Resumo

A complexidade e diversidade de processamento que se consegue alcançar com sistemas digitais é consideravelmente maior que aquele que se consegue obter com sistemas puramente analógicos. O elevado grau de integração que as tecnologias CMOS permitem, bem como o baixo tempo de resposta, tem motivado uma cada vez maior migração de processamento de sinal para o domínio digital, mesmo em funções que até há pouco se consideravam circunscritas ao domínio analógico. Um exemplo típico é a tentativa de processar digitalmente todos os elementos associados à modulação e desmodulação de sinal em comunicações sem fios. Tal procedimento coloca, no entanto, uma pressão elevada nas interfaces com o mundo físico que é por natureza analógico.

Cada vez mais se exigem conversores A/D a funcionar em regime de frequência RF para cumprir o desígnio de um total processamento digital. O presente documento centra-se neste aspeto fundamental de conversão A/D em RF, tendo como objetivo fornecer ao leitor um suporte teórico, conceptual e de estados da arte que permitam entender as escolhas tomadas no desenvolvimento desta tese que propõe um conversor A/D baseada na arquitetura $\Sigma\Delta$ (Sigma-Delta) para aplicações de comunicação móvel na banda LTE. O circuito foi implementado usando uma tecnologia de 28 nm CMOS com uma frequência de amostragem de 1.6 GHz e IF a 700 MHz. Partindo de uma alimentação de 1.8 V, obteve-se um SNDR de 56 dB, considerando uma banda de 100 MHz e medido por simulação, em circuito ao nível do transístor.

Abstract

The complexity and diversity of processing that can be achieved with digital systems is considerably larger than that achieved with purely analogue systems. The high degree of integration that CMOS technologies allow, as well as the low response time, has motivated an increasing migration of signal processing to the digital domain, even in functions that until recently were considered circumscribed to the analogue domain. A typical example is the attempt to digitally process all elements associated with signal modulation and demodulation of signals in wireless communications. Such a procedure, however, places a high pressure on the interfaces with the physical world, which is, by nature, analogue.

More than ever are A/D converters required to operate at RF frequency to fulfil the design of a total digital processing. This document focuses on this fundamental aspect of RF A/D conversion, aiming to provide the reader with theoretical and conceptual supporting components and the state-of-the-art that justify the choices taken during the development of the thesis work, which proposes an A/D converter based on a $\Sigma\Delta$ (Sigma-Delta) architecture for mobile communication in the LTE band. The circuit was implemented in a 28 nm CMOS technology using 1.6 GHz sampling rate and 700 MHz IF. With a 1.8 V power supply, 56 dB SNDR is achieved over a 100 MHz bandwidth.

Acknowledgements

First and foremost, I would like to express my sincere gratitude to Professor Vítor Grade Tavares for the opportunity he has conceded me to do this dissertation work. Professor Vítor has always been a strong presence in my academic life and his guidance throughout my degree has enable me to grow as an engineer. Despite the distance between us, Professor Vítor was always promptly available and extremely helpful. His assistance was surely crucial to the success of this project.

I'm deeply thankfully to Professor Terry Sai Weng Sin for the same opportunity I was given. Professor Terry was always extremely supportive and encouraging throughout my stay in Macau. I've learnt a lot with him and realised the potential future I have in this field. I hope this alliance may continue as the future of science and technology relies on cooperation and interchange of culture and knowledge.

Iman Kianpour helped me during my Cadence software training. In the short time we have spent together, mainly in room I223, he gave some advising on relevant topics for my future work. For this I thank him.

A special thanks goes to Sam Jiang for the many advices he provided me during my stay in the State Key Laboratory of Analogue and Mixed-Signal VLSI. He helped on countless occasions and took interest in my personal progress. To all my friends in room 3014 a warm thank you, Hubert, for the moments of guidance and advice and Frank for critical help on the transistor technology and switches. To my friend Still a warm thank you for the moments of friendship we shared. Hope you do well with your future endeavours.

I would also like to thank my friends at room I221 for the endless moments of learning, fun and bonding we had, during the preparation phase of this dissertation. No personal achievement would be complete without the camaraderie we shared.

Last, but not least, I thank my loving family and girlfriend for all the support they have provided me embarking on such a journey and keeping me strong and guided during it. Not all moments were easy but they stood by my side and helped me turning any frown upside down.

Luís Filipe Brochado Reis

"Better an oops than a what if."

Beau Taplin

Contents

List of Figures

List of Tables

Listings

Acronyms and Symbols

ΔM	Delta Modulation
ΣΔ	Sigma-Delta
4G	4^{th} generation of mobile networks
5G	5^{th} generation of mobile networks
AA	Anti-Aliasing
A/D	Analogue-to-Digital
AC	Alternating Current
ADC	Analogue-to-Digital Converter
AMSV	Analogue and Mixed-Signal VLSI
BW	Bandwidth
BPSD	Bandpass Sigma-Delta
CIFB	Cascade of Integrators with Feedback
CIFF	Cascade of Integrators with Feed-forward
CMOS	Complementary Metal-Oxide-Semiconductor
CRFB	Cascade of Resonators with Feedback
CRFF	Cascade of Resonators with Feed-forward
CT	Continous Time
D/A	Digital-to-Analogue
DAC	Digital-to-Analogue Converter
DC	Direct Current
DNL	Differential Non-Linearity
DR	Dynamic Range
DT	Discrete Time
E-UTRA	Evolved Universal Terrestrial Radio Access
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FOM	Figure of Merit
GBW	Gain Bandwidth
GLONASS	Global Navigation Satellite System
GND	Ground
GPS	Global Positioning System
HDL	Hardware Description Language
HSPA	High-Speed Packet Access
IMD	Inter-Modulation Distortion
INL	Integral Non-Linearity
LSB	Least Significant Bit
LTE	Long Term Evolution
MASH	Multi-stage Noise Shaping

MOS	Metal-Oxide-Semiconductor
MOSFET	MOS Field-Effect Transistor
MSB	Most Significant Bit
NFC	Near Field Communication
NMOS	N-channel MOSFET
NRZ	Non Return to Zero
NTF	Noise Transfer Function
Op-amp	Operational Amplifier
OSR	Oversampling Ratio
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PMOS	P-Channel MOSFET
RF	Radio Frequency
RZ	Return to Zero
SC	Switched Capacitor
S/H	Sampler and Holder
SFDR	Spurious Free Dynamic Range
SINAD	Signal to Noise plus Distortion Ratio
SNDR	Signal to Noise plus Distortion Ratio
SNR	Signal to Noise Ratio
SQNR	Signal to Quantisation Noise Ratio
STF	Signal Transfer Function
THD	Total Harmonic Distortion
VLSI	Very Large Scale Integration
VCM	Common Mode Voltage

f_B	Bandwidth
f_c	Central Frequency
f_{IF}	RF Input Frequency or Central Frequency
f_s	Sampling Frequency
N_{ef}	Effective Number of Bits
p_e	Error Probability
V_{in}	Input Voltage
V_{LSB}	LSB or minimum voltage
V_{out}	Output Voltage
V_{pp}	Peak-to-peak Voltage
V_Q	Quantisation Error
V_{ref}	Reference Voltage

Chapter 1

Introduction

1.1 Motivation

Analogue-to-digital conversion plays an increasingly important role in modern electronic systems. The Analogue-to-Digital Converter (ADC), together with the DAC (digital to analogue converter), is the electronic building block that actually bridges the digital domain with the real world. Such components are needed to process analogue signals and, more particularly, to support base-band modulation for data transmission through radio links with high debits. In fact, digital systems are the ticking clock of modern smart systems. Being universal machines, the possibilities are endless. This is something not possible (at least not yet) to accomplish with analogue systems. Although they have many advantages that should not be overlooked, such as power efficiency and inherent parallel computing, analogue solutions that can match the processing power found with digital systems is yet to be found. There are good indications that, eventually, such trend will change when new computation paradigms arrive, namely those inspired in biological systems. Nevertheless, the pressure to accomplish faster processing and interaction with the end user is still, and will be in the times to come, the driving force of modern technology development and of consumer electronics. It is supported on digital computational paradigms, which, by far, are the most substantial part of the overall processing. However, faster interaction, together with remote and intense data exchange, pays a toll on communication spectrum usage. Modulations that improve spectral efficiency are then of surmount importance. The so called "software defined radio" and "cognitive radio" are paradigms that try to solve this problem. In principle, a full radio could become totally digital. Such system demands ADCs that are capable of very high data-rate conversion, in the RF range and with sufficient bit resolution so that the analogue elements in the system are almost nonexistence, perhaps just reduced to the LNA (low noise amplifier) and the inherent analogue processing associated with the ADC itself. This is the motto behind the work reported here.

1.2 Challenges in Deep-Submicron Analogue Design

ADC applications stretch from sensors, audio and data acquisition systems, to video, radar and communications interfaces. The most demanding systems, requiring the highest sampling frequencies, are found in RF communication.

The increasing pressure to decrease chip sizes makes the design of analogue circuits evermore challenging. Consequences of miniaturisation are the decrease in working voltages, the limited signal-to-noise ratio due to lower headroom, and lower intrinsic transistor gains, resulting from the short channel lengths. Higher data-rates and small power budgets demand higher sample-rates, bandwidth and lower power dissipation for ADCs. Although the scaling of CMOS technologies has increased the performance of processing units, analogue circuits have not closely followed the same trend.

In light of these difficulties, new techniques and methods need to be developed in order to cope with the limitations imposed by lower size technologies, but also that take advantage of ever faster and more compact circuitry. One possibility is to abandon encoding the information in the amplitude/time domain and translate it just in time, such that instead of the original signal, only the voltage difference between samples is transmitted. This signal is then converted into digital codes for further, more efficient, digital processing. The challenge is now to perform a conversion with good linearity and time resolution, such that the signal can be recovered back with a sufficiently high number of effective bits.

There are several ways to accomplish this conversion. One off the best is the $\Sigma\Delta$ modulator that, using a low bit resolution ADC (as low as 1-bit), can accomplish very high resolution, as high as 12 bits. The modulator works by shaping the quantisation noise through a low-pass filter, thus moving it to higher frequencies, away from the signal bandwidth. This method, however, is not appropriate for high frequency signals, in the RF region. A band-pass modulator is required, where the central frequency is shifted away from DC to the desired carrier. Now the quantisation noise is shifted above and below the passing band of the signal, thus achieving similar results to the low-pass case.

1.3 Problem and Goals

In light of these challenges, this dissertation presents a new architecture and design of a band-pass $\Sigma\Delta$ converter to operate at a sampling frequency of 1.6 GHz, with the intermediate frequency lying in the RF frequency range of 700 MHz. The employed technology is a 28 nm CMOS fabrication process. Low-power consumption, low-area usage and good FOM values are targeted, making the converter suitable for portable devices and capable of competing with current state-of-the-art solutions. The concrete application is focused on conceiving an ADC that is capable of achieving a direct A/D conversion of radio signals, specifically those in the lower-end of the UMTS spectrum, associated with network protocols such as LTE. A possible LTE-Advance solution, with the full aggregated bandwidth of 100 MHz can also be envisioned, as long as a down conversion is first

accomplished to the lower 700 MHz band at the receiver or a undersampling technique is used. An SNR in the order of 40 dB was expected, achieving approximately seven bit conversion.

1.4 Document Structure

This document is divided into six chapters, corresponding the first to the present chapter that serves as an introduction to the developed work and its motivation. A background on the analogue-to-digital conversion subject matter and its key aspects are given in Chapter 2. In Chapter 3, the development of $\Sigma\Delta$ converters, and technology until present day, is outlined. A brief historical introduction is given followed by some theoretical background on $\Sigma\Delta$ modulation. Several implementation solutions and common problems associated with their design are also discussed. The chapter concludes with a collection of State-of-the-art $\Sigma\Delta$ ADCs. The proposed ADC architecture is introduced in Chapter 4. A small motivation for this particular design is given, followed by a thorough functional analysis in Matlab. Simulation results are given along with several performance plots to prove its feasibility. Chapter 5 shifts to the circuit level implementation. Several design blocks used are discussed and a circuit-level schematic of the converter is presented. The chapter is concluded with transistor level simulations and with a comparison of results with state-of-the-art converters. Finally, concluding this document, in Chapter 6, an outlining of the problem and proposed solution is given as a summary. A retrospective is made concerning the objectives for this work and achieved goals. The final results are briefly discussed within a real world application scenario, ending with future work directions. An appendix is also added, presenting the relevant Matlab code used in the scope of this work.

Chapter 2

Fundamentals of Analogue-to-Digital Conversion

This chapter summarises the fundamental concepts that a reader should understand in order to comprehend the options taken during the course of work which led to this dissertation. First, a brief introduction to the topic is given, followed by important aspects and performance specifications of ADCs. Several converter architectures are also discussed. Important reference publications were followed in the development of this chapter. For more detail on the subject it is recommend the reading of [2], [5], [6] and [7].

2.1 Analogue-to-Digital Converter

An ideal A/D converter is a device that takes an analogue input (e.g. voltage), a reference voltage V_{ref} and produces a digital output B_{out}. The conversion naturally produces an error that is related with the final finite bit resolution – the quantum $Q = 1\ \text{LSB} = 1/2^N$, being N the number of bits. This error is commonly referred as the quantisation error, V_x, defined as:

$$-\frac{1}{2}V_{\text{LSB}} \leq V_{\text{x}} \leq \frac{1}{2}V_{\text{LSB}} \tag{2.1}$$

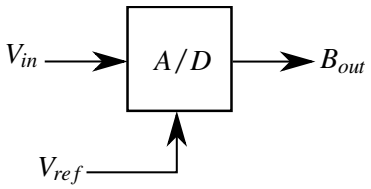

Figure 2.1: ADC typical block.

V_{LSB} is the voltage difference between adjacent bits (the quantum). The LSB (least significant bit) is an equivalent measure but it has no units:

$$V_{\mathrm{LSB}} = \frac{V_{ref}}{2^N} = 1\ \mathrm{LSB} \times V_{ref} \tag{2.2}$$

Then the output can easily be calculated with the following expression, where b_N is the most significant binary bit (MSB) and b_1 the least (LSB):

$$V_{\mathrm{ref}}\left(b_1\, 2^{-1} + \cdots + b_{\mathrm{N}}\, 2^{-N}\right) = V_{\mathrm{in}} \pm V_x \tag{2.3}$$

As Fig. 2.2 shows, there are several input values that can produce one single digital output. This uncertainty is the quantisation error. If transitions are positioned with an offset of $1/2\,V_{\mathrm{LSB}}$, the error has zero mean. All inputs should be kept within the quantisation interval of $\left[-1/2^{N-1}\cdot V_{ref}, \left(2^N-1\right)/2^N \cdot V_{ref}\right]$, otherwise the quantisation error would be larger than $V_{\mathrm{LSB}}/2$ (overloading).

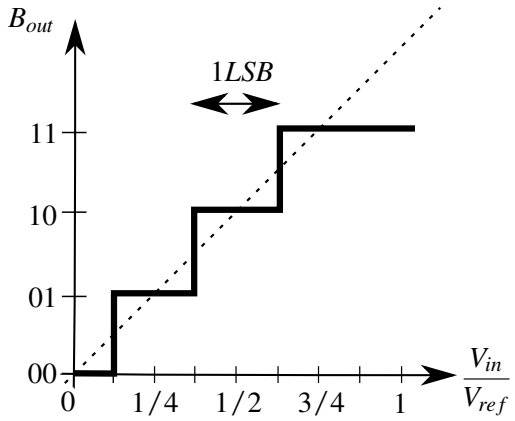

Figure 2.2: ADC transfer curve.

2.1.1 Digital-to-Analogue Converters

An ideal D/A converter performs the inverse task of the ADC.

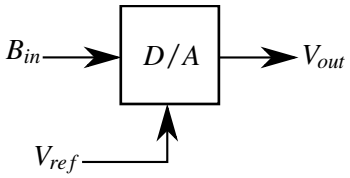

Figure 2.3: DAC typical block.

The input will be a stream of bits that are converted into analogue outputs. The result can be calculated as:

$$V_{\mathrm{out}} = V_{\mathrm{ref}}\left(b_1 2^{-1} + \cdots b_{\mathrm{N}} 2^{-N}\right) = V_{\mathrm{ref}}\, B_{\mathrm{in}} \tag{2.4}$$

The transfer curve, shown in Fig. 2.4, presents well defined analogue values at the output. This is a direct result of quantisation since, digitally, we use a finite number of levels to define a signal. The maximum possible value of V_{out} is not V_{ref} but ($V_{ref} - V_{LSB}$).

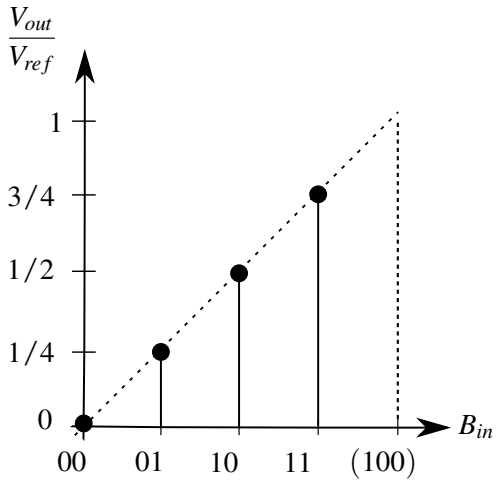

Figure 2.4: DAC transfer curve.

2.2 Quantisation

Converting the signal involves quantisation, which is bound to introduce an error, even in ideal ADCs. The size of the error depends on how large the quantisation intervals are.

An ADC works by taking the voltage on a pin and assigning a digital number to it, depending on the quantisation law in use. There can only be a limited amount of digital codes in use so there will always be quantisation errors made. The error will depend on how big the intervals are related to the signal's amplitude span. A critical situation is when the signal is too big for the code scale in place, resulting in a big quantisation error. One should choose the interval layout and maximum amplitude in such a way that the signal is entirely within its limits, but also that all levels are used, so that efficiency is at its maximum and the signal does not drown in quantisation noise.

The quantisation error is simply the difference between the output voltage level and the input one, as illustrated in Fig. 2.5.

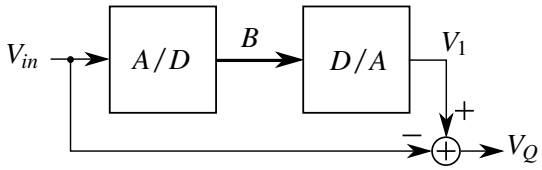

Figure 2.5: Quantisation error.

When there is a high number of quantisation levels and samples, the error can be modelled as an additive white noise with a uniform probability distribution [5].

The following Figs. 2.6 and 2.7 show the quantisation error when a ramp signal is applied to the input.

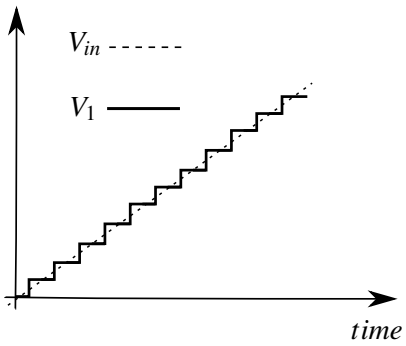

Figure 2.6: Quantised ramp signal.

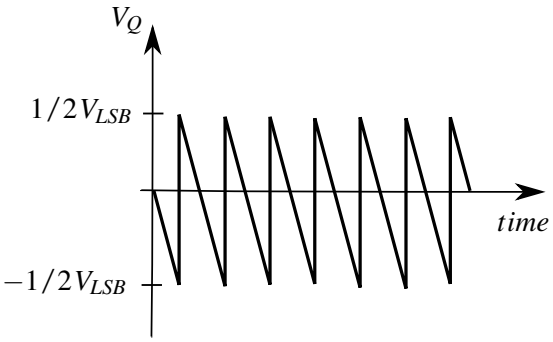

Figure 2.7: Quantisation error of ramp signal.

In order to calculate the quantisation noise power, one can use a stochastic approach in which the noise is a random variable uniformly distributed in the interval $\pm$ $V_{LSB}/2$. The probability density function p_e will be a constant value, in an interval, as shown in Fig. 2.8.

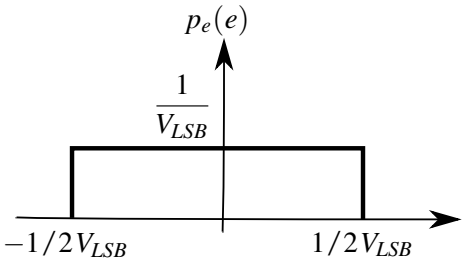

Figure 2.8: Error probability density function.

Finally, in order to calculate the noise power, and bearing in mind that the average value of the distribution is null, we calculate the distribution's variance:

$$V_q{}^2 = \int_{-\infty}^{\infty} x^2 p_e \, dx \tag{2.5}$$

$$V_q{}^2 = \int_{-V_{LSB}}^{V_{LSB}} x^2 \, dx \tag{2.6}$$

$$V_q{}^2 = \frac{V_{LSB}{}^2}{12} \tag{2.7}$$

From the previous figures one can verify that, for each additional bit added, the size of V_{LSB} halves. From the quantisation noise final expression, one can easily see that by adding one bit the power decreases by a factor of four, or equivalently 6 dB.

2.3 Specifications

2.3.1 Sampling Performance

In general, an A/D converter has to have the input stable, unchanged, for a minimum period of time that corresponds to the minimum time needed for converting a voltage to its correct binary code. Sample and hold circuits are those responsible for sampling and then holding the sampled value constant during the time necessary for a correct conversion. We assess their performance using specific parameters, along with ADCs and DACs. It is useful to lay them out before further discussion.

- **Conversion Time** is the time taken for the converter to complete a single measurement. It includes the acquisition time of the input.
- The **Sampling Rate** is the speed at which samples can be converted. Typically, it is calculated as the inverse of the conversion time.
- **Settling Time** is set as the time that it takes for the converter to settle on a specific amount of the final value.
- **Aperture Jitter**, **Aperture Uncertainty** or **Sampling Time Uncertainty** is the result of the changing sampling time between samples. This effect is more noticeable with high speed signals since the input changes more rapidly.
- The **Sampling Pedestal** or **Hold Step** is an error that occurs whenever a sample-and-hold goes from the sample to hold mode. There will always be a small error in the voltage to be held during this operation change. This error should not only be made as small as possible but also signal independent, in order to avoid non-linear distortion.
- One other parameter is the measure of **isolation of the sample signal** from the input during hold mode. The output voltage should not follow any change of the input. Realistically, there is always some leakage due to parasitic capacitances.
- The **Tracking Speed** is the speed at which a sample and hold circuit can track the input signal. The sample and hold will always have limitations on the input since it introduces a -3 dB bandwidth and has finite slew rate.
- The **Droop Rate** consists in the slow change in the output voltage, when in hold mode, due to leakage currents. This parameter is not relevant for CMOS and high-speed designs since its effect is rather small in both.

2.3.2 Static Performance

Static performance parameters are measured with low-frequency signals or with an actual DC input. For A/D converters it is easier to measure transitions rather than midpoint values. Therefore, all errors will be measured in terms of analogue transition values, V_{ij}.

- **Resolution** of a converter is defined as the number of analogue levels that correspond to distinct digital words. A N-bit resolution converter means that it defines 2^N analogue encoding levels.

- In an A/D converter, the **Offset Error** is defined as the deviation of $V_{0\ldots01}$, from 1/2 LSB or:

$$E_{\text{off}} = \frac{V_{0\ldots01}}{V_{\text{LSB}}} - 1/2\,LSB \tag{2.8}$$

  For a D/A converter, it is defined as the actual input for the input code that should produce a zero output, or:

$$E_{\text{off}} = \left.\frac{V_{\text{out}}}{V_{\text{LSB}}}\right|_{0\ldots0} \tag{2.9}$$

- **Gain Error** is defined as the difference in full-scale values of the ideal and actual curves. For an A/D converter it can be calculated as:

$$E_{\text{gain}} = \left(\frac{V_{1\ldots1}}{V_{\text{LSB}}} - \frac{V_{0\ldots01}}{V_{\text{LSB}}}\right) - \left(2^N - 2\right) \tag{2.10}$$

  Similarly, for a D/A converter:

$$E_{gain} = \left(\left.\frac{V_{out}}{V_{LSB}}\right|_{1\ldots1} - \left.\frac{V_{out}}{V_{LSB}}\right|_{0\ldots0}\right) - \left(2^N - 1\right) \tag{2.11}$$

- After the offset and gain errors have been removed, the **Integral Non-Linearity** (INL) can be measured as the characteristic's deviation from a straight line, which can be defined either as the one that ties the endpoints of the converter's transfer response or the best-fit straight line such that the maximum difference is minimized. INL is defined for each digital word. An example of maximum INL can be observed in Fig. 2.9 (DAC example).

- **Differential Non-Linearity** (DNL) is defined as the variation in analogue step sizes that differ from 1 LSB. An ideal converter has the maximum DNL set at 0 for all digital values. DNL is also defined for each digital word.

- **Monotonicity** characterises if a converter's output increases as the input increases as well. In other words, a converter is monotonic if its transfer slope has only one sign along the characteristic.

- **Missing Codes** happen when the DNL is bigger than 1 LSB or the INL is bigger than 0.5 LSB, as shown in Fig. 2.10.

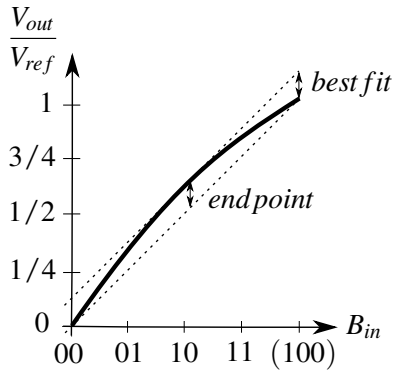

Figure 2.9: Integral Non-Linearity.

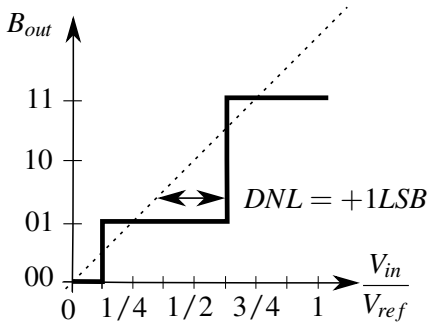

Figure 2.10: Differential Non-Linearity.

2.3.3 Dynamic Performance

- The **Dynamic Range** is defined as the ratio between the output power of a sinusoidal input, with a given amplitude, and the output power noise level [1].

- **Signal to Noise Ratio** (SNR), as the name implies, is the ratio between these two quantities defined in dBs. Typically, it is defined for a sinusoidal input signal, that varies between 0 and V_{ref}:

$$\begin{aligned} SNR &= 20\log\left(\frac{V_{\text{in(rms)}}}{V_{\text{Q(rms)}}}\right) \\ &= 20\log\left(\frac{V_{\text{ref}}/(2\sqrt{2})}{(V_{\text{LSB}}/(\sqrt{12}))}\right. \\ &= 20\log\left(\sqrt{\frac{3}{2}}2^N\right) \end{aligned} \tag{2.12}$$

$$SNR = 6.02N + 1.76dB \tag{2.13}$$

  As a rule of thumb, each bit added equals 6 dB increase in SNR, and vice-versa.

- Similarly, one can introduce the concept of **Effective Number of Bits** (N_{ef}). An N-bit converter may not be able to deliver N data bits at the output. With oversampling, the exact opposite may occur in which the N_{ef} is bigger than the number of working bits of the converter.

- **Signal to Noise plus Distortion Ratio** (SNDR)

  This performance measure is similar to SNR except that non-linear distortion, generated by the converter, are also taken into account. Noise components will be root-mean-square summed with harmonics. SNDR, also called SINAD, is dependent on both the amplitude and frequency of the input.

- **Total Harmonic Distortion** (THD)

  THD is the ratio of the signal power to the total power of the harmonics of the fundamental signal. The number of harmonics accounted for depends on the manufacturers choice, and normally follows the IEEE standard [8], which recommends to use up to the tenth harmonic.

- **Spurious Free Dynamic Range** (SFDR)

  SFDR is the ratio between the RMS value of the input amplitude and the RMS value of the highest spurious spectral component. The SFDR provides information similar to the total harmonic distortion but focusing on the worst tone. There is dependency on the input amplitude since large signals give the highest tone, otherwise tones due to the non-linear nature of the converter become dominant.

- **Intermodulation Distortion** (IMD)

  IMD accounts for tones caused by the mixing modulation between several sine waves in the input, resulting in spectral components at the sum and difference of frequencies.

2.3.4 Converter Performance Comparison

A Figure of Merit (FOM) was proposed by [9] and adapted by [10] to compare the performance of different $\Sigma\Delta$ modulators. The formula is as follows:

$$FOM = \frac{Power(W)}{2^{Resolution(bit)} \times DOR(S/s)} \times 10^{12} \tag{2.14}$$

Resolution is in fact the effective number of bits and DOR is the Digital Output Rate which equals the double of the signal's bandwidth. The FOM translates the amount of energy, in pico-joules per bit, needed per conversion. Many current papers use the following definition for the FOM:

$$FOM = \frac{Power(W)}{2^{ENOB(bit)} \times 2BW(Hz)} \tag{2.15}$$

Another adaptation of the FOM formula was made by [11] for band-pass converters, since the previous definition is more suitable to low-pass modulators and having the input signal at the IF frequency also consumes more power [12]. The formula is the following, where f_N corresponds to the Nyquist rate:

$$FOM_{BP} = \frac{Power}{2^{ENOB} \times 2BW\left(1+3\frac{f_{IF}}{f_N}\right)} \tag{2.16}$$

2.4 ADC Architectures

There are two types of ADCs:

- **Nyquist Converters** generate outputs that have a single correspondence with the input value. These converters rarely work at Nyquist rate since aliasing would be extremely hard to avoid.

- **Oversampling Converters** operate at much higher frequencies than the Nyquist rate, at least 20 times. They increase the output's SNR by trading in samples for effective bits, since the noise will spread out over a larger bandwidth.

2.4.1 Flash

Flash converters are a good approach for high-speed converters. First, the input signal is applied to the 2^N comparators. Each one of them is connected both to the input voltage and to a node V_{ri}, which serves as the reference voltage for comparison. During the second step, the comparators' output is coded and converted into an N bit binary word.

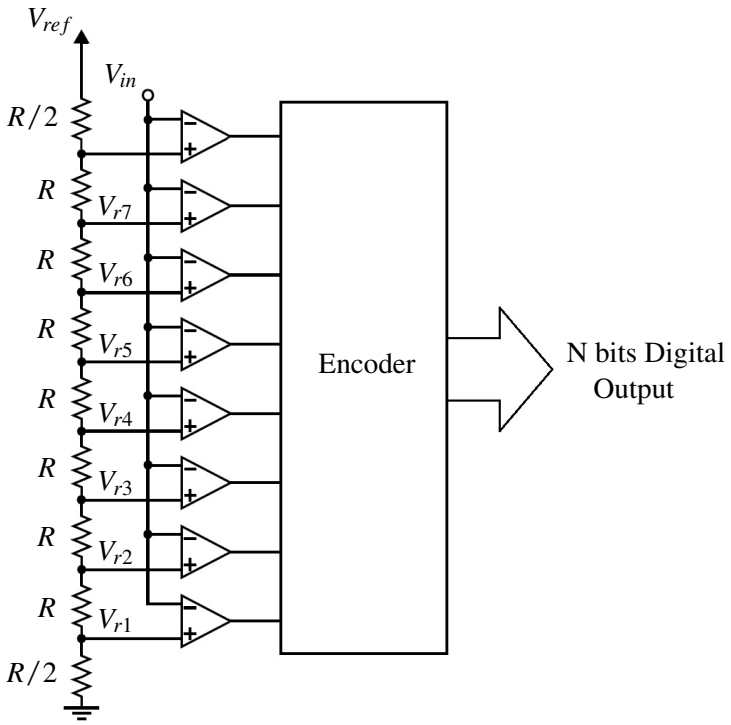

Figure 2.11: Flash Converter.

While this topology allows fast conversion, it requires a large number of comparators, which takes up a lot of area and has a high-power consumption. Other problems that flash converters present are:

- **High Input Capacitive Load** because of the high number of comparators. This limits the conversion's speed and requires a power-hungry buffer;

- **Comparator Latch-to-Track Delay** – a comparator takes some time to come from latch mode to track mode when the input is of opposite polarity from the previous one;
- **Signal and/or Clock Delay** – small clock differences at different comparators may cause noticeable errors;
- **Bubble Error** – sometimes it may happen that an output bit is set to "1", within a string of 0s due to the comparator's metastability, noise, cross talk, limited bandwidth, etc.

2.4.2 Two Step Flash

Two Step Flash converters are more popular than normal Flash because they require less silicon area, dissipate less power, have lower capacitive load and the comparators need to handle less rigorous voltages, even though a higher latency results.

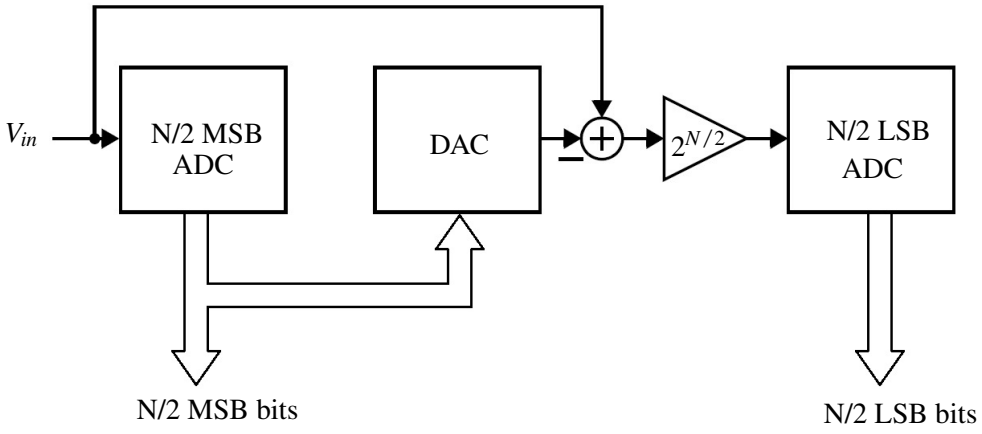

Figure 2.12: 2 Step Flash Converter.

The first step of conversion provides the N/2 most significant bits. This result will be converted back to analogue and subtracted from the original input signal. The difference is amplified to the same converting range and fed back to obtain the remaining bits. This topology requires $2^{(N/2+1)}$ which is considerably less than the Flash method requires.

2.4.3 1 bit Pipeline

The two-stage architecture can be generalised to multiple ones, each of them providing a single bit. The first stage finds the most significant bit, and the last one the least significant. To maximise efficiency a pipeline approach is taken where no 1-bit converter stays idling. This way, after N-1 clock cycles, a full conversion will be complete every cycle. This approach is advantageous when small area of implementation is needed. It also presents low offset and gain errors with high resolution and linearity at the expense of low complexity circuitry. Unfortunately, errors are propagated through the pipeline process. This means that accuracy is constrained by the first stages of the pipeline.

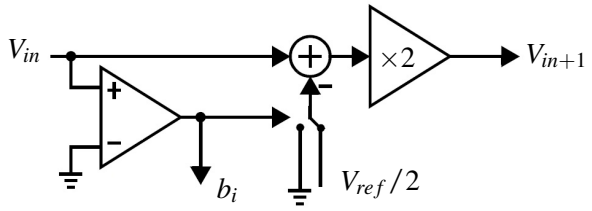

Figure 2.13: 1-bit Pipeline Converter.

2.4.4 Double Integration Ramp

In the Double Integration Ramp method, conversion is performed in two steps: first a ramp is generated during a fixed time, with a slope proportional to the input voltage; the second step will involve decreasing this value until zero with a constant slope, controlled by a reference voltage, and measuring the time it takes, which is directly proportional to the input voltage. Time is counted by a binary counter which outputs the final digital word.

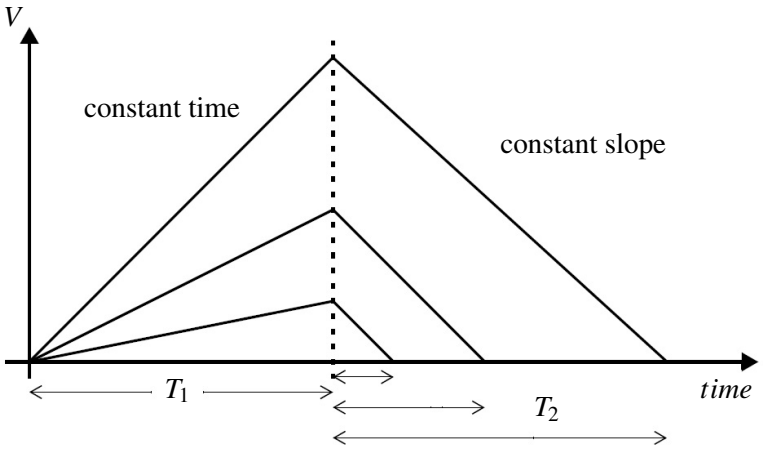

Figure 2.14: Integrating ramp.

Though this method does not present gain error it can have offset error, however, it can be removed with a quad-slope conversion. Another disadvantage is the slow speed conversion and input voltage dependency.

2.4.5 Successive Approximations

Successive Approximations converters have a good compromise balance between conversion time and circuit complexity. The conversion process uses a set of approximations, from a successive approximations register (SAR), starting with the most significant bit. After each iteration, different reference voltages are applied to find out the current bit, from MSB to LSB. This is basically a binary search algorithm which tries to find the closest digital word that matches the input signal.

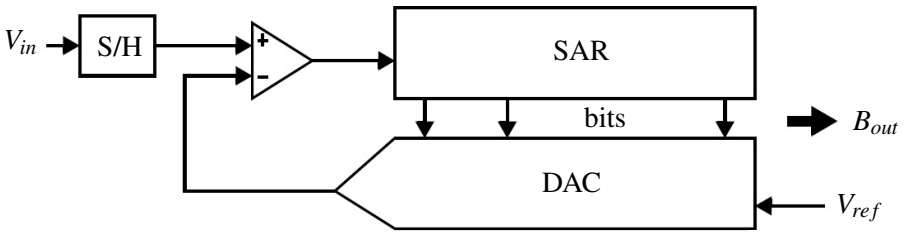

Figure 2.15: Successive approximations converter.

2.4.6 Time Interleaved

A Timer Interleaved conversion makes use of one ADC topology, repeated and connected in parallel. The input signal is sampled and then fed to several sample-and-hold circuits that feed their own ADC. Each stage performs a part of the full conversion which enables for a frequency N times bigger, with N being the number of parallel ADCs.

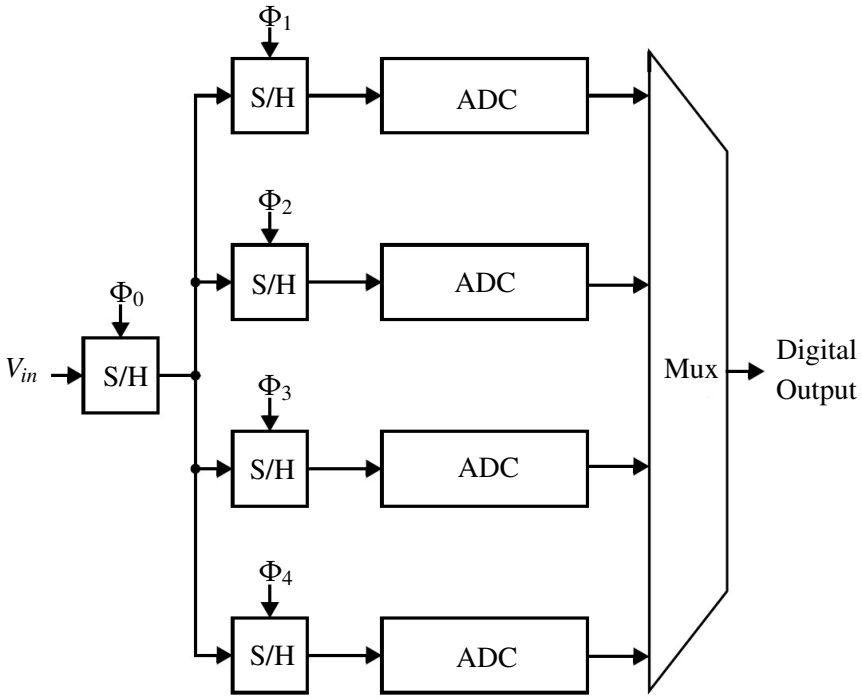

Figure 2.16: Time Interleaved Converter.

Time interleaving is a good option to increase the frequency of conversion but it carries some constraints in performance. Though each individual S/H is not critical, the first one is, and should be properly designed. The remaining ones may suffer from a small amount of jitter without compromising the final result. Despite this, all channels must be really well matched.

2.5 Oversampling

Oversampling is the process of sampling a signal at much higher frequency than the Nyquist rate. Although this rate would be theoretically enough for a perfect reconstruction, oversampling improves typical real world problems such as bad resolution, noise, aliasing and phase distortion.

Oversampling relaxes the requirements on the analogue circuits, at the expense of more complicated digital circuitry. This trade-off becomes more relevant for modern submicron technologies where complicated high-speed digital circuitry is more easily realised with lesser area. These technologies also employ low voltage power supplies, which is challenging when designing high-resolution analogue circuitry.

With oversampling, analogue components do not require so strict matching tolerances and amplifier gains. Anti-aliasing filters and smoothing filters on D/A conversion also have their requirements simplified. Furthermore, a sample-and-hold is usually not required at the input of such a converter.

2.5.1 Oversampling Advantage

Oversampling is the process of sampling a signal, which has a limited bandwidth f_0, at a sample rate higher than the Nyquist or $2f_0$. The oversampling ratio is defined as:

$$OSR = \frac{f_s}{2f_0} \tag{2.17}$$

Since the signal information resides below the frequency f_0, the sampled quantised output can be filtered, removing any quantisation noise or interference signals higher than this frequency threshold.

The spectral density of the quantisation noise is defined as follows:

$$k_x = \frac{V_{LSB}}{\sqrt{12}} \frac{1}{\sqrt{f_s}} \tag{2.18}$$

Oversampling will allow for the quantisation noise to be spread out on a larger bandwidth. Since the spectral density is constant, the noise power will be lower in the band of interest, as Fig. 2.17 shows.

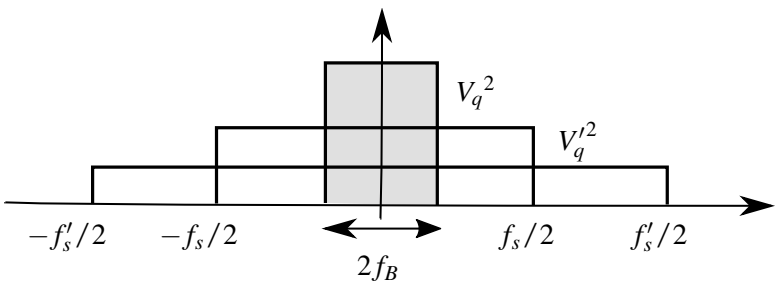

Figure 2.17: Noise spreading due to oversampling.

2.5.2 Signal to Noise Ratio

If we consider a sinusoidal input, its maximum value, without the occurrence of clipping, is:

$$\frac{\left(2^N V_{LSB}\right)}{2} \tag{2.19}$$

The power of such a signal is:

$$P_s = \frac{1}{2}\left(\frac{2^N V_{LSB}}{2}\right)^2 \tag{2.20}$$

$$P_s = \frac{2^{2N} {V_{LSB}}^2}{8} \tag{2.21}$$

Now we have to calculate the power of the noise that is present in the bandwidth of interest:

$$P_e = \int_{-\frac{f_S}{2}}^{\frac{f_S}{2}} {k_x}^2 |H(f)|^2 df \tag{2.22}$$

$$P_e = \int_{-f_0}^{f_0} {k_x}^2 df \tag{2.23}$$

$$P_e = \frac{{V_{LSB}}^2}{12}\frac{1}{OSR} \tag{2.24}$$

Oversampling has the advantage of decreasing the quantisation noise power in half for each doubling in the sampling frequency. Remembering our rule of thumb, that equals 0.5 bits, since doubling the SNR translates into a 3 dB increase.

Knowing the signal and noise power we can now calculate the maximum achievable SNR or, more correctly defined Signal-to-Quantisation-Noise Ratio (SQNR).

$$SQNR = 10\log\left(\frac{P_s}{P_e}\right) \tag{2.25}$$

$$SQNR = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log OSR \tag{2.26}$$

$$SQNR = 6.02N + 1.76 + 10\log OSR \tag{2.27}$$

This expression is recognisable has having the same form as equation 2.13, the typical SNR value of an N-bit quantiser, only added with a term that translates the oversampling advantage. Here we can more easily see the 3 dB/octave increase in SNR. This happens because, when oversampled, the signal's samples are averaged and added linearly. The noise portion is added as the square root of the sum of all squared components.

It is worth noting that other forms of noise present in the circuit, such as thermal noise, will probably also be filtered out. Therefore, expression 2.27 generally holds.

Chapter 3

Sigma-Delta ADC

In this section the State-of-the-Art of ΣΔ modulators will be presented. To develop this chapter several documents were taken into account. Some references are worth highlighting, such as [13], [2], [14], [15], [16], [17] and [18]. Some other authors will be cited throughout the chapter.

First, an historical perspective followed by some breakthroughs throughout history will be given [19]. Afterwards details on how conversion operates with these ADCs will be unfold and its advantages, along with common problems, will also be described. The chapter will carry on with different implementations of this particular modulator.

It is worth noting the terms converter and modulator have the same meaning and are used along this document interchangeably.

3.1 Historical Perspective

Sigma-Delta modulation or, more correctly, Delta-Sigma modulation, was first proposed in [20] as an alternative to Pulse Code Modulation (PCM) and Delta Modulation (ΔM). These schemes had much higher transmission efficiency than previous techniques because they transmitted only the value changes (Δ) between consecutive samples, instead of the actual sample [21].

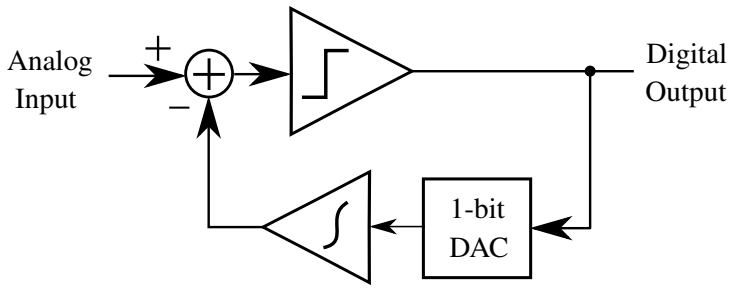

Figure 3.1: Delta Modulation Scheme.

In ΔM, as shown in Fig. 3.1, the analogue signal is quantised by a single-bit ADC. The feedback loop converts the digital outback to an analogue signal. This is integrated and subtracted

from the input. The digital output can only assume two different values, a “1” or a “0”. These can be interpreted, respectively, as a positive excursion from the previous sample and a negative one. If there is no change, the transmitted signal is a pattern of equally alternating “0s” and “1s”.

ΔM has no limit on the tracked signal’s amplitude because it is possible to transmit any number of pulses with the same sign. The problem is that slope clipping exists. If the analogue signal changes too quickly the quantiser may not be able to keep up the pace. To avoid this, high sampling rates are required, much higher than Nyquist rate. Also, since information is carried in the differentiation of the signal at the sending end, there has to be integration at the receiving end to get the signal back, which leads to accumulative errors.

Over the following years concepts such as oversampling and noise shaping were introduced, which helped achieving higher resolution. The concepts present in the ΣΔ ADC were now almost all laid out. Digital filtering and decimation were not, since the technology at the time was not good enough to do so. So, in 1962 the paper [20] was published and in 1963 [22] a second one gave excellent theoretical background on the concepts of oversampling and noise shaping.

As previously stated, this ADC design offers several advantages over other architectures, namely for high resolution and low frequency applications. The one-bit ADC is inherently linear and the low-cost CMOS foundry process can be applied, because of the digital nature present. Modern CMOS ΣΔ are the first choice of converters for voice and audio applications. Also, low-frequency ΣΔ ADCs have replaced older integrating converters in precision industrial measurement applications.

3.1.1 Noise Shaping

Though oversampling improves the SNR by reducing the amount of quantisation noise in the signal’s bandwidth, it is possible to further shape the noise transfer function using a feedback approach, so that it moves to higher frequencies, further away from the band of interest, as shown in Fig. 3.2. The dynamic range will be considerably improved compared to no noise shaping at all. Noise shaping is a corner stone of the ΣΔ converter.

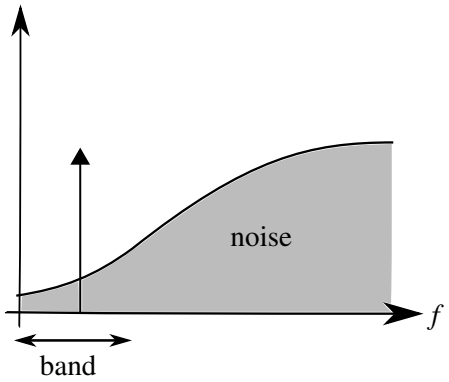

Figure 3.2: Noise shaping.

3.2 The ΣΔ Converter

The ΣΔ modulation scheme, as the name suggests, realises two different operations: Σ or integration and Δ or difference. Thus, the converter continuously integrates the differences. There is some discussion in the scientific community on whether it is called ΣΔ or ΔΣ. In this report the naming ΣΔ will be used, though some references use the other nomenclature.

The following figure is a general representation of a sigma-delta modulator. It comprises a loop filter and a quantiser, followed by a feedback feeding.

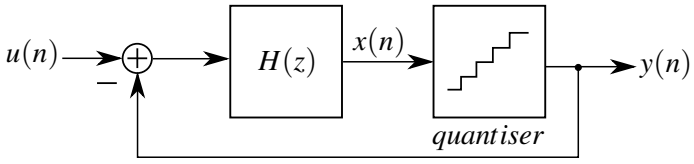

Figure 3.3: ΣΔ converter generic schematic.

The input will be integrated over the loop filter H(z). The quantiser will then produce the equivalent digital symbol. Depending on whether the quantiser produces a logical or a voltage value, a DAC maybe required in the feedback loop. The output will be subtracted to the next sample input and the process repeats. Fig 3.4 provides a visual aid in understanding the internal workings of the modulator.

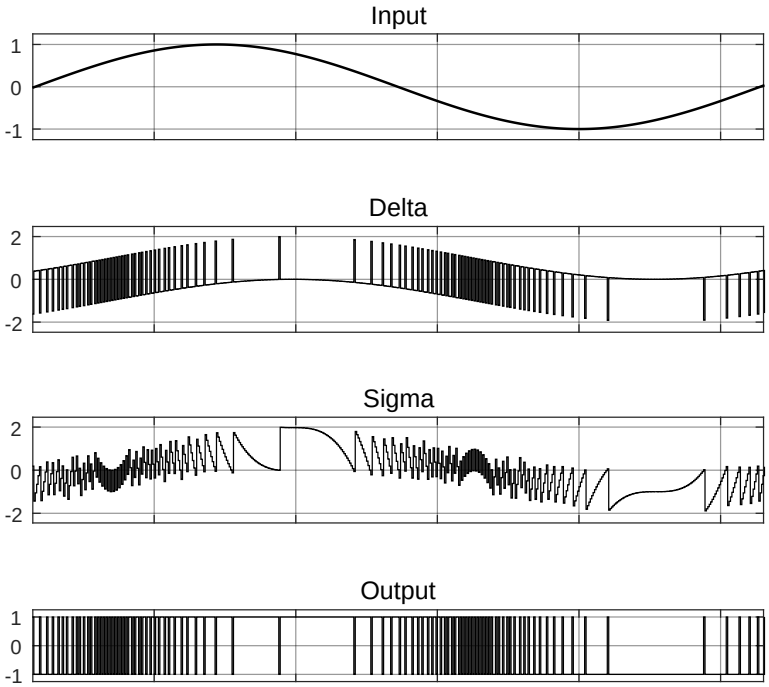

Figure 3.4: Internal signals of a ΣΔ modulator.

We can also represent a linear model of the modulator, where the quantiser can be modelled by an additive, input independent noise.

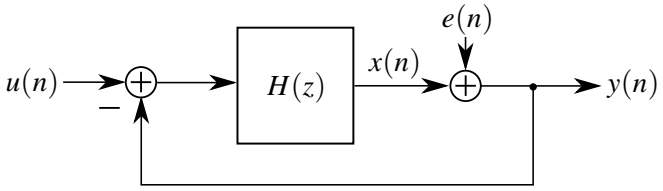

Figure 3.5: ΣΔ converter linear noise model

Analysing this linear model, we can deduce the transfer function, taking into account two independent inputs, the signal input giving rise to the STF and the noise input to the NTF. Note that considering these inputs independent is an approximation and does not represent reality.

$$STF(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{(1+H(z))} \tag{3.1}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{(1+H(z))} \tag{3.2}$$

The final transfer function of the modulator is:

$$Y(z) = STF(z)\,U(z) + NTF(z)\,E(z) \tag{3.3}$$

To help us shape the noise it is useful to note that the poles of the loop filter match the zeros of the NTF, resulting in it going to zero when the filter goes to infinity. The STF should be approximately unit over the band of interest. This is achievable by choosing a H(z) that has large magnitude in this very band. Noise present in higher frequencies will not be affected, however, one can digitally filter it out.

The user should be aware that, since H(z) has large gain in the bandwidth, the input signal can easily saturate the filter, x(n). In reality, the input signal should actually be significantly smaller than the saturation level, in order to meet stability requirements.

3.2.1 Advantage of Single-bit Converters

A common problem in conversion is linearity. Oversampling improves the SNR but does not affect linearity. As an example, to realise a 8-bit converter using an oversampled 4-bit one, an INL lower than 1/8 LSB or an accuracy of $1/2^8$ which equals 0.4 %, is required.

Such accuracies may be difficult to achieve. That is why the ΣΔ converter uses a 1-bit quantiser, as it is inherently linear. Since the quantiser only has two output values, the characteristic curve is a straight line connecting these two points.

3.2.2 First order Shaping

First-order shaping is the simpler noise shaper that a ΣΔ modulator can realise. To implement it, it is useful to remember the relation between H(z) and NTF. The noise has to be high-pass filtered. Thus, its transfer function must have a zero at DC resulting in a $\left(1-z^{-1}\right)$ NTF. This translates into a pole at DC for the filter's transfer function H(z):

$$H(z) = \frac{1}{z-1} \tag{3.4}$$

H(z) should then be a discrete-time integrator. A implementation using only discrete time unit delay blocks and 1-bit quantisation is suggested in Fig 3.6.

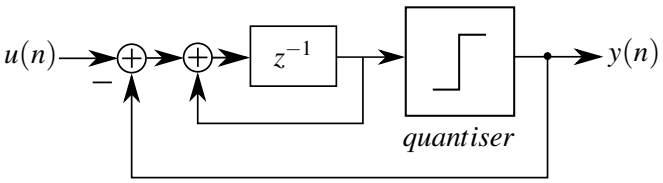

Figure 3.6: 1st order low-pass ΣΔ converter

Analysing the overall transfer function of the first-order modulator presented in Fig. 3.6, and taking into account the linear model shown in Fig. 3.5 we get:

$$Y(z) = z^{-1}U(z) + \left(1-z^{-1}\right)E(z) \tag{3.5}$$

The signal at the output will be a delayed version of the input signal together with a high-passed noise band.

In order to determine the overall SQNR of this modulator we need to calculate the amount of noise present in the band of interest. We first analyse the noise transfer function and replace z with $e^{j2\pi f/f_s}$, which leads to:

$$|NTF(f)| = 2\sin\left(\frac{\pi f}{f_s}\right) \tag{3.6}$$

To calculate the quantisation noise power that falls into the band of interest, 0 to f_0, similarly to 2.22 and 2.23, we do:

$$P_e = \int_{-f_0}^{f_0} {k_x}^2 \left|N_{TF}(f)\right|^2 df \tag{3.7}$$

After some approximations and assuming the input signal power in 2.20, we obtain the maximum achievable SQNR for this first-order ΣΔ converter:

$$SQNR = 6.02N + 1.76 - 5.17 + 30\log(OSR) \tag{3.8}$$

Comparing to 2.27, we get an SNR improvement of 9 dB, per each doubling in OSR, instead of 3 dB with no noise shaping. In terms of effective bits, a gain of 1.5 bits/octave is achieved with first-order noise shaping against 0.5 bit/octave, with no shaping at all.

3.2.3 Second order Shaping

In order to realise a second-order shaping the STF will remain z^{-1} but the noise transfer function will be squared:

$$NTF = \left(1 - z^{-1}\right)^2 \tag{3.9}$$

A schematic of a second-order ΣΔ modulator, realising this NTF is presented in Fig 3.7. Note that two feedback stages are now necessary, one per each order increase. An implementation using only discrete time unit delay blocks is suggested in Fig 3.8.

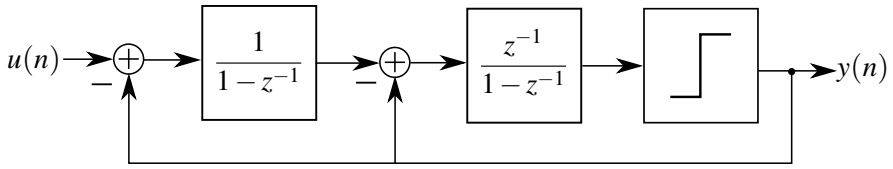

Figure 3.7: 2nd order low-pass ΣΔ converter.

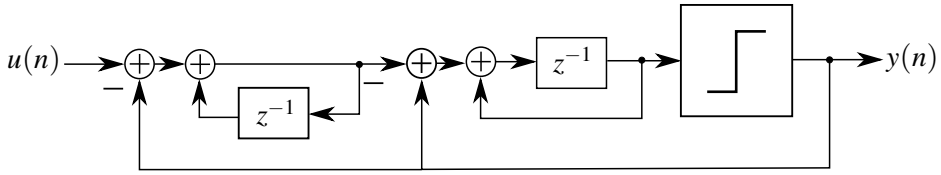

Figure 3.8: 2nd order low-pass ΣΔ converter.

To determine the maximum SQNR the same procedure as before, in 3.6 and 3.7, is applied. This leads to the following expression:

$$SQNR = 6.02N + 1.76 - 12.9 + 50\log(OSR) \tag{3.10}$$

Now comparing to first-order shaping and its maximum achievable SNR in 3.10, we get 15 dB and 2.5 bits per octave increases versus 9 dB and 1.5 bits.

3.2.4 Higher Order Shaping

Increasing the noise shaping order allows for higher resolution since more noise power is being pushed outside the signal's bandwidth. Higher noise shaping also allows to achieve the same resolution with lower sampling rate, thus relaxing the requirements on analogue hardware.

An L order modulator, following the previous implementations, will realise a STF with a unit delay z^{-1} while the NTF will contain L zeros at DC, $\left(1-z^{-1}\right)^L$ [23].

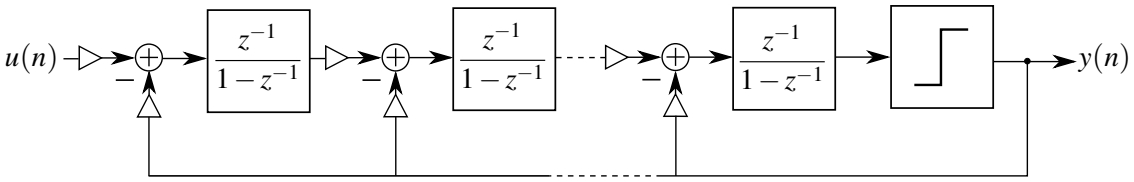

Figure 3.9: Example L[th] order low-pass ΣΔ modulator.

Adding further stages to the modulator, performing an L[th] order noise shaping, it can be shown that the maximum achievable SQNR is:

$$SQNR = 6.02N + 1.76 - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \tag{3.11}$$

Thus, the SQNR increases, with each doubling in OSR, by (6L+3) dB or, equivalently, (0.5+L) bits.

Other possible implementations will be discussed in 3.4, such as cascaded topologies, as these implement both low and band-pass modulators.

3.2.5 MASH Structure

One approach to realise higher order ΣΔ modulators is the Multi-Stage Noise Shaping (MASH) [24][25]. Fig. 3.10 shows an example of a MASH converter. The quantisation error of each stage is fed to the next one. With the aid of digital processing it is possible to cancel the noise generated by quantisation in the previous stage, using the digital output of the current one.

The main advantage of a MASH structure is that stability is guaranteed for the whole system if each individual stage is stable. First and second-order modulators are unconditionally stable. Thus, these are common block in the building of MASH structured converters.

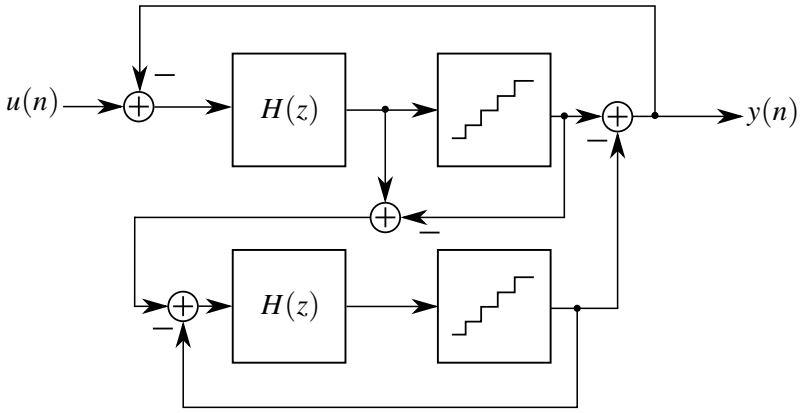

Figure 3.10: MASH structure example.

3.2.6 Multi-bit Converters

Despite their high linearity, or at least their ability to realise highly linear data conversion, 1-bit converters have disadvantages such as instability, since there is a high nonlinearity in the feedback, and idle tones. In order to obtain high SNR using a 1-bit quantiser, high order modulation is needed, which carry difficulties in using high OSR and instability.

The amplifier's bandwidth must be higher than the clock frequency. This imposes a big constraint on speed and power usage, limiting their use to a handful of applications. Due to the high output swing of op-amps, reference voltages are a fraction of the supply voltage. Thus, using low voltage supply can make the reference voltage lower than the thermal noise, drowning it. The op-amp slew rate, together with the reference voltage, limits the maximum usable frequency. For the 1-bit quantiser, the maximum input of the integrator is about $2\,V_{ref}$. If V_{ref} is too big, the slew rate must be proportionally lower. Using a multi-bit quantiser lowers the maximum input by lowering the difference between samples.

Naturally, using a multi-bit quantiser improves the ENOB, but at the expense of more power consumption. There is a power trade-off between OSR and number of bits in the quantiser.

3.3 Band-pass ΣΔ Converters

Not all signals are suitable for the standard low-pass ΣΔ converter. The low-pass converter has its signal band between DC and a given frequency, which stands a given ratio below the frequency sample. But, some signals, for instance, radio signals, have been modulated around a high frequency carrier, though with a smaller or bigger amount of information bandwidth. Therefore, it would be useful to have a shaping that would remove noise only from this bandwidth. After conversion, the desired signal could be band-pass filtered, removing any out of the band noise and adjacent channels. This is where the band-pass ΣΔ converter comes in handy. Instead of having the loop filter H(z) with a high DC gain, band-pass ΣΔ modulators shift the high gain to a frequency f_c with a bandwidth f_B dependent on the OSR. It should be noted that a second-order band-pass ΣΔ converter's dynamic range matches a first-order low-pass one.

3.3.1 Second-order Band-pass Modulator

In order to obtain a second-order modulator, with $f_c = f_s/4$, the loop filter must have its poles at $\pm j$ which gives a resonator with infinite gain at this frequency:

$$H(z) = \frac{z}{z^2+1} \tag{3.12}$$

An implementation of the resonator is suggested in Fig. 3.11. The overall transfer function will be:

$$Y(z) = \frac{z}{z^2+z+1}U(z) + \frac{z^2+1}{z^2+z+1}E(z) \tag{3.13}$$

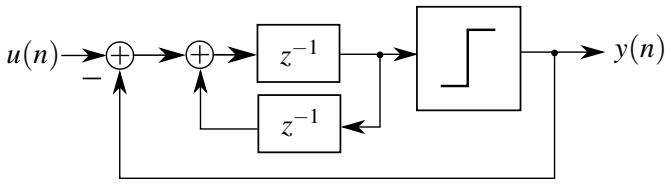

Figure 3.11: 2nd order band-pass ΣΔ converter.

When the input frequency is $f_0/4$, since $z = e^{j2\pi f/f_s}$, z will equal $e^{j\pi/2}$ or $\pm j$. Analysing the transfer function one can see that, with this input, the STF will be unit and the NTF will be zero.

As mentioned before, the second-order band-pass modulator will match the first-order low-pass in terms of dynamic range. This is why the SNR will also increase 9 dB/octave. To achieve the same 15 dB/octave a fourth-order modulator, presented in the next section, has to be used.

3.3.2 Fourth-order Band-pass Modulator

To obtain the equivalent fourth-order band-pass converter, a transformation of z^{-1} to $-z^{-2}$ can be applied to the second-order low-pass converter. An implementation [26] is proposed in Fig. 3.12. The resulting transfer function is:

$$Y(z) = -z^{-2}U(z) + \left(1+z^{-2}\right)^2 E(z) \tag{3.14}$$

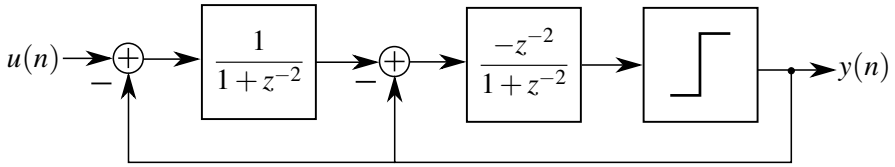

Figure 3.12: 4th order band-pass ΣΔ converter.

The dynamic range increase matches that of the second-order low-pass modulator, that is 15 dB/octave.

3.3.3 Multi Path Architecture

Multi path architecture is much easier to implement in band-pass ΣΔ design, because of multi-rate processing. The hardware used for a converter is replicated N times and time-interleaved, allowing each path to work a frequency N times lower than the effective sampling rate. A N-path architecture works using multi-rate processing as the signal is combined back together at output to the effective final rate.

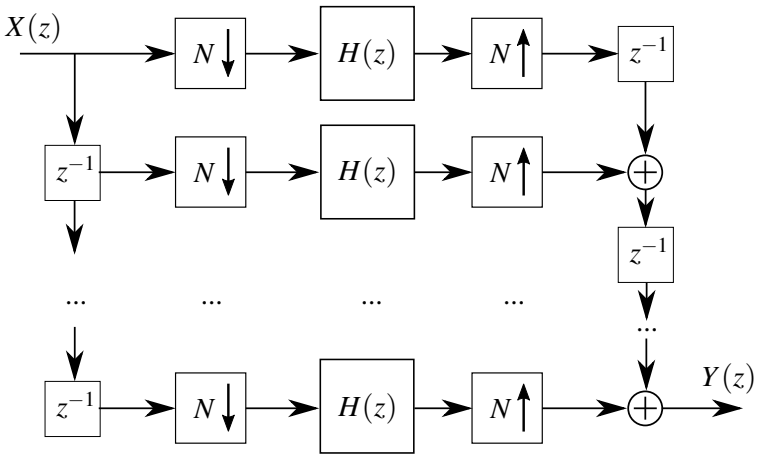

Figure 3.13: N-path converter architecture example.

For the multi-path architecture shown in Fig. 3.13, it can be shown that if the NTF of each path is $1-z^{-1}$, using a N-path architecture it is transformed to:

$$H(z^N) = 1 - z^{-N} \tag{3.15}$$

This technique allows a band-pass $\Sigma\Delta$ modulator to be built using low-pass converters in each of the paths. Each path works at a rate of 1/N the final effective sampling rate. An adding multiplexer combines each paths' output. Ideally the OSR increases in the same ratio as the effective sampling frequency. Unfortunately, for $N > 2$ this is not true as some noise shaping is applied to unnecessary frequency locations.

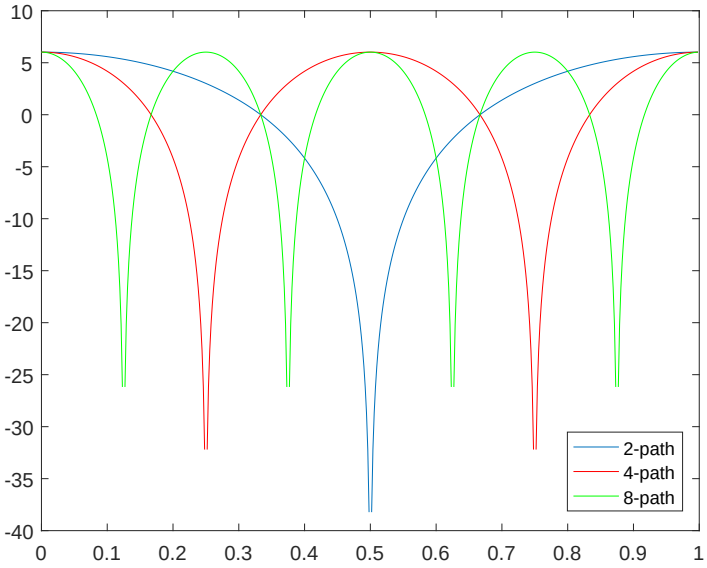

Figure 3.14: Multi-path NTF curves for different path numbers.

Fig. 3.14 shows the noise shaping curves for a 2, 4 and 8 path modulator. One can observe that there is, respectively, zeros placed at 1, 2 and 4 different locations. This is only useful if one wants several frequencies to be filtered. Since the two-path architecture is the only one placing a single zero, it is the most popular choice for multi-path implementations.

3.4 Cascaded Implementations

In this section different cascaded topologies will be discussed [27], using feed-forward and feedback loops. Although both techniques provide the same NTF, they present different signal transfer characteristics and have some performance differences.

3.4.1 Cascade of Integrators with Feedforward

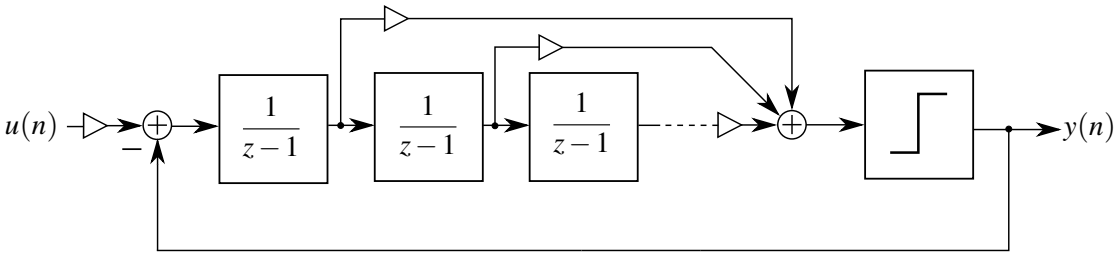

Figure 3.15: CIFF modulator schematic.

The first topology discussed is the CIFF structure. Here, a fraction of the output of each integrator stage is added to the output of the final stage. The block diagram for this topology is shown in Fig. 3.15. The STF and NTF are:

$$STF = \frac{\sum_{i=1}^{n} a_{\text{n-i+1}}.(z-1)^{i-1}}{(z-1)^n + \sum_{i=1}^{n} a_{\text{n-i+1}}.(z-1)^{i-1}} \tag{3.16}$$

$$NTF = \frac{(z-1)^n}{(z-1)^n + \sum_{i=1}^{n} a_{\text{n-i+1}}.(z-1)^{i-1}} \tag{3.17}$$

One can easily see that the zeros of the NTF are all placed at DC. The drawback of adding zeros to the STF is the peaking created at certain frequencies due to the filter characteristic, thus overloading the modulator.

3.4.2 Cascade of Resonators with Feedforward

The CIFF structure places all NTF zeros at DC, which is not desirable since it places some quantisation noise at low frequencies. CRFF modulators can spread zeros along the signal bandwidth.

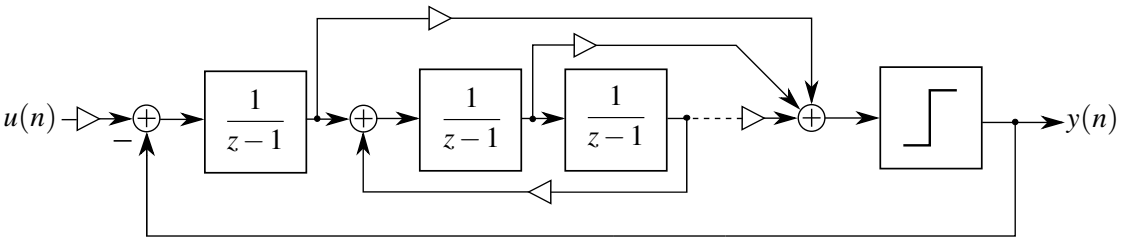

Figure 3.16: CRFF modulator schematic.

One can shift the zeros by adding a negative feedback term around pairs of integrators, which creates resonator stages. The general transfer function of a resonator is:

$$H(z) = \frac{z}{z^2+1} \tag{3.18}$$

It is then possible to implement a filter, by picking the desired stop-band frequency. The schematic for such topology is shown in Fig. 3.16.

3.4.3 Cascade of Integrators with Feedback

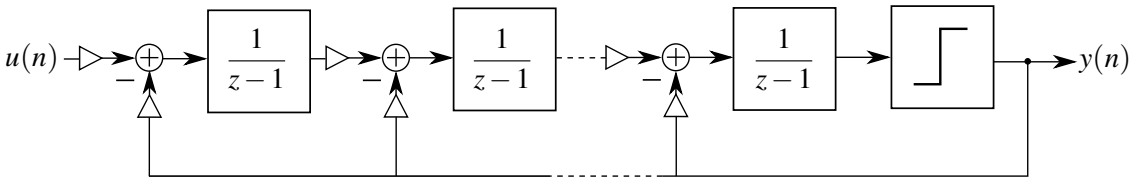

Figure 3.17: CIFB modulator schematic.

Now, feedback structures are presented, which implement the zeros of the NTF as before. The first topology shown in Fig. 3.17 is a CIFB, with each integrator stage receiving a fraction of the output. The transfer functions are:

$$STF = \frac{1}{(z-1)^n + \sum_{i=1}^{n} a_i.(z-1)^{i-1}} \tag{3.19}$$

$$NTF = \frac{(z-1)^n}{(z-1)^n + \sum_{i=1}^{n} a_i.(z-1)^{i-1}} \tag{3.20}$$

As before, all zeros of the NTF lie at DC while the STF has no zeros. A downside to this architecture is the significant amount of input signal and quantisation noise being outputted by the integrators.

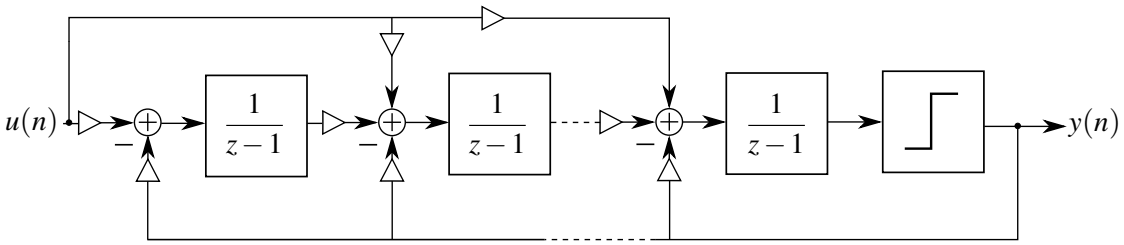

Figure 3.18: CIFB with feedforward paths modulator schematic.

In this architecture, the STF is dependent on the NTF. To overcome this, feedforward paths can be added between the input node and each integrator's summing node, depicted in Fig. 3.18, resulting in the transfer functions:

$$STF = \frac{\sum_{i=1}^{n} b_{\text{n-i+1}}.(z-1)^{i-1}}{(z-1)^n + \sum_{i=1}^{n} a_{\text{i}}.(z-1)^{i-1}} \tag{3.21}$$

$$NTF = \frac{(z-1)^n}{(z-1)^n + \sum_{i=1}^{n} a_{\text{i}}.(z-1)^{i-1}} \tag{3.22}$$

Note that now the STF is independent from the NTF, by choosing the b coefficients. One can now choose the zeros of the STF so that they cancel some poles or perform a better filtering of the desired signal.

3.4.4 Cascade of Resonators with Feedback

Similarly to the CRFF structure, the CRFB uses a CIFB added with resonator stages to shift the NTF zeros away from DC. The block diagram of this implementation is shown in Fig. 3.19.

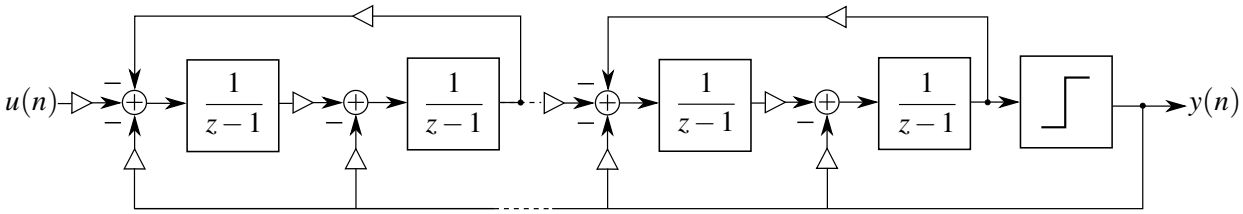

Figure 3.19: CRFB modulator schematic.

3.4.5 Comparison between Feedforward and Feedback

Both feedback and feedforward topologies achieve similar results since both are capable of improving the stability of the loop. Despite this, there are differences between them. The feedforward

approach feeds only the quantisation noise into the loop filter, yielding less power consumption. The feedback topology feed both quantisation noise and input signal.

As shown in 3.17 the CIFF behaves as a first order low pass filter, because the $(n-1)$ zeros cancel the n poles out. The CIFB STF expression shown in 3.19 can be seen as a n^{th} order low-pass filter. Thus, CIFB has a much better filtering performance over the input signal. The pole to zero cancellation process in the CIFF is not ideal. Thus, peaks at given frequencies occur. Since the CIFB's STF does not present zeros, there is no peaking.

Another advantage of the feedback structure, as previously stated, is the addition of resonator stages which allows the shifting of zeros away from DC to the signal's bandwidth, providing better filtering and band-pass architectures.

3.5 Problems

There are several aspects that have to be taken into consideration when designing a modulator. An improper implementation would lead to a failing modulator due to one or more of the problems to be discussed next.

3.5.1 Stability

Feedback systems always have the possibility of becoming unstable. Stability is achieved whenever the input of the quantiser does not overload it, resulting in an output that exceeds the quantisation interval of $\pm\Delta/2$.

For a 1-bit modulator, stability criteria is not well understood. Therefore, several methods are used to determine stability conditions. A common one is to use extensive simulations to determine such conditions. A real-time approach can also be done, using circuitry that detects long strings of 1s or 0s or any other suspicious patterns. This is called resetting of filter states and, when said patterns are detected, loop filters' states are set back to zero. A continuous overloading of the modulator may cause periodic reset events and should also be avoided under normal operating conditions [28]. Another solution is to simulate the maximum possible input voltage and monitor it in the circuit level. If the limit is exceeded, the converter can be assumed under unstable conditions.

3.5.2 Linearity

Ideally, a 1-bit converter would be inherently linear, however, they hold some limitations that affect linearity.

If the transfer characteristic of the converter becomes a function of the low-frequency signals present in the supplying voltages, distortion will occur. Similar effects happen with clock feedthrough of the switches or when different amounts of charge are taken for the two different output bits.

An important limitation for linearity is when memory exists between output levels. When using an NRZ modulation scheme the power of each symbol is dependent of the previous. It is imperative to use an RZ or some other memory free modulation scheme, so all symbols are transmitted with the same power.

3.5.3 Idle Tones

When a DC level is applied to a 1-bit quantiser, the output will be a periodic sequence of 1s and 0s. For instance, if we apply a level of 1/2 we get the sequence:

$$y(n) = \{1,0,1,0,1,0,...\} \tag{3.23}$$

This pattern has a period of two cycles and thus its power is around $f_s/2$. If we apply a lower level of 1/4 we would get a sequence with period $f_s/4$:

$$y(n) = \{1,1,1,0,1,1,1,0,...\} \tag{3.24}$$

Such high frequencies would be removed by the post processing low-pass filter. But imagine we have a DC level that produces much lower frequency tones and that the OSR is low. With an oversampling ratio of 16 and a tone at $f_s/32$, the filter would not remove the tone.

It is worth mentioning that these tones might not lie on a well defined frequency but instead may vary randomly in a given bandwidth.

3.5.3.1 Dithering

In order to remove any idle tones, it is necessary to perturb any possible cycles, by favouring the random behaviour. Accordingly, since the cycles are due to correlated behaviours, it is necessary to use an auxiliary input capable of breaking the cycles. This method is called dithering and the auxiliary signal is the dither. Obviously the dither must be effective against the tones and should not alter the signal.

3.5.4 In-band Tones

If the threshold voltages of the two input transistors of the opamp do not match, an offset will incur. The effect is similar to a voltage mismatch. Thus additional tones will appear in the spectrum.

Other gain mismatches, caused by capacitor mismatch fabrication, will add even more tones to the spectrum, thus affecting the SNR in the bandwidth of interest. Gain mismatches are relevant in multi-path architectures as applying different gains to each path results in an extra in-band tone. Clock skew also generates tones that can easily and severely damage the SNR.

3.5.5 Opamp Gain

All previous calculations take into account a infinite gain amp-op. A finite gain limits the quantisation noise shaping, since the NTF will not be zero at DC but close, for the low-pass case. The resulting transfer function, for a switch-capacitor integrator, taking into account the finite gain A, is:

$$\frac{V_{out}(Z)}{V_{in}(Z)} = -\frac{1}{Z\left(1+\frac{1}{A}\right)-1} \tag{3.25}$$

The NTF's zeros will now be at $Z = (1-1/A)$. The 3 dB break frequency will now be around 1/A rad/sample. The band of interest should be greater than that frequency since quantisation noise is flat below and noise-shaping is not being used, thus not benefiting from that. We can write the following requirement:

$$\frac{f_0}{f_s} > \frac{1/A}{2\pi} \tag{3.26}$$

Since $OSR = f_s/(2f_0)$:

$$A > \frac{OSR}{\pi} \tag{3.27}$$

As a rule of thumb, designers will ensure that the opamp gain is at least twice the oversampling ratio.

3.6 Continuous Time ΣΔ Modulators

In discrete time, sampling is done before the modulation while in continuous time sampling is only done after the loop filter, thus working with an s domain transfer function. Fig. 3.20 illustrates the internal workings of the modulator in the different time domains.

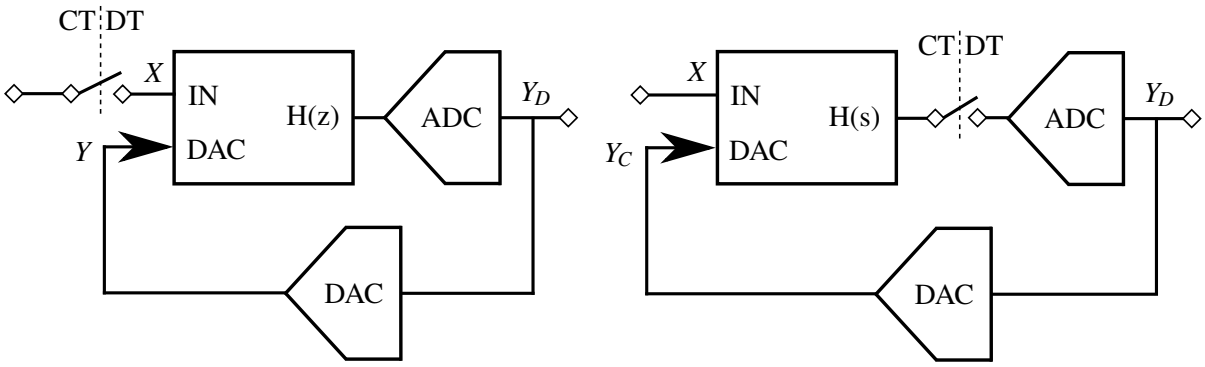

Figure 3.20: DT (left) vs CT (right) converter.

CT modulators can be integrated in any available bipolar technology such as BiCMOS, whereas DT circuits cannot. In CT, sampling occurs inside the loop which means any non-idealities are also attenuated, as quantisation noise is. Since, in DT, sampling occurs outside the loop, sampling non-ideal effects have higher degrading impact on performance.

Because the feedback and input are step signals, a DT converter's integrator requires a big slew-rate. In CT, since conversion is distributed over the clock, slew-rate can be lower. This, however, represents a disadvantage as well. Supply voltages are also lower in CT since DT switching requires high voltages [29][30].

Since the coefficients in a DT switch-cap approach are set by the ratios between capacitors, the clock rate can be chosen arbitrarily, taking into account technology limits. In a CT approach coefficients are determined with ratios between time constants and sampling period, thus fixing the sampling rate. The STF on a CT converter is not flat while it is for its counter-part. Common-mode rejection is much bigger in the DT case. Although not properly discussed here, the DAC in the feedback loop is quite important for CT solutions since its errors affect conversion performance [31]. This is a big contributor for the main problem of CT modulation, which is the limitation in linearity.

CT solutions are advantageous for large bandwidth signals and lower power consumption. Cellphones, for instance, communicate using several protocols, at different carriers. DT approaches allow for easy frequency tuning, unlike CT converters. One could use fewer converters in devices by choosing DT converters over CT.

3.7 State-of-the-art of ΣΔ ADCs

Tables 3.1, 3.2 and 3.3 enumerate some recent Sigma Delta Modulators, using continuous and discrete time approaches. Only band-pass type converters are presented for the CT architecture, while low and band-pass are shown in the DT case. DT band-pass ΣΔ converters are few compared to CT, with little to no development over the past ten years.

Several parameters were collected and displayed here. Note that the used FOM expression is the band-pass adaptation, if the converter is of band-pass type (expression 2.16). Further calculation was made as not all authors presented the converter's FOM or the used adaptation. Some solutions will be discussed in more detail depending on relevance.

Despite continuous-time architectures not being the focus of this dissertation, it is still relevant to perform a state-of-the-art research on the matter, for a performance comparison. CT approaches are more commonly used for high sampling frequencies.

The authors in [33] propose a very interesting approach by using under-sampling to lower the sampling frequency to $3f_s/4$, from the usual $f_s/4$. A signal replica at $f_s/4$ is also considered usable output because it can be applied to the digital signal processing circuit for down-conversion and filtering. The used area was $0.27\,\text{mm}^2$ with a supply voltage of $1.3\,\text{V}$. The actual sample frequency is $3.256\,\text{GHz}$ and central frequency $2.442\,\text{GHz}$.

Table 3.1: Current continous time BPSD Converters.

Ref.	**FOM_{BP}** (pJ/conv)	**f_s** (GHz)	**f_{IF}** (GHz)	**f_B** (MHz)	**SNDR** (dB)	**Power** (mW)	**Technology**	**Architecture**
[32]	29.6	3.8	0.95	1	59	75	0.25 µm BiCMOS	4^{th} order, 1-bit
[33]	2.3	3.3	2.4	25	34	26	0.13 µm CMOS	2^{nd} order, 1-bit
[34]	4.1	3	2.4	60	40	40	90 nm CMOS	6^{th} order, 1-bit
[35]	0.18	0.8	0.2	25	69	35	65 nm CMOS	6^{th} order, 17 level
[37]	0.654	4	0.55	100	69	550	65 nm CMOS	6^{th} order, 17 level
[38]	0.19	3.2	0.8	20	70	20	40 nm CMOS	6^{th} order, 1-bit
[39]	2.22	0.8	0.2	10	68	160	0.18 µm CMOS	6^{th} order, 2-bit
[68]	10	8.88	2.22	80	42	164	40 nm CMOS	4^{th} order, 6×1.5-bit
[69]	0.385	0.8	0.2	24	58	12	65 nm CMOS	4^{th} order, 9-level

The architectures described in [38] and [68] use 40 nm process. A sixth order architecture with 1 bit quantiser is used [38] in while [68] used an array of 6 TI 1.5 bit quantisers, relaxing clock requirements, achieving the highest sampling frequency reported so far at 8.88 GHz. [38] used 0.4 mm^2 with 1 V supply and 0.4 mm^2, with supply at 1.1 V.

In [34], two TI 1-bit quantisers. It also makes use of the under or, here called, sub-sampling technique. Previous converters have yielded an SFDR, at most, a few dB more than the SNDR. This work managed to achieve an SFDR of 62 dB and SNDR of 40 dB. Total active area use is 0.8 mm^2. A supply voltage of 1 V achieves a power consumption of 40 mW.

The work in [69], better detailed in [67] uses only 12 mW and still achieves good SNDR values. The low power is due to the introduction of a single-amplifier resonator, which halves power consumption. The used area was 0.2 mm^2 with supply at 1.25 V. It also achieved the lows FOM at 0.385 pJ/step.

A complex highly tunable structure is presented in [37]. Both low and band-pass structures are available. IF frequencies vary from 0 to 1 GHz. With IF at 550 MHz, a 100 MHz BW is achieved. If the IF is placed at 1 GHz, BW is only 35 MHz. The full chip uses 5.5 mm^2 area with dual 2.5 V and 1 V supplies. Power consumption is high at 550 mW but FOM is only 0.654 pJ/step.

Table 3.2: Current discrete time switch capacitor Bandpass Sigma-Delta Converters.

Ref.	**FOM** (pJ/conv)	$\mathbf{f_s}$ (MHz)	$\mathbf{f_{IF}}$ (MHz)	$\mathbf{f_B}$ (MHz)	**SNDR** (dB)	**Power** (mW)	**Technology**	**Architecture**
[41]	8	26	6.5	5	26	2	0.18 µm CMOS	4^{th} order, 1-bit
[36]	0.25	200	50	10	46	2	0.18 µm CMOS	4^{th} order, 5×TI, 3-bit
[42]	64.2	40	10.7	0.2	79	208	0.15 µm CMOS	6^{th} order, 4-bit
[3]	2.22	120	40	2.5	69	150	0.18 µm CMOS	6^{th} order, 3-stage MASH, 5-level
[46]	20	80	20	2.5	61	44	0.18 µm CMOS	6^{th} order, 3-bit
[11]	1.8	120	40	1	65	16	0.18 µm CMOS	4^{th} order, 2-path TI, 4-bit

One can easily see that switch capacitor converters are more suitable for lower frequency uses. The lowest power consumption examples are [41] and [45], using only 2 mW, something quite valuable for mobile applications. There are significantly fewer discrete-time converters than their continuous-time counterparts. No band-pass DT converters have been published in recent years. Existing converters of this type have low sampling rates, no more than a few hundred MHz.

In [46], a tunable band-pass modulator is introduced with noise-coupling to increase the effective order of the modulator by two, from 4^{th} to 6^{th} order shaping, retaining the power consumption of the former. Unfortunately the noise shaping is not the most efficient one as there are three zeros at different locations, with only one at the IF frequency. No area figures are mentioned.

Fourth order noise shaping is used in [11], again with a two-path architecture but with a second-order modulator in each path. Noise cross-coupling between both paths is also implemented. The NTF zeros are intentionally split apart so the bandwidth is increased. Therefore two close notches can be observed in the band of interest, close to each other. The chip consumed an area of 0.44 mm^2. One can observe that chip sizes are relatively similar throughout the presented state-of-the-art converters, despite the different technology sizes in use.

A simple two-path with noise cross-coupling and a low-pass modulator on each path is used in [3], thus achieving 2^{nd} order band-pass noise shaping, at $f_s/3$. This converter is then applied to a 3-stage MASH structure in order to achieve an overall 6^{th} order noise shaping. Compared with other cross-coupling approaches, this one achieved the highest SNDR at 72 dB but with high power consumption, 150 mW. There was no optimisation made in this matter though. Despite the complex MASH structure, each stage is composed by a simple and straightforward architecture.

A direct comparison between band and low-pass converters is not fair. Despite this, a brief research on low-pass converters is still pertinent. Discrete-time converters of low-pass type are

shown in Table 3.3.

Table 3.3: Current discrete time switch capacitor Lowpass Sigma-Delta Converters.

Ref.	**FOM** (pJ/conv)	$\mathbf{f_s}$ (MHz)	$\mathbf{f_B}$ (MHz)	**SNDR** (dB)	**Power** (mW)	**Technology**	**Architecture**
[40]	1.03	450	25	63	56.7	0.13 µm CMOS	3rd order, varying bit number
[43]	0.07	240	5	77	4.2	65 nm CMOS	3rd order, 2-1 MASH, 4-bit
[44]	0.75	120	2	53	1.56	90 nm CMOS	2nd order, 9-level, 2-path TI
[45]	0.75	120	2	56	1.56	90 nm CMOS	2nd order, 3-bit, 2-path TI
[47]	0.09	240	5	71	12	0.13 µm CMOS	3rd order, 2-path TI, 9-level
[48]	0.26	240	15	66	12.7	22 nm CMOS	2nd order, 8-bit
[49]	0.6	400	20	64	34.7	0.13 µm CMOS	3rd order, 3.5-bit

The work in [40] has a complex architecture, making use of a multi-level quantiser that changes the number of levels depending on the chosen bandwidth. This allows for high reconfigurability. The sampling frequency is the highest amongst the presented converters.

The approach in [48] is interesting regarding the scope of this dissertation. It is implemented using Intel's 22 nm Tri-gate technology. It occupies an area of only 0.04 mm^2 while retaining a complex topology.

Two similar converters are described in [44] and [45] using a two-path, noise-couple, low-pass architecture. A PhD thesis better reports the circuit [50]. The first one presents a SNDR of 53 dB against the 56 dB of the second. Despite this, the latter uses one comparator less in the quantiser. This is quite an interesting approach since by simply feeding the quantisation noise of one path to the other, one can significantly improve the noise shaping and thus the in-band SNR. This architecture also shares the opamp so that only one is used for both paths, since each path only uses it half the time. This does require for it to run at full clock rate instead of the usual half-rate. No area figures are mentioned.

Although the work in [43] presents the lowest FOM, it is accomplished with quite complex circuitry, using two-stage MASH structure with one stage of 2nd and the other of 1st order. Used area is only 0.066 mm^2.

Another use of the two-path with noise cross-coupling is in [47], thus increasing the noise shaping to third order. It achieved the lowest FOM value of only 90 fJ/conversion. Area usage is 0.328 mm^2.

The converters in [44] and [45] make use of the two-path TI structure with noise-cross coupling, only achieving a low-pass noise modulation instead of band-pass in [3]. One can see that noise-coupling has been an active topic of research in recent years and in the field of ΣΔ modulation. For the band-pass topology it is quite useful as one can reduce complexity by simply using low-pass filters in each path. The converter used in each of the stages in [3] is quite simple and robust and also achieving good results. Since a dissertation document is available, a more detailed explanation of the implementation is accessible which is of high value in understanding how to implement this particular converter. As this converter will be the basis of this dissertation work, the details of the achieved performance and implementation will be discussed in more detail. No 28 nm converters are presented as none were found. This technology is still not being actively deployed in the field of ΣΔ conversion thus proving its state-of-the-art status.

3.8 Cross-Coupled Two-Path Bandpass ΣΔ Modulator

The work reported in [3] was later detailed in the PhD dissertation [4]. It proposed a two path time-interleaved ΣΔ modulator, with cross-coupling of the noise terms between the two paths, shifting the notch position from the regular $f_s/4$ to $f_s/3$. This relaxes requirements on hardware by avoiding tones present at $f_s/4$, caused by either path gain mismatch or opamp offset, as shown in Fig. 3.21.

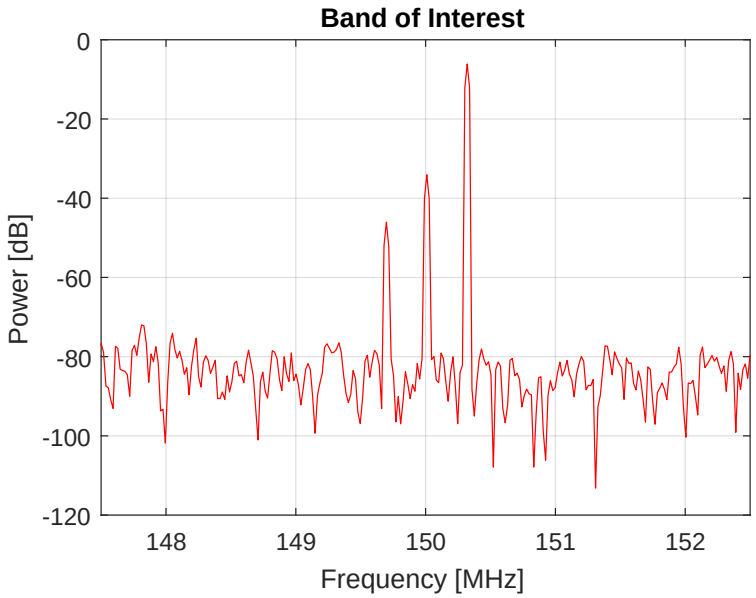

Figure 3.21: Example of the path-mismatch and opamp offset tones present in the signal band.

Each path makes use of a highpass modulator $(1+z^{-1})$, with a zero at $f_s/2$. It is implemented by modulating the input and output of the low-pass modulator with a 1, -1, 1, -1 sequence, resulting in a $z \rightarrow -z$ transformation. This technique is called chopping.

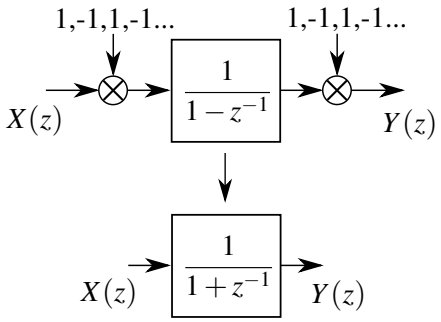

Figure 3.22: Lowpass to highpass transformation.

The NTF for a standard 2nd order ΣΔ converter is $1+z^{-2}$, which fixes the NTF zero at $f_s/4$. The second order transformation, $z \to z^2$, is done according to the multi-rate theorem described in Section 3.3.3. The notch is shifted to $f_s/3$ by introducing an extra z^{-1} term, using cross-coupling of the noise terms between the two paths. This is an efficient design as the the cross-coupling paths barely add any hardware cost on the converter, while relaxing requirements on several composing blocks of the modulator. The block diagram can be seen in Fig. 3.23. By analysing the block diagram, the overall transfer function can be calculated [4]:

$$Y = X z^{-3} + (1 + z^{-1} + z^{-2})\, E \tag{3.28}$$

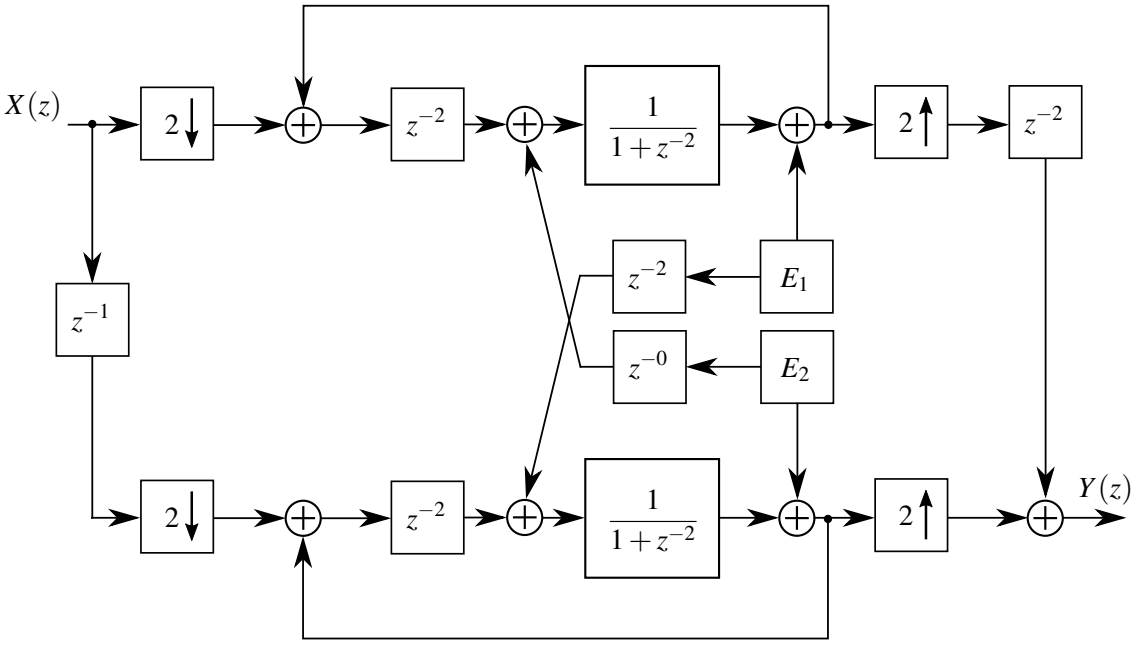

Figure 3.23: Block diagram of the converter proposed in [3][4].

The complexity of this design is very similar to the low-pass case. This modulator is later used in a 3 stage MASH structure, achieving 6^{th} order noise shaping. Though, ideally, the MASH structure should be stable, as the only requisite is that each stage is itself stable for global stability, the overall converter had issues regarding this matter. It would be interesting to improve the single stage modulator, without adding too much complexity, by further noise shaping using cross-coupling of the quantisation noise.

The circuit was implemented on 0.18 µm, using 1.1 mm^2 of area. The effective sampling frequency is 60 MHz, with IF at 40 MHz, BW of 2.5 MHz and 72 dB SNR, consuming 150 mW.

Chapter 4

CMOS RF ΣΔ Converter

4.1 Architecture definition

The architecture that is studied in this dissertation is inspired in the work reported in [4], it actually forms the grounds for the proposal that is reported next. As discussed before, this converter placed the notch frequency at $f_s/3$ instead of the usual $f_s/4$, thus avoiding two common problems: the operational amplifier offset and the gain mismatch image caused by unbalanced paths in the time-interleaved scheme. Consequently, a higher frequency notch allows lower sampling rate.

Since the targeted sampling rate for this dissertation is 1.6 GHz, there is a big gap to [4]'s 120 MHz, by a factor of around 13. The used technology was 0.18 µm, thus 28 nm should enable most of the rate boosting needed. As mentioned in Chapter 1, the end goal of this work targets mobile applications, which require low power consumption. The reported work in [4] consumed 150 mW but no optimisation for any particular application was made.

The topology used in [4] involved the MASH structure, cascading three 2^{nd} order converters to achieve a 6^{th} order one. This severely complicates the circuit which has many particular aspects that can easily cause the modulator to fail. Considering the promising results, mainly regarding the SNDR, it would be interesting to replicate them using less complex architectures.

Finally, [4] achieved the reported performance for a 2.5 MHz bandwidth and current mobile communication standards transmit 5 to 100 MHz bandwidths.

4.2 Proposal

In [4] is concluded that it was impossible to remove all inband tone causing imperfections with, at the time, present technology. The traditional architecture, with NTF $(1+z^{-2})$, has unwanted tones in the signal band. This was the authors' motivation to extend the function to $(1+z^{-1}+z^{-2})$. By

replacing z with $e^{j\omega/f_s}$ we calculate the zeros' placement:

$$\begin{aligned} |1+e^{-j\omega/f_s}+e^{-j2\omega/f_s}| &= 0 \\ &= 1+2\cos\omega/f_s \end{aligned} \tag{4.1}$$

The zero is achieved for $\omega/f_s = 2\pi/3$, or $f_0 = f_s/3$.

The problem now is that we do not want to increase the system complexity, yet, for better results, one would have to resort to higher-order modulation. To avoid complexity, one can add a single zero thus having a highpass behaviour or, a pseudo 3rd order band-pass converter. If the second zero is placed after the initial one, this means that the signal's band is increased, by creating a flatter noise curve. This way, it is possible to tune different bandwidths with quite similar performance.

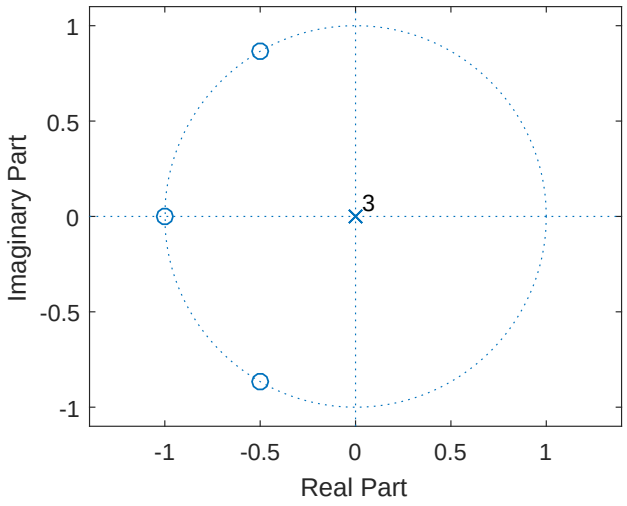

Figure 4.1: Pole-zero plot of the proposed transfer function.

The second zero can be added by multiplying the previous NTF by $(1+z^{-1})$ resulting in $(1+2z^{-1}+2z^{-2}+z^{-3})$. This fixes the second zero at $f_s/2$ or Nyquist, which is the only place where a zero can be added with 3rd order. Fig. 4.1 shows the pole-zero diagram of the proposed NTF. The second zero is too far away from the first one, thus no advantage is achieved. The only solution is to shift the first closer to Nyquist. A tunable notch is achieved with NTF $(1+az^{-1}+az^{-2}+z^{-3})$, where a is the notch tuning gain. With $a=2$ the $f_s/3$ notch is achieved and right shifting with increasing a. Applying the same process as in Eq. (4.1) a precise relationship between notch frequency and parameter can be calculated:

$$a = 1-2\cos\left(2\pi\frac{f_{notch}}{f_s}\right) \tag{4.2}$$

It is known how to generate the $(1+z^{-1}+z^{-2})$ noise transfer function. Now, it is necessary to determine how to modify the schematic and add the desired gains along with the extra z^{-3} term.

4.3 3rd Order Bandpass ΣΔ Converter

The original design [4] implements a 2nd order converter. 3rd order band-pass loop filters do not exist. Since the z^{-1} term was added by the cross coupling of the noise terms, this reasoning can be extended to introduce the extra z^{-3}. Simply adding an extra noise coupling path, but with two extra delays, one can achieve the desired result.

Adjusting the z^{-1} term gain is straightforward as this is achieved by directly introducing an amplifier on the cross coupling path. The z^{-2} term is generated by the loop filter and thus requires a modification to it. A $1/(1+az^{-2})$ filter has to be introduced along with a feedback gain of a to cancel out the delayed output feedback term. The final proposed converter is shown in Fig. 4.2.

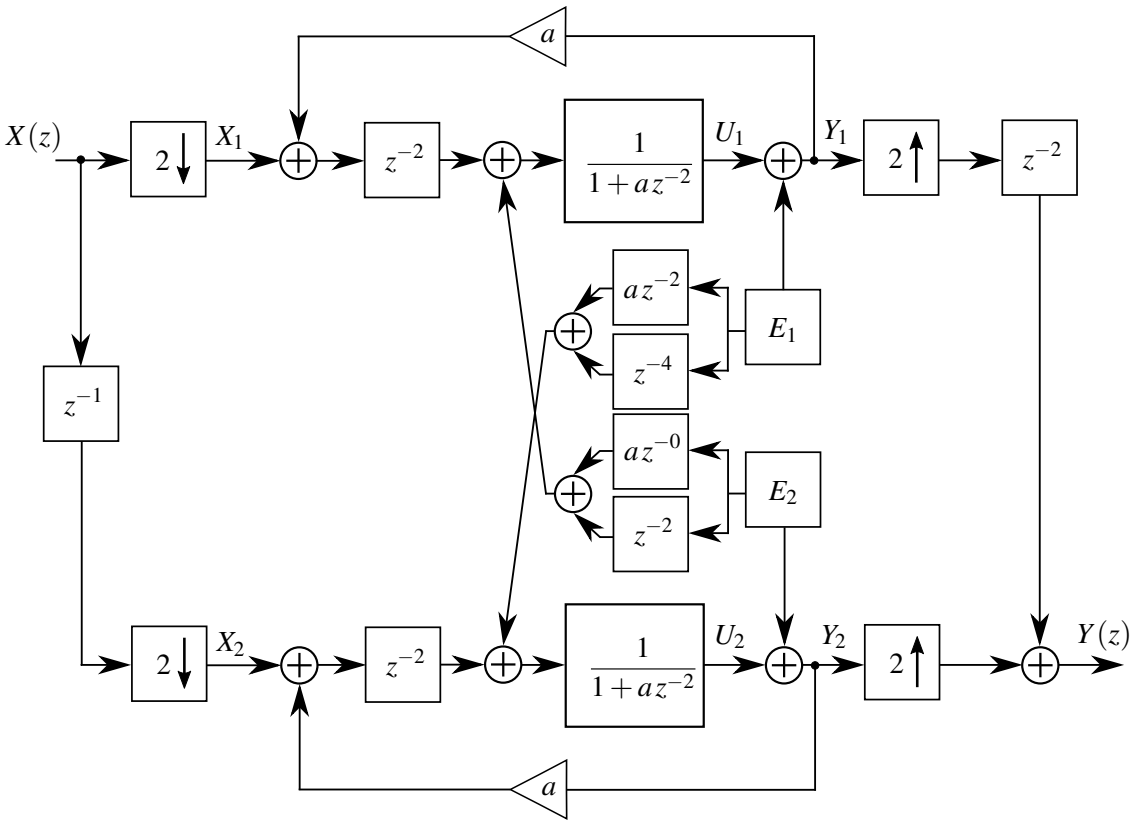

Figure 4.2: Block diagram of the proposed 3rd order BP ΣΔ converter.

The overall transfer function of the schematic presented in Fig. 4.2 is now deduced. The first path's output is:

$$\left[(X_1+aY_1)z^{-2}+E_2\left(a+z^{-2}\right)\right]\frac{1}{1+az^{-2}}+E_1=Y_1 \tag{4.3}$$

$$Y_1 = X_1 z^{-2} + E_2\left(a + z^{-2}\right) + E_1\left(1 + az^{-2}\right) \tag{4.4}$$

The output of the second path is:

$$Y_2 = X_2 z^{-2} + E_1\left(az^{-2} + z^{-4}\right) + E_2\left(1 + az^{-2}\right) \tag{4.5}$$

After up-sampling, both outputs are combined by adding Y_2 to a unit delayed version of Y_1:

$$\begin{aligned} Y &= Y_1 z^{-1} + Y_2 \\ &= \left(X_1 + X_2 z\right) z^{-3} + z^{-1}\left(1 + az^{-1} + az^{-2} + z^{-3}\right) E_1 + \left(1 + az^{-1} + az^{-2} + z^{-3}\right) E_2 \\ &= X z^{-3} + \left(1 + az^{-1} + az^{-2} + z^{-3}\right) E \end{aligned} \tag{4.6}$$

As demonstrated, the desired noise transfer function $\left(1 + az^{-1} + az^{-2} + z^{-3}\right)$ is achieved.

4.4 Stability

Stability is a critical property of ΣΔ converter design due to the non-linear feedback control system. If unstable, the system's output may be unbounded for certain inputs. Often, in the ΣΔ converter, integrator stability is critical for zero input and a DC stimuli. Each path is a first order ΣΔ modulator, which is unconditionally stable [51][28]. Despite this, introducing cross-coupling noise terms challenge stability as does the use of an unstable integrator $\left(1 / \left(1 + az^{-2}\right)\right)$. A deeper analysis will be done.

Despite the integrator having its poles outside the unit circle, thus making it unstable, the overall modulator is not as feedback moves them back into the unit circle. One can perform a time-domain analysis of one path. From Fig. 4.2 the integrator's output u for the first path is:

$$\begin{aligned} u_1[n] &= x_1[n-1] + a\,y_1[n-1] + a\,e_2[n] + e_2[n-1] - a\,u1[n-1] \\ &= x_1[n-1] + a\,e_2[n] + e_2[n-1] + a\,e_1[n-1] \end{aligned} \tag{4.7}$$

Ideally, the quantisation errors are bounded. Assuming the same for input, the integrator's output will be stable. Under normal operation conditions, the input will be bounded to operating voltages. But, if by any reason, it is not, or if there is a high voltage injected somewhere in the circuit, the quantiser will be saturated and the quantisation error will no longer be bounded. For a standard integrator this would not be a problem [4] but the used one imposes a multiplying a term on previous errors. Under these conditions, the modulator is unstable. Since the opamp's output saturates to the quantiser's input range, instability is never actually achieved. The simulated output of one of the converter's integrators can be seen in Fig. 4.3.

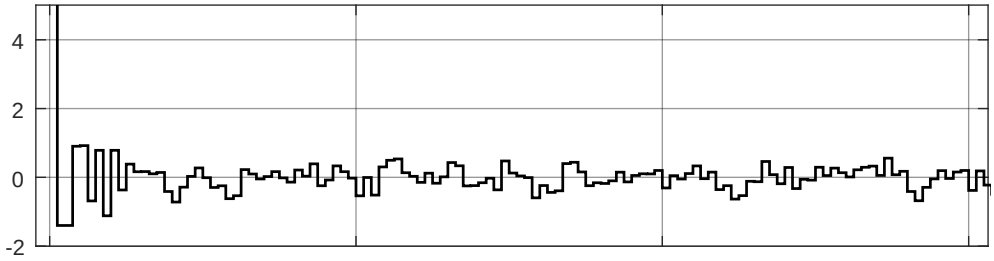

Figure 4.3: Output of the converter's integrator.

4.5 Simulation Results

The system was simulated using Mathwork's tools MATLAB and Simulink Toolbox. Fig. 4.4 shows the implemented Simulink model of the proposed converter. This model is launched from a configurable MATLAB script for quick programmable simulation. This is useful to promptly benchmark performance measures for circuit level simulations.

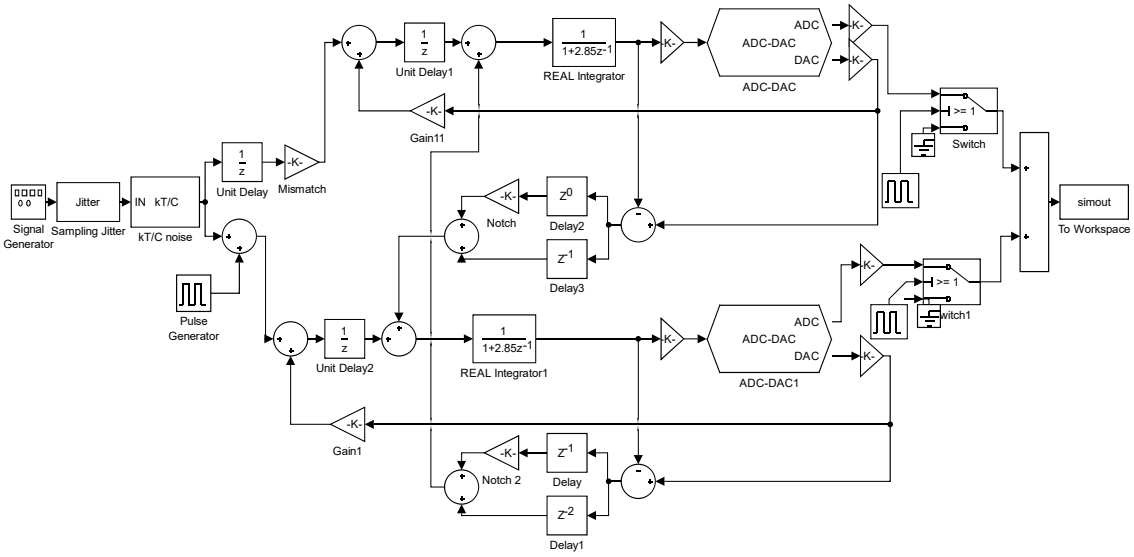

Figure 4.4: Simulink model diagram of the proposed converter.

Non-idealities are introduced in the system, as described in [52]. Clock jitter and thermal noise are modelled as additive white noise. The op-amp offset is introduced as a $f_s/4$ pulse. The integrator model takes into account op-amp finite gain, slew rate and settling. Some modifications had to be done to [52], as the latter used a standard integrator model, not suitable for this application. The gain mismatch between both paths is achieved applying a different gain for each one. The ADC uses 4 bits in quantisation and the DAC simulates capacitor mismatching. The output data is fed back to the MATLAB workspace for further processing. The output spectrum is plotted, the

achieved SNR is calculated and compared against theoretical values.

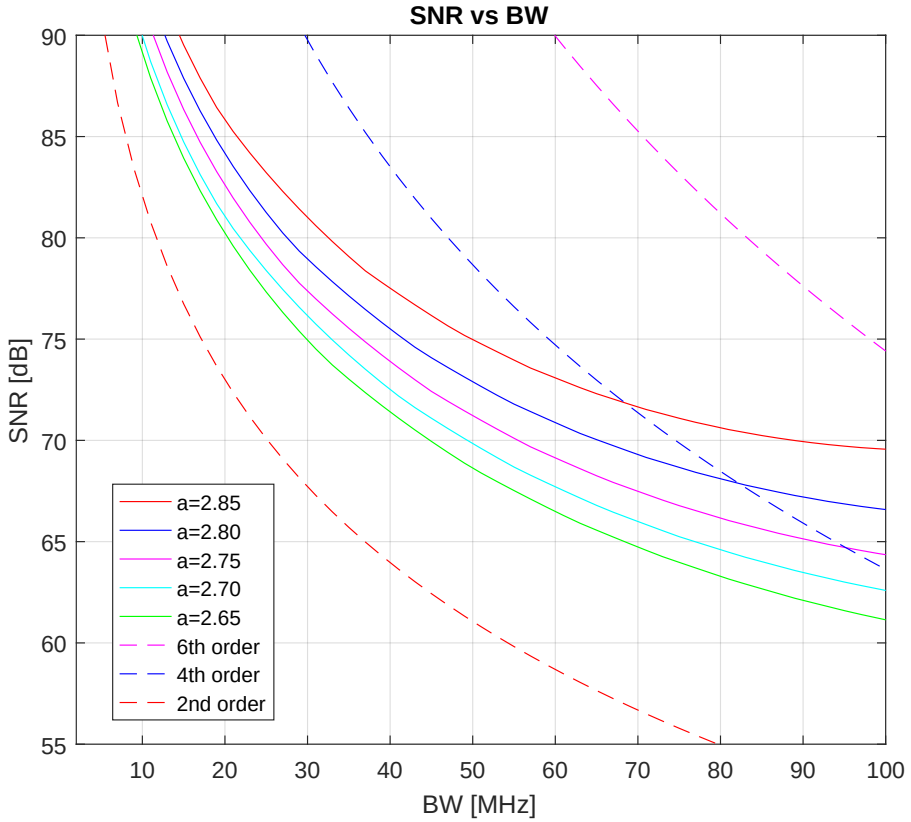

Figure 4.5: Theoretical SNR for different bandwidths and notch frequencies.

Fig. 4.5 shows a plot of theoretical SNR values versus bandwidth, for several notch positions, controlled by the a parameter, and also the [4]'s results in a 2^{nd}, 4^{th} and 6^{th} order extrapolation. The curves are generated using the noise power calculated from the integral in expression 3.7. A 4 bit quantiser and full-scale input are assumed. One can see the increase in SNR with increasing notch frequency. Depending on the chosen notch position and bandwidths, one can surpass the results achieved by the 2^{nd} and 4^{th} and also get close to the 6^{th} order converter. As one can observe, the SNR curve for the proposed converter gets much flatter with increasing bandwidth.

Normally the measured bandwidth is centred around the notch's frequency. Since this converter makes use of a second zero at Nyquist, there is an asymmetry in the noise shaping curve. This implies that the optimal centre for the bandwidth or f_0 is not coincident with the tuned zero's frequency. From simulation it was concluded that the bandwidth centre is at $1.04\,f_{IF}$.

For $a = 2.85$, which corresponds to a 700 MHz notch, one can expect SNR of 86 dB, 77 dB and 69 dB for BW of 20 MHz, 40 MHz and 100 MHz respectively. The input saturation limits were simulated to be around −4 dB. This will be discussed further on.

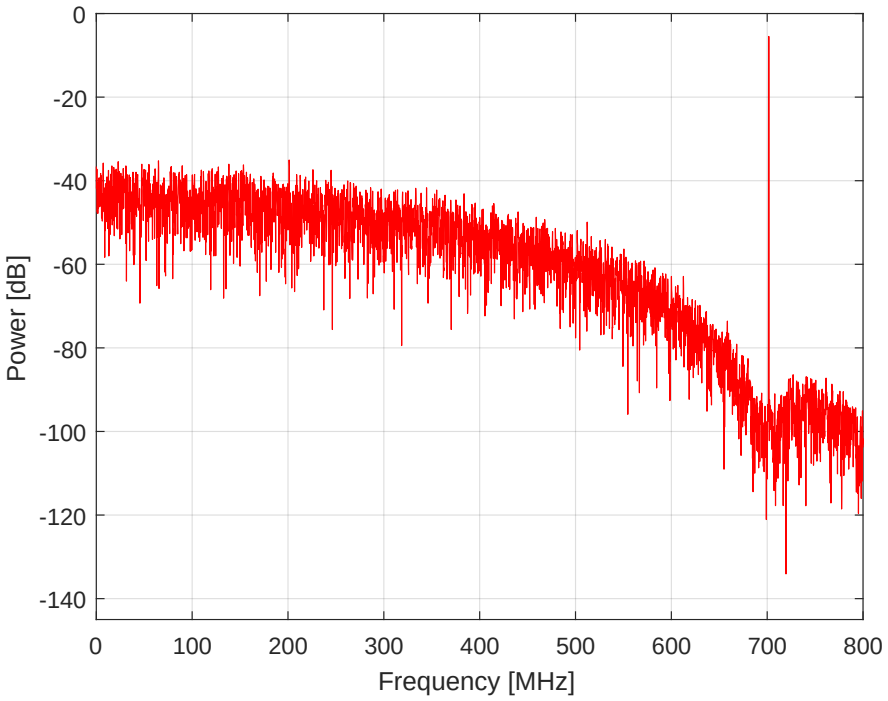

Figure 4.6: Matlab simulated output power density spectrum.

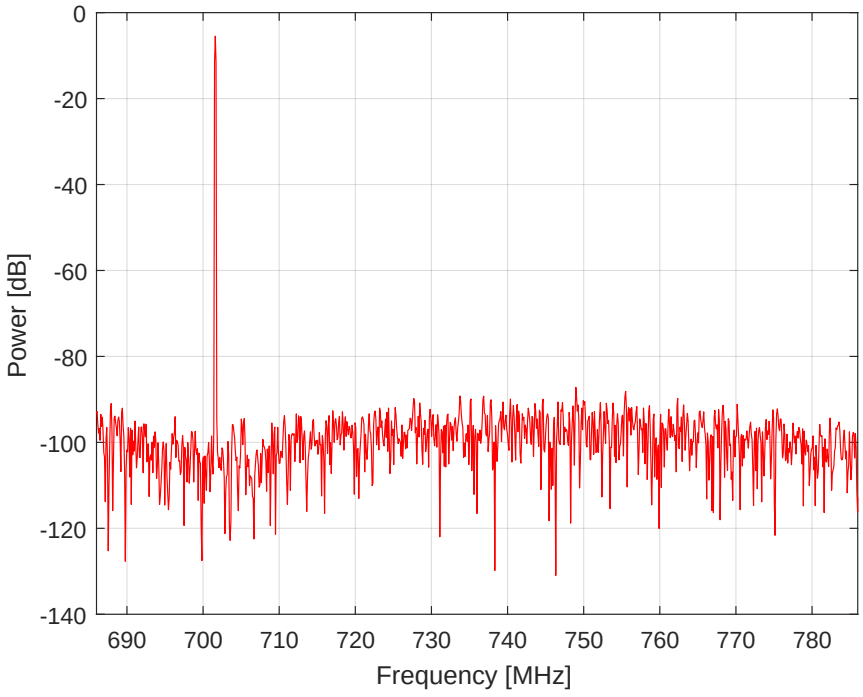

Figure 4.7: Matlab simulated spectrum in the signal band.

The power spectrum of the converter's output is shown in Fig. 4.6 and a bandwidth zoom in Fig. 4.7. Each path operates at half of the effective clock rate, so 800 MHz each. The zero was chosen to be at 0.46 f_s or 736 MHz, because of LTE standards [53], which forces $a = 2.85$. One can tune it to any desired position but closer to Nyquist rate achieves higher SNR. The second zero is inherently fixed at Nyquist rate by the architecture design. This design requires strict AA (anti-aliasing) filters. One has to leave a big enough safety margin from Nyquist so the image spectrum can be safely removed and no aliasing occurs, but also no attenuation affects the signal.

With this setup, for bandwidths of 20 MHz, 40 MHz and 100 MHz, SNR of 76 dB, 70 dB and 64 dB are achieved respectively. Even with path gain mismatch, clock skew and opamp offset added in the simulation, no parasite tones are observed in the band of interest, as one expected, and overall results are close to theoretical values. This forms a proof of concept for the extra noise coupling term added by performing the $1 + 2.85z^{-1} + 2.85z^{-2} + z^{-3}$ noise transfer function.

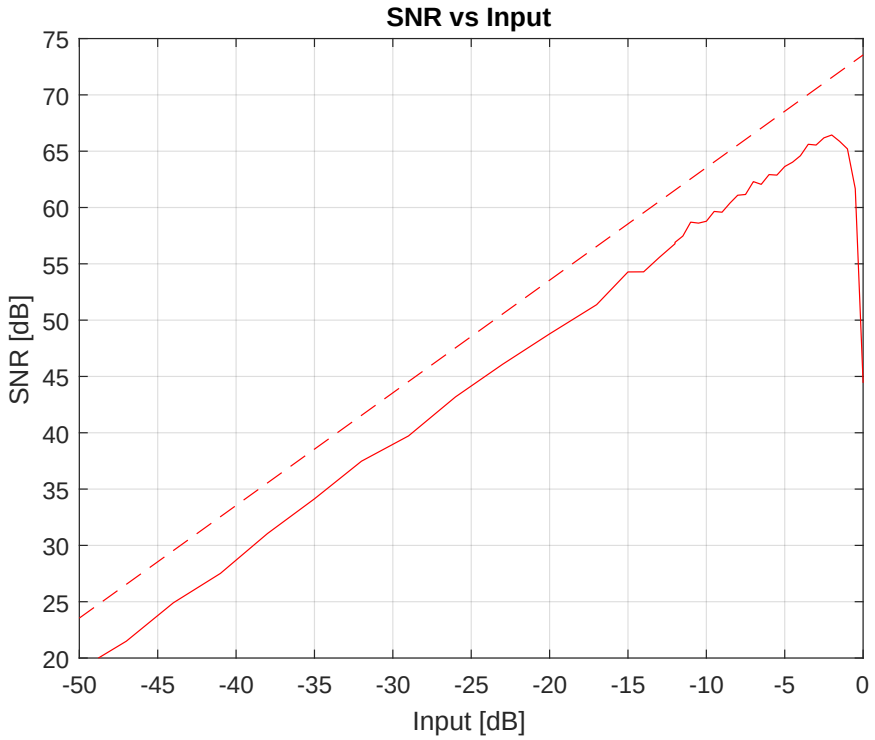

Figure 4.8: Simulation of achieved SNR versus input power.

In order to understand the limits of the input signal which saturate the converter, the input power was swept. The SNR was calculated using both the real and ideal models of the converter. An OSR of 8 was used, corresponding to the 100 MHz bandwidth. Results are shown in Fig. 4.8. They are plotted against theoretical values, represented with a dashed line. In the range of −50 dB to −2 dB input, the results are close to theoretical calculations, while with inputs bigger than −2 dB saturation occurs and the SNR quickly drops to zero.

A sweeping of the bandwidth was made using the Matlab model of the converter, which took into account real non-idealities. The results are plotted in Fig. 4.9 against the theoretical values, with a dashed line. Real life limitations were taken into account such as a 70 dB opamp DC gain, 16 GHz GBW, opamp offset, path mismatch, jitter, kTC noise and opamp limited output swing. Results are in average about 5 dB apart from theory.

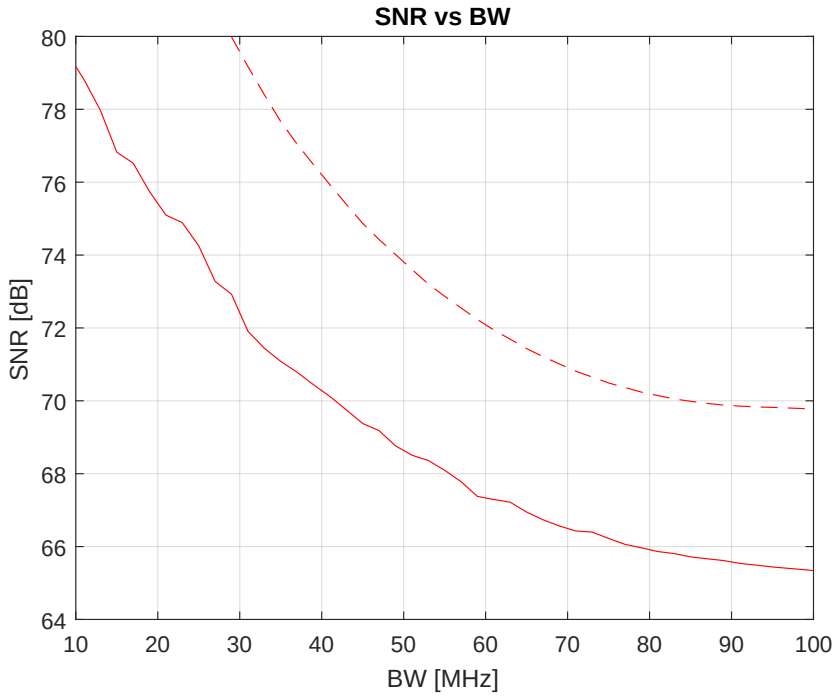

Figure 4.9: 3rd order converter Matlab simulated SNR values.

The DC gain and GBW requirements on the opamp were tested by sweeping these parameters and calculating the achieved SNR values. Fig. 4.10 plots simulated SNR values versus the opamp's DC gain. The three curves represent three different OSR values. One can see that the SNR saturates to about the open loop DC gain of the opamp. Thus, if a 70 dB SNR is desired, the DC gain should also be the same value and similarly for any other desired SNR. A GBW of 16 GHz, or 10 times the sampling frequency, was concluded to meet the specifications.

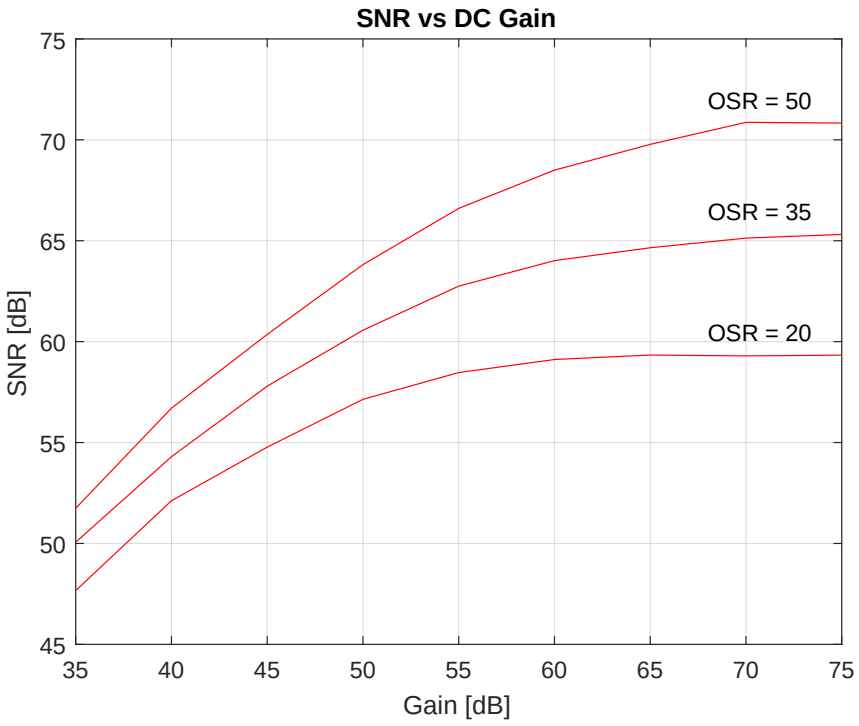

Figure 4.10: Matlab simulation plot of SNR vs op-amp DC gain.

Chapter 5

Circuit Implementation

This chapter describes the implementation at circuit-level of the proposed converter. The software used for the IC design was Cadence. References [54], [55] and [56] provided fundamental knowledge in electronics and circuit design as well as transistor layout design and problems.

5.1 Sampling Circuitry

Any switch-cap circuit requires sampling of the input signals. A voltage is applied to the sampling capacitors and the resulting charge will be later transferred between the circuits' capacitors. This requires the use of switches, which are implemented using MOS transistors. Two main problems they present are charge injection and clock feedthrough, capable of destroying the overall performance.

A transistor works as a switch by applying a voltage at the gate, thus allowing or not the flow of current from drain to source. Charge injection occurs when the parasitic capacitance connected to the gate discharges to the sampling capacitor, thus inducing an error, after sampling is completed and the switch is turned off. This effect has the added disadvantage of having a non-linear dependency on the input signal.

Bottom-plate sampling [57] can attenuate the charge injection effect. It consists on switching the bottom-plate of the sampling capacitor from ground slightly sooner than the input switch, leaving a floating capacitor with no more charge being accumulated. A constant offset will appear due to the earlier switching. It is often tolerable or even easily removed. Since the used circuitry is fully-differential, the offset will be removed at the output. Since bottom-plate sampling is widely used in the design of switched-cap circuits, and it is of most convenience to be used in the development of the present proposal, it will not be explicitly refereed throughout the dissertation, though it is always employed where it is convinient.

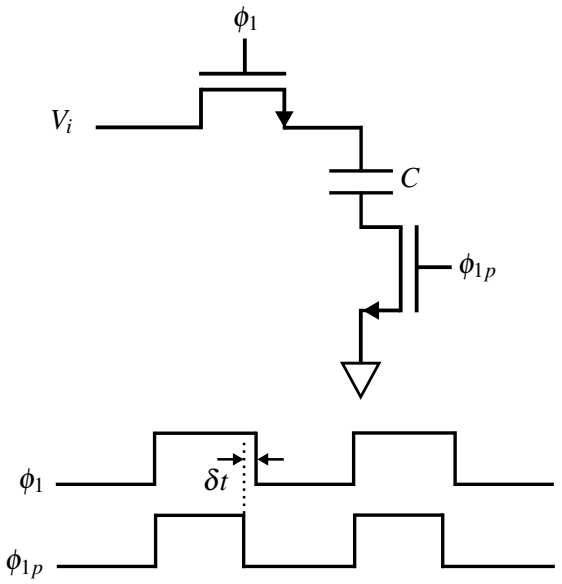

Figure 5.1: Bottom-plate switching.

5.2 Integrator

The integrator is the central block of the ΣΔ converter. It is the main block responsible for the noise shaping. The used switch-cap integrator's circuit diagram is shown in Fig. 5.2. In phase ϕ_1 the input and output signals are sampled using capacitors C_{s_1} and C_{s_2}, respectively. During the next phase ϕ_2, both sampling capacitors are connected to the input of the opamp thus transferring the stored charges to the feedback capacitor C_f. This phase completes the integration process.

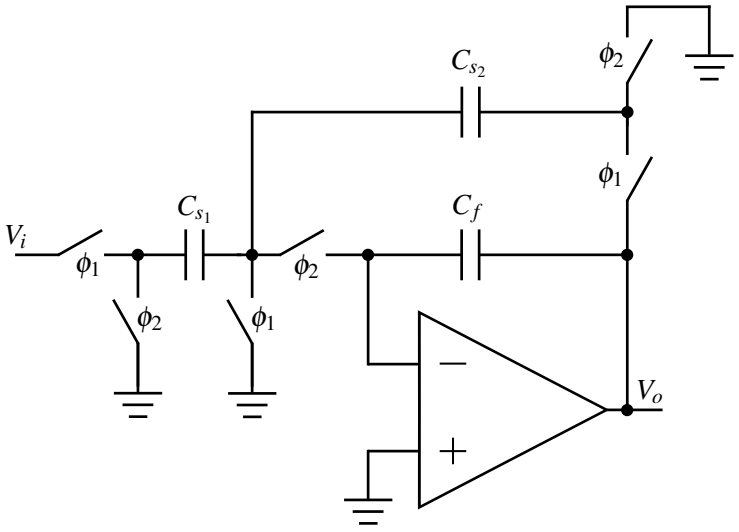

Figure 5.2: Circuit schematic of the deployed integrator.

Analysing the circuit we verify that the charge at the end of phases ϕ_1 and ϕ_2 are:

$$Q_{\phi_1} = -v_i[n-1]\,C_{s_1} - v_o[n-1]\,C_{s_2} - v_o[n-1]\,C_f \tag{5.1}$$

$$Q_{\phi_2} = -v_o[n-1/2]\,C_f \tag{5.2}$$

Taking into account that $v_o[n] = v_o[n-1/2]$ the final transfer function can be written as:

$$H(Z) = \frac{C_{s_1}}{C_f}\frac{z^{-1}}{1-(C_{s_2}/C_f+1)\,z^{-1}} \tag{5.3}$$

Thus $a = (C_{s_2}/C_f + 1)$. C_{s_2} must be 1.85 times bigger than C_f so $a = 2.85$.

In reality, a fully-differential integrator is used. This is done by mirroring the circuit, using both inputs of the opamp and a differential output as well. Two advantages of using fully-differential architecture is doubling the output swing and better rejection of the common-mode. Also, a unipolar supply can be used, i.e. V_{DD} and GND, with a V_{CM} centred signal.

5.3 Converter

The circuit diagram for one path of the converter can be seen in Fig. 5.3. The integrator presented before is used. To change the transfer function from $1-z^{-1}$ to $1+z^{-1}$ the input signal must be multiplied with a sequence of alternating 1 and -1. This achieved by feeding input the positive and negative signals alternately.

During ϕ_2 the feedback is integrated together with both noise cross-couplings. The non-delayed version is feed through a capacitor with $a \cdot C_u$ capacity, performing the necessary gain. The delayed version of the cross-coupling is more complicated. The output of the other path's integrator must be stored and only integrated during the next sample. To realise this, there are two capacitors that sample and inject this signal in alternating ϕ_2 phases, realising a full z^{-1} delay.

Unlike the block diagram, the other path is symmetrical except it uses complementary clocks. One other exception is the polarity of the cross-coupling. Since the input is modulated with a 1,-1 sequence, both paths are working with different polarities at any given instance. Thus the cross-coupling on the other path is fed with symmetric signal.

The circuit can be optimised by reusing some capacitors to inject different signals. This way, area is saved and the feedback factor is reduced from $1/(3a+2)$ to $1/(2a+1)$. For $a = 2.85$ this is an improvement from $1/10.55$ to $1/6.7$. The resulting circuit diagram is shown in Fig. 5.4. The result is achieved by simply rearranging the injection point of all signals. This optimisation not only saves area through less capacitors being used but also uses five switches fewer.

As this arrangement proved to require high swings at the output's integrator, one could apply a feedforward technique to relax requirements on that specific hardware. Using this technique the loop filter needs only to process the quantisation noise. This allows more efficient opamp architectures and relaxes linearity requirements [58].

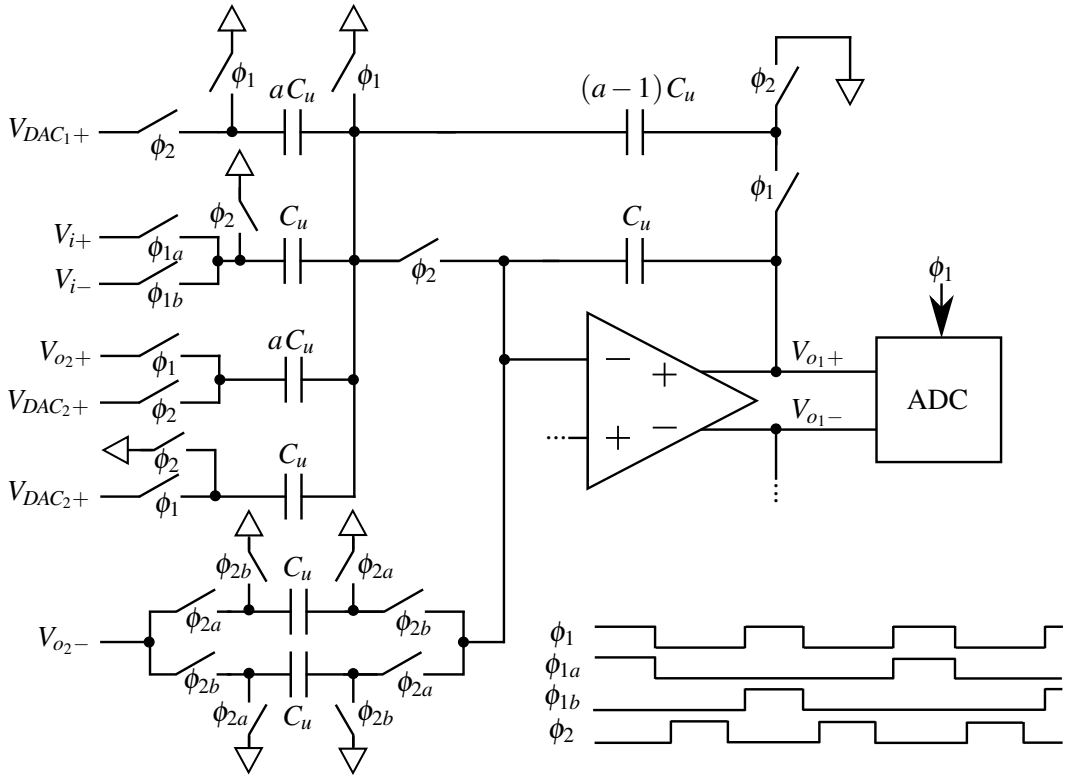

Figure 5.3: 3rd order band-pass ΣΔ converter schematic.

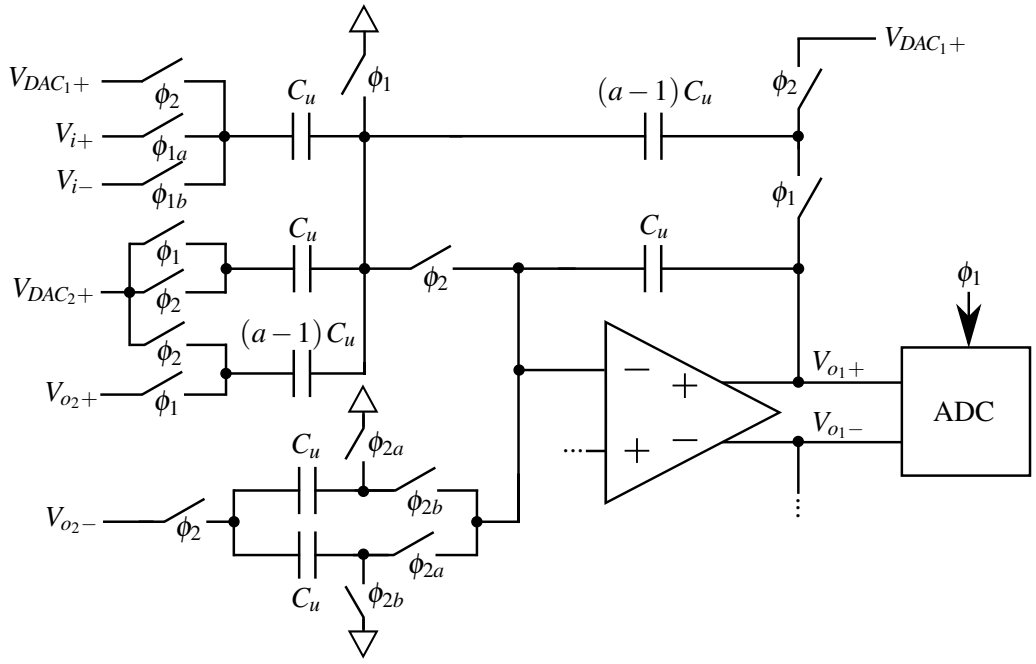

Figure 5.4: 3rd order band-pass ΣΔ converter optimised schematic.

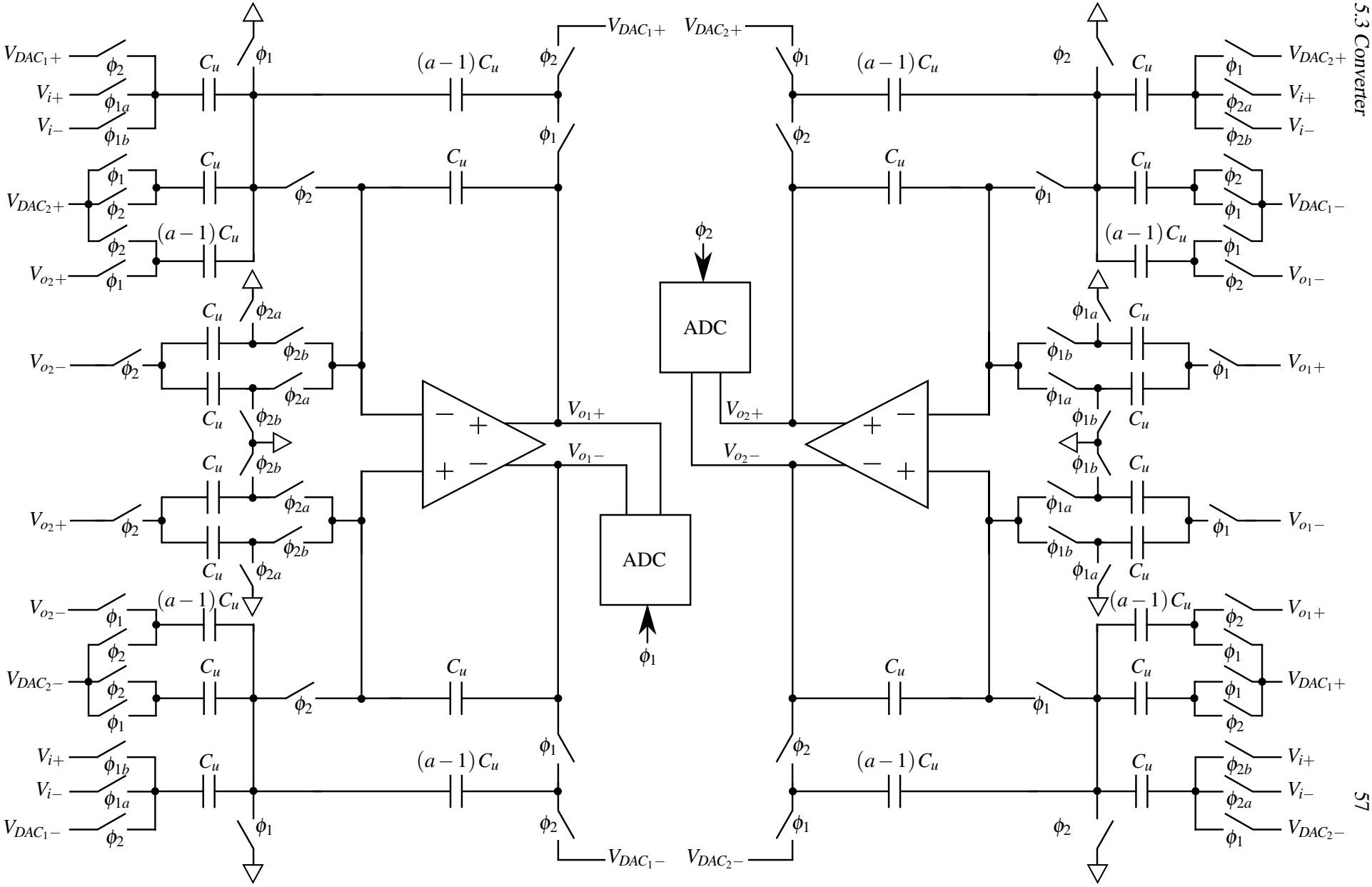

Figure 5.5: 3rd order band-pass ΣΔ converter full schematic.

5.4 Switches

The switch technologies used are: NMOS switch, CMOS transmission gate and Bootstrap switch. A CMOS gate, Fig. 5.6 consists of a PMOS and NMOS transistors in parallel. Since a single NMOS or PMOS transistor's impedance is input dependent, one suitable for high input while the other for low, one can achieve a flat characteristic by combining both, each working under conditions that are favourable to itself.

The Bootstrap switch [59][60][61][62] shown in Fig. 5.7 tries to maintain a constant on-resistance by fixing the gate-source voltage, even with varying input. This example represents the basic concept of this switch architecture. During phase ϕ_2 the bootstraping capacitor C_b is connected to VDD and GND. In ϕ_1 the capacitor is connected between the input and the transistor gate, imposing a constant V_{GS}.

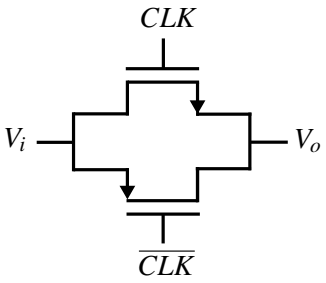

Figure 5.6: CMOS transmission gate.

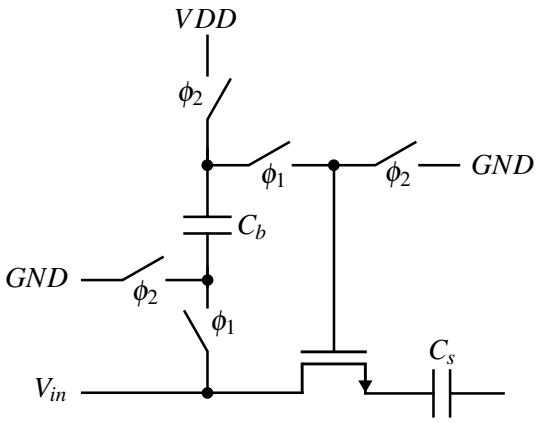

Figure 5.7: Bootstrap switch.

The implemented bootstrap switch is shown in Fig. 5.8. NMOS is used for the ground connections while PMOS is used for the VDD. The transistor M_5, connected to the top plate of C_b capacitor, must be a PMOS since this is a high voltage point. M_2 senses the input in sampling mode and therefore must be an NMOS as M_1 is. M_6 limits the voltage at M_7 so it does not rise above VDD. Since M_2 can present high resistance for high input values we also bootstrap it. Naturally, hold mode begins at rising edge of ϕ_2 while sampling is done during ϕ_1. The complete description of the workings for this circuit are detailed in [59]. Only the driving main transistor, M_1 has a significant large width, required for a high speed design. The remaining do not bear such strict requirements and have only about 1/10 the width. The bootstraping capacitor is chosen to be the same size of the sampling one.

The bootstrap switch is used for the input signal and the integrator's output. A disadvantage is the complexity of the architecture since each switch requires the use of seven transistors, including PMOS and NMOS. The CMOS gate is used for the feedback DAC and also for the bottom plate sampling of all but one specific signal. The bottom-plate sampling switch connects all capacitors to VCM demanding a high performance. NMOS switches are only used for the bottom plate sampling of delayed cross-coupled integrator output.

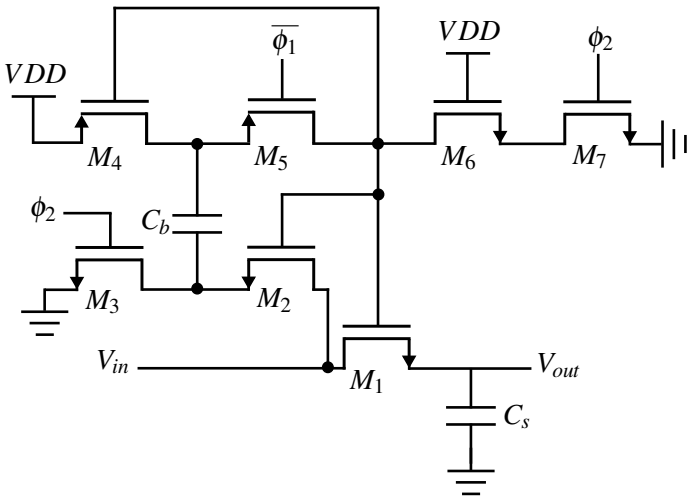

Figure 5.8: Implemented bootstrap switch schematic.

5.5 Switch Noise

Noise is a big contribution to the performance limits of ΣΔ converters. A big source is the thermal noise which is due to thermal motion of the charge carriers in the channel of the device, causing random fluctuation in the drain current [64]. Switches' transistors operate in triode region, behaving as resistors. The noise can be modelled by a voltage source in series with the device's resistance.

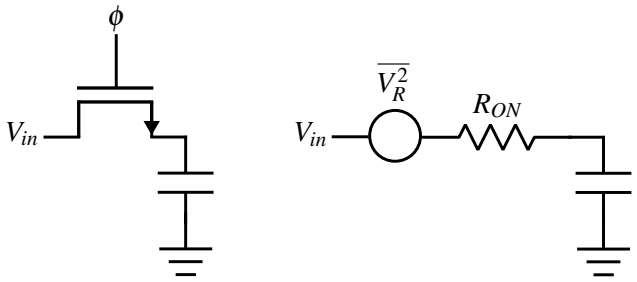

Figure 5.9: Switch thermal noise model.

It is therefore important to calculate the required sampling capacitor size needed to achieve the desired SNR. With input at −4 dB, the signal power can be calculated as:

$$\overline{v_s^2} = \frac{1}{2}\frac{(0.7\,\mathrm{V})^2}{2} = 0.1225\,\mathrm{V}^2 \tag{5.4}$$

For 60 dB SNR, we should achieve −69 dB thermal noise, so at most 1 dB is lost overall, with in-band noise at 1.54×10^{-8} V^2. The final acceptable noise value is:

$$\overline{v_n^2} = \overline{v_{n,in-band}^2} \times OSR \tag{5.5}$$

For a 100 MHz bandwidth, OSR equal to 8, the total acceptable noise value is 1.23×10^{-7} V^2. Since there are several input capacitors, one calculate the unit sampling capacitor size, taking into account the noise contribution of all but the feeedback capacitor, since this is noise shaped. From Fig. 5.4, two input capacitors are unit size while two other are $(a-1)$ times the unit size.

$$C_u = \frac{4kT}{\overline{v_n^2}} \left(2 + \frac{2}{a-1}\right) \tag{5.6}$$

The required unit capacitor size is calculated to be 750 fF. This number is indicative and further simulation should be carried out to determine the noise limit. One has to bear in mind a noise of −69 dB is considered for a full-scale 0 dB input. In the Matlab simulations, a lower input is used because of quantiser saturation levels. Therefore, in this case, one can think a −65 dB noise is the actual limit. These limits have to be studied in the circuit level. If the input swing cannot be increased, and the thermal noise is the SNR bottleneck, higher bit quantiser should be considered, in order to reduce the noise contribution in the output swing, thus enabling bigger input swings. The actual resolution of the quantiser needs not to be increased.

5.6 Operational Amplifier

Due to time limitations it was not possible to fully develop all the blocks of this converter. For this particular task, there are some high requirements on the opamp such as 60 dB gain, 16 GHz GBW and a high output swing, all difficult using the 28 nm technology. The used operational amplifier was developed by Frank, a PhD student within the AMSV laboratory, who kindly agreed to cede the project.

The actual amplifier has a 85 dB gain and 18 GHz bandwidth, while consuming about 9 mW of power. It consists of a telescopic OTA design, using an 1.8 V power supply, achieving an 1.4 V output swing. More details are not disclosed as it was the author's wish. Since this converter's design is of switch-capacitor type, the common-mode feedback circuit had to be redesigned, as per a switched capacitor type, as in Fig. 5.10.

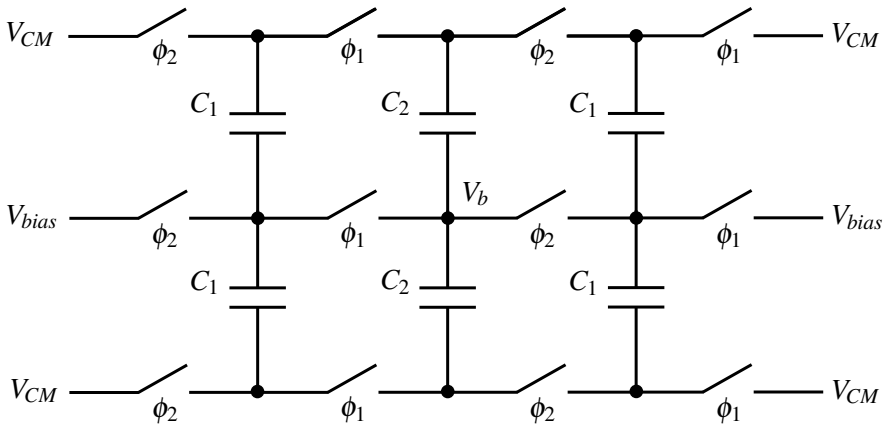

Figure 5.10: Common-mode Feedback Circuit [63].

Although high performance, this opamp is not the most suitable for this converter as it has output load limitations and also imposes noise bottlenecks. The design was slightly modified to tailor this converter's requirements, but this is still insufficient for an optimal implementation. The original gain was lowered a bit by shrinking transistor size which decreased the parasitic capacitance. These are in the same order of the sampling capacitors, which naturally entangles high performance. To compensate this, the biasing current was also increased, with the side effect of higher power consumption. The total power usage of one opamp is now roughly 14 mW. Since this design requires high slew, one could also use the slew-rate booster technique to improve power consumption without sacrificing any high slew capabilities [65][66].

5.7 Quantiser

5.7.1 Comparator

The comparator is the building block of the quantiser. It is responsible to compare the input voltage with the given reference and produce a digital output bit. The implemented comparator, Fig. 5.11 is composed by a switched cap circuit that calculates the output logic level, a dynamic latch comparator [76][77][78][79][81], a buffer and a final D-type latch [80].

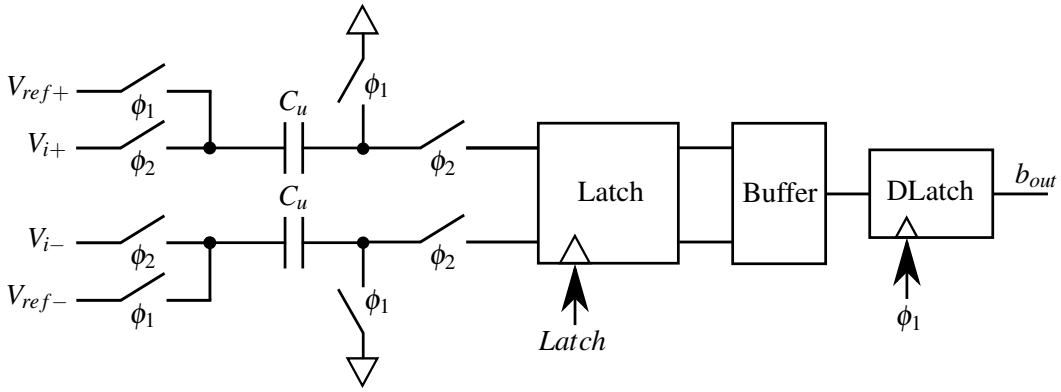

Figure 5.11: Comparator.

During ϕ_1 the capacitor is charged to the reference voltage. In ϕ_2 the capacitor is connected to the input of the dynamic latch and the signal input voltage thus feeding the difference between these two. The Latch signal triggers the comparison just before ϕ_1, so the result is available at that time. At the output, a VDD or GND signal will be produced according to the previous voltage difference, during ϕ_1, and VDD during reset at ϕ_2. Afterwards, the differential signal is fed to a buffer that balances the load of the previous latch and serves as a differential to single output block. At the very end there is a D-type latch that holds the logic value for a full clock cycle.

The dynamic latch in Fig.5.12 was proposed by [81]. It featured reset and a tracking phases. When the clock signal is low, the output is reset to VDD. During the track phase, comparison is made and the differential output will go to VDD or GND according to the differential input.

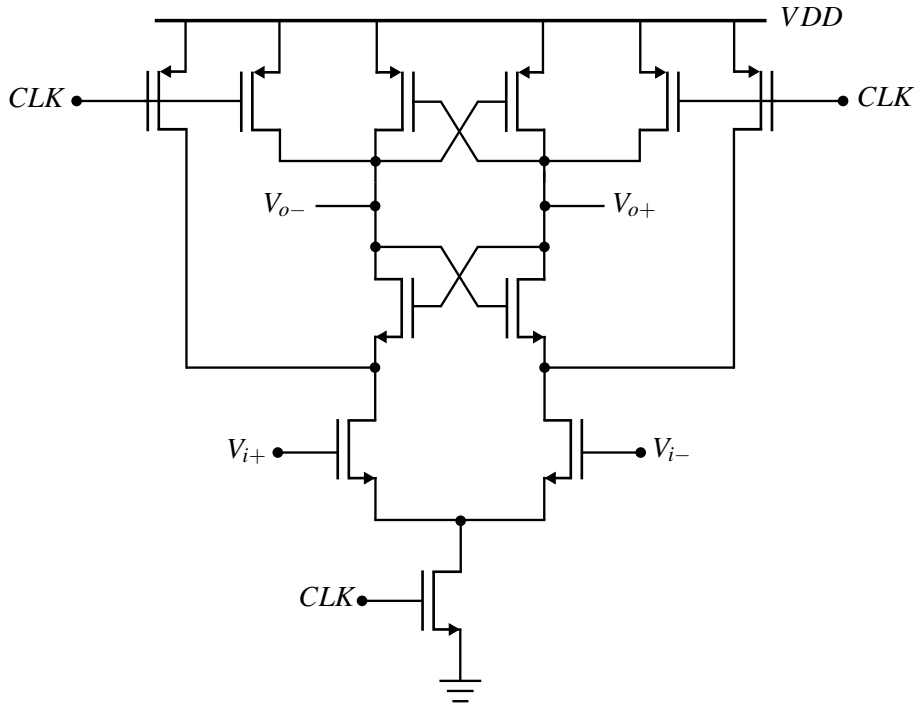

Figure 5.12: Comparator latch schematic.

The output buffer, 5.13 is composed by two inverters, with one providing output and the other connected to an inverter that drives both inverters, thus enabling a more precise result. This buffer allows for an even output load on the comparator.

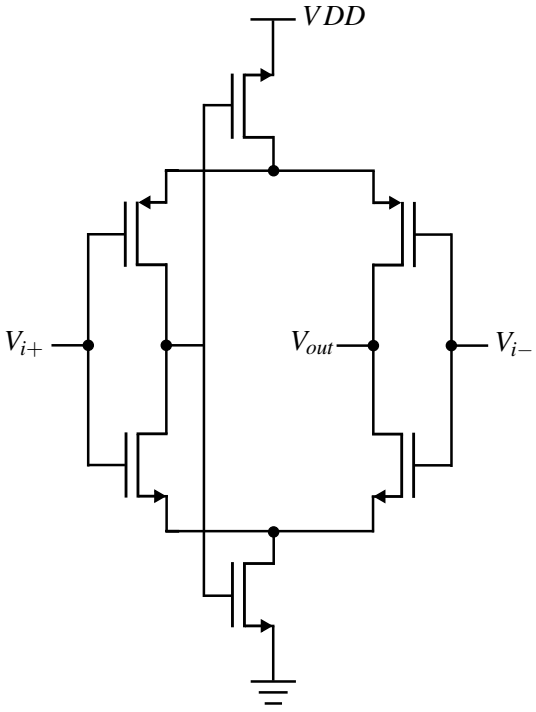

Figure 5.13: Buffer schematic.

The D Latch, 5.14, creates a perfect binary value by keeping the logic value until the next clock cycle appears. It is composed of two inverters connected with a positive feedback loop. By using a switch, the output can be isolated from the input.

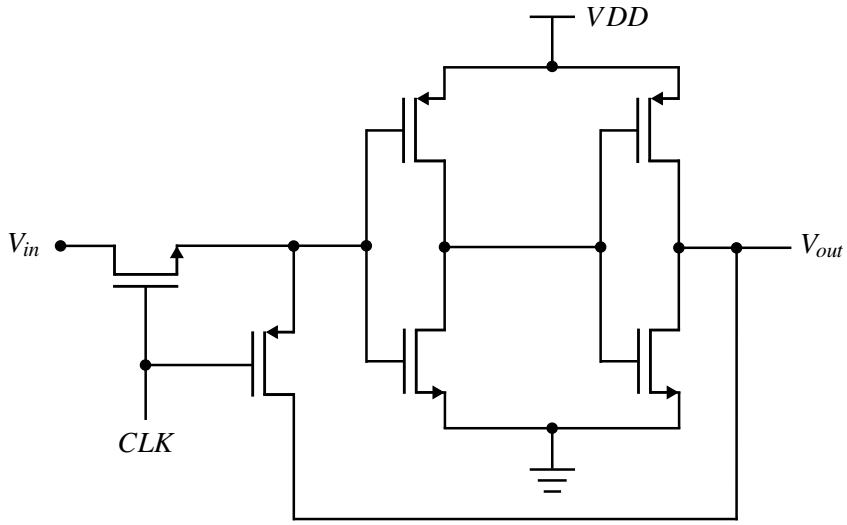

Figure 5.14: Dlatch schematic.

Extensive simulation was carried out. The most critical aspect of the comparator is the voltage offset. Through Matlab simulation it was determined that a random offset across all comparators, following a normal distribution, with a standard deviation of 30 mV would not hurt the SNR performance. The work reported in [82] describes a method on how to measure this parameter using simulation on the circuit level. The results showed a standard deviation offset of around 19 mV. Thus, the requirements set by Matlab simulation are met on the circuit level.

5.7.2 Flash ADC

In this design, a 16 level flash quantiser is used, using an array of 15 switched capacitor fully differential comparators, as shown in Fig. 5.15. The threshold voltages are derived from the resistor ladder. In fact, Fig. 5.15 shows two resistor ladders, since two different comparison voltages are needed for the differential input. This was only done for a better schematic representation. In reality, only one ladder is needed, with the appropriate routing. The size of the resistors are all equal and must be dimensioned according to the power/speed trade-off.

The output of the comparator array can be used to drive the feedback DAC. Despite this, a true binary signal is still needed at the output, for post-processing. This demands a thermometer-to-binary encoder, which was described using Verilog-A HDL [83].

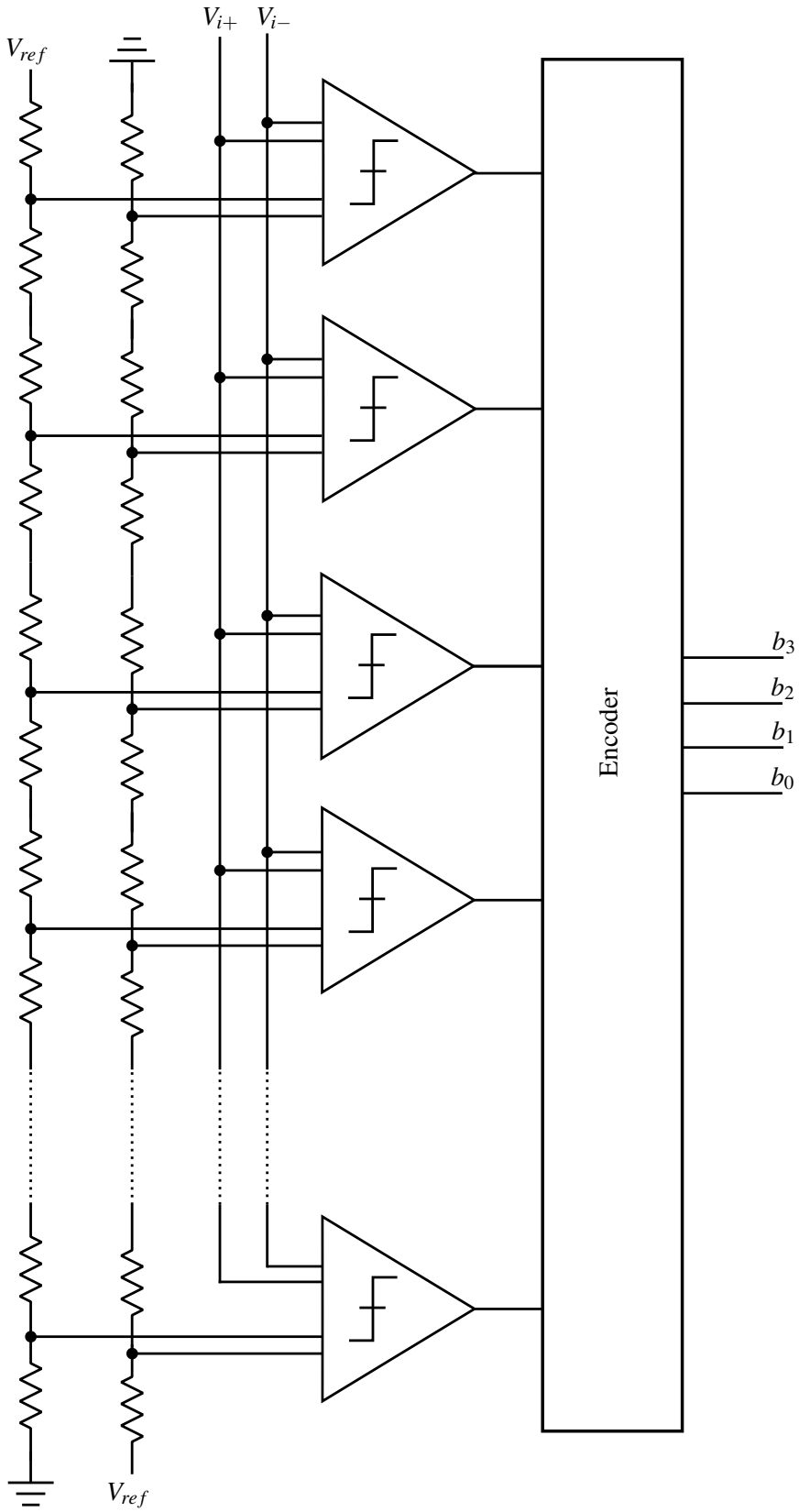

Figure 5.15: Flash ADC schematic.

5.8 Feedback DAC

The feedback DAC is composed of 16 capacitors, $1/16^{th}$ the size of the feedback capacitor. Either one is connected to the positive or negative reference in order to feed the desired voltage levels. The 16^{th} capacitor is connected only to VCM, thus charged to neutral. Though the DAC needs only 15 capacitors, 16 are used because of other signals, sharing them, need the full C_u capacitance.

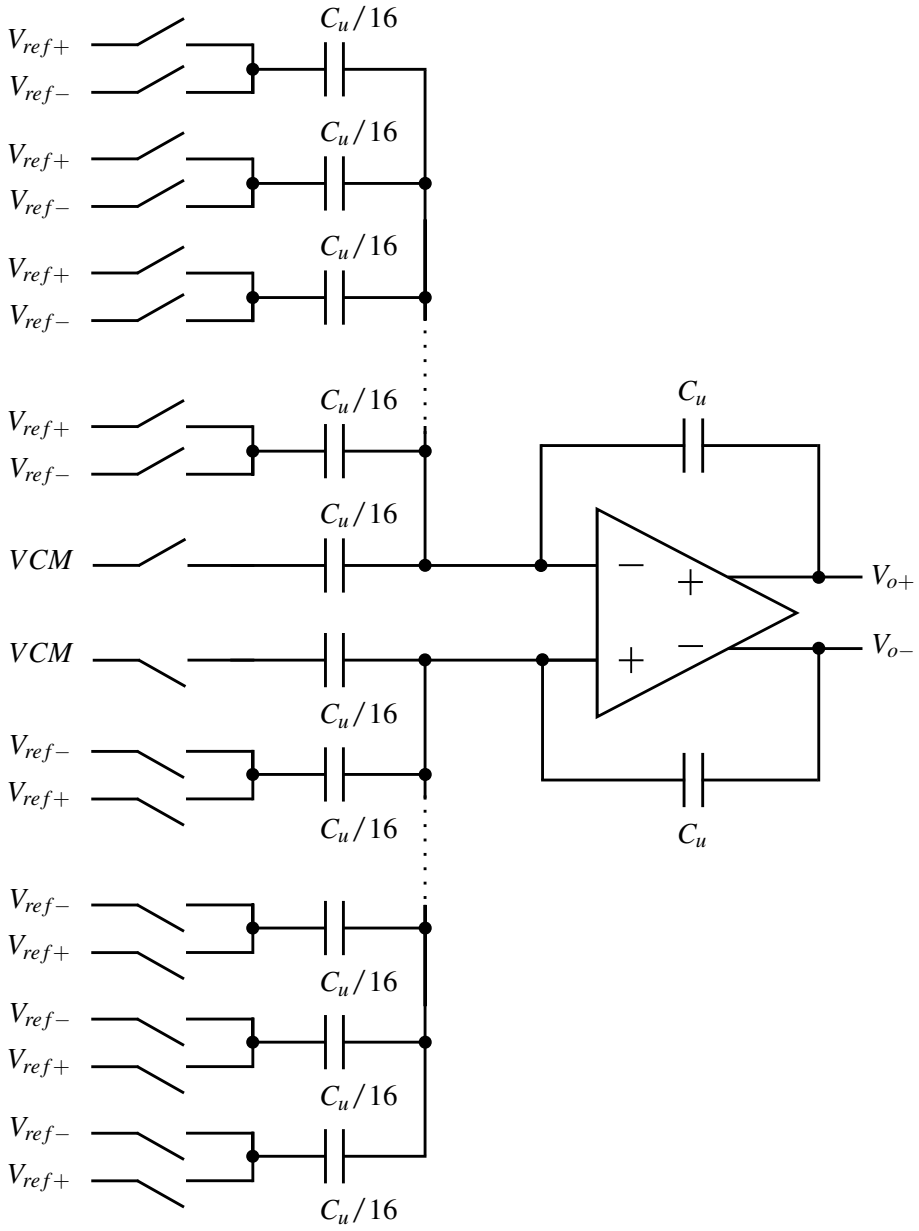

Figure 5.16: Feedback DAC.

5.9 Simulation Results

Transistor level simulations are done using Cadence IC design software. The circuit is implemented using 28 nm technology. In order to plot the output spectrum of the converter, 1024 samples, each one clock cycle apart, are captured out of 1250 generated. The signal is digitally reconstructed in Matlab, as chopping must be made.

5.9.1 Transient Noise

Cadence allows for the injection of transient noise in the circuit [75], thus simulating the thermal noise effect of the switches. From simulation it was concluded that a 100 fF was the maximum value without imposing a bottleneck, due to high load. This value does limit the overall SNDR performance to about 56 dB, due to thermal noise. Thus, one should bear this limit in mind or design a new opamp and increase the sampling capacitor size for a future tape-out.

5.9.2 Power Consumption

Power consumption is an important aspect for portable device applications. The individual blocks were tested and the used power was measured. Results are shown in Table 5.1. The opamp has the highest power usage and this design requires two. The remaining components represent only a small fraction of the total power, with the Flash ADC being the second most power-hungry component, though still under the milliwatt range. The total power is 30 mW.

Table 5.1: Power consumption by block.

Component	Power
Opamp	14 mW
Flash ADC	0.6 mW
Comparator	2 µW
Arm-Latch	1 µW
Buffer	0.2 µW
D-Latch	0.2 µW
Bootstrap switch	24 µW
CMOS Switch	1 µW

5.9.3 Performance Results

The power output spectrum of the transistor level simulation is shown in Figures 5.17 and 5.18. One can observe the tone at 400 MHz, or $f_s/4$, due to the opamp offset. This has no effect in the overall SNDR which is of 61 dB. The measured bandwidth is centred at 736 MHz or $0.46 f_s$ and ranges 100 MHz for an OSR of 8. For the bandwidths of 40 MHz and 20 MHz SNDRs of 67.5 dB and 72.7 dB were, respectively, achieved.

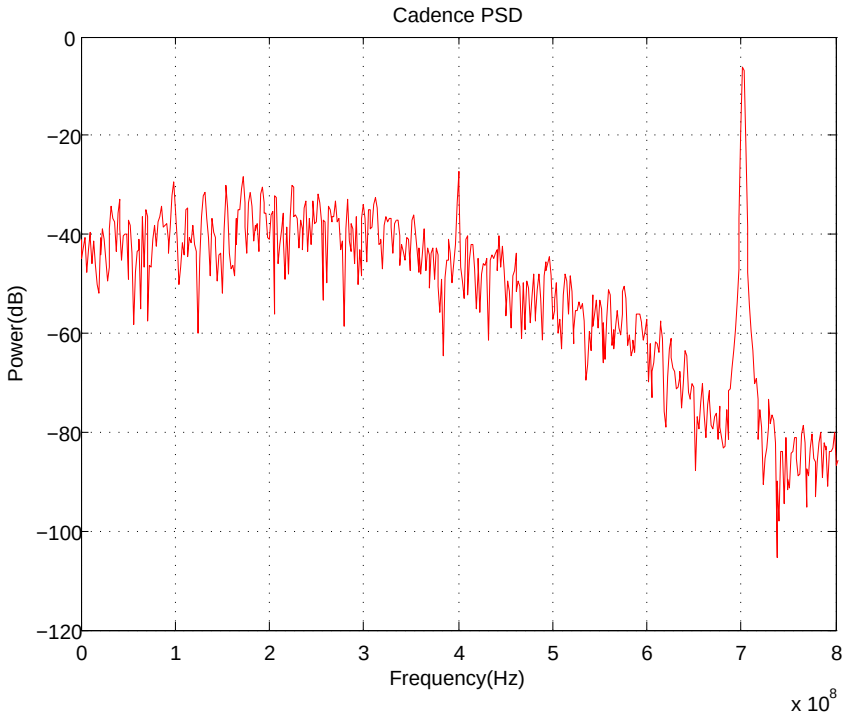

Figure 5.17: Cadence simulation output PSD.

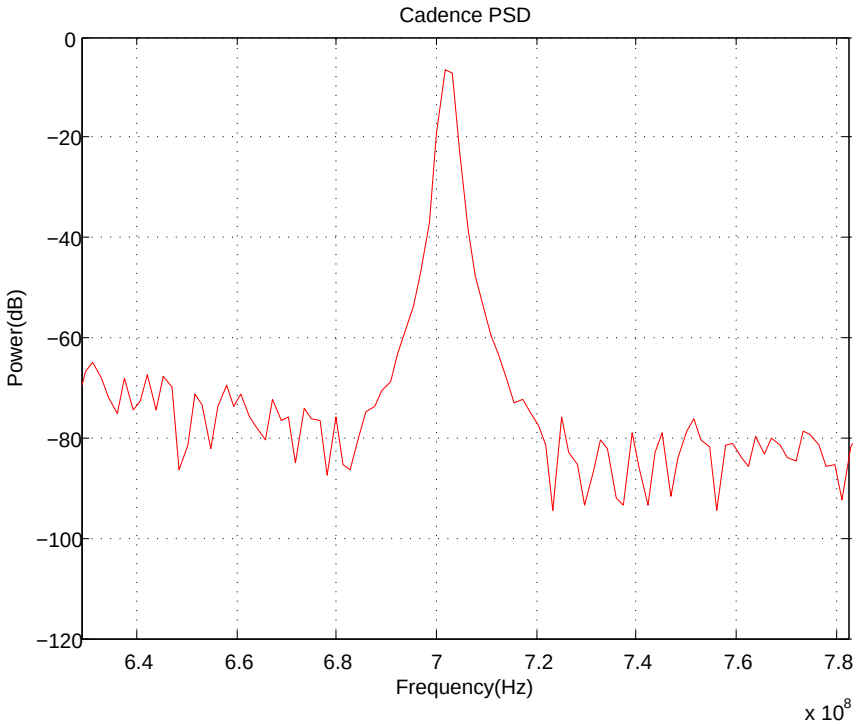

Figure 5.18: In-band zoom of the output PSD.

The small tone observed at 400 MHz is due to the slight asymmetry introduced between both paths. This proves that the circuit is tolerant to path mismatch, as the result tone is outside of the signal spectrum.

As discussed before, the overall limitation of the converter is thermal noise which limits the maximum performance to 56 dB. A high sampling capacitor is required but opamp limitations makes this impossible. One possible solution is to increase the number of bits used in quantisation so that the error is made smaller and the input signal can be increased without saturating the quantiser. The quantiser needs not complicated matching techniques as the design is still tolerant to offsets and they are noise-shaped, as they are inside the loop. For the achieved SNDR of 61 dB or 9.85 bits ENOB, a FOM of 0.043 pJ/conv is achieved. The overall results are summarised in table 5.2 against state-of-the-art works.

Table 5.2: Summary of the measured results from this design and references.

	[37]	[68]	[34]	**This Work**	
RF	0.55	2.2	2.4	**0.736**	GHz
Sampling Rate	4	8.88	3	**1.6**	GHz
Signal Bandwidth	100	80	60	**100**	MHz
Oversampling Ratio	20	55.5	40	**8**	
SNDR	69	42	40	**56**	dB
ENOB	11.17	6.68	6.35	**9**	bits
Power Consumption	550	164	40	**30**	mW
FOM	0.654	10	4.1	**0.077**	pJ/conv
Power Supply	1/±2.5	1.5	1	**1.8**	V
Technology	65	40	90	**28**	nm
Architecture	CT	CT	CT	**DT**	
Order	6^{th}	4^{th}	6^{th}	**2^{nd}**	

Chapter 6

Conclusion

6.1 Summary

Current wireless communication standards are suffering a fast and increasing growth. Mobile communication standards like LTE are already using signal bands of 20, 40 all the way up to 100 MHz, with experiments pushing wider. 5G standards have already been in development for some time and the wider-band trend is ongoing. The presence of multiple standards, demanding a variety of signal specifications, pressures the IC industry for wideband tunable designs. At the same time, miniaturisation is ever trending while power efficiency, size and cost goals are increasingly more demanding. Current mobile phone devices work with a wide variety of wireless protocols, including 3 generations (4 in the near future) of mobile communication standards, Wi-Fi, Bluetooth, GPS and NFC, and in due time GALILEO and GLONASS navigation systems. Flexible and versatile receivers are in demand.

Band-pass $\Sigma\Delta$ converters are an attractive ADC architecture for RF receivers as they shape the noise away from the RF. They also allow more efficient design by shifting some of the effort from the analogue to the digital domain, which CMOS technologies are increasingly more suitable for. Unfortunately, band-pass $\Sigma\Delta$ converters have not been an active topic of research in present years and available designs do not suit the industry's demands.

A 3^{rd} order band-pass $\Sigma\Delta$ Time-Interleaved A/D converter using cross-coupled quantisation noise terms was presented. The proposed architecture uses 1^{st} order modulators since the shaping order is doubled by the cross-coupling between the two paths. The third-order term is also introduced by adding another cross-coupling term, which imposes a fixed zero at Nyquist rate. The extra zero allows for a more wideband noise shaping with low OSR applications.

Compared to the standard 2-path TI $\Sigma\Delta$ converter proposed in [3], this dissertation's proposal is able to increase the achieved SNDR for lower OSR. The extra zero is introduced at very little hardware cost, as only one extra noise-coupling connection is needed. This work's converter has also achieved considerably higher speed, thus being suited for state-of-the-art applications such as LTE.

The new band-pass ΣΔ converter was implemented using a 28 nm CMOS technology. A 1.8 V power supply is used. The effective sampling rate is 1.6 GHz, as each path operates at half of it. For a 100 MHz bandwidth, not including thermal noise, 61 dB SNDR was measured (56 with thermal noise), while 72.7 dB and 67.5 dB were achieved for 20 MHz and 40 MHz signal bands.

6.2 Applications

The converter developed in the scope of this dissertation focuses in providing the industry with a wideband, low-power and simple architecture converter design, suitable for a wide variety of wireless communication standards, used by mobile devices. This proposal is of discrete-time type which allows high tunability.

Considering the LTE communication standard, there are established protocols operating in the 700 MHz region. Table 6.1 shows some operating bands currently in use [70].

Table 6.1: LTE operating bands.

E-UTRA Band	**Uplink Band** (MHz)	**Downlink Band** (MHz)
3	1710 - 1755	2210 - 2155
5	824 - 849	869 - 894
6	830 - 840	875 - 885
8	880 - 915	925 - 960
12	699 - 716	729 - 746
13	777 - 787	746 - 756
14	788 - 798	758 - 768
17	704 - 716	734 - 746
18	815 - 830	860 - 875
19	830 - 845	875 - 890
20	832 - 862	791 - 821
40	2300 - 2400	2300 - 2400
41	2496 - 2690	2496 - 2690

LTE is still an important topic of research despite the ongoing development of 5G technologies [71]. LTE deployed standards commonly used transmission bandwidths of 10 and 20 MHz. LTE-Advanced is still in development and the latest Release 10 is capable of aggregating 5 different channels for a total of 100 MHz, achieving data-rates of up to 3 Gbps on the downlink [72][73]. None of the 700 to 800 MHz bands shown are capable of 100 MHz bandwidths. At best an aggregation of bands 18, 19 and 20 would result in a total bandwidth of 47 MHz. LTE-Advanced is still not actively deployed and currently the only bands capable of full 100 MHz duplex signal band are in the 2 to 3 GHz range. Undersampling [33] could be used to bring the signal down to the desired range.

Other possible applications may include land, maritime and aeronautical military systems or wireless audio. With further improvement, new technologies such as Galileo and GLONASS navigation systems can also be targeted [74].

6.3 Future Work

The proposed converter has promising performance results. Thus, further research is worthwhile in order to improve its specifications and develop a final industry usable product. First of all, a new op-amp should be designed to better suit the purposes of the present design. Nevertheless, the op-amp kindly provided by the student at the AMSV lab allowed to understand well the limitations of design. A layout design and tape-out is the natural step towards the silicon proof of the concept proposed in this document.

One possible future course of research would be to implement a MASH structure, aggregating two 3^{rd} order converters, resulting in a 6^{th} order NTF. From theoretical calculation a 35 dB improvement is seen, thus it is fair to conclude one could expect roughly 90 dB over the 100 MHz bandwidth, instead of 60 dB. There are no converters achieving such results. Current state-of-the-art modulators, achieving wide bands use complex high order structures. This proposal would imply a 6^{th} order NTF but with 4^{th} order effort. Fig. 6.1 shows the theoretical noise transfer functions for both 3^{rd} and 6^{th} order modulation, along with Ying's[3] work, for the 3 different orders. Fig. 6.2 shows expected SNR values for the several architectures, on an ideal level. A clear advantage for the proposed MASH structure can be observed, surpassing the performance of the standard cross-coupled design with the 3 stage MASH structure.

Despite the limited study carried out in this dissertation work, the promising results ensue more effort in the development of this concept. A solid ground work was established and a final simple yet high-performance $\Sigma\Delta$ converter was proven to be feasible.

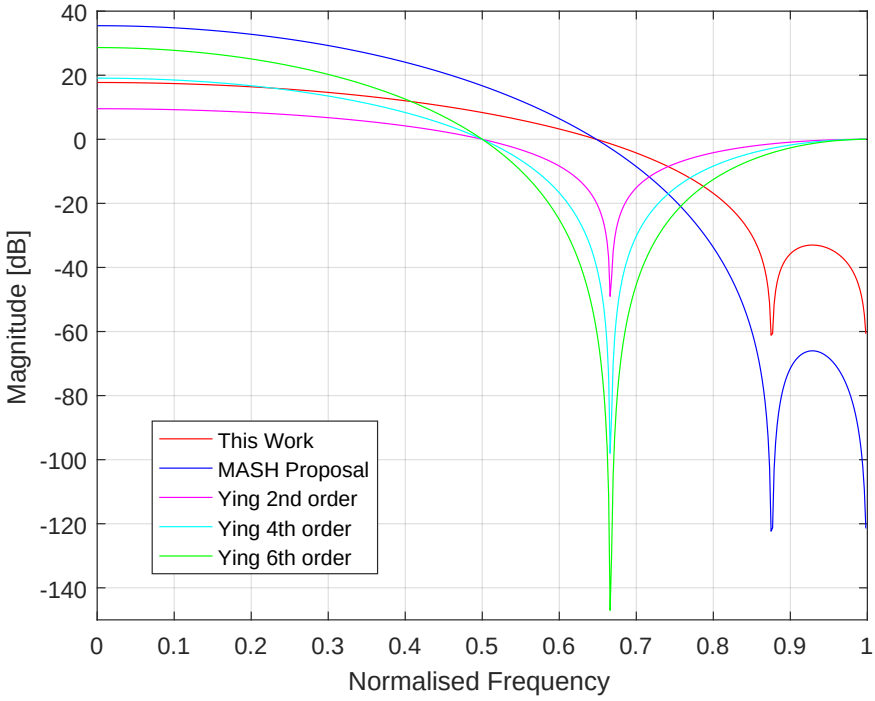

Figure 6.1: NTF comparison for different converter schemes.

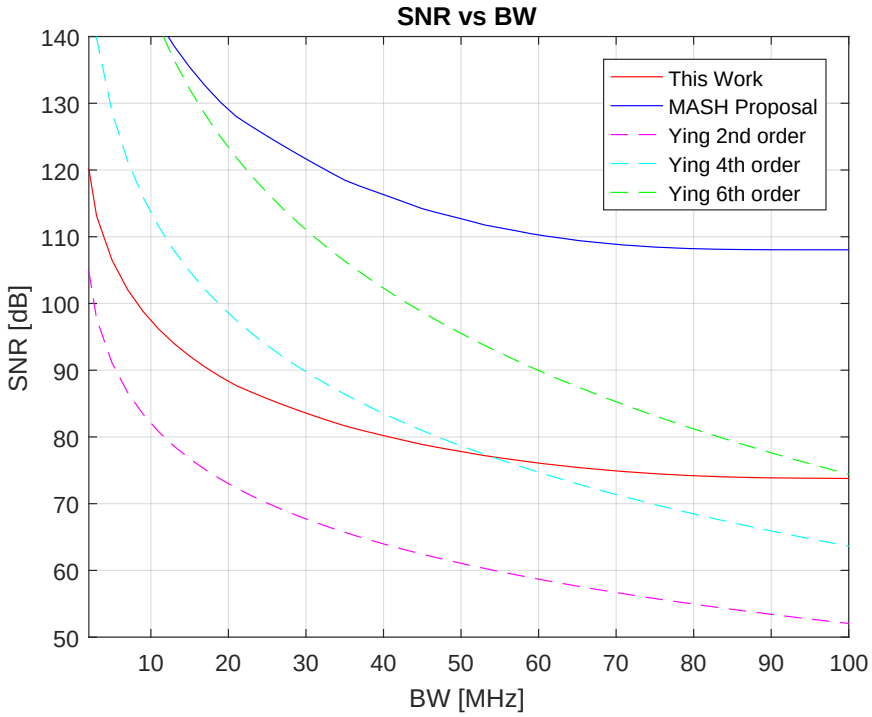

Figure 6.2: SNR curve comparison for different converter schemes.

Appendix A

Matlab Model

A.1 Simulink Model

The Simulink converter model was already presented and discussed in 4.5. The several non-idealities were implemented using [52]. KTC noise, jitter and real opamp model are discussed. Some adaptations were needed to fit the proposed architecture. This section briefly describes them so the reader better, but summarily understands them. For deeper understanding [52] should be consulted.

A.1.1 Non-Idealities

The error introduced when a sinusoidal signal is sampled at an instant which is in error by an amount δ is given by:

$$x(t+\delta) - x(t) \approx 2\pi f_{in}\delta A\cos(2\pi f_{in}t) = \delta\frac{d}{dt}x(t) \tag{A.1}$$

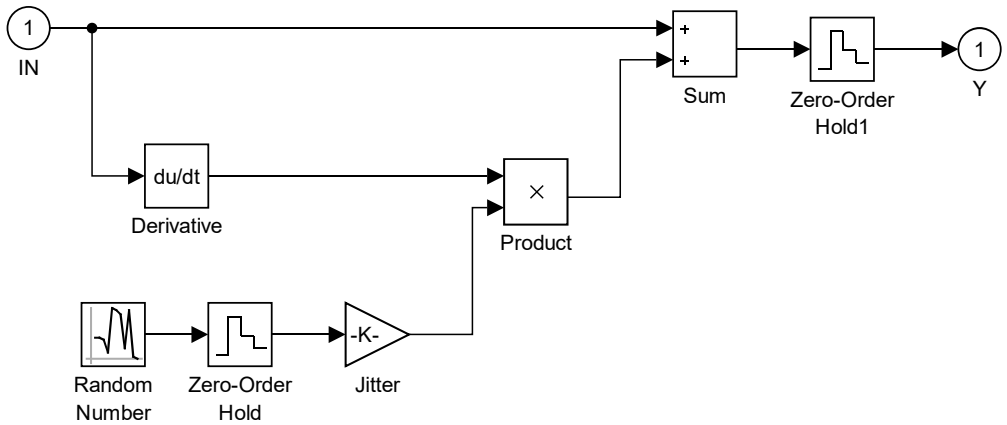

Figure A.1: Jitter modelling.

The input signal and its derivative, both continuous-time signals, are sampled by a zero-order hold. The model implements expression A.1 by assuming the sampling uncertainty to be a Gaussian random process.

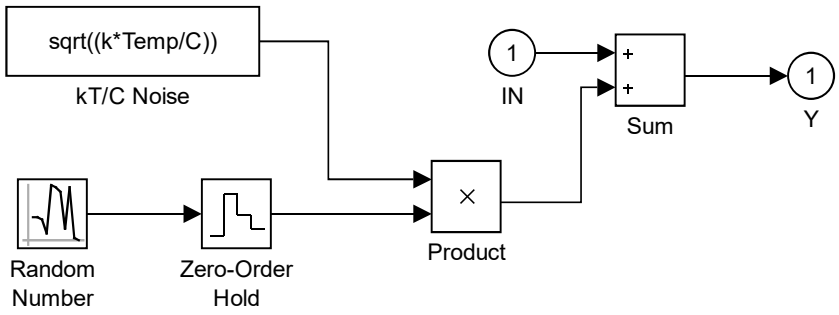

Figure A.2: KTC noise modelling.

The noise generated by the switches and also intrinsic to the opamp can be simulated by means of a modified noisy integrator with transfer function:

$$H(z) = b\frac{z^{-1}}{1-z^{-1}} \tag{A.2}$$

The factor b represents the ratio C_s/C_f, between the sampling and feedback capacitors. The kT/C Noise block multiplies the input by b. The total noise power sampled to C_s with a switch, with finite impedance R_{on}, is given by:

$$e_T^2 = \int_0^\infty \frac{4kTR_{on}}{1+(2\pi f R_{on}C_s)^2}\,df = \frac{kT}{C_s} \tag{A.3}$$

The noise voltage e_T is now added to the input voltage $x(t)$:

$$\begin{aligned} y(t) &= [x(t)+e_T(t)]\,b \\ &= \left[x(t)+\sqrt{\frac{kT}{C_s}}n(t)\right]b \end{aligned} \tag{A.4}$$

where $n(t)$ denotes a Gaussian random process with unit standard deviation, while $b = C_s/C_f$ is the integrator's coefficient.

A.1.2 The Integrator

The integrator's Simulink model is depicted in Fig. A.3. This model makes use of a single unit delay feedback, with loop gain equal to the product of the parameter a by the finite DC gain coefficient α, to implement the desired integrator function. Besides the finite gain of the opamp, other included non-idealities are the output saturation levels and an input block that simulates the GBW and slew-rate imposed by the opamp. This function was modified to include the non-standard "unstable" integrator used in this dissertation's proposed converter.

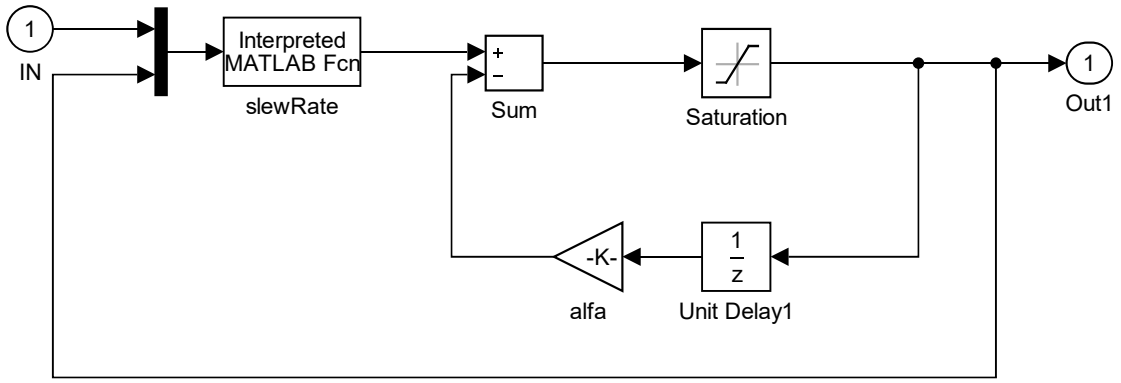

Figure A.3: Matlab model of the integrator.

For any integrator, a limited opamp loop gain will result in only a fraction α of the previous output being added to the next one. The transfer function taking into account this leakage is given by:

$$H(z) = \frac{z^{-1}}{1-\alpha z^{-1}} \tag{A.5}$$

The DC gain is then $1/(1-\alpha)$. The implemented SC integrator was already shown in Fig. 5.2. A standard integrator does not include the extra capacitor which samples the previous output. [52] took into account the standard integrator and wrote the output voltage expression as:

$$v_o(t) = v_o(nT_s - T_s) + \alpha V_{in}(nT_s - T_s/2)\left(1 - e^{-t/\tau}\right), 0 < t < \frac{T_s}{2} \tag{A.6}$$

This formula does not take into account the extra capacitor charge. The extra term must added thus the resulting expression is:

$$v_o(t) = v_o(nT_s - T_s) + \alpha\left[v_{in}(nT_s - T_s/2) + a\, v_o(nT_s - T_s/2)\right]\left(1 - e^{-t/\tau}\right) \tag{A.7}$$

The Matlab function implemented by the *slewRate* block in Fig. A.3 is called *slew* and takes into account expression A.7. This models the output of the ideal integrator with finite DC gain, slew-rate and bandwidth.

Listing A.1: Integrator slew function.

```
function out = slew(in,alfa,sr,GBW,Ts,notch,out1)
% Models the operational amplifier finite bandwidth and slew rate
% for a discrete time integrator (by S. Brigati, P. Malcovati)
% (adapted by luis.brochado@fe.up.pt)
%
%
% in:           Input signal amplitude
% alfa:         Effect of finite gain (ideal amplifier alfa=1)
% sr:           Slew rate in V/s
% GBW:          Gain-bandwidth product of the integrator loop gain in Hz
% Ts:           Sample time in s
% out:          Output signal amplitude

tau=1/(2*pi*GBW);  % Time constant of the integrator
Tmax = Ts/2;

slope=alfa*abs(in)/tau + alfa*abs(out1)*(notch-1)/tau;

if slope > sr                    % Op-amp in slewing
        tsl = ((abs(out1)*(notch-1)+abs(in))*alfa)/sr - tau;  % Slewing time
        if tsl >= Tmax
                error_in = abs(in) - sr*Tmax;
        error_out1 = abs(out1) - sr*Tmax;
        else
                texp = Tmax - tsl;
                error_in = ((abs(in))*(1-alfa)) + (abs(in)*alfa - sr*tsl) *
                    exp(-texp/tau);
        error_out1 = ((abs(out1)*(notch-1))*(1-alfa)) + (((abs(out1)*(notch
            -1))*alfa) - sr*tsl) * exp(-texp/tau);
    end
else                                    % Op-amp in linear region
        texp = Tmax;
        error_in = ((abs(in))*(1-alfa)) + alfa*(abs(in)) * exp(-texp/tau);
    error_out1 = ((abs(out1)*(notch-1))*(1-alfa)) + alfa*(abs(out1)*(notch
        -1)) * exp(-texp/tau);
end

out = in - sign(in)*error_in + sign(out1)*error_out1;
```

A.2 Matlab Setup Code

The following code snippets are important blocks used in this dissertation work, responsible for the SNR calculations of all simulations. Other simpler scripts or functions are not transcribed. These include a launcher for the Simulink model, enabling quick setup, and some other scripts which were used for the plotting of some figures in previous chapters.

Listing A.2: Calculation of the achieved SNR.

```
function [snrdB,ptotdB] = calcSNR(vout,f,f0,fB,w,N,Vref)
% SNR calculation in the time domain (P. Malcovati, S. Brigati)
% vout: Sigma-Delta bit-stream taken at the modulator output
% f:    Normalized signal frequency (fs -> 1)
% fB:   Base-band frequency bins
% w:    windowing vector
% N:    samples number
% snrdB:         SNR in dB
% ptotdB:        Bit-stream power spectral density (vector)
fB=ceil(fB);
signal=(N/sum(w))*sinusx(vout(1:N).*w,f0,N); % Extracts sinusoidal signal
noise=vout(1:N)-signal;                      % Extracts noise components
stot=((abs(fft((vout(1:N).*w)'))).^2);       % Bit-stream PSD
ssignal=(abs(fft((signal(1:N).*w)'))).^2;    % Signal PSD
snoise=(abs(fft((noise(1:N).*w)'))).^2;      % Noise PSD
pwsignal=sum(ssignal(f-fB/2:f+fB/2));        % Signal power
pwnoise=sum(snoise(f-fB/2:f+fB/2));          % Noise power
snr=pwsignal/pwnoise;
snrdB=dbp(snr);
norm=sum(stot)/Vref^2;                       % PSD normalization
if nargout > 1
        ptot=stot/norm;
        ptotdB=dbp(ptot);
end
if nargout > 2
        psig=ssignal/norm;
        psigdB=dbp(psig);
end
if nargout > 3
        pnoise=snoise/norm;
        pnoisedB=dbp(pnoise);
end
```

Listing A.3: Function *sinusx*.

```
function outx = sinusx(in,f,n)
% Extracts of a sinusoidal signal (S. Brigati, P. Malcovati)
%
% in:   Input data vector
% f:    Normalized input signal frequency
% n:    Number of simulation points
%
% outx: Sinusoidal signal
%

sinx=sin(2*pi*f*[1:n]);
cosx=cos(2*pi*f*[1:n]);
in=in(1:n);
a1=2*sinx.*in;
a=sum(a1)/n;
b1=2*cosx.*in;
b=sum(b1)/n;
outx=a.*sinx + b.*cosx;
```

Listing A.4: Function *dbp*.

```
function y = dbp(x)
% Calculates the input value in dB dbp(x) = 10*log10(x)
% (by S. Brigati, P. Malcovati)
%
% x: Input
%
% y: Output in dB
%

y = -Inf*ones(size(x));
nonzero = x~=0;
y(nonzero) = 10*log10(abs(x(nonzero)));
```

Listing A.5: Calculation of the theoretical SNR for the 3rd order ΣΔ converter.

```
 function [SNR] = theory_SNR(OSR,f0,fs,N,a)
% 3rd order modulator theoretical SNR (luis.brochado@fe.up.pt)
%
% OSR: Oversampling ratio
% f0:  Central frequency
% fs:  Sampling frequency
% N:   Quantiser bit number
% a:   Notch parameter

fB = fs / (2 * OSR);
ps = 10*log10 ((2^(2*N))/8);       % Calculate Signal Power

X = (f0*fs-fB/2):0.1:(f0*fs+fB/2); % Integration range vector
Y = (a*(exp(1j*2*pi*X/fs).^(-1))+a*(exp(1j*2*pi*X/fs).^(-2))+(exp(1j*2*pi*X/
    fs).^(-3))+1);                 % NTF expression

pe = 10*log10(trapz(X,(abs(Y).^2)) / (12 * fs)); % Noise calculation
SNR = ps - pe;
```

References

[1] José M. de la Rosa, Belén Pérez-Verdú, and Angel Rodríguez-Vázquez. *Systematic design of CMOS switched-current bandpass sigma-delta modulators for digital communication chips*. Kluwer Academic, Boston, 2002. OCLC: 54435900. URL: http://site.ebrary.com/id/10067373.

[2] F. Maloberti. *Data converters*. Springer, Dordrecht, Netherlands, 2007. OCLC: ocn123432673.

[3] Feng Ying and Franco Maloberti. A mirror image free two-path bandpass ΣΔ modulator with 72 dB SNR and 86 dB SFDR. In *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pages 84–514. IEEE, 2004. URL: http://ieeexplore.ieee.org/abstract/document/1332605/.

[4] Feng Ying. *A Cross-Coupled Two-Path Bandpass Sigma-Delta Modulator*. PhD thesis, University of Texas, Dallas, May 2004.

[5] Tony Chan Carusone, David Johns, Kenneth W. Martin, and David Johns. *Analog integrated circuit design*. John Wiley & Sons, Hoboken, NJ, 2nd ed edition, 2012.

[6] Behzad Razavi. *Design of analog CMOS integrated circuits*. McGraw-Hill Education, New York, NY, second edition edition, 2017.

[7] Timmy Sundström, Linköpings universitet, and Institutionen för systemteknik. *Design of high-speed analog-to-digital converters using low-accuracy components*. PhD thesis, Department of Electrical Engineering, Linköping University, Linköping, 2011. OCLC: 938846944.

[8] IEEE Instrumentation and Measurement Society, Waveform Measurement and Analysis Technical Committee, Institute of Electrical and Electronics Engineers, IEEE Standards Board, and IEEE Standards Association. *IEEE standard for terminology and test methods for analog-to-digital converters*. Institute of Electrical and Electronics Engineers, New York, 2001. OCLC: 50141272.

[9] F. Goodenough. Analog Technologies of all Varieties Dominate ISSCC. *Electronic Design*, 44:96–111, February 1996.

[10] Fernando Medeiro, Angel Pérez-Verdú, and Angel Rodríguez-Vázquez. *Top-Down Design of High-Performance Sigma-Delta Modulators*. Springer US, Boston, MA, 1999. URL: http://link.springer.com/10.1007/978-1-4757-3003-6.

[11] Ivano Galdi, Edoardo Bonizzoni, Piero Malcovati, Gabriele Manganaro, and Franco Maloberti. 40 MHz IF 1 MHz Bandwidth Two-Path Bandpass Sigma-Delta; Modulator With

72 dB DR Consuming 16 mW. *IEEE Journal of Solid-State Circuits*, 43(7):1648–1656, July 2008. URL: http://ieeexplore.ieee.org/document/4550636/, doi:10.1109/JSSC.2008.923728.

[12] C. Sadner, M. Clara, A. Snatner, T. Hartig, and F. Kuttner. A 6-bit 1.2 GS/s low-power flash-ADC in 0.13um digital CMOS. *IEEE J. Solid-State Circuits*, 40(7):1499–1505, July 2005.

[13] Richard Schreier and Gabor C. Temes. *Understanding delta-sigma data converters*. IEEE Press ; Wiley, Piscataway, NJ : Hoboken, N.J. ; Chichester, 2005. OCLC: ocm53156181.

[14] Tony Chan Carusone, David Johns, Kenneth W. Martin, and David Johns. *Analog integrated circuit design*. John Wiley & Sons, Hoboken, NJ, 2nd ed edition, 2012.

[15] Sangil Park. Digital Signal Processors. 1993. URL: http://pr.radom.net/~pgolabek/APR8-sigma-delta.pdf.

[16] Alonso Morgado, Rocío del Río, and José M. de la Rosa. ΣΔ ADCs: Basic Concepts, Topologies and State of the Art. In *Nanometer CMOS Sigma-Delta Modulators for Software Defined Radio*, pages 23–57. Springer New York, New York, NY, 2011. URL: http://link.springer.com/10.1007/978-1-4614-0037-0_2.

[17] David Jarman. No. Brief Introduction to Sigma Delta Conversion. 1995. URL: http://uglyduck.ath.cx/PDF/Harris/AN9504.pdf.

[18] Behzad Razavi. The Delta-Sigma Modulator [A Circuit for All Seasons]. *IEEE Solid-State Circuits Magazine*, 8(2):10–15, 2016. URL: http://ieeexplore.ieee.org/document/7495092/, doi:10.1109/MSSC.2016.2543061.

[19] Walt Kester. Adc architectures iii: Sigma-Delta ADC basics. *Analog Devices, MT022*, 2008. URL: http://www.mouser.be/pdfdocs/src-tutorials/ADC-Architectures-III.PDF.

[20] H. Inose, Y. Yasuda, and J. Murakami. A Telemetering System by Code Modulation - ΔΣ Modulation. *IRE Transactions on Space Electronics and Telemetry*, pages 204–209, September 1962.

[21] Max W. Hauser and Maurice Deloraine Edmond. Princples of Oversampling A/D Conversion. *Journal Audio Engineering Society*, 39(1/2):3–26, February 1991.

[22] Hiroshi Inose and Yasuhiko Yasuda. A unity bit coding method by negative feedback. *Proceedings of the IEEE*, 51(11):1524–1535, 1963. URL: http://ieeexplore.ieee.org/abstract/document/1444552/.

[23] Pervez M. Aziz, Henrik V. Sorensen, and Jan Van Der Spiegel. Overview of Sigma-Delta Converters: How a 1-bit ADC achieves more than 16-bit resolution. *IEEE Signal Processing Magazine*, pages 61–84, January 1996.

[24] Zhipeng Ye and Michael Peter Kennedy. Reduced Complexity MASH ΔΣ Modulator. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 54(8):725–729, August 2007. URL: http://ieeexplore.ieee.org/document/4277945/, doi:10.1109/TCSII.2007.896940.

[25] N. Maghari, S.Kwon, G.C. Temes, and U.Moon. Sturdy MASH ΔΣ modulator. *Electronics Letters*, 42(22):1269–1270, 2006. URL: http://ieeexplore.ieee.org/abstract/document/4015909/.

[26] R. Jacob Baker and Vishal Saxena. Design of Bandpass Delta Sigma Modulators: Avoiding Common Mistakes. *various universities and companies*, 2007. URL: http://cmosedu.com/jbaker/papers/talks/BP_DSM_talk.pdf.

[27] Nuno Pereira and Nuno Paulino. *Design and Implementation of Sigma Delta Modulators for Class D Audio Amplifiers using Differential Pairs*. Springer, Caparica, 2015.

[28] Josephus Adrianus Engelbertus Paulus van Engelen. *Stability analysis and design of bandpass sigma delta modulators*. OCLC: 247757439.

[29] Amit Gupta. What's The Difference Between Continuous-Time And Discrete-Time Delta-Sigma ADCs, May 2014. URL: http://www.electronicdesign.com/analog/what-s-difference-between-continuous-time-and-discrete-time-delta-sigma-adcs.

[30] Xi Yang and others. *Design of a continuous-time bandpass delta-sigma modulator*. PhD thesis, Massachusetts Institute of Technology, 2014. URL: http://dspace.mit.edu/handle/1721.1/87939.

[31] Richard Schreier. Understanding Continuous-Time, Discrete-Time Sigma-Delta ADCs And Nyquist ADCs, February 2009. URL: http://www.electronicdesign.com/analog/understanding-continuous-time-discrete-time-sigma-delta-adcs-and-nyquist-adcs.

[32] Bharath Kumar Thandri and Jose Silva-Martinez. A 63 dB SNR, 75 mW Bandpass RF ΣΔ ADC at 950 MHz Using 3.8-GHz Clock in 0.25-μm SiGe BiCMOS Technology. *IEEE Journal of Solid-State Circuits*, 42(2):269–279, February 2007. URL: http://ieeexplore.ieee.org/document/4077178/, doi:10.1109/JSSC.2006.889389.

[33] Nicolas Beilleau, Hassan Aboushady, Franck Montaudon, and Andreia Cathelin. A 1.3 V 26mw 3.2 GS/s undersampled LC bandpass ΣΔ ADC for a SDR ISM-band receiver in 130nm CMOS. In *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, pages 383–386. IEEE, 2009. URL: http://ieeexplore.ieee.org/abstract/document/5135563/.

[34] Julien Ryckaert, Jonathan Borremans, Bob Verbruggen, Lynn Bos, Costantino Armiento, Jan Craninckx, and Geert Van der Plas. A 2.4 GHz Low-Power Sixth-Order RF Bandpass ΔΣ Converter in CMOS. *IEEE Journal of Solid-State Circuits*, 44(11):2873–2880, November 2009. URL: http://ieeexplore.ieee.org/document/5308613/, doi:10.1109/JSSC.2009.2028914.

[35] A 69 dB SNDR, 25 MHz BW, 800 MS/s Continuous-Time Bandpass Modulator Using a Duty-Cycle-Controlled DAC for Low Power and Reconfigurability. *IEEE Journal of Solid-State Circuits*, 51(3):649–659, March 2016. URL: http://ieeexplore.ieee.org/document/7390200/, doi:10.1109/JSSC.2016.2514442.

[36] Inhee Lee, Gunhee Han, and Youngcheol Chae. A 2 mW, 50 dB DR, 10 MHz BW 5×Interleaved Bandpass Delta-Sigma Modulator at 50 MHz IF. *IEEE*

Transactions on Circuits and Systems I: Regular Papers, 62(1):80–89, January 2015. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6913582, doi:10.1109/TCSI.2014.2347234.

[37] Hajime Shibata, Richard Schreier, Wenhua Yang, Ali Shaikh, Donald Paterson, Trevor C. Caldwell, David Alldred, and Ping Wing Lai. A DC-to-1 GHz Tunable RF ΔΣ ADC Achieving DR = 74 dB and BW = 150 MHz at f_0 = 450 MHz Using 550 mW. *IEEE Journal of Solid-State Circuits*, 47(12):2888–2897, December 2012. URL: http://ieeexplore.ieee.org/document/6331570/, doi:10.1109/JSSC.2012.2217860.

[38] Jeffrey Harrison, Michal Nesselroth, Robert Mamuad, Arya Behzad, Andrew Adams, and Steve Avery. An LC bandpass ΔΣ ADC with 70 dB SNDR over 20 MHz bandwidth using CMOS DACs. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pages 146–148. IEEE, 2012. URL: http://ieeexplore.ieee.org/abstract/document/6176901/.

[39] Cho-Ying Lu, Jose Fabian Silva-Rivas, Praveena Kode, Jose Silva-Martinez, and Sebastian Hoyos. A Sixth-Order 200 MHz IF Bandpass Sigma-Delta Modulator With Over 68 dB SNDR in 10 MHz Bandwidth. *IEEE Journal of Solid-State Circuits*, 45(6):1122–1136, June 2010. URL: http://ieeexplore.ieee.org/document/5482513/, doi:10.1109/JSSC.2010.2048505.

[40] Luca Bettini, Thomas Christen, Thomas Burger, and Qiuting Huang. A Reconfigurable DT ΔΣ Modulator for Multi-Standard 2G/3G/4G Wireless Receivers. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 5(4):525–536, December 2015. URL: http://ieeexplore.ieee.org/document/7347471/, doi:10.1109/JETCAS.2015.2502162.

[41] Chanyong Jeong, Yonghwan Kim, and Soowon Kim. Efficient Discrete-Time Bandpa ss Sigma-Delta Modulator for Multistandard Wireless Applications. In *Consumer Electronics, 2008. ICCE 2008. Digest of Technical Papers. International Conference on*, pages 1–2. IEEE, 2008. URL: http://ieeexplore.ieee.org/abstract/document/4588015/.

[42] Takaya Yamamoto, Masumi Kasahara, and Tatsuji Matsuura. A 63 mA 112/94 dB DR IF Bandpass ΔΣ Modulator With Direct Feed-Forward Compensation and Double Sampling. *IEEE Journal of Solid-State Circuits*, 43(8):1783–1794, August 2008. URL: http://ieeexplore.ieee.org/document/4578764/, doi:10.1109/JSSC.2008.925618.

[43] Liang Qi, Sai-Weng Sin, Seng-Pan U, Franco Maloberti, and Rui Paulo Martins. A 4.2-mW 77.1-dB SNDR 5-MHz BW DT 2-1 MASH ΣΔ Modulator With Multirate Opamp Sharing. *IEEE Transactions on Circuits and Systems I: Regular Papers*, pages 1–14, 2017. URL: http://ieeexplore.ieee.org/document/7913658/, doi:10.1109/TCSI.2017.2693921.

[44] Erkan Bilhan and Franco Maloberti. A wide-band 2-path cross-coupled sigma delta ADC. In *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on*, pages 1220–1223. IEEE, 2008. URL: http://ieeexplore.ieee.org/abstract/document/4541644/.

[45] E. Bilhan and F. Maloberti. A Wideband Sigma-Delta Modulator With Cross-Coupled Two-Paths. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 56(5):886–893, May 2009. URL: http://ieeexplore.ieee.org/document/4798185/, doi:10.1109/TCSI.2009.2016867.

[46] Shu-Chuan Huang and Ting-Yen Wang. A tunable SC bandpass delta-sigma modulator with noise-coupled architecture. In *Circuits and Systems (MWSCAS), 2011 IEEE 54th International Midwest Symposium on*, pages 1–4. IEEE, 2011. URL: http://ieeexplore.ieee.org/abstract/document/6026518/.

[47] Maarten De Bock and Pieter Rombouts. A double-sampling cross noise-coupled Sigma Delta modulator with a reduced amount of opamps. In *Custom Integrated Circuits Conference (CICC), 2013 IEEE*, pages 1–4. IEEE, 2013. URL: http://ieeexplore.ieee.org/abstract/document/6658466/.

[48] Chun Lee, Erkan Alpman, Skyler Weaver, Cho-Ying Lu, and Jad Rizk. A 66 dB SNDR 15 MHz BW SAR assisted ΣΔ ADC in 22 nm tri-gate CMOS. *2013 Symposium on VLSI Circuits Digest of Technical Papers*, June 2013.

[49] Thomas Christen and Huang Qiuting. A 0.13 µm CMOS 0.1-20 MHz Bandwidth 86-70 dB DR Multi-Mode DT ΣΔ ADC for IMT-Advanced. *ESSCIRC, 2010 Proceedings of the*, pages 414–417, September 2010. doi:10.1109/ESSCIRC.2010.5619731.

[50] Erkan Bilhan. *Very low power sigma delta modulator for WCDMA*. The University of Texas at Dallas, 2008. URL: http://search.proquest.com/openview/ce4d35750c9e51f6c096a6aacd71a15d/1?pq-origsite=gscholar&cbl=18750&diss=y.

[51] Erwin Janssen and Arthur van Roermund. *Look-Ahead Based Sigma-Delta Modulation*. Springer Netherlands, Dordrecht, 2011. DOI: 10.1007/978-94-007-1387-1. URL: http://link.springer.com/10.1007/978-94-007-1387-1.

[52] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto. Behavioral modeling of switched-capacitor sigma-delta modulators. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 50(3):352–364, March 2003. URL: http://ieeexplore.ieee.org/document/1193017/, doi:10.1109/TCSI.2003.808892.

[53] The LTE Standard. Technical report, Signals Research Group, April 2014. URL: https://www.qualcomm.com/media/documents/files/the-lte-standard.pdf.

[54] Pedro Guedes Oliveira and Dinis Magalhães Santos. Electrónica. February 2015.

[55] Vítor Grade Tavares. *Microelectronics*. Faculty of Engineering of the University of Porto, 2016.

[56] Vítor Grade Tavares and José Machado da Silva. Electronics 3 Course Slides, FEUP, 2014.

[57] Wei Yu and Bosco Leung. Distortion and noise performance of bottom-plate sampling mixers. In *Circuits and Systems, 1998. ISCAS'98. Proceedings of the 1998 IEEE International Symposium on*, volume 4, pages 401–404. IEEE, 1998. URL: http://ieeexplore.ieee.org/abstract/document/698883/.

[58] A. Gharbiya and D.A. Johns. On the implementation of input-feedforward delta-sigma modulators. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 53(6):453–457, June 2006. URL: http://ieeexplore.ieee.org/document/1643460/, doi:10.1109/TCSII.2006.873829.

[59] Behzad Razavi. The Bootstrapped Switch [A Circuit for All Seasons]. *IEEE Solid-State Circuits Magazine*, 7(3):12–15, 2015. URL: http://ieeexplore.ieee.org/document/7258484/, doi:10.1109/MSSC.2015.2449714.

[60] Hongmei Chen, Lee He, Honghui Deng, Yongsheng Yin, and Fujiang Lin. A High-performance Bootstrap Switch for Low Voltage Switched-Capacitor Circuits. *IEEE International Symposium on Radio-Frequency Integration Technology*, 2014.

[61] Hegong Wei, Peng Zhang, Bibhu Datta Sahoo, and Behzad Razavi. An 8 Bit 4 GS/s 120 mW CMOS ADC. *IEEE Journal of Solid-State Circuits*, 49(8):1751–1761, August 2014. URL: http://ieeexplore.ieee.org/document/6784501/, doi:10.1109/JSSC.2014.2313571.

[62] Andrew M. Abo and Paul R. Gray. A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter. *IEEE Journal of Solid-State Circuits*, 34(5):599–606, 1999. URL: http://ieeexplore.ieee.org/abstract/document/760369/.

[63] O. Choksi and L.R. Carley. Analysis of switched-capacitor common-mode feedback circuit. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 50(12):906–917, December 2003. URL: http://ieeexplore.ieee.org/document/1255674/, doi:10.1109/TCSII.2003.820253.

[64] R. Schreier, J. Silva, J. Steensgaard, and G.C. Temes. Design-oriented estimation of thermal noise in switched-capacitor circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 52(11):2358–2368, November 2005. URL: http://ieeexplore.ieee.org/document/1528681/, doi:10.1109/TCSI.2005.853909.

[65] Zhongyi Huang, Menglian Zhao, Sheng Liu, Liyu Lin, Haozhou Zhang, and Xiaobo Wu. A novel switched-OTA utilizing slew-rate boosting for Sigma-Delta modulators. In *Electron Devices and Solid-State Circuits (EDSSC), 2014 IEEE International Conference on*, pages 1–2. IEEE, 2014. URL: http://ieeexplore.ieee.org/abstract/document/7061078/.

[66] Hong-Yi Huang, Bo-Ruei Wang, and Jen-Chieh Liu. High-gain and high-bandwidth rail-to-rail operational amplifier with slew rate boost circuit. In *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, pages 4–pp. IEEE, 2006. URL: http://ieeexplore.ieee.org/abstract/document/1692733/.

[67] Hyungil Chae. *Low Power Continuous-time Bandpass Delta-Sigma Modulators*. PhD thesis, The University of Michigan, 2013.

[68] Ewout Martens, André Bourdoux, Aissa Couvreur, Robert Fasthuber, Peter Van Wesemael, Geert Vander Plas, Jan Craninckx, and Julien Ryckaert. RF-to-Baseband Digitization in 40 nm CMOS With RF Bandpass $\Delta\Sigma$ Modulator and Polyphase Decimation Filter. *IEEE Journal of Solid-State Circuits*, 47(4):990–1002, April 2012. URL: http://ieeexplore.ieee.org/document/6156481/, doi:10.1109/JSSC.2012.2185149.

[69] Hyungil Chae, Jaehun Jeong, Gabriele Manganaro, and Michael Flynn. A 12 mW low-power continuous-time bandpass ΣΔ modulator with 58 dB SNDR and 24 MHz bandwidth at 200 MHz IF. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pages 148–150. IEEE, 2012. URL: http://ieeexplore.ieee.org/abstract/document/6176940/.

[70] Evolution to LTE. 4G Market & Technology Update, Global Mobile Suppliers Association, Sawbridgeworth, United Kindgom, October 2015. URL: https://gsacom.com/content/uploads/2015/10/151013-Evolution_to_LTE_report.pdf.

[71] LTE and 5g Innovation: Igniting Mobile Broadband. Technical report, 4G Americas/Rysavy Research, August 2015. URL: http://www.5gamericas.org/files/9214/3991/2167/4G_Americas_Rysavy_Research_LTE_and_5G_Innovation_white_paper.pdf.

[72] Anritsu. Understanding LTE-Advanced, September 2013. URL: http://dataedge.ie/wp-content/uploads/2013/07/Network-Testing-Understanding-Carrier-Aggregation-web.pdf.

[73] M Kottkamp, A Roessler, and J Schlienz. LTE-Advanced Technology Introduction. Technical report, Rohde & Schwarz, Munich, Germany, August 2012. URL: https://cdn.rohde-schwarz.com/pws/dl_downloads/dl_application/application_notes/1ma169/1MA169_3e_LTE-Advanced_technology.pdf.

[74] Electronic Communications Committee. The European Table of Frequency Allocations and Appications in the Frequency Range 8.3 KHz to 3000 GHz (ECA Table), June 2016.

[75] Thomas Noulis. CMOS process transient noise simulation analysis and benchmarking. In *Power and Timing Modeling, Optimization and Simulation (PATMOS), 2016 26th International Workshop on*, pages 70–75. IEEE, 2016. URL: http://ieeexplore.ieee.org/abstract/document/7833428/.

[76] Phillip E. Allen. Analog Integrated Circuit Design II - Course Slides, 2002. URL: http://pallen.ece.gatech.edu/Academic/ECE_6412/Spring_2003/L400-Discrete-TimeComp-2UP.pdf.

[77] D. Jackuline Moni and P. Jisha. High-speed and low-power dynamic latch comparator. In *Devices, Circuits and Systems (ICDCS), 2012 International Conference on*, pages 259–263. IEEE, 2012. URL: http://ieeexplore.ieee.org/abstract/document/6188715/.

[78] Haideh Khorramabadi. Analog-Digital Interface Integrated Circuits - Course Slides, 2005. URL: https://inst.eecs.berkeley.edu/~ee247/fa05/lectures/L1_f05.pdf.

[79] Akira Matsuzawa. High speed and low power ADC design with dynamic analog circuits. In *ASIC, 2009. ASICON'09. IEEE 8th International Conference on*, pages 218–221. IEEE, 2009. URL: http://ieeexplore.ieee.org/abstract/document/5351489/.

[80] Depu S. P. *Design of Low Power Thermometer Code To Binary Code Encoder Based Flash ADC*. PhD thesis, National Institute of Technology Rourkela, Rourkela, Odisha, India, 2014. URL: http://ethesis.nitrkl.ac.in/6028/1/212EC2129-17.pdf.

[81] Behzad Razavi. The StrongARM Latch [A Circuit for All Seasons]. *IEEE Solid-State Circuits Magazine*, 7(2):12–17, 2015. URL: http://ieeexplore.ieee.org/document/7130773/, doi:10.1109/MSSC.2015.2418155.

[82] Achim Graupner. A Methodology for the Offset - Simulation of Comparators. *The Designer's Guide Community*, 1:1–7, 2006. URL: https://pdfs.semanticscholar.org/e1f5/9620883cebc42d8ecd093ce1915673dcfd6d.pdf.

[83] Open Verilog International. Verilog-A - Language Reference Manual, August 1996.