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ADVANCED FAST HVDC CIRCUIT BREAKERS

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Dissertation

submitted to the Faculty of Engineering
of University of Porto,
in partial fulfilment of the requirements for the degree of
Doctor of Philosophy

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Then of the Thee in Me who works behind
The Veil of Universe I cried to find
A Lamp to guide me through the darkness; and
Something then said - 'An Understanding blind.'

Omar Khayyam, Iranian Mathematician, Philosopher, and Poet, 1048-1131.

Translated by Edward FitzGerald, British Poet and Writer, 1809-1883.

To my wife,
Fatemeh,

for her love,
her patience,
and her faith.

&

To my parents,
Naiemeh & Rahim,

for guiding me,
supporting me,
and for missing me.

Summary

Climate change will be one of the biggest threatening challenges for mankind in the following decades. This phenomenon is caused by global temperature rise on the surface of Earth which is called global warming. The main reason for global warming is the increasing emissions of man-made greenhouse gases (GHGs) in the atmosphere. Increasing population of the world will increase the total consumption and demand for energy. More population together with the growing economy in the developing countries will increase the amount of GHG emissions in the future if strict measures are not taken.

In order to mitigate the GHG emissions, the demanded energy must be supplied from carbon-free resources such as hydro, wind, solar and etc. European Union (EU) as the third producer of GHG plays a significant role in preventing the destructive consequences of the climate change from happening. EU is now leading the world in harvesting green energy from offshore and onshore wind farms.

Due to the geographical location, average distance and size of newly constructed and planned offshore wind farms, High Voltage Direct Current (HVdc) has been employed as the power transmission technology by the project developers. The interconnections between the HVdc converters and offshore wind farms can form a Multi-terminal HVdc (MT-HVdc) grid. The MT-HVdc grid can reduce the effects of fluctuation in renewable energy generation, enhance the security of supply and improve the reliability.

Although a European offshore MT-HVdc grid connecting offshore wind farms to shore could provide significant financial, technical and environmental benefits to the European electricity market, it has not been yet realized due to a few technical drawbacks. The main obstacle to the establishment of an MT-HVdc grid is immaturity of HVdc current interrupting technologies. The existing HVdc circuit breaker solutions suffer from either long interruption time, high conduction losses or high implementation cost.

Therefore, the main objective of this thesis is to propose and study improved HVdc circuit breaker topologies. The main challenges associated with the solid-state and hybrid dc circuit breakers include the need for a large number semiconductor switches in their main breaker branch and large surge arresters to limit the transient recovery voltage and absorb the system energy. This thesis proposes novel approaches for improving the performance if HVdc circuit breakers in order to tackle the mentioned problems. Furthermore, this thesis proposes a new type of dc circuit breaker with additional functionality as a current flow controller.

A comprehensive literature review on different types of HVdc circuit breakers including electromechanical, solid-state and hybrid dc circuit breakers has been carried out. The dc circuit breakers have been classified in several categories. The superiorities of each topology have been highlighted and the main drawbacks of each dc circuit breaker type have been identified.

In order to reduce the conduction power losses of the solid-state dc circuit breaker a couple of topological changes have been proposed and studied. Firstly, the semiconductor switches of the solid-state dc circuit breaker are connected unidirectionally. This approach halves the number of series connected switches. Secondly, a new current releasing branch is proposed and employed instead of the surge arrester branch. The new current releasing branch limits the transient recovery voltage across the solid-state dc circuit breaker more effectively and reduce the number of series connected switches. Therefore, the conduction power losses of the solid-state dc circuit breaker can be reduced significantly using the proposed scheme.

Unidirectional HVdc circuit breakers are technically attractive due to the less number of switches and peripheral circuitries and also the reduced requirement for cooling systems. A unidirectional protection strategy is proposed for the protection of MT-HVdc grid using the unidirectional dc circuit breakers. The proposed strategy has been validated through the integration of unidirectional hybrid dc circuit breaker into the MT-HVdc grid. In addition, the proposed unidirectional solid-state dc circuit breaker is integrated to the MT-HVdc grid and the results are compared with the typical solutions.

Another identified issue is related to the requirement for employment of parallel branches in the structure of main breaker unit and large surge arrester branch in the hybrid dc circuit breaker structure. A superconducting fault current limiter unit is integrated into the hybrid dc circuit breaker and its impact on the current interruption capability and the amount of absorbed energy by the surge arresters are assessed. The results show a significant reduction in the maximum fault current interruption capability of the hybrid dc circuit breaker after employment of superconducting fault current limiter. Moreover, the amount of absorbed energy by the surge arresters is notably reduced. Furthermore, the size of the current limiting inductor can be reduced without increasing the current interruption capability.

The number of required semiconductor switches by the hybrid dc circuit breaker can be comparable to a converter station in some HVdc configurations. A novel concept of multi-port hybrid dc circuit breaker is proposed for offshore MT-HVdc applications. The proposed hybrid dc circuit breaker has n ports and can substitute $n-1$ hybrid dc circuit breakers at a dc node with one converter station and $n-1$ adjacent transmission lines. The proposed scheme can mitigate the number of semiconductor switches and the size of surge arresters dramatically, particularly when the number of adjacent transmission lines increases.

The power flow control is also one of the identified challenges in the realization of a complex form of MT-HVdc grid called meshed HVdc grid. In order to control the power flow in the meshed HVdc grids, additional power flow controller devices are required. A novel three-port hybrid dc circuit breaker is proposed to address both protection and power flow problems in meshed HVdc grids. This circuit breaker can connect a power converter station with two adjacent transmission lines. The proposed hybrid dc circuit breaker possesses an embedded dual H-bridge current flow controller and can control the power flow in one of the adjacent transmission lines. This method can reduce the number of required semiconductor switches and the size of surge arresters, significantly.

Since this thesis proposes a few novel concepts in dc circuit breaker field, a notable amount of future work can be planned. Briefly, the medium voltage implementation and tests of the proposed surge-less dc circuit breaker, lab-scale prototype development of multi-port hybrid dc circuit breaker, and lab-scale prototype implementation of the current flow controlling hybrid dc circuit breaker can be listed as some of the future experimental works. In addition, the theoretic analysis will continue to cover the current commutation process in the multi-port hybrid dc circuit breakers, failure modes of hybrid dc circuit breaker, common failure modes of multi-port and current flow controlling hybrid dc circuit breaker and reliability analysis of the multi-port and the current flow controlling hybrid dc circuit breakers.

Sumário

As alterações climáticas serão, nas próximas décadas, um dos mais ameaçadores desafios que a humanidade enfrentará. Na sua origem está o aumento global da temperatura à superfície do planeta, fenómeno habitualmente designado de aquecimento global. A principal causa do aquecimento global é o crescente aumento das emissões de gases de efeito de estufa (GEE) para a atmosfera, com origem sobretudo na atividade humana. O aumento da população, conjugado com o crescimento das economias, sobretudo nos países em vias de desenvolvimento, traduzir-se-á no curto/médio prazo num aumento da procura de energia, o que terá como consequência certa, no caso de não serem tomadas as medidas adequadas para o seu controlo, o aumento das emissões de GEE.

De forma a mitigar as emissões de GEE, o aumento da procura de energia deverá ser satisfeita a partir de fontes renováveis, livres de carbono, tais como as energias hídrica, eólica ou solar. Detendo a terceira posição a nível mundial no que diz respeito às emissões de GEE, a União Europeia (UE) tem um papel determinante na prevenção do aquecimento global, cujas consequências podem ser devastadores. A UE é atualmente líder mundial na produção de energia verde com origem eólica, tendo centrais instaladas tanto em terra como ao longo da plataforma marítima continental.

Devido à sua posição geográfica na plataforma marítima continental, à distância média a terra e ao tamanho dos parques eólicos já construídos e projetados, a opção escolhida para transportar a energia neles produzida tem sido a alta tensão em corrente contínua, HVdc na sigla inglesa. A constituição de uma rede HVdc Multi-terminal (MT-HVdc), englobando vários parques eólicos localizados na plataforma marítima continental, pode contribuir para a redução da flutuação na produção associada a este tipo de energia, melhorando o aprovisionamento e a fiabilidade da rede de abastecimento. Apesar de apresentar consideráveis vantagens a nível técnico e económico e, consequentemente, benefícios a nível ambiental, a concretização deste objetivo não tem sido fácil, sobretudo devido a limitações técnicas. A principal dificuldade prende-se com a imaturidade da tecnologia associada aos disjuntores para HVdc. As soluções atualmente existentes apresentam limitações, nomeadamente no que diz respeito aos tempos de abertura elevados e às perdas em condução, para além do elevado custo de implementação.

O objetivo principal desta tese é o de propor novas soluções tendo em vista a melhoria das topologias dos disjuntores para HVdc. Os principais desafios associados aos disjuntores baseados em semicondutores ou disjuntores dc híbridos prendem-se com a necessidade de incluir um elevado número de comutadores no ramo principal do disjuntor, assim como um número elevado de supressores de sobretensões, por forma a limitar o transitório de tensão e a absorver a energia do sistema. A tese propõe soluções inovadoras para melhorar o desempenho dos disjuntores para HVdc com o objetivo minorar os problemas descritos. Para além disso, é ainda proposto um novo tipo de disjuntor para HVdc, com funcionalidades adicionais, nomeadamente um controlador de intensidade da corrente elétrica.

Após uma ampla revisão bibliográfica que incluiu diferentes tipos de disjuntores para HVdc - eletromecânicos, de estado sólido e híbridos, estes foram classificados por categoria, tendo-se identificado as vantagens apresentadas por cada topologia e os problemas associados a cada tipo.

Com o objetivo de reduzir as perdas em condução associadas aos disjuntores de estado sólido, foram

estudadas e propostas algumas alterações de ordem topológica. A primeira delas prende-se com a unidirecionalidade da condução, medida que permite a redução para metade do número de comutadores ligados em série. Em segundo lugar, é proposta a criação de um ramo alternativo para desviar a corrente em alternativa ao ramo utilizado para suprimir sobretensões. O novo ramo limita a amplitude do transitório de tensão aplicado ao disjuntor de estado sólido de forma mais eficiente, reduzindo igualmente o número de comutadores ligados em série. Desta forma, as perdas de condução do disjuntor dc de estado sólido podem ser significativamente reduzidas.

Os disjuntores unidirecionais para HVdc são tecnicamente atrativos devido ao menor número de comutadores e circuitos periféricos necessários e, consequentemente, menores requisitos em termos do sistema de arrefecimento associado. A estratégia proposta de proteção unidirecional para redes MT-HVdc suportada por disjuntores unidirecionais para HVdc foi validada com a integração de um disjuntor unidirecional híbrido para HVdc numa rede MT-HVdc, sendo os resultados obtidos comparados com outras soluções já conhecidas.

Outro dos problemas identificados prende-se com a utilização de ramos em paralelo com o ramo principal do disjuntor e no ramo supressor de sobretensões que fazem parte da estrutura do disjuntor dc híbrido. Uma unidade supercondutora, limitadora da corrente de falha foi integrada no disjuntor dc híbrido, tendo sido avaliado o seu impacto na capacidade de corte do disjuntor e na energia absorvida pelos supressores de sobretensões. Os resultados mostram uma redução significativa da corrente de falha. Acresce também que a quantidade de energia absorvida pelos supressores de sobretensões é notavelmente reduzida, ao passo que o tamanho da bobine limitadora de corrente pode ser reduzida sem comprometer a capacidade de corte do disjuntor.

O número de comutadores de estado sólido do disjuntor dc híbrido é comparável ao número de comutadores de um conversor de potência para HVdc. Um novo conceito para disjuntor dc híbrido multiporta é proposto para aplicações MT-HVdc localizadas na plataforma marítima continental. Este disjuntor inclui n portas e pode substituir n-1 disjuntores dc híbridos existentes num nó dc constituido por um conversor de potência e n-1 linhas de transmissão adjacentes. O esquema proposto mitiga o número de comutadores de estado sólido e o tamanho dos supressores de sobretensões de forma dramática, particularmente se existir um aumento no número de linhas de transmissão adjacentes. O controlo do trânsito de potência é também um dos desafios identificados na conceção de um sistema MT-HVdc de maior complexidade, denominado malha de redes MT-HVdc. O controlo do trânsito de potência nesta malha de redes MT-HVdc requere controladores adicionais. Como forma de colmatar esta necessidade, é proposto um novo disjuntor híbrido dc de três portas, o qual suporta funções de proteção e outras relacionadas com o trânsito de potência em malha de redes MT-HVdc. Este disjuntor, que inclui no seu seio um controlador de trânsito de corrente suportado por duas pontes H, permite interligar um conversor de potência a duas linhas de transmissão adjacentes, sendo capaz de controlar o trânsito de potência numa dessas linhas. Este método reduz o número de comutadores necessários e o tamanho dos supressores de sobretensões de forma significativa.

Dado que esta tese propõe vários conceitos inovadores na área dos disjuntores dc, uma quantidade apreciável de trabalho futuro pode ser desde já identificado. De forma breve, destaca-se a implementação e teste do disjuntor proposto para média tensão sem supressor de sobretensões e o desenvolvimento de um disjuntor dc híbrido multiporta e de um protótipo do disjuntor dc híbrido capaz de controlar o trânsito de potência, ambos em escala laboratorial. Para além disto, a continuação da análise teórica incidirá no processo de comutação de corrente nos disjuntores dc híbridos multiporta, na identificação dos modos de falha do disjuntor dc híbrido e do disjuntor dc híbrido multiporta controlado por corrente e na análise da fiabilidade do disjuntor dc híbrido multiporta controlado por corrente.

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Part I

Introduction & Literature Review

1
Introduction

The Earth also has a thermostat, and until recently the Earth was in charge of its own temperature setting. But much to the surprise of many scientists, and the disbelief of almost everyone else, over the past two centuries some of that control has been taken over by humans.

Tony Eggleton, A Short Introduction to Climate Change, 2012

1.1 General Background

According to the United States Environmental Protection Agency (US EPA), climate change refers to "any significant change in the measures of climate lasting for an extended period of time. In other words, climate change includes major changes in temperature, precipitation, or wind patterns, among other effects, that occur over several decades or longer" [1]. The reality and significance of climate change have been doubted by different groups, frequently. Even the climate scientists have been accused of over-interpreting the human impacts on climate system to attract media attention and funding for their research [2]. However, recent findings based on the available evidences confirm that the impacts of climate change have been under-estimated by the scientists. For instance, some of the key findings can be listed as follows [2]:

- The rainfall has increased earlier than predicted in already rainy areas.
- The global average sea level rise was equal to 3.4 mm/yr for period between 1994 and 2009, which is 80% higher than the past IPCC[1] predictions.
- Increase in surface ocean temperature between 1963 and 2003 was 50% higher compared to the previous calculations.
- The melting of Arctic sea-ice phenomenon has accelerated significantly exceeds the expectations.
- CO_2 emissions can be fit to the worst-case scenarios developed in 1999.

[1] Intergovernmental Panel on Climate Change

Climate change is a consequence of global warming which refers to the recent and ongoing rise in global average temperature near

Earth's surface [1]. The main cause of global warming is the high emission of man-made Greenhouse Gases (GHGs) in the atmosphere of Earth [3]. Figure 1.1 shows the atmospheric CO_2 content since 1750 until 2000. Figure 1.2 depicts the global land-based temperature since 1880 until 2000 [4].

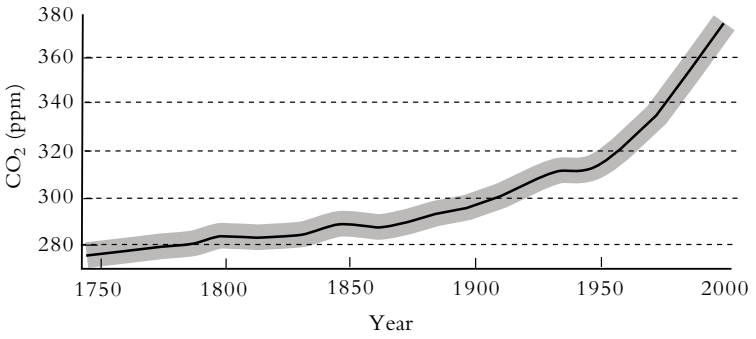


Figure 1.1: Atmospheric CO_2 content from 1750 to 2000. The pale gray strip covers the range of variation between the different studies [4].

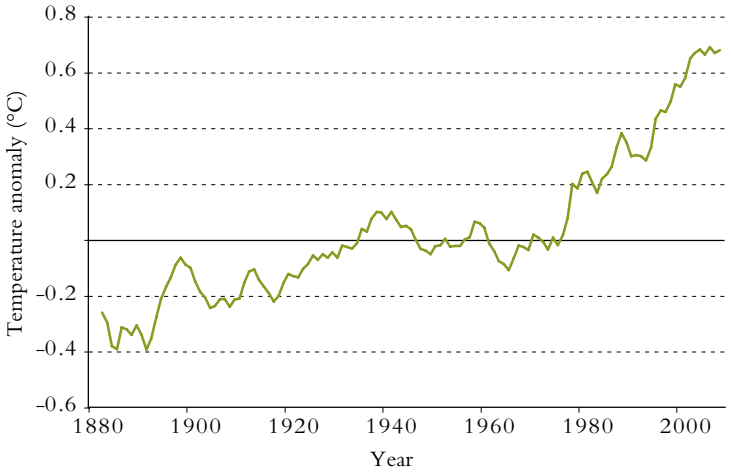


Figure 1.2: The global land-based temperature anomaly (5-year running mean). The base period for the anomaly (black line) is 1951-80 [4].

Many years ago, environmental disruption has been related to the population, consumption per person and damage per unit of consumption by John P. Holdren [5]. Despite the simplicity of this relation, it has been identified to be valid for GHG emissions in new era. A very recent study on identification of key impact factors on carbon emission based on the data of 125 countries figures out that the key impact factors (KIFs) of global carbon emission are affluence[2], technology[3] and population [6]. Figure 1.3 illustrates the significance of each factor in global carbon emission.

The world population[4] has been tripled since 1950. The world population is foreseen to reach 9.268 billion till 2050, which is approximately 23% more than the current population [7]. In other words, the world will have almost 150000 additional people each day. The increasing population requires to have access and consume more resources to address its vital and also unessential needs. It is also projected that a large portion of the population growth is related with the

[2] Affluence represents the average consumption of each person in the population.

[3] Technology represents the amount of damage per unit of consumption.

[4] The world population in 1950 was 2.524 billion and as April of 2017 it is almost 7.5 billion.

increase of population in the urban areas in developing countries [8]. Urban areas are the social center of human life and consumption. The primary sources of energy consumption and hence GHG emissions are cities. The cities emit almost 70% of the world's GHGs [9].

There is a global agreement that the world needs ambitious climate change mitigation and adaptation plans of action [10]. The climate change would have destructive effects on different aspects of human life. The combined impact of climate change on global annual Gross Domestic Product (GDP) is projected to be between 1.0% up to 3.3%, until 2060. Climate induced damages from extreme events (e.g. hurricanes), as well as damages incurred due to energy and tourism are expected to have a significant impact on a local scale [11,12]. The hydro-power generation can be decreased in future due to the impacts of climate change. For instance, hydro-power generation in Portugal may decrease by 41% in 2050. Even considering the developments in the solar and wind energy sectors, this can result in up to 17% higher electricity prices [13].

The combustion of fossil fuels is by far the largest human source of GHG emissions [14]. The GHG emissions should be mitigated at both consumer and supply sides. However, the supply-side policies can be more effective. Majority of consumers consume the energy provided by the system. Therefore, supplying the consumer with green energies in entire world is definitely required[5], which is not straightforward. If the global temperature rise is to be kept under the 2 °C limit of the Paris agreement[6] [10], one-third of the world's oil reserves, more than 90% of Australia's coal reserves, and virtually all Canada's oil sands must be left in the ground [16].

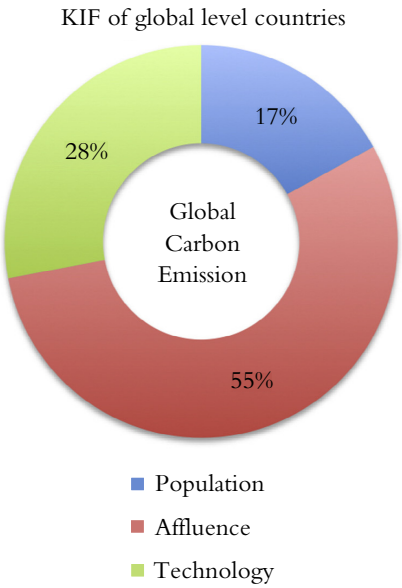


Figure 1.3: Key impact factors on global carbon emission [6].

[5] The electricity and heat production, as the primary source of global GHG emissions was responsible for a quarter of total GHG emissions in 2014 [15].

[6] The Paris Agreement is an agreement within the United Nations Framework Convention on Climate Change (UNFCCC). This agreement deals with the mitigation, adaptation and financing of global GHG emissions [10].

1.2 *Technical Motivation*

European Union (EU) has been the third GHG emitter after China and the United States (US), responsible for 10.9% of the global GHG emissions [17]. As one of the main players in mitigating the GHG emissions, EU had reduced its GHG emissions by 19.2% in 2012 as compared to its emissions in 1990 [18]. Wind, hydro and solar energy resources are the main renewable energy resources in Europe. Most of the suitable lands for harvesting these types of energy have already been exploited. Particularly, the potential areas of wind energy resources with capacity for massive power generation are located near sea or offshore far from the consumption centers in Europe [19].

The average rated capacity of turbines installed in 2016 was 4.8 MW, 15.4% larger than their size in 2015. In the last ten years, the average size of wind farm has increased dramatically from 46.3 MW to 379.5 MW for offshore wind farms under construction in 2016. The average water depth of offshore wind farms with grid-connections in 2016 was 29.2 m and the average distance to shore was 43.5 km. Even, plans for construction of offshore wind farms at 200 km distance from the coast have been consented [20].

Considering the plant size, distance from consumption centers and submarine transmission requirements, conventional ac transmission link cannot be the best solution. However, due to the less power losses, available submarine cables, less cable charging current and better active and reactive power control the High-Voltage Direct Current (HVdc) transmission technology has been identified to be the most effective solution for integration of most of the offshore wind farms into the conventional ac grid in Europe [19].

The HVdc substations can be interconnected and form a Multi-terminal HVdc (MT-HVdc) grid. MT-HVdc grid can increase the integration of all renewable energy resources e.g. hydro, wind and solar from different geographical areas. Consequently, the integration of renewable resources through an MT-HVdc grid can decrease their variability due to the different weather conditions. The MT-HVdc grid can increase the reliability and also the security of supply. Moreover, the MT-HVdc grid can contribute into the stability of conventional ac grid and also provide the ac grid with reactive power support [21].

In addition to the lack of investment and political motivation, there are a couple of technical challenges toward realization of multi-GW MT-HVdc grids. The main issues can be listed as follows:

- Power flow control.
- MT-HVdc protection.

A complex form of MT-HVdc grid with meshed connections is called Meshed HVdc (M-HVdc) grid. The M-HVdc grid can face power flow control problems. Typically, the power flow in the M-HVdc grid is controlled by regulating the converters' dc side voltage considering the transmission line impedance. Due to the M-HVdc grid topology, there are multiple paths for the current to circulate between two different nodes. Several solutions have been proposed in the literature including additional Current Flow Controller (CFC) devices. However, their behavior under different conditions of the M-HVdc grid must be investigated further [22].

Along with the development of MT-HVdc concept, the protection issue has been identified as a major drawback of its realization. The MT-HVdc grid protection is not as mature as the protection system of the conventional ac grid [21]. The main issue is related to the dc current interruption which has been an engineering challenge since the dawn of HVdc technology. Due to the absence of natural zero crossing point in dc current, the ac circuit breakers become useless for dc applications [23].

The early research in this field led to development of mechanical HVdc circuit breakers in 70s. The old mechanical HVdc circuit breakers are designed based on the protection requirements of Line-Commutated Converter (LCC) based point-to-point HVdc links. However, the protection requirements of MT-HVdc grids based on Voltage Source Converters (VSCs) are different. The new protection requirements can be determined considering the power converter behavior during the dc short circuit fault. Typically, the power converters with

less power losses are defenseless against the short circuit faults in their dc side. The semiconductor components of these types of converters are exposed to high currents during the dc fault condition and cannot survive more than a few milliseconds without additional measures [24]. Therefore, the development of fast HVdc circuit breakers is strongly needed to protect the power converter stations.

On the other hand, the fault tolerant power converters can prevent the dc fault current from propagation and provides the reactive power support for the ac grid during the dc fault condition. These converter topologies have more power losses than the other topologies [25].

The application of Fault Current Limiters (FCLs) in either ac or dc sides of the power converters can also limit the peak of fault current. The fault tolerant power converters and the FCL application may limit the need for fast HVdc circuit breaker and also may reduce the circuit breaker size. But, to keep the grid protection scheme seamless and selective and to disconnect the faulty line from the healthy parts of the grid, the HVdc circuit breakers will still be needed [21].

1.3 Research Questions

There is a little doubt that the dc Circuit Breakers (dcCBs) have to be investigated further in order to propose more efficient solutions from both electrical and economic points of view. The main objective of this thesis is:

> *"to propose and study advanced solid-state and hybrid dc circuit breaker topologies with improved technical performances."*

Five research questions and related methodologies that have been addressed in this thesis are as follows:

1. *Is it possible to reduce the conduction power losses of an SSCB by more than 50%?*
   - Study the switching overvoltage in fast dcCBs interrupting load or fault current.
   - Propose a new topology considering the origin of overvoltage.
   - Modeling and theoretic analysis of the proposed scheme.
   - Propose the detailed design process for integration into the MT-HVdc grid.
   - Comprehensive computational analysis of the proposed scheme.
   - Development and test of a small lab-scale prototype as proof of concept.
2. *How can an MT-HVdc grid be protected by unidirectional dcCBs?*
   - Propose a unidirectional protection strategy for protection of MT-HVdc grid.
   - Study the application and performance of unidirectional Hybrid dc Circuit Breaker (HCB) in an MT-HVdc grid protected by the proposed strategy.

- Study the application and performance of the proposed dc circuit breaker in chapter 3 in an MT-HVdc grid protected by the proposed strategy.

3. *What is the impact of SFCL on the current interruption capability of proactive HCB in MT-HVdc grids protected by fast fault identification relays?*

   - Introduce the fault current limiting HCB.
   - Develop suitable models of superconducting fault current limiting unit for simulation and analysis.
   - Perform the analysis using the simplified model of a dc system.
   - Computational analysis of the current limiting HCB in an MT-HVdc grid protected by state of the art fast protective relays.
   - Sensitivity analysis of the current limiting HCB

4. *Is it possible to have a multi-port interrupting device instead of conventional two-port dcCB concept for protection of MT-HVdc grid?*

   - Introduce the basic and generalized topology of a novel multi-port HVdc circuit breaker.
   - Perform the analysis using the simplified model of an MT-HVdc grid.
   - Computational analysis of the multi-port hybrid dc circuit breaker in an MT-HVdc grid protected by state of the art fast protective relays.
   - Perform a comparison study considering the existing method.

5. *Is it possible to have a dcCB which can control the power flow in the MT-HVdc grid?*

   - Introduce the topology of a novel 3-port current flow controlling hybrid HVdc circuit breaker.
   - Perform the analysis using the simplified model of an MT-HVdc grid.
   - Computational analysis of the current flow controlling hybrid dc circuit breaker in an MT-HVdc grid protected by state of the art fast protective relays.
   - Perform a comparison study considering the existing method.

1.4 Thesis Outline

This thesis is organized in five parts. Each part includes one or more chapters dealing with the aforementioned topics.

Part I. Introduction & Literature Review

Part I includes chapters 1 and 2. The general background and the motivation for research on HVdc circuit breakers are presented in chapter 1. The behavior of different power converters during dc side short circuit fault has been surveyed in chapter 2. Thereafter, a comprehensive literature review on different technologies of HVdc circuit breakers has been carried out. Superiorities and drawbacks associated with each type of dc circuit breakers have been highlighted in chapter 2.

Part II. Surge-less dc Circuit Breaker & its Application in MT-HVdc

Chapters 3 and 4 are included in Part II. After exploring the transient switching overvoltage issue in the fast dcCBs, a new topology of surge-less SSCB called CRCB is proposed in chapter 3. The transient recovery voltage across the proposed CRCB can be kept below 1.2 pu and hence the CRCB does not require surge arresters for overvoltage limiting. Suitable model of the proposed CRCB has been developed and analysis has been carried out based on the developed model. The results from detailed computational analysis based on Electro Magnetic Transients Program (EMTP) of the proposed CRCB are presented. The sensitivity of CRCB performance on variation of its internal parameters and also the grid parameters are studied through the computational sensitivity analysis. Finally, a small lab-scale prototype is developed and tested in order to proof the proposed concept.

The proposed CRCB in chapter 3 is a unidirectional type dcCB. In order to clarify the application of unidirectional dcCBs in protection of the MT-HVdc systems, a unidirectional protection strategy is introduced in chapter 4. Firstly, the performance of unidirectional HCB in protection of the MT-HVdc grid based on the proposed strategy is investigated. Thereafter, the proposed CRCB is employed as the protective device to protect the MT-HVdc grid. Finally, important remarks on the application of unidirectional dcCBs in protection of MT-HVdc grid based on the obtained results are provided.

Part III. Fault Current Limiting dc Circuit Breaker

Part III includes only chapter 5. Chapter 5 proposes the series connection of a superconducting based fault current limiter (SFCL) with an HCB. The chapter aims to study the impacts of SFCL unit on different parameters of dcCB including current interruption capacity, current limiting inductor size and energy capability of surge arresters. The novelty of this chapter is mainly due to performing this study for an MT-HVdc grid protected by fast protective relays which typically does not require fault current limiters. After theoretic evaluation of the proposed scheme, detailed computational analysis have been carried out to study the aforementioned impacts. The obtained results are discussed and a computational sensitivity analysis is also carried out.

Part IV. Multi-port HVdc Circuit Breakers

Two chapters are included in Part IV of this thesis. Chapter 6 presents a novel topology of hybrid Multi-port dc Circuit Breaker (Mp-HCB). Theoretic analysis of the Mp-HCB integrated into the MT-HVdc grid is carried out. Thereafter, a comparison study between the existing solution and the Mp-HCB is done. The performed analysis is validated through a simulation study using a three-terminal grid model. Moreover, the functionality of Mp-HCB is examined through a simulation study of a detailed MT-HVdc model with a state of the art protection system.

Chapter 7 presents a new Current Flow Controlling dc Circuit Breaker (CFCCB). Despite the conventional concept of dcCB, the CFCCB has three ports and can connect a converter station with two adjacent transmission lines. Firstly, the topology and operation principles are presented and thereafter, the proposed scheme has been analyzed theoretically. Results from computational analysis to validate the functionality of the proposed CFCCB are demonstrated. Finally, a comparison study has been carried out between the CFCCB and the typical solution.

Part V. Conclusion & Future Work

Chapter 8 presents the general conclusions of this thesis and also a brief proposal on future works is included in this chapter.

2
Literature Review

Money cannot buy everything, and at some point even the fattest wallet empties out. By contrast, knowledge does not. We can always generate more. .... Knowledge is the most democratic source of power.

Alvin Toffler, Powershift: Knowledge, Wealth, and Violence at the Edge of the 21st Century, 1990.

The general motivation behind the development of the MT-HVdc grid is presented in the introduction chapter. Furthermore, it was mentioned that the main challenge in the realization of MT-HVdc grid is related to its protection.

The introduction of the Insulated Gate Bipolar Transistor (IGBT) in the 90s paved the way for the realization of VSCs in high power and voltage scales. The VSCs demonstrate enough outstanding features (e.g. high controllability, black-start capability, power transfer reversal without requirement for voltage reversal, no reactive power consumption, etc) to be known as the best candidate to form the backbone of the future MT-HVdc grids [19,21,26]. The VSC technology has been operational by realization of conventional two-level converter topology and nowadays it is represented by Modular Multilevel Converter (MMC) topologies [27,28].

The behavior of different types of converters under dc side short circuit fault condition are reviewed in this chapter. After that, different technologies of dcCBs are surveyed and classified in four main categories. Finally, the superiorities and drawbacks of each technology are highlighted and the potential areas for further research are identified.

Some parts of this chapter has been published in:

Mokhberdoran, A.; Carvalho, A.; Leite, H.; Silva, N., "A review on HVDC circuit breakers," *The 3rd Renewable Power Generation Conference (RPG2014)*, 24-25 September, 2014, pp. 1-6, doi: http://10.1049/cp.2014.0859.

2.1 Voltage Source Converters Under dc Fault

2.1.1 Conventional Voltage Source Converters

Conventional VSCs include two-level and three-level converters. The two-level converters have been applied in several HVdc projects including Estlink1[1], BorWin1[2], East-West Interconnect[3] and etc [21].

Figure 2.1 shows a two-level VSC when a pole-to-ground short circuit fault happens at its dc side. The pole-to-ground fault includes two stages as follows [29]:

- Capacitor discharge stage
- Grid current feeding stage

After occurrence of a pole-to-ground fault at one of the poles of VSC, the corresponding capacitor starts discharging with a high rate of rise current due to the lower inductance between the capacitor and the fault location [29]. The dc link voltage will not drop to zero and hence no freewheel diode conduction occurs [29]. The capacitor discharging stage continues until its voltage drops to below any grid phase voltage [29]. At this time, the fault current will be supplied by the ac grid [30], which can be considered as the forced response of the system.

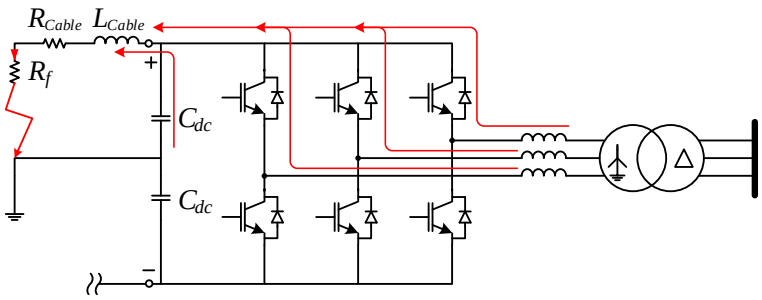


Figure 2.1: Two-level VSC during pole-to-ground short circuit dc fault.

Figure 2.2 shows a two-level VSC when a pole-to-pole short circuit fault happens at its dc side. The pole-to-pole fault includes three stages as follows [29]:

- Capacitor discharge stage
- Diode free-wheel stage
- Grid current feeding stage

Upon occurrence of a pole-to-pole fault, both dc side capacitors start discharging and cause a sharp fault current [29]. The capacitors discharging stage continues until the voltage of dc link falls to zero [30]. At this time, the diode free-wheel stage starts due to the discharge of cable inductance. This is the most severe phase for the VSC antiparallel diodes. During this stage the fault current flows through the antiparallel diodes of the VSC. The initial value of free-wheel current

[1] Estlink1 is an HVdc submarine power cable between Estonia and Finland. The total length of connection is 105 km and the power capacity is equal to 350 MW. The dc side has two poles and its voltage is ±150 kV.

[2] BorWin1 is the first VSC-HVdc connection in the world that has been built for importing power from an offshore wind park to shore. Borwin1 is installed for for transferring the power from the offshore wind park BARD Offshore 1 and other offshore wind farms in Germany near Borkum to the ac power grid. The total length of connection is 200 km and the power capacity is equal to 400 MW. The dc side has has a bipole configuration with the voltage of ±150 kV.

[3] East-West Interconnect is an HVdc submarine and subsoil power cable which connects the British and Irish power grids. The total length of connection is 261 km and the power capacity is equal to 500 MW. The dc side has has a bipole configuration with the voltage of ±200 kV.

can be very high and can immediately damage the diodes [30]. After the diode free-wheel stage, the fault current will be supplied by the ac grid [30]. Depending on the short circuit level of the ac grid, the dc fault current can have a high steady-state value [31,32].

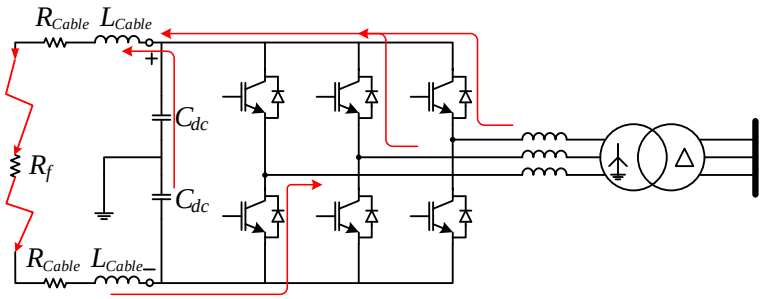


Figure 2.2: Two-level VSC during pole-to-pole short circuit dc fault.

Three-level converters have been utilized in two HVdc projects so far including Murray link[4] and Cross Sound Cable[5] [33].

The three-level converters mainly include Neutral Point Clamped (NPC) and Active Neutral Point Clamped (ANPC) converters and were initially proposed in [34]. The NPC converter can generate positive and negative voltage at its output similar to the conventional two-level converters. In addition, this type of converter can generate zero voltage level [34].

The three-level VSC is employed to enhance transmission capacity of the VSC-HVdc system and the principles of active and reactive power control for the HVdc system based on this type of converter are presented in [35]. A precise and comprehensive model of the back-to-back HVdc system based on the NPC converter using the generalized state-space averaging method and the principle of power balance are presented in [36]. The developed model introduces a systematic design procedure for the ac side controllers, the voltage balancer of the dc side capacitors and the net dc-bus voltage controller [36]. The application of Selective Harmonic Elimination (SHE) Pulse Width Modulation (PWM) for a three-level NPC converter in VSC based HVdc has been investigated [37]. The results show notable improvement in the switching losses of converter as compared to the two-level VSC [37]. The power flow control and dc capacitor voltage balancing using fast optimum-predictive-based controllers in the NPC converter based HVdc systems have been investigated in [38]. A direct power control scheme for NPC based HVdc system is demonstrated in [39].

The NPC converters can be designed to synthesize more number of levels than the three-level converter. Although, the application of multi-level converters would be advantageous in HVdc projects, the drawbacks of NPC converters do not allow them to become a permanent player in the HVdc industry. The NPC converters, utilizes dc link capacitors in series connection, which makes their voltage balancing problematic. Furthermore, the series connection of

[4] Murray link is an HVdc link between Berri in South Australia and Red Cliffs in Victoria, connecting the two state electricity grids. The total length of connection is 180 km and the power capacity is equal to 220 MW. The dc side has has a bipole configuration with the voltage of $\pm$150 kV.

[5] Cross Sound Cable is an HVdc submarine power cable between New Haven, Connecticut, USA and Shoreham, Long Island New York, USA. The total length of connection is 40 km and the power capacity is equal to 330 MW. The dc side has has a bipole configuration with the voltage of $\pm$150 kV.

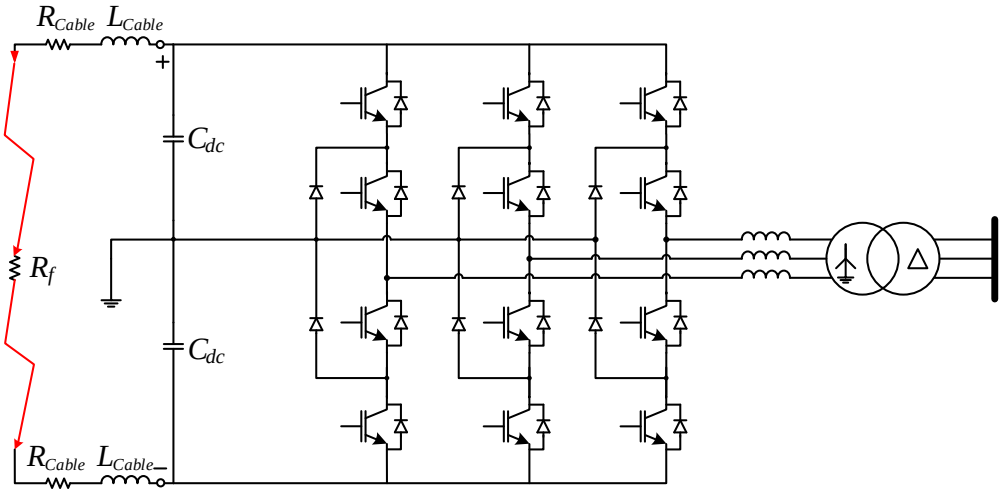


Figure 2.3: Three-level NPC converter topology.

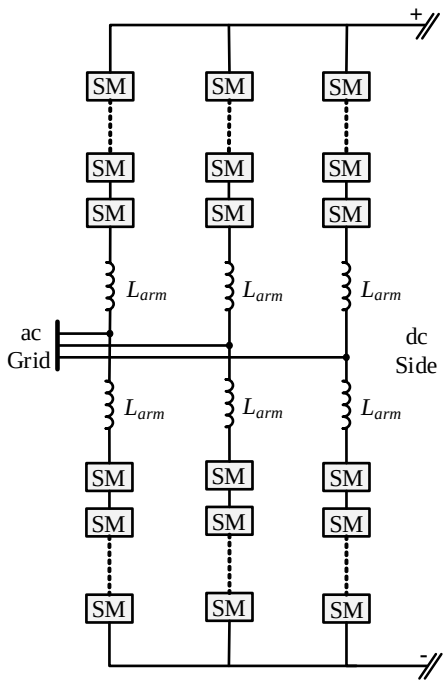


Figure 2.4: The structure of a modular multilevel converter.

semiconductor switches in the converter arms remain as an undesired feature similar to the conventional two-level converters.

In addition to the mentioned drawbacks, the inability of NPC converters in blocking the dc side short circuit fault current makes them unsuitable for application in the future MT-HVdc grids. Figure 2.3 depicts the topology of a three-level NPC converter. As can be seen in the figure, due to the arrangement of the antiparallel diodes of the semiconductor switches, this type of converter is not able to block the dc side short circuit fault current.

2.1.2 *Half-Bridge Modular Multilevel Converter*

The implementation of conventional two-level VSCs for HVdc applications have been done using the series connection of semiconductor switches (e.g. IGBTs). In addition to the dynamic and static voltage balancing issues, the series connection of many semiconductor components might reduce the reliability of system.

The introduction of Modular Multilevel Converter (MMC) with half-bridge submodules was the dawn of a new era in the implementation of high voltage converters for the HVdc and Flexible Alternative Current System (FACTS) applications [40,41]. The MMC offers bidirectional power flow and ac/dc conversation while it maintains the important advantages of cascaded converters in terms of modularity, less harmonic contents and scalability [33].

The adoption of half-bridge MMC within the industry has been quick. Siemens AG was the first company that employed the MMC for HVdc transmission and installed it in the Trans Bay Cable[6] link project in the US in 2010. Currently, most of the recent HVdc projects developed by all major HVdc manufactures are designed based on the variants of half-bridge MMC technology [33]. Some of the important HVdc projects based on MMCs include [25]:

[6] Trans Bay Cable project connects the California cities of Pittsburg and San Francisco using a submarine cable. The dc side voltage of this HVdc link is equal to ±200 kV and has the power transfer capacity of 400 MW. The project has been in operation since November, 2010 [25]

- Tennet Off-shore Wind Farm Complex[7]
- South-west link[8]
- Dalian City Infeed[9]
- France-Spain Electrical Interconnection[10]
- Zhoushan Multi-terminal dc Interconnection[11]

The half-bridge MMC employs two IGBTs in each submodule, which make its application attractive from the power losses and implementation cost points of view [42]. The structure of a modular multilevel converter is shown in Figure 2.4. Depending on its submodules, the MMC can be classified as half-bride, full-bridge or other modified topologies [25,28]. Figure 2.5 depicts the half-bridge MMC behavior under dc short circuit fault. After the fault current reaches specific threshold, the IGBTs are blocked and the antiparallel diodes will conduct the current. In this stage, the half-bridge MMC can be represented by a six-pulse diode bridge with additional arm inductances [43,44]. Due to the contribution of the adjacent transmission lines in MT-HVdc networks, the dc fault current can rapidly increase. The rate of rise of fault current in MMC based dc grids is lower than the networks based on the two-level converters. MMCs have bulky arm inductors, which limit the rate of rise of current during the fault condition. Furthermore, the dc bus capacitors of the MMC based systems are smaller than the two-level based systems. Thus, the initial capacitor contribution into the fault current is not as critical as it is in the two-level based MT-HVdc grid [45].

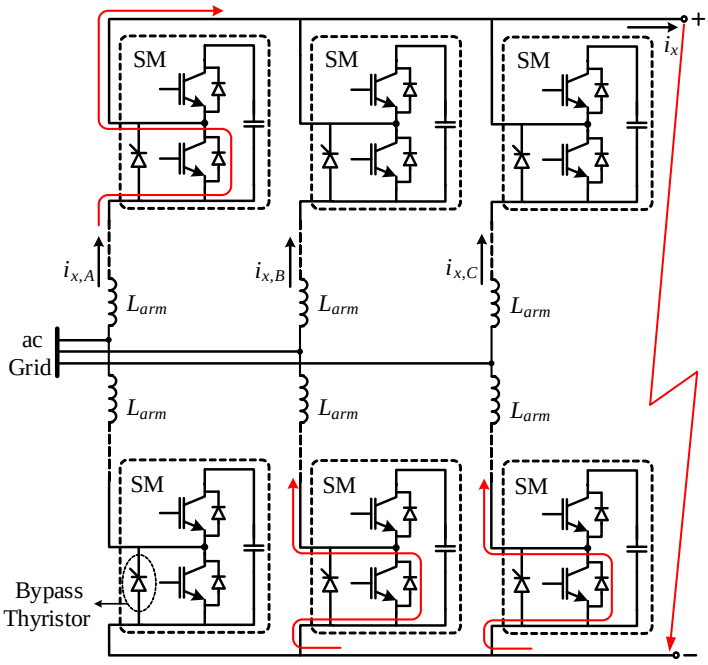


Figure 2.5: Half-bridge MMC under dc pole-to-pole short circuit fault.

The half-bridge MMC cannot block the dc side short circuit current. However, its control during the fault condition can influence how much energy is discharged into the fault [46]. The impact of control

[7] This wind farm complex is located in the North Sea, near to the German coast. It is composed of several wind parks with different transmission technologies and commissioned by different providers.

[8] This project interconnects the Barveryd and Hurva cities in Sweden with an MMC based HVdc system. The transmission distance is 250 km and the power is 1440 MW.

[9] This project feeds the city center of Dalian in China by underground dc cables. The project was commissioned by CEPRI for transmission of 1000 MW over 43 km by using a ±320 kV cable.

[10] This HVdc link interconnects Spain and France using underground cables. The distance is equal to 65 km is under construction. The project has two dc links, each transmitting 1000 MW and operating at ±320 kV.

[11] In this project, a group of small islands near the coast region south of Shanghai, China, are interconnected by an MMC based HVdc, creating a multi-terminal connection. The voltage of this dc link is ±200 kV and the total power is 400 MW.

of half-bridge based MMC on different fault stages is investigated in [47]. To protect the antiparallel diodes of the half-bridge MMC additional components might be required. These components include high current thyristors and metallic contacts. Each submodule can be equipped by one or two bypass thyristors [48], which can be connected in parallel with the submodule. After blocking the semiconductor switches in fault condition the bypass thyristor of each submodule, which is illustrated in Figure 2.5 must be triggered [49]. An alternative approach has been proposed in [50] where additional thyristor branches are attached between the as grid and the half-bridge MMC. The mentioned method is shown in Figure 2.6. By firing the thyristor branches, a large portion of fault current flowing from the ac grid is redirected into the thyristors and hence the antiparallel diodes of the MMC carry a negligible amount of current during the fault condition [50].

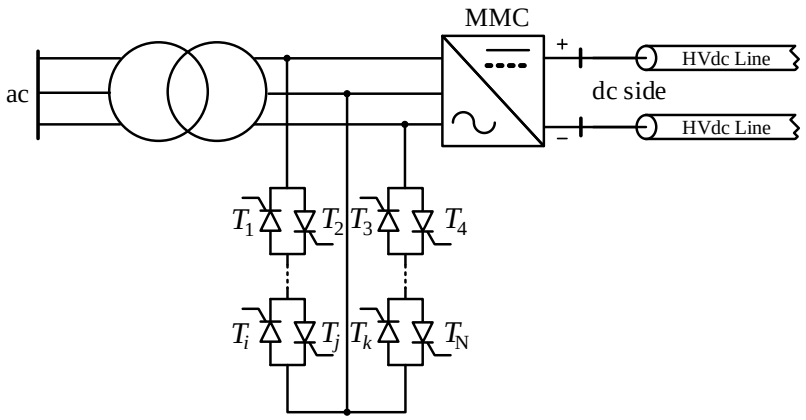


Figure 2.6: Protection of half-bridge MMC using external thyristor branches [50].

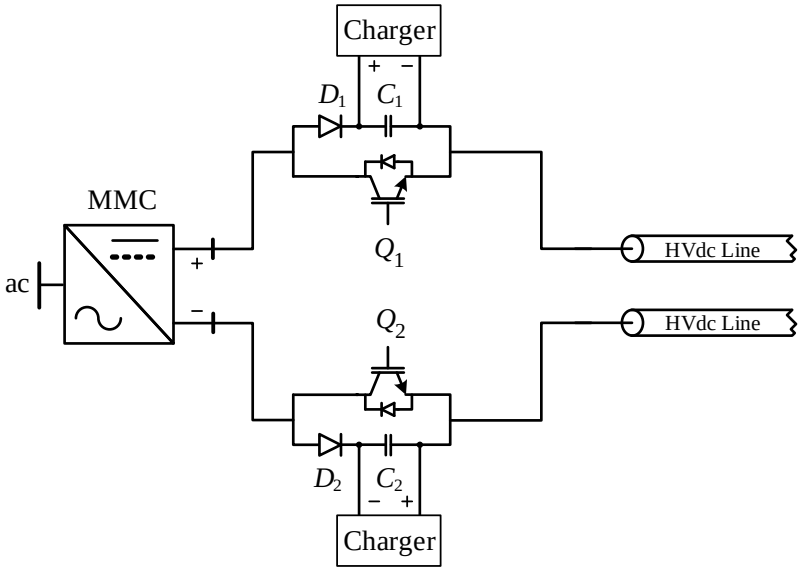


Figure 2.7: Protection of half-bridge MMC using external pre-charged capacitors [51].

As another protective method, the attachment of pre-charged ca-

pacitors to the dc poles of the half-bridge MMC has been investigated in [51,52]. Figure 2.7 depicts the schematic structure of the mentioned method. The capacitors are required to be charged up to $\frac{\sqrt{3}V_{dc}}{4}$ where V_{dc} represents the dc link voltage. In case of a dc side fault the mentioned capacitors must be inserted into the current path to oppose the grid voltage [51,52].

2.1.3 Fault Tolerant Power Converters

Due to the inability of half-bridge MMC in blocking the dc fault current, different topologies with fault blocking capability have been investigated. The most famous topology is called full-bridge based MMC [25,28]. A full-bridge submodule is shown in Figure 2.8.

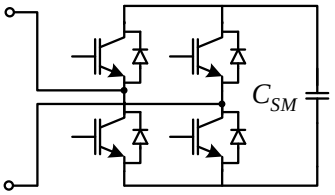


Figure 2.8: A full-bridge submodule for MMC application.

Despite the half-bridge submodule, the full-bridge one has four semiconductor switches. The full-bridge submodules can be connected in series to form one leg of the MMC. The dc side short-circuit fault reduces the full-bridge MMC dc bus voltage, but the submodule capacitors do not discharge completely. Therefore, the full-bridge MMC remains operational and can produce positive and negative voltage. In its simplest form, the IGBTs can be blocked to stop the flow of dc fault current. Since the submodules can control the current, the antiparallel diodes do not need to be protected against overcurrent [53,54].

Due to the disadvantages associated with the full-bridge MMC including higher power losses and higher number of IGBTs as compared to the half-bridge MMC, other topologies have also been proposed in the literature. A clamped double-cell topology is shown in Figure 2.9. This topology is realized by adding an extra switch into the half-bridge cell. Under normal condition extra switch is always conducting and the operation of submodule is similar to the half-bridge MMC operation. Upon occurrence of a dc fault, extra switch will be blocked and the operation of submodule will change to a full-bridge operation [55].

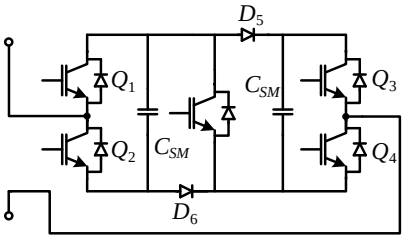


Figure 2.9: Clamped-Double-Submodule configuration for MMC application.

[12] This topology is also known as series connected double submodule [56].

Figure 2.10 shows a cross connected double submodule[12] [57]. This submodule is resulted from connection of two typical half-bridge cells using a diode, a semiconductor switch and its antiparallel diode. The arrangement of semiconductor switches and the antiparallel diodes can redirect the fault current into the submodule capacitors when the switches are blocked. Therefore, upon occurrence of a dc side fault the active power provided by converter falls to zero while the reactive power can be supplied to the ac grid [56,57].

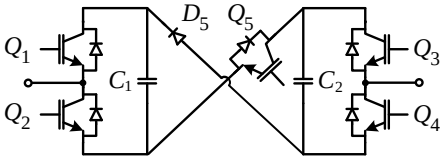


Figure 2.10: Three-level cross-connected submodule.

A new mixed commutation cell structure can be created by combining the half-bridge and full-bridge cells as shown in Figure 2.11(a) [27,58]. The mixed commutation submodule offers the benefits of both basic submodules. The mixed commutation submodule can generate four voltage levels at its output varying from $-V_C$ to $+2V_C$ [27]. This submodule is a fault tolerant submodule since it employs a full-bridge cell in the current path. An asymmetric commutation submodule is depicted in Figure 2.11(b) [27,58]. This submodule

can generate four voltage levels at its output similar to the previous case. The asymmetric commutation submodule can block the dc fault current.

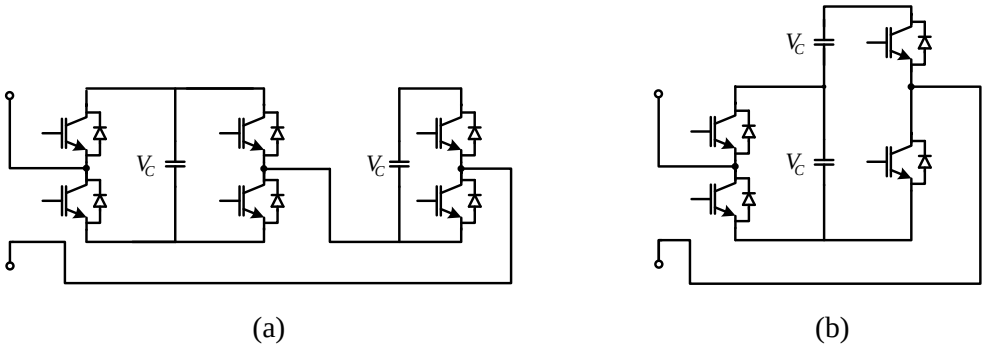


Figure 2.11: Mixed commutation cell structures [27,58].

Figure 2.12 depicts a submodule resulted from parallel connection of two full-bridge cells. The capacitors' voltage ripple can be reduced by connecting the cell capacitors in parallel. The parallel connection of the full-bridge cells can also decrease the current rating of the required components [27]. This submodule is a fault tolerant submodule.

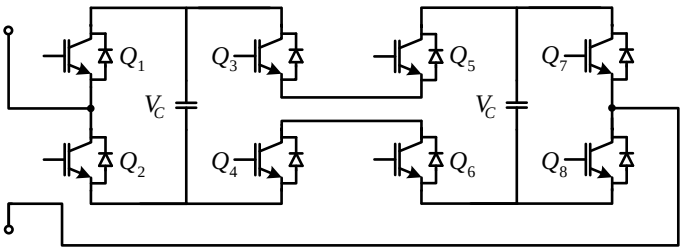


Figure 2.12: Parallel connected full-bridge cells [27].

A cross connected submodule is shown in Figure 2.13. This submodule topology is able to block the fault current and also can generate five voltage levels varying from $-2V_C$ to $+2V_C$. By connecting more intermediate capacitors in this structure higher number of voltage levels can be achieved [59].

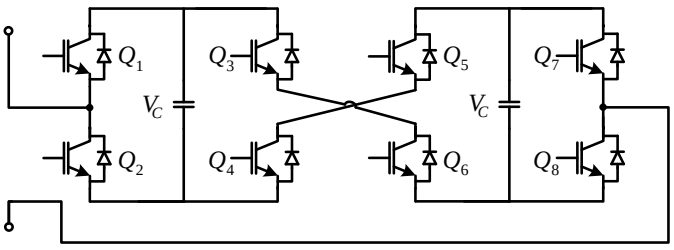


Figure 2.13: Cross connected full-bridge cells [27].

A new cell based MMC for ac/ac and ac/dc applications is proposed in [60]. This topology employs an efficient Packed U-Cell (PUC) structure to create an MMC. As can be seen in Figure 2.14, each PUC submodule is composed of two capacitors and six semiconductor switches and can generate seven voltage levels varying from $-3V_C$ to $+3V_C$. Due to the arrangement of semiconductor switch and their

antiparallel diodes, the PUC submodule is able to block the dc side fault current.

An Alternate-Arm Converter (AAC) has been proposed in [61,62]. The AAC combines the features of conventional two-level converter with the full-bridge based MMC. Figure 2.15 depicts the structure of an ACC. The AAC employs series connection of gate controlled semiconductor switches, which is called director switch [61]. Due to the utilization of full-bridge submodules, the AAC is able to generate larger voltage at its ac side as compared to the dc side voltage. In addition, the AAC is a fault tolerant type VSC. During a dc side short circuit fault the AAC can still be in operation despite the low voltage at the dc link [62]. Even if the dc link voltage drops to zero and the AAC would not be able to inject active power to the grid, it can be operated in the STATCOM mode providing the ac grid with the reactive power support [62].

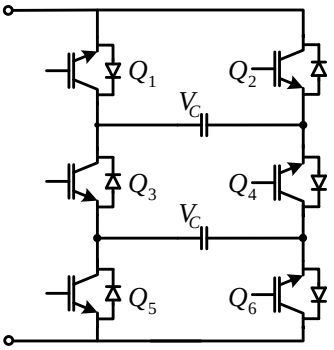


Figure 2.14: Seven-level submodule [60].

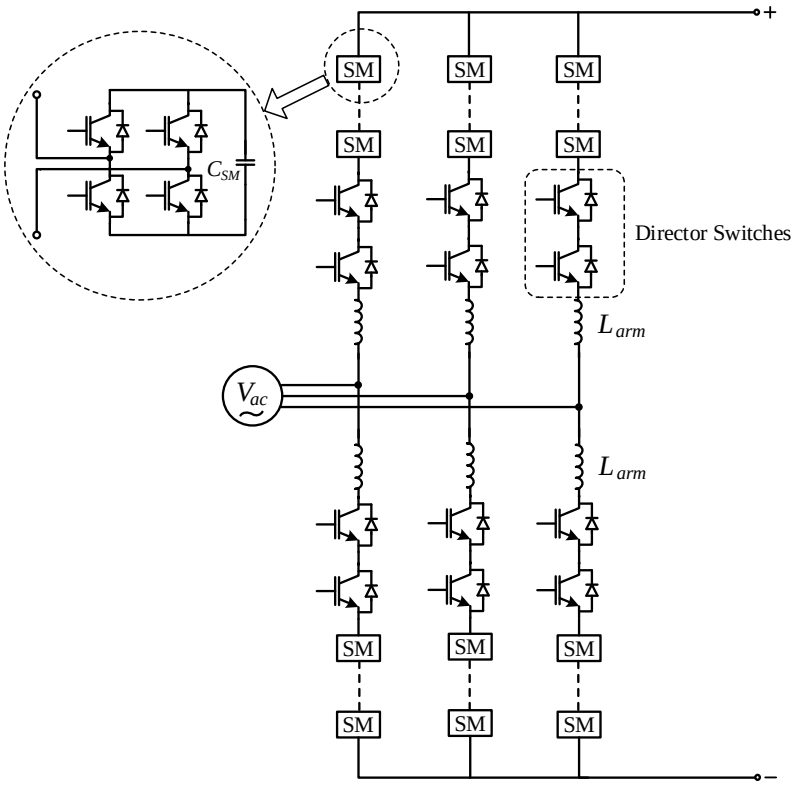


Figure 2.15: The structure of an alternate arm converter (AAC).

A unipolar voltage full-bridge submodule has been proposed and investigated in [57]. Figure 2.16 depicts the structure of this submodule. As can be seen in the figure, the unipolar voltage submodule employs two more diodes and one more semiconductor switch as compared to the typical half-bridge submodule. Upon happening dc side short circuit fault the semiconductor switches should be blocked. Consequently, the fault current will charge the submodule capacitor via the diodes.

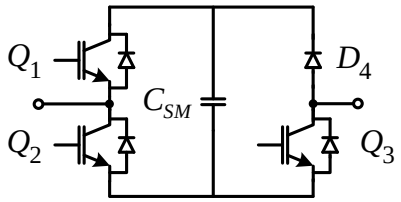


Figure 2.16: Unipolar voltage full-bridge submodule.

2.2 dc Circuit Breakers

The half-bridge based MMC demonstrates significant benefits for the MT-HVdc applications. However, it is vulnerable against dc side short circuit faults. The fault tolerant converter topologies may handle the dc side fault by fully blocking or limiting the flowing fault current. However, the application of most of the fault tolerant topologies requires accepting higher power losses and larger amount of investment on the converter station. This means that, in addition to the greater initial cost of the project, the operational costs also will be larger due to the higher power losses. Furthermore, although the fault tolerant converters may block the dc side fault current, they cannot provide the MT-HVdc grid with a selective fault clearing protection. Particularly, when the number of adjacent transmission lines to a dc terminal in an MT-HVdc grid and the capacity of MT-HVdc grid increase, blocking the converter station for a long time due to a fault on one of the adjacent transmission lines may cause stability issues in both MT-HVdc and ac grids [21].

The half-bridge MMC has been adopted by most of the HVdc vendors [33]. It can be expected that a significant part of the future MT-HVdc grid will employ the half-bridge MMC as the power conversion station. The protection of MMC can rely on the ac side circuit breakers. This approach may sustain the semiconductor components of the MMC by the help of additional thyristors but will not provide the selectivity for protection of the MT-HVdc grid. Moreover, the long operation time of the ac circuit breakers can cause satiability problems in the grid. Hence, additional measures are required to protect the MMC and other MT-HVdc grid components against the high current stress following occurrence of a dc short circuit fault [21,23,24].

The selective protective measures in an MT-HVdc grid include the applications of fault identification methods, dc circuit breakers and dc fault current limiters.

2.2.1 Electromechanical dc Circuit Breakers

The mechanical circuit breakers without auxiliary circuitries cannot be used for interruption of high dc currents because the arc will be drawn between the metallic contacts of the circuit breaker and it cannot be quenched [24]. The research on Electro-Mechanical dc Circuit Breakers (MCBs) for HVdc applications can be traced back to 70s. The main theory of dc current interruption using the mechanical circuit breakers is based on creating artificial zero crossing point in the fault current [63]. The artificial zero crossing point in the fault current can be achieved by use of either active or passive commutation path in parallel with the MCB.

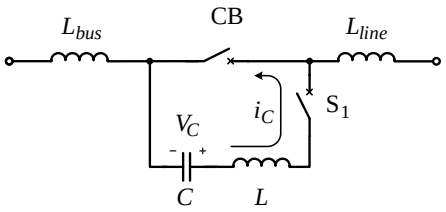


Figure 2.17: Electromechanical dc circuit breaker with pre-charged capacitor [63].

Figure 2.17 shows the configuration of a traditional MCB for HVdc applications. An auxiliary circuit composed of a capacitor, an inductor and a switch (S_1) is attached in parallel to the circuit breaker (CB). The capacitor is a pre-charged capacitor and hence this scheme is an active

commutation scheme. In case that the capacitor is not pre-charged, the scheme can be considered as a passive commutation scheme. During the normal conditions, the CB is closed and S_1 is opened. Hence the current flows through the CB. Upon occurrence of a fault, the CB should be opened to draw the arc between its contacts and S_1 must be closed. By closing S_1, a counter-current will flow through the CB and will create a zero crossing point in the fault current. The magnitude of counter-current depend upon the capacitor voltage and the surge impedance of discharge path (, which is equal to $\sqrt{\frac{L}{C}}$) [63]. The values of inductor and the capacitor in the active commutation MCB can be optimally selected to enhance the performance of the MCB [64]. A load MCB using non-linear resistors and commutation switches in the parallel branch has been proposed in [65]. The proposed load MCB aims to reduce the implementation cost of the HVdc circuit breakers by considering the requirements for load current interruption [65]. Saturable reactors can be employed in the structure of MCB when the active current injection method is used. By applying saturable reactors, it is possible to minimize the sizes of capacitor and inductor of the active resonant circuit and hence reducing the size of whole MCB and consequently decrease the implementation cost [66].

In [67], the application of Crossed Field Interrupt (CFI) tubes in MCB design has been investigated. The proposed MCB can interrupt the fault current faster as compared to the previously proposed MCBs. The configuration of mentioned MCB is depicted in Figure 2.18. The field tests of the proposed MCB shows that the interruption time of this circuit breaker would be around 60 ms. [68,69]. The oscillation frequency of discharging counter-current can reach a few tens of kilo hertz [63]. It means that the zero crossing point in the fault current may reach in 5-10 ms. However, the main drawback in the fast interruption of dc current using MCBs is the delay in opening of the metallic contacts. The metallic contacts may require almost 50 ms to reach the required distance to prevent the arc re-ignition after quenching [70]. The interruption speed of conventional MCB has been improved using fast hydraulic actuators, four SF_6 interrupters and four vacuum interrupters (VIs). The fast hydraulic actuators has a travel velocity equal to 400 in/s, which can reach the distance of 4 cm in almost 4 ms [70].

The main requirements for the MCB in HVdc applications include high $\frac{di}{dt}$ and high $\frac{dv}{dt}$ capabilities. Furthermore, the MCB must be able to withstand under Transient Recovery Voltage (TRV) after current interruption [71]. The performances of gas and vacuum interrupters have been compared based on the aforementioned requirements and the vacuum interrupter was suggested for HVdc applications [72]. An MCB configuration using trigger gap and pulse transformer with shunt arrangement of surge arresters is shown in Figure 2.19 [72]. This MCB uses a pre-charged capacitor in series with the trigger gap. The surge arresters are connected to the ground via switch S_1. Similar concept has been employed for the development of a prototype in the scales of 250 kV and 1.2 kA in [73]. As shown in Figure 2.20,

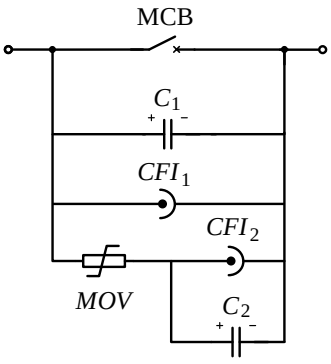


Figure 2.18: Crossed field interrupt tubes based MCB for HVdc applications [67].

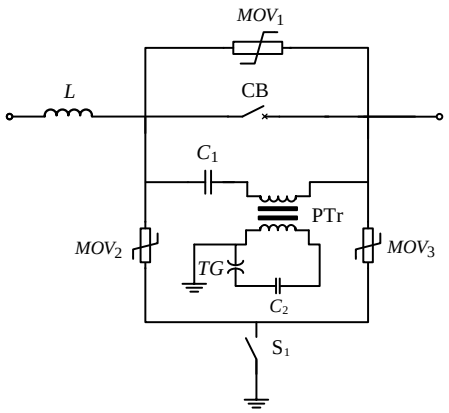


Figure 2.19: MCB for HVdc applications using trigger gap and pulse transformer [72].

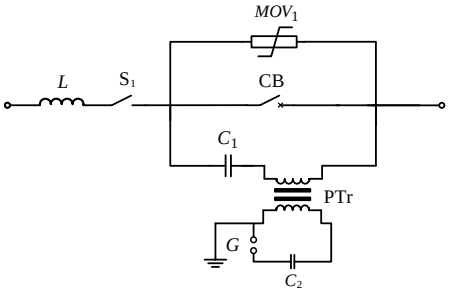


Figure 2.20: MCB for HVdc applications using trigger gap and pulse transformer with parallel surge arrester [73].

Figure 2.22: The configuration of 500 kV airblast HVdc circuit breaker [76].

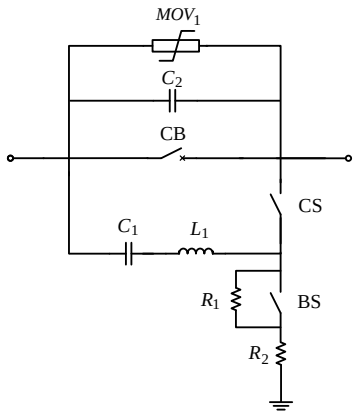


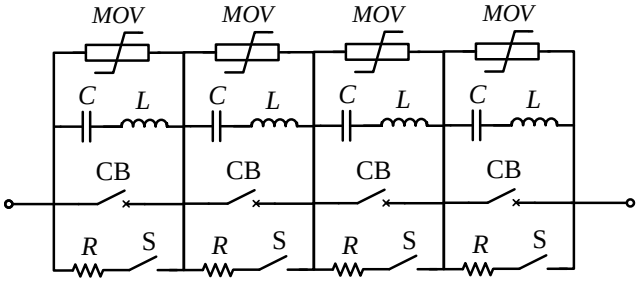
Figure 2.21: The configuration of developed prototype for the interruption of 8 kA at 250 kV [75].

[13] The Pacific dc Intertie (also called Path 65) transmits electric power from the Pacific Northwest to the Los Angeles area. This project was completed in 1970. The dc side voltage is equal to ±500 kV and the transmission line is an overhead line based on ACSR conductors. The distance between two converters id 1362 km.

the developed prototype uses a different arrangement for the surge arrester branch. Another prototype based on the vacuum interrupter has been developed and tested for the interruption of 10 kA at 3.3 kV [74].

A prototype has been developed and tested for the interruption of 8 kA at 250 kV aiming to address the demand for development of dcCBs for the MT-HVdc applications [75]. The configuration of developed prototype is shown in Figure 2.21. The developed prototype uses the basic principles of MCB design for dc current interruption. The capacitor C can be charged through Closing Switch (CS), R_1 and R_2. The Bypass Switch (BS) will be closed at the final charging stage of the capacitor in order to decrease the charging resistance value by bypassing R_1.

The airblast breakers units can also be employed in the development of dcCBs [76]. A prototype using four airblast breakers as the main interrupter units has been developed and tested at the scales of 500 kV and 2 kA. Figure 2.22 depicts the configuration of the developed MCB, which has four interrupters in series connection to withstand under the system voltage and TRV. Each interrupter unit has an LC branch in parallel connection. This MCB uses the passive commutation concept where the capacitors are not pre-charged. The counter-current oscillation frequency can reach 6-7 kHz in this approach [76]. The current interruption capability of the airblast MCB has been upgraded to 4 kA and has been tested successfully [77].



A 500 kV HVdc circuit breaker prototype for switching the load and fault currents up to 2.2 kA has been developed in [78]. Figure 2.23 illustrates the topology of this prototype. The prototype consists of four modules connected in series to meet the voltage requirements. Each module has an SF_6 interrupter, a parallel capacitor, a surge arrester, a closing switch and a resistor. Both the developed prototypes in [76] and [78] have been tested in full scale on the ±400 kV, 1360 km long Pacific dc Intertie[13] in 1985 [79].

A hybrid combination of a mechanical switch, a power charge-storage diode and a surge arrester has been studied in [80]. The structure of this type of MCB is shown in Figure 2.24. In normal condition, the load current flows though the mechanical breaker. The diode should be charged by a high current pulse in forward direction before opening the contacts of the mechanical breaker. Upon opening the metallic contacts the diode provides a short circuit path for the

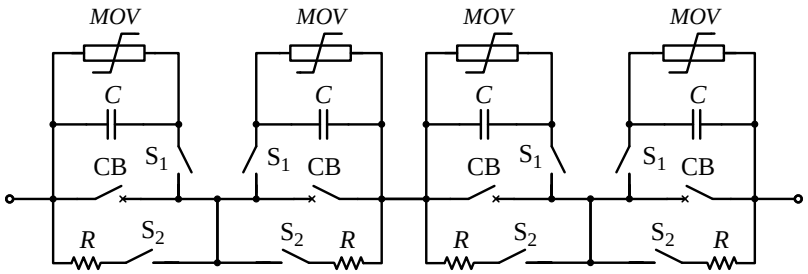


Figure 2.23: The configuration of 500 kV SF_6 based HVdc circuit breaker [78].

fault current in its reverse direction until the charge accumulated in the diode is evacuated [80].

The VI units can be connected in series. Figure 2.25 shows a suggested topology based on the series connection of the VI units. As can be seen in the figure, only one commutation branch in parallel with all VI units is employed [81]. Similar topology has also been investigated in [82]. As an alternative approach, the series connection of a vacuum interrupter unit and an SF_6 interrupter unit has been investigated in [83]. Figure 2.26 shows the proposed topology, which has voltage dividing resistors, LC branch and capacitor charging circuit [83]. The insulation characteristics and arc characteristics of SF_6 and vacuum interrupters must be coordinated in this topology.

In recent years, the MCB has become attractive again. In addition to the investigation on the modeling of MCBs [84,85], several research activities focus on the reduction of ratings of the required auxiliary components and increasing the interruption speed. An experimental test of MCB based on VI unit and active commutation branch demonstrates the interruption of 5.8 kA at 2 kV in only 2 ms. However, the possibility of achieving similar time performance in high voltage scales is still unclear [86]. Another implementation of MCB demonstrates an interruption time in the order of 8-10 ms for interrupting 5 kA at 100 kV [66]. Optimal design of active commutation branch has been considered in [87] and it has been concluded that the interruption probability can be improved. In addition, the commutation time can be reduced by early triggering of the commutation branch. The reduced commutation time can decrease the contact erosion and hence increase the lifetime of VI unit [87].

A couple of MCBs have been proposed in [88,89] aiming to reduce the rating of required semiconductor components. Figure 2.27 depicts the generic configuration of the prospered MCBs. These MCBs use VI units as the main interrupter and create the counter-current by the help of a power electronic based converter. The converter mainly utilizes a resonant LC circuit and by making the voltage reversal increases the magnitude of generated voltage [89]. Although the suggested scheme can decrease the requirement for high voltage rating semiconductor valves, the discharge process of its capacitor is not clear. This can be an important issue since the capacitor will be charged up to the system nominal voltage after the current inter-

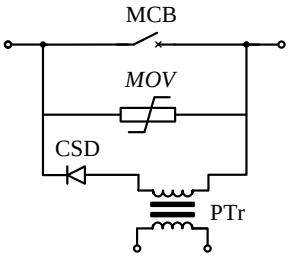


Figure 2.24: The configuration of MCB using power diode in the commutation path [80].

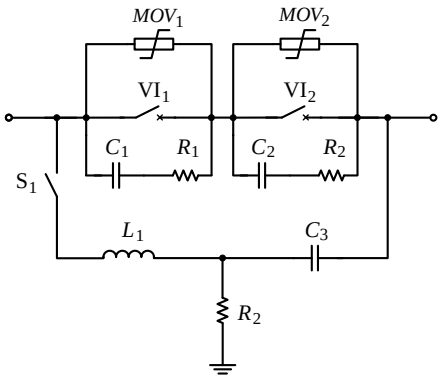


Figure 2.25: The configuration of MCB based on series connection of the vacuum interrupters [81].

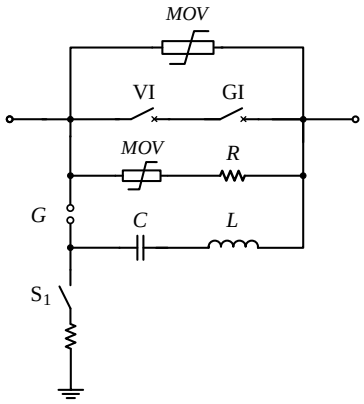


Figure 2.26: The configuration of MCB based on series connection of the vacuum and SF_6 interrupters [83].

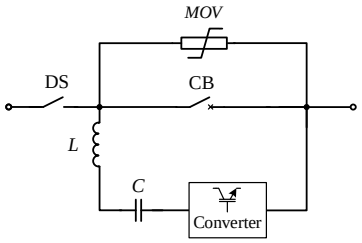


Figure 2.27: The configuration of MCB with reduced rating auxiliary semiconductors [88].

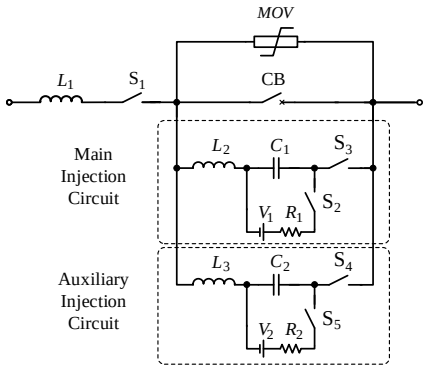


Figure 2.28: The configurations of bidirectional MCBs [91].

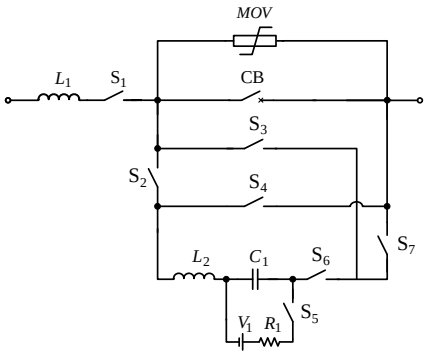


Figure 2.29: The configurations of bidirectional MCBs [91].

[14] In case of load current the $\frac{\mathrm{d}i}{\mathrm{d}t}$ can be close to zero.

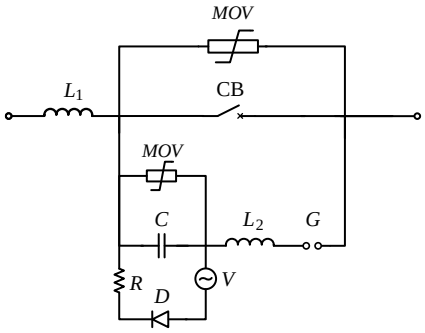


Figure 2.30: Active resonance MCB topology [92].

ruption and hence there might be a need for high voltage valves or switches.

The application of Multiple Series Gaps (MSG) in the design of active resonance circuit has been investigated in [90]. The suggested scheme has voltage-dividing network and self-charging trigger device. The research concluded that the MSG can avoid self-breakdown and also ensure reliable triggering. Moreover, the oscillating circuit can be on standby at any moment and the ground insulation of the oscillating circuit can be fully utilized [90]. The bidirectional current breaking capability of MCBs has been investigated in [91]. A couple of modified MCB topologies have been suggested and studied. Figures 2.28 and 2.29 show two suggested bidirectional MCB topologies.The MCB depicted in Figure 2.28 uses two parallel commutation branch to be able to provide the counter-current in both directions whereas the other topology (see Figure 2.29) employs four switches to define the direction of the injected current.

An active resonance MCB topology has been suggested and prototyped in [92,93]. The prototype has been tested for interruption of currents of 16 kA, 5 kA and 0.5 kA. The interruption of currents of 16 kA and 5 kA has been done at the first zero crossing point of the fault current whereas for the interruption of 500 A several zero crossing points were required. When the magnitude of flowing current is not high the $\frac{\mathrm{d}i}{\mathrm{d}t}$ at the zero crossing point can exceed the $\frac{\mathrm{d}i}{\mathrm{d}t}$ capability of the VI unit. This is due to the large derivative of discharged inverse current as compared to the $\frac{\mathrm{d}i}{\mathrm{d}t}$ of flowing current which can be very small[14] [92,93]. Therefore, this type of MCB similar to the most of discussed topologies of MCB cannot guarantee the successful interruption of the load current in normal or over current fault conditions.

2.2.2 *Solid-state dc Circuit Breakers*

Typical solid-state dc Circuit Breakers

The pure Solid-state dc Circuit Breakers (SSCBs) employ the semiconductor switches for load current conduction and fault current interruption [94]. The simplest topology of an SSCB is depicted in Figure 2.31. A typical SSCB utilizes series connection of gate controlled semiconductor switches in its main current path. The switches can be selected among different Insulated Gate Bipolar Transistors (IGBTs) [95] or Integrated Gate Commutated Thyristors (IGCTs) [96] or Gate Turn-Off Thyristors (GTOs). Upon receiving a trip command the semiconductor switches should be opened. Opening the semiconductor switches redirects the flowing current into the surge arrester branch [94]. Following the current interruption, the voltage across the SSCB increases until it is clamped by the surge arrester branch. The surge arrester absorbs the stored energy in the inductive elements of the system [97]. The voltage rating of the main breaker unit of SSCB must be designed according to the TRV of SSCB, which can be defined by the Over Voltage Protection (OVP) of the surge arrester

[24,94,97]. Typically, a safety margin around 20 % is desirable to be considered in the design of main breaker [95]. Due to the fast turn off characteristics of most of the gate controlled semiconductor switches, the current interruption time of a typical SSCB can be in order of a few tens of micro seconds [24]. Equal dynamic and static voltage devision across the series connected switches can be achieved using snubber circuits [95,96,98]. However, the mismatch in the actual values of the components of snubber circuit may cause dynamic voltage unbalance. This issue can be solved by employing active driving signal adjustment techniques [99].

The surge arrester branch can be connected in series with a diode stack and placed in shunt connection with the load side of the main breaker unit [97,100]. This topology is shown in Figure 2.32. In this case the surge arrester should have a lower OVP level as compared to the typical SSCB. During the fault current interruption the voltage at the cathode of the freewheeling diode becomes negative and after reaching the OVP level of the surge arrester the current will flow though the shunt branch [97].

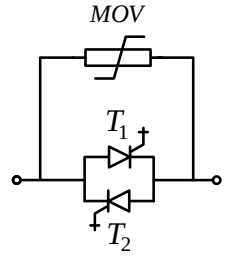


Figure 2.31: The configuration of a typical solid-sate dc circuit breaker.

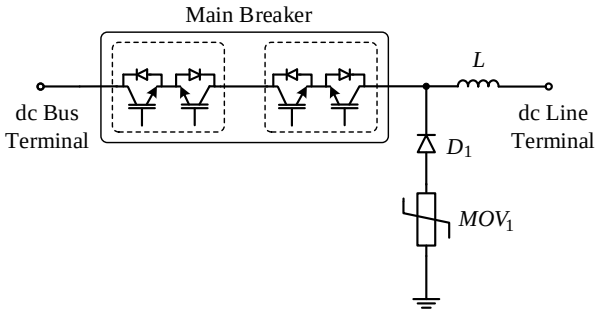


Figure 2.32: The configuration of a solid-sate dc circuit breaker with freewheeling diode.

Figure 2.33 shows a topology of SSCB which has been proposed in [101]. This topology aims to eliminate the surge arresters. Therefore, it employs two coupled inductors, a diode and a capacitor in its structure. The suggested topology has not been studied through accurate models.

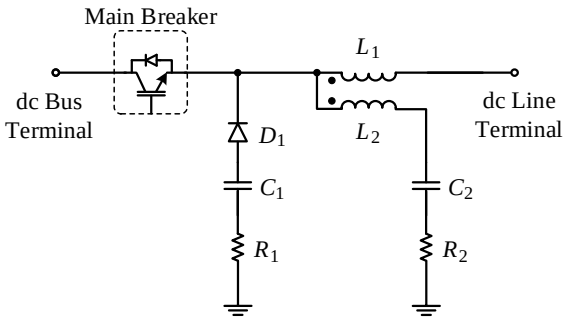


Figure 2.33: The configurations of bidirectional MCBs [101].

The thyristors can be applied in the main breaker unit of the SSCBs [102]. The main issue associated with thyristors is their inability in turning off using the gate signal. Auxiliary circuits can address this problem by providing the required conditions for thyristor commutation. Figure 2.34 depicts a topology of SSCB, which employs thyristors

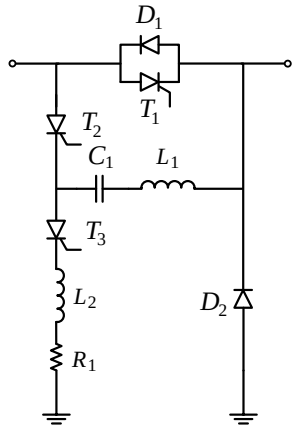


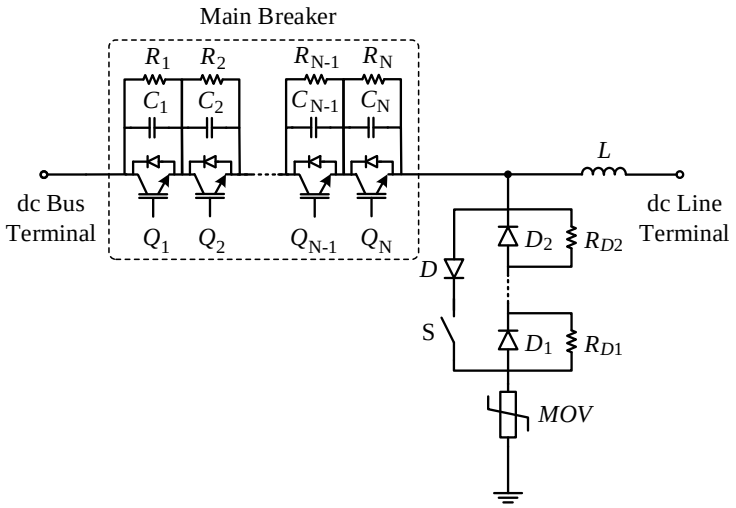
Figure 2.34: Thyristor based solid-state dc circuit breaker [102].

in its main current path. During the normal conditions, T_1 carries the load current. The capacitor C_1 can be charged through L_1, T_3, L_2 and R_1. As soon as receiving a trip command T_2 should be triggered and then the capacitor C_1 will be discharged via the antiparallel diode of the main thyristor. Hence, the voltage across S_1 becomes negative and the thyristor may be turned off. Thereafter, the fault current will flow through the parallel branch including T_2, C_1 and L_1 until the capacitor is charged up to the system nominal voltage [102].

As mentioned earlier, the number of series connected semiconductor switches depends upon the maximum value of TRV which is limited by the OVP level of surge arrester branch. If the TRV of an SSCB could be reduced, the number of series connected switches will be decreases and consequently the conduction losses of the SSCB will become lower. Reducing the TRV level cannot be accomplished by decreasing the OVP level of the surge arrester branch as it can cause additional power losses due to the flowing current through the surge arresters.

A different design of SSCB is shown in Figure 2.35 [97]. This SSCB can be considered as a surge-less SSCB since it does not generate large TRV. In the normal condition, the current flows through the semiconductor switches in the main branch and upon happening of a fault the semiconductor switches must be opened and redirect the current into the parallel snubber capacitors. Thereafter, the voltage at the load side of the SSCB becomes negative due to the effect of inductive elements of the system which oppose the quick change in the current. As soon as this negative voltage reaches the OVP level of the shunt surge arrester, it starts conducting the current and will not allow the voltage at the load side to drop more. The OVP level of the shunt surge arrester defines the maximum level of TRV across the SSCB [97].

Figure 2.35: A surge-less solid-state dc circuit breaker [97].



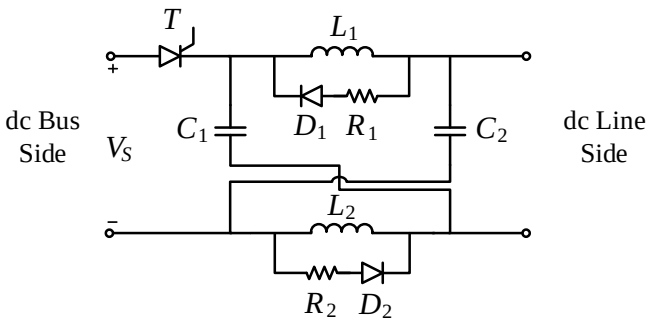


Figure 2.36: Basic topology of z-source solid-state dc circuit breaker [102].

Z-source based dc Circuit Breakers

The forced commutation of main path thyristor requires several full rated components in the auxiliary circuits [103]. This issue can be solved by employing the z-source inverter concept in designing SSCBs for dc applications [104]. Figure 2.36 depicts the topology of a z-source SSCB which has been initially introduced in [105].

The z-source SSCB consists of a thyristor, a crossed LC connection, diodes and resistors [106]. During the normal condition the current flows through the thyristor. When a fault happens at the load side the current increases rapidly. However, the inductors do not allow any quick change in their current. Hence, the fault current will be redirected into the crossed LC branches and the voltage across the thyristor will become negative and the thyristor will be turned off naturally. The z-source SSCBs can be connected in series or in parallel to increase the voltage or current capabilities, respectively [106]. Although the basic topology of z-source SSCB offers a few benefits as compared to the typical SSCBs, a few drawbacks can be listed for this topology as follows:

- The bidirectional power flow cannot be maintained by this topology unless it is modified.
- The z-source SSCB cannot receive a trip command to interrupt the current and it can only interrupt the current when its output is short circuited.
- The z-source SSCB cannot interrupt the load current.
- Although the z-source SSCBs can be connected in series, during a short circuit fault only the most closed z-source SSCB will be turned off. This can increase the voltage across the commutated thyristor while the other z-source SSCBs are not turned off, yet.
- The successful operation of z-source SSCB depends upon the value of rate of rise of the fault current.
- The basic topology of z-source SSCB should be located on both poles of system.

An alternative design of z-source SSCB is shown in Figure 2.37 [107]. As can be seen in the figure, the number of employed components is similar to the basic topology of z-source SSCB. During the

normal condition the load current flows through the thyristor and upon occurrence of a short circuit fault due to the high rate of rise of current the inductors will not allow the fault current to change. Thereafter the current will be redirected into the capacitors and its direction in the thyristor will be reversed. This will turn off the thyristor naturally. In both topologies, the capacitor size is inversely related to the magnitude of fault current and the inductor size. The values of inductor and capacitor should be selected optimally in a trade off with the fault resistance [108].

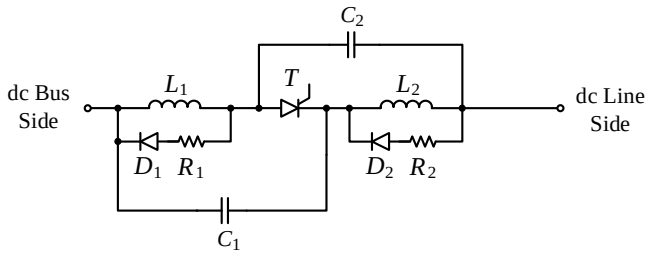


Figure 2.37: Modified z-source solid-state dc circuit breaker [107].

Other modified topologies of z-source SSCBs have been proposed in the literature [109,110]. The bidirectional power flow issue related to the z-source SSCB has been investigated in [111–113]. A topology of bidirectional z-source SSCB with current limiting capability is shown in Figure 2.38. It can be seen from the figure that the number of required components for this approach increases notably and its economic feasibility would be a matter of concern.

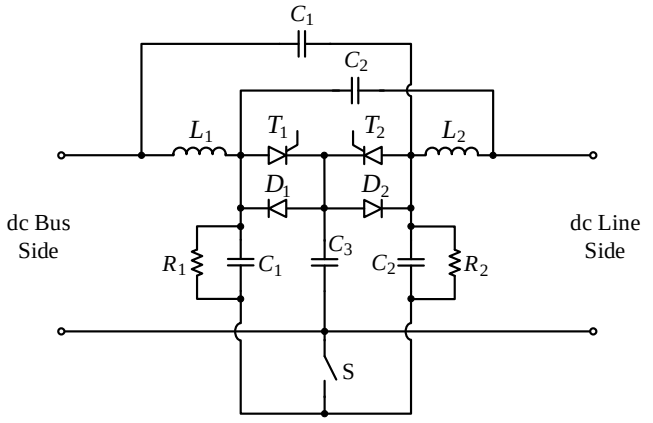


Figure 2.38: Bidirectional z-source solid-state dc circuit breaker [113].

Due to the aforementioned drawbacks of the z-source SSCBs, most of the proposed topologies can be applicable in low or medium voltage dc grids [112,114,115].

Wide Band Gap Switch based dc Circuit Breakers

The main issue regarding the application of SSCBs is related to their high power losses. However, the SSCB can be used as Neutral Bus Switch (NBS) in the HVdc systems. The NBS is not in the main current path but has an important role in dc fault clearing process in the point-to-point VSC-HVdc systems. Normally, the NBS is used to

isolate the neutral bus of a stopped converter from the operating pole after operation of the ac side circuit breaker. The current interruption capability and the time performance of NBS can be improved significantly by employing SSCB as NBS. Therefore, the dc side fault can be isolated even before the completion of the ac side circuit breaker operation [116].

Another approach to decrease the conduction power losses of SSCBs is to replace the silicon based semiconductor switches by the Wide Band Gap (WBG) based power devices [117,118]. The WBG semiconductor switches can be manufactured with higher blocking voltage levels as compared to the typical semiconductor devices. For instance, a 22 kV Silicon Carbide (SiC) p-type Emitter Turn Off (ETO) (p-ETO) thyristor as single switch has been reported [119]. A typical design for WBG based SSCB is proposed in [120]. Similar to the typical SSCB design, the WBG based SSCB should have different levels of internal protection including overload fault, large overcurrent fault and short circuit fault [117]. The external power requirement of WBG based SSCB has been investigated in [121] and a new self-power scheme for normally on SiC Junction Gate Field-Effect Transistor (JFET) based SSCB has been proposed and tested in lab scales. This type of SSCB detects the short circuit fault by sensing the sharp voltage rise between its two terminals and draws power from the fault condition itself to turn and hold off the SiC JFETs. The self-powered SSCB can be directly placed in a circuit branch without requiring any external power supply [121].

dc/dc Converters as dc Circuit Breakers

dc/dc converters can offer voltage step while they can be used to limit or interrupt the dc fault current [122]. Figure 2.39 shows a topology of thyristor based bidirectional dc/dc converter for high power applications. In addition to the voltage stepping, this converter can regulate the power flow and isolate the faulty segment of the MT-HVdc grid without affecting the healthy parts. Due to their lower power losses, the thyristors have been suggested in design of this converter. The thyristors are employed in antiparallel configuration to provide the bidirection power flow [123].

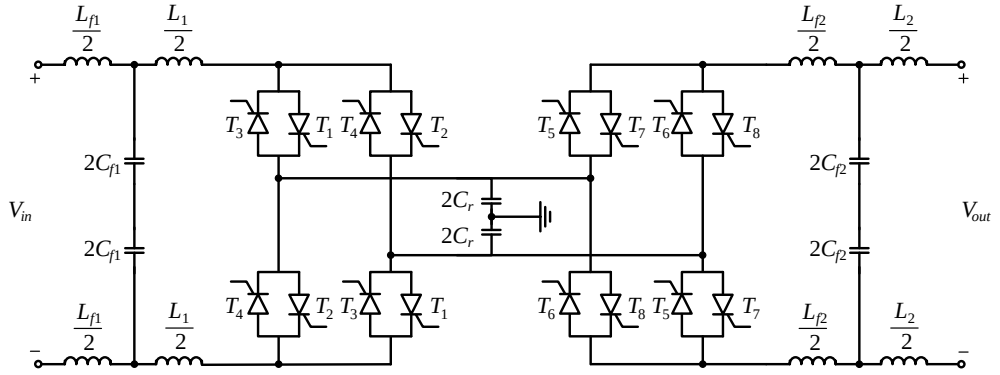
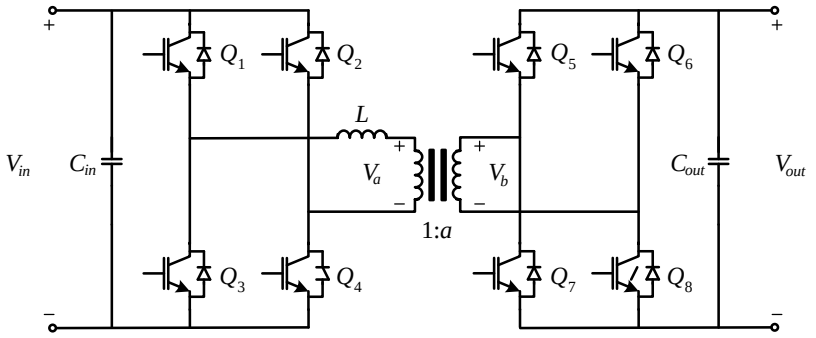


Figure 2.39: Thyristor based bidirectional dc/dc converter for high power applications [123].

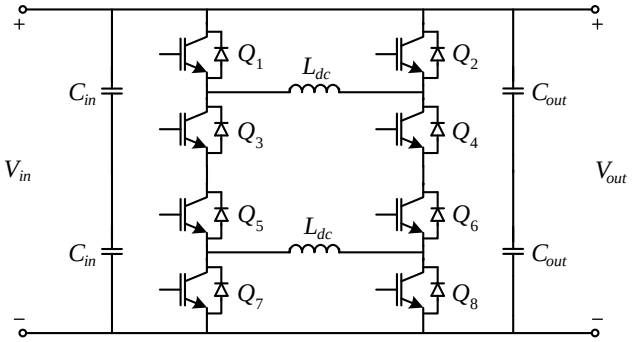
Figure 2.40: Dual active bridge dc/dc converter as dc circuit breaker [124].



The topology of a dual active bridge dc/dc converter is shown in Figure 2.40. The simulation studies show that the dual active bridge converter is able to clear short circuit fault in almost 5 ms.

Figure 2.41 shows a topology of bidirectional dc/dc converter.

Figure 2.41: Bidirectional dc/dc chopper as dc circuit breaker [125].



This converter is able to block the dc short circuit fault and has been suggested for dc microgrid applications [125]. Three dc/dc chopper topologies with reduced number of switches can be derived from the mentioned bidirectional dc/dc converter topology as shown in Figures 2.42, 2.43 and 2.44. These dc/dc choppers are able to block the dc fault current in one direction.

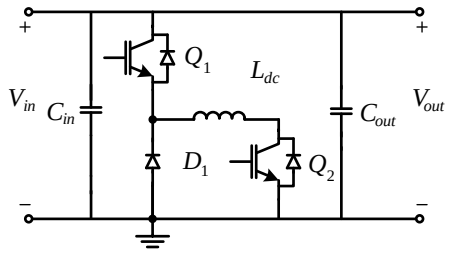


Figure 2.42: A double switch topology of a dc/dc chopper [126].

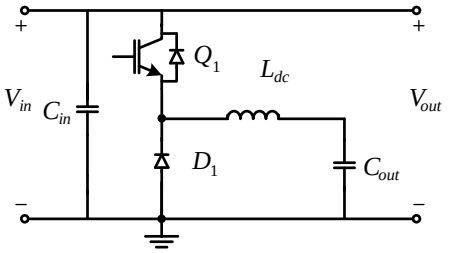


Figure 2.43: A modified double switch topology of a dc/dc chopper [126].

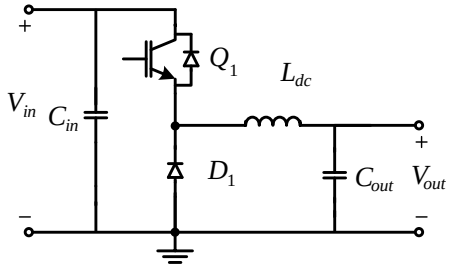


Figure 2.44: Single switch topology of a dc/dc chopper [126].

A topology of unidirectional LLC dc/dc converter is depicted in Figure 2.45 [127]. The switching frequency of this converter can reach 20 kHz. High switching frequency of the converter increase the efficiency of system. The structure of transformer is expected to be complex and special insulation requirements are needed [127].

Coupled Inductor based dc Circuit Breakers

Figure 2.46 shows an SSCB topology which has two coupled inductors. In normal condition the load current flows through the diode and the fast mechanical switch. As the current flowing through the primary side of the coupled inductor is dc current, no current flows through the secondary side. When a short circuit fault occurs, the variation in current of the primary side of the coupled inductor induces a current flowing through the secondary side. When the magnitude of counter-current becomes equal to the current flowing from the source

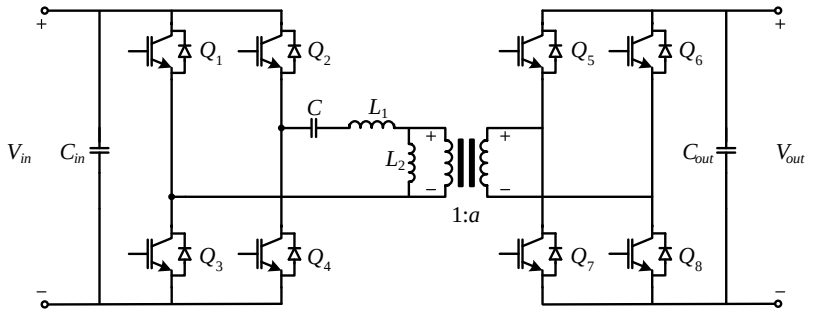


Figure 2.45: Bidirectional dc/dc chopper as dc circuit breaker [127].

side a zero-crossing point is created. The current in the main branch cannot be negative due to the presence of the diode and hence the fast mechanical switch can disconnect without arcing. [128]. However, the main drawback of this SSCB is its inability in providing bidirectional power flow.

The inductors in the z-source converters can be realized as coupled inductors since they carry equal amount of current during the normal condition [129]. The application of coupled inductors in the z-source based SSCB allows a reduction in the inductance by 30% and also a reduction in the inductor volume by about 25%. Moreover, one of the capacitors can be removed thanks to presence of the coupled inductors [129,130]. Figure 2.47 and 2.48 depicts two suggested topologies for z-source SSCB based on coupled inductor. The topology shown in Figure 2.47 has a unidirectional scheme with reduced number of capacitors whereas the topology depicted in Figure 2.48 is a bidirectional SSCB.

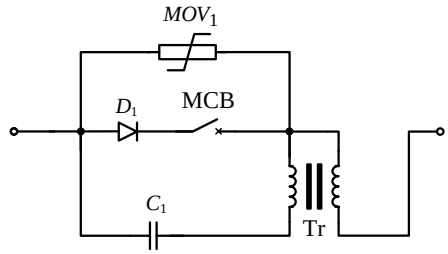


Figure 2.46: The configurations of SSCB based on coupled inductors [128].

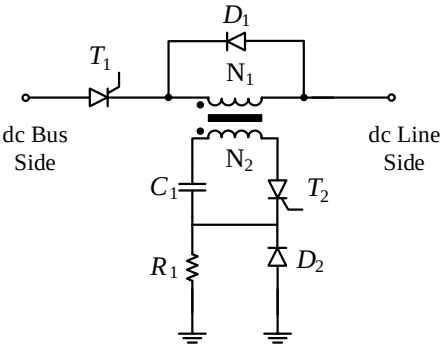


Figure 2.47: A unidirectional SSCB based on coupled inductors [128].

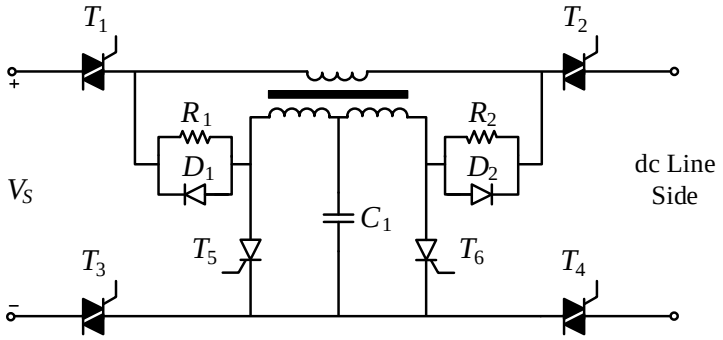


Figure 2.48: A bidirectional SSCB based on coupled inductors [128].

2.2.3 *Hybrid dc Circuit Breakers*

The Hybrid dc Circuit Breakers (HCBs) combine the features of MCBs and SSCBs to achieve low power losses together with the fast interruption performance [24]. Typically, an HCB has a main low losses current path, a semiconductor based main breaker (MB) unit and an energy absorber branch. Note that most of the MCB topologies also consist of a low power losses path (mechanical interrupter unit), parallel semiconductor based path and energy absorber path. However, these topologies cannot be considered as the hybrid topologies

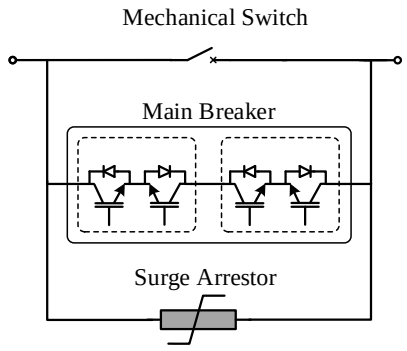


Figure 2.49: The basic topology of hybrid dc circuit breaker [134].

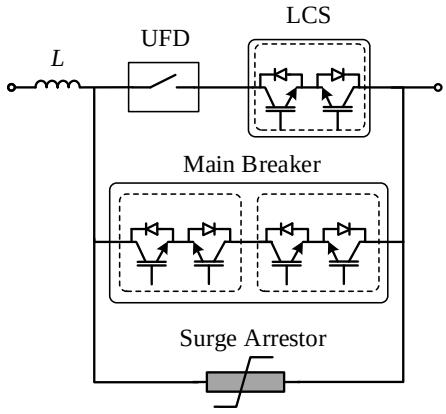


Figure 2.50: The topology of proactive hybrid dc circuit breaker [134].

since the main current interruption is done inside the mechanical interrupter unit. The parallel path does not interrupt the current and typically generates a counter-current to oppose the fault current. The main feature of a hybrid topology is to interrupt the fault current in an auxiliary branch connected to the main conduction branch.

A basic topology of an HCB for dc applications is depicted in Figure 2.49 [131–133].

The load currents flow through the main current path which includes a mechanical interrupter. The parallel path is the MB unit of this breaker and is composed of series connection of IGBTs or IGCTs. The parallel path should be closed prior to opening of the mechanical interrupter to keep the voltage across the mechanical breaker near zero. Therefore, the mechanical interrupter can be opened without arcing and the current will be commutated into the parallel path. Finally, the parallel path will be opened and the current will be redirected into the surge arrester branch. A prototype of this topology has been built and tested by interrupting 1 kA at 600 V [131]. The performance of this topology in medium voltage dc system has been investigated in [135]. The basic HCB topology employing VI unit and SiC based semiconductor switches has been considered in [136]. Another prototype has been tested for interruption of the fault current when it reaches 10 kA at recovery voltage of 1 kV [137].

The main drawback of this topology is the high possibility of commutation failure in the high voltage levels. In high voltage applications hundreds of IGBTs or IGCTs might be required to be connected in series to tolerate the TRV. Hence the voltage drop across the MB unit can be in the order of a few hundreds of volt, which can exceed the arc voltage. When the arc voltage is lower than the voltage drop across the MB unit the current cannot be redirected into the MB unit and commutation failure can happen.

Figure 2.50 depicts an improved hybrid HVdc circuit breaker which was reported in [134]. This HCB is also known as ABB HCB and proactive HCB [134].

The main current path of the proactive HCB consists of a Load Commutation Switch (LCS) unit in series connection with an Ultra-Fast Mechanical Disconnector (UFD). The LCS is responsible to commutate the load current into the parallel semiconductor switch based branch. When the HCB receives a trip command the MB unit must be closed and the LCS should be opened to commutate the current into the MB[15]. After completion of current commutation, whose required time would be in the order of a couple of hundreds of micro seconds [138,139], the UFD can be opened in almost zero current without arcing. The time that required for this stage depends upon the technology of UFD. The operation time of such a disconnector can be assumed as 2 ms [24,134,138–140]. After completely opening of the UFD the MB unit must be opened to interrupt the fault current. The MB unit is composed of fast semiconductor switches as IGBTs or IGCTs. Therefore, the opening time of this branch is quite fast and would be in the order of tens of micro seconds. Thereafter, the

[15] This process can be started even before receiving a trip command when the current starts to increase. The MB unit can be closed whenever a disturbance in the current is detected. Predictive operation may accelerate the current interruption process as it can save whole or a part of time delay caused by UFD unit.

current will be redirected into the surge arrester branch and will be diminished [134].

A prototype of this HCB has been built and tested by ABB. The prototype has successfully interrupted 9 kA at 80 kV. This prototype does not include the UFD unit as it is reported in [134]. The TRV across the MB unit reaches 125 kV for the line voltage of 80 kV [134]. The prototype and the test circuit have been extended to include the UFD unit in [140]. The extended system has been tested under aforementioned conditions and similar results were obtained. The voltage rating of LCS unit is very low as compared to the system rated voltage. For instance, the peak voltage across the LCS unit does not exceed 3.5 kV for a commutation current of 1 kA at 300 kV system voltage. Therefore, the number of series connected semiconductor switches in the LCS unit can be limited to only a few switches [141]. A lab-scale implementation of HCB employing SiC based semiconductor switches and VI unit has been reported in [142].

The integration of proactive HCB to the MT-HVdc grid [143–147], its detail and system level modeling [148–151] and the current commutation process [141,142] have been a research subject in recent years. In addition, a self-powered IGBT gate driver circuit has been proposed for HCB applications in [152].

A different load current commutation approach employing diode, pre-charged capacitor, inductor and thyristor is shown in Figure 2.51 [153]. Upon happening a fault, the thyristor should be triggered. Due to the stored energy in the capacitor an inverse current will flow though the inductor opposing the fault current. This will continue until the flowing current of the mechanical switch falls to zero. By designing the values of capacitor and the inductor the current flowing through the mechanical switch can be kept near zero for a specific time interval due to the presence of diode. When the current in mechanical switch becomes zero, it can be opened without arc. Finally, the MB unit can be opened to interrupt the fault current. This topology can be changed to a bidirectional HCB by employing antiparallel thyristors. However, the control process will be complicated in case of bidirectional HCB [153]. The main drawback of this topology is providing the time required by the mechanical switch for opening the contacts, which can lead to employment of bulky capacitor and inductor.

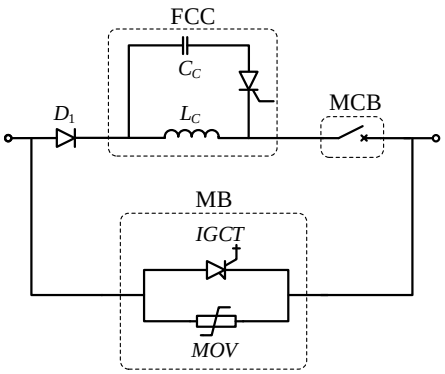
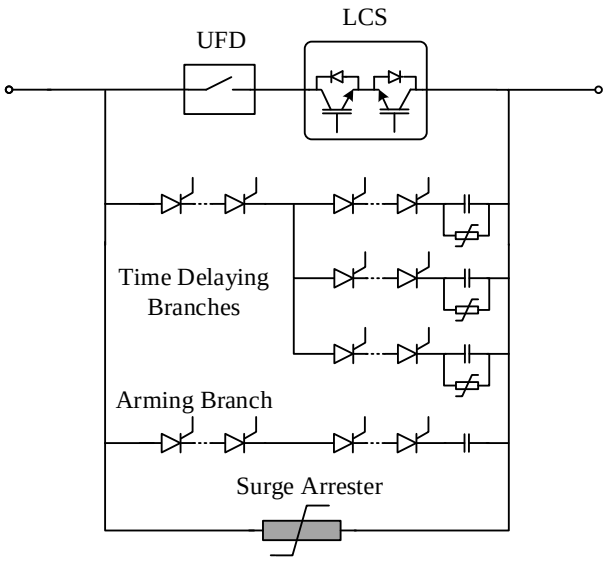


Figure 2.51: The topology of forced commutation hybrid dc circuit breaker [153].

The topology of an HCB proposed by one of the HVdc systems manufacturers namely Alstom is depicted in Figure 2.52 [154]. The main branch of this HCB is similar to that of the proactive HCB. The difference can be observed in the MB unit. As can be seen in Figure 2.52, the MB unit employs thyristors, capacitors and surge arresters. The main role of MB unit is to carry the fault current while the UFD unit is opening. Upon receiving the trip signal, the first delay branch which has a large capacitor should be triggered. Thereafter, the voltage across the capacitor will increase. The capacitors in the delay branches are not high voltage capacitors. When the voltage of capacitor in the first delay branch reaches specific value the second

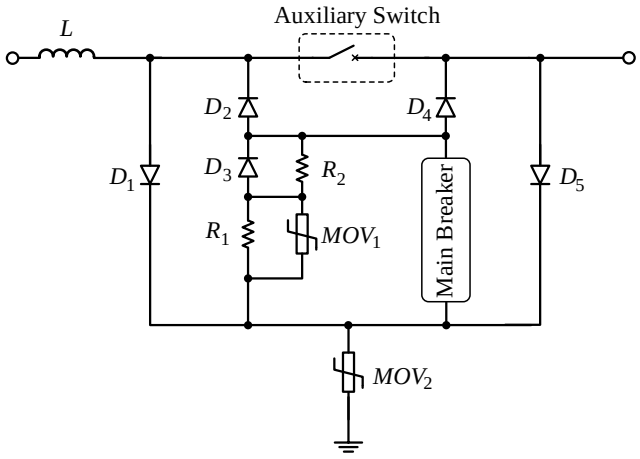
Figure 2.52: The topology of hybrid dc circuit breaker proposed by Alstom Grid [154].



delay branch will be triggered. Finally, after completion of UFD unit operation, the arming branch will be triggered. The arming branch is a full rated branch which will carry the fault current charging its capacitor. Finally, the surge arrester branch will diminish the current. A prototype of this topology has been developed and tested for interruption of 7.5 kA at 120 kV. The TRV across the MB unit reaches 160 kV during the current interruption [154].

Figure 2.53 depicts the configuration of a different HCB [155].

Figure 2.53: The topology of a current injecting hybrid dc circuit breaker [155].



In normal condition, the current flows though the auxiliary branch. As reported in [155], the configuration of auxiliary branch is similar to the structure of main current path in the proactive HCB. Upon receiving a trip command, the main breaker unit should be closed. The current will be shared between the auxiliary branch and the MB unit via diodes D_1 and D_4. Thereafter, the current can be fully commutated into the MB unit by opening the auxiliary branch. After completion of current commutation, the main beaker should be opened. In final stage, the fault current will continue to flow via

R_2, D_3 and D_4 until falling to zero. The converter side current can flow though D_1 and SA_1 until becoming zero. Due to the presence of rectifying diodes, the MB unit can be implemented as a unidirectional SSCB. A different design for the MB unit is shown in Figure 2.54. This MB unit employs additional switches, inductors and capacitors to inject a counter-current in order to interrupt the fault current more effectively. The simulation results show a maximum TRV of 800 kV for a nominal voltage of 500 kV.

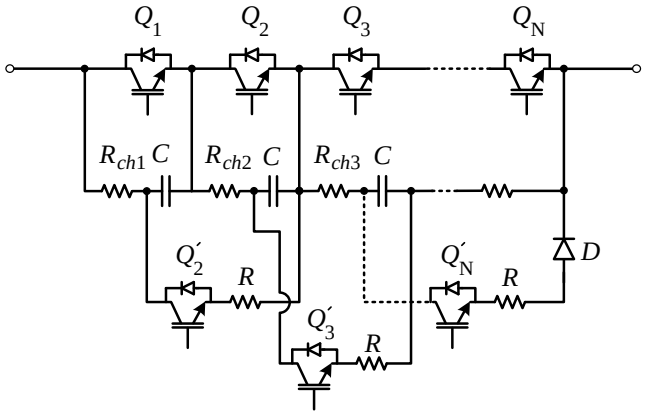


Figure 2.54: The configuration of main breaker unit of current injecting hybrid dc circuit breaker [155].

An alternative design and implementation of HCB using full-bridge submodules in the LCS and MB units has been reported [156]. Figure 2.55 depicts the configuration of full-bridge based HCB. The designed HCB aims to satisfy the protection requirements of Zhoushan five-terminal HVdc project [157]. Experimental test results show successful interruption of 15 kA in less than 3 ms. The TRV across 50 kV cell of this HCB exceeds 75 kV [156]. The current commutation process using the capacitor of full-bridge submodule in the LCS unit is not clear in the report. The employment of full-bridge submodules in the MB unit of HCB can increase the implementation cost significantly. In addition, the discharge process of fully charged capacitors of full-bridge submodules in the MB unit is not clear and it may require additional devices which will be another cause of implementation cost increase.

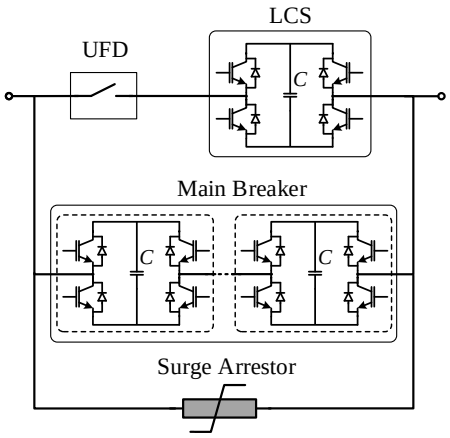


Figure 2.55: The configuration of full-bridge based hybrid dc circuit breaker [156].

A different current commutation circuit for HCB applications has been shown in Figure 2.56. This topology has been implemented and tested for current commutation of 3.4 kA at 44 kV scale. The current commutation can be accomplished in no more than 130 μs [158,159].

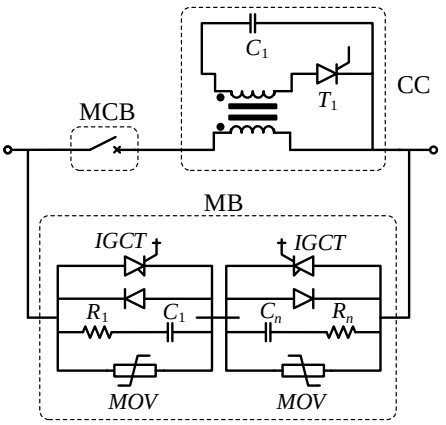
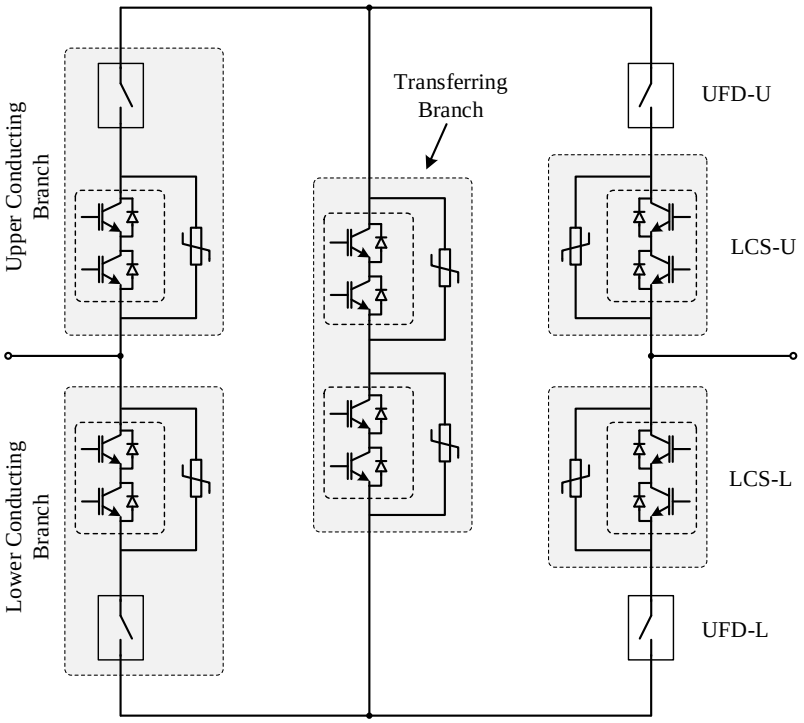


Figure 2.56: The configuration of a hybrid dc circuit breaker with current commutation drive circuit [158,159].

Figure 2.57 depicts the topology of an H-bridge based HCB [160]. This HCB uses a unidirectional MB unit but in fact, it can be operated as a bidirectional HCB due to its H-bridge configuration. During the normal conditions all the UFD units are closed. In addition, the upper LCSs are closed whereas the lower LCSs are opened. The current flows though the upper branches. Upon receiving a trip command, the lower LCS units and the MB unit should be turned on to provide the increasing fault current with an additional path. Thereafter, the upper LCS unit at the fault side should be opened to commutate the current into to MB unit. After completion of UFD unit operation,

Figure 2.57: The configuration of an H-bridge based hybrid dc circuit breaker [160].



the MB unit can interrupt the fault current and the surge arrester branch can absorb the energy [160]. Although this topology employs less number of semiconductor switches in the MB unit as compared to the proactive HCB, it requires two additional UFD units. Due to unavailability of economic data regarding the UFD unit, it is not straightforward to assess the economic superiority of this design over the conventional design.

Another design based on SiC semiconductor switches aiming to reduce the number of gate controlled semiconductor switches in the MB unit of an HCB is shown in Figure 2.58 [161].

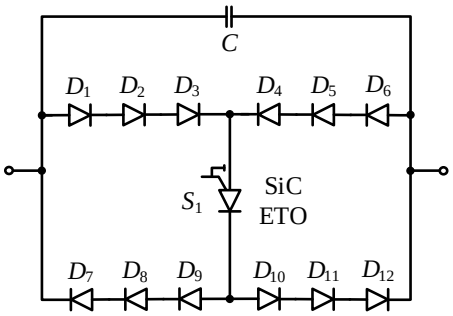


Figure 2.58: The topology of SiC based hybrid dc circuit breaker with unidirectional MB unit [161].

The assembly HCB is a recent proposal for reducing the implementation cost of hybrid current interrupting devices while maintaining its low losses and high interruption speed [162]. Figure 2.59 depicts the topology and configuration of an assembly circuit breaker. The assembly circuit breaker is composed of Active Short Circuit Breaker (ASCB), Accessory Discharging Switch (ADS), MB, UFD and surge arresters. As shown in Figure 2.59, the assembly HCB can be divided in two parts as part A and Part B. Part A can be shared with several HCBs of adjacent transmission lines. Upon receiving a trip command, ASCB and ADS should be closed. These branches will create two artificial short circuit points across the main current branch, which include the UFD ad MB units. Therefore, the voltage across the UFD and LCS units will be close to zero. The MB unit can be opened and then the UFD can be opened. Thereafter, the current in the ADS branch will fall to zero and the thyristors will be turned off naturally. Finally, the ASCB must be opened and interrupt the fault current [162].

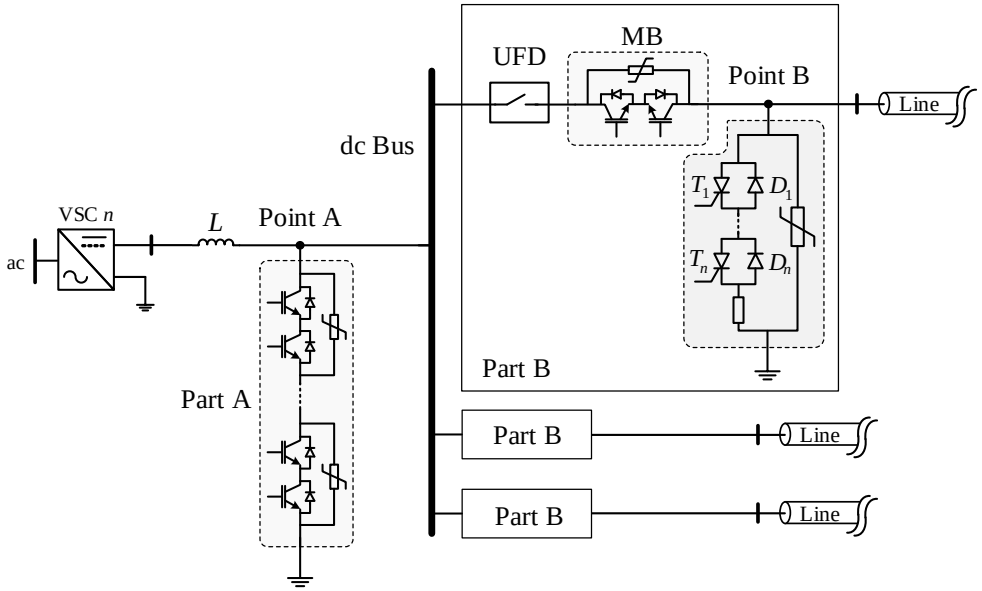


Figure 2.59: The configuration of assembly hybrid dc circuit breaker [162].

A thyristor controlled resistor can be connected in series with the current limiting inductor of the HCB or SSCB in order to reduce the amount of absorbed energy in the surge arresters of dcCB. Figure 2.60 shows the configuration of a VSC system employing the mentioned concept [163].

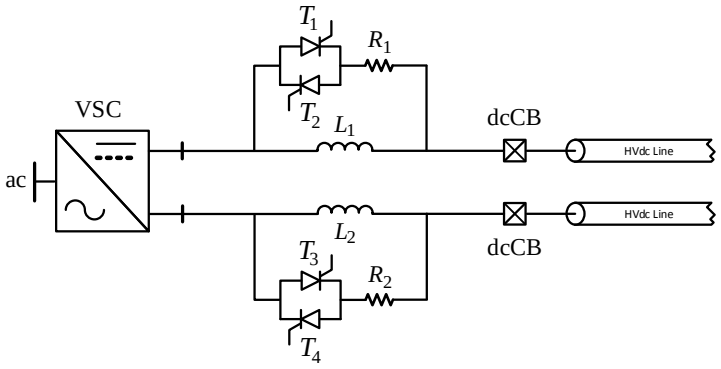


Figure 2.60: The configuration of thyristor controlled resistor in parallel with the current limiting inductor [163].

2.2.4 *Current Limiting dc Circuit Breakers*

Current limiting dc circuit breakers are able to limit maximum of the fault current or its rate of rise. The fault current limiting in low and medium dc voltage levels can be done using semiconductor switch driver action for a very limited period of time [164]. In the high voltage applications the dcCB can be equipped by Fault Current Limiter (FCL) unit. The FCL unit may employ inductive, resistive or superconducting elements to limit the fault current [165–168]. The superconducting FCL (SFCL) units can automatically sense the current rise and limit the fault current. Generally, the SFCLs can be categorized into quench type and non-quench type SFCLs [169].

The dc current limiting characteristics of different types of SFCLs, including dc dual reactor type using the switching operation of High

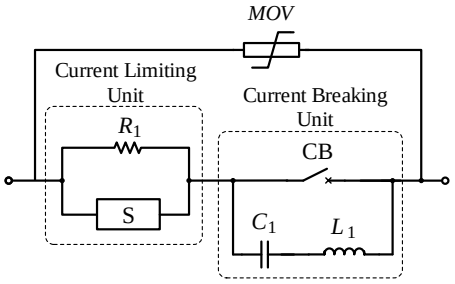


Figure 2.61: The configuration of a current limiting MCB [178].

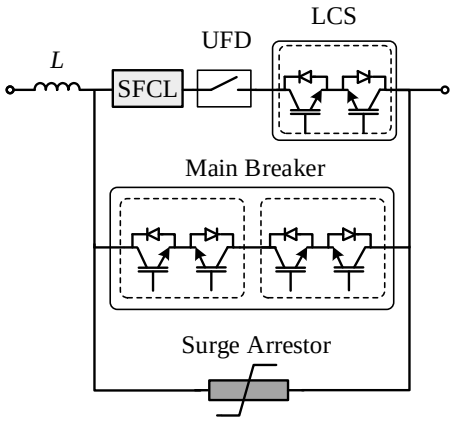


Figure 2.62: The configuration of proactive HCB with SFCL in its main current path [182].

Temperature Superconducting (HTSC) elements [169], dc type SFCL composed of superconducting transformer [170] and dc resistive type SFCL [171] have been discussed in the literature. The application of SFCL in different dc systems, including dc grids protected by slow MCBs [172], point to point VSC-HVdc[173] and MT-HVdc grid based on the two-level converter stations [174] has also been a research topic. A modeling approach for SFCLs applied in HVdc systems has been investigated in [175]. As a resistive type SFCL, Yttrium Barium Copper Oxygen (YBCO)-coated conductor tapes has been identified to be suitable for HVdc applications [169,176].

The SFCL units can be combined with different dcCB topologies [177]. The resistive type SFCL can be connected in series with an MCB unit to reduce the current interruption requirements of GI unit [178,179]. The topology of such combination is shown in Figure 2.61. The experimental test results confirms that the current limiting part containing superconducting tapes and parallel resistance can limit the fault current from 20 to 1 or 2 kA very quickly within 1 ms [180]. The application of SFCL based current limiting MCB in selective protection of MT-HVdc grids has been studied in [181].

Combining SFCL unit with HCB topologies can reduce their required current interruption capability. Figure 2.62 depicts a proactive HCB with an SFCL unit in its main current path [182]. The presence of SFCL can reduce the peak of commutating current and may decrease the current rating of the LCS unit. However, as soon as the MB unit is closed large portion of the fault current will be commutated into the MB unit and the fault current will rise quickly as there is no SFCL in the MB unit path. A feasibility study of this HCB has been carried out in [183]. Simplified model of MT-HVdc grid with the Π-model of HVdc cables have been considered, which may not be sufficient for this type of studies. The MT-HVdc grid protection system time response is considered to be in the order of 20 ms which seems to be far from the time range of the proposed fault identification algorithms in the literature [184].

The impact of SFCL on dc fault current interruption in the MT-HVdc grids employing Continuous Wavelet Transform (CWT) protection method and the proactive HCBs has been studied in [185]. The simulation and analysis results from different modeling approach shows that the SFCL can reduce the current interruption requirement of the HCBs. In addition, the authors suggest a parallel resistance for SFCL to prevent it from experiencing overvoltage and overheat [185].

2.3 Remarks

The modern HVdc circuit breakers can be classified in three main categories including Electro-mechanical dc Circuit Breakers, Solid-state dc Circuit Breakers and the Hybrid dc Circuit Breakers. The MCBs demonstrate low power losses as compared to the other types of dcCBs. However, their main drawbacks can be listed as follows:

- *Current Interruption Time*: The interruption time of MCB depends upon two factors including the time required for opening the contacts and the required time for creating the first zero crossing point in the fault current [87]. The contact opening time can increase as the rated voltage of MCB increases. This is due to the longer distance between the contacts in higher voltage levels. This issue might be addressed by developing faster mechanical parts or employing lower voltage interrupter units in series connection. However, the series connection of interrupter units in HVdc applications might be challenging due to the highly non-linear $V - I$ characteristics of the arc which can cause strong inequality in the voltage across the interpreter units during the current interruption process. The minimum reported current interruption time in the MCBs is in the order of 8-10 ms for interruption of 5 kA at the voltage of 100 kV. However, it is not still clear that if this time performance would be repeatable at higher voltage and current scales e.g. 16 kA, 320 kV.
- *Long Deionization Time*: Deionization time can also be quite long e.g. 300 ms for the MCBs [116]. In the case of temporary fault, the MCB can be reclosed again after deionization time of the fault-arc path. The deionization time depends on many factors such as line voltage, conductor type, atmosphere at fault location, fault current [116]. This means that the reclosing action cannot be done quickly after an interruption action. Although this would be a common issue for almost all types of dcCBs due to the presence of non-linear surge arresters, it can cause a significant delay in MCB based systems.
- *Dependency on* $\frac{\mathrm{d}i}{\mathrm{d}t}$: The successful interruption possibility is highly dependent on the $\frac{\mathrm{d}i}{\mathrm{d}t}$ at the zero crossing point [186]. The high rate of rise of current can happen when MCB interrupts lower current as compared to its rated interruption capability. In this case, the fault current (or load current) has a small magnitude as compared to the counter-current magnitude generated by the auxiliary circuit and hence the rate of rise current at the zero crossing point can be very high.

The rate of rise of fault current in MT-HVdc grids can exceed 6 kA/ms. Considering an interruption time of 8 ms, the prospective fault current can easily reach the maximum short circuit level of the converter station at its dc side. Therefore, the MCB can be applied in protection of MT-HVdc grid if either additional FCL devices or fault tolerant converter topologies are employed.

The SSCBs show a very fast current interruption time performance. The quick current interruption can prevent the fault current from reaching the converter blocking threshold. The protection of MT-HVdc grid by SSCBs can guarantee the full selectivity of protection system without converter station blocking. Since the SSCB can interrupt the fault current in early stage of its propagation, it may contribute to reduce the current rating of converter station and the size of current limiting inductance. However, the high power losses associated with SSCBs is their main application drawback.

The high power losses of SSCB is due to the presence of large number of semiconductor based switches e.g. IGBTs, IGCTs or GTOs. The conduction power losses of SSCB is related to the number of series connected switches. Therefore, the power losses can be decreased by reducing the number of series connected switches.

The number of series connected switches can be halved if the main breaker unit is implemented as a unidirectional current interrupting unit. However, the inability of the unidirectional dcCB in clearing the faults in its backward direction would be a matter of concern.

The number of series connected switches are defined by the maximum TRV across the SSCB. Therefore, if the TRV can be reduced the number of switches can also be decreased. The reduction in the TRV cannot be achieved with decreasing surge arrester units with lower OVP level as it will cause additional high power losses and thermal problems in the normal conduction mode. However, reducing the TRV using auxiliary circuits can lead to promising solutions.

The HCB concept can be the most feasible solution for the fast and selective protection of an MT-HVdc grid. However, its implementation cost seems to be a drawback. Although there is no clear economic estimation available in the literature for HCB (and SSCB), the large number of required semiconductor in the MB unit, large size of surge arresters and the requirement for UFD units show that this type of circuit breaker is the most expensive type as compared to the other technologies.

The interruption time for most of the fast HCBs lies in the range of 2.5-4 ms. During this time range the fault current in MT-HVdc grid can reach 20 kA even in presence of large current limiting inductor. Therefore, the semiconductor switches may also be connected in parallel in addition to their series connection. The reduction in the number of semiconductor switches either by reducing the series connected or parallel connected switches can reduce the total implementation cost.

Part II

Surge-less dc Circuit Breaker & its Application in MT-HVdc

3
Surge-less dc Circuit Breaker

Give me a place to stand, and I shall move the world.

Archimedes of Syracuse, Greek Mathematician, Philosopher, Scientist and Engineer.

As it was explained in Chapter 2, the SSCBs are technically attractive due to their ultra-fast current interruption performance. Moreover, the improvements and the expectation for more advances in the field of high power semiconductor switches and also wide-band gap devices can be listed as the main motivations of research on the SSCBs. Furthermore, the HCBs utilize a solid-state breaker branch to interrupt the fault current and therefore, improvements in the SSCB technology may also improve the performance of HCBs.

While the SSCBs can offer several benefits due to their fast current interruption characteristics, their operation can cause a large magnitude switching surge voltage. The excessive voltage can damage the semiconductor switches of the SSCB at the first step. In addition, this surge voltage may damage the system insulations.

As a typical approach to limit the switching overvoltage, snubber circuits might be attached to individual semiconductor switches. However, due to the large inductive elements of the system and high voltage and current levels the snubber circuits cannot handle the situation. Therefore, non-linear varistor or surge arresters are required to be employed by the SSCBs.

This chapter focuses on a recently proposed surge-less fast SSCB topology, which is called Current Releasing dc Circuit Breaker (CRCB). The CRCB has different operation principles as compared to the typical SSCBs. The chapter will continue by reviewing the surge

This chapter is based on the following publications and patent:

A. Mokhberdoran, A. Carvalho, N. Silva, H. Leite and A. Carrapatoso, "A new topology of fast solid-state HVdc circuit breaker for offshore wind integration applications," *Power Electronics and Applications (EPE'15 ECCE-Europe), 17th European Conference on*, Geneva, 2015, pp. 1-10, doi: http://10.1109/EPE.2015.7309270.

A. Mokhberdoran, A. Carvalho, N. Silva, H. Leite, A. Carrapatoso, "Design and Implementation of Fast Current Releasing DC Circuit Breaker", *Electric Power Systems Research Journal*, Volume 151, October 2017, doi: 10.1016/j.epsr.2017.05.032.

A. Mokhberdoran, N. Silva, A. Carrapatoso, A. Carvalho, H. Leite, "Fault current managing branch for surge-less current interruption in dc system," Patent No. WO2017025927 A1, Filing date Aug 11, 2016, Publication date Feb 16, 2017.

voltage phenomena in SSCBs in section 3.1. The operation principles of CRCB is explained in section 3.2. section 3.3 includes the analysis of the CRCB through an aggregated model. Design remarks are provided in section 3.4 and simulation results through a conceptual design example in section 3.5. Finally, the chapter is concluded in section 3.7 after demonstrating the experimental results from an implemented lab-scale prototype in section 3.6.

3.1 Transient Recovery Voltage

3.1.1 Definition

Figure 3.1 shows a simplified dc power transmission system. The ideal dc voltage source feeds the load through a transmission line, which is modeled by its resistance and inductance. As shown in the figure, there is a circuit breaker between the source and the transmission line. Assume that a short circuit fault occurs at time t_f and connects the point F to the ground. Consequently, the circuit breaker opens at $t = t_{br}$. Also, we assume that the current falls to zero at time t_e.

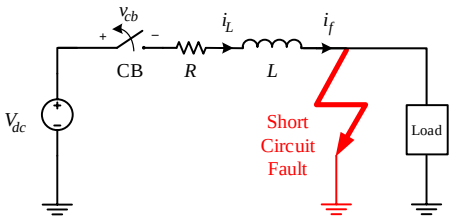


Figure 3.1: dc current interruption.

The voltage across the CB after current interruption instance can be given by:

$$v_{cb}(t) = V_{dc} - L\frac{\mathrm{d}i_f(t)}{\mathrm{d}t} - Ri_f(t), \quad t > t_{br} \tag{3.1}$$

where i_f represents the fault current. Due to the continuous decrease in the fault current after interruption instance the following equation can be given:

$$\frac{\mathrm{d}i_f(t)}{\mathrm{d}t} < 0, \quad t_{br} < t < t_e \tag{3.2}$$

If the resistance of the dc transmission line is neglected[1] [187], it can be found out that the voltage across the CB (v_{cb}) always exceed the value of V_{dc}. This overvoltage is called Transient Interruption Voltage (TIV) or Transient Recovery Voltage (TRV). Based on Equation (3.1), the TIV depends on three parameters:

- The magnitude of dc current at the interruption instance ($i_f(t_{br})$)
- The time in which the current becomes zero ($\mathrm{d}t$)
- The system inductance (L)

In fact, the interruption of larger fault current causes higher overvoltage across the CB. The magnitude of fault current at the interruption instance depends on the fault identification system performance[2] and the inductance between the dc source and the fault location[3]. It can also be understood from Equation (3.1) that the faster circuit breakers are expected to have higher TIV due to small value of $\mathrm{d}t$. The system inductance can increase the overvoltage level. However, in high current systems the limiting impact of system inductance is dominate.

[1] In contrary with the ac lines, dc transmission lines have less resistance. This is due to absence of skin effect in dc transmission lines during the normal conditions. Although the resistance of a real cable or an overhead line is a frequency dependent parameter and can increase during the fault condition, still it can be neglected against $L\frac{\mathrm{d}i_f(t)}{\mathrm{d}t} - Ri_f(t)$.

[2] dc system protection schemes have different response times [184]. The longer fault detection time, the higher fault current magnitude at the interruption instance.

[3] The inductive parts of system limit the fault current derivative and therefore prevent it from reaching high values [188].

3.1.2 Typical Solution

Metal Oxide Varistor

Metal-Oxide Varistors (MOVs) are a kind of surge protective device [189]. MOVs are widely used in the existing power system to damp the system overvoltages. In addition to the surge protective role of

Figure 3.2: Metal oxide elements [192].

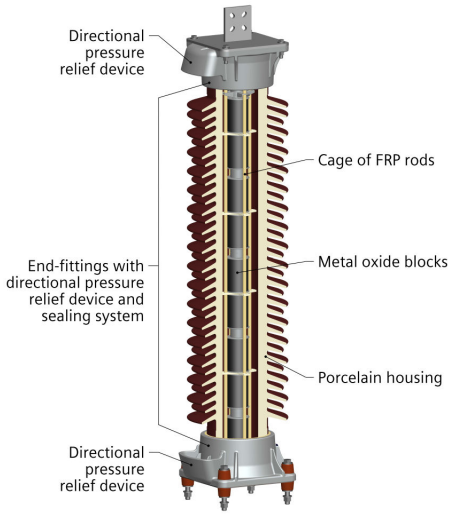


Figure 3.3: A Siemens MOV with porcelain housing [192].

[4] For instance, a pole-to-ground fault in a symmetric monopole MMC-HVdc system can cause transient overvoltage on the cables [195].

[5] In calculation of the equivalent inductance of system, the ac side inductive parts and the converter arm inductors should be considered. The ac side inductors include the transformer short circuit inductance and the coupling ac reactors [188].

MOVs in high-voltage systems, large size MOVs are needed to reduce the system insulation level [190]. A high voltage MOV consists of several individual highly non-linear metal-oxide elements enclosed within a housing [191]. Examples of metal-oxide elements are depicted in Figure 3.2. The available housings include directly molded silicone rubber, silicone housing with a composite hollow core design and the porcelain housings [192,193]. Figure 3.3 shows a the design of a high voltage MOV with porcelain housing.

The material characteristics and the number of metal-oxide elements and their diameter defines the operating voltage and the energy absorption capability of the MOV. The MOV has a very non-linear voltage-current characteristic. The MOV resistance depends on its voltage. Under nominal system voltage almost no current flows through the MOV whereas at higher voltage levels the MOV resistance decreases significantly and allow the current to pass through it [194].

MOVs are also commonly installed in the HVdc systems to protect the transmission lines and the converters stations. The overvoltage in the system may occur due to an external phenomena such as lightning or the system related issues such as switching actions and faults[4]. The surge arresters are typically installed at the ac bus, ac filter and ac filter bus. Furthermore, five groups of surge arresters are installed to protect the dc elements of the HVdc station. The dc side surge arresters include the valve, converter, dc bus, neutral dc bus and dc filter arresters [196–198]. The dc bus arrester group is installed close to the smoothing reactor (L_{sm}) and also close to the dc transmission line connection in order to protect both converter station elements and the dc transmission line insulation against overvoltage coming from the dc side of system.

MOV Application in dc Circuit Breaker

As mentioned in chapter 2 most of the present HVdc circuit breakers utilize the MOVs to limit the TIV. Limiting the circuit breaker TIV demands absorbing the stored energy in the inductive parts of system. Therefore, the circuit breaker's MOV should be rated based on the largest possible released energy during fault current interruption. The stored energy in the inductive parts of system holds:

$$E_{sc}\left(t_{br}\right) = \frac{1}{2} L_{eq} i_f^2\left(t_{br}\right), \tag{3.3}$$

where, L_{eq} represents the equivalent inductance of system at the dc side[5]. $i_f\left(t_{br}\right)$ represents the value of short circuit fault current at the interruption instance. The stored energy in the inductive parts of system depends on two parameters:

- The time period between the fault occurrence instance and the interruption instance $(t_{br} - t_f)$
- The system equivalent inductance (L_{eq})

The magnitude of fault current at the interruption instance ($i_f\,(t_{br})$) depends on the two mentioned factors. The larger inductance between the fault location and the Point of Common Coupling (PCC) can limit the rate of rise of fault current and reduce its value at the interruption instance. The longer fault identification or the longer dcCB operation time can lead to higher current value at the interruption instance. Figure 3.4 depicts a typical SSCB. As explained in chapter 2, the typical SSCB utilizes several semiconductor switches in series connection to withstand under the TIV. Depending on the current capability of the semiconductor switches and also the maximum possible current at the interruption instance the SSCB may possess few parallel semiconductor switch branches. As can be seen in Figure 3.4, L_{cb} is the current limiting inductor of SSCB. An MOV is also attached across the semiconductor branch in order to limit the TIV and preserve the switches from destruction after current interruption.

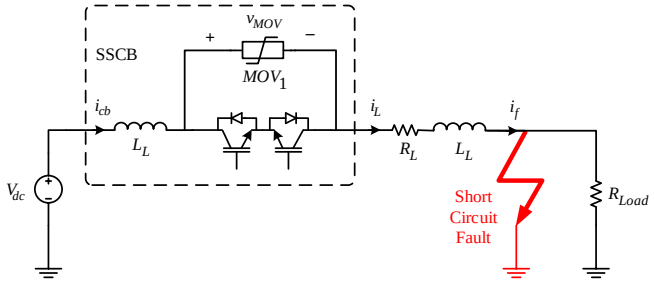


Figure 3.4: MOV application in solid-state dc circuit breaker [196].

Surge arresters have a non-linear voltage-current characteristic. To have a rough estimation, MOV's parameters can be approximated by assuming its voltage to be constant until its current falls to zero. Figure 3.5 illustrates the voltage and current approximation method used for the SAs. It can be seen in Figure 3.5(a) the MOV voltage rises instantaneously up to its rated voltage and remains constant until its current fall to zero (see Figure 3.5(b)). It is also assumed that the surge arrester current reaches its maximum instantaneously and then decreases linearly (see Figure 3.5(b)). V_r represents the OVP of MOV_1.

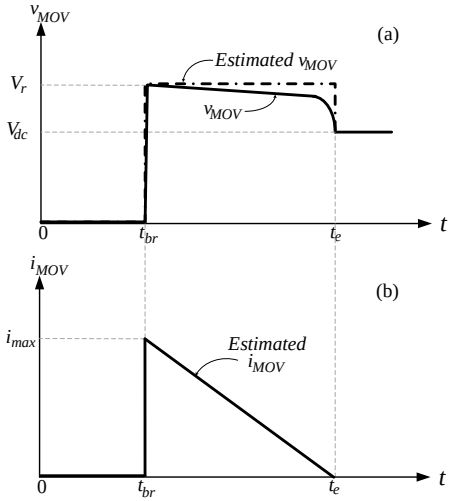


Figure 3.5: Surge arrester approximated current and voltage.

Considering (3.1) and neglecting the transmission line resistance (R_L), the TIV across MOV_1 can be given by:

$$TIV = V_{dc} + (L_{cb} + L_L)\frac{i_f\,(t_{br})}{t_e - t_{br}} \tag{3.4}$$

The current in MOV_1 reaches zero when its voltage falls below its rated voltage. The TIV is limited by the rated voltage of the surge arrester. Therefore, using Equation (3.4), the maximum required time for MOV_1 current to fall to zero can be given as:

$$(t_e^{max} - t_{br}) = (L_{cb} + L_L)\frac{i_f\,(t_{br})}{V_r - V_{dc}} \tag{3.5}$$

The absorbed energy in MOV_1 holds:

$$E_{MOV} = \int_{t_{br}}^{t_e} V_{MOV}\,(t) \cdot i_f\,(t)\,dt \tag{3.6}$$

Assuming linear decrease of fault current for $t_{br} < t < t_e$ and also constant voltage across MOV_1, the maximum absorbed energy in MOV_1 can be given as:

$$E_{MOV}^{max} = \int_{t_{br}}^{t_e^{max}} V_r \cdot \frac{i_{max} \cdot (t - t_e^{max})}{(t_{br} - t_e)} dt = \frac{V_r \cdot i_{max} \cdot (t_e^{max} - t_{br})}{2} \tag{3.7}$$

We obtain the maximum absorbed energy in MOV_1 by rearranging equations (3.5) and (3.7):

$$E_{MOV}^{max} = \frac{1}{2}(L_{cb} + L_L) \cdot i_{max}^2 \left(\frac{V_r}{V_r - V_{dc}} \right) \tag{3.8}$$

The term $\frac{1}{2}(L_{cb} + L_L) \cdot i_{max}^2$ in Equation (3.8) represents the instantaneous stored energy in the inductive elements of system at the interruption instance. Equation (3.8) implies that the maximum absorbed energy in the surge arrester is always larger than the stored energy in the inductive elements of system at the interruption instance by a factor of $\left(\frac{V_r}{V_r - V_{dc}}\right)$. The circuit in Figure 3.4 is simulated using a set of preliminary values[6] to clarify the impact of surge arrester OVP on energy absorption. The MOV's non-linear $V - I$ characteristic is modeled based on the data in [195] and using the piecewise modeling approach in PSCAD/EMTDC. Figure 3.6 depicts the employed $V - I$ characteristics of MOV.

[6] V_{dc} = 320 kV, L_{cb} = 50 mH, L_L = 274 mH, R_L=320 Ω

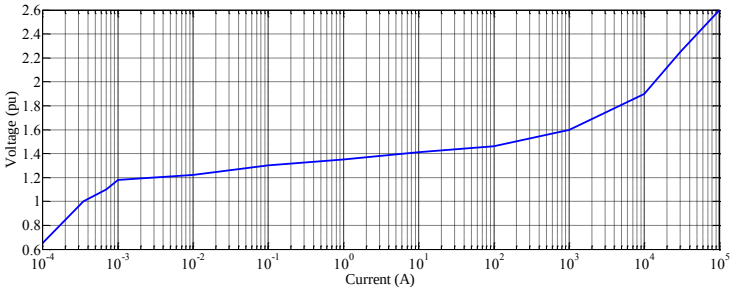


Figure 3.6: Nonlinear $V - I$ characteristic for an MOV [195].

V_{dc} is modeled as an ideal voltage source. A short circuit fault occurs at $t = 0$ s and the SSCB interrupts the current as soon as its current (i_{cb}) exceeds 2.5 kA. The simulation is carried out for five different values of MOV_1 OVP[7]. Figure 3.7 shows the voltage across MOV_1. Figure 3.8 depicts the current in SSCB before and after the fault. The current in the MOV with higher OVP reaches zero in shorter time as compared to the MOVs with lower OVP. The absorbed energy in MOV_1 is depicted in Figure 3.9. The numerical values for the maximum absorbed energy in the surge arrester and the maximum required time for energy absorption are illustrated in Table 3.1. Based on Equation (3.3), the stored energy at the interruption instance in the inductive elements of system is equal to 1.0125 MJ. It can be seen in Figure 3.9 that the total absorbed energy in the MOV is larger than the stored energy in the inductive elements of system. The MOV with higher OVP absorbs less energy as compared to the MOVs with lower

[7] $OVP_{MOV1} = \{380, 420, 480, 520, 580\}$ $[kV]$

OVP. Table 3.1 implies that the values obtained from equations (3.5) and (3.8) are close to the simulation results particularly, for MOVs with higher OVP.

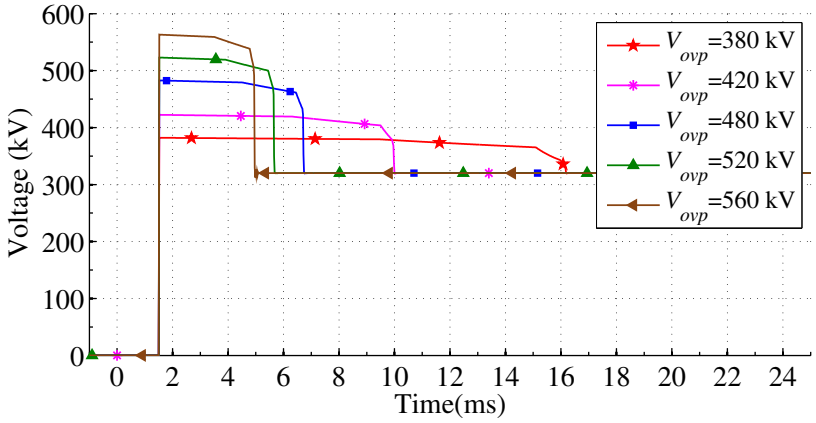


Figure 3.7: Voltage across MOV_1.

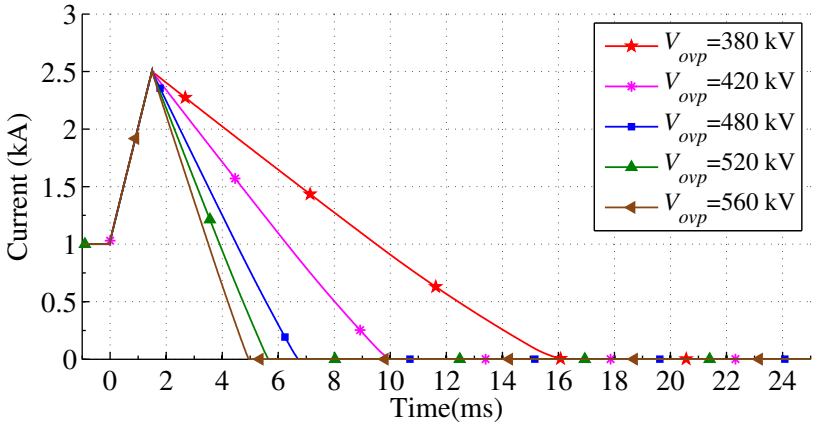


Figure 3.8: Current in SSCB (i_{cb}).

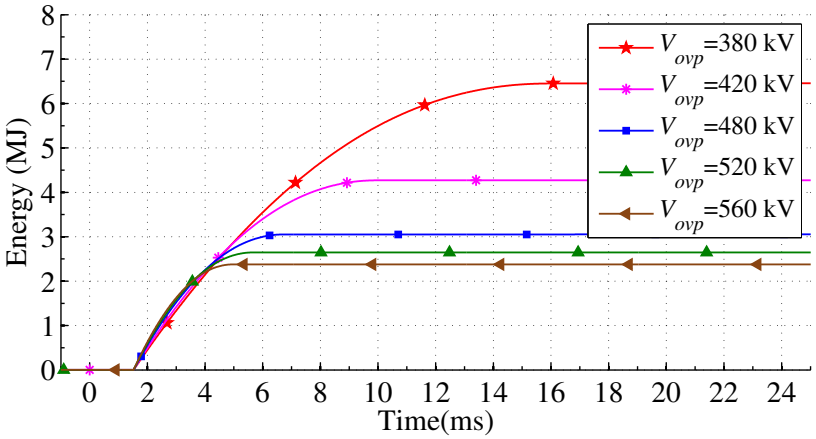


Figure 3.9: Absorbed energy in MOV_1.

Table 3.1: The absorbed energy by MOV_1 and energy absorption time.

MOV OVP (V_r)	**Energy Absorption time (t_e) [ms]**		**Absorbed Energy (E^{max}_{MOV}) [MJ]**	
	Simulation	Equation (3.5)	Simulation	Equation (3.8)
380 kV	14.5	13.5	6448	6409.12
420 kV	8.4	8.1	4279	4252.5
480 kV	5.2	5.06	3052	3037.5
520 kV	4.1	4.05	2646	2632.5
580 kV	3.2	2.23	2376	2258

Drawbacks

The dc circuit breaker is a protective device and should be designed with high reliability to interrupt the fault current without damage to nearby equipments or self-destruction. Although the surge arresters are utilized in the HVdc and ac systems for protection the equipments against the surge voltages, there are few drawbacks that may make their application in the dc circuit breakers challenging:

- Due to the large magnitude of short circuit current and also large cable inductance in an HVdc grid the MOV must be able to absorb a substantial amount of energy. Therefore, the energy absorption capability of MOVs are crucial in their application in dcCBs [188]. Typical MOVs are composed of Zinc-oxide (ZnO) nonlinear resistor elements. In order to increase the energy capability of ZnO varistors their physical dimensions have to be enlarged. Physical enlargement of ZnO varistors can affect the electrical uniformity of the material [199]. The non-uniformity in electrical and thermo-physical characteristics can cause a reduction in MOV energy absorption capability [190].
- Puncture failure mode due to the high current concentration [200].
- Cracking failure mode due to nonuniform heating, which can cause thermal stresses higher than the failure stress of the material [200].
- Lower energy absorption capability for shorter pulse width [190].
- The aging of electrical materials due to the exposure to high temperatures, the composition of the surrounding material, the level of oxygen,presence or not of ozone, the degree and type of impurities, the presence of radiation such as ultraviolet light, overheating, pollution, humidity and an excessive electric field [201].
- Dependency of the MOV aging on factors as wave shape, mean current density discharged by the resistor, average temperature of the resistor, surge polarity and number of discharges [201,202].
- Quantitative dependency of MOV lifetime on the surge arrester location and installation on the networks and on the region keraunic levels [201].

3.2 Proposed Surge-less dc Circuit Breaker

3.2.1 Topology

Figure 3.10 depicts the topology of proposed surge-less dc circuit breaker. The proposed dc circuit breaker will be referred as the current releasing dc circuit breaker (CRCB) in this thesis. The CRCB is composed of main breaker (MB) unit, charging branch, discharging branch, capacitor and a current limiting inductor. The MB unit of the CRCB can be realized by series (and parallel) connection of power semiconductor switches. It can be seen in Figure 3.10, the semiconductor switches in the MB unit are connected in one direction, which implies that the CRCB is able to interrupt the current only in its forward direction (line side). The current flow in the backward direction (converter side) of the CRCB cannot be interrupted by the CRCB. Hence, the proposed CRCB is a unidirectional dcCB.

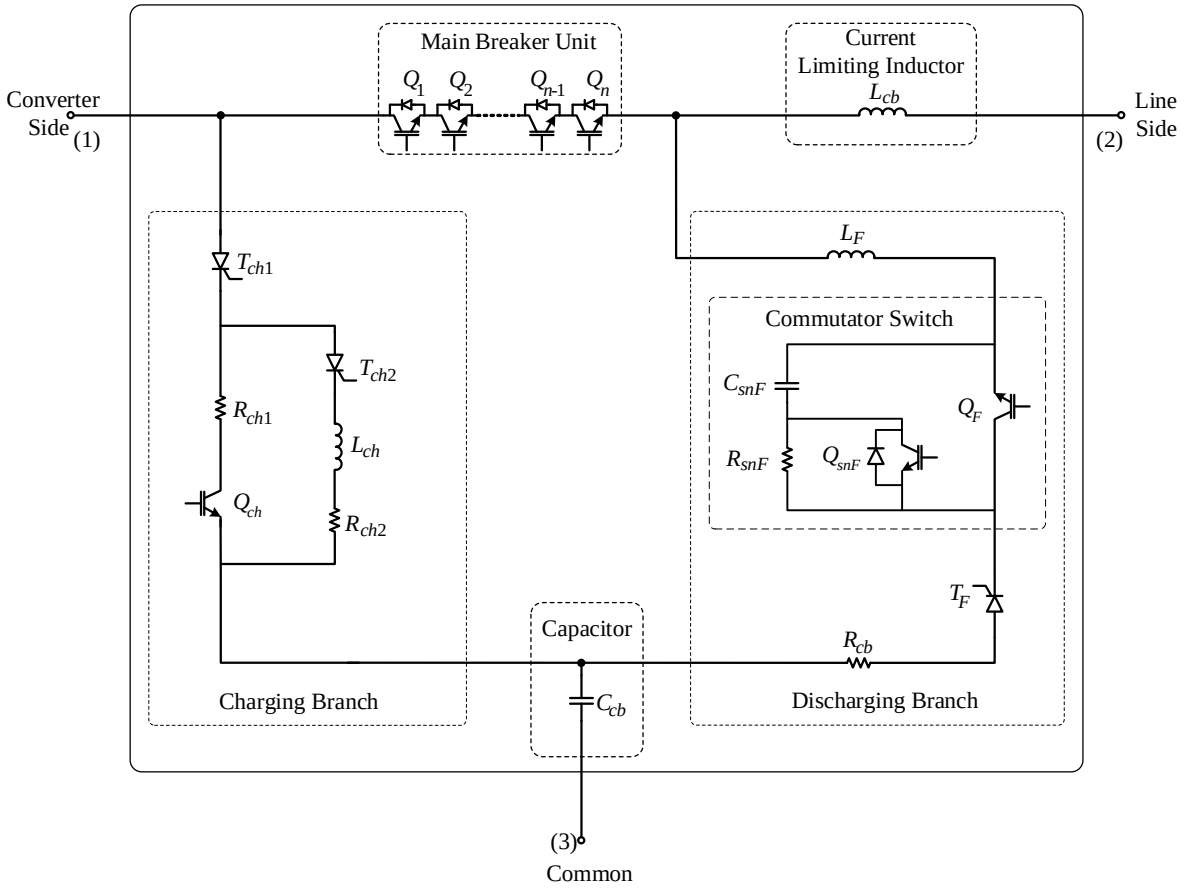


Figure 3.10: Topology of the current releasing dc circuit breaker (CRCB).

The charging branch consists of two thyristor banks (T_{ch1} and T_{ch2}), a low voltage gate controlled semiconductor switch (Q_{ch}), two resistors (R_{ch1} and R_{ch2}) and an inductor (L_{ch}). The discharging branch is composed of a thyristor bank (T_F), resistor (R_{cb}), two low voltage gate controlled semiconductor switches (Q_F and Q_{snF}), a low voltage resistor (R_{snF}) and a low voltage capacitor (C_{snF}).

3.2.2 *Operation Principles*

The CRCB can be integrated into the existing HVdc configurations including asymmetric and symmetric monopole and bipolar systems. Figure 3.11 shows the CRCB integration into the different HVdc configurations. The metallic return path might be installed in the asymmetric monopole and the bipole systems. Therefore, the metallic return is depicted by the dashed line in Fig 3.11(a) and (c). The operation principles of CRCB are detailed for the asymmetric monopole system and pole-to-ground fault in this subsection. Figure 3.12 depicts a detailed schematic of CRCB when it is integrated into a point-to-point asymmetric HVdc system. It is assumed that VSC 1 and VSC 2 operate in the rectifier and inverter modes, respectively. The operation procedure for a pole-to-pole fault in symmetric monopole system is similar to the pole-to-ground fault in asymmetric monopole system but two CRCBs at both positive and negative poles of VSC must trip. The pole-to-ground fault interruption process in the bipolar system is equivalent to the pole-to-ground fault in the asymmetric monopole system.

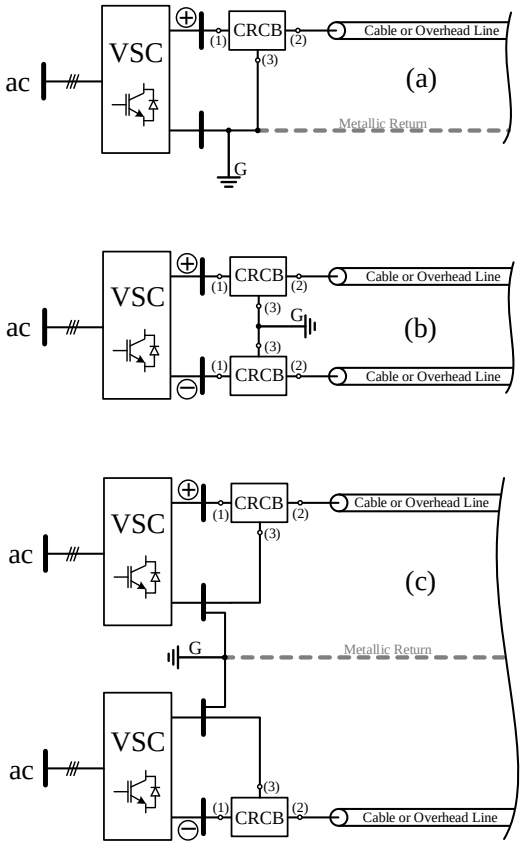


Figure 3.11: CRCB integrated to different HVdc configurations: (a) Asymmetric monopole, (b) Symmetric monopole, (c) Bipolar.

Normal Conduction Mode

When the CRCB is in open mode, all switches in the MB unit (Q_1-Q_n) are turned off. T_F should not be triggered whereas Q_{ch} and Q_F must be turned on. The CRCB can be closed by turning on all the switches

in the MB unit. The prerequisite of current interruption in the fault operation mode is the capacitor C_{cb} charging stage, which can be done upon energization of the dc bus side of the CRCB. When the CRCB is closed the current can flow in its forward and backward directions due to presence of antiparallel diodes of the switches in the MB unit. Figure 3.14 shows the current path in the normal conduction mode of the CRCB. The current flows through the semiconductor switches of MB_1, the transmission line and the antiparallel diodes of MB_2 from rectifier side to the inverter side. The current direction can be reversed without extra measures since the MB units at both CRCBs are in the close states.

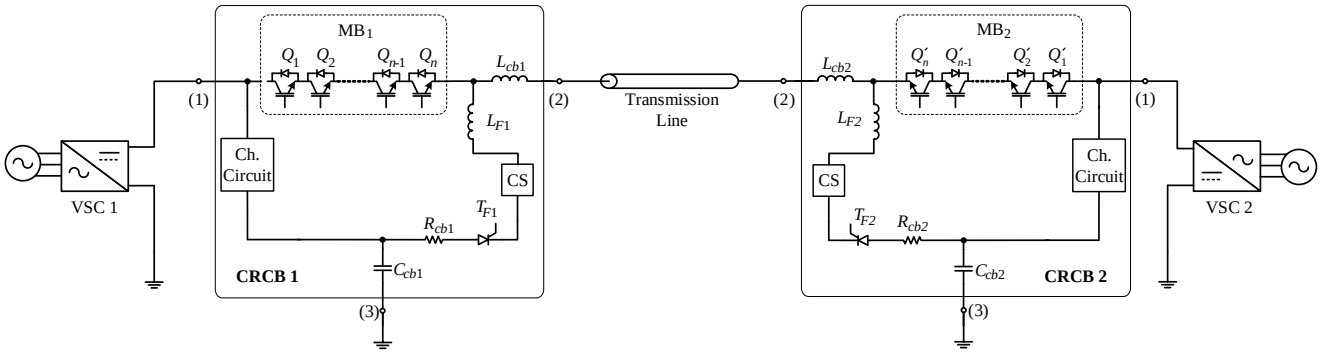


Figure 3.12: Detail schematic of the CRCB integration into an asymmetric monopole HVdc system.

Charging Mode

Capacitor charging has two stages. The first charging stage can start by triggering the gate of T_{ch1}. Figure 3.13 depicts the current path after T_{ch} is triggered. As soon as the charging current reaches specific value, T_{ch2} must be triggered and simultaneously Q_{ch} must be opened. This action will starts the second charging stage. In the second charging stage, the current is commutated into T_{ch2}, R_{ch2} and L_{ch}. The new current path will charge the CRCB capacitor (C_{cb}) to a voltage larger than the dc bus voltage due to the presence of L_{ch}. The charging stage will be analytically detailed in section 3.3.

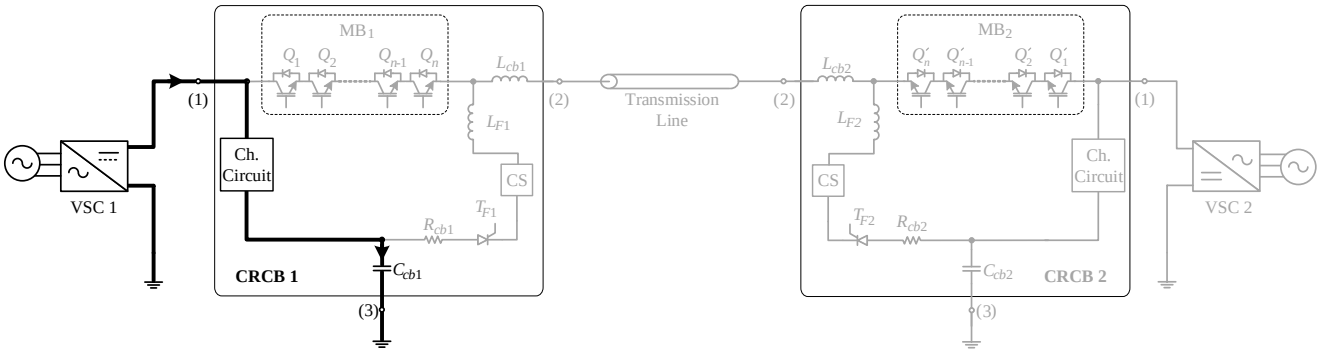


Figure 3.13: The capacitor charging stage.

The charging current peak in the first stage is limited by R_{ch1}. In the second charging stage the voltage difference between the dc bus

and the CRCB capacitor is in the range of few kilo volts and hence the value of R_{ch2} can be selected smaller than R_{ch1}. C_{cb} must be kept charged and if its voltage drops below specific value the charging process must be repeated.

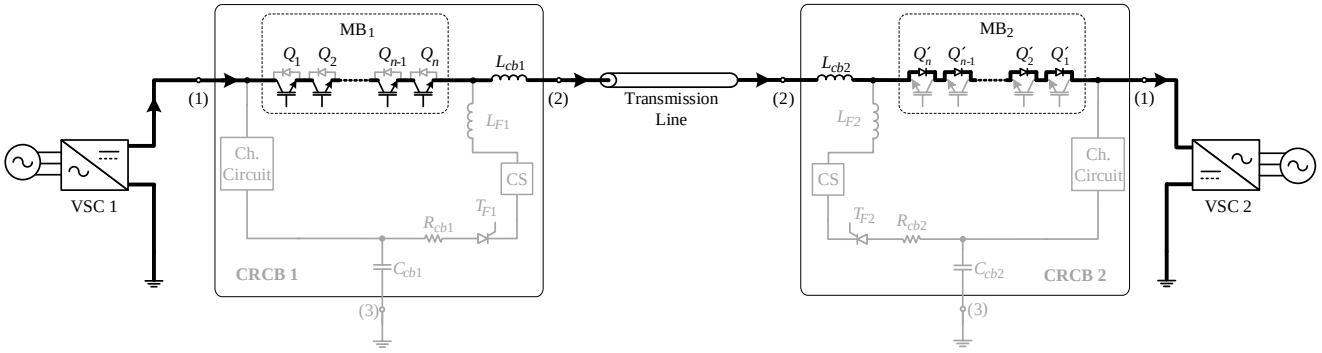


Figure 3.14: Normal conduction stage.

Current Interruption Mode

Upon detection of a fault on a transmission line both CRCBs attached to the faulty transmission line should trip. The time delay between the trip command and fault inception depends on the protection scheme features. Figure 3.15 shows the current interruption stage when a pole-to-ground short circuit fault occurs on the transmission line.

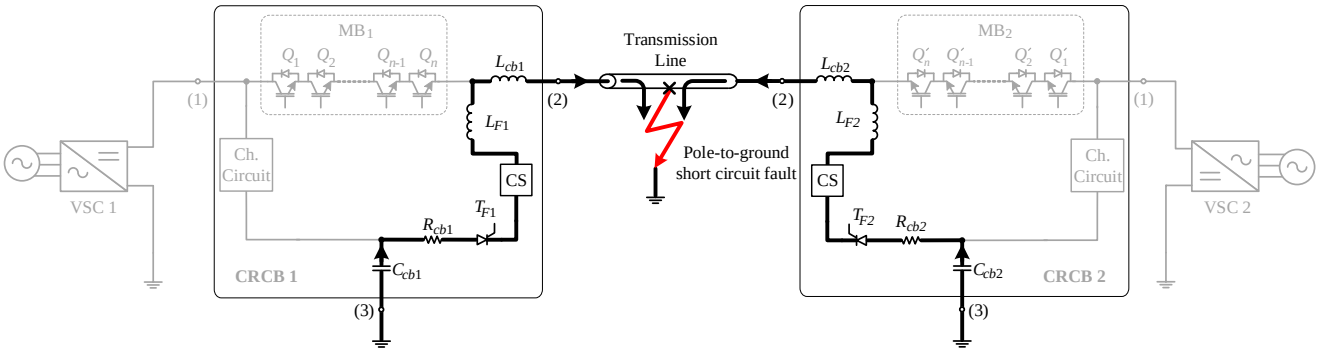


Figure 3.15: Current interruption stage.

To interrupt the fault current and isolate it from the VSC, the MB units in both CRCB 1 and 2 must be opened and T_{F1} and T_{F2} should be triggered. Triggering T_{F1} discharges C_{cb1} to the faulty transmission line and feeds the fault point by the limited stored energy in the capacitor. In other words, discharging the capacitor does not allow the voltage at point A to collapse rapidly. The same process should be done in CRCB 2 at the other end of the transmission line. Therefore, the switches in the MB units turn off softly without high surge voltage. Stored energy in the current limiting inductor and the inductance of cable is also discharged and dissipated in R_{F1} and R_{F2}, cable

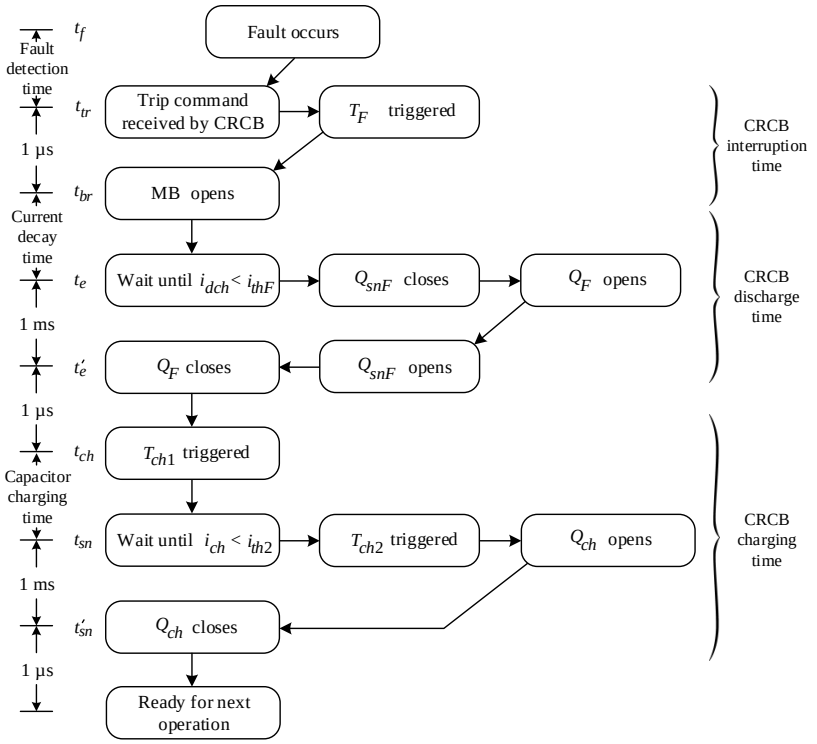


Figure 3.16: CRCB fault current interruption process.

resistance and fault resistance. To avoid commutation failures in T_{F1} and T_{F2} a low voltage gate controlled switch (Q_{F1} and Q_{F2}) is included in the topology of each CRCB. Q_{F1} and Q_{F2} should be turned off for a short period of time after the corresponding capacitor is discharged in order to interrupt the residual current and commutate T_{F1} and T_{F1} by the help of their active RC snubber circuits. Figure 3.16 depicts the sequential current interruption process in the CRCB. The time period $t_{br} - t_f$ depends on the perception scheme fault identification time. The current interruption time of CRCB lies in range of few tens of micro seconds due to fast turn-off of semiconductor switches. However, after current interruption the CRCB capacitor will discharge till time $t = t_e$. An additional time is considered to guarantee the current commutation in the discharging branch. Hence, the CRCB discharge time will be equal to $t'_e - t_{br}$. The CRCB discharge time depends on the fault location and the fault impedance.

3.3 Theoretic Analysis

This subsection aims to analyze the detailed behavior of CRCB in the charging and current interruption processes. The converter is modeled as an ideal dc voltage source in this analysis. The analysis are presented for charging and fault interruption modes of the CRCB.

3.3.1 Charging Mode

Figure 3.17 depicts the equivalent circuit of the charging branch in the CRCB. This circuit has two operation stages including The first and the second charging stages.

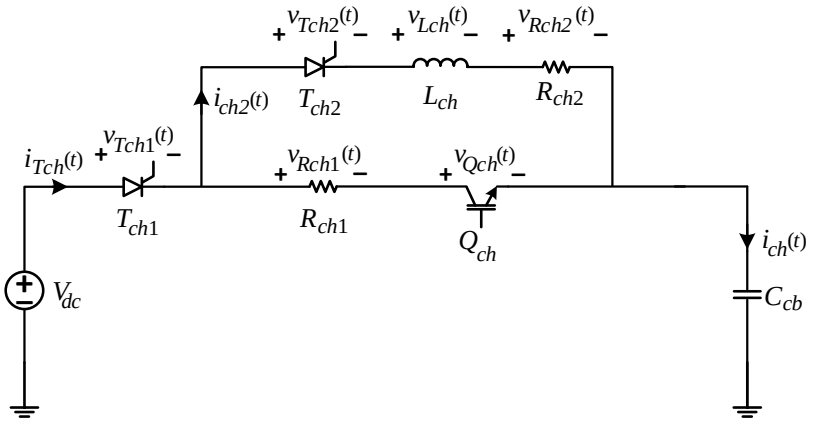


Figure 3.17: Equivalent circuit of a charging stage of the CRCB.

The First Charging Stage

As it was mentioned in subsection 3.2.2, Q_{ch} is always closed during the first stage of charging mode. Figure 3.18 shows that the current flows through T_{ch1}, Q_{ch} and R_{ch1} and charges the capacitor.

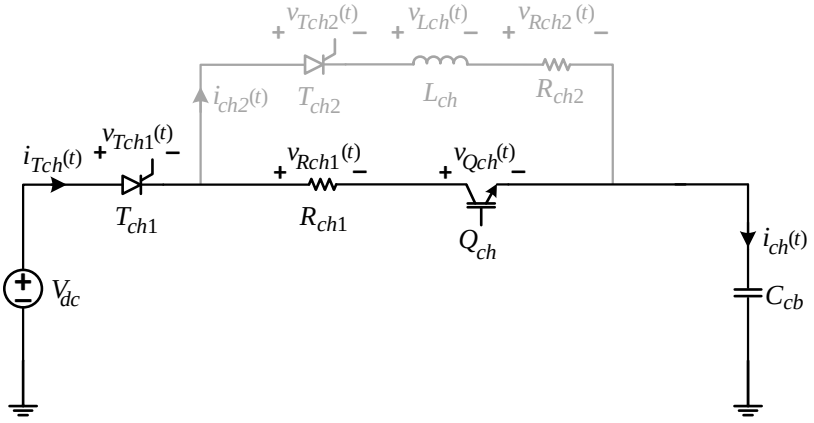


Figure 3.18: Equivalent circuit of a charging stage of the CRCB.

Neglecting the voltage drop across T_{ch} and Q_{ch}, the equivalent circuit represents a well-known series RC circuit [203]. The current

and voltage equations can be given as follows:

$$\begin{aligned} v_{Ccb}(t) &= V_{dc}\left(1 - e^{-\frac{t}{R_{ch1}C_{cb}}}\right); \quad v_{Ccb}(t_0) = 0 \\ i_{Ccb}(t) &= \frac{V_{dc}}{R_{ch1}} e^{-\frac{t}{R_{ch1}C_{cb}}}; \quad v_{Ccb}(t_0) = 0 \end{aligned} \tag{3.9}$$

The Second Charging Stage

T_{ch1} may be turned off naturally if its current falls below its holding current. However, the thyristor commutation can only be guaranteed if the voltage across the thyristor is reversed for a sufficient period of time and its reverse recovery current is provided. This period should not be less than the circuit commutated turn-off time of the thyristor. Hence, in order to grantee the successful turn-off of the thyristor a different scheme is proposed and applied in the CRCB. The second stage starts when the charging current (i_{ch}) falls below a specific level (i_{th2}) by triggering T_{ch2} and opening Q_{ch}. This action commutates the current into T_{ch2}. Figure 3.19 depicts the equivalent circuit for the second stage.

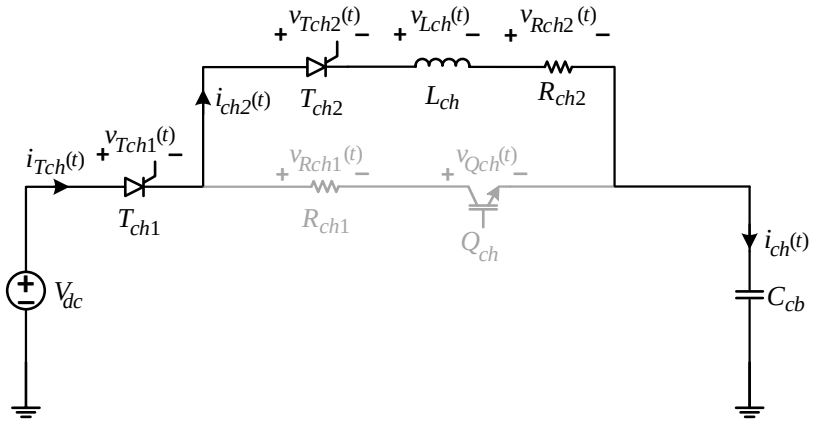


Figure 3.19: Equivalent circuit of a charging stage of the CRCB.

As can be seen in Figure 3.19, the circuit represents a series RLC circuit. Assume that the charging current of the first stage falls below i_{th2} at $t = t_1$. The voltage difference between C_{cb} and the dc voltage source at $t = t_1$ can be given by:

$$\Delta V = V_{dc} - v_{Ccb}(t_1) = R_{ch1} i_{ch}(t_1); \quad t_0 < t \tag{3.10}$$

After Q_{ch} is opened and T_{ch2} is triggered, the current flows through the parallel branch via T_{ch2}, L_{ch} and R_{ch2}. The differential equation for this stage of operation can be given as follow:

$$\frac{\mathrm{d}^2 i_{ch}(t)}{\mathrm{d}t^2} + \frac{R_{ch2}}{L_{ch}} \cdot \frac{\mathrm{d}i_{ch}(t)}{\mathrm{d}t} + \frac{1}{L_{ch}C_{cb}} i_{ch}(t) = 0 \tag{3.11}$$

The damping factor of the snubber circuit can be given by:

$$\xi = \frac{R_{ch2}}{2}\sqrt{\frac{C_{cb}}{L_{ch}}} \tag{3.12}$$

If the inductor and capacitor in the snubber circuit are designed for under-damped operation the current equation for $\xi < 1$ can be given by [203]:

$$i_{ch}(t) = ke^{-\alpha t} sin(\omega_d t + \theta) \tag{3.13}$$

where

$$\begin{aligned} \omega_d &= \sqrt{\omega_0^2 - \alpha^2} \\ \omega_0 &= \frac{1}{\sqrt{L_{ch} C_{cb}}} \\ \alpha &= \frac{R_{ch2}}{2L_{ch}} \end{aligned} \tag{3.14}$$

and k and θ should be obtained based on the initial conditions of the circuit. Initially, the current in the inductor and the capacitor voltage are zero. In addition, at initial instance the snubber inductor acts as open circuit and the applied voltage appears across the inductor. Therefore the initial conditions of the circuit can be given by:

$$\begin{aligned} i_{Lch}(t_1) &= 0 \\ v_{Lch}(t_1) &= \Delta V \\ &= L_{ch} \frac{\mathrm{d}i_{ch}(t)}{\mathrm{d}t}\bigg|_{t=t_1} \end{aligned} \tag{3.15}$$

Therefore, the current derivative at $t = t_1$ can be evaluated as:

$$\frac{\mathrm{d}i_{ch}(t)}{\mathrm{d}t}\bigg|_{t=t_1} = \frac{v_{Lch}(t_1)}{L_{ch}} \tag{3.16}$$

Using Equation (3.15), the constants k and θ can be obtained as follows:

$$\begin{aligned} k &= \frac{\Delta V}{L_{ch}\omega_d} \\ \theta &= 0 \end{aligned} \tag{3.17}$$

The current equation can be rearranged as:

$$i_{ch}(t) = \frac{\Delta V}{L_{ch}\omega_d} e^{-\alpha t} sin(\omega_d t) \tag{3.18}$$

Equation 3.18 implies that the current in L_{sn} oscillates under two envelopes including $e^{-\alpha t}$ and $-e^{-\alpha t}$. The oscillation frequency is equal to ω_d. However, in this circuit, as soon as the current in the snubber branch reaches zero, the thyristors (T_{ch1} and T_{ch2}) will not allow the current direction to be reversed. In order to analyze the behavior of charging circuit, the capacitor and the inductor voltages must be obtained for the instant when the current in L_{ch} reaches zero. Considering the oscillation frequency, the current in inductor reaches zero at $t_2 = t_1 + \frac{\pi}{\omega_d}$. The inductor voltage can be derived as follows:

$$\begin{aligned} v_{Lch}(t) &= L_{ch} \frac{\mathrm{d}i_{ch}(t)}{\mathrm{d}t} \\ &= \frac{\Delta V \left(-\alpha e^{-\alpha t} sin(\omega_d t) + \omega_d e^{-\alpha t} cos(\omega_d t)\right)}{\omega_d} \end{aligned} \tag{3.19}$$

Therefore, the inductor voltage when its current reaches zero at $t_2 = \frac{\pi}{\omega_d}$ can be given by:

$$v_{Lch}\left(\frac{\pi}{\omega_d}\right) = -\Delta V e^{-\alpha\frac{\pi}{\omega_d}} \tag{3.20}$$

The capacitor current holds:

$$i_{Ccb}(t) = C_{cb}\frac{\mathrm{d}v_{Ccb}(t)}{\mathrm{d}t} \tag{3.21}$$

Hence, its voltage can be given by:

$$v_{Ccb}(t) = \frac{1}{C_{cb}}\int i_{Ccb}(t)\,dt + V_{Ccb0} \tag{3.22}$$

where, V_{Ccb0} represents the initial voltage of capacitor, which is equal to its voltage at $t = t_1$. Considering that the initial voltage of snubber capacitor is almost zero the capacitor voltage can be derived as follows:

$$\begin{aligned} v_{Ccb}(t) &= \frac{1}{C_{cb}}\int_0^t \frac{\Delta V}{L_{ch}\omega_d}e^{-\alpha t'}sin\left(\omega_d t'\right)dt' + V_{Ccb0} \\ &= \frac{\Delta V\left(-\omega_d e^{-\alpha t'}cos\left(\omega_d t'\right) - \alpha e^{-\alpha t'}sin\left(\omega_d t'\right)\right)}{L_{ch}C_{cb}\omega_d\left(\omega_d^2+\alpha^2\right)}\Bigg|_0^t + V_{Ccb0} \\ &= \frac{\Delta V\left[\left(-\omega_d e^{-\alpha t}cos\left(\omega_d t\right) - \alpha e^{-\alpha t}sin\left(\omega_d t\right)\right) + \omega_d e^{-\alpha t}\right]}{L_{ch}C_{cb}\omega_d\left(\omega_d^2+\alpha^2\right)} \\ &+ V_{Ccb0} \end{aligned} \tag{3.23}$$

Using the relations among ω_d, ω_0 and α from Equation (3.14), Equation (3.23) can be rearranged as follows:

$$\begin{aligned} v_{Ccb}(t) &= \frac{\Delta V}{\omega_d}\left[\left(-\omega_d e^{-\alpha t}cos\left(\omega_d t\right) - \alpha e^{-\alpha t}sin\left(\omega_d t\right)\right) + \omega_d e^{-\alpha t}\right] \\ &+ V_{Ccb0} \end{aligned} \tag{3.24}$$

Assuming $t_1 = 0$ s the snubber capacitor voltage when its current reaches zero (at time t_2) can be given by:

$$\begin{aligned} v_{Ccb}(t_2) &= v_{Ccb}\left(\frac{\pi}{\omega_d}\right) \\ &= \Delta V\left(1 + e^{\frac{-\alpha\pi}{\omega_d}}\right) + V_{Ccb0} \end{aligned} \tag{3.25}$$

From KVL at $t = t_2^+$ we have:

$$\begin{aligned} V_{dc} - v_{Tch1}\left(t_2^+\right) - v_{Tch2}\left(t_2^+\right) - v_{Lch}\left(t_2^+\right) - v_{Rch2}\left(t_2^+\right) \\ - v_{Ccb}\left(t_2^+\right) = 0 \end{aligned} \tag{3.26}$$

As previously mentioned, the voltage of C_{cb} is almost constant for $t > t_2$. The voltage across R_{ch2} and L_{ch} for $t > t_2$ is zero since

no current flows through them. Therefore, the voltage across the thyristors at $t = t_2^+$ can be obtained as follows:

$$\begin{aligned} v_{TchT}\left(t_2^+\right) &= v_{Tch1}\left(t_2^+\right) + v_{Tch2}\left(t_2^+\right) \\ &= V_{dc} - v_{Ccb}\left(t_2^+\right) \\ &= \Delta V - \Delta V\left(1 + e^{\frac{-\alpha\pi}{\omega_d}}\right) - V_{Ccb0} \end{aligned} \tag{3.27}$$

Considering that $V_{Ccb0} = V_{dc} - \Delta V$, Equation (3.27) can be rearranged as follows:

$$v_{TchT}\left(t_2^+\right) = -\Delta V e^{\frac{-\alpha\pi}{\omega_d}} \tag{3.28}$$

Equation (3.28) can be expanded as follows:

$$v_{TchT}\left(t_2^+\right) = -\Delta V e^{\frac{-\pi}{\sqrt{\frac{4L_{ch}}{R_{ch2}^2 C_{cb}} - 1}}} \tag{3.29}$$

Equation (3.28) illustrates that voltage across thyristor will be negative for $t > t_2$ until Q_{ch} closes at $t = t_3$. The magnitude of negative voltage for a given CRCB capacitor depends upon the ratio of values of the inductor and charging resistor (R_{ch2}). At $t = t_3$, Q_{ch} is closed.

3.3.2 *Fault Interruption Mode*

The First Stage

As shown in Figure 3.15, a pole-to-ground fault in an asymmetric monopole system divides the system in two independent sections. The two sections are named as section A and B. In order to analyze the CRCB behavior one section should be considered. Figure 3.20 shows the equivalent circuit of section A in the asymmetric monopole dc system depicted in Figure 3.15. The other parameters of the circuit can be given as:

- sw_1: Thyristor T_F
- sw_2: Main breaker unit (Series connection of Q_1,...,Q_n)
- R_{cb}: CRCB resistor
- C_{cb}: CRCB capacitor
- L_{cb}: Main current limiting inductor
- L_F: Thyristor current derivative limiting inductor
- R_L: Transmission line resistance
- L_L: Transmission line inductance
- R_f: Fault resistance

To analyze the circuit, semiconductor switches are replaced by ideal switches. As mentioned in chapter 2, the fault impedance for both pole-to-ground and pole-to-pole faults in HVdc cables is very low. The equivalent circuit of the system can be aggregated more

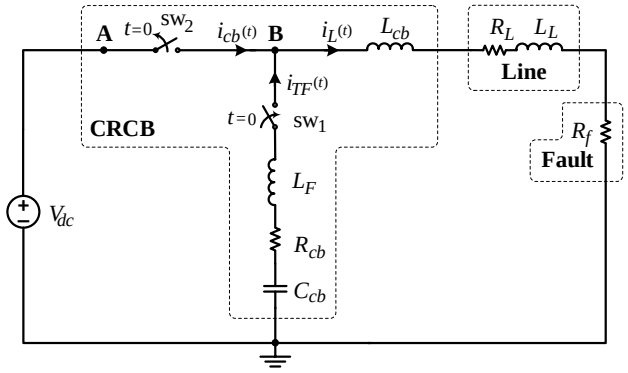


Figure 3.20: Equivalent circuit of a simplified dc system in presence of the CRCB.

by combining few elements of the circuit. Figure 3.21 shows the aggregated equivalent circuit of the system. As it is illustrated in (3.30), L represents the sum of current limiting inductor and the line inductance and also R represents the sum of fault and transmission line resistances.

$$\begin{aligned} L &= L_{cb} + L_L \\ R &= R_f + R_L \end{aligned} \tag{3.30}$$

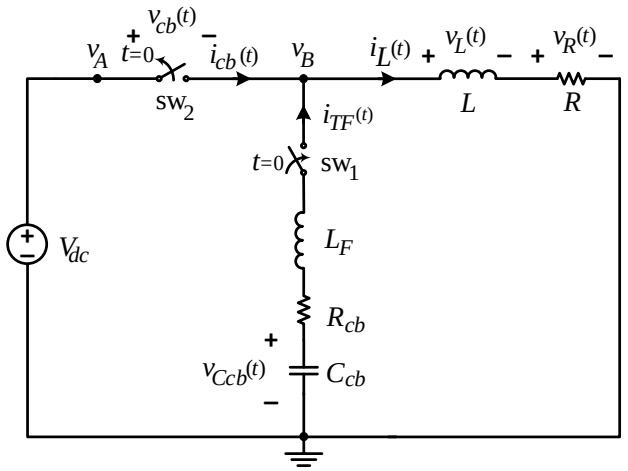


Figure 3.21: Aggregated equivalent circuit of a dc system in presence of the CRCB.

Based on the CRCB operation principles, it is assumed that sw_2 is opened and almost simultaneously sw_1 is closed at time $t = t_{br}$. At the interruption instance the voltage of CRCB capacitor is almost equal to the dc bus voltage. Hence, the initial conditions of the circuit can be approximately given by:

$$\begin{aligned} v_C\left(t_{br}\right) &= V_{C0} \\ i_L\left(t_{br}\right) &= i_{max} \end{aligned} \tag{3.31}$$

where $v_C\left(t_{br}\right)$ and $i_L\left(t_{br}\right)$ are the initial voltage of the CRCB capacitor and the initial current of its inductor, respectively. i_{max} is the fault current magnitude at the interruption instance. After switching action is done at $t = t_{br}$, the depicted equivalent circuit in Figure 3.21 represents a second order series RLC circuit. The well-known

differential equation for this circuit is given by (3.32) [203].

$$\frac{\mathrm{d}^2 i_L(t)}{\mathrm{d}t^2} + \frac{(R+R_{cb})}{(L+L_F)} \cdot \frac{\mathrm{d}i_L(t)}{\mathrm{d}t} + \frac{1}{LC_{cb}} i_L(t) = 0 \tag{3.32}$$

The damping factor of the RLC circuit can be given by (3.33).

$$\xi = \frac{R+R_{cb}}{2}\sqrt{\frac{C_{cb}}{L+L_F}} \tag{3.33}$$

When $\xi > 1$ the circuit has an over-damped response and for $\xi < 1$ the response is under-damped. For proper operation of CRCB it is necessary to avoid line current oscillation. Therefore, the internal parameters of CRCB should be designed to push the circuit to over-damped regime. Hence, here the behavior of circuit for the over-damped condition is analyzed. Solving the second order differential equation, the line current can be given by (3.34).

$$i_L(t) = k_1 e^{s_1 t} + k_2 e^{s_2 t} \tag{3.34}$$

where

$$s_1 = \frac{-(R+R_{cb})}{2(L+L_T)} + \sqrt{\frac{(R+R_{cb})^2}{4(L+L_T)^2} - \frac{1}{(L+L_F)C_{cb}}} \tag{3.35}$$

$$s_2 = \frac{-(R+R_{cb})}{2(L+L_F)} - \sqrt{\frac{(R+R_{cb})^2}{4(L+L_F)^2} - \frac{1}{(L+L_F)C_{cb}}} \tag{3.36}$$

$$k_1 = \frac{1}{s_1 - s_2}\left(\frac{V_{C0} - (R+R_{cb})\, i_{max}}{L+L_F} - s_2 i_{max}\right) \tag{3.37}$$

$$k_2 = \frac{1}{s_2 - s_1}\left(\frac{V_{C0} - (R+R_{cb})\, i_{max}}{L+L_F} - s_1 i_{max}\right) \tag{3.38}$$

The voltage at point B (v_B) for $t > t_{br}$ can be given as follows:

$$\begin{aligned} v_B(t) &= L\frac{\mathrm{d}i_L(t)}{\mathrm{d}t} + Ri_L \\ &= k_1 s_1 L e^{s_1 t} + k_2 s_2 L e^{s_2 t} + Ri_L \end{aligned} \tag{3.39}$$

Assuming v_A equal to V_{dc} after opening sw_2, $v_{cb}(t)$ can be derived as (3.40).

$$v_{cb}(t) = V_{dc} - k_1 s_1 L e^{s_1 t} - k_2 s_2 L e^{s_2 t} - Ri_L \tag{3.40}$$

The current peak in transmission line will be reached at $t = t_{imax}$ when the derivative of Equation (3.34) will be zero. t_{imax} can be given as follows:

$$t_{imax} = \frac{\ln\left(-\frac{k_1 s_1}{k_2 s_2}\right)}{(s_2 - s_1)} \tag{3.41}$$

The current peak in the transmission line after interruption instant can be given by:

$$I_{L,max} = k_1\left(-\frac{k_1 s_1}{k_1 s_1}\right)^{\frac{s_1}{s_2 - s_1}} + k_2\left(-\frac{k_1 s_1}{k_2 s_2}\right)^{\frac{s_2}{s_2 - s_1}} \tag{3.42}$$

The maximum TIV across the MB unit of the CRCB can be obtained by finding the time when its voltage derivative is zero. The time for maximum voltage can be given as:

$$t_{vmax} = \frac{\ln\left(-\frac{k_1 s_1^2}{k_2 s_2^2}\right)}{(s_2 - s_1)} \tag{3.43}$$

Consequently, the maximum transient inverse voltage across the main breaker unit can be given by Equation (3.44):

$$\begin{aligned} V_{cb,max} = V_{dc} &- k_1 \left(R + (L + L_T)\, s_1\right) \left(-\frac{k_1 s_1^2}{k_1 s_1^2}\right)^{\frac{s_1}{s_2 - s_1}} \\ &- k_2 \left(R + (L + L_T)\, s_2\right) \left(-\frac{k_1 s_1^2}{k_1 s_1^2}\right)^{\frac{s_2}{s_2 - s_1}} \end{aligned} \tag{3.44}$$

The Second Stage

In the second operation stage Q_F should be opened for a short period of time to generate a negative voltage across T_F. The equivalent circuit in this stage is shown in Figure 3.22. Q_F is closed while Q_{snF} is opened and C_{cb} discharges via Q_F into the current limiting inductor and the transmission line. The voltage across the snubber circuit (R_{snF} and C_{snF}) is equal to the conduction voltage drop across Q_F.

As soon as the discharging current (i_{TF}) falls below specific level

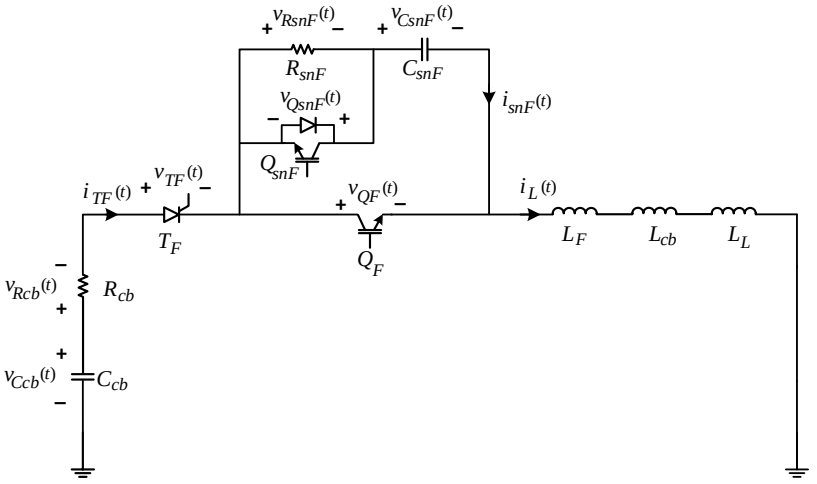


Figure 3.22: CRCB fault current interruption process.

(i_{th1}), Q_F will be opened and Q_{snF} will be closed at $t = t_0$. Figure 3.23 depicts the current path for $t > t_0$. The current limiting inductor L_{cb}, the thyristor current derivative limiting inductor (L_F) and the transmission line inductance L_L are replaced by their sum, which is represented by L_T. By closing Q_{snF}, the current cannot flow through R_{snF}. Therefore, the equivalent circuit contains two capacitors, one resistors and one inductor in series. The voltage difference between C_{cb} voltage and the voltage at fault location in the equivalent circuit in Figure 3.23 at $t = t_0$ is called ΔV. At $t = t_0$, the derivative of i_{TF}

has a small value compared to the initial discharge current. This can be valid also for the transmission line current. Therefore, ΔV can be given as follows:

$$\Delta V = v_A - v_{Ccb}(t_1) = R_{cb} \cdot i_{TF}(t_0) \tag{3.45}$$

C_{cb} and C_{snF} are in series connection. The initial voltage of C_{snF}

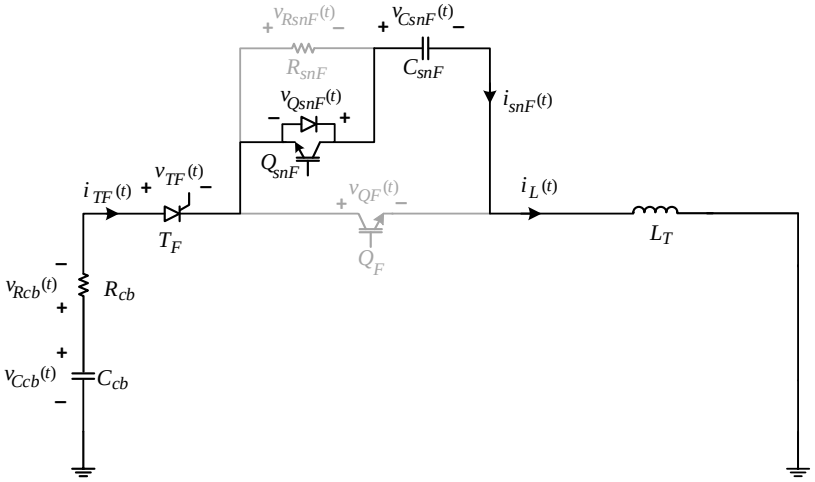


Figure 3.23: CRCB fault current interruption process.

is zero whereas the initial voltage of C_{cb} is equal to ΔV. The initial conditions of circuit can be given by:

$$\begin{aligned} i_L(t_0) &= I_0 \\ v_{Ccb}(t_0) &= \Delta V \end{aligned} \tag{3.46}$$

In order to simplify the analyze of this circuit we replace two capacitor by C_T, which is equal to series equivalent of two capacitors. The initial voltage of C_T will be equal to the initial voltage of C_{cb}. In addition, we replace two resistors by their series equivalent (R_T) as follow:

$$C_T = \frac{C_{cb}C_{snF}}{C_{cb} + C_{snF}}; \quad V_{CT}(t_0) = -\Delta V \tag{3.47}$$

The differential equation for this stage of operation can be given by:

$$\frac{\mathrm{d}^2 i_{snF}(t)}{\mathrm{d}t^2} + \frac{R_{cb}}{L_T} \cdot \frac{\mathrm{d}i_{snF}(t)}{\mathrm{d}t} + \frac{1}{L_T C_T} i_{snF}(t) = 0 \tag{3.48}$$

The damping factor of the snubber circuit can be given by:

$$\xi = \frac{R_{cb}}{2}\sqrt{\frac{C_T}{L_T}} \tag{3.49}$$

The inductor and capacitor in the snubber circuit should be designed for under-damped operation. Therefore, it is assumed that $\xi < 1$. Equation (3.49) can be solved considering the initial conditions from 3.46 [203]. The current equation for $\xi < 1$ can be given by:

$$i_{snF}(t) = \frac{\Delta V \omega_0^2 C_T e^{-\alpha t}}{\omega_d} sin(\omega_d t) + \frac{I_0 \omega_0 e^{-\alpha t}}{\omega_d} cos(\omega_d t + \phi); \quad t_0 < t < t_1 \tag{3.50}$$

$$v_{CT}(t) = \frac{-\Delta V \omega_0 e^{-\alpha t}}{\omega_d} cos(\omega_d t - \phi) + \frac{I_0 e^{-\alpha t}}{\omega_d C_T} sin(\omega_d t); \quad t_0 < t < t_1 \tag{3.51}$$

where

$$\begin{aligned} \omega_d &= \sqrt{\omega_0^2 - \alpha^2} \\ \omega_0 &= \frac{1}{\sqrt{L_T C_T}} \\ \alpha &= \frac{R_{cb}}{2L_T} \\ \phi &= \frac{\alpha}{\omega_d} \end{aligned} \tag{3.52}$$

In equations (3.50) and (3.51), t_1 represents the instant when the first zero crossing in the current happens. As soon as the snubber current reaches zero at $t = t_1$, it will not be able to reverse its direction due to the presence of the thyristor in the circuit. Therefore, the snubber capacitor will be charged until time t_1. Using trigonometric rules Equation (3.50) can be rearranged as follows:

$$\begin{aligned} i_{snF}(t) =& e^{-\alpha t}(Bsin(\omega_d t) + Acos(\omega_d t + \phi)) \\ =& e^{-\alpha t}\sqrt{A^2 + B^2 - 2ABsin(\phi)} \\ & \cdot cos\left(\omega_d t + tan^{-1}\left(\frac{Asin(\phi) - B}{Acos(\phi)}\right)\right) \end{aligned} \tag{3.53}$$

where

$$A = \frac{I_0 \omega_0}{\omega_d} \tag{3.54}$$

$$B = \frac{\Delta V \omega_0^2 C_T}{\omega_d} \tag{3.55}$$

Time t_1 can be obtained as follows:

$$\begin{aligned} & i_{snF}(t_1) = 0 \\ \Rightarrow \quad & cos\left(\omega_d t_1 + tan^{-1}\left(\frac{Asin(\phi) - B}{Acos(\phi)}\right)\right) = 0 \\ \Rightarrow \quad & t_1 = \frac{1}{\omega_d}\left(\frac{\pi}{2} - tan^{-1}\left(\frac{Asin(\phi) - B}{Acos(\phi)}\right)\right) \end{aligned} \tag{3.56}$$

Therefore, the voltage of equivalent capacitor at t_1 can be derived using Equations (3.51) and (3.56). If the snubber capacitor is chosen small enough compared to the CRCB capacitor we can write:

$$C_{snF} \ll C_{cb} \Rightarrow C_T \approx C_{snF} \tag{3.57}$$

As was mentioned, when Q_F opens the discharging current has a small value. Therefore, the peak of i_{snF} will have a small value too. Considering Equation (3.57), the voltage derivative across C_{cb} will be negligible against that of C_{snF}.

$$\left.\begin{aligned} \frac{dv_{Ccb}(t)}{dt} &= \frac{i_{snF}(t)}{C_{cb}} \\ \frac{dv_{CsnF}(t)}{dt} &= \frac{i_{snF}(t)}{C_{snF}} \end{aligned}\right\} \Rightarrow \frac{dv_{Ccb}(t)}{dt} \ll \frac{dv_{CsnF}(t)}{dt} \tag{3.58}$$

Using Equations (3.57) and (3.58), the voltage of C_{snF} at $t = t_1$ can be given by:

$$v_{CsnF}(t_1) = v_{CT}(t_1) + \Delta V \tag{3.59}$$

From KVL at $t = t_1^+$ we have:

$$v_{Ccb}(t_1^+) - v_{Rcb}(t_1^+) - v_{TF}(t_1^+) - v_{CsnF}(t_1^+) - v_{LT}(t_1^+) = 0 \tag{3.60}$$

Since the current in the circuit value is zero for $t > t_1$, the voltage across the resistor and the inductor will be zero. therefore, Equation (3.60) can be simplified as follows:

$$v_{Ccb}(t_1^+) - v_{TF}(t_1^+) - v_{CsnF}(t_1^+) = 0 \tag{3.61}$$

Using Equation (3.45) the voltage across the thyristor can be given by:

$$v_{TF}(t_1^+) = v_{CsnF}(t_1^+) \tag{3.62}$$

Depending on the CRCB resistor (R_{cb}) and the snubber capacitor (C_{cb}) values, $v_{CsnF}(t_1^+)$ can be several times greater than ΔV. Hence, the voltage across the thyristor will be negative for $t > t_1$ until Q_F is closed at time t_2. Figure 3.24 depicts the current path after Q_F is closed and Q_{snF} is opened. As can be seen the snubber capacitor will be discharged via the snubber resistor (R_{snF}) and Q_F. As soon as Q_F is closed the charging process can be started.

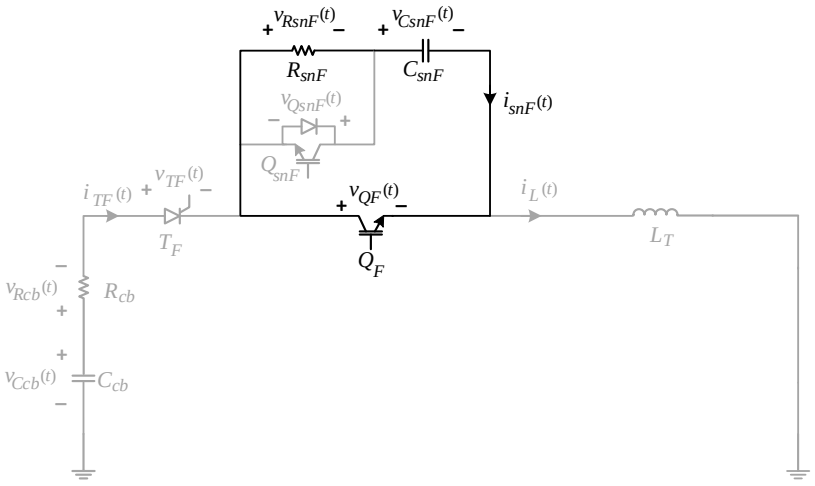


Figure 3.24: CRCB fault current interruption process.

3.3.3 *Power Losses*

The major part of the power losses in the CRCB is caused by the MB unit. The MB unit conducts the nominal current of the system in the normal condition. Figure 3.25 shows the structure of MB unit. In order to satisfy the voltage requirements of the grid the MB unit contains several semiconductor switches in series. depending on the current breaking capability The MB unit might have few parallel branches. IGBTs and IGCTs with antiparallel diodes are typically employed in realization of dcCBs. Depending on the power flow

direction in the dc transmission line, the current can flow through the switches or their antiparallel diodes. Therefore, the power losses caused by the semiconductor switches and diodes should be obtained.

The conduction power losses for both IGBTs and IGCTs can be approximated by modeling them as the series connection of a constant dc voltage source (u_{T0}), which represents the on-state collector-emitter voltage at zero-current and a resistor (r_C) representing the on-state resistance of semiconductor switch. Hence the collector-emitter voltage can be given by Equation (3.63) [204].

$$u_{CE}(t) = u_{T0} + r_c i_c(t) \tag{3.63}$$

where, i_c represents the current flowing through the collector of the semiconductor switch. Therefore, the conduction power losses for one IGBT or IGCT can be given as:

$$p_{c,sw}(t) = u_{CE}(t)\, i_C(t) = u_{T0} i_C(t) + r_c i_c^2(t) \tag{3.64}$$

Assuming a one-branch configuration of series semiconductor switches, the conduction power losses of MB unit during normal operation can be given by Equation (3.65).

$$p_{cs,sw}(t) = N_s \left(u_{T0} i_{MB}(t) + r_c i_{MB}(t)^2 \right) \tag{3.65}$$

where, N_s and $i_{MB}(t)$ represents the number of IGBTs in series connection and the current flowing through the MB unit. As it is shown in Figure 3.25, the MB unit may contain few parallel branches. Assuming that all the parallel branches will be turned on and turned off together, the nominal current will be shared between them almost equally. Therefore we have:

$$\begin{aligned} p_{cT,sw}(t) &= N_p N_s \left(u_{T0} \frac{i_{MB}(t)(t)}{N_p} + r_c \left(\frac{i_{MB}(t)}{N_p} \right)^2 \right) \\ &= \underbrace{N_s u_{T0} i_{MB}(t) + N_s r_c i_{MB}(t)^2}_{P_{cs,sw}} - N_s \frac{N_p - 1}{N_p} r_c i_{MB}(t)^2 \end{aligned} \tag{3.66}$$

Equation (3.66) implies that the total conduction power losses reduces by increasing the number of parallel branches for fixed number of switches in series. The power losses approximation for the antiparallel diodes is similar to that of IGBT [204]. The conduction power losses in the diodes considering the number of elements in series and the number of parallel branches can be given by:

$$p_{cT,D}(t) = N_s u_{D0} i_{MB}(t) + \frac{N_s}{N_p} r_D i_{MB}(t)^2 \tag{3.67}$$

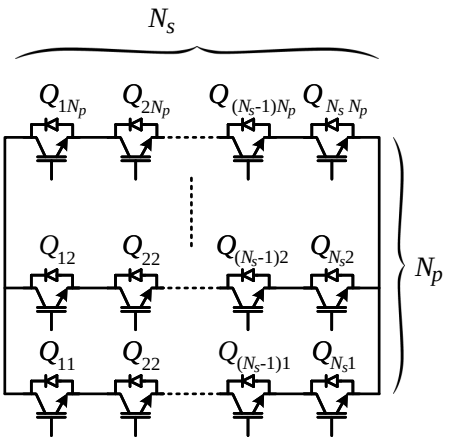


Figure 3.25: CRCB fault current interruption process.

3.3.4 *Bipolar System*

In bipolar HVdc configuration, three types of fault should be taken into account: pole-to-ground, pole-to-pole and pole-to-pole-to-ground faults. Pole-to-ground fault in one pole of bipolar system is similar to

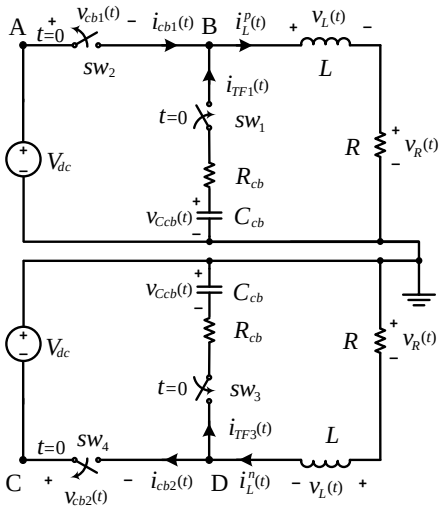


Figure 3.26: Equivalent circuit of the bipole HVdc system during Pole-to-pole-to-ground short circuit fault.

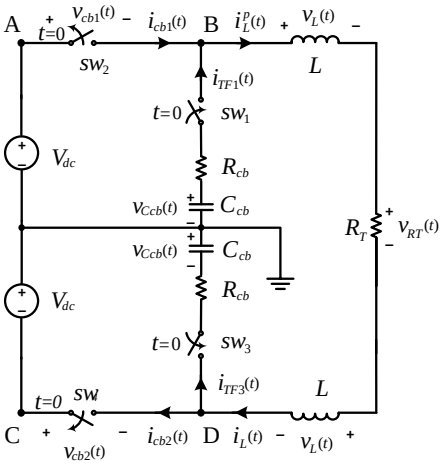


Figure 3.27: Equivalent circuit of the bipole HVdc system during Pole-to-pole short circuit fault.

the pole-to-ground fault in the asymmetric monopole system. Therefore, the analysis from section 3.3.2 is valid for the mentioned type of fault in bipolar HVdc systems. Fig. 3.26 shows the simplified equivalent circuit in presence of a low impedance pole-to-pole-to-ground short circuit fault in a bipolar configuration.

It can be seen in Figure 3.26 that the circuit can be analyzed as two independent circuits. Hence, the obtained equations in section 3.3.2 are also valid for this case. Figure 3.27 shows the simplified equivalent circuit of the bipolar system during a pole-to-pole fault. In this case after opening sw_2 and sw_4 and closing sw_1 and sw_3 the current of positive and the negative poles will be equal. The differential equation of the circuit can be given as:

$$\frac{\mathrm{d}^2 i_L^p(t)}{\mathrm{d}t^2} + \frac{(R_T + 2R_{cb})}{2L} \cdot \frac{\mathrm{d}i_L^p(t)}{\mathrm{d}t} + \frac{1}{2L\left(\frac{C_{cb}}{2}\right)} i_L^p(t) = 0 \tag{3.68}$$

where R_T represents the sum of high frequency resistance of faulted sections of two transmission lines and the fault resistance. Note that $2R >> R_T$ and hence R_T can be replaced by $2R_T$. Thereafter the differential equation can be rearranged as follows:

$$\frac{\mathrm{d}^2 i_L(t)}{\mathrm{d}t^2} + \frac{(R_T + R_{cb})}{L} \cdot \frac{\mathrm{d}i_L^p(t)}{\mathrm{d}t} + \frac{1}{L} i_L^p(t) = 0, \tag{3.69}$$

which is identical to (3.32). Therefore, the line current after interruption of a pole-to-pole short circuit fault in a bipolar configuration is similar to that of a monopole system. During interruption of a pole-to-pole fault because of simultaneous operation of the CRCBs in both poles of the system, the overall capacitance is divided by half and the overall resistance and also the inductance are doubled and the equations from subsection 3.3.2 are valid.

3.3.5 *Symmetric Monopole System*

The interruption of pole-to-ground fault in the symmetric monopole system is similar to that of the asymmetric monopole system. Therefore, the analysis from subsection 3.3.2 is valid for this type of fault in the symmetric monopole system. Moreover, the interruption of pole-to-pole and pole-to-pole-ground faults in symmetric monopole system are similar to interruption mentioned types of fault in the bipolar system. Thus, the analysis from subsection 3.3.4 is valid for the mentioned types of fault in the symmetric monopole systems.

3.4 *Detailed Design Process*

The sequential design process of the CRCB is illustrated in Figures 3.28 and 3.29.

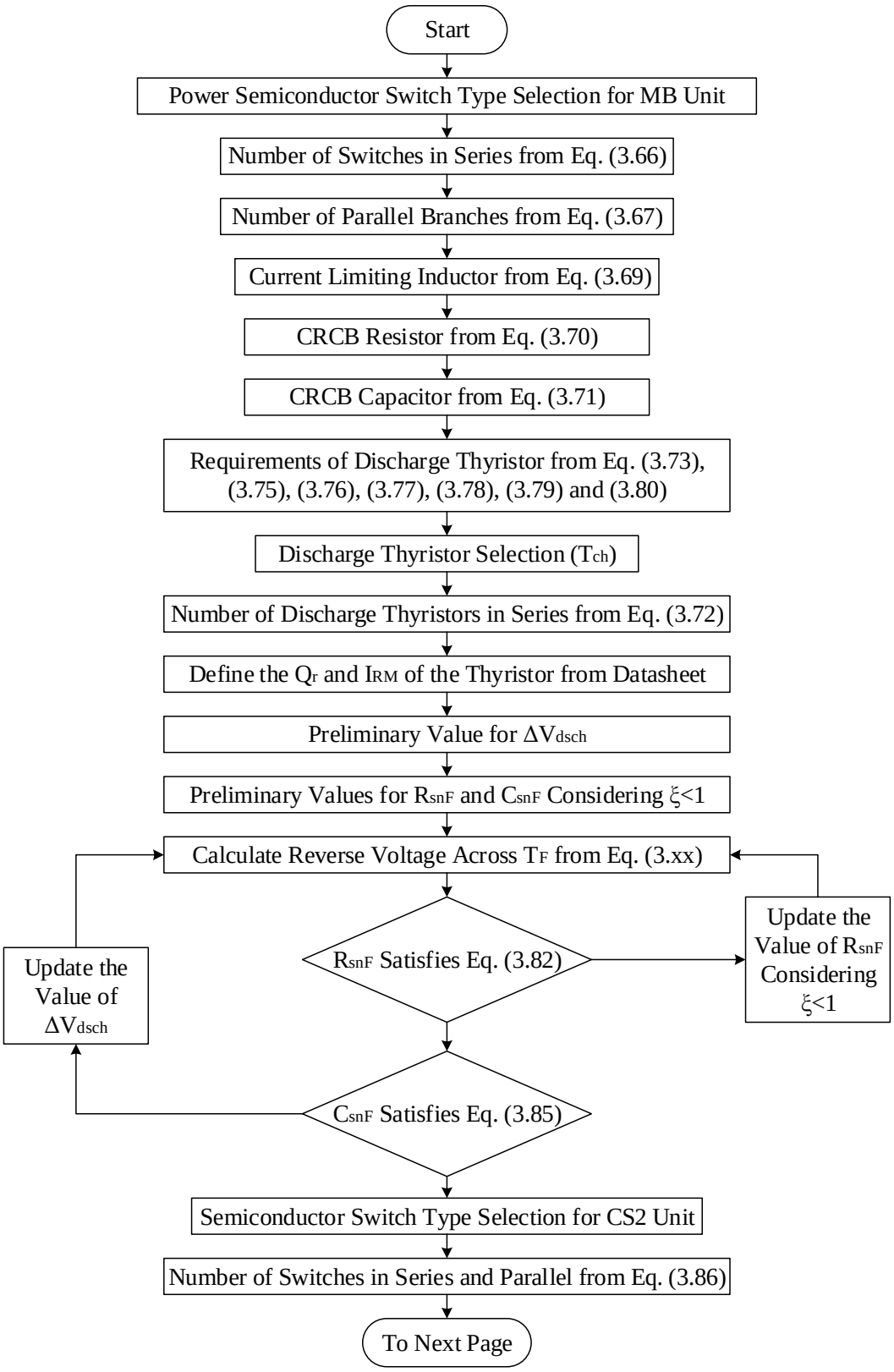


Figure 3.28: CRCB fault current interruption process.

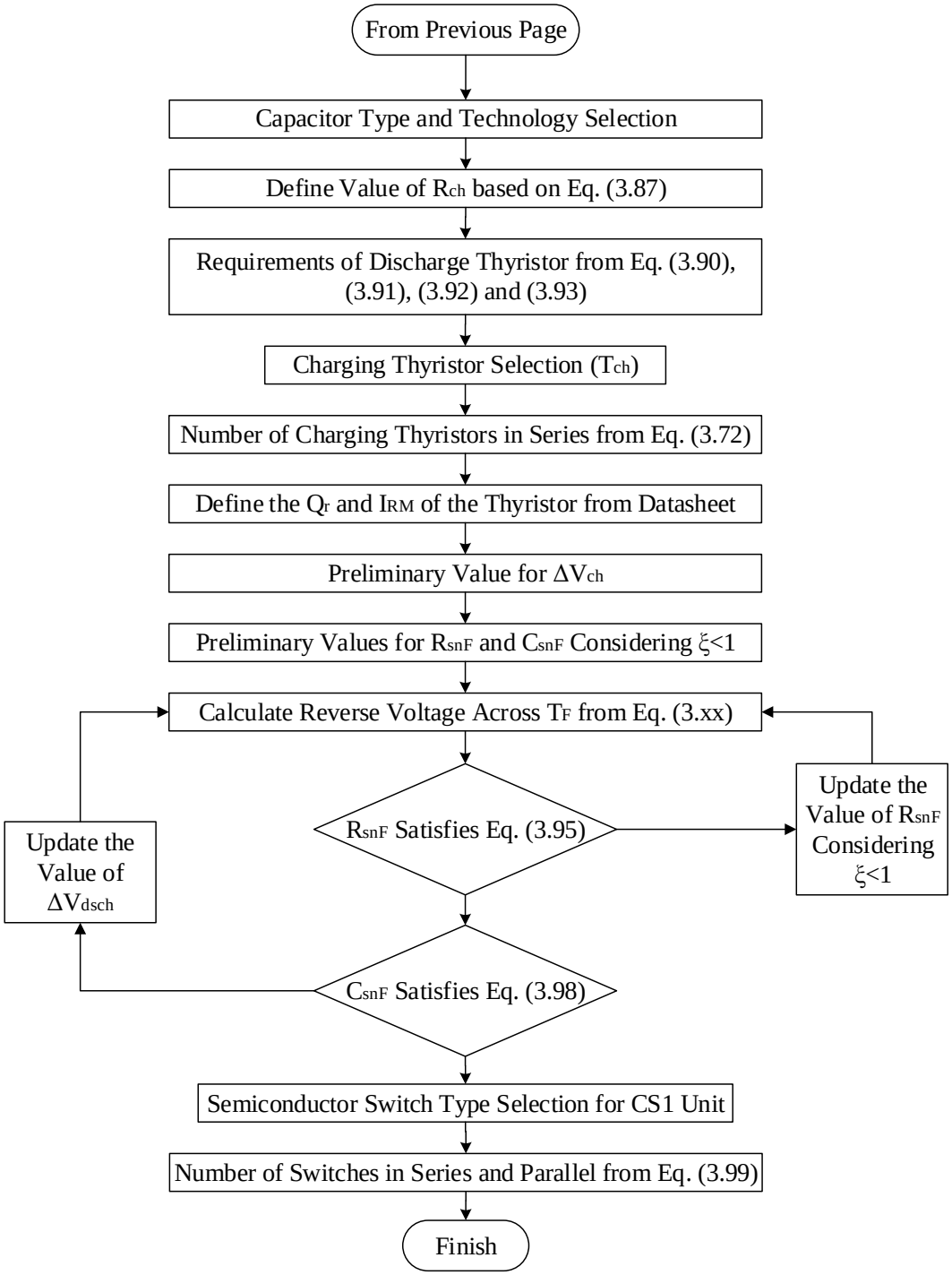


Figure 3.29: CRCB fault current interruption process

The CRCB can be designed based on the system parameters and design requirements. At the end of design process The designed parameters should be verified by detailed simulation model based on the detailed model of cable and the power converter. Table 3.2 illustrates the parameters and their descriptions that should be taken into the account in the design process of the CRCB. V_{dc}, I_n, TLL, L_L^{HF}, R_L^{HF} are the system related parameters. $T_{id0,max}$ is related to the protection relay performance and represents the maximum possible

time for generating a trip signal for a fault on transmission line with 0 km distance from the dc bus. Note that $T_{id0,max}$ includes the fault detection, signal processing and sensor delay times. TIV_{max} and $I_{br,max}$ are the design requirements.

Parameter	Description
V_{dc}	System nominal voltage
I_n	System nominal current
TLL	Transmission line length
L_L^{HF}	Transmission line lumped inductance per kilometer in high frequency
R_L^{HF}	Transmission line lumped resistance per kilometer in high frequency
$T_{id0,max}$	Maximum trip signal generation time for fault with 0 km distance
TIV_{max}	Maximum TIV across the MB unit of CRCB in per unit
$I_{br,max}$	Maximum current breaking capability of the CRCB

Table 3.2: The CRCB design requirements and system parameters.

3.4.1 MB Unit

Firstly, the semiconductor switch type must be chosen. As mentioned, IGBTs ad IGCTs are most common components to be applied in the dcCBs implementation. However, other types of fast gate controlled devices would be potential candidates to be employed in the implementation of CRCB. The most important parameters of powers semiconductor devices are listed in the Table (3.3).

Parameter	Description
V_{CES}	Collector-emitter break down voltage
$I_{c,nom}$	Collector-emitter continuous dc current
r_c	Collector-emitter on-state resistance
V_{T0}	Collector-emitter zero current threshold voltage
I_{sc}	Collector-emitter short circuit current
I_{CRM}	Repetitive peak collector current
I_F	Continuous dc forward current (though antiparallel diode)
I_{FRM}	Repetitive peak forward current (though antiparallel diode)
I^2t	I^2t value
$V_{CE,D}$	Collector-emitter dc stability voltage

Table 3.3: The CRCB design requirements and system parameters.

In addition to the blocking voltage and current capabilities, V_{T0} and r_C can be listed as two important parameters in selecting the semiconductor switch type in the the SSCB implementation. For a given collector-emitter voltage, the devices with lower V_{T0} and lower on-state collector-emitter resistance are expected to have less power losses. V_{T0} and on-state collector-emitter resistance are not directly accessible from the datasheet numerical information due to their dependency on the gate-emitter voltage. These two parameters can be obtained by evaluating $I_C - V_{CE}$ curve in the power semiconductor switch datasheet. Figure 3.30 shows a typical $I_C - V_{CE}$ curve for an IGBT. Depending on the gate-emitter voltage the collector-emitter voltage can have different values for specific current level. r_c can be

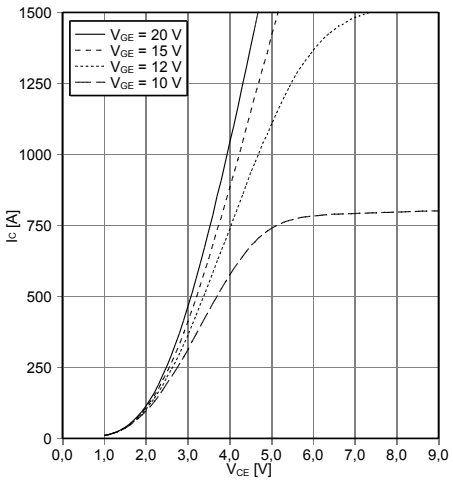


Figure 3.30: Typical $I_C - V_{CE}$ curve [206].

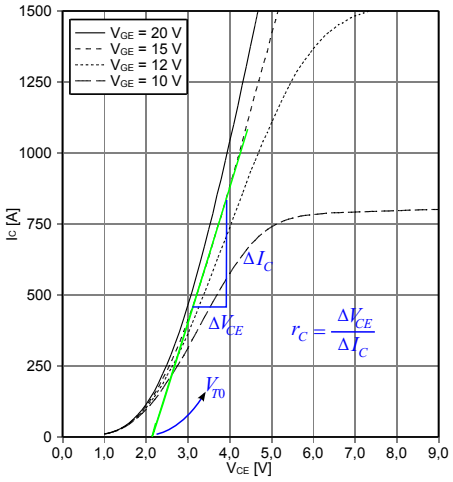


Figure 3.31: Typical $I_C - V_{CE}$ curve [205,206].

[8] Failures in Time (FIT) is a standard industry value defined as the device failure rate per billion hours [208].

estimated by evaluating the slope of the corresponding gate voltage curve in its linear area [205]. Figure 3.31 illustrate the application of this method. As can be seen in Figure 3.31, the line, which was used for defining r_c can be extended to reach V_{CE} axis to point out the value of V_{T0} [205].

The number of power switches in series connection in each branch of MB unit can be defined based on the maximum TIV requirement and the voltage capability of the power semiconductor switch. V_{CES} is the highest voltage that can be applied in any condition between the collector and emitter of the device. Any exceeding voltage may cause device permanent damage due to the break-down [207]. Therefore, V_{CES} cannot be applied in design of the MB unit. $V_{CE,D}$ represents the collector-emitter dc stability voltage and typically is given for 100 FIT [8] Typically, the collector-emitter dc stability voltage lies in the range of 0.5-0.6 of collector-emitter break-down voltage. Therefore, the number of IGBTs in series connection can be obtained based on the following Equation:

$$N_s = \left\lceil \frac{TIV_{max} \cdot V_{dc}}{V_{CE,dc}} \right\rceil \tag{3.70}$$

where, $\lceil\rceil$ represents the ceiling function. $\lceil x \rceil$ is equal to the smallest integer greater than or equal to x. The number of parallel branches should be defined considering the most sever scenario from current magnitude and detection time points of view. The most sever case happens when a fault happens at the other end of the transmission line and is not detected by the protection relay. In this case the fault current increases until it reaches the CRCB maximum current breaking capability. When $I_{br,max}$ threshold is reached, the CRCB opens independently from the protection system. Therefore, in this scenario the current is increasing up to $I_{br,max}$ level in a relatively long period of time. Depending on the transmission line characteristics this time period may reach few milliseconds. I_{sc} represents the collector-emitter short circuit current and usually is given for a time period less than 10 μs. If the current exceeds this value for a time period longer than 10 μs, the power semiconductor switch may face turn-off failure and consequently permanent damage. The overcurrent period in a dc system can be larger than this short time period. Therefore, the current breaking capability of the CRCB cannot be defined based on the mentioned value. I_{CRM} represents the maximum repetitive forward current in the IGBT. Typically, I_{CRM} is given for a pulse with duration of 1 ms. Therefore, I_{CRM} also cannot be suitable for defining the number of parallel branches. The safest method is to use the continuous collector-emitter nominal dc current value to define the number of parallel branches as follows:

$$N_p = \left\lceil \frac{I_{br,max}}{I_{cn}} \right\rceil \tag{3.71}$$

3.4.2 Current Limiting Inductor

The largest rate of rise of current occurs when a fault happens very close to the circuit breaker. In this case the fault can exceed the maximum current breaking capability of the CRCB very quickly even before it is detected by either the protection relay or the CRCB internal protection unit. Therefore, L_{cb} is included in the topology of the CRCB as the current limiting inductor in order to limit the rate of rise of fault current. The size of current limiting inductor can be defined by considering the maximum zero distance fault identification time ($T_{id0,max}$) and the voltage level. Assume that a short circuit fault happens in a location with 0 km distance to the CRCB. The maximum rate of rise of current in the MB unit of the CRCB can be given by:

$$\frac{\mathrm{d}i_{f,max}}{\mathrm{d}t} = \frac{V_{dc}}{L_{cb}} \tag{3.72}$$

Equation (3.72) gives the maximum current derivative since in practice the dc bus voltage drops during the short circuit fault conditions. In case of MMC based system due to the absence of large capacitor at the dc side of converter and the presence relatively large arm inductors, the system inductance will be larger than L_{cb}. The current limiting inductor should be sized in order to limit the value of fault current below the maximum current breaking capability of the CRCB for the faults with 0 km distance. Therefore, we have:

$$L_{cb} = \frac{V_{dc} T_{id0,max}}{m_1 I_{br,max} - I_n}; \quad 0.6 < m_1 < 1 \tag{3.73}$$

where, m_1 is introduced as a design constant. If m_1 is selected to be equal to 1, the current limiting inductor will limit the value of fault current to the maximum current breaking capability of the CRCB during the maximum zero distance fault detection time.

3.4.3 Discharging Branch

Discharging branch consists of one thyristor bank, a resistor, an inductor and a gate controlled semiconductor switch and its snubber circuit.

Resistor R_{cb}

R_{cb} should be designed in order to provide the system with discharging current with a peak larger than the maximum current breaking capability of the CRCB. Therefore the acceptable range for R_{cb} can be given as:

$$R_{cb} = \frac{V_{Ccb0}}{m_2 I_{br.max}}; \quad 1 < m_2 < 1.1 \tag{3.74}$$

where m_2 is introduced as a design constant and V_{Ccb0} is the capacitor C_{cb} voltage level after it is fully charged. Both m_2 and V_{Ccb0} must be selected at this stage of design.

Capacitor C_{cb}

After calculating the resistor value, the minimum value of CRCB can be obtained. The capacitor should be sized in order to keep the fault interruption circuit in the over-damped regime in any condition. As can be found out from Equation (3.33), for a given value of C_{cb} the damping factor increases by increasing the circuit resistance and also it increases by reducing the value of system inductance. The smallest ξ for a given value of C_{cb} happens when the circuit resistance has its lowest value and the inductance has its largest value. This case happens when a short circuit fault with 0 Ω occurs at the far end of the line. Therefore, the acceptable range for the value of C_{cb} to have $\xi > 1$ in all fault scenarios can be obtained as follows:

$$\xi > 1 \Rightarrow C_{cb} > \frac{4\left(L_{cb} + TLL \cdot L_L^{HF}\right)}{R_{cb}^2} \tag{3.75}$$

Thyristor T_F and Inductor L_T

The most relevant parameters in selecting the thyristor are listed and described in Table (3.4).

Table 3.4: The CRCB design requirements and system parameters.

Parameter	Description
V_{DWM}	Maximum working forward voltage
V_{RWM}	Maximum working reverse voltage
I_{TSM}	Surge current
I^2t	I^2t value
$\left(\frac{di_T}{dt}\right)_{cr}$	Critical rate of rise of on-state current
$\left(\frac{dv_D}{dt}\right)_{cr}$	Critical rate of rise of off-state voltage
t_q	Circuit commutated turn-off time

T_F must be able to withstand under the system nominal voltage. Therefore its V_{DWM} and V_{RWM} must be higher than the system voltage level. In some cases, the off-state dc voltage of the thyristor is given by the manufacturer, which can be used as the reference for selecting the thyristor for dc applications. However, V_{DWM} and V_{RWM} of the selected thyristor should lie in range of $1.35V_{dc}$ to $1.5V_{dc}$. The commercial high power thyristors are available up to 12 kV[9] operating forward and reverse voltage levels. Therefore, in HVdc systems the thyristors will be connected in series to withstand under the high voltage. The number of required thyristors for series connection can be given as follows:

[9] FT1500AU-240 from Mitsubishi is an example of 12 kV general purpose thyristor [209].

$$N_{TF,s} = \left\lceil \frac{m_3 V_{dc}}{V_{DWM}} \right\rceil; \quad 1.35 < m_3 < 1.5 \tag{3.76}$$

T_F is used to discharge the CRCB capacitor. Therefore, it must have sufficient surge current capability due to the initial high discharging current. I_{TSM} of the selected thyristor must be above the discharge current maximum value. The maximum value of current is given by Equation (3.42). $I_{L,max}$ depends upon the fault location and resistance,

interrupted current value and the capacitor voltage at the interruption instance. The largest $I_{L,max}$ happens when all the following conditions becomes valid:

- Short circuit fault resistance to be equal to 0 Ω.
- Fault occurs with 0 km distance to the CRCB.
- The capacitor to be fully charged at the interruption instance.
- The interrupted current to be equal to the maximum current interruption capability of the CRCB.

Therefore, the maximum possible current peak of the thyristor can be given as follows:

$$\begin{aligned}
I_{TF,max} &= k_1' \left(-\frac{k_1' s_1'}{k_1' s_1'} \right)^{\frac{s_1'}{s_2'-s_1'}} + k_2' \left(-\frac{k_1' s_1'}{k_2' s_2'} \right)^{\frac{s_2'}{s_2'-s_1'}} \\
s_1' &= \frac{-R_{cb}}{2L_{cb}} + \sqrt{\frac{R_{cb}^2}{4L_{cb}^2} - \frac{1}{L_{cb}C_{cb}}} \\
s_2' &= \frac{-R_{cb}}{2L_{cb}} - \sqrt{\frac{R_{cb}^2}{4L_{cb}^2} - \frac{1}{L_{cb}C_{cb}}} \\
k_1' &= \frac{1}{s_1' - s_2'} \left(\frac{V_{dc} - R_{cb} i_{max}}{L_{cb}} - s_2' I_{br,max} \right) \\
k_2' &= \frac{1}{s_2' - s_1'} \left(\frac{V_{dc} - R_{cb} i_{max}}{L_{cb}} - s_1' I_{br,max} \right)
\end{aligned} \tag{3.77}$$

Furthermore, T_F must have enough I^2t capability in order not to be overloaded during the discharging period. Typically, the I^2t value for the high power thyristors is given for a half sinusoid current waveform with either duration of $t_p = 8.3$ ms or $t_p = 10$ ms. The total I^2t value for all the discharging period can be derived using the current equation from Equation (3.34) as follows:

$$\int_0^\infty i_{TF}^2(t)\, dt = \frac{k_1^2}{2s_1} + \frac{2k_1k_2}{s_1+s_2} + \frac{k_2^2}{2s_2} \tag{3.78}$$

where k_1, k_2, s_1 and s_2 can be calculated from Equations (3.37), (3.38), (3.35) and (3.36), respectively. The discharging current always decreases upon the time. Therefore, the thyristor I^2t value must be evaluated for initial discharging time period equal to t_p from the manufacturer datasheet. The I^2t value for the time period equal to t_p can be given as:

$$\begin{aligned}
\int_0^{t_p} i_{TF}^2(t)\, dt = \frac{k_1^2}{2s_1}\left(e^{2s_1 t_p} - 1\right) + \frac{2k_1k_2}{s_1+s_2}\left(e^{(s_1+s_2)t_p} - 1\right) \\
+ \frac{k_2^2}{2s_2}\left(e^{2s_2 t_p} - 1\right)
\end{aligned} \tag{3.79}$$

Using Equations (3.77) and (3.79) the current capability criteria for T_F can be given as follows:

$$\begin{aligned}
I_{TSM} &> I_{TF,max} \\
I^2t &> \int_0^{t_p} i_{TF}^2(t)\, dt
\end{aligned} \tag{3.80}$$

In addition to the voltage and current capability of the thyristor its critical rate of rise for current and voltage must be considered. $\left(\frac{\mathrm{d}v_T}{\mathrm{d}t}\right)_{cr}$ is given for the rate of rise of voltage when the thyristor is turned off. The voltage across T_F increases when the capacitor is being charged. The rate of rise of voltage across the thyristor is equal to that of the capacitor. Using the capacitor voltage equation from (3.9) the maximum of thyristor voltage derivative can be given as by:

$$\left(\frac{\mathrm{d}v_T}{\mathrm{d}t}\right)_{max} = \frac{V_{dc}}{R_{ch}C_{cb}} \tag{3.81}$$

Therefore, the critical rate of rise of off-state voltage of the selected thyristor must be less than the maximum thyristor voltage derivative:

$$\left(\frac{\mathrm{d}v_T}{\mathrm{d}t}\right)_{cr} > \frac{V_{dc}}{R_{ch}C_{cb}} \tag{3.82}$$

T_F turns on at $t = t_{br}$. The rate of rise of current in T_F is limited by L_F at $t = t_{br}$. The maximum rate of rise of on-state current in the thyristor can be derived by considering point B in Figure (3.21) and its voltage equation from (3.39). The current derivative for $t = t_{br}^{+}$ can be given as follows:

$$\left(\frac{\mathrm{d}i_T}{\mathrm{d}t}\right)_{max} = \frac{V_{dc} - v_B\left(t_{br}\right)}{L_F} = \frac{V_{dc} - \left(k_1's_1' - k_2's_2'\right)L_{cb}}{L_F} \tag{3.83}$$

where, s_1', s_2', k_1' and k_2' can be calculated from Equation (3.77). Therefore, the critical rate of rise of on-state current of the selected thyristor must be less than the maximum thyristor current derivative:

$$\left(\frac{\mathrm{d}i_T}{\mathrm{d}t}\right)_{cr} > \frac{V_{dc} - \left(k_1's_1' - k_2's_2'\right)L_{cb}}{L_F} \tag{3.84}$$

The circuit commutated turn-off time of the thyristor should also be considered in the design process.

Q_F and its Snubber Circuit

As was previously mentioned the role of Q_F and its snubber circuit is to provide T_F with reverse voltage in order to completely turn it off. In addition to reverse voltage, the reverse recovery current of the thyristor must be supplied for sufficient period of time. A typical thyristor reverse recovery current curve is depicted in Figure (3.32). The thyristor turn off process has four phases including the first (t_{s1}) and the second (t_{s2}) storage times and the first (t_{f1}) and the second (t_{f2}) fall times [210]. The total thyristor turn-off time depends upon the thyristor forward current, gate voltage and hole lifetime in the n base. [210]. Typically, the maximum recovered charge (Q_r) and the peak reverse recovery current are given as a function of thyristor current derivative and the junction temperature by the manufacturer.

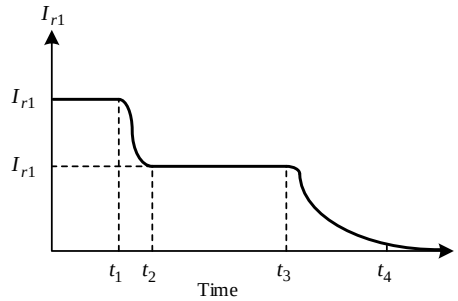


Figure 3.32: Typical curve for thyristor reverse recovery current [210].

The snubber circuit should be designed in order to provide the peak reverse recovery current of the thyristor and the recovered charge. As was explained in subsection 3.3.2 the current in thyristor reaches

zero at $t = t_1$, which is given by Equation (3.56). Using the current equation from (3.53), the current derivative when it reaches zero can be given as:

$$\frac{\mathrm{d}i_{TF}(t_1)}{\mathrm{d}t} = -\omega_d \sqrt{A^2 + B^2 - 2ABsin(\phi)} \cdot e^{-\alpha t_1} \tag{3.85}$$

where, A and B can be calculated from Equations (3.54) and (3.55). A typical curve of peak reverse recovery current vs thyristor current derivative is shown in Figure (3.33) [211]. After obtaining the current derivative from Equation (3.85), the value of peak reverse recovery current can be find from a similar curve to Figure (3.33) from the manufacturer datasheet.

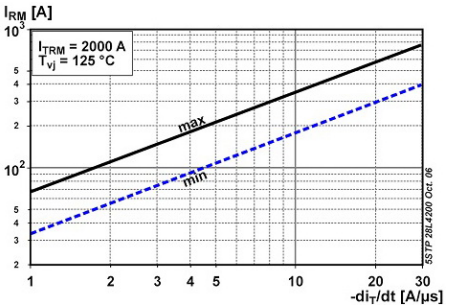


Figure 3.33: A typical curve for peak reverse recovery current [211]

This will set the first criteria in design of the snubber circuit. The sum of snubber and CRCB resistors must be low enough to provide the peak reverse recovery current. therefore, we have:

$$R_{snF} < \frac{v_{TF}(t_1^+)}{I_{RM}} - R_{cb} \tag{3.86}$$

where, I_{RM} is the peak reverse recovery current of the thyristor. After having the value of R_{snF}, C_{snF} should be selected in order to make the damping factor of the circuit quite smaller than one. Smaller ξ will increase the generated negative voltage across the thyristor. Therefore, we have:

$$\xi < 1 \Rightarrow \quad C_{snF} < \frac{4(L_{cb} + L_T)}{R_{cb}^2} \tag{3.87}$$

In addition to the damping factor criteria the capacitor should be Large enough to be able to provide the recovered charged during the turn-off process of the thyristor. Considering that C_{snF} is small enough against C_{cb}, we neglect the large C_{cb} capacitor since it is in series connection with C_{snF}. Therefore, the maximum charge can be supplied by the snubber circuit can be given as:

$$Q_{max} = C_{snF} \cdot v_{TF}(t_1^+) \tag{3.88}$$

where, $v_{TF}(t_1^+)$ is the voltage across the thyristor and can be calculated by Equation (3.62). Hence the following criteria must also be satisfied:

$$C_{snF} \cdot v_{TF}(t_1^+) > Q_r \tag{3.89}$$

where, Q_r is the recovered charge during the thyristor turn-off process. The recovered charge for a given current derivative can be found from the manufacturer datasheet for a thyristor. Figure (3.33) depicts a typical curve of recovered charge vs thyristor current derivative [211]. As was illustrated in subsection 3.3.2, v_{TF} despond on several parameters including C_{snF} and ΔV. In order to evaluate the Equation (3.89), the value of C_{snF} can be kept fixed and then a value for ΔV can be selected. Q_F can be realized by series and parallel connection of either high power IGBTs or IGCTs or GTOs. The current rating of Q_F should be equal to that of T_F. Therefore, the number of switches in parallel connection must be calculated considering the surge current

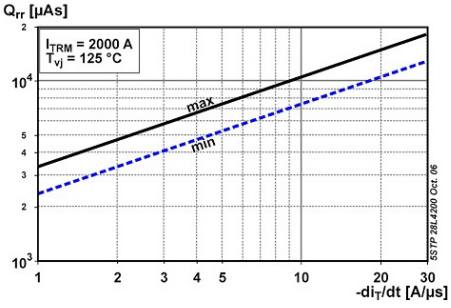


Figure 3.34: A typical curve of recovered charge vs thyristor current derivative [211].

rating of T_F. The number of switches in series can be found based on the voltage of C_{snF} at $t = t_1^+$. In case that Q_F is to be realized by IGBTs, the number of IGBTs in series and parallel connections can be given by:

$$\begin{aligned} N_{QF,s} &= \left\lceil \frac{v_{CsnF}\left(t_1^+\right)}{V_{CE,dc}} \right\rceil \\ N_{QF,p} &= \left\lceil \frac{I_{L,max}}{I_{cn}} \right\rceil \end{aligned} \tag{3.90}$$

The voltage rating of Q_{snF} is similar to that of Q_F. Therefore, the number of series switches can be found using the first equation in (3.90). However, the number of semiconductor switches in parallel connection considering the current capability of Q_{snF} can be obtained as follows:

$$N_{QsnF,p} = \left\lceil \frac{v_{CsnF}\left(t_1^+\right)}{R_{cb} I_{cn}} \right\rceil \tag{3.91}$$

3.4.4 Charging Branch

Charging branch consists of one thyristor bank, a resistor and a gate controlled semiconductor switch and its snubber circuit.

Resistor R_{ch1}

R_{ch1} should limit the peak of charging current below maximum allowed peak current. Typically, the capacitors have a large charging current peak. Hence, the charging current is limited by the allowed peak current from dc bus and power converter points of view. Assuming the allowed peak current equal to $I_{ch,max}$, R_{ch1} can be derived as follows:

$$R_{ch1} < \frac{m_4 V_{dc}}{I_{ch,max}}; \quad 1.1 < m_4 < 1.5 \tag{3.92}$$

where m_4 is a design factor to limit the charging current peak in range of 0.66 to 0.9 of $I_{ch,max}$. The first stage charging circuit time constant can be given as follows:

$$\tau_{ch} = R_{ch1} C_{cb} \tag{3.93}$$

The capacitor can be charged up to almost 99.315 % of system dc voltage after $5\tau_{ch}$ s.

Resistor R_{ch2} and Inductor L_{ch}

In the second charging stage, the charging current flows through R_{ch2} and L_{ch}. Both values affect the final value of capacitor voltage. R_{ch2} can be a very small resistance. Depending on the copper resistance of L_{ch}, R_{ch2} can be even eliminated from the circuit. The capacitor must be charged up to a voltage level higher than the system nominal voltage in order to grantee the successful commutation of the thyristors

in T_{ch1} and T_{ch2}. After selecting the value of R_{ch2} and using Equation (3.29), the value of L_{ch} can be obtained as follows:

$$L_{ch} = \frac{1}{4}\left(R_{ch}^2 C_{cb}\right)\left[\frac{\pi^2}{ln^2\left(\frac{V_T chT}{\Delta V}\right)} + 1\right] \tag{3.94}$$

Gate Controlled Switch Q_{ch}

similar to Q_F, Q_{ch} can be realized by series and parallel connection of either high power IGBTs or IGCTs or GTOs. The current rating of Q_{ch} should be equal to that of T_{ch1}. Therefore, the number of switches in parallel connection must be calculated considering the surge current rating of T_{ch1}. The number of switches in series can be found based on the voltage of L_{ch} at $t = t_1^+$. The voltage of L_{ch} at $t = t_1^+$ is equal to ΔV. In case that Q_{ch} is to be realized by IGBTs, the number of IGBTs in series and parallel can be given by:

$$\begin{aligned} N_{QF,s} &= \left\lceil \frac{\Delta V}{V_{CE,dc}} \right\rceil \\ N_{QF,p} &= \left\lceil \frac{I_{ch,max}}{I_{cn}} \right\rceil \end{aligned} \tag{3.95}$$

Thyristor T_{ch1}

T_{ch1} must be able to withstand under the system nominal voltage. Therefore its total V_{DWM} and V_{RWM} must be higher than the system voltage level. The number of thyristors in series can be calculated from Equation (3.76). The peak of charging current must be considered in selecting the thyristor. The total I^2t value for all the charging period can be derived using the current equation from Equations (3.9) and (3.13) as follows:

$$\int_0^\infty i_{Tch}^2(t)\,dt = \int_0^{t_1} i_{ch1}^2(t)\,dt + \int_{t_1}^{t_1+\frac{\pi}{\omega_d}} i_{ch2}^2(t)\,dt \tag{3.96}$$

where t_1 represents the time when the second charging stage starts and can be calculated as follows:

$$t_1 = -R_{ch1}C_{cb} \cdot ln\frac{i_{th2}R_{ch1}}{V_{dc}} \tag{3.97}$$

Using Equations (3.96) and (3.97), the total I^2t value can be given as follows:

$$\begin{aligned} \int_0^\infty i_{Tch}^2(t)\,dt =& \frac{V_{dc}^2 C_{cb}}{2R_{ch1}} - \frac{i_{th}^2 C_{cb} R_{ch1}}{2} \\ &+ \frac{\Delta V^2}{L_{ch}^2\omega_d^2}\left(\frac{2\alpha}{4\alpha^2 + 4\omega_d^2} - \frac{1}{4\alpha}\right)\left(e^{\frac{-2\alpha\pi}{\omega_d}} - 1\right) \end{aligned} \tag{3.98}$$

The charging current always decreases upon the time. Therefore, the thyristor I^2t value must be evaluated for initial discharging time period equal to t_p from the manufacturer datasheet. The I^2t value for the time period equal to t_p can be given as:

$$\int_0^{t_p} i_{Tch}^2(t)\,dt = \frac{V_{dc}^2 C_{cb}}{2R_{ch}}\left(e^{-\frac{2t_p}{R_{ch}C_{cb}}} - 1\right) \tag{3.99}$$

Using Equation (3.99) and the peak of charging current, the current capability criteria for T_{ch} can be given as follows:

$$\begin{aligned} I_{TSM} &> I_{ch,max} \\ I^2t &> \int_0^{t_p} i_{Tch}^2(t)\,dt \end{aligned} \tag{3.100}$$

The voltage across T_{ch1} increases when the capacitor is being discharged. The rate of rise of voltage across the thyristor is equal to the rate of decrease of voltage in the capacitor. Using the capacitor voltage equation from (3.9) the maximum of thyristor voltage derivative can be given as by:

$$\left(\frac{\mathrm{d}v_T}{\mathrm{d}t}\right)_{max} = -\frac{k_1+k_2}{2N_{Tch1,s}C_{cb}} \tag{3.101}$$

where, k_1 and k_2 can be calculated from Equations (3.37) and (3.38), respectively and $N_{Tch1,s}$ represents the number of thyristors in series connection. Therefore, the critical rate of rise of off-state voltage of the selected thyristor must be less than the maximum thyristor voltage derivative:

$$\left(\frac{\mathrm{d}v_T}{\mathrm{d}t}\right)_{cr} > -\frac{k_1+k_2}{2N_{Tch1,s}C_{cb}} \tag{3.102}$$

Due the presence of arm inductors in MMC based HVdc systems [40], additional current derivate limiting inductor is not required in the charging branch. The maximum rate of rise of on-state current in the thyristor can be derived by considering the equivalent inductance of system till point of common connection [46].

Thyristor T_{ch2}

As mentioned, T_{ch2} is triggered in the second charging stage. The voltage rating of T_{ch2} should be higher than the system nominal voltage. Therefore its total V_{DWM} and V_{RWM} must be higher than the system voltage level. The number of thyristors in series can be calculated from Equation (3.76). The peak of charging current in the second stage should also be considered in selecting the thyristors for T_{ch2}. The total I^2t value for T_{ch2} can be obtained using the current equation from Equation (3.13) as follows:

$$\begin{aligned} \int_0^{\infty} i_{Tch}^2(t)\,dt &= \int_0^{\frac{\pi}{\omega_d}} \frac{\Delta V^2}{L_{ch}^2\omega_d^2} e^{-2\alpha t} sin^2(\omega_d t)\,dt \\ &= \frac{\Delta V^2}{L_{ch}^2\omega_d^2}\left(\frac{2\alpha}{4\alpha^2+4\omega_d^2} - \frac{1}{4\alpha}\right)\left(e^{\frac{-2\alpha\pi}{\omega_d}} - 1\right) \end{aligned} \tag{3.103}$$

Similar to the previous case, the thyristor I^2t value must be evaluated for initial discharging time period equal to t_p from the manufacturer datasheet. The current peak in T_{ch2} can be derived as follows:

$$I_{Tch2max} = \frac{\Delta V}{L_{ch}\omega_d} e^{\frac{-\alpha\pi}{2\omega_d}} \tag{3.104}$$

Using Equations (3.99) and (3.104) the current capability criteria for T_{ch2} can be given as follows:

$$\begin{aligned} I_{TSM} &> I_{Tch2max} \\ I^2t &> \int_0^{t_p} i_{Tch2}^2(t)\,dt \end{aligned} \tag{3.105}$$

The voltage across T_{ch1} increases when the capacitor is being discharged. The rate of rise of voltage across the thyristor is equal to the rate of decrease of voltage in the capacitor. Using the capacitor voltage equation from (3.9) the maximum of thyristor voltage derivative can be given as by:

$$\left(\frac{\mathrm{d}v_T}{\mathrm{d}t}\right)_{max} = -\frac{k_1 + k_2}{2N_{Tch2,s}C_{cb}} \tag{3.106}$$

where, k_1 and k_2 can be calculated from Equations (3.37) and (3.38), respectively and $N_{Tch2,s}$ represents the number of thyristors in series connection. Therefore, the critical rate of rise of off-state voltage of the selected thyristor must be less than the maximum thyristor voltage derivative:

$$\left(\frac{\mathrm{d}v_T}{\mathrm{d}t}\right)_{cr} > -\frac{k_1 + k_2}{2N_{Tch2,s}C_{cb}} \tag{3.107}$$

3.5 Computational Analysis

Computational analysis includes three main subsections:

- Verification of the most relevant equations from subsection 3.3
- Computational analysis of a conceptual design example based on the developed equation in subsection 3.3.
- Computational analysis of mentioned conceptual design example based on the detailed model of system.

3.5.1 Verification

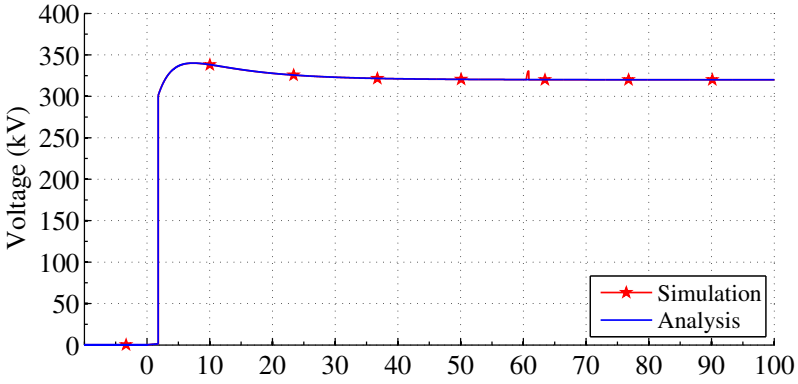
The CRCB voltage and the line current equations from subsection 3.3 are the main equations that the CRCB can be design based on them. The verification of mentioned equations are done using ten sets of preliminary values for the main parameters of CRCB. Table 3.5 illustrates the randomly selected values for the CRCb parameters.

Table 3.5: Preliminary values for equations verification study.

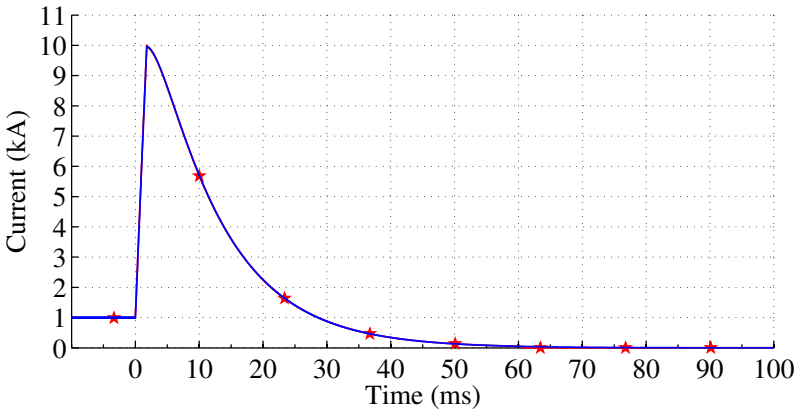
Set Number	L_{cb}	**Fault Location**	R_f	C_{cb}	R_{cb}	i_{br, max}
1	50 mH	100 km	0 Ω	400 μF	30 Ω	10 kA
2	100 mH	100 km	0 Ω	1000 μF	40 Ω	5 kA
3	40 mH	0 km	10 Ω	500 μF	100 Ω	3 kA
4	20 mH	50 km	2 Ω	200 μF	20 Ω	5 kA
5	10 mH	80 km	10 Ω	100 μF	20 Ω	6 kA
6	60 mH	70 km	1 Ω	2000 μF	18 Ω	15 kA
7	70 mH	40 km	0 Ω	1000 μF	20 Ω	13 kA
8	30 mH	20 km	1 Ω	50 μF	40 Ω	6 kA
9	70 mH	20 km	5 Ω	600 μF	50 Ω	7 kA
10	90 mH	0 km	0 Ω	1500 μF	40 Ω	7 kA

The voltage and current waveforms obtained from the simulation of developed model and its analysis are compared in Figures 3.35, 3.36, 3.37, 3.38, 3.39, 3.40, 3.41, 3.42, 3.43 and 3.44. As can be seen in the figures, in all the cases the current and voltage waveforms plotted using the equations from previous subsection accurately fit to the voltage and current waveforms obtained by simulation.

Figure 3.35: (a) Voltage and (b) current waveforms for set 1.

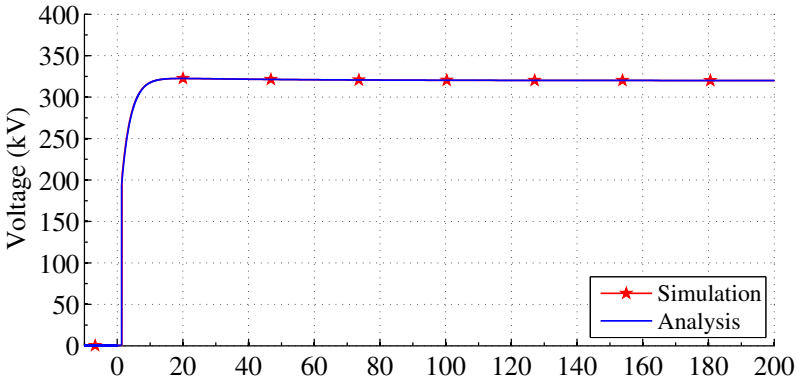


(a) Voltage across the MB unit

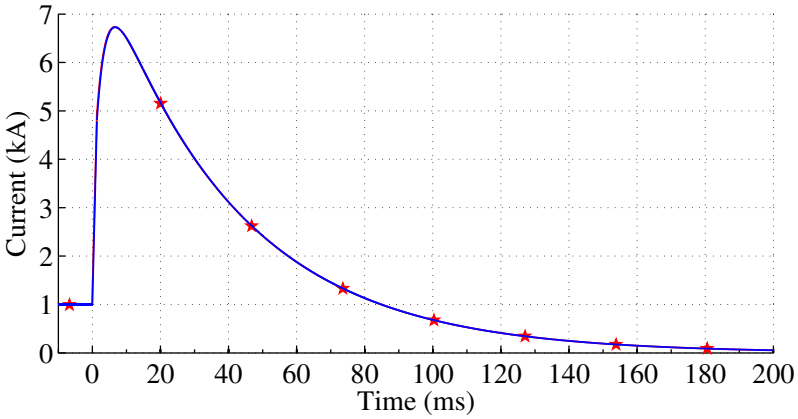


(b) Line current before and after fault occurence

Figure 3.36: (a) Voltage and (b) current waveforms for set 2.

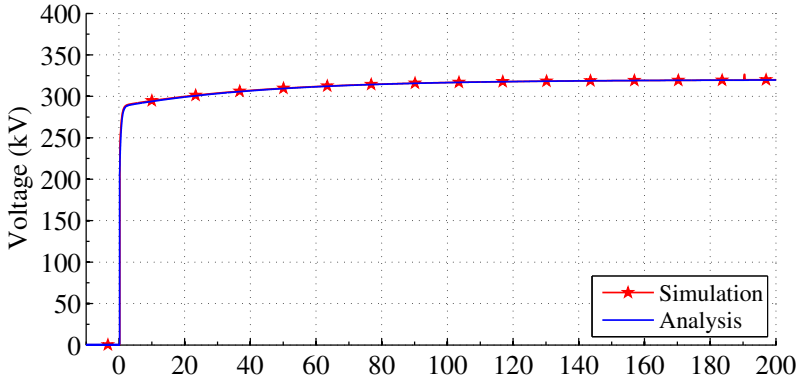


(a) Voltage across the MB unit

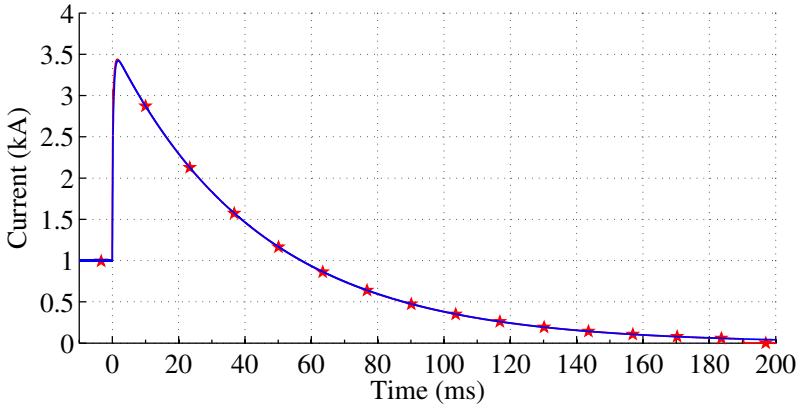


(b) Line current before and after fault occurence

Figure 3.37: (a) Voltage and (b) current waveforms for set 3.

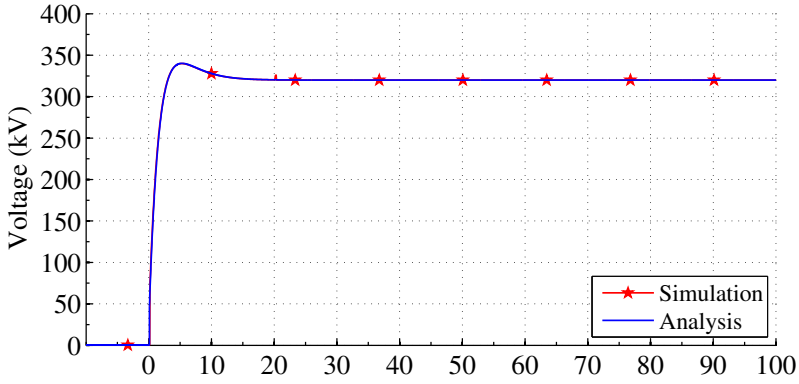


(a) Voltage across the MB unit

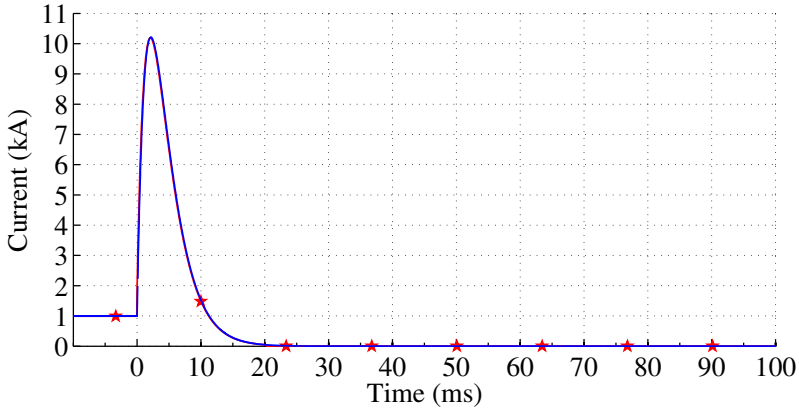


(b) Line current before and after fault occurence

Figure 3.38: (a) Voltage and (b) current waveforms for set 4.

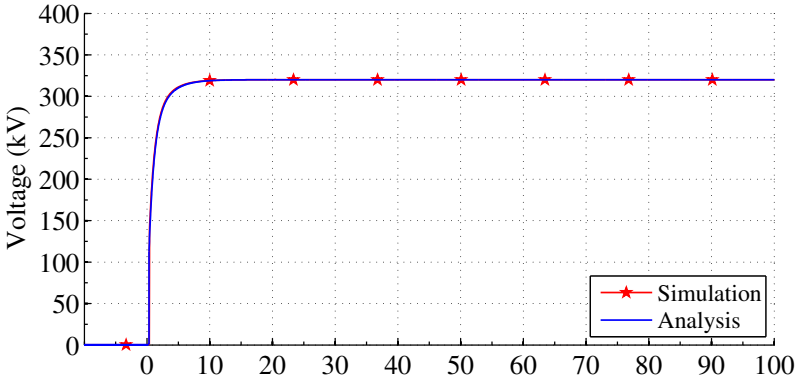


(a) Voltage across the MB unit

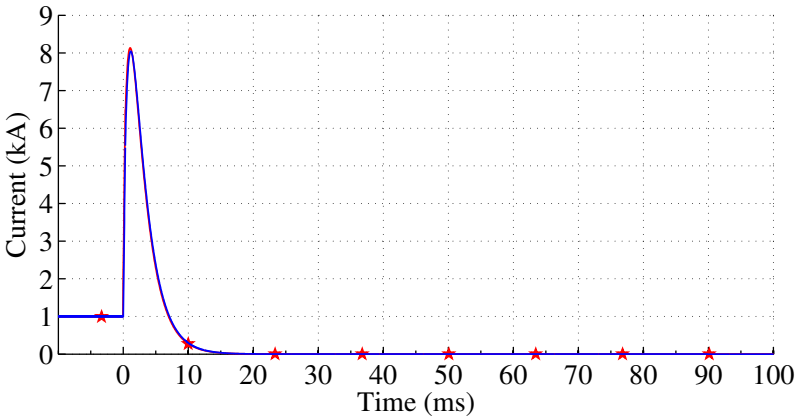


(b) Line current before and after fault occurence

Figure 3.39: (a) Voltage and (b) current waveforms for set 5.

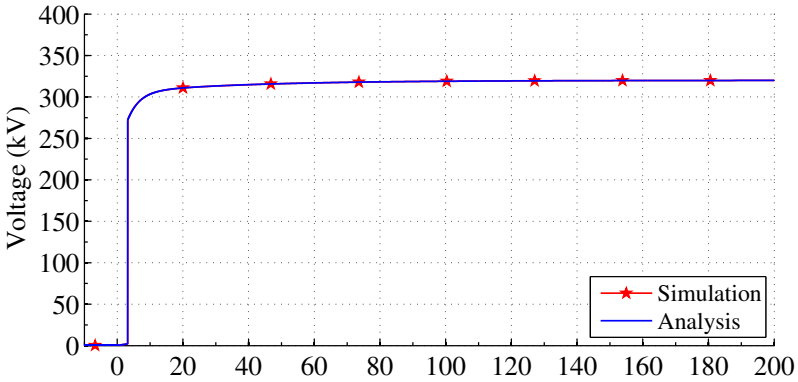


(a) Voltage across the MB unit

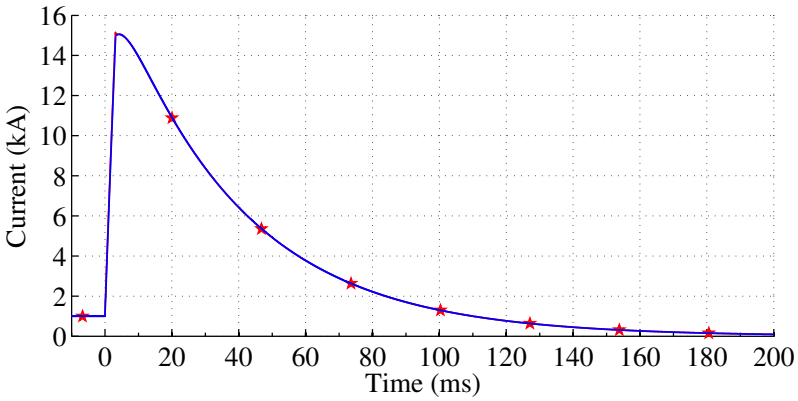


(b) Line current before and after fault occurence

Figure 3.40: (a) Voltage and (b) current waveforms for set 6.

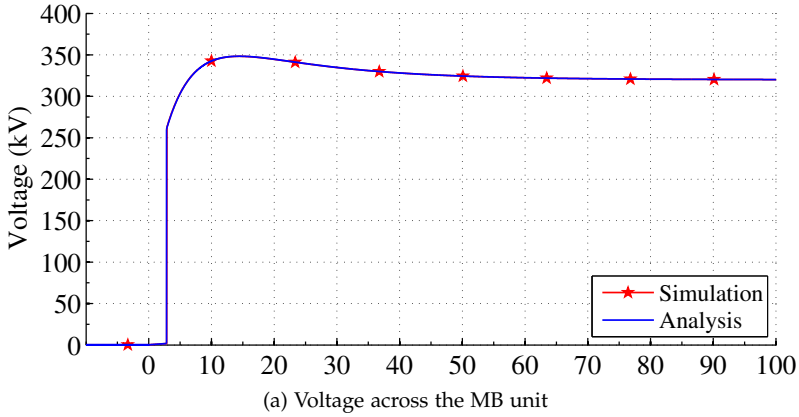


(a) Voltage across the MB unit

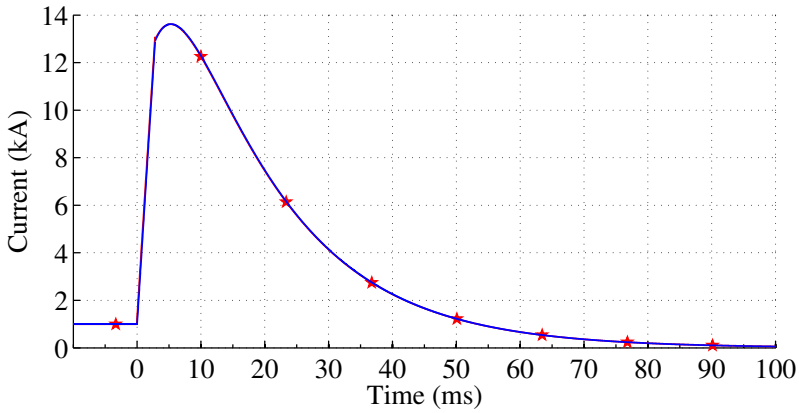


(b) Line current before and after fault occurence

Figure 3.41: (a) Voltage and (b) current waveforms for set 7.

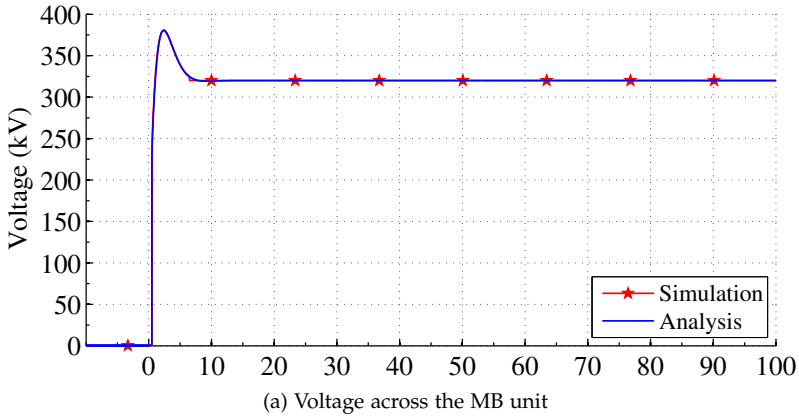


(a) Voltage across the MB unit

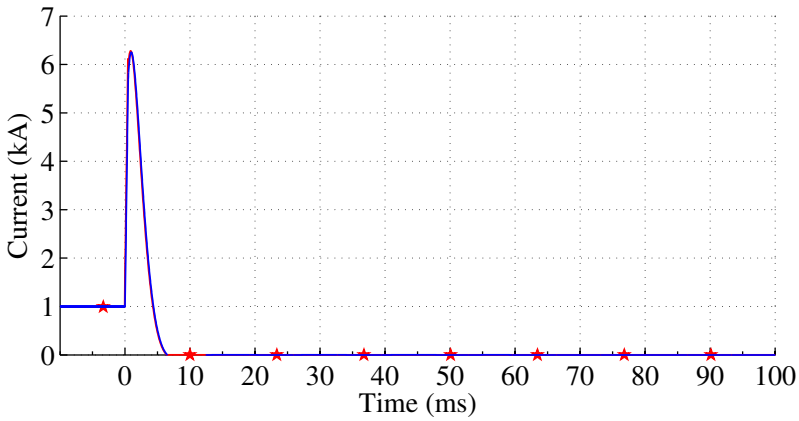


(b) Line current before and after fault occurence

Figure 3.42: (a) Voltage and (b) current waveforms for set 8.

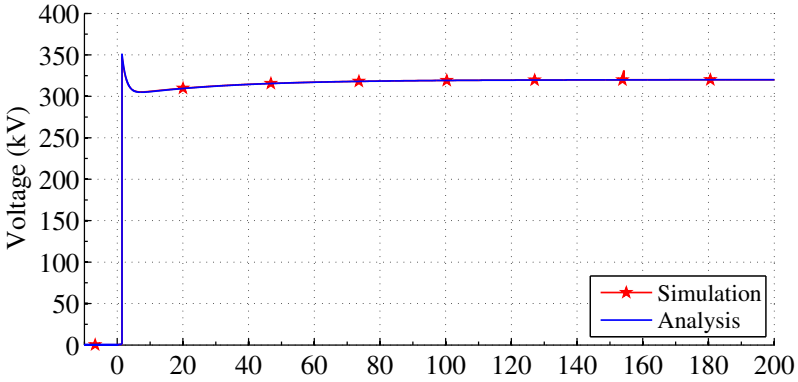


(a) Voltage across the MB unit

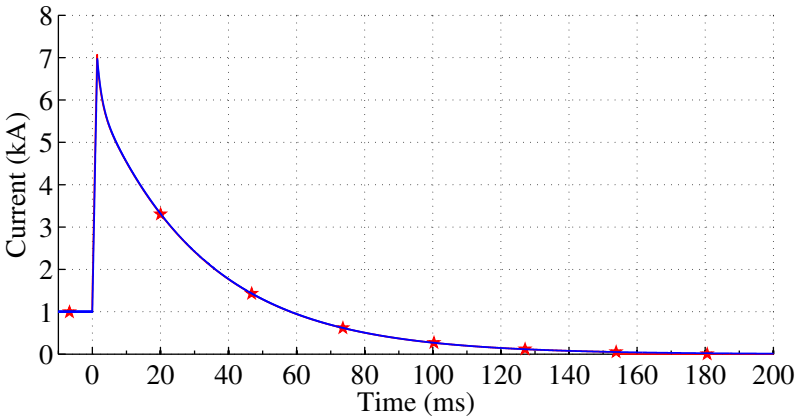


(b) Line current before and after fault occurence

Figure 3.43: (a) Voltage and (b) current waveforms for set 9.

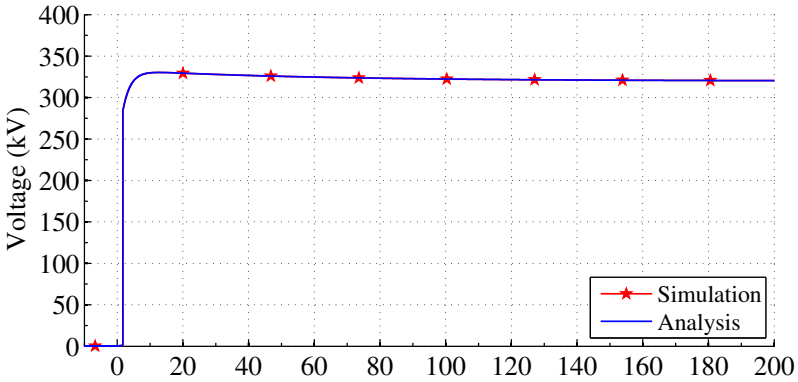


(a) Voltage across the MB unit

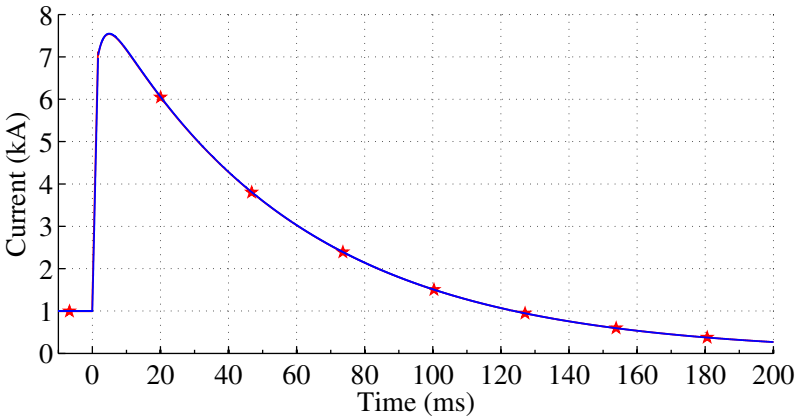


(b) Line current before and after fault occurence

Figure 3.44: (a) Voltage and (b) current waveforms for set 10



(a) Voltage across the MB unit



(b) Line current before and after fault occurence

3.5.2 *Conceptual Design Example*

A CRCB is designed based on the analysis and design remarks from sections 3.3 and 3.4 and then the impacts of variation in different parameters on behavior of the CRCB investigated through sensitivity analysis of the relevant parameters.

Design Case

Table 3.6 illustrates the case study system parameters and the CRCB design requirements.

Table 3.6: Conceptual design example parameters and requirements.

Parameter	Description	Value
V_{dc}	System nominal voltage	320 kV
I_n	System nominal current	1 kA
TLL	Transmission line length	100 km
L_L	Transmission line inductance per kilometer	2.9 mH/km
R_L	Transmission line resistance per kilometer	10 mΩ/km
L_L^{HF}	Transmission line high frequency inductance per kilometer	0.11 mH/km
R_L^{HF}	Transmission line high frequency resistance per kilometer	23 mΩ/km
$T_{id0,max}$	Maximum zero distance fault identification time	1 ms
$I_{ch,max}$	Maximum allowed charging current	1.8 kA
TIV_{max}	Maximum TIV across the MB unit of CRCB	1.15 pu
$I_{br,max}$	Maximum current breaking capability of the CRCB	10 kA

L_L, R_L, L_L^{HF} and L_L^{HF} are obtained using PSCAD line constant program [187] for an XLPE insulated HVdc cable. The cross-section and parameters of HVdc cable are illustrated in Figure 3.45 and Table 3.7, respectively [212].

Table 3.7: dc cable data.

Layer	Radius (mm)	Resistivity (Ωm)	Rel. permeability	Rel. permittivity
(1) Core	25.2	1.72×10^{-8}	1	1
(2) Insulator	40.2	-	1	2.3
(3) Sheath	43.0	2.20×10^{-7}	1	1
(4) Insulator	48.0	-	1	2.3
(5) Armor	53.0	1.80×10^{-7}	10	1
(6) Insulator	57.0	-	1	2.1

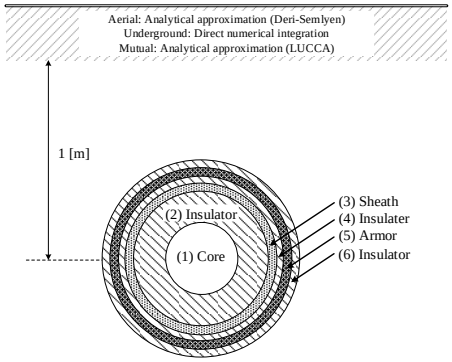


Figure 3.45: XLPE cable cross-section [212].

The value of current limiting inductor is obtained using (3.73) and set to 50 mH. FZ750R65KE3 as one of the commercial IGBTs with highest available blocking voltage is selected. Based on the TIV and maximum current requirements from Table 3.6, the number of IGBTs in series and parallel branches are calculated as 97 and 14, respectively from the (3.70) and (3.71). Based on (3.74) and assuming $V_{C0} = 320$ kV, R_L should be smaller than 32 Ω. By selecting 30 Ω as the value of R_L, the marginal value of C_{cb} can be calculated from (3.75). The minimum value of C_{cb} is obtained as 238.28 μF. Figure 3.46 depicts the damping factor of equivalent circuit for different values of resistor and capacitor around obtained values. The red dashed line represents the criteria set by (3.72). Point A illustrates the coordination of $R_{cb} = 30$ Ω and the obtained marginal value for C_{cb}. In order to satisfy the TIV

requirement of this design case the value of C_{cb} can be selected as 400 μF, which is shown by point B in Figure 3.46. As can be seen in the figure the TIV is expected to lie in the range of 1.08-1.12 pu.

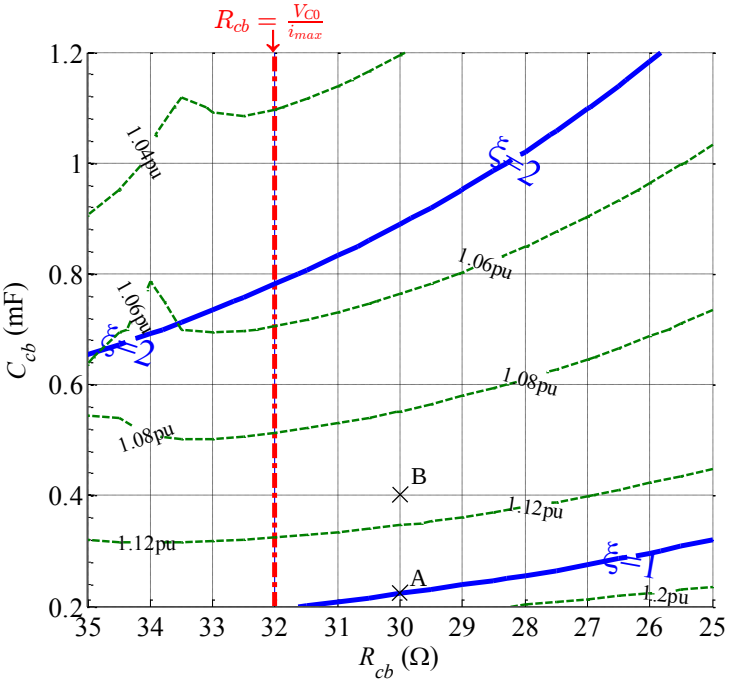


Figure 3.46: Design area considering the circuit damping factor.

Considering the value of maximum allowed charging current from Table 3.6, R_{ch1} can be calculated as 200 Ω using Equation (3.92). Note that the design factor m_4 is set to 1.13. R_{ch2} can be set to 5 Ω and consequently the value of L_{ch} can be calculated as 100 mH. Furthermore, the I^2t value for T_{ch1} for $t_p = 10$ ms can be calculated as 22.7 kA^2s. The total I^2t value for the charging stage can be obtained as 100.75 kA^2s. The maximum current in T_{ch2} can be calculated as 948 A while its I^2t value for $t_p = 10$ is equal to 8.40 kA^2s.

The maximum line current can be calculated as 10.23 kA. The I^2t value for T_F for $t_p = 10$ ms can be calculated as 685 kA^2s. In addition, total I^2t value for discharging period in the worst case can be obtained as 776 kA^2s. The values of R_{snF} and C_{snF} are calculated as 20 Ω and 30 μF, respectively. Moreover, the inductance of L_F can be set to 200 μH.

Detailed Operation Cycle

The detailed operation cycle of the designed CRCB is simulated using electromagnetic transient type software namely PSCAD. Figures 3.47 and 3.48 depict the most important parameters of the designed CRCB when interrupting a short circuit pole-to-ground fault with 100 km distance. Different stages of the CRCB operation are labeled by letters A, B, C, D, E and F in all figures. The descriptions of labels are illustrated in Table 3.8.

Figure 3.47(a) shows gate signals for different semiconductor switches in the CRCB structure. T_{ch1} is fired at $t = 50$ ms. The duration of

gate pulse is set to 10 ms. T_{ch2} is fired after the charging current falls below 100 A. The charging current is shown in Figure 3.48(a). Simultaneously, Q_{ch} is turned off for duration 10 ms. Upon receiving the trip command, T_F is fired and the MB unit is opened. The pulse width for the gate of T_F is set to 3 ms in order to compensate the thyristor gate delay and the MB unit turn-on delay times. When the discharging current falls below 150 A, Q_F is opened for duration of 10 ms. Upon closing Q_F, Q_{snF} is opened for duration of 10 ms in order to discharge C_{snF} through R_{snF}.

Table 3.8: Description of different labels used in the figures.

Label	Description
A	The first charging stage starts. (T_{ch1} is fired.)
B	The second charging stage starts. (T_{ch2} is fired.)
C	The charging stage is completed. (The CRCB is ready for interruption.)
D	Fault occurs.
E	The CRCB receives trip command. Discharging stage starts.
F	Discharging stage is accomplished. The CRCB is ready for next operation.

Figure 3.47(b) depicts the transmission line and the MB unit currents. The pre-fault current is set to 1 kA using a constant load. As can be seen in Figure 3.47(b), the charging stages has no impact on the transmission line and the MB unit current. The transmission line and the MB unit currents are equal until the CRCB trips (E). As soon as the short circuit fault happens on the transmission line, the current increases until reaches the maximum current interruption capacity of the designed CRCB. It is obvious that the current interruption must be done in smaller current levels. However, to consider the most sever scenario, the current is interrupted when it reached 10 kA (, which is the maximum current interruption level for this design case). As can be seen in Figure 3.47(b), after the CRCB trips, the current in its MB unit falls to zero quickly. The time range for the MB unit current to reach zero can be around few tens of micro seconds[10]. Despite quick decrease in the MB unit current, the current in the transmission line reduces smoothly. In this stage, the transmission line current is equal to the capacitor discharging current. As can be seen in Figure 3.47(b), the current in the transmission line falls to zero in almost 50 ms.

[10] This time depends upon the characteristics of parallel snubber circuits and also the turn-off characteristics of the employed semiconductor switches in th structure of the MB unit.

Figure 3.47(c) shows the voltage across the MB unit of the CRCB and the CRCB capacitor voltage. The pre-fault voltage across the MB unit is equal to the sum of the voltage drop across its semiconductor switches. The initial voltage of the CRCB capacitor is zero and as soon as T_{ch1} is fired, its voltage starts increasing. As can be seen in the figure, the capacitor voltage at the end of the first charging stage (B) reaches almost 300 kV. After firing T_{ch2}, due to the presence of L_{ch}, the capacitor voltage reaches almost 332 kV. Upon the CRCB tripping, the capacitor voltage reduces until it reaches almost zero. As can be seen in Figure 3.47(c), the maximum TIV across the MB unit of CRCB is equal to 340 kV. The CRCB voltage after current interruption increases up to the system nominal voltage.

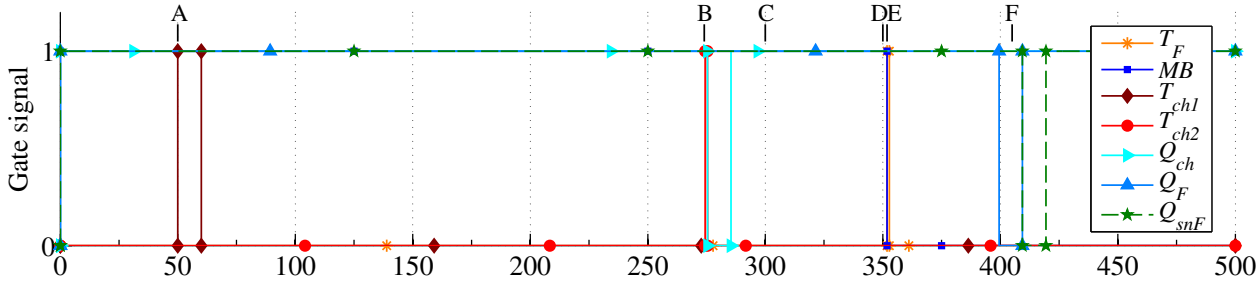
The voltage across the thyristors T_{ch1}, T_{ch2} and T_F is depicted in Figure 3.47(d). As it was discussed in the previous sections the mentioned thyristor banks are required to tolerate the system nominal

voltage. As can be seen in the figure, the rate of rise voltage does not have a large value.

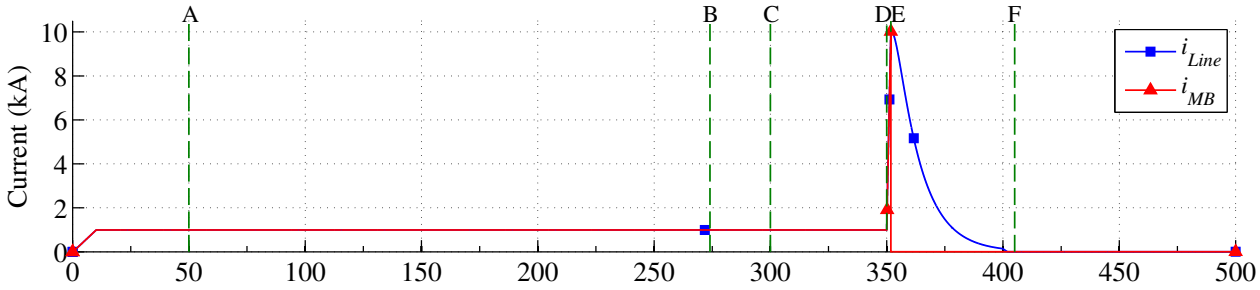
The voltage across R_{cb} and L_{cb} is shown in Figure 3.47(e). The voltage stress across R_{cb} and L_{cb} happens when the CRCB interrupts the fault current. The current limiting inductor is required to be rated for the nominal system voltage. However, in this design case the voltage across the current limiting inductor reaches almost 260 kV, which is lower than the system nominal voltage. The voltage across R_{cb} increases up to 300 kV and then decreases gradually till reaches zero.

Figure 3.48(a) shows the charging and discharging currents. The charging current peak in the first charging stage reaches almost 1.6 kA, which can be acceptable for a system with nominal current of 1 kA. The second peak of charging current happens at $t = 283$ ms and is equal to 950 A. The capacitor discharging current reaches almost 10 kA and then reduces smoothly until reaches zero.

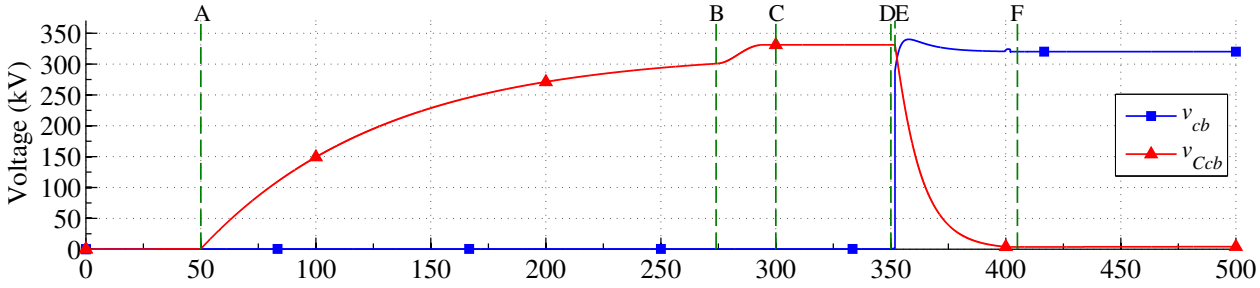
The I^2t value for T_{ch1} and T_F are shown in Figure 3.48(b). The total I^2t value for the charging stage reaches 100.73 kA^2s, which is almost equal to the value obtained using the analytical equations. The total I^2t value for T_F is equal to 772 kA^2s, which is almost equal to the value obtained using the analytical equations. Figure 3.48(b) depicts the I^2t value for T_{ch2}. As can be seen in the figure, the total I^2t value for T_{ch2} reaches 8.43 kA^2s, which is almost equal to the value obtained using the analytical equations.



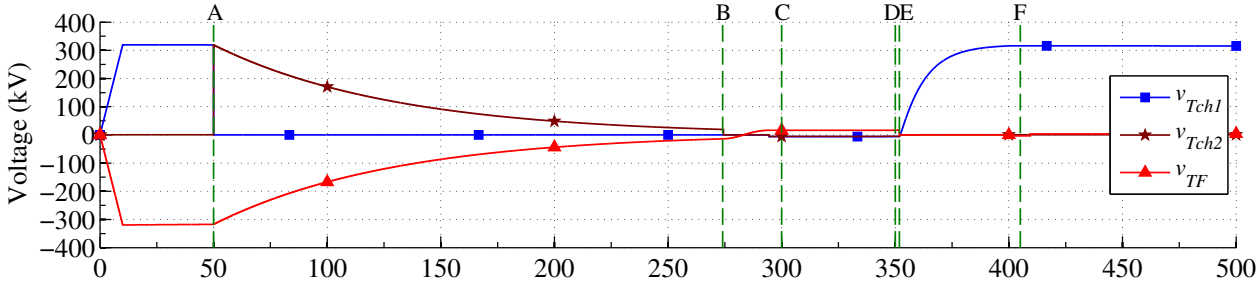
(a) Gate signals of different semiconductor switches



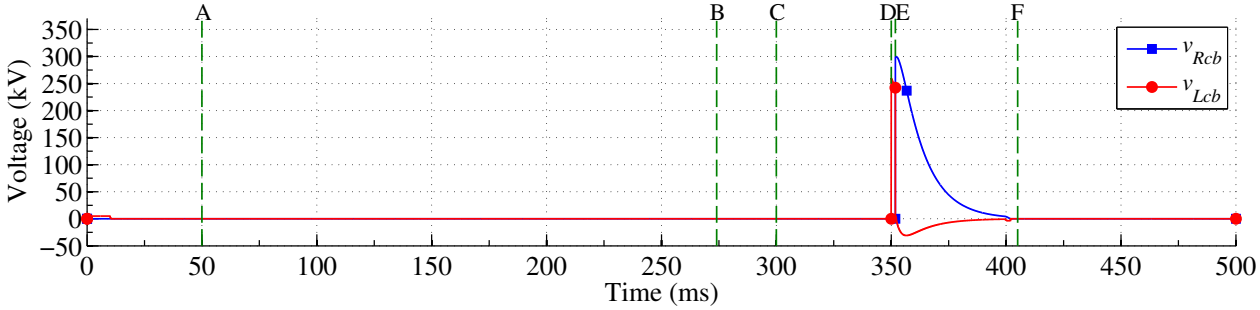
(b) The MB unit and the transmission line currents



(c) The CRCB capacitor voltage and the voltage across the MB unit

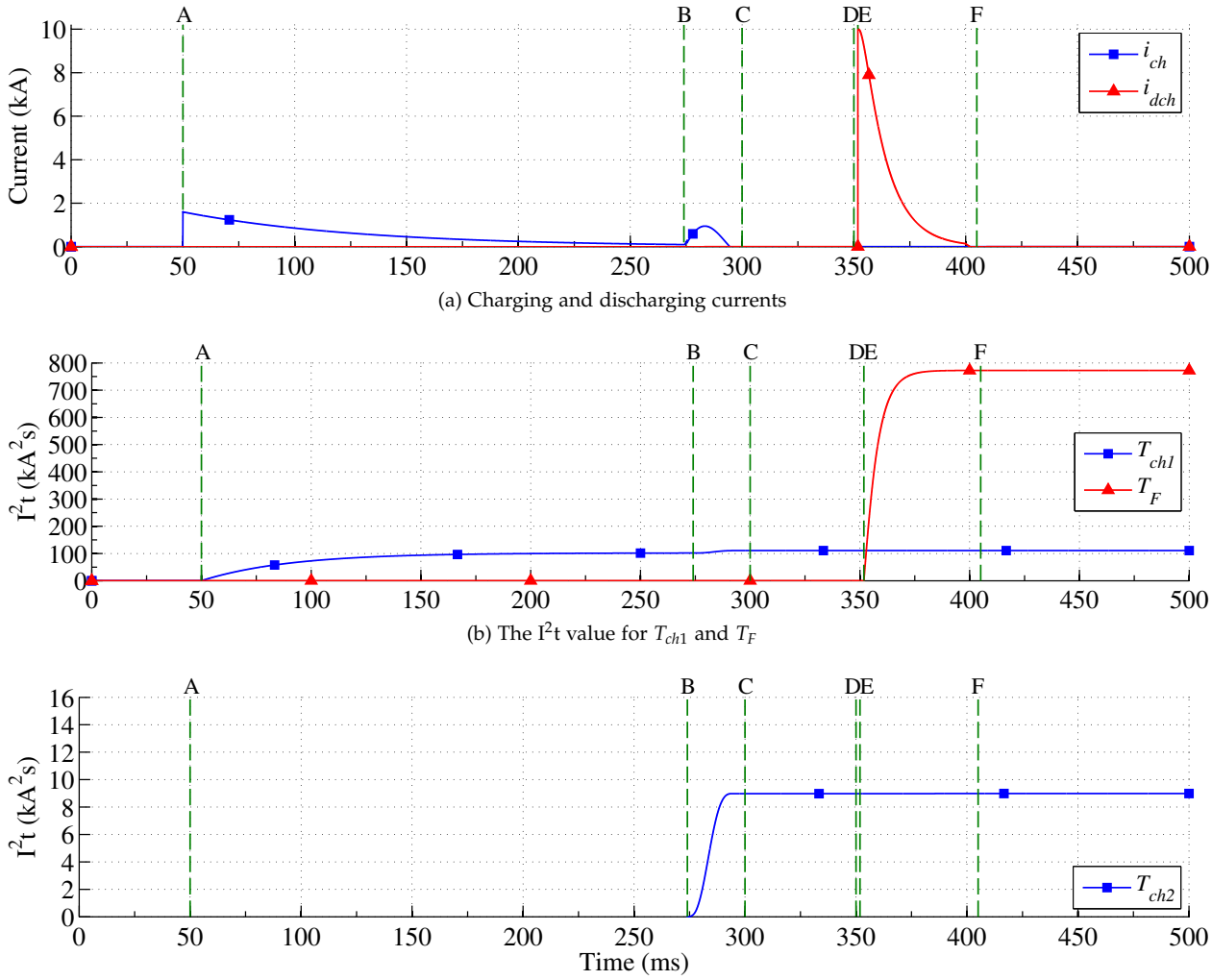


(d) Voltage across the thyristors T_{ch1}, T_{ch2} and T_F



(e) The voltage across R_{cb} and L_{cb}

Figure 3.47: Various CRCB parameters during a full cycle of operation.



(a) Charging and discharging currents

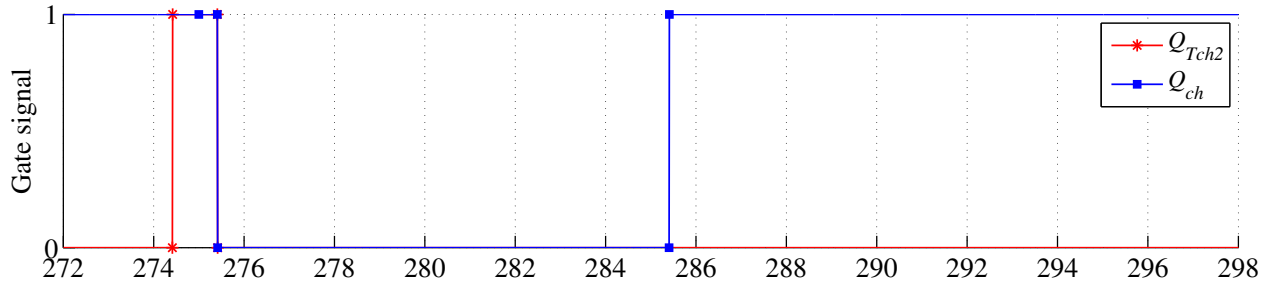
(b) The I^2t value for T_{ch1} and T_F

(c) The I^2t value for T_{ch2}

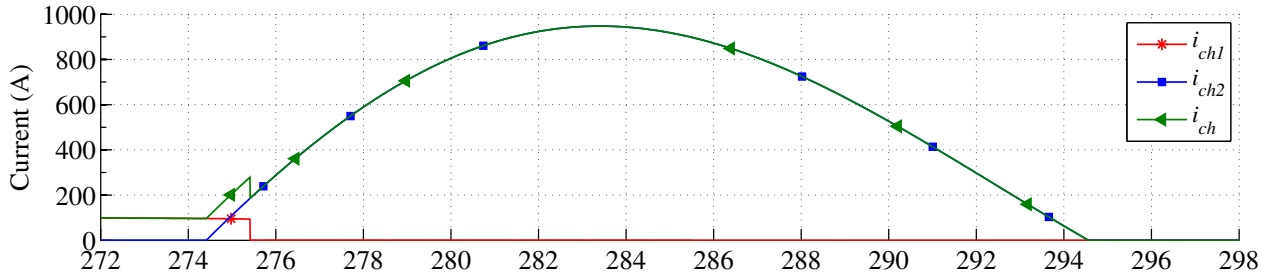
Figure 3.48: Various CRCB parameters during a full cycle of operation.

Figure 3.49 illustrates the behavior of relevant components during the second charging stage. Figure 3.49(a) shows the gate signals for T_{ch2} and Q_{ch}. The pulse width for firing T_{ch2} is equal to 1 ms. As can be seen in Figure 3.49(a), Q_{ch} is turned off 1 ms after firing T_{ch2}. It can be seen in Figure 3.49(b), after firing T_{ch2}, the charging current (i_{ch}) increases due to the reduction in the resistance of circuit by activating the branch that includes R_{ch2}. As soon as Q_{ch} is opened, i_{ch1} falls to zero and i_{ch} will be equal to i_{ch2} and the current will be divided between the resistors R_{ch1} and R_{ch2}. The charging current waveform confirms the validity of Equation 3.18.

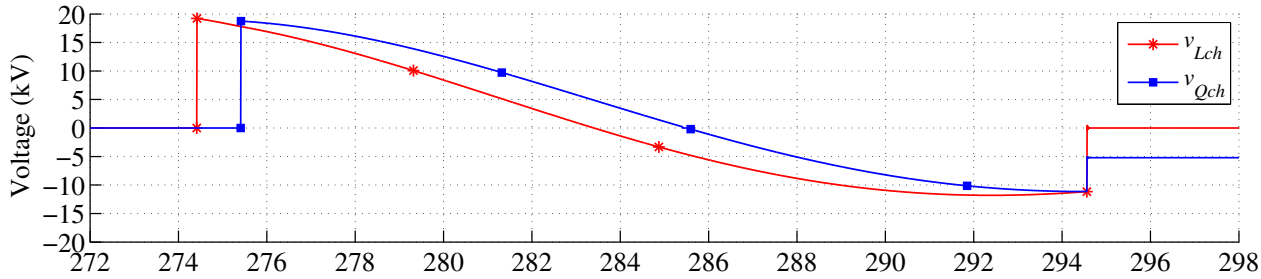
Figure 3.49(c) depicts the voltage across L_{ch} and Q_{ch}. After firing T_{ch2}, the current in L_{ch} cannot change instantaneously. Therefore, at the initial instance the voltage across L_{ch} is equal to the voltage difference between the dc bus and the CRCB capacitor (almost 19.5 kV). Thereafter, the current in the inductor increase gradually. The voltage across the semiconductor switch Q_{ch} increases up to the voltage difference between the dc bus and the CRCB capacitor at the instance of truing off. In continue, the voltage across the inductor



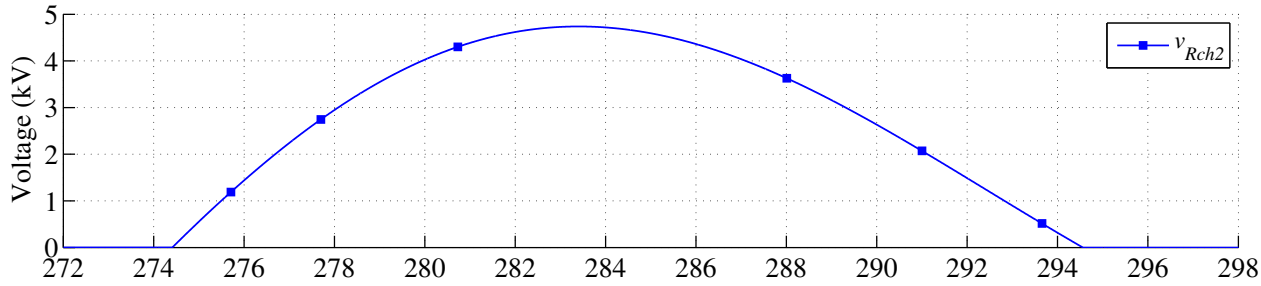
(a) Gate signals for T_{ch2} and Q_{ch}



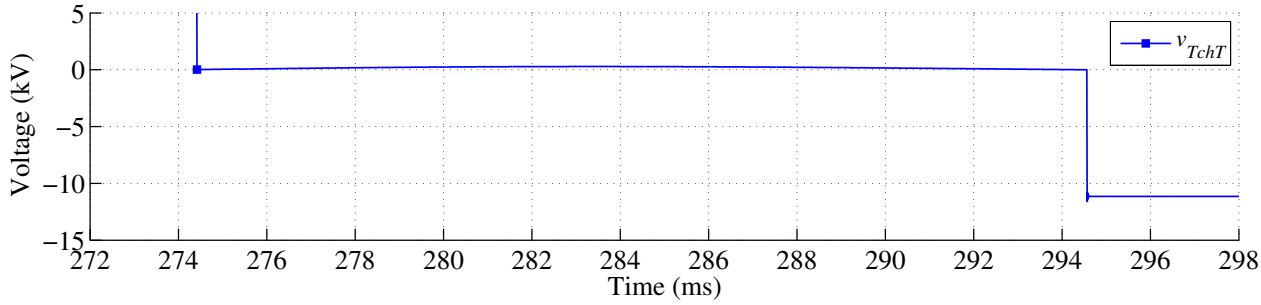
(b) Charging currents



(c) Voltage across the charing inductor L_{ch} and Q_{ch}



(d) Voltage across the second charing resistor R_{ch2}



(e) The sum of voltages across the thyristors T_{ch1} and T_{ch2}

Figure 3.49: Voltage and currents during the second stage of charging.

changes its polarity. However, as soon as its current falls to zero, its voltage also falls to zero. This is due to the presence of thyristors T_{ch1} and T_{ch2}, which do not allow the current reversal.

The voltage across the second charging resistor (R_{ch2}) is depicted in Figure 3.49(d). The voltage across R_{ch2} reaches almost 4.75 kV, which confirm that this resistor has a quite low voltage rating.

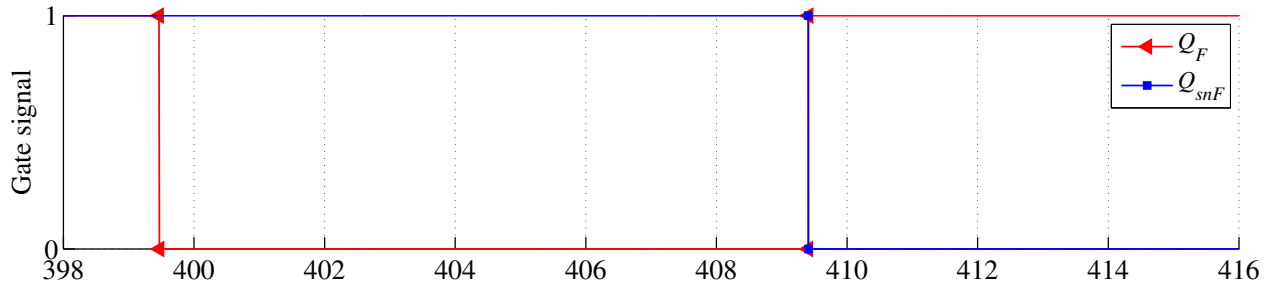
Figure 3.49(e) shows the sum of voltages across the thyristor T_{ch1} and T_{ch2}. As can be seen in the figure, upon firing T_{ch2} the voltage across both thyristors falls to zero due to the conduction of both of them. At the end of charing period, due to the extra charged voltage in the CRCB capacitor, the voltage across the thyristors is equal to -12 kV. Generating negative voltage across the thyristor banks is crucial in guaranteeing their successful commutation.

The behavior of most relevant components during the final stage of the CRCB discharge is illustrated in Figure 3.50. Figure 3.50(a) shows the gate signals for semiconductor switches Q_F and Q_{snF}. Q_F is opened when the discharging current (i_{dch}) falls below 150 A for duration of 10 ms while Q_{snF} is closed during the mentioned period. Figure 3.50(b) depicts the discharging current and the current in the snubber circuit. As can be seen in the figure, the discharging current is commutated into the snubber circuit after opening Q_F. The current in the snubber circuit charges C_{snF}.

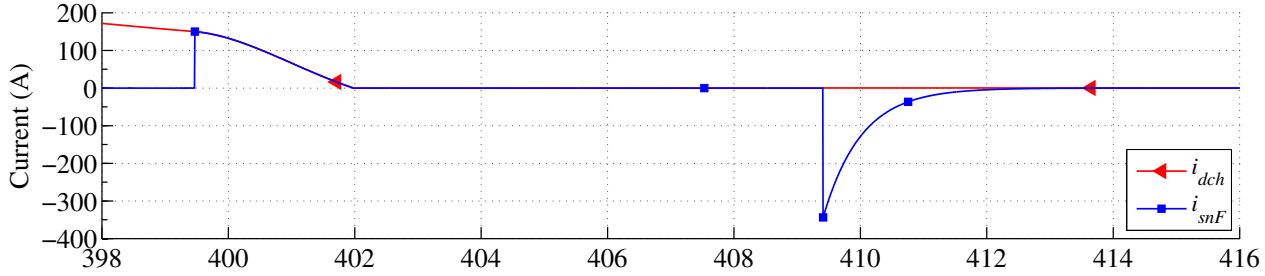
The snubber capacitor (C_{snF}) voltage is shown in Figure 3.50(c). It can be seen that the capacitor is charged up to almost 7 kV. Figures 3.50(b) and (c) illustrate that after the capacitor is charged the current reaches zero. Figure 3.50(d) shows the voltage across the thyristor T_F. The voltage across the thyristor becomes equal to -3.5 kV when the current in the snubber circuit (i_{snF}) reaches zero. The negtive voltage across the thyristor bank grantees the successful turn-off of the switch.

At the end of this cycle, Q_{snF} is opened and Q_F is closed. In this stage, if the snubber capacitor has some charge, it can be discharged via R_{snF}. It can be seen in Figure 3.50(b) that the current in R_{snF} reaches almost 350 A. The voltage across this resistor is depicted in Figure 3.50(c). In the worst case, the voltage across this resistor reaches almost -7 kV.

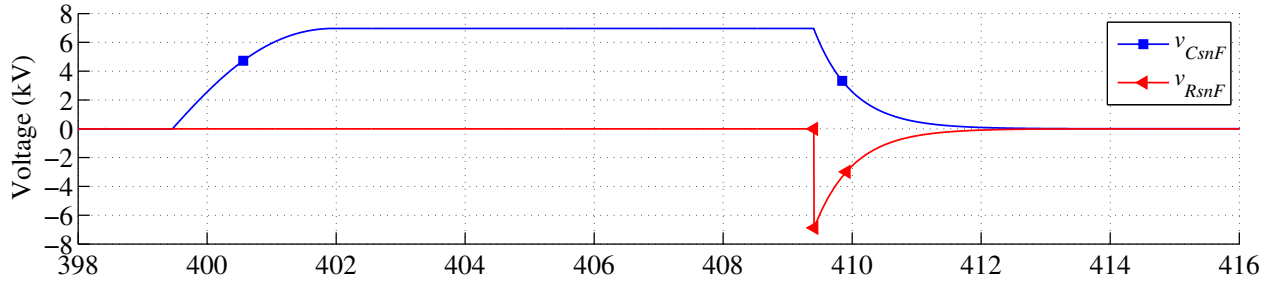
The voltage across Q_F and Q_{snF} is shown in Figure 3.50(e). Q_F and Q_{snF} are required to be rated for the maximum charged voltage of C_{snF}.



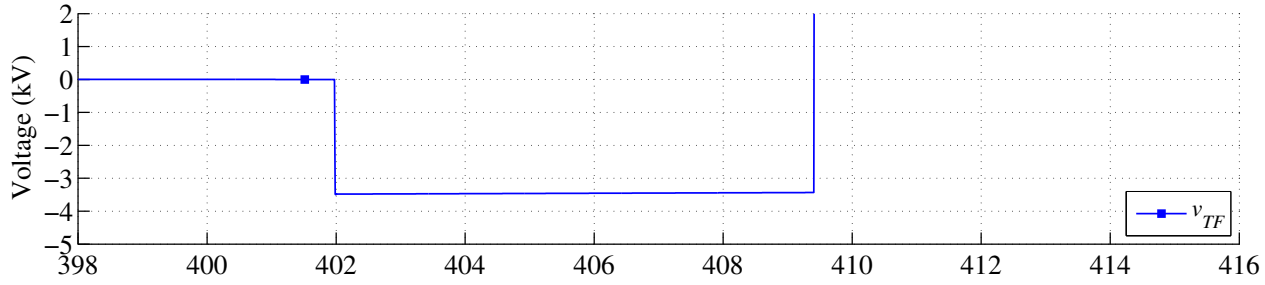
(a) Gate signals for Q_F and Q_{snF}



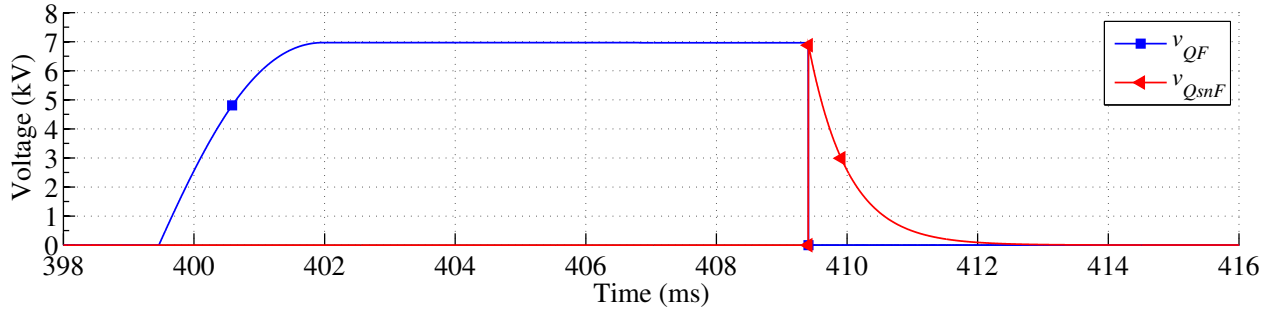
(b) Current in the snubber circuit



(c) Voltage across C_{snF} and R_{snF}



(d) Voltage across the thyristor T_F



(e) Voltage across Q_F and Q_{snF}

Figure 3.50: Voltage and currents during the final stage of the CRCB discharging.

Impact of The CRCB Resistor and Capacitor

Impacts of variation in deferent CRCB and system parameters are investigated using analytical equations from subsection 3.3.2. The behavior of CRCB when interrupting the fault current equal to its maximum interruption capability and also interrupting the fault current equal to 60% of its maximum interruption capability is considered.

The impact of change in the internal resistor and capacitor of the CRCB is depicted in Figure 3.51(a) and (b). Figure 3.51(a) shows the TIV versus values of C_{cb} and R_{cb}. The fault distance from CRCB is set to 100 km and the CRCB interrupts its maximum rated current (10 kA). In addition, the value of current limiting inductor is set to 50 mH. The capacitor value changes from 200 to 1200 μF and the resistor takes the value in the range of 25 to 32 Ω. Minimum excessive voltage across the CRCB can be achieved when it is equipped with the largest resistor and capacitor. The change in the resistance below its marginal value (can be calculated from Equation (3.74)) does not change the TIV value, remarkably. However, small values of R_{cb} can increase the maximum line current up to 15%. The value of C_{cb} has the largest impact on the TIV of CRCB, whereas it has a negligible impact on the maximum line current when R_{cb} is selected close to its marginal value.

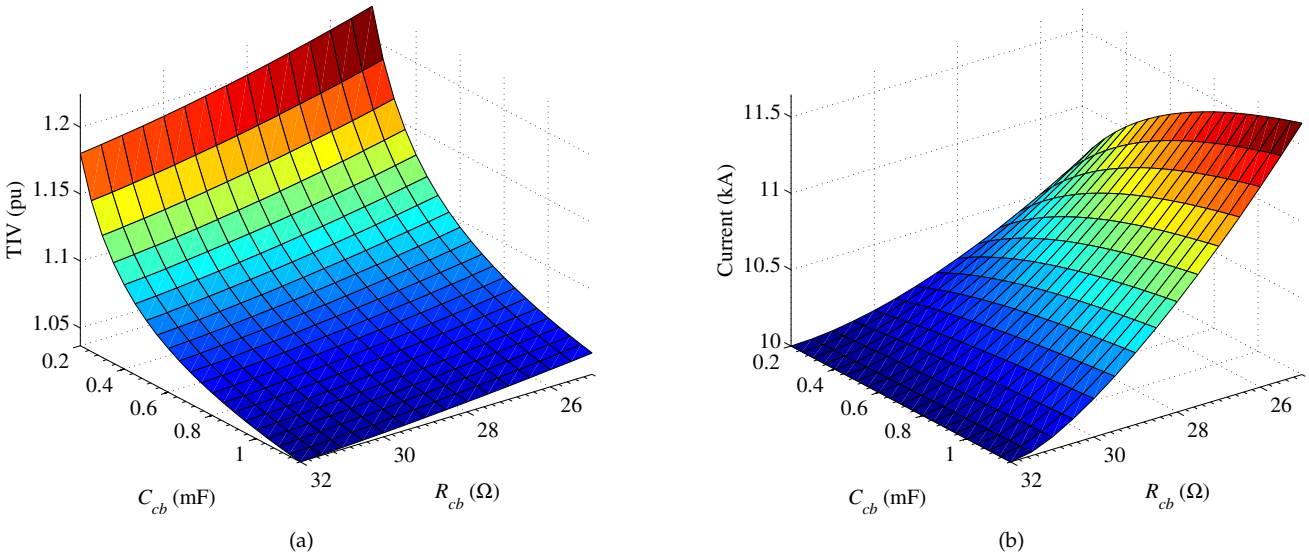
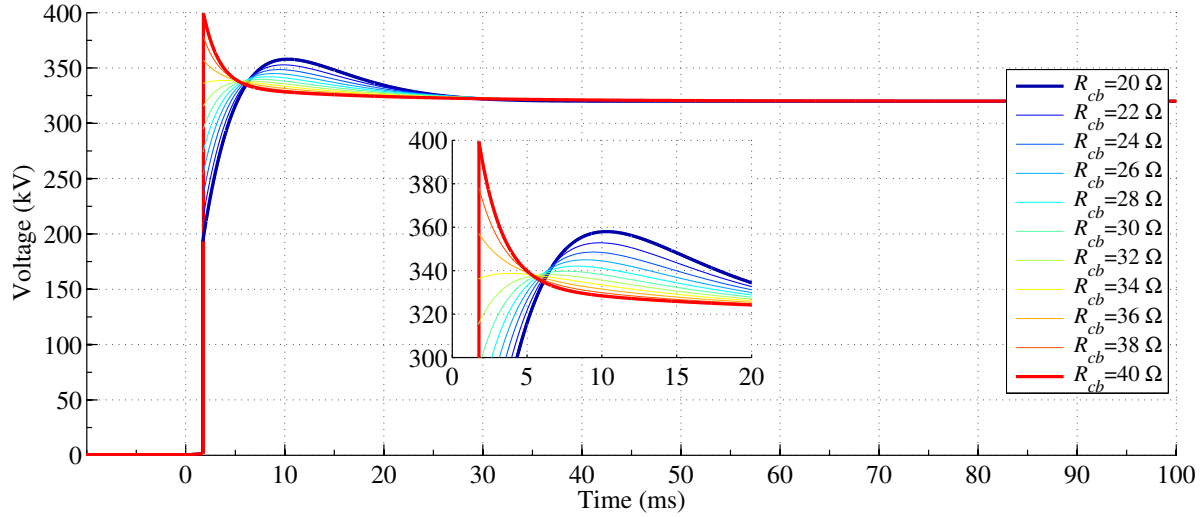


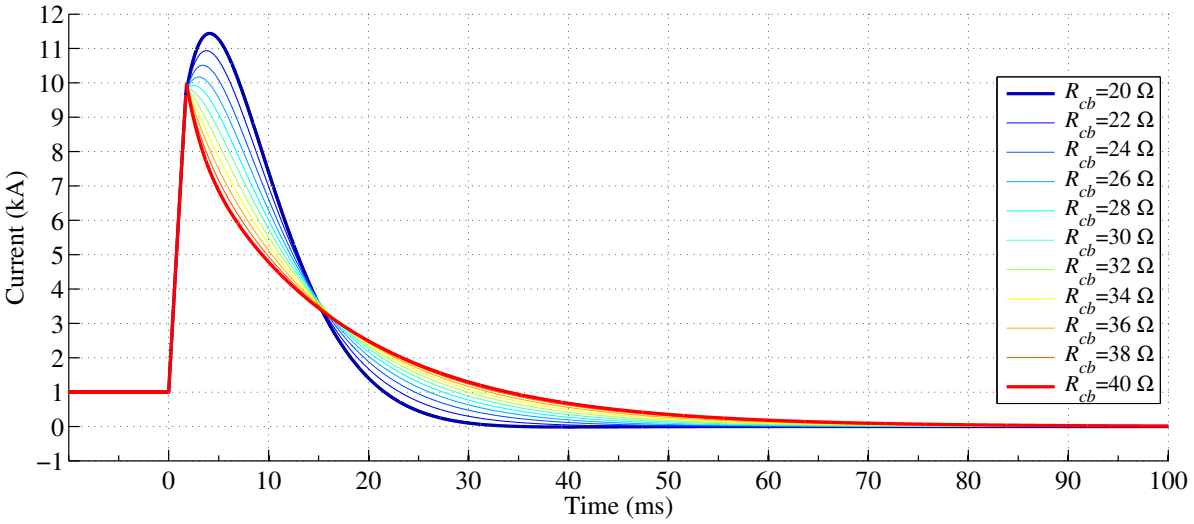
Figure 3.51: (a) TIV and (b) maximum line current variation by changing C_{cb} and R_{cb}.

The CRCB voltage and the line current for different values of R_{cb} with fixed 400 μF capacitor are depicted in Figure 3.52(a) and (b), respectively.

It can be seen in Figure 3.52(b) that the CRCB interrupts the fault current when it reaches 10 kA, which is equal to the maximum interruption capability of the CRCB. Increasing the resistor value up to its marginal value decreases the excessive voltage on the device while increases the line current discharge time. The minimum TIV can be achieved by selecting the resistor value equal to its marginal



(a) Voltage across the MB unit

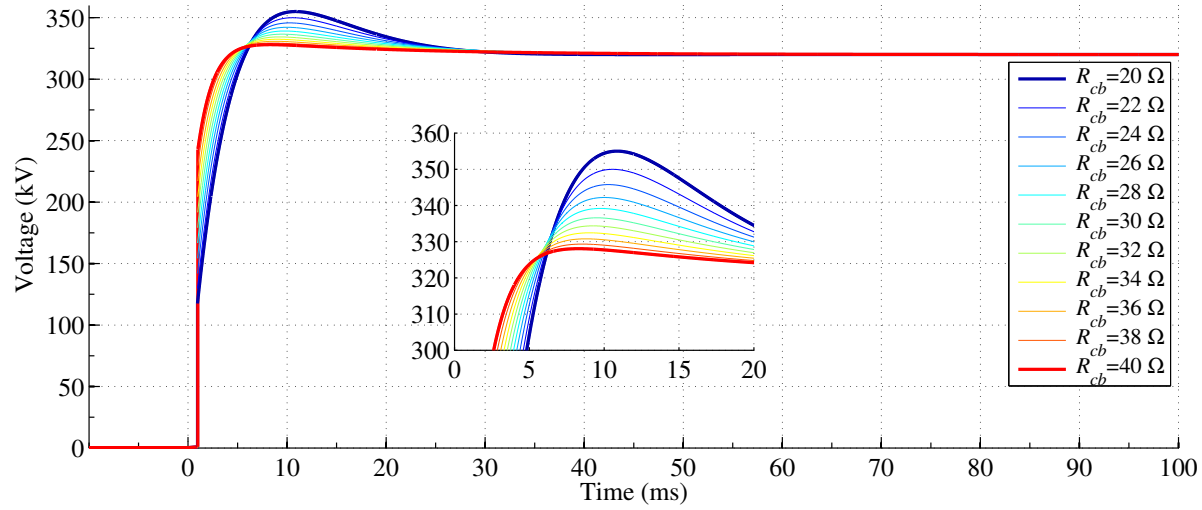


(b) The transmission line current before and after fault occurrence

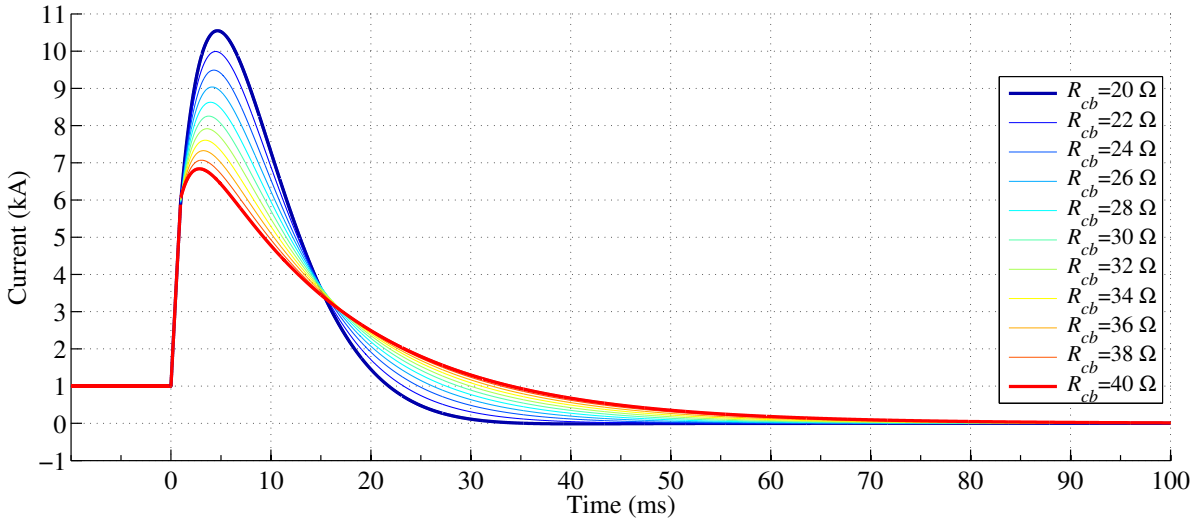
Figure 3.52: (a) Voltage and (b) current waveforms for designed CRCB.

value. Figure 3.52(a) shows that the TIV across the CRCB reaches almost 338 kV (1.056 pu) when the value of resistor is set to 32 Ω. However, it is recommended to choose the resistor value smaller than the marginal value. The TIV can reach almost 359 kV (1.12 pu) if the value of resistor is reduced down to 20 Ω. Note that when the value of resistor is selected larger than its marginal value, the operation regime of the equivalent circuit will be changed and hence the TIV across the CRCB can increase dramatically. Figure 3.52(b) shows that decreasing the value of resistor can increase the line current peak during the discharge stage of operation. The current peak in the transmission line and consequently in the discharging thyristor (T_F) can reach 11.5 kA if the value of resistor is set to 20 Ω. Selecting resistance values larger than 26 Ω can keep the current peak smaller than the maximum interrupted current.

Figure 3.53(a) and (b) illustrate the CRCB voltage and the transmis-



(a) Voltage across the MB unit

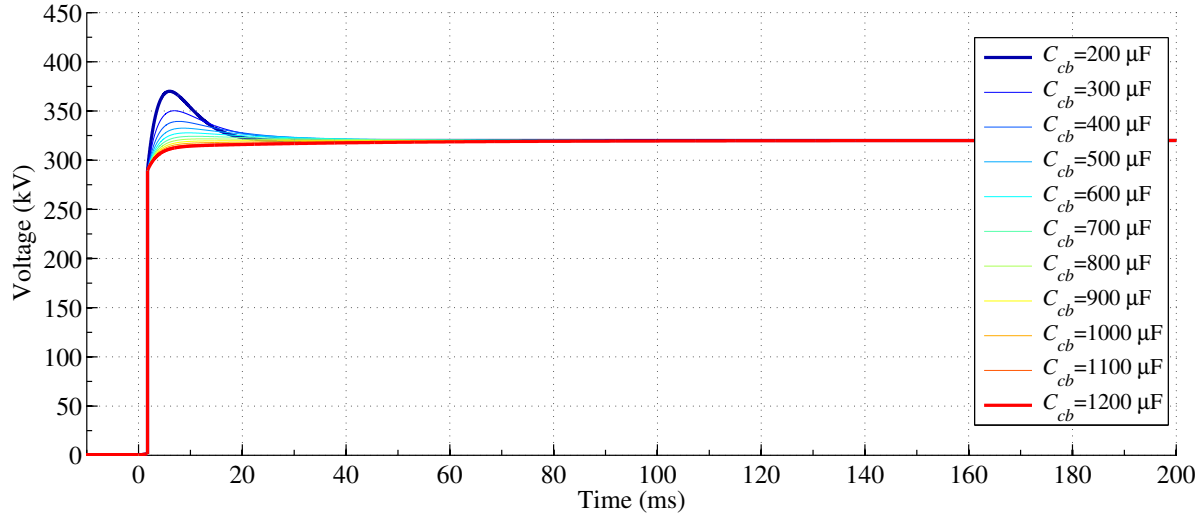


(b) The transmission line current before and after fault occurence

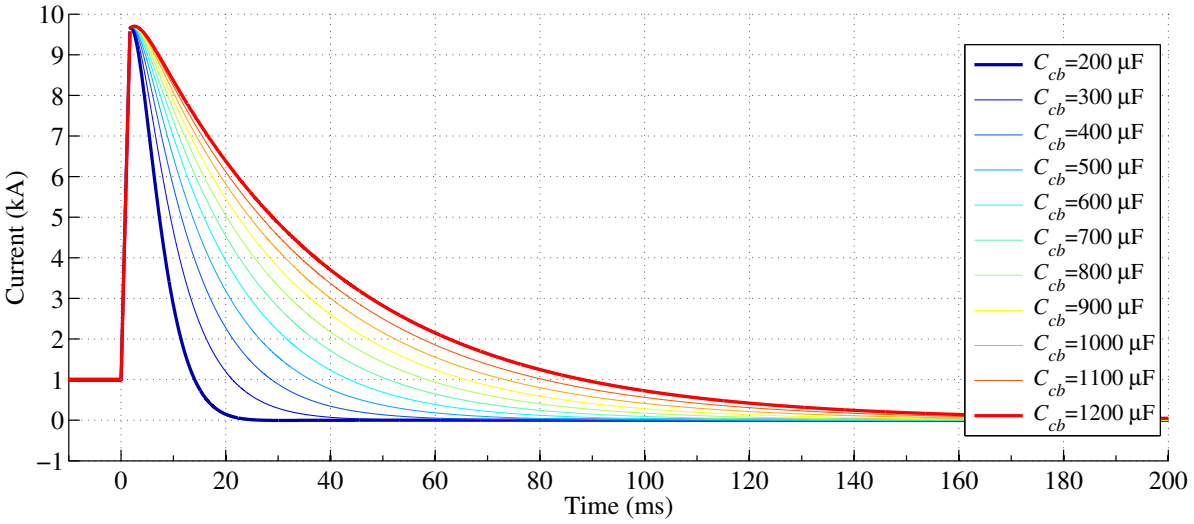
Figure 3.53: (a) Voltage and (b) current waveforms for designed CRCB.

sion line current when it interrupts the fault current when it reaches 6 kA (, which is equal to 60% of its maximum current interruption capability.). It can be seen in Figure 3.53(a), when the value of resistor is selected equal to its marginal value the TIV across the CRCB is equal to almost 334 kV (1.043 pu). Despite the CRCB operation in the maximum current interruption capability condition, the TIV across the CRCB reduces by increasing the value of resistor to larger than its marginal value. For instance, the TIV can be limited to 327 kV (1.021 pu) when the resistance value is set to 40 Ω. Figure 3.53(b) shows that the current peak in the transmission line can reach 11.5 kA when the value of resistor is set to 20 Ω, similar to the previous case.

Figure 3.52(a) and (b) depict the voltage across the CRCB and the transmission line current when the value of R_{cb} is set to 30 Ω and the capacitor value varies from 200 to 1200 μF. The marginal value of the CRCB capacitor was calculated as 238.28 μF. It can be seen in the Figure 3.52(a) when the capacitance is selected below its



(a) Voltage across the MB unit

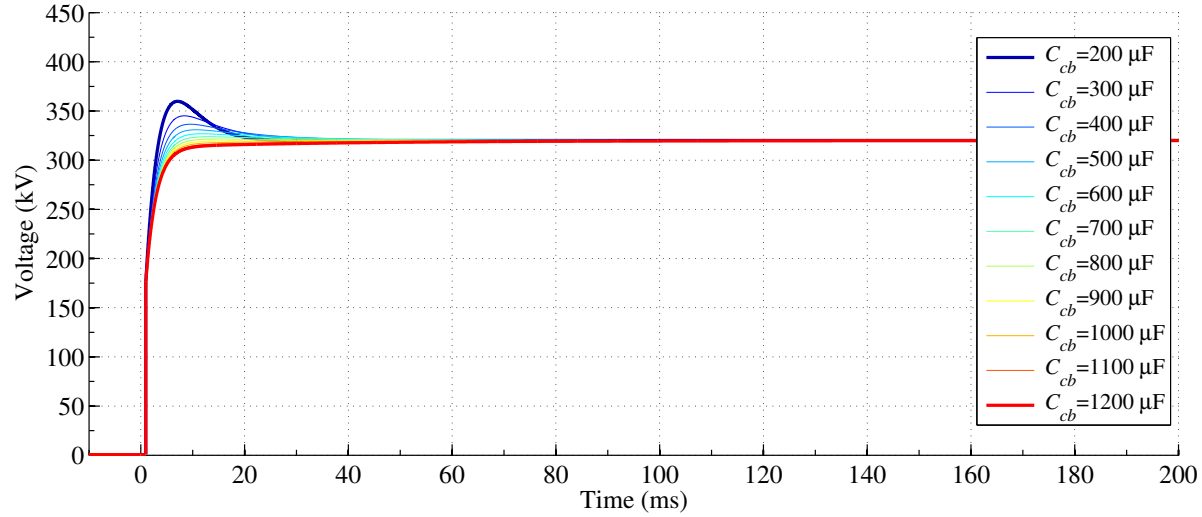


(b) The transmission line current before and after fault occurrence

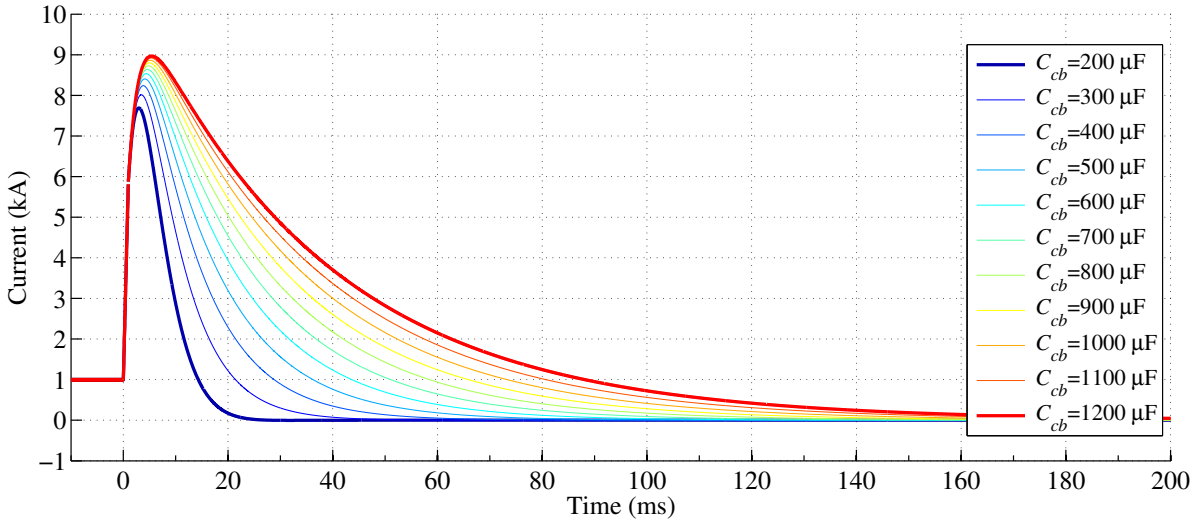
Figure 3.54: (a) Voltage and (b) current waveforms for designed CRCB.

marginal value the TIV across the CRCB increases remarkably. For instance, when the CRCB capacitor is set to 200 μF, the TIV can reach almost 370 kV (1.15 pu). Increasing the value of C_{cb} decreases the TIV whereas increases the line current discharge time. If the CRCB capacitor has a relatively large capacitance the CRCB can operate even without excessive voltage. It can be seen in Figure 3.52(a) when the capacitor value is set to 600 μF the TIV across the CRCB is almost zero. Figure 3.52(b) shows that the capacitor size does not have a significant impact on the current peak in the transmission line. However, larger capacitors can increase the CRCB discharge time.

The CRCB voltage and the transmission line current when the CRCB interrupts the fault current when it reaches 6 kA are depicted in Figure 3.53(a) and (b). Comparing to the full capacity interruption case, the TIV across the CRCB is reduced. As can be seen in Figure



(a) Voltage across the MB unit



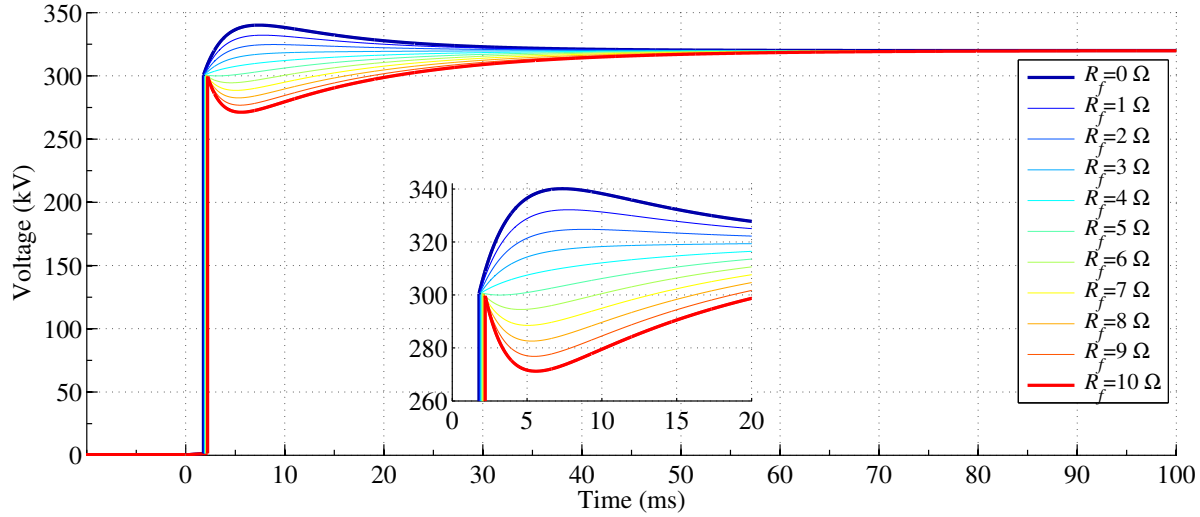
(b) The transmission line current before and after fault occurrence

Figure 3.55: (a) Voltage and (b) current waveforms for designed CRCB.

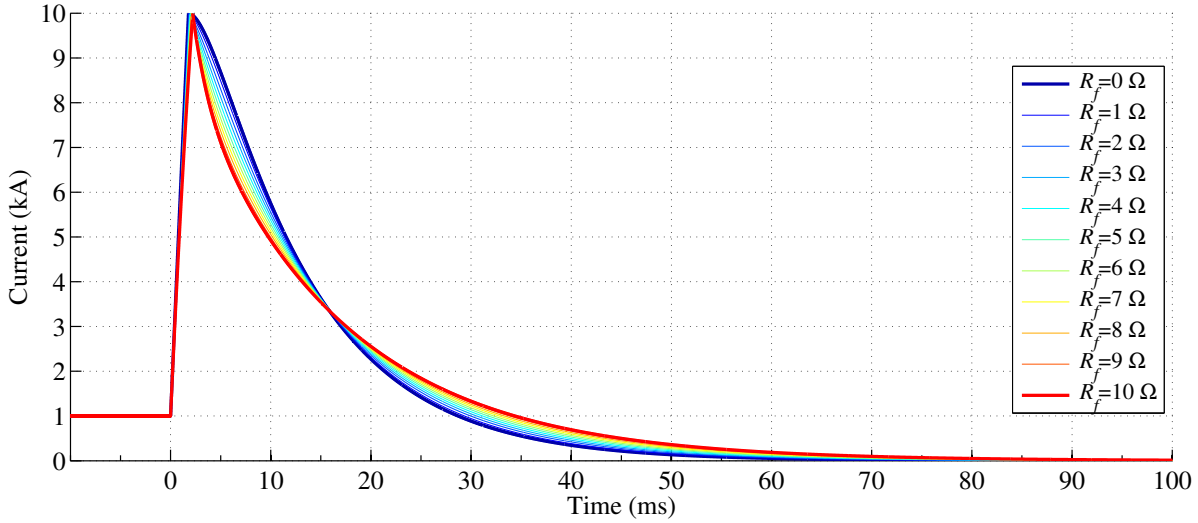
3.53(a), the voltage waveform is smoother than the voltage waveform when the CRCB interrupts the maximum interruptible current. As can be seen in Figure 3.53(b) the current peak does not exceed 9 kA when the CRCB operates in 60% of its interruption capacity.

Impact of Fault Resistance

The impact of fault impedance in two current interruption scenarios is investigated. Figure 3.56(a) and (b) depict the voltage across the CRCB and the transmission line current when the CRCB interrupts a fault current in its full interruption capacity. As the worst case a short circuit fault at the end of the transmission line is investigated when the values of C_{cb} and R_{cb} are set to 400 μF and 30 Ω, respectively and the fault resistance varies from 0 to 10 Ω. As can be seen in Figure 3.56(a), the fault resistance has a significant impact on the voltage waveform. The largest TIV across the CRCB happens when it interrupt a short



(a) Voltage across the MB unit

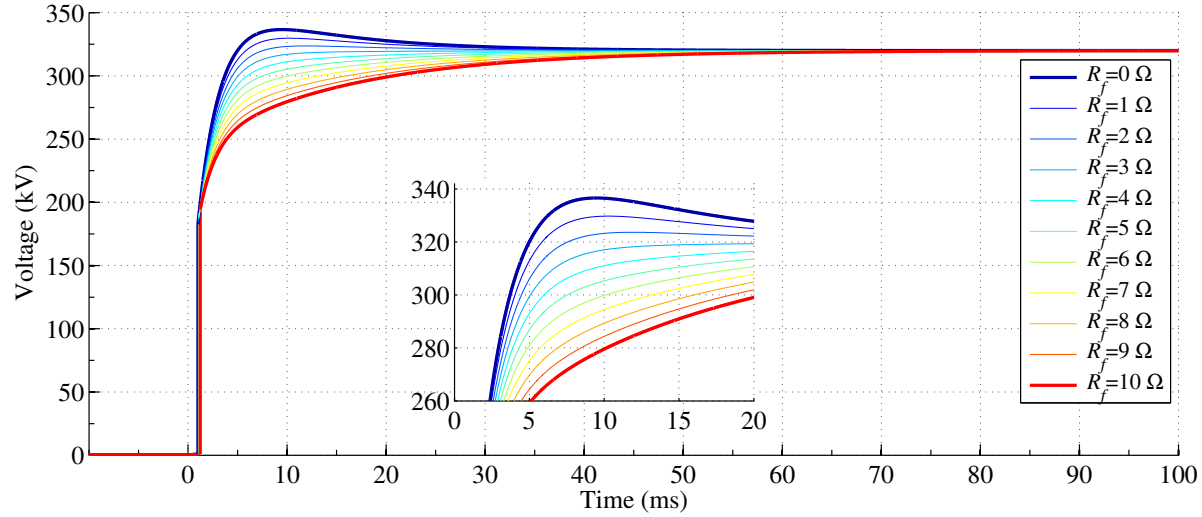


(b) The transmission line current before and after fault occurrence

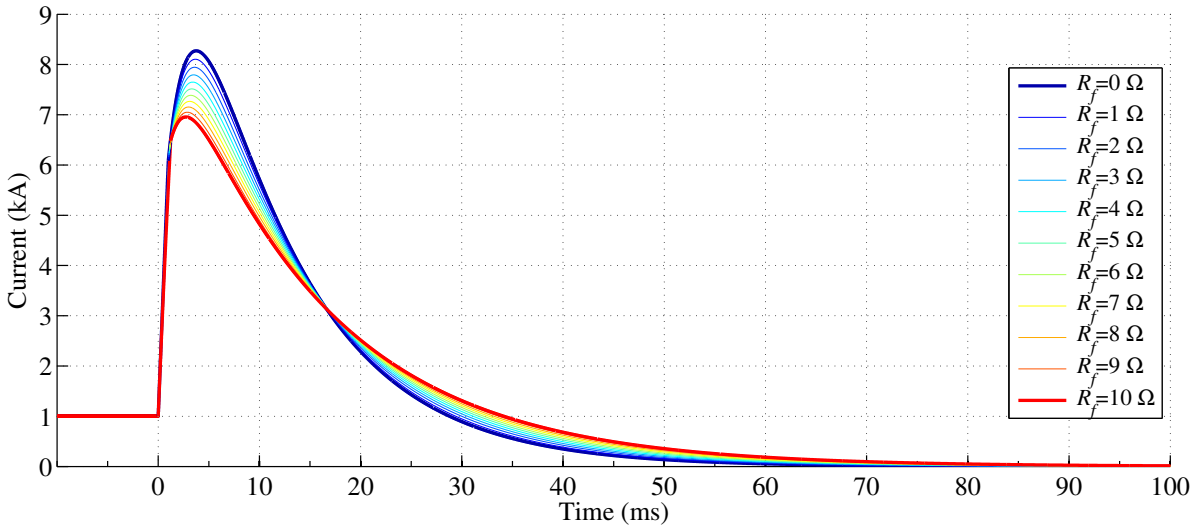
Figure 3.56: (a) Voltage and (b) current waveforms for designed CRCB.

circuit fault with $R_f = 0\ \Omega$. When the fault impedance increases the TIV across the CRCB reduces, notably. For instance, when the fault impedance is equal to 0 Ω, the TIV reaches 340 kV whereas when it is equal to 3 Ω no excessive voltage can be observed. In fact, the higher impedance faults increase the damping factor of the equivalent circuit. Therefore, interrupting high impedance faults does not cause notable overvoltage on the CRCB. Figure 3.56(b) show the transmission line current for different fault resistances. As can be seen the impact of fault resistance on the transmission line current is negligible.

Figure 3.57(a) and (b) show the voltage across the CRCB and the current in transmission line when the CRCB interrupts a fault current in 60% of its full interruption capacity. Figure 3.57(a) show similar trend as compared to Figure 3.56(a) although with different waveform shapes. The impact of fault resistance on the transmission line current



(a) Voltage across the MB unit



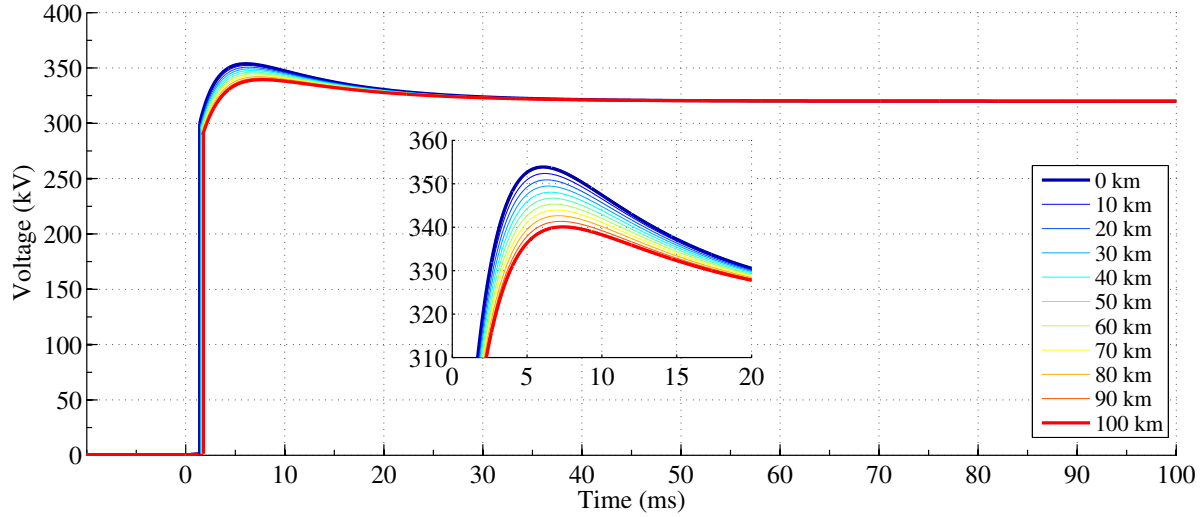
(b) The transmission line current before and after fault occurrence

Figure 3.57: (a) Voltage and (b) current waveforms for designed CRCB.

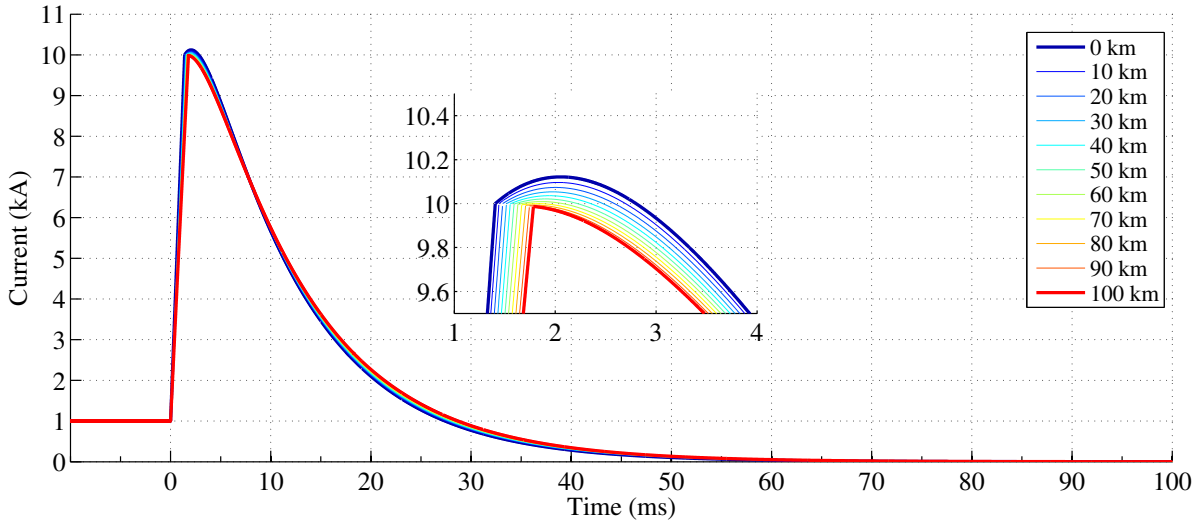
is more clear as compared to the previous case. Lower fault resistances cause larger peak in the transmission line current. The impact of fault impedance on the CRCB discharge time is not remarkable.

Impact of Fault Location

Figure 3.58(a) and (b) show the impact of fault distance from the CRCB on its voltage and the transmission line current. As it is expected the amount of stored energy in the line inductance during the faults far from the CRCB is higher as compared to the closer faults. However, it can be seen in Figure 3.58(a) when a fault occurs close to the CRCB, its interruption causes slightly larger TIV across the CRCB as compared to the faults with longer distances to the CRCB. As was previously mentioned, the transmission line resistance depends on the frequency. Although the line resistance is typically small and negligible it can increase during the fault current interruption due to



(a) Voltage across the MB unit

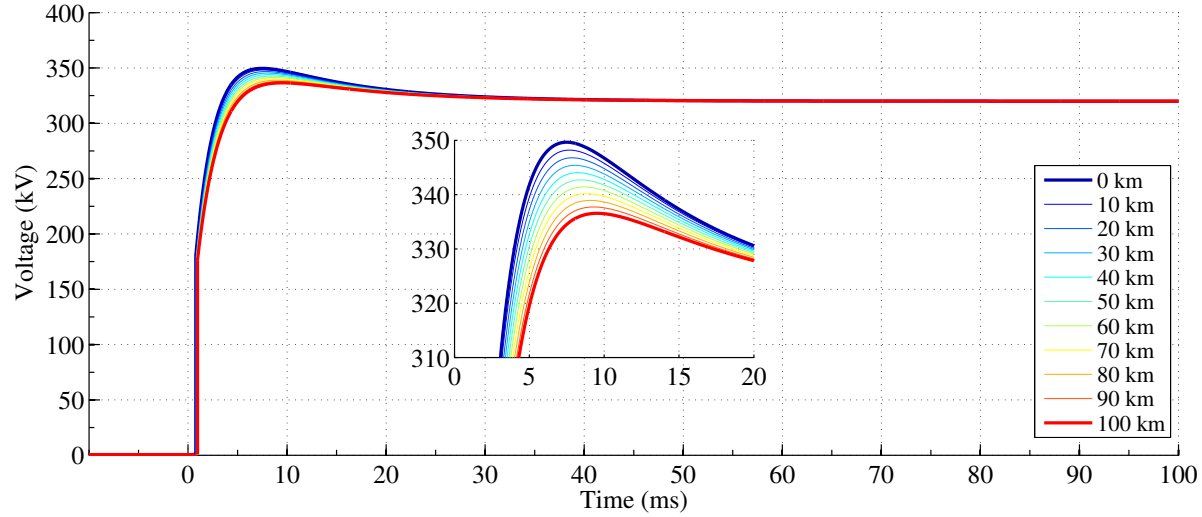


(b) The transmission line current before and after fault occurrence

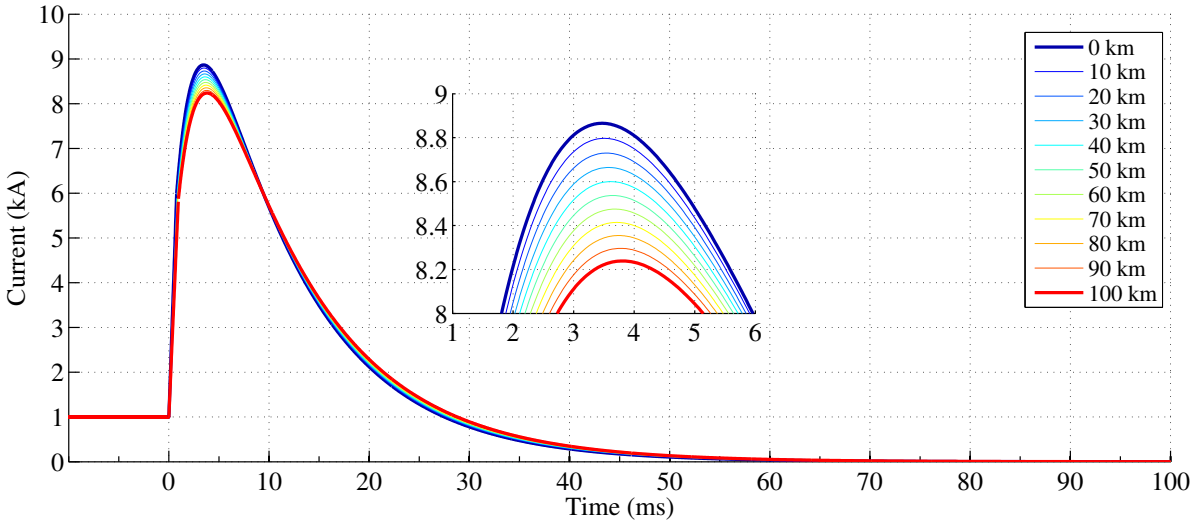
Figure 3.58: (a) Voltage and (b) current waveforms for designed CRCB.

the high frequency components of fault current and the skin effect [187].

Moreover, the line inductance decreases remarkably as compared to its pre-fault value. The inductance and resistance of employed cable in this study for $f = 0.001$ Hz is equal to 2.9 mH/km and 10 mΩ/km, respectively whereas for $f = 1000$ Hz the values change to to 0.11 mH/km and 23 mΩ/km. Therefore, when the CRCB interrupts a fault with 100 km distance the high frequency line resistance increases the damping factor of the equivalent circuit and reduces the overvoltage across the CRCB. When the fault occurs very close to the CRCB, the system inductance is equal to value of current limiting inductor while the line resistance between the CRCB and the fault location is equal to zero. Hence, larger TIV can be observed when the fault occurs very close to the CRCB. The TIV across the CRCB for



(a) Voltage across the MB unit

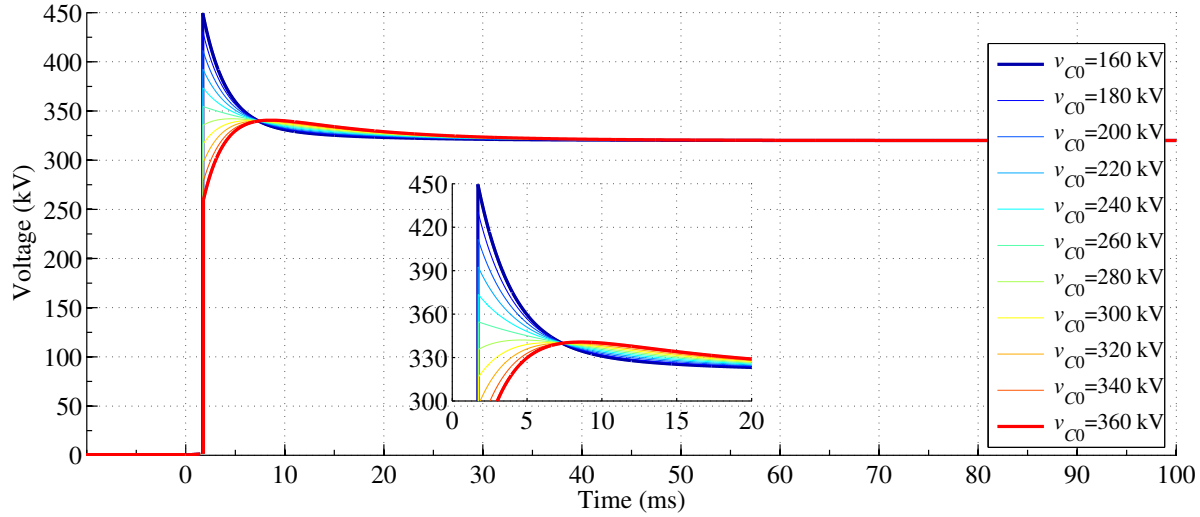


(b) The transmission line current before and after fault occurence

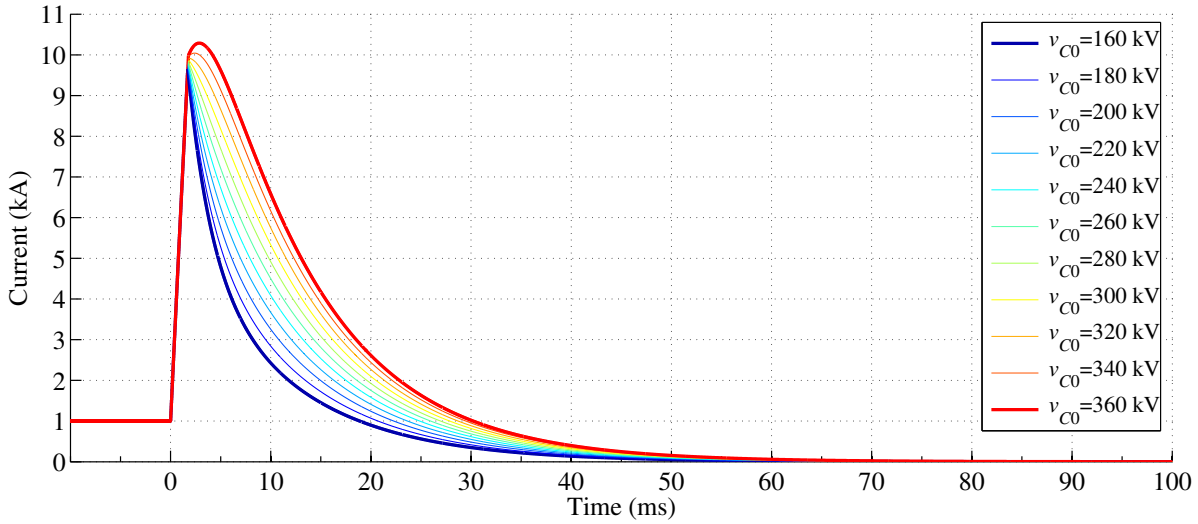
Figure 3.59: (a) Voltage and (b) current waveforms for designed CRCB.

0 km and 100 km faults reaches 354 kV and 340 kV, respectively. In other words, for a transmission line with 100 km length the TIV can change up to 4.3% of the system nominal voltage depending on the fault distance. In addition, Figure 3.58(b) illustrates that decreasing the fault distance reduces the resistance between the CRCB and the fault location and slightly increases the maximum line current.

Figure 3.59 (a) and (b) depict the CRCB voltage and the current in the transmission line when the CRCB interrupts a fault current in 60% of its maximum interruption capacity. Due to the lower magnitude of the interrupted current the TIV across the CRCB is reduced as compared to the previous case. However, the TIV can change up to 4.68% of the system nominal voltage depending on the fault distance. It can be seen in Figure 3.59(b) that the transmission line current peak varies between 8.23 kA and 8.85 kA.



(a) Voltage across the MB unit

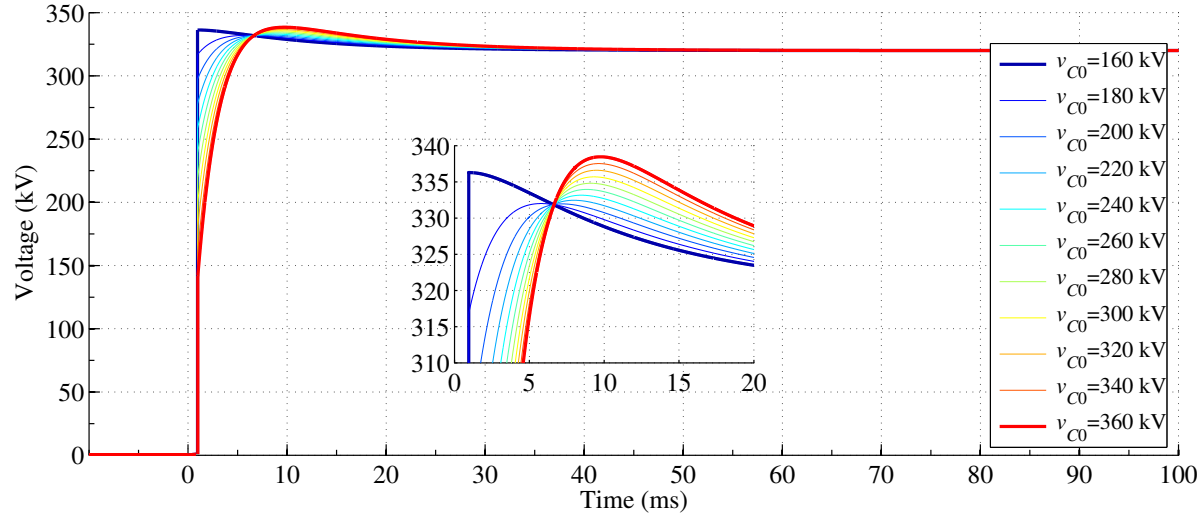


(b) The transmission line current before and after fault occurence

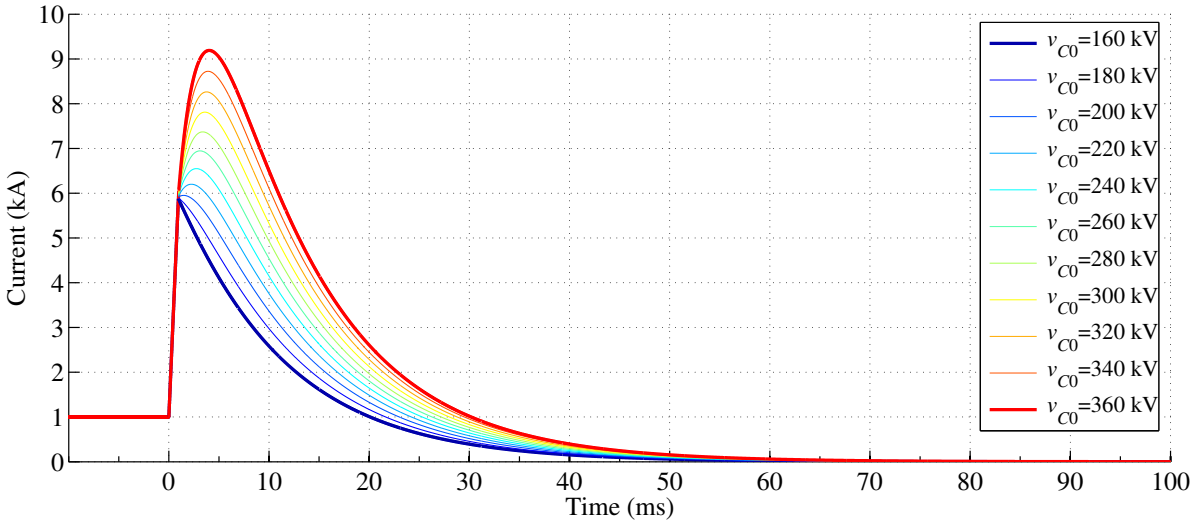
Figure 3.60: (a) Voltage and (b) current waveforms for designed CRCB.

Impact of Capacitor Initial Voltage

Figure 3.60(a) and (b) depict the impact of CRCB capacitor charged voltage on the CRCB voltage and the line current waveforms when the CRCB interrupts a fault current in its full interruption capacity. In order to clarify the impact of undercharged and overcharged capacitor on the CRCB behavior the capacitor charged voltage is varied between 160 kV and 360 kV. As was mentioned previously, the CRCB capacitor is designed to be charged more than the dc bus voltage. When the capacitor is charged up to the system voltage, the CRCB satisfies the design requirements. As can be seen in Figure 3.60(a) when the capacitor voltage varies between 280 kV and 360 kV the maximum TIV across the CRCB is almost constant. In other words, when the capacitor is undercharged down to 280 kV, the CRCB still satisfies the TIV requirement in this design case. However, decreasing the



(a) Voltage across the MB unit

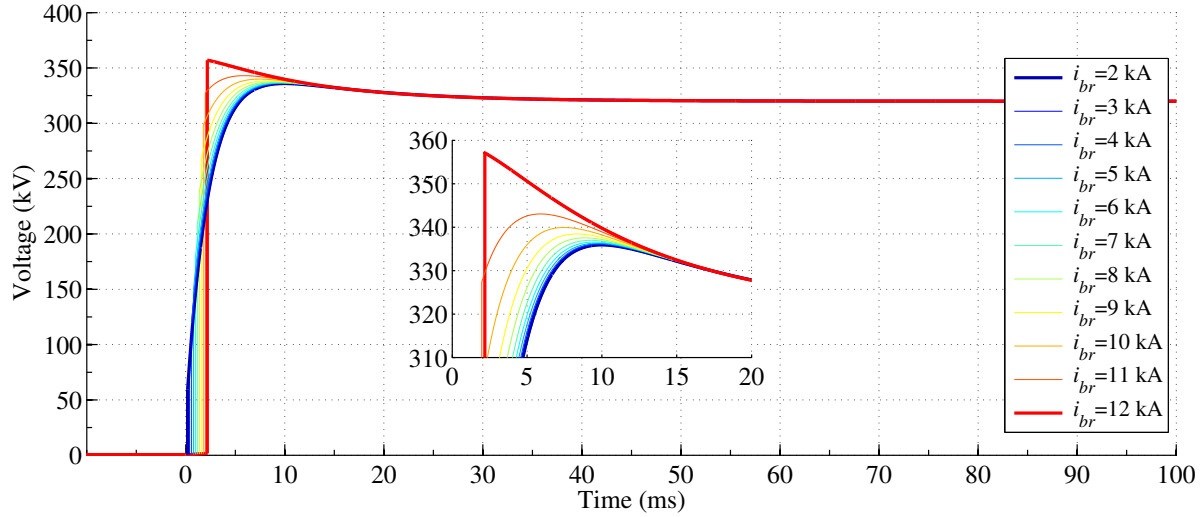


(b) The transmission line current before and after fault occurence

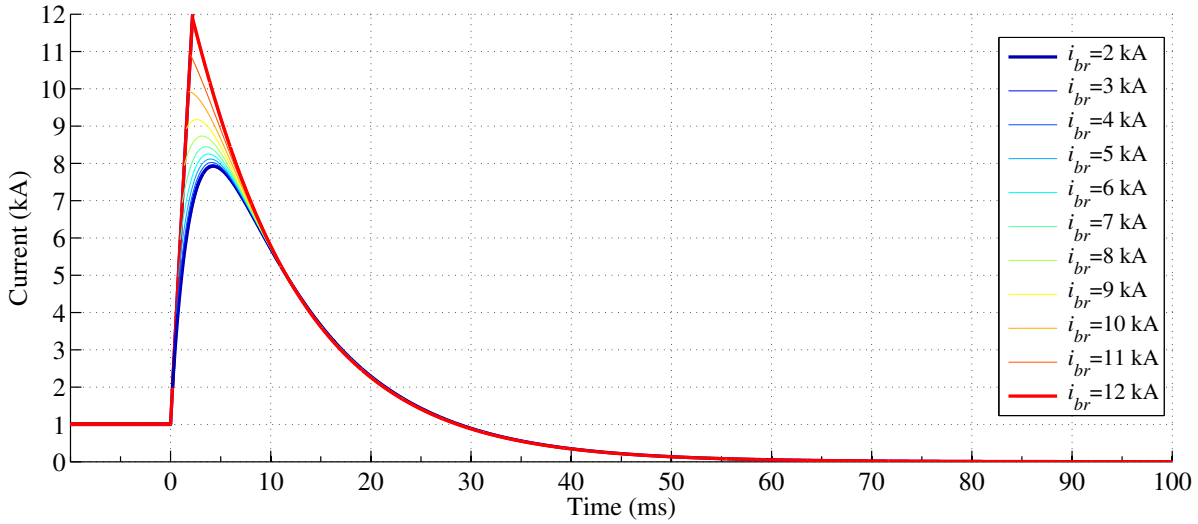
Figure 3.61: (a) Voltage and (b) current waveforms for designed CRCB.

voltage of capacitor below 260 kV increases the overvoltage across the CRCB. It can be seen in Figure 3.60(b) that larger capacitor voltage can increase the transmission line current peak slightly. However, the capacitor voltage does not have remarkable impact on the CRCB discharge time.

The impact of CRCB capacitor charged voltage on the CRCB voltage and the line current waveforms when the CRCB interrupts a fault current in 60% of its full interruption capacity is depicted in Figure 3.61(a) and (b). Figure 3.61(a) shows that maximum TIV reduces when the capacitor voltage is reduced from 360 kV to 180 kV. The reduction in the maximum TIV value is due to the impact of capacitor voltage on generated current peak in the current limiting inductor and the transmission line. As can be seen in Figure 3.61(b), despite the full current interruption case the transmission line current peak increases significantly when the capacitor charged voltage increases.



(a) Voltage across the MB unit



(b) The transmission line current before and after fault occurence

Figure 3.62: (a) Voltage and (b) current waveforms for designed CRCB.

Similar to the full current interruption case, the CRCB discharge time does not notably depend on the capacitor charged voltage.

Impact of Magnitude of Interrupted Current

The impact of fault current value at the interruption instance ($t = t_{br}$) on the CRCB performance is depicted in Figure 3.62(a) and (b). Since the CRCB is designed to interrupt the maximum fault current (in this case $I_{max} = 10$ kA), the interruption of lower currents can be done with lower TIV. It can be seen in Figure 3.62(a) that the interruption of a fault current with 2 kA magnitude causes 336 kV (1.05 pu) TIV across the CRCB whereas it can reach 340 kV (1.06 pu) when interrupting 10 kA. Note that, interruption of currents with larger value than the CRCB maximum current interruption capability increases the excessive voltage across the CRCB. Although

the maximum CRCB interruption capability is designed for 10 kA, the CRCB can interrupt a fault current with 110% of its maximum interruption capability with only 0.058% larger TIV. Figure 3.62(b) shows the current in transmission line for different magnitude of interrupted fault current. As can be seen the interrupted fault current magnitude does not have remarkable impact on the CRCB discharge time.

3.5.3 *Detailed Simulation Study*

Simulation Model

A four-terminal HVdc grid model which was initially proposed in [213] is employed to perform the simulation studies considering the impact of power converter on the behavior of designed CRCB. More details on four-terminal HVdc grid model are included in Appendix A. This simulation study focuses on operation of the CRCB at two dc buses. Figure 3.63 depicts the four-terminal HVdc grid model including CRCBs at both ends of transmission lines.

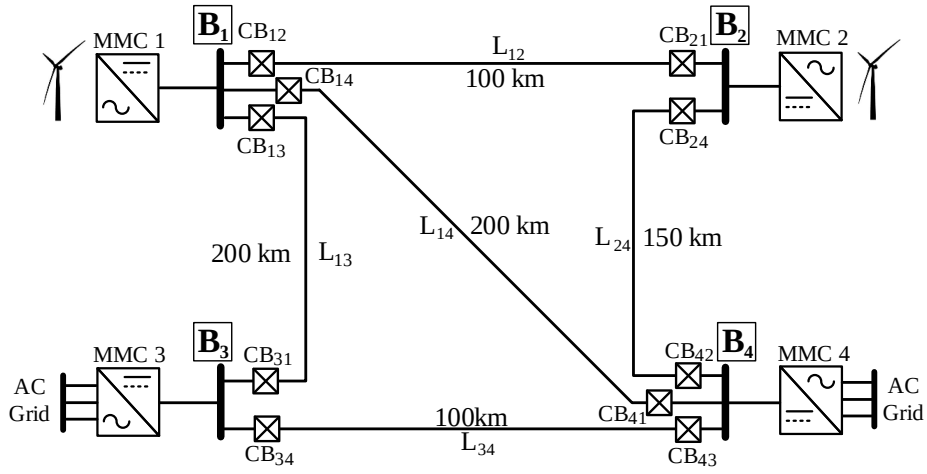
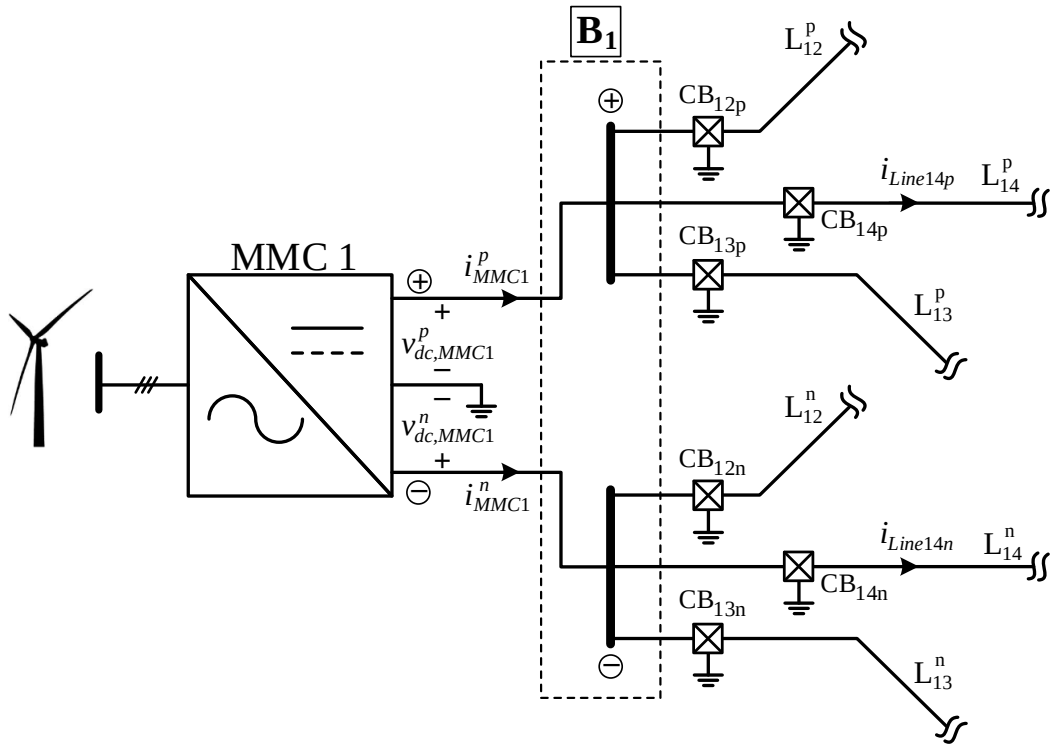


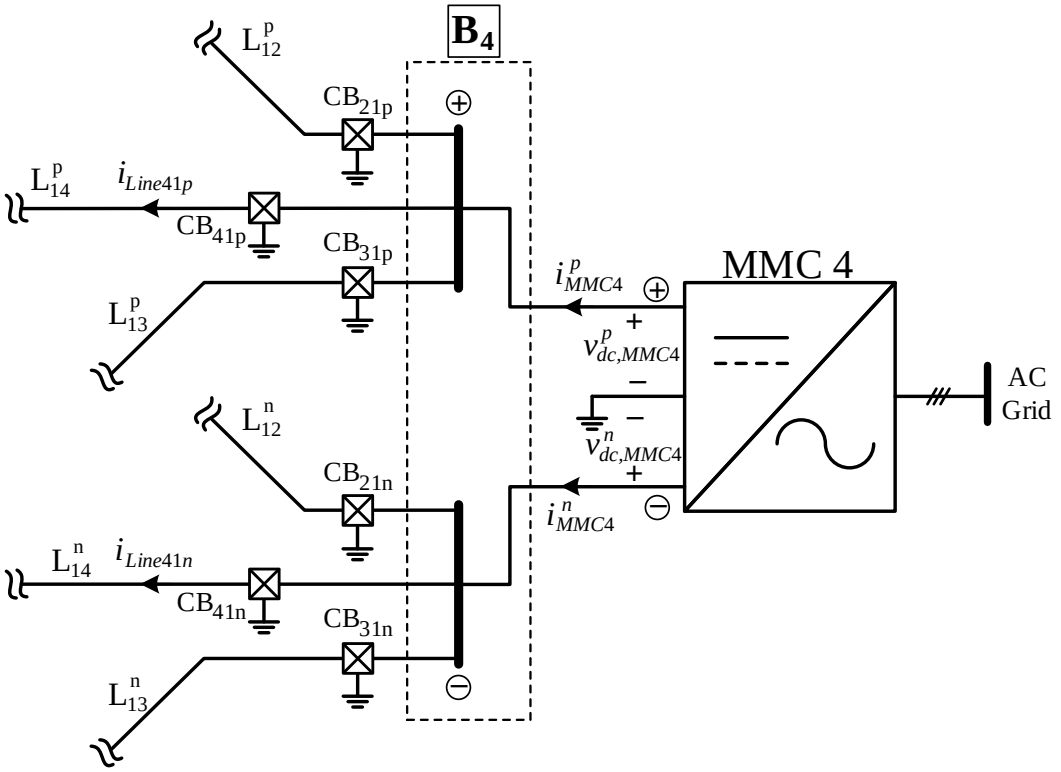
Figure 3.63: Test multi-terminal HVdc grid.

The test system model has a symmetric monopole configuration. The dc side ground point is available from the midpoint of converters' dc link capacitors. The CRCB can be integrated into the mentioned system based on the proposed configuration in Figure 3.11(b). Hence, each transmission line should be equipped by two CRCBs at each end. The directions of semiconductor switches in the negative pole CRCB should be different than the those of semiconductor switches in the positive pole CRCB. The CRCB attached to the positive pole transmission line ij is represented by CB_{ijp} and CB_{ijn} represents the CRCB attached to the negative pole transmission line ij. Figure 3.64(a) depicts dc bus 1 and its connections with MMC 1 and adjacent transmission lines. Figure 3.64(b) depicts dc bus 4 and its connections with MMC 4 and adjacent transmission lines.

The CRCB simulation models for positive and negative poles are shown in Figure 3.65 (a) and (b) respectively.

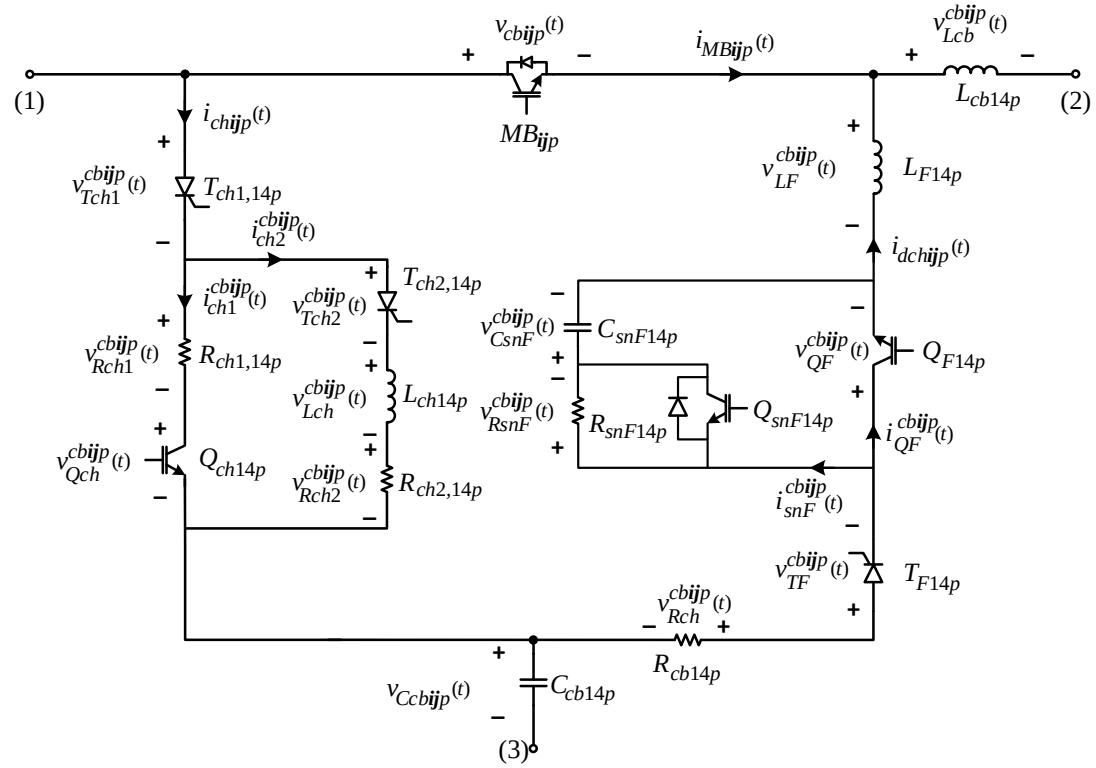


(a) MMC 1 and its associated dc buses and lines

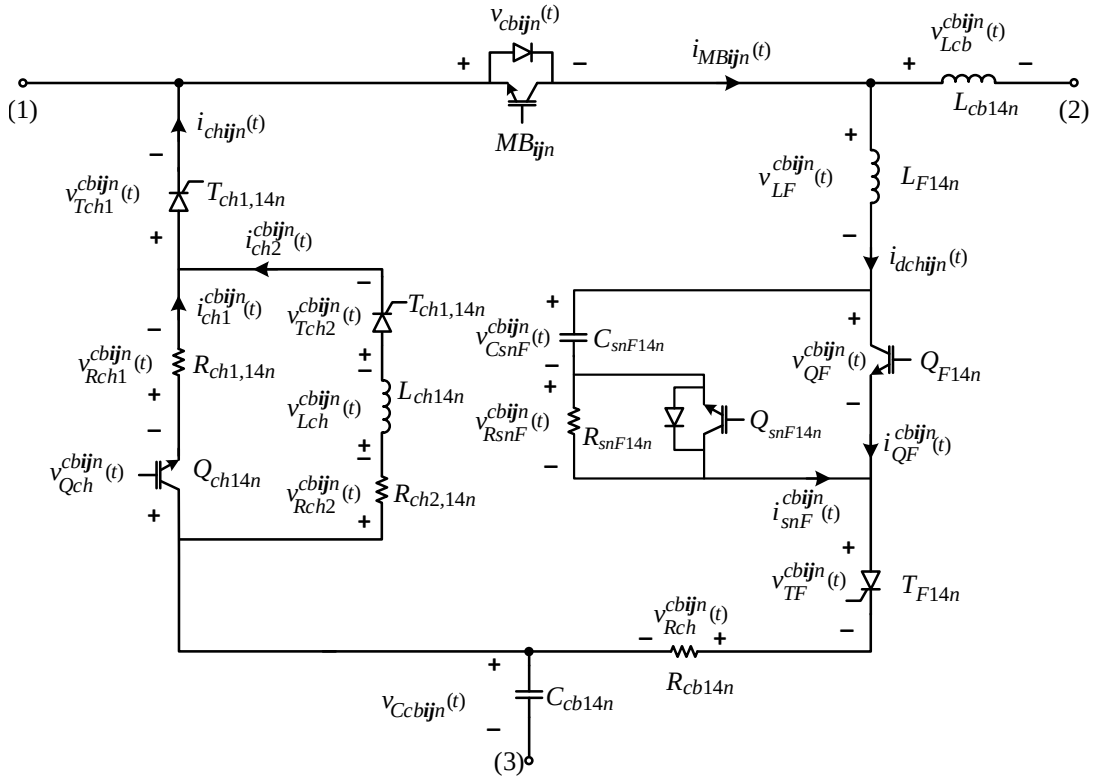


(b) MMC 4 and its associated dc buses and lines

Figure 3.64: MMC 1 and 4 and their associated buses and lines.



(a) Simulation model for the positive pole CRCB



(b) Simulation model for the negative pole CRCB

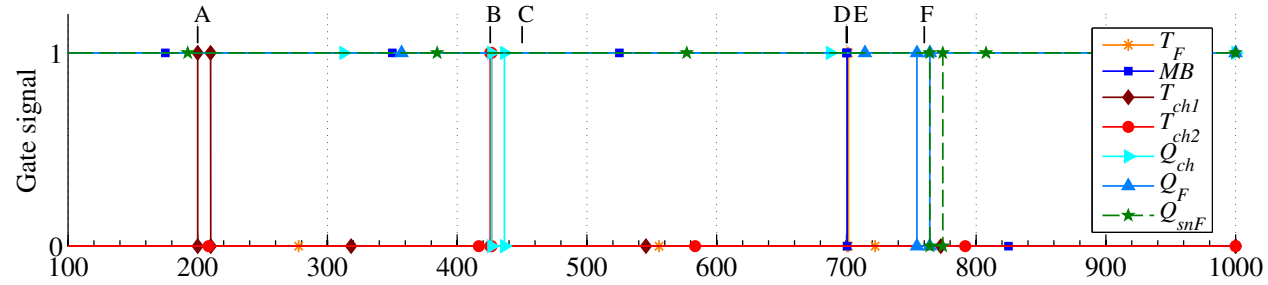
Figure 3.65: Simulation model for the positive and negative poles CRCBs.

Simulation Results For The Rectifier Side (Bus 1)

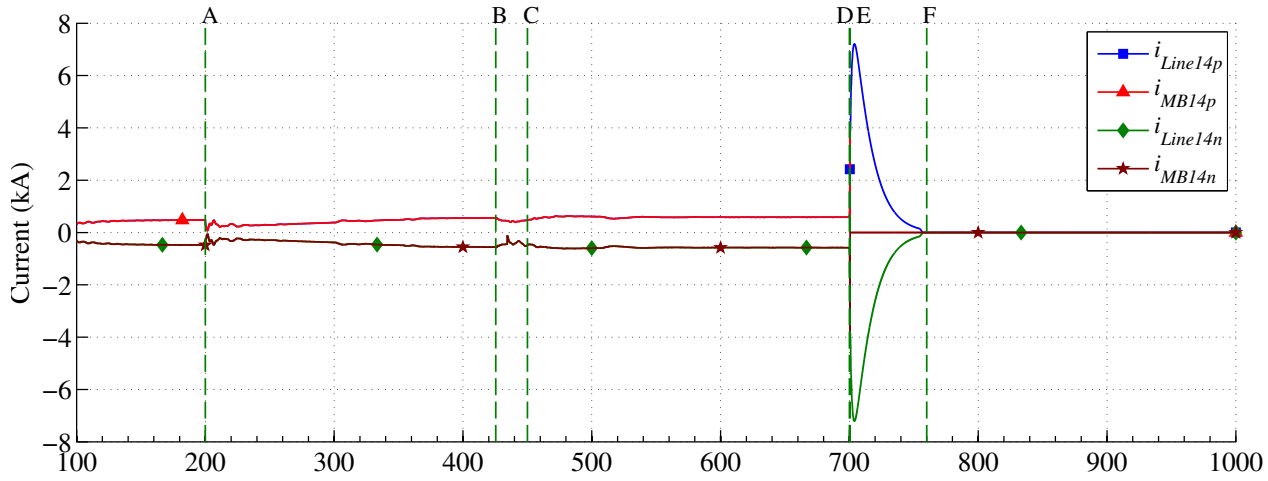
The detailed operation cycle of the CRCB in the symmetric monopole HVdc system is simulated using electromagnetic transient type software namely PSCAD. Figures 3.66 and 3.67 depict the most important parameters of the designed CRCB when interrupting a pole-to-pole short circuit fault at the midpoint of transmission line L_{14} at $t = 700$ ms. Therefore, the fault location has equal distances from CB_{14p}, CB_{14n}, CB_{41p} and CB_{41n}. Different stages of the CRCB operation are labeled by letters A, B, C, D, E and F in all figures, similar to subsection 3.5.2. The descriptions of labels are illustrated in Table 3.8.

Figure 3.66(a) shows the semiconductor switches gate signals in the CRCB structure. $T_{ch1,14p}$ and $T_{ch1,14n}$ are fired at $t = 200$ ms. The duration of gate pulse is set to 10 ms. $T_{ch2,14p}$ and $T_{ch2,14n}$ are fired after the charging current falls below 100 A. The charging current is shown in Figure 3.67(a). Simultaneously, Q_{ch14p} and Q_{ch14n} are turned off for duration 10 ms. Upon receiving the trip command, $T_{F14p}$and T_{F14n} are fired and MB_{14p} and MB_{14n} are opened. The pulse width for the gate of T_{F14p} and T_{F14n} is set to 3 ms in order to compensate the thyristor gate delay and the MB unit turn-on delay times. When the absolute value of discharging current falls below 150 A, Q_{F14p} and Q_{F14n} are opened for duration of 10 ms. Upon closing Q_{F14p} and Q_{F14n}, Q_{snF14p} and Q_{snF14n} are opened for duration of 10 ms, respectively in order to discharge C_{snF14p} and C_{snF14n} through R_{snF14p} and R_{snF14n}, respectively.

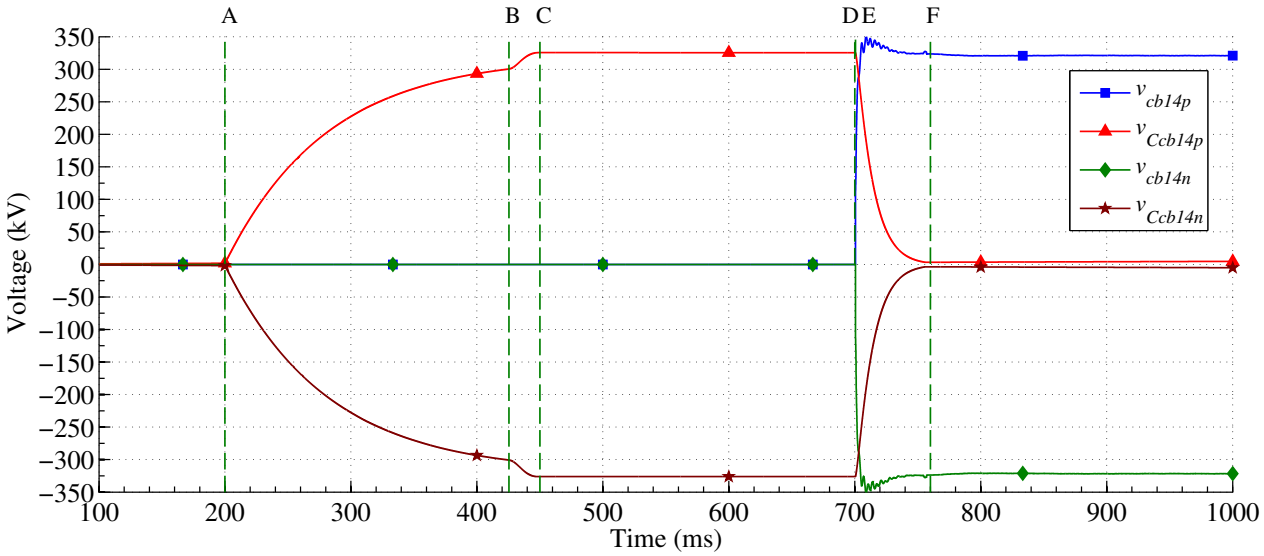
The transmission line and the MB unit currents for both negative and positive poles are depicted in Figure 3.66(b). The pre-fault current in transmission line L_{14} is equal to 577 A. As can be seen in Figure 3.66(b), the first charging stage reduces the transmission line and the MB unit current. This is due to higher charging current, which is drawn from MMC 1. The line current is recovered in almost 150 ms as the positive and negative poles CRCBs are charged up to the second charging stage threshold. The second charging stage starts at $t = 426$ ms (B) and it is accomplished at $t = 450$ ms (C). The transmission line and the MB unit currents are equal until the CRCBs trip (E). As soon as the short circuit fault happens on the transmission line, the current increases until the four-terminal test grid protection system sends the trip command to CB_{14p}, CB_{14n}, CB_{41p} and CB_{41n}. As can be seen in Figure 3.66(b), the fault current in line L_{14} is interrupted when it reaches 3.76 kA. As was explained in the previous sections, despite quick decrease in the MB unit current, the current in the transmission line reduces smoothly. In this stage, the transmission line current is equal to the capacitor discharging current. As can be seen in Figure 3.66(b), the current in the transmission line falls to zero in almost 58 ms in both negative and positive poles transmission lines.



(a) Gate signals for different semiconductor switches for CB_{14p}



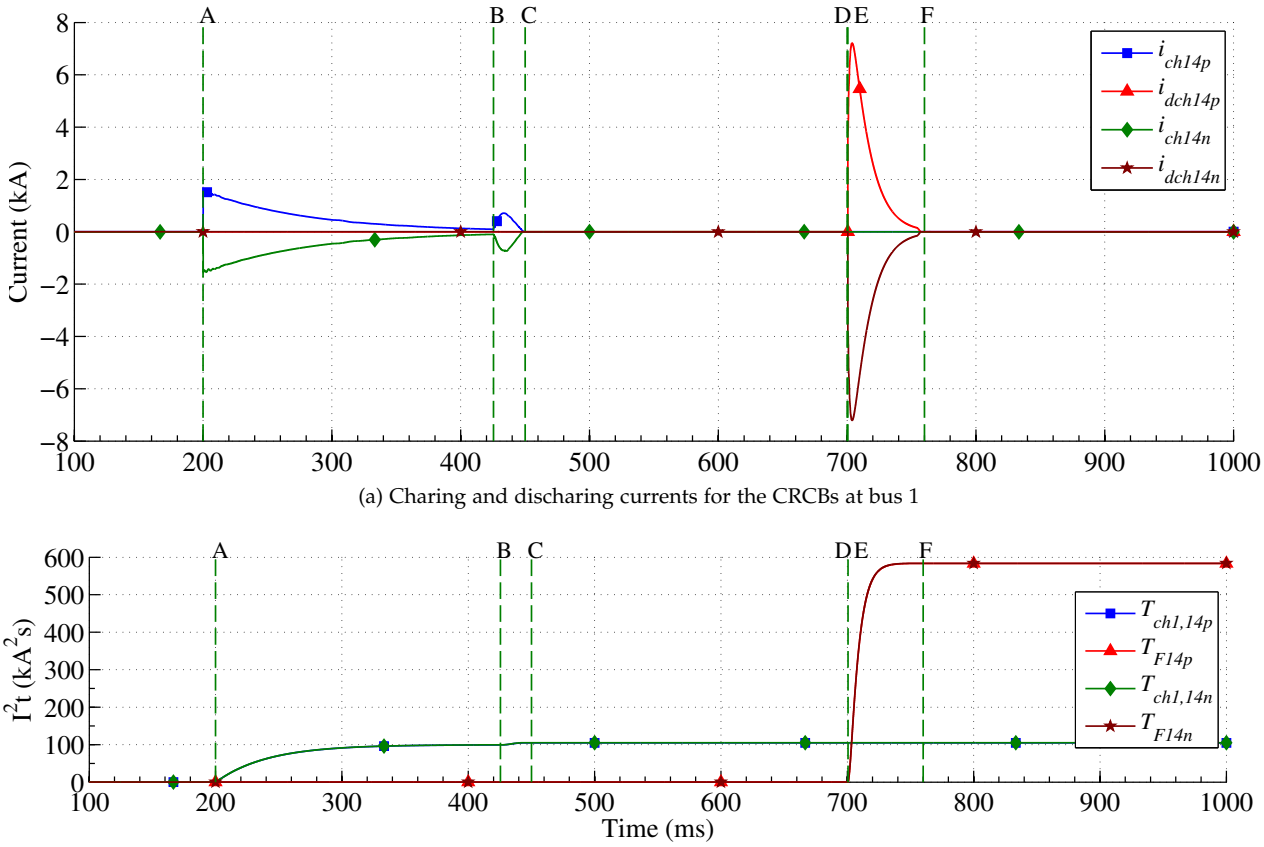
(b) Current in the positive and negative poles transmission lines and current in the MB units of the CRCBs at bus 1



(c) The CRCB and its capacitor voltage for positive and negative poles for the CRCBs at bus 1

Figure 3.66: Gate signals and current and voltage waveforms of positive and negative poles CRCBs during an operation cycle in a symmetric monopole HVdc grid.

Figure 3.66(c) shows the voltage across the MB unit of the CRCB and the CRCB capacitor voltage for positive and negative poles. The pre-fault voltage across MB unit is equal to the sum of the voltage drop across its semiconductor switches. The initial voltage of the CRCB capacitor is zero and as soon as T_{ch1p} in both positive and negative CRCBs are fired, their voltage starts increasing. As can be seen in the figure, the positive and negative poles capacitors voltage



(a) Charing and discharing currents for the CRCBs at bus 1

(b) I^2t for charging and discharging thyristors of the CRCBs at bus 1

Figure 3.67: Charging and discharging currents and I^2t value of thyristors in positive and negative poles CRCBs during an operation cycle in a symmetric monopole HVdc grid.

at the end of the first charging stage (B) reach +300 kV and -300 kV, respectively. After firing $T_{ch2,14p}$ and $T_{ch2,14n}$, due to the presence of L_{ch14p} and L_{ch14n}, the capacitor voltage reaches almost +325.49 kV and -325.94 kV, respectively. Upon the CRCB tripping, the absolute value of positive and negative poles capacitor voltages reduce until reach almost zero. As can be seen in Figure 3.66(c), the maximum TIVs across the MB units of positive and negative poles CRCBs are equal to +350 kV and -350 kV, respectively. The positive and negative poles CRCBs voltage after current interruption fall to +320 kV and -320kV, respectively.

Figure 3.67(a) shows the charging and discharging currents. The charging current peak in the first charging stage reaches almost 1.55 kA. The second peak of charging current happens at $t = 426$ ms and is equal to 706 A. The capacitor discharging current reaches almost 7.21 kA and then reduces smoothly until reaches 150 A. At this instance, Q_{F14p} and Q_{F14n} together with their snubber circuits are activated to commutate the discharging thyristor.

The I^2t value for $T_{ch1,14p}$, $T_{ch1,14n}$, T_{F14p} and T_{F14n} are shown in Figure 3.48(b). The total I^2t value for the charging stage in both positive and negative poles CRCBs reaches 104.79 kA^2s, which is almost equal to the value obtained using the analytical equations. The

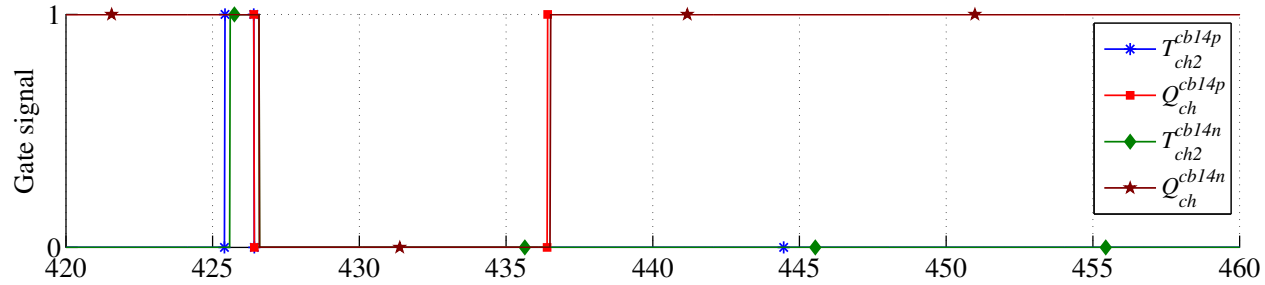
total I^2t value for T_{F14p} and T_{F14n} is equal to 583.18 kA^2s.

Figure 3.68 illustrates the behavior of relevant components of CB_{14p} and CB_{14n} during the second charging stage. Figure 3.68(a) shows the gate signals for T_{ch2} and Q_{ch} in positive and negative poles CRCBs. The pulse width for firing T_{ch2} is equal to 1 ms.

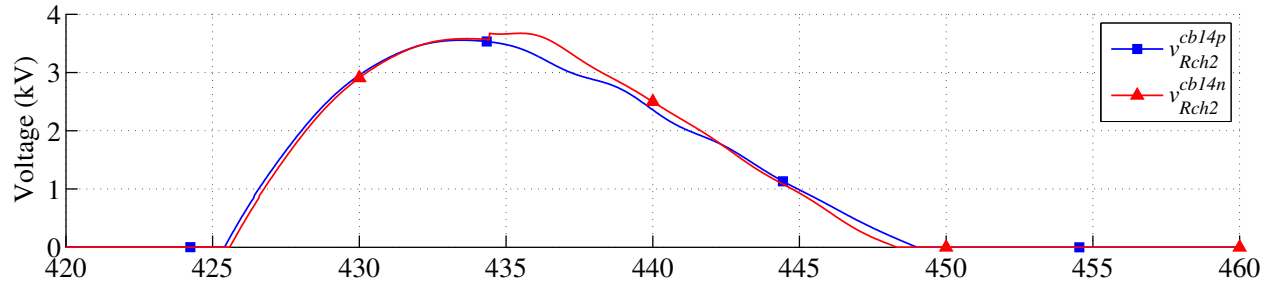
Figure 3.68(b) depicts the voltage across $R_{ch2,14p}$ and $R_{ch2,14n}$. The voltage across R_{ch2} reaches almost 3.6 kV, which confirms the low voltage rating of this resistor. The voltage across $L_{ch2,14p}$ and $L_{ch2,14n}$ is shown in Figure 3.68(c). After firing T_{ch2} (in positive and negative CRCBs), the current in $L_{ch2,14p}$ and also $L_{ch2,14n}$ cannot change instantaneously. Therefore, at the initial instance the voltage across $R_{ch2,14p}$ and $R_{ch2,14n}$ is equal to the voltage difference between the dc bus and the CRCB capacitors (positive and negative poles), which is almost equal to 19 kV. Thereafter, the current in the inductors increases and their voltage decreases gradually. The voltage across the semiconductor switches Q_{ch14p} and Q_{ch14n} is depicted in Figure 3.68(d). The voltage across the semiconductor switches Q_{ch14p} and Q_{ch14n} increases up to the voltage difference between the dc bus and the CRCB capacitor at the instance of truing off (In this case the voltage difference is almost equal to 16 kV). In continue, the voltage across the inductor changes its polarity. However, as soon as its current falls to zero, its voltage also falls to zero. This is due to the presence of thyristors T_{ch1} and T_{ch2} in positive and negative poles CRCBs, which do not allow the current reversal.

Figure 3.68(e) shows the sum of voltages across the thyristors $T_{ch1,14p}$ and $T_{ch2,14p}$ and also $T_{ch1,14n}$ and $T_{ch2,14n}$. As can be seen in the figure, upon firing T_{ch2} in positive and negative poles CRCBs, the voltage across both thyristors in each CRCB falls to zero due to the conduction of both of them. At the end of charing period, due to the extra charged voltage in the CRCB capacitor, the voltage across the thyristors in the positive pole CRCB is equal to -4 kV and in the negative pole CRCB is equal to -2 kV.

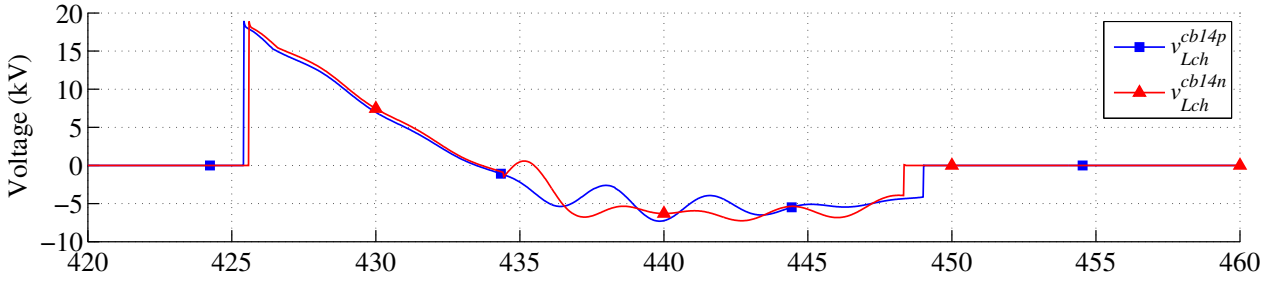
The behavior of most relevant components during the final stage of the CRCB discharge is illustrated in Figure 3.69. Figure 3.69(a) shows the gate signals for semiconductor switches Q_F and Q_{snF} for both negative and positive poles. Q_F is opened when the discharging current (i_{dch}) falls below 150 A for duration of 10 ms while Q_{snF} is closed during the mentioned period. Figure 3.69(b) depicts the current in the thyristor commutator circuit. The discharging current is redirected into the thyristor commutator circuit after opening Q_{F14p} and Q_{F14np}. The current in the thyristor commutator circuit charges C_{snF14p} in the positive pole CRCB and C_{snF14n} in the negative pole CRCB.



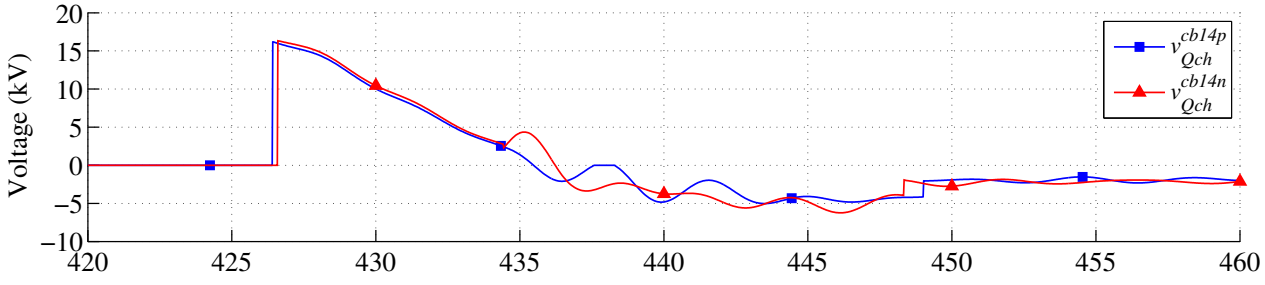
(a) Gate signals of T_{ch2} and Q_{ch} for positive and negative poles CRCBs



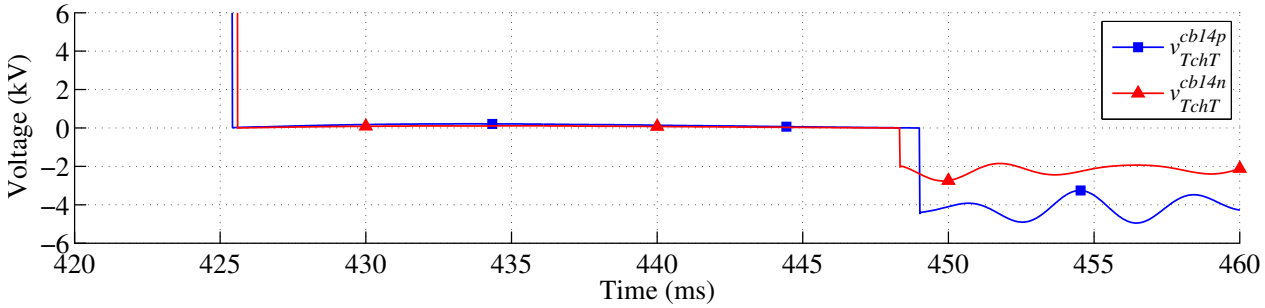
(b) Voltage across R_{ch2} in positive and negtive poles CRCBs



(c) Voltage across L_{ch} in positive and negtive poles CRCBs

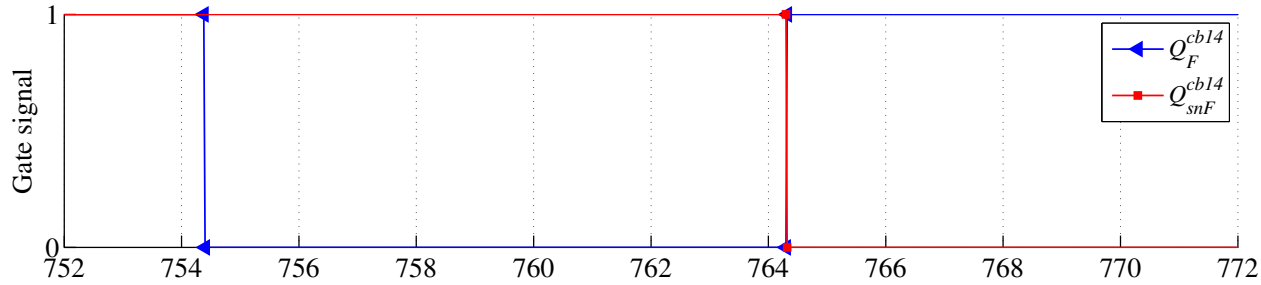


(d) Voltage across Q_{ch} in positive and negtive poles CRCBs

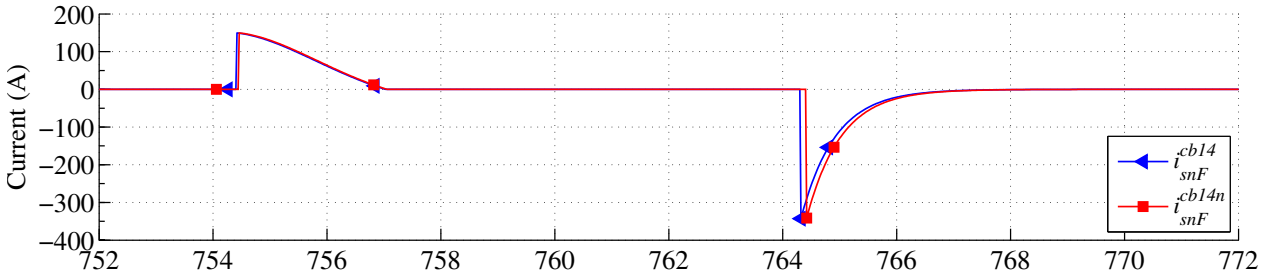


(e) The sum of voltages across T_{ch1} and T_{ch2}

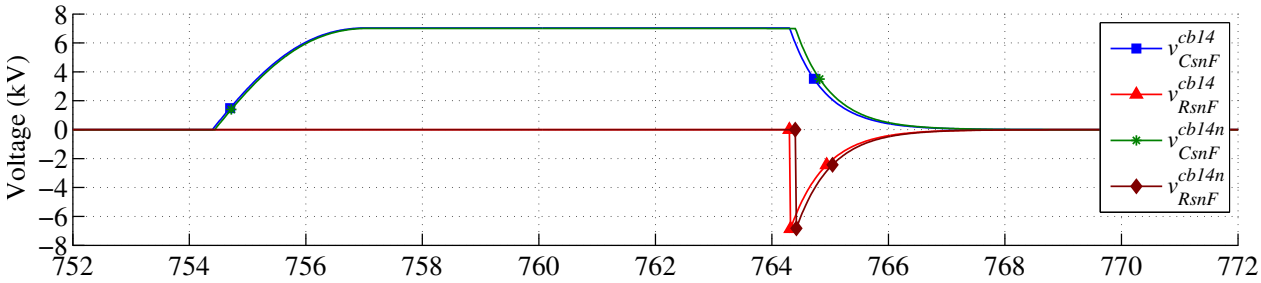
Figure 3.68: Current and voltage waveforms of relevant components' during the second charging stage in positive and negative poles CRCBs.



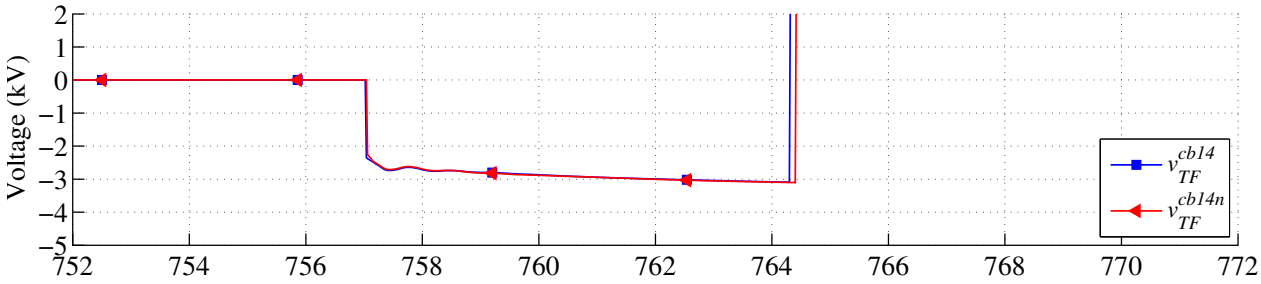
(a) Gate signals of Q_F and Q_{snF} for positive and negative poles CRCBs



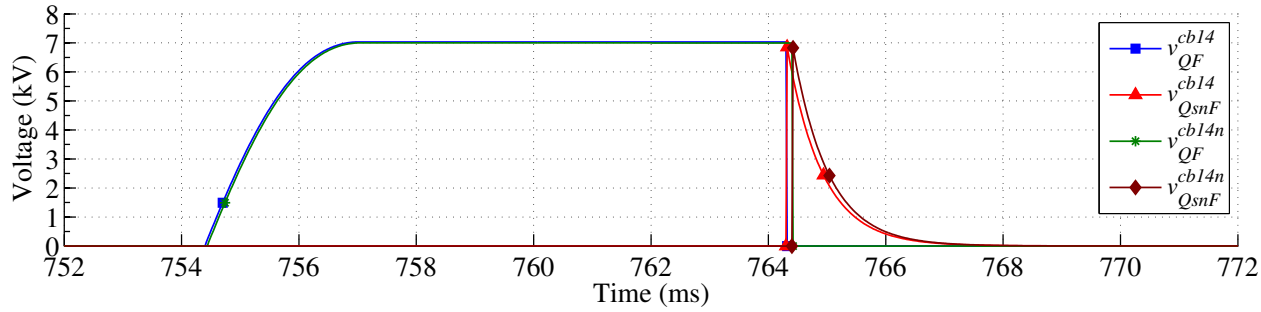
(b) Current in the discharging thyrisyor current commutator circuit



(c) Voltage across C_{snF} and R_{snF} in positive and negtive poles CRCBs

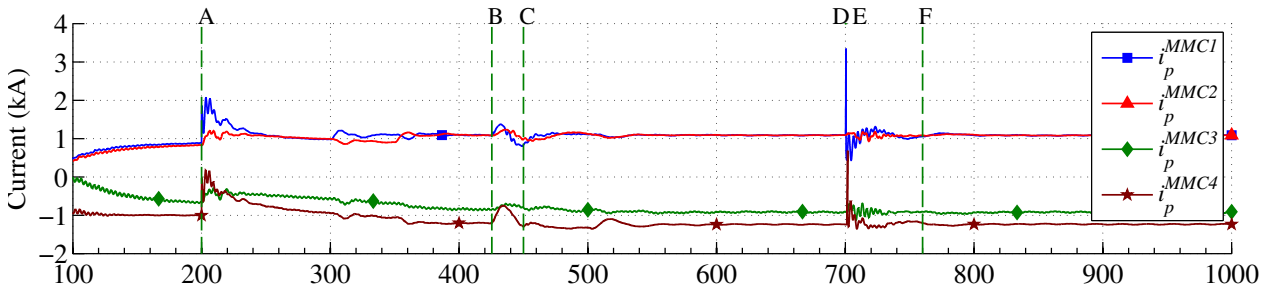


(d) Voltages across T_F in positive and negtive poles CRCBs

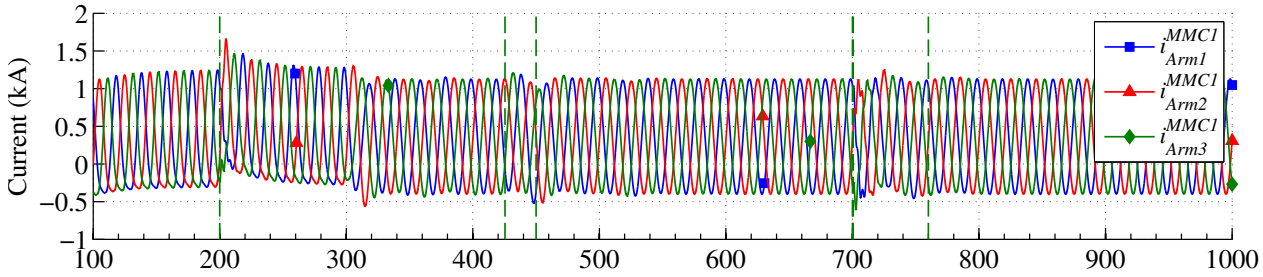


(e) Voltage across Q_F and Q_{snF} in positive and negtive poles CRCBs

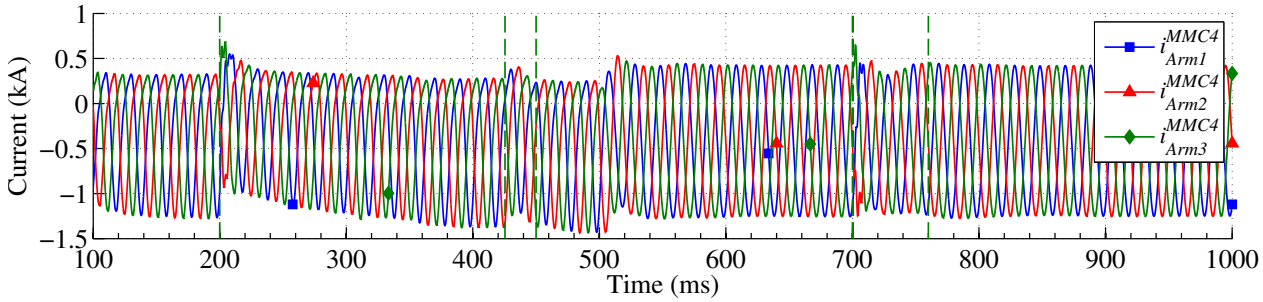
Figure 3.69: Current and voltage waveforms of relevant components' during discharging thyristor current commutation stage in positive and negative poles CRCBs.



(a) Currents in the dc side of converters MMC 1, 2, 3 and 4



(b) Arm currents in MMC 1



(c) Arm currents in MMC 4

Figure 3.70: Arm currents and dc side currents in MMCs.

The capacitors (C_{snF14p} and C_{snF14n}) voltage is shown in Figure 3.69(c). It can be seen that the capacitors are charged up to almost 7 kV. Furthermore, Figure 3.69(c) shows the voltage across R_{snF14p} and R_{snF14n}. The voltage across the mentioned resistors reaches 7 kV upon opening Q_{snF14p} and Q_{snF14n}. Figure 3.69(d) shows the voltage across the thyristors T_{F14p} and T_{F14n}. The voltage across the thyristors become equal to almost 3 kV when the current in the commutator circuits (i_{snF}^{14p} and i_{snF}^{14n}) reach zero. The negative voltage across the thyristor bank grantees the successful turn-off of the switch.

At the end of this cycle, Q_{snF14p} and $Q_{snF14pn}$ are opened whereas Q_{F14p} and Q_{F14n} are closed. In this stage, if the capacitors of commutator circuits have some charge, they can be discharged via R_{snF14p} and R_{snF14n}. The voltage across Q_{F14p}, Q_{F14n}, Q_{snF14p} and Q_{snF14n} is shown in Figure 3.69(e). Q_{F14p}, Q_{F14n}, Q_{snF14p} and Q_{snF14n} are required to be rated for the maximum charged voltage of C_{snF14p} and C_{snF14n}.

The dc side currents of MMC 1, 2, 3 and 4 are shown in Figure 3.70(a). MMC 1 dc side current rises up to almost 2 kA when the first

charging stage starts. Since MMC 4 operates in the inverter mode, its dc side current falls to zero when the first charging stage starts. The current disturbance in the second stage of charging is quite small as compared to the first charging stage. The arm currents in MMC 1 are depicted in Figure 3.70(b). As can be seen in the figure, the current in Arm 2 reaches almost 1.65 kA when the first charging stage starts. This value is smaller than the blocking threshold of MMC 1. The arm current of MMC 1 increases almost 100 A when the second charging stage starts. Figure 3.70(c) shows the arm currents in MMC 4. It can be seen in the figure that the current in Arm 2 reaches almost 0.7 kA when the first charging stage starts. This value is smaller than the blocking threshold of MMC 4. The arm current of MMC 4 increases almost 250 A when the second charging stage starts. The difference in behavior of MMC 1 and MMC 2 is due to their different operation modes.

Simulation Results For The Inverter Side (Bus 4)

As mentioned in the previous subsection, the pole-to-pole short circuit fault happens at $t = 700$ ms at the midpoint of transmission line L_{14}. Therefore, In addition to CB_{14p} and CB_{14n}, CB_{41p} and CB_{41n} must trip. Figures 3.71 and 3.72 depict the most important parameters of CB_{41p} and CB_{41n} when interrupting the fault current. Different stages of the CRCB operation are labeled by letters A, B, C, D, E and F in all figures, similar to the previous subsection. The descriptions of labels are illustrated in Table 3.8.

Figure 3.71(a) shows the semiconductor switches gate signals in the CRCB structure. $T_{ch1,41p}$ and $T_{ch1,41n}$ are fired at $t = 200$ ms. The duration of gate pulse is set to 10 ms. $T_{ch2,41p}$ and $T_{ch2,41n}$ are fired after the absolute value of charging current falls below 100 A. The charging current is shown in Figure 3.72(a). Simultaneously, Q_{ch41p} and Q_{ch41n} are turned off for duration 10 ms. Upon receiving the trip command, T_{F41p} and T_{F41n} are fired and MB_{41p} and MB_{41n} are opened. The pulse width for the gate of T_{F41p} and T_{F41n} is set to 3 ms in order to compensate the thyristor gate delay and the MB unit turn-on delay times. When the absolute value of discharging current falls below 150 A, Q_{F41p} and Q_{F41n} are opened for duration of 10 ms. Upon closing Q_{F41p} and Q_{F41n}, Q_{snF41p} and Q_{snF41n} are opened for duration of 10 ms, respectively in order to discharge C_{snF41p} and C_{snF41n} through R_{snF41p} and R_{snF41n}, respectively.

The transmission line and the MB unit currents for both negative and positive poles are depicted in Figure 3.71(b). As can be seen in Figure 3.71(b), despite the CRCBs at the rectifier side, the first charging stage increases the transmission line and the MB unit current. In the inverter side the a portion of charging current is drawn from transmission line L_{14}. Similar to the rectifier side, the line current is recovered in almost 150 ms as the positive and negative poles CRCBs are charged up to the second charging stage threshold. The second charging stage starts at $t = 426$ ms (B) and it is accomplished at

$t = 450$ ms (C). The timings of charging stages are equal to the those of CRCBs at the rectifier side. The transmission line and the MB unit currents are equal until the CRCBs trip (E). CB_{41p} and CB_{41n} receives trip command at $t = 701.8$ ms. As can be seen in Figure 3.71(b), the fault current in line L_{14} is interrupted when it reaches 2.4 kA. During the current interruption process, the transmission line current is equal to the capacitor discharging current. As can be seen in Figure 3.71(b), the current in the transmission line falls to zero in almost 50 ms in both negative and positive poles transmission lines.

Figure 3.71(c) shows the voltage across the MB unit of the CRCB and the CRCB capacitor voltage for positive and negative poles. As can be sen in the figure, the positive and negative poles capacitors voltage at the end of the first charging stage (B) reach +300 kV and -300 kV, respectively. After firing $T_{ch2,41p}$ and $T_{ch2,41n}$, due to the presence of L_{ch41p} and L_{ch41n}, the capacitor voltage reaches almost +325.29 kV and -325.54 kV, respectively. Upon the CRCB tripping, the absolute value of positive and negative poles capacitor voltages reduce until reach almost zero. As can be seen in Figure 3.66(c), the maximum TIVs across the MB units of positive and negative poles CRCBs are almost equal to +350 kV and -350 kV, respectively. The positive and negative poles CRCBs voltage after current interruption fall to +320 kV and -320kV, respectively.

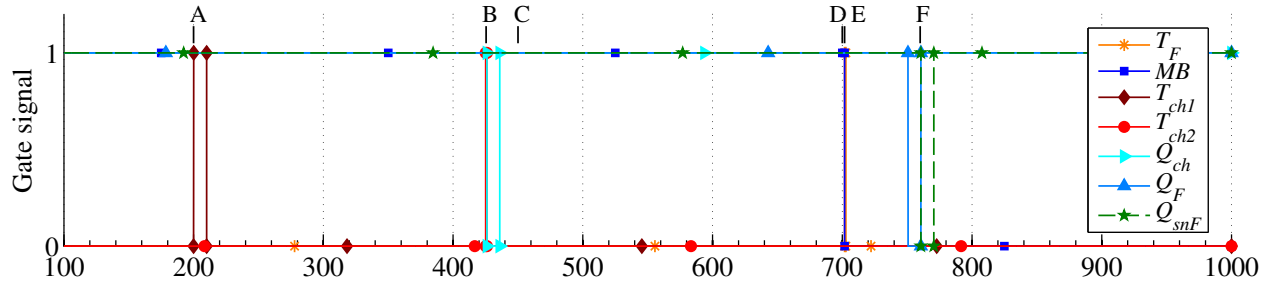
Figure 3.72(a) shows the charging and discharging currents. The charging current peak in the first charging stage reaches almost 1.54 kA. The second peak of charging current happens at $t = 426$ ms and is equal to 704 A. The capacitor discharging current reaches almost 6.2 kA and then reduces smoothly until reaches 150 A. At this instance, Q_{F41p} and Q_{F41n} together with their snubber circuits are activated to commutate the discharging thyristor.

The I^2t value for $T_{ch1,41p}$, $T_{ch1,41n}$, T_{F41p} and T_{F41n} are shown in Figure 3.72(b). The total I^2t value for the charging stage in both positive and negative poles CRCBs reaches 104.58 kA^2s, which is almost equal to the value obtained using the analytical equations. The total I^2t value for T_{F14p} and T_{F14n} is equal to 582.41 kA^2s.

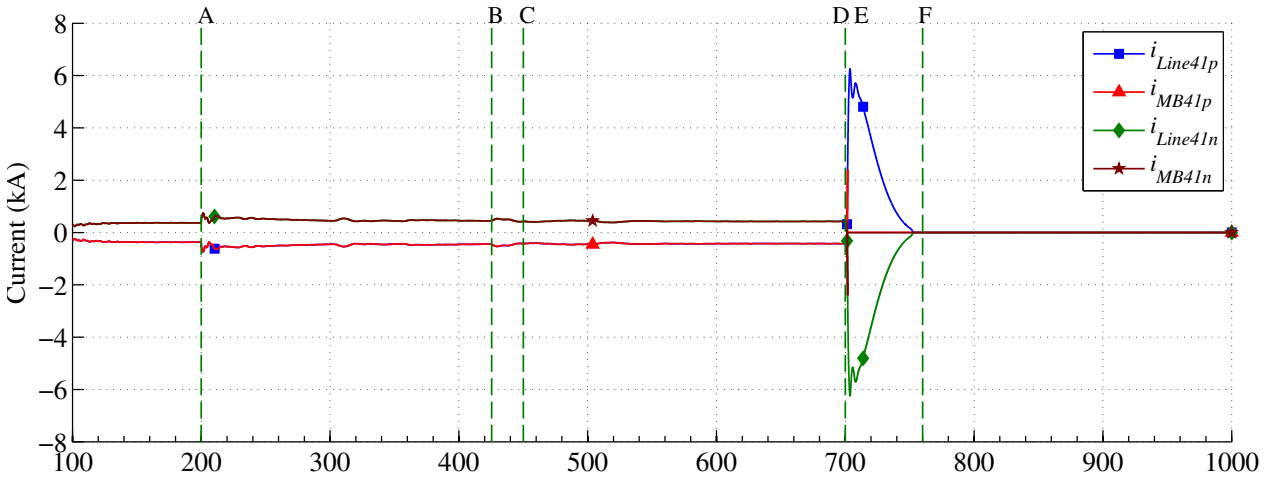
Impact of Converter Behavior on TIV of CRCB

Figure 3.73(a) depicts the voltage of dc buses 1 and 4 in operation cycle of the CRCBs. As can be seen in the figure, when the first charging stage starts, the positive and negative dc bus voltage of MMC 1 falls o 299 kV and -299 kV, respectively. In case of MMC 4, the dc bus voltage drop is smaller as compared to MMC 1 (almost 1 kV).

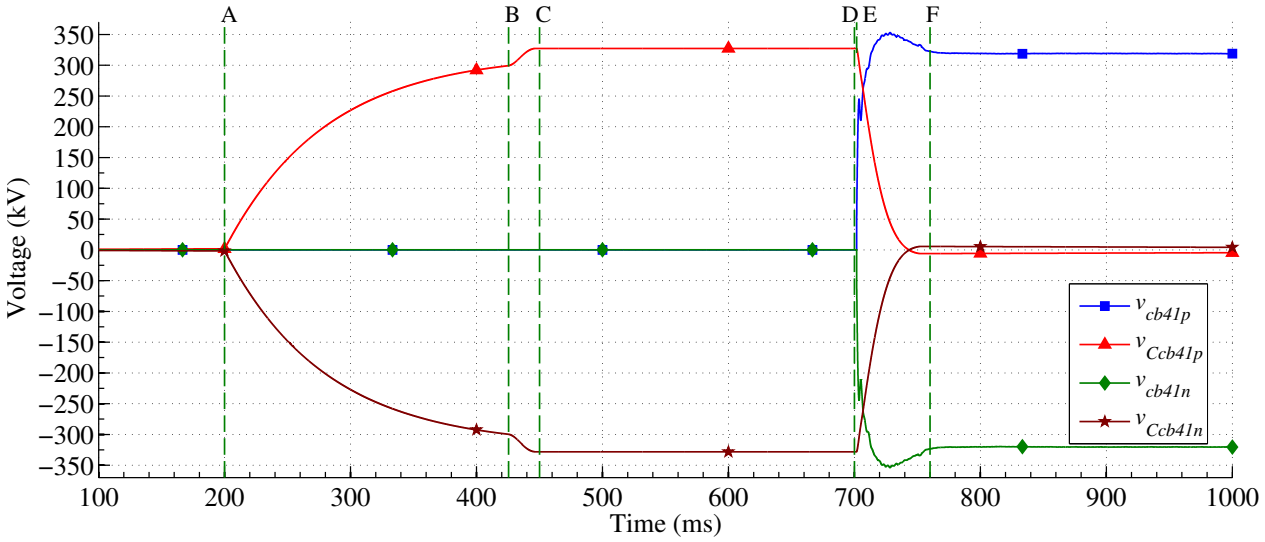
The impact of second charging stage is almost negligible on the voltage of dc buses 1 and 4. The impact of short circuit fault occurrence on the voltage of dc buses is depicted in Figure 3.73(b)-(e). As can be seen in Figure 3.73(b), after short circuit fault occurs, the dc bus 1 positive pole voltage decreases until the CRCB interrupts the fault current. Thereafter, a few overshoots can be observed in the



(a) Gate signals for different semiconductor switches for CB_{41p}



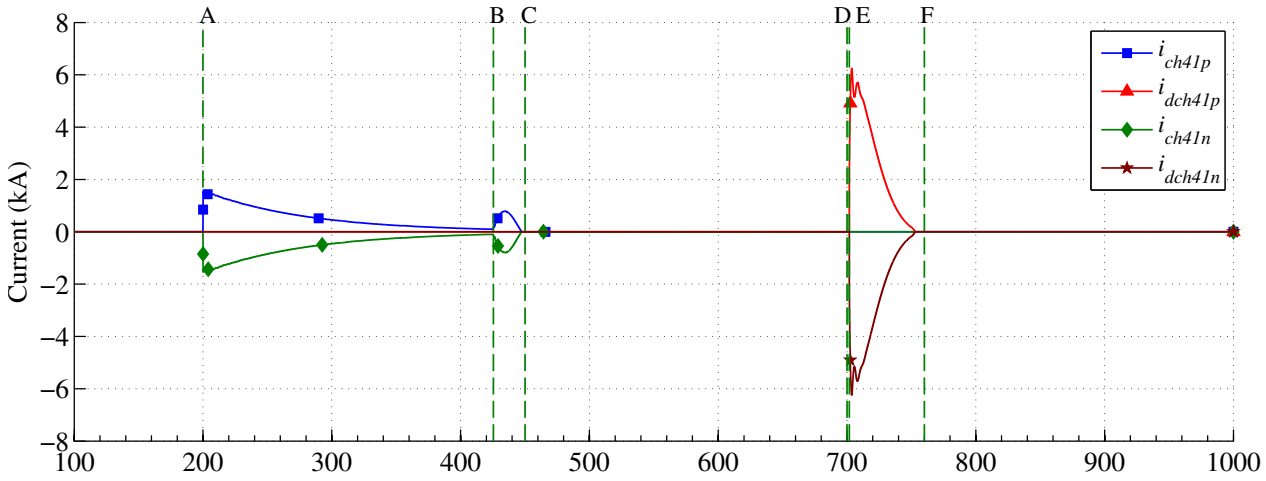
(b) Current in the positive and negative poles transmission lines and current in the MB units of the CRCBs at bus 4



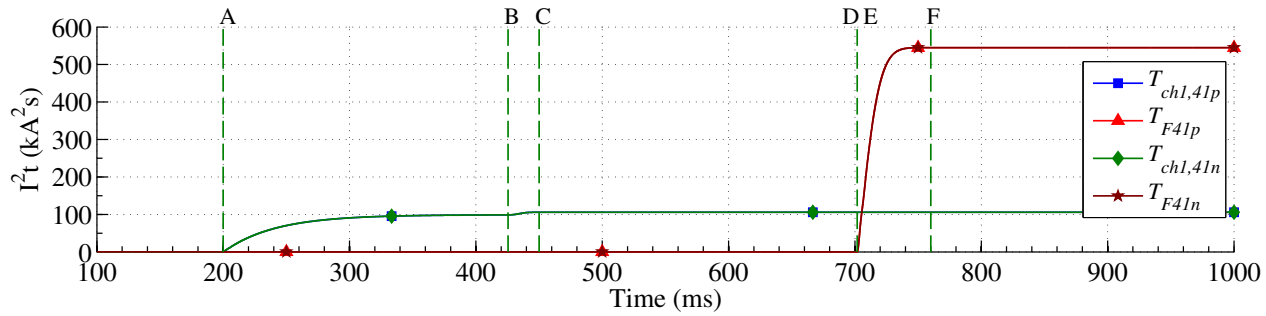
(c) The CRCB and its capacitor voltage for positive and negative poles for the CRCBs at bus 4

Figure 3.71: Gate signals, current and voltage waveforms of positive and negative poles CRCBs.

voltage since the MMC 1 tries to regulate the dc bus voltage. The maximum overshoot depends on the MMC control system behavior and dc bus capacitor size. It can be seen in Figure 3.73(b) that the positive dc bus voltage of MMC 1 after fault current interruption reaches 350 kV whereas Figure 3.73(c) shows that the positive dc bus voltage of MMC 4 reaches 332.5 kV. Figure 3.73(c) shows the negative pole voltage at dc bus 1. It can be seen in the figure that the absolute



(a) Charing and discharging currents for the CRCBs at bus 4

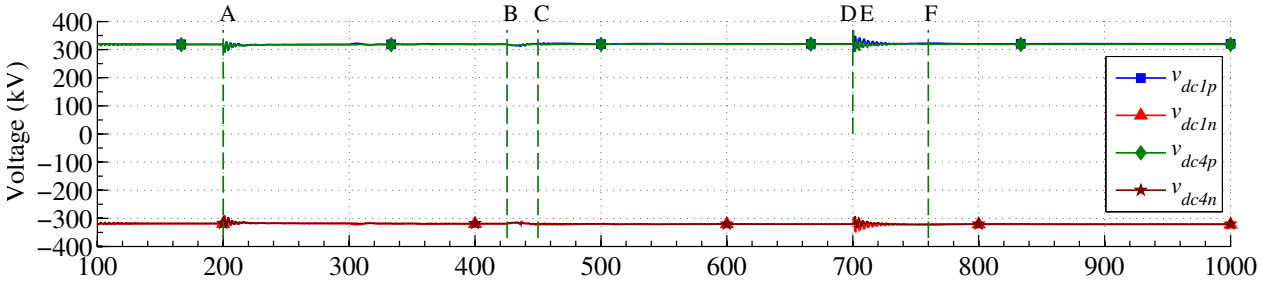


(b) I^2t for charging and discharging thyristors of the CRCBs at bus 1

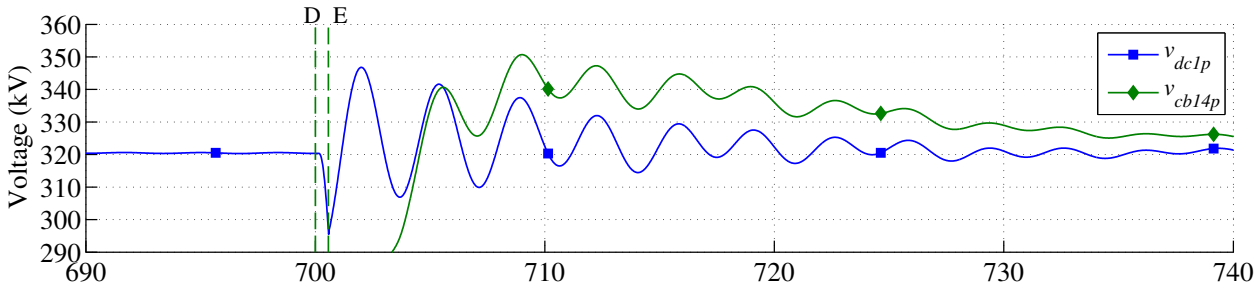
Figure 3.72: Charging and discharging currents and I^2t value of thyristors in positive and negative poles CRCBs during an operation cycle in a symmetric monopole HVdc grid.

value of voltage drops to 296 kV. The negative pole voltage at dc bus 4 is depicted in Figure 3.73(e). The absolute value of negative pole voltage at dc bus 4 drops to 291 kV.

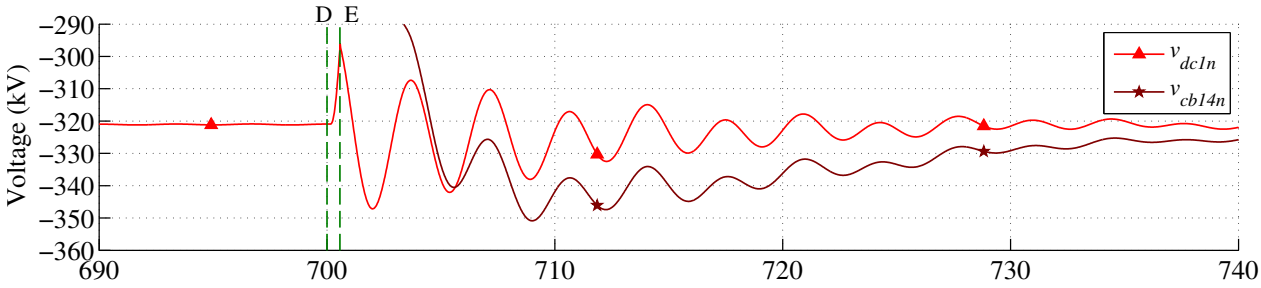
As can be seen in Figure 3.73, the maximum TIV across the CRCB is slightly larger than the value of TIV obtained from analysis. This is mainly due to the voltage fluctuation at the the dc buses after current interruption. The voltage fluctuation at the rectifier side is larger as compared to the inverter side and hence the value of maximum TIV at the inverter (332.5) side is smaller than that at the rectifier side (350 kV). The largest maximum TIV value on all studied CRCBs is equal to 1.093 pu. Therefore, it still satisfies the design requirements from previous section, which was set to 1.15 pu.



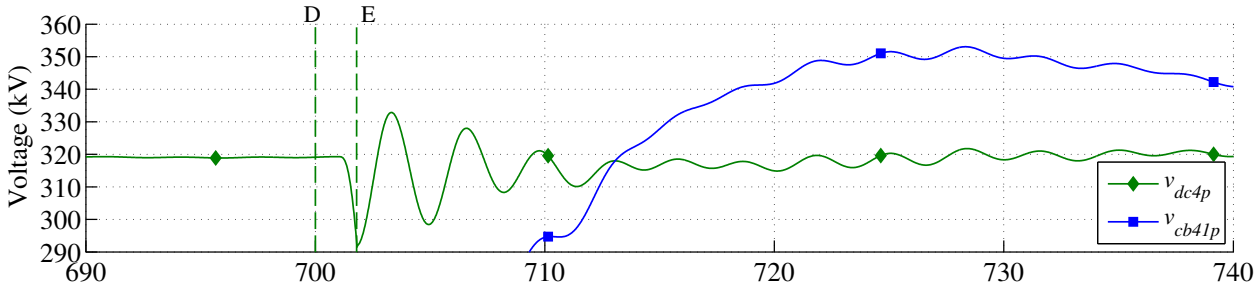
(a) Negative and positive voltages at dc buses 1 and 4



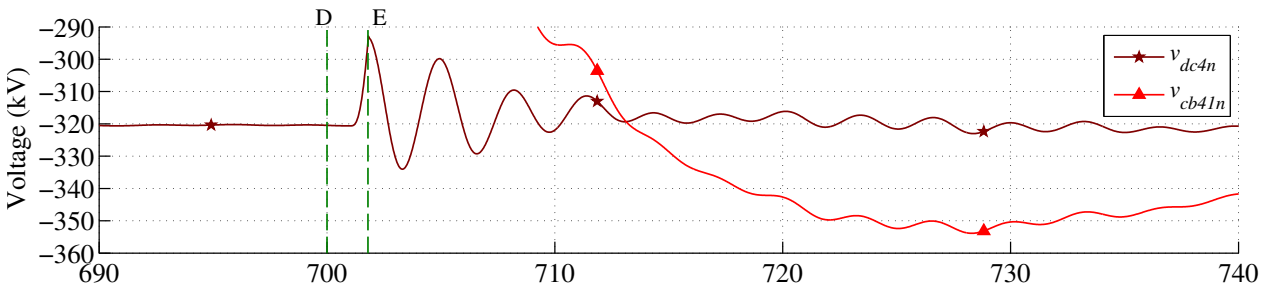
(b) Voltage across CB_{14p} and the positive voltage at dc bus 1



(c) Voltage across CB_{14p} and the negative voltage at dc bus 1



(d) Voltage across CB_{41p} and the positive voltage at dc bus 4



(e) Voltage across CB_{41n} and the negative voltage at dc bus 4

Figure 3.73: The voltage across CRCBs and corresponding dc buses.

3.6 Lab-scale Prototype

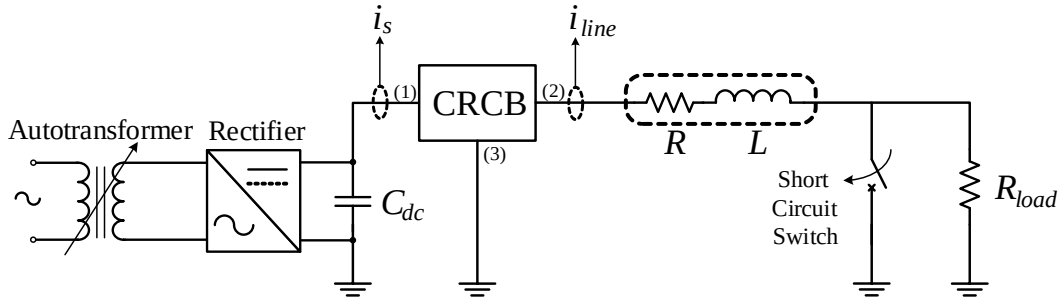
A low voltage prototype has been built up to examine the practical functionality of the proposed CRCB. The employed components for implementation of the CRCB are illustrated in Table 3.9.

Component	Part number	Type	Description
T_F, T_{ch}	BT152-400R	Thyristor	Thyristor
MB, Q_{ch}, Q_F	HGTG20N60B3	N-Channel IGBT	600 V, 40 A
R_{ch}	6.3 Ω	Resistor	5 W
R_{cb}	4.7 Ω	Resistor	5 W
C_{cb}	1000 μF	Capacitor	200 V
R_{load}	27 Ω	Resistor	150 W
R	600 mΩ	Resistor	Equivalent series resistance of the line inductor
L	6.2 mH	Inductor	-
C_{dc}	6600 μF	Capacitor	300 V
IGBT Driver	HCPL316J	IC	2.5 Amp gate drive optocoupler
Voltage sensor	ACPL-C87	IC	Precision optically isolated voltage sensor
Current sensor	ACS712	IC	Hall effect-based linear current sensor IC
Controller	dspic30F4011	IC	16-bit,120 MHz digital signal controller

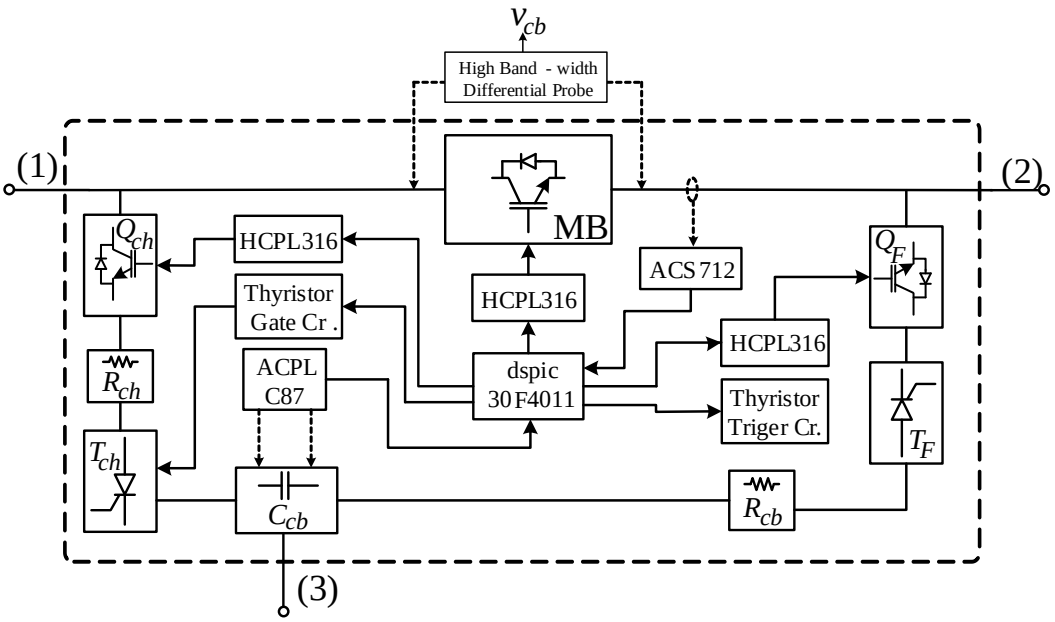
Table 3.9: Employed components for prototyping.

Fig. 3.74(a) shows the experimental setup configuration. As can be seen in Figure 3.74(a) the CRCB is connected to a dc link, which is fed by an autotransformer through a diode rectifier. The transmission line and the current limiting inductor is represented by an inductor and its equivalent series resistance. A short circuit fault is placed using an ac mechanical circuit breaker. Figure 3.74(b) shows the internal block diagram of implemented CRCB. The line current is measured using a hall effect-based linear current sensor. In order to carry out the experiment, the short circuit is detected by an overcurrent detector program, which is developed on a 16-bit digital signal controller. The threshold of overcurrent detector is set to 17.5 A. Note that the no-load dc link voltage is 135 V whereas it drops to 108 V when the resistive load is connected. The pre-fault current of system is almost 4 A. The gate signal of MB unit IGBT is changed to 15 V after the thyristor gate pulse is generated. The thyristor gate pulse width is set to 1 ms. The implemented CRCB is depicted in Figure 3.75.

The experimental results have been observed and recorded using a DSOX2024A Agilent oscilloscope. The dc source and CRCB voltage waveforms are shown in Figure 3.76. As can be seen in Figure 3.78, the voltage increases sharply up to 108 V and thereafter rises up to the dc link no-load voltage value (135 V), smoothly. As can be seen in the area, which is marked by red arrow and "A" letter the dc source voltage increases to its no-load value after the fault current is interrupted. Therefore, the slight difference between the dc source voltage and the CRCB voltage right after fault interruption can be considered as the TRV across the CRCB, which is around 5 V (4.6% of V_{dc}). Figure 3.77 shows the line (i_{line}) and dc source (i_s) current



(a) Experimental setup configuration



(b) Implemented CRCB block diagram

Figure 3.74: Experimental setup configuration and implemented CRCB block diagram

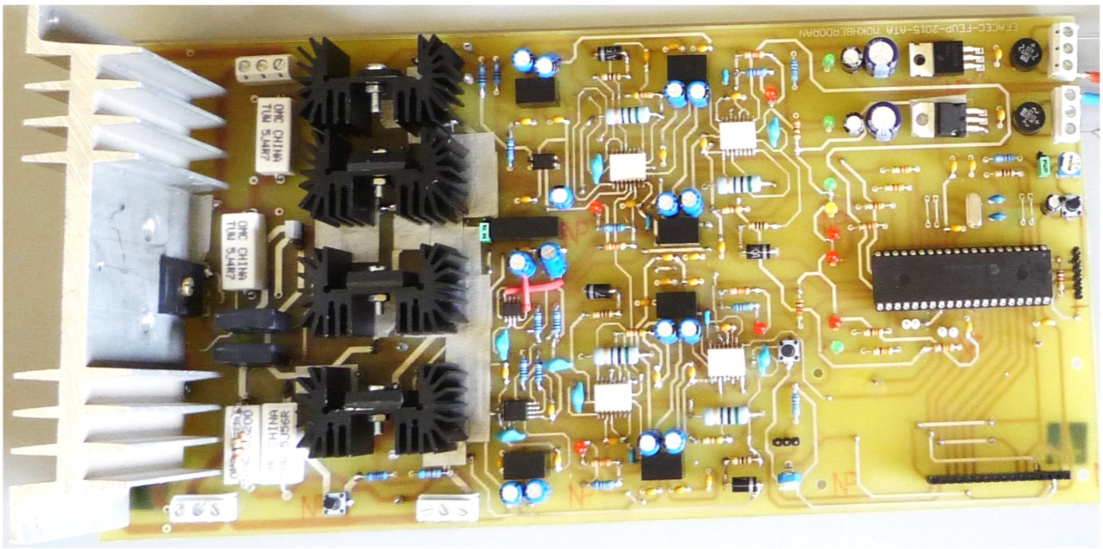


Figure 3.75: The lab-scale prototype.

waveforms in blue and red colors, respectively. As can be seen in the figure, after fault inception the line current rises rapidly and when it reaches 17.5 A, the CRCB trips. The line current is diminished in less than 28 ms. Figure 3.78 shows the capacitor voltage waveform together with the CRCB voltage. As can be seen in the figure, the capacitor voltage before discharging is equal to 98 V and decreases after interruption instance. Figure 3.79 shows the magnified current waveforms. It can be seen in Figure 3.79, the source current reaches zero in less than 10 μs, which can be considered as the interruption time of the implemented CRCB for the aforementioned conditions.

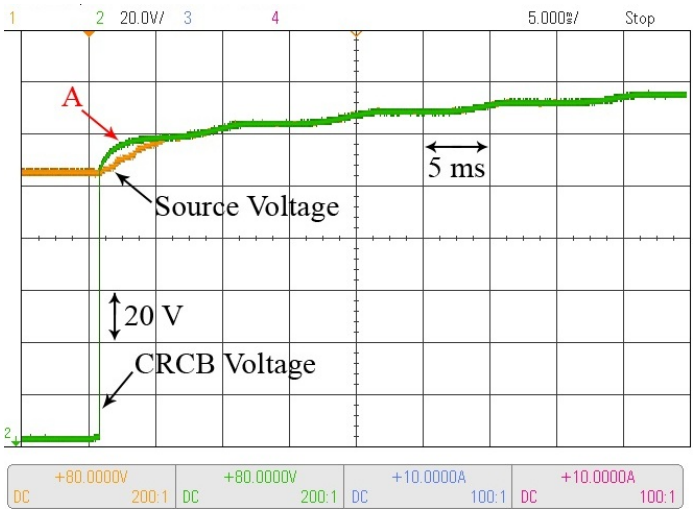


Figure 3.76: CRCB (green) and dc link (orange) voltages

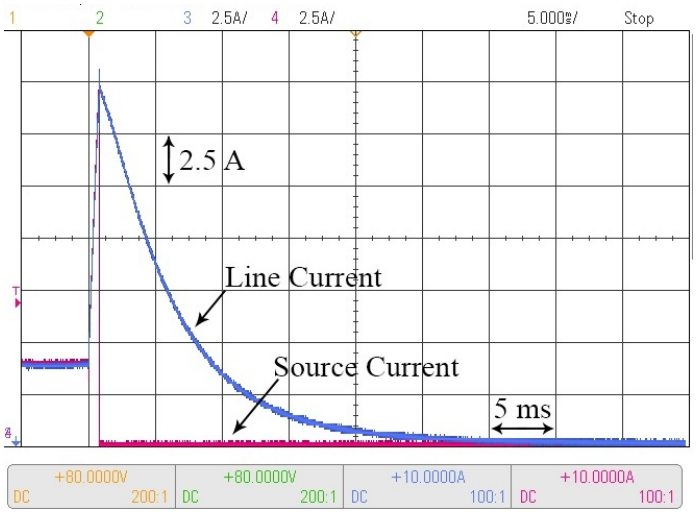


Figure 3.77: Line (blue) and dc source (red) currents

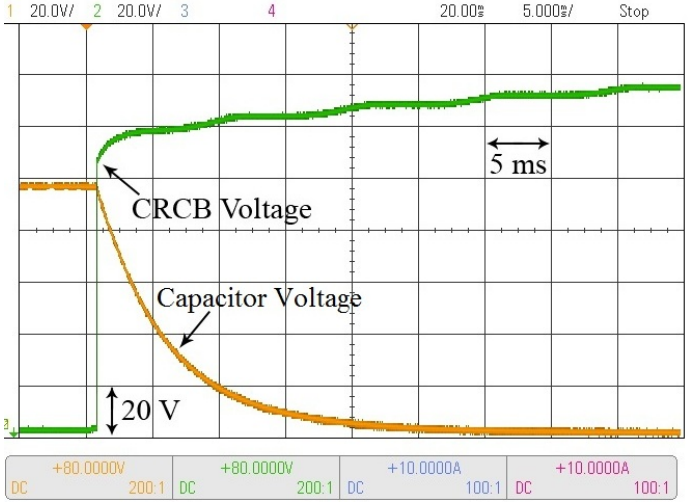


Figure 3.78: CRCB (green) and capacitor voltage (orange) waveforms

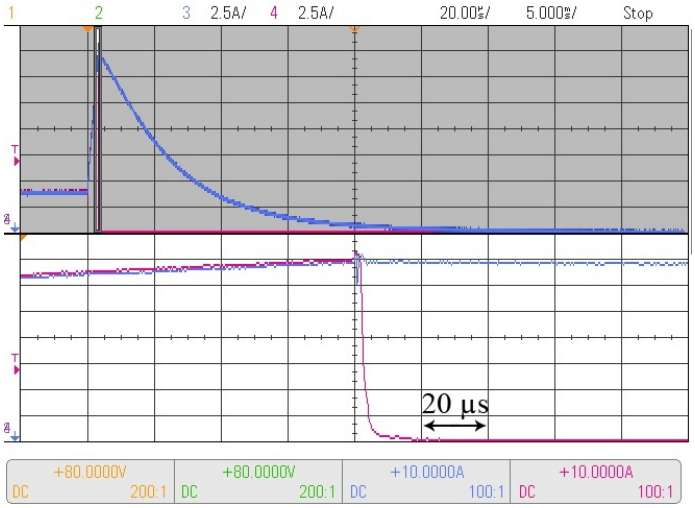


Figure 3.79: Magnified line (blue) and dc source (red) currents

3.7 Conclusion

Interrupting dc current is more challenging as compared to the ac one. In addition to the lack of natural zero crossing in dc current, the high TIV across the dcCB and handling the stored energy in the dc transmission line can be listed as the main issues. The large TIV during the current interruption increases the number of semiconductor switches in series connection. A different approach for dc fault current interruption and saving the power converter from destructive fault currents namely current releasing dc circuit breaker is investigated through the analysis, simulation and experiments in this chapter. The CRCB is a solid-state type dc circuit breaker.

The results from this study show that by selecting suitable values for the internal parameters of CRCB the dc fault currents can be interrupted without generating surge voltage. In addition, by selecting the CRCB capacitor larger than the marginal value and also the CRCB resistor smaller than its marginal value the TIV across the CRCB can be effectively limited.

Sensitivity analysis implies that the interruption of high impedance pole-to-ground or pole-to-pole faults can be done even without excessive voltage. Despite expectation, the largest TIV appears across the CRCB when the fault occurs very close to the dc bus. When the fault occurs at the remote end of the transmission line, the cable resistance increases during the fault interruption process. This mainly due to the high frequency components of the dc fault current which causes skin effect in the cable. The increased resistance of cable reduces the overvoltage across the CRCB when the fault happens in far distance from the CRCB. The CRCB can be integrated into the different HVdc system configurations including the monopole and the bipolar configurations.

In this case study the TIV is limited below 1.15 pu. Comparing with the typical SSCBs, the TIV in CRCB is reduced 35%. The CRCB has at least 60% less power losses as compared to the typical SSCBs due to the less number of semiconductor switches. The functionality of CRCB is examined and validated through implementing a lab-scale prototype. The short circuit test of the prototype confirms the surge-less operation of the CRCB.

Additional circuits with low voltage ratings are included in the CRCB configuration. These circuits guarantee the successful turn-off of the charging and discharging thyristor banks, which is essential in the real applications.

4
Unidirectional Protection of MT-HVdc Grid

Mokhberdoran A., Silva N., Leite H. and Carvalho A., "A directional protection strategy for multi-terminal VSC-HVDC grids," *2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*, Florence, 2016, pp. 1-6.

and

Mokhberdoran, A.; Pirooz Azad, S.; Van Hertem, D.; Silva, N., Carvalho, A., "Unidirectional Protection of HVdc Grids Using Fast dc Circuit Breakers and Local Protection Algorithm," *The 13th IET international conference on AC and dc Power Transmission*, Manchester, UK, February 2017, pp. 1-6.

The job might be difficult, it might require skill, but it's a job. Your art is what you do when no one can tell you exactly how to do it. Your art is the act of taking personal responsibility, challenging the status quo, and changing people. I call the process of doing your art "the work."
The job is not the work.
Seth Godin, 2010, Linchpin: Are You Indispensable?

As was mentioned in chapter 2, the conventional VSCs and the half-bridge MMCs are highly vulnerable against dc side short circuit fault due to the behavior of IGBTs' antiparallel diodes. HVdc circuit breaker as a promising solution may solve the protection problem in the MT-HVdc grid [21,23]. Although HCBs and SSCBs can interrupt the current fast enough, their realization cost for MT-HVdc grid can be notably expensive due to the large number of required semiconductor switches [162].

Some parts of this chapter is also based on the following open access publication:

Mokhberdoran, A.; Silva, ; N. Leite, H.; Carvalho, A., "Unidirectional Protection Strategy for Multi-terminal HVdc Grids," *Transactions on Environment and Electrical Engineering Journal*, Volume 1, Issue 4, November 2016, Pages 58-65, dio: http://dx.doi.org/10.1016/j.epsr.2016.09.008.

SSCBs and HCBs are typically considered to be bidirectional and hence interrupt the current in their forward and backward directions [23]. Unidirectional HVdc circuit breakers (UCBs) conduct the current in their forward and backward directions whereas interrupts the current only in one direction. The main concern regarding the application of UCB in the MT-HVdc grid is its inability in interrupting the fault current flowing in its backward direction as it may occur in a dc bus short circuit fault scenario.

Unidirectional hybrid and solid-state circuit breakers require half the number of required semiconductor switches in the main breaker unit of the typical bidirectional hybrid and solid-state circuit breakers. Therefore, their application in protection of the future MT-HVdc grid would be technically and economically attractive.

This chapter focuses on the protection of MT-HVdc grid based on the UCBs. Firstly, a typical protection strategy of MT-HVdc grid based on bidirectional HVdc circuit breakers (BCBs) is explored in section 4.1 and thereafter a unidirectional protection strategy based on UCBs is suggested for MT-HVdc grid in section 4.2. The suggested strategy attempts to overcome the main drawback of UCB application in MT-HVdc grid. Protection logics for dc bus and transmission line faults are investigated.

In order to study the performance of suggested strategy, two different types of UCBs including unidirectional hybrid HVdc circuit breaker (UHCB) and the proposed current releasing HVdc circuit breaker (CRCB) are considered. The application of UHCB in protection of the four-terminal HVdc grid model is investigated in section 4.3. Furthermore, the application of the proposed CRCB in protection of MT-HVdc grid has been studied through different fault scenarios in the four-terminal HVdc grid model in section 4.4. Moreover, the superiorities and limitations of unidirectional protection of the MT-HVdc grid are assessed and the impacts of suggested strategy on the MT-HVdc grid elements are also studied. Finally, this chapter is concluded in section 4.5.

4.1 Typical Protection Strategy

Three different protection strategies for the MT-HVdc grids are identified [21]:

- Handshaking approach with ac breakers
- Fault-tolerant converters with disconnector switches
- Fast fault identification relays with fast dcCBs

In this chapter, the third protection strategy together with the fast dcCBs are considered. The dcCBs can be placed at ends of each transmission line and also at the dc side of converters. Figure 4.1 shows the typical BCBs arrangement and the protection zones in a three-terminal HVdc grid. CB_{xy} represents the dcCB attached to line L_{xy} close to bus B_x. Also, CB_{xx} represents the dcCB attached to VSC_x at bus B_x.

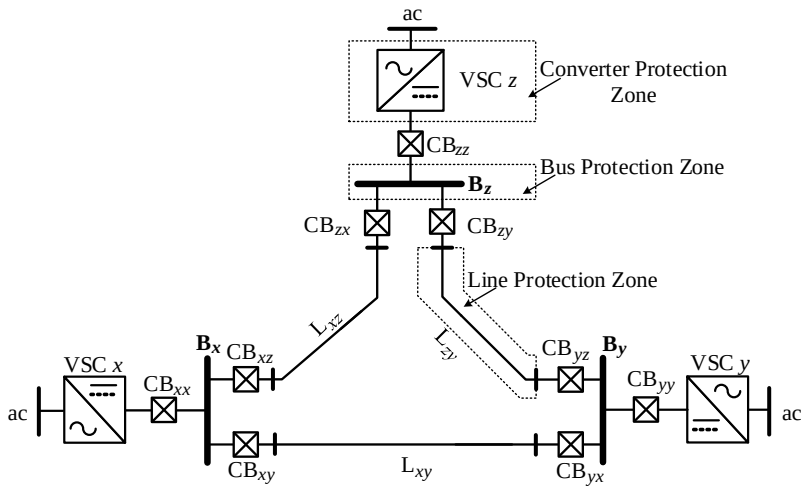


Figure 4.1: BCBs arrangement in a multi-terminal HVdc grid.

4.1.1 dc Bus Fault

Typically, a dc bus[1] is protected by bus differential protection scheme. In a dc bus, sum of all incoming and outgoing currents must be zero. If a short circuit fault occurs at the dc bus, the sum of incoming and outgoing currents becomes non-zero. Therefore, dc bus trip signal can be generated if the sum of currents exceeds a near zero value. The differential protection scheme is quite fast and selective due to its low computing burden. The fault clearance in the dc bus zone can be done by opening all adjacent dcCBs. If the dc bus is connected to a converter, the converter dcCB should also be opened. Assume n transmission lines are connected to bus B_x. The protection logic can be given as (4.1).

$$Fault\ at\ B_x \Rightarrow Trip(CB_{x1}, ..., CB_{xx}, ..., CB_{xn}) \tag{4.1}$$

[1] Occurrence of a dc bus short circuit fault is not common even in ac power system. Similar to the other published works so far, in this work also a simple busbar configuration is considered. However, more complex busbar configurations can improve the dc bus reliability and reduce the risk of dc bus outage and power discontinuity during a short circuit fault. Note that complex busbars may require more dcCBs or disconnectors.

4.1.2 *Transmission Line Fault*

A transmission line can be protected by either non-unit communication-less or communication-based[2] protection schemes. Moreover, combination of both methods can also be considered in protection of a transmission line against short circuit faults. Communication-based protection schemes process the data from local and remote relays to detect a fault and to confirm the trip command. On the other hand, fast non-unit protection schemes rely on local measurement of current, voltage, current derivative, voltage derivative or their combination [21]. In any transmission line protection method, if a fault is detected on the line, both dcCBs (local and remote dcCBs) of faulty line should trip. The typical protection logic can be given as follows:

$$Fault\ on\ \mathrm{L}_{xy} \Rightarrow Trip(\mathrm{CB}_{xy}, \mathrm{CB}_{yx}) \tag{4.2}$$

[2] One of the concerns regarding the application of communication-based protection schemes for the MT-HVdc grid is low communication speed. Note that the communication can be done through fiber-optic cables with an acceptable speed. However, there might be additional delays related with the signal conditioning and computing circuitries. In contrary with HVac cables, the submarine HVdc cables are not typically equipped with the embedded fiber-optic cable. Hence, extra deep-sea fiber-optic cables might be required for communication purposes. Anyway, both embedded and external fiber optic cables may suffer from reliability issues as during a physical fault occurrence, they also might be damaged. Nevertheless, the reliability can be improved by employing different alternative communication methods together.

4.2 *Unidirectional Protection Strategy*

Figure 4.2 depicts the arrangement of UCBs in a three-terminal HVdc grid. The arrow in the UCB symbol shows its current interruption direction. A protection strategy covering the dc bus and the transmission line zones based on the UCBs is suggested for the MT-HVdc grids in this section.

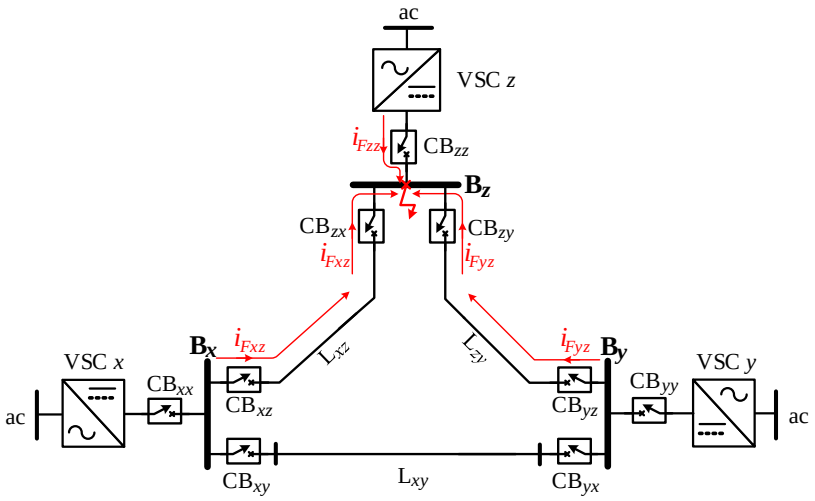


Figure 4.2: UCBs arrangement and directions and fault current directions during dc bus fault.

4.2.1 *dc Bus Fault*

Figure 4.2 shows the fault currents during a short circuit fault at dc bus B_z. Three fault currents flow though three adjacent UCBs. Since the fault current i_{Fzz} flows in the forward direction of CB_{zz}, it can be interrupted by CB_{zz}. Fault currents i_{Fxz} and i_{Fyz} flow through the adjacent lines to the fault location and are in the backward directions of CB_{zx} and CB_{zy} and cannot be interrupted by them.

As shown in Figure 4.2, i_{Fxz} flows in the forward direction of CB_{xz} and can be interrupted by this UCB, which is placed at the remote

end of line. Any other fault current flowing from the adjacent lines can be interrupted by the remote UCB. The protection logic for the dc bus fault can be given by:

$$Fault\ at\ \mathrm{B}_x \Rightarrow Trip(\mathrm{CB}_{1x}, ..., \mathrm{CB}_{xx}, ..., \mathrm{CB}_{nx}) \tag{4.3}$$

The trip command for remote dcCB can be generated locally or communicated between two buses. In the communication-based method, fault detection is done locally in the faulted bus and the trip command is communicated to the remote dcCBs. On the other hand, the communication-less method relies on the fault detection at the remote buses. In communication-less method, a fault at B_x can be detected by the remote dcCBs at the other buses of system either based on the non-unit protection or overcurrent protection schemes.

4.2.2 *Transmission Line Fault*

Figure 4.3 shows a short circuit fault in line L_{xy}. Two fault currents flow from both ends of the transmission line into the fault location. In any line fault condition, the fault currents flow in the forward directions of corresponding UCBs. Therefore, the fault can be cleared by opening the corresponding UCBs. Unidirectional protection logic for transmission line fault is similar to (4.2).

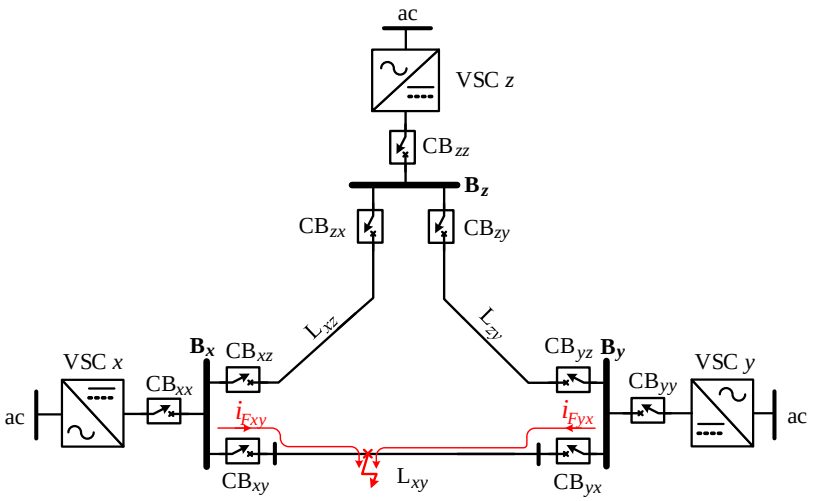


Figure 4.3: UCBs arrangement and directions and fault current directions during dc transmission line fault.

4.3 Application of Unidirectional Hybrid dc Circuit Breakers in Protection of MT-HVdc Grid

4.3.1 Typical and Unidirectional Hybrid dc Circuit Breaker

The configuration of a proactive HCB is depicted in Figure 2.50 in chapter 2 [134,138]. The operation principles and different units of the proactive HCB is explained in chapter 2. The mentioned HCB will be referred as typical HCB in this thesis. In order to allow bidirectional current flow and also bidirectional fault current interruption the semiconductor switches should be connected in anti-series. The number of semiconductor switches in series connection in the MB unit can be obtained as follows:

$$N_{s,HCB} = 2\left\lceil \frac{OVP_{SA}}{V_{CE,dc}} \right\rceil \tag{4.4}$$

where, $V_{CE,dc}$ represents the collector-emitter dc stability voltage in case of IGBTs.

The topology of a unidirectional hybrid dc circuit breaker for the positive pole of an HVdc system is depicted in Figure 4.4.

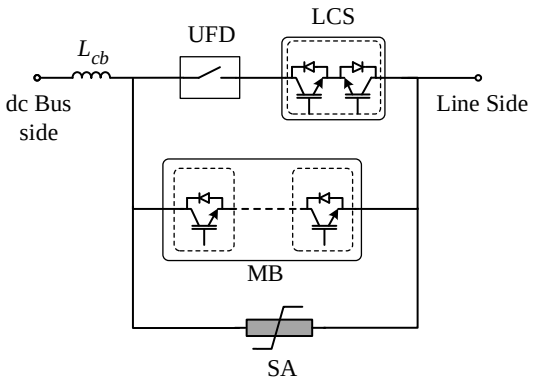


Figure 4.4: Unidirectional hybrid dc circuit breaker schematic.

In the UHCB topology, two anti-series semiconductor switches are replaced by one switch. Therefore, the UHCB is only able to interrupt the fault current in the transmission line side. The normal power flow can be maintained in both forward and backward directions due to the presence of antiparallel diodes. The UHCB requires half the number of semiconductor switches in its MB unit as compared to the typical HCB. The number of semiconductor switches in series connection in the MB unit of UHCB can be given as follows:

$$N_{s,UHCB} = \left\lceil \frac{OVP_{SA}}{V_{CE,dc}} \right\rceil \tag{4.5}$$

The operation principles of UHCB for the transmission line fault are similar to the typical HCB. Note that during a dc bus fault the current flowing through the LCS unit can be commutated into the MB unit by opening the LCS unit. After current commutation is done the UFD can also be opened. In this case the current in the MB unit cannot be interrupted by due to the conduction of antiparallel diodes. However, the MB unit can tolerate high fault current, since it is rated

for it. The UHCB attached to the faulty dc bus conducts the fault current in its backward direction until the fault current is interrupted by the remote UHCB.

4.3.2 Models

Test System

The four-terminal meshed HVdc grid model, which is explained in appendix A is employed in this chapter [213]. The system configuration is shown in Figure 4.5. HVdc transmission lines are modeled based on the XLPE insulated cable using frequency dependent modeling approach. The cable cross-sections and properties of material are illustrated in Figure A.2 and Table A.2, respectively [212].

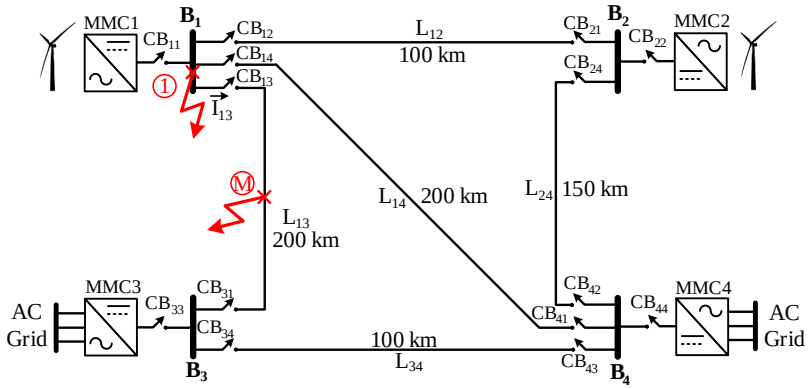


Figure 4.5: Test multi-terminal HVdc grid.

Circuit Breaker Model

The aggregated models of HCB and UHCB are employed in this chapter. Figure 4.6(a) and (b) depict the aggregated models of HCB and UHCB, respectively. As shown in Figure 4.6(b) the UHCB model is derived from HCB model by adding one parallel diode (D). The L_{cb}, R_v and T_{cb} represent the limiting inductor, surge arrester and the circuit breaker operation time delay, respectively. The value of limiting inductor (L_{cb}) of the line dcCBs is set to 100 mH. The L_{cb} for the converter station dcCBs is set to 10 mH. The OVP of surge arresters is set to 480 kV. The HCB operation delay (T_{cb}) is set to 2.5 ms, which includes time delays in the LCS, UFD and MB unit operations [134]. The trip command is received by the dcCB and breaker component interrupts the current independent of its magnitude after a time delay equal to T_{cb}.

Protection System

The system performance is studied based on the typical and the suggested unidirectional protection strategies. A state of the art non-unit scheme, which has recently been proposed in [214] is employed for transmission line protection. The utilized method uses the local

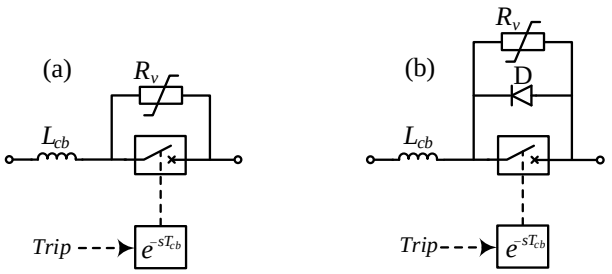


Figure 4.6: Aggregated models (a) typical HCB, (b) UHCB.

current measurements for line fault detection. More details regarding this protection scheme can be found in appendix B. The mentioned non-unit scheme is also used in the unidirectional protection strategy. Two different schemes for the dc bus fault detection are considered in the unidirectional protection strategy including:

- Local fault detection (communication-based)
- Remote overcurrent fault detection (communication-less)

In the first method a bus fault is detected by the bus differential relay and the trip command is communicated to the remote UHCBs. Communication time is modeled by a time delay block. In the second method a communication-less system is considered. The bus fault is detected at the remote healthy buses when the line current exceeds specific threshold.

4.3.3 Simulation Results

The results from study of four fault scenarios are presented and compared in this subsection.

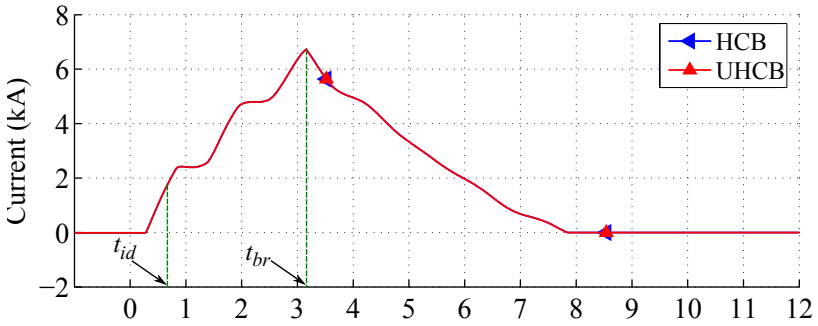
Transmission Line Fault

Transmission line fault is studied through three independent permanent pole-to-pole low impedance ($R_{fault} = 100$ mΩ) short circuit faults at the middle of lines L_{12}, L_{13}, L_{14}. The line fault incepts at time 0 s. As discussed in section 4.2, the line fault clearing process for UHCBs and HCBs are the same. Therefore, to clear the line fault from the system dcCBs at both ends of the faulty line should trip. The numerical values of fault identification time are illustrated in Table 4.1. Due to the longer length of L_{13} and L_{14}, the midpoint fault is detected later than the similar fault in L_{12}. Since the fault is placed on the midpoint of the transmission lines, it is detected in almost similar time ranges from both ends of the transmission line.

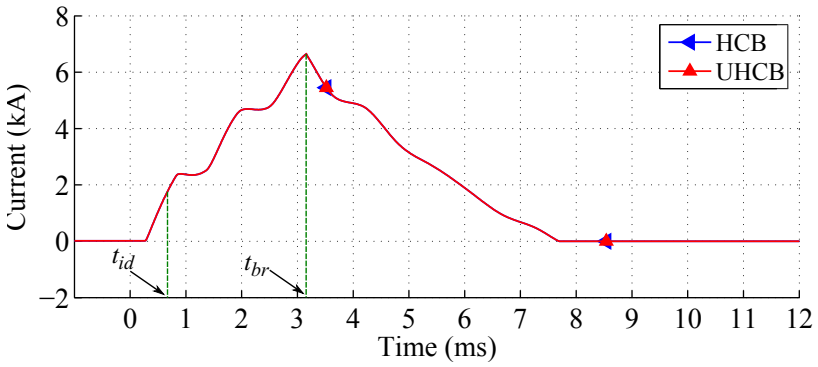
Figures 4.7, 4.8 and 4.9 show the current in corresponding dcCBs for the short circuit fault in different transmission lines. t_{id} and t_{br} represent the fault identification time and the dcCB current interruption time instance for related dcCB, respectively. Note that the fault identification and the trip command generation are assumed to be simultaneous.

dcCB	Trip time (t_{id}) [ms]							
	Fault at B_1		Fault on L_{12}		Fault on L_{13}		Fault on L_{14}	
	BCB	**UCB**	**BCB**	**UCB**	**BCB**	**UCB**	**BCB**	**UCB**
CB_{11}	0.1	0.1	-	-	-	-	-	-
CB_{12}	0.1	0.1	0.79	0.79	-	-	-	-
CB_{21}	5	1.5	0.66	0.66	-	-	-	-
CB_{13}	0.1	0.1	-	-	1.05	1.05	-	-
CB_{31}	10	2	-	-	0.95	0.95	-	-
CB_{14}	0.1	0.1	-	-	-		1.05	1.05
CB_{41}	10	2	-	-	-	-	0.95	0.95

Table 4.1: Trip times for different Types of dc circuit breakers for dc bus and transmission line faults.



(a) Current in CB_{12}



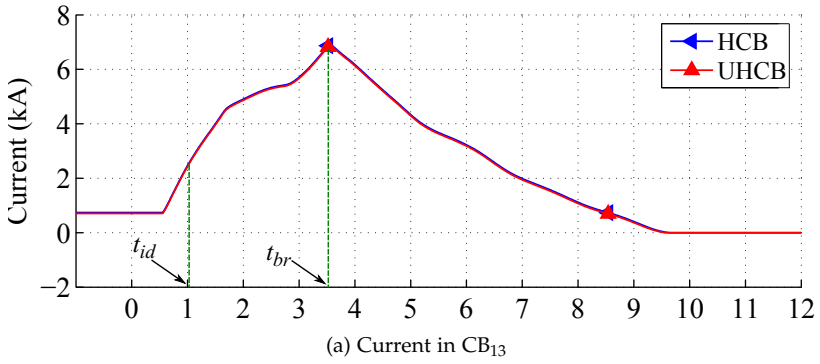
(b) Current in CB_{21}

Figure 4.7: Current in CB_{21} and CB_{12} during fault on transmission line L_{12} for HCB based and UHCB based protection schemes.

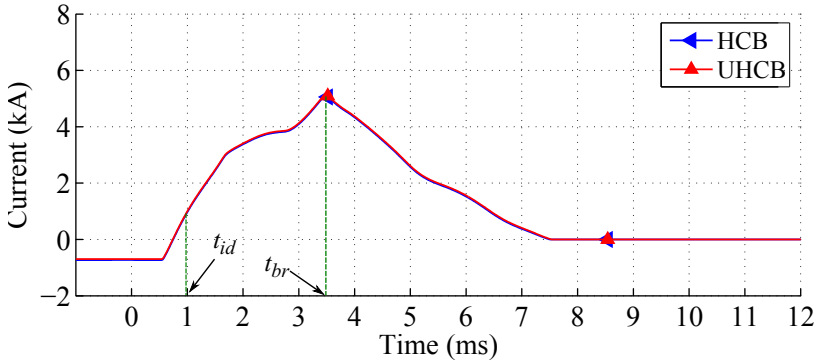
The currents in CB_{12} and CB_{21} when a fault occurs on transmission line L_{12} are depicted in Figures 4.7(a) and (b), respectively. As can be seen in the figures the current in both types of dcCBs are equal. Due to near zero pre-fault current of transmission line L_{12}, the currents in CB_{12} and CB_{21} are almost equal. Figures 4.8(a) and (b) show the currents in CB_{13} and CB_{31} during a short circuit fault on transmission line L_{14}, respectively. Similar to the previous case, the currents in both types of dcCBs are equal. Due to the positive pre-fault current in CB_{13}, its current reaches larger magnitude as compared to CB_{31}. However, the identification time does not depend on the direction of current in the dcCB.

Figures 4.9(a) and (b) depict the currents in CB_{14} and CB_{41} during a short circuit fault on transmission line L_{14}, respectively. As expected, the currents in both types of dcCBs are identical. The fault current in CB_{14} reaches larger value as compared to CB_{41} due to the same directions of pre-fault and fault currents in CB_{14}. The fault identification times for both ends of the transmission line are almost equal.

Figure 4.8: Current in CB_{31} and CB_{13} during fault on transmission line L_{13} for HCB based and UHCB based protection schemes.

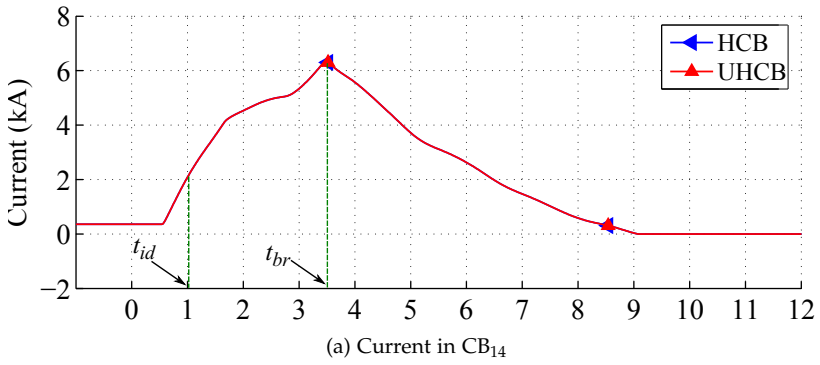


(a) Current in CB_{13}

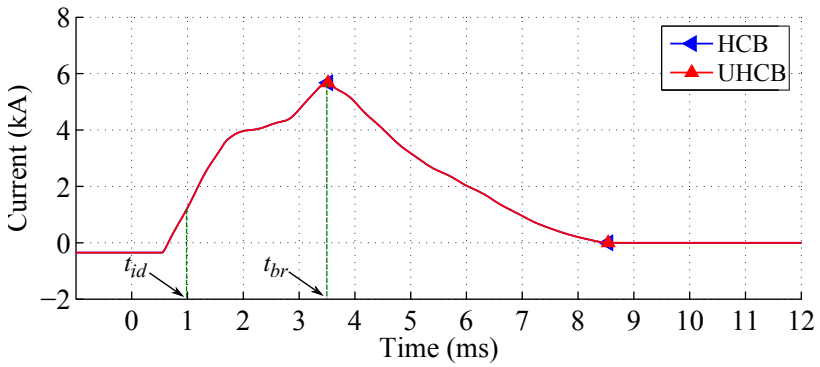


(b) Current in CB_{31}

Figure 4.9: Current in CB_{41} and CB_{14} during fault on transmission line L_{14} for HCB based and UHCB based protection schemes.

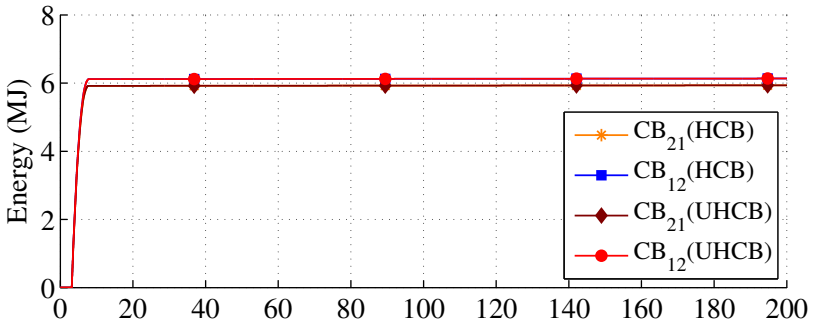


(a) Current in CB_{14}

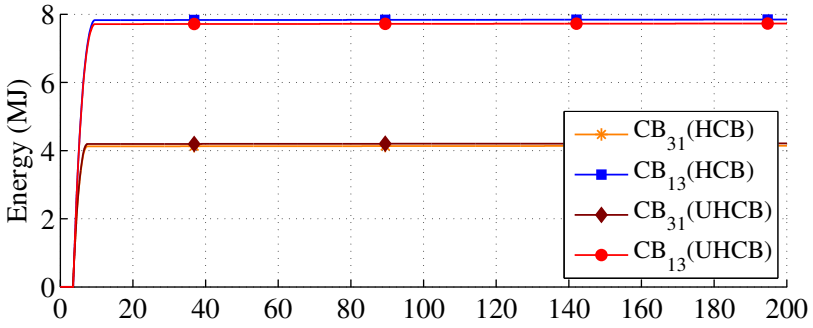


(b) Current in CB_{41}

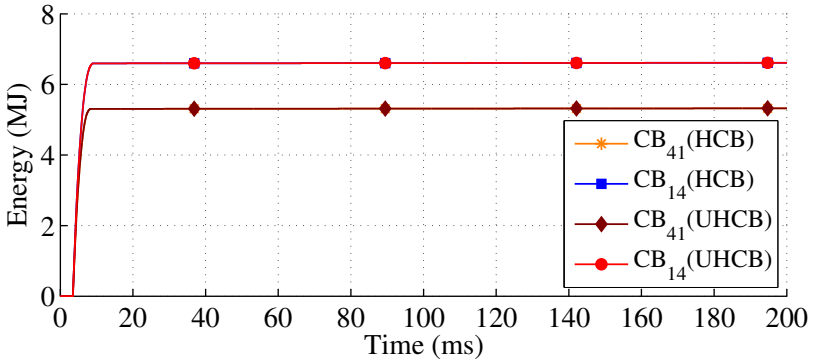
Absorbed energy by the surge arrester of each dcCB is depicted in Figure 4.10. The difference in dissipated energy in the surge arresters is due to unequal interrupted fault currents in corresponding dcCBs and also different fault distances from dcCB. The dcCBs with positive



(a) Absorbed energy in the surge arrester of CB_{12} and CB_{21}



(b) Absorbed energy in the surge arrester of CB_{13} and CB_{31}



(c) Absorbed energy in the surge arrester of CB_{14} and CB_{41}

Figure 4.10: Absorbed energy in the surge arresters of corresponding dcCBs for HCB based and UHCB based systems.

pre-fault current (pre-fault and fault currents are in the same direction) reach higher current than the dcCB with negative pre-fault current and therefore, larger amount of energy is dissipated in their surge arresters.

dc Bus Fault

During a bus fault in the MT-HVdc grid, due to the low inductance between the converter and fault location, high fault current flows in the dc side of the converter. The fault current may exceed the self-protection threshold of the MMC and cause the MMC blocking if it is not detected timely. Protection of converter against dc bus faults can rely on either ac side circuit breaker or the converter station dcCB. In this study, the MMC is protected by a dcCB at its dc side. A permanent pole-to-pole low impedance ($R_{fault} = 100$ mΩ) short circuit fault incepts at bus B_1 at $t = 0$ s. In the typical protection

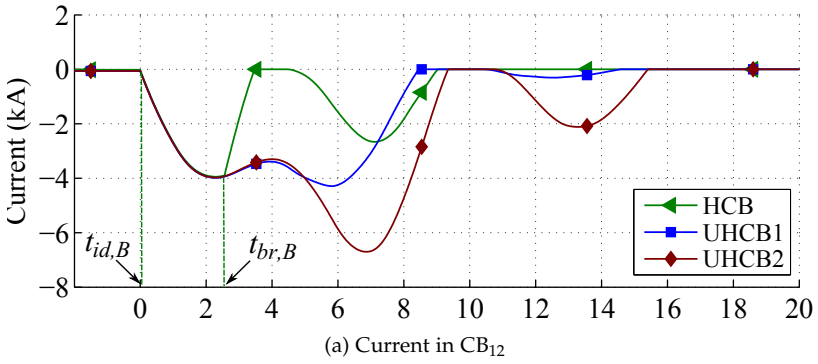
strategy upon fault detection by the dc bus protection scheme, CB_{11}, CB_{12}, CB_{13}, CB_{14} should trip and disconnect the adjacent lines from B_1. Therefore, terminal 1 of the MT-HVdc grid will be disconnected from rest of the system and consequently, the amount of harvested energy from generation nodes of system will be reduced. Hence, MMC 3 and 4 will absorb less power as compared to pre-fault conditions. The remote dcCBs of the adjacent lines trip after a longer time delay to disconnect the cables from healthy dc buses.

In the unidirectional protection strategy, upon fault detection at bus B_1 all adjacent UHCBs including CB_{11}, CB_{12}, CB_{13}, CB_{14} are opened. The fault currents flow in the backward directions of CB_{12}, CB_{13}, CB_{14} and these UHCBs are unable to interrupt the fault current. Therefore, based on 4.3, CB_{21}, CB_{31} and CB_{41} should trip. The dc bus fault clearing is studied through two protection schemes as explained in section 4.2. In the communication-based method, communication delay is modeled by a time delay block. The time delay block represents sum of propagation and transmitter/receiver delays. The propagation delay is set to 5 μs/km and the transmitter/receiver delay is set to 1 ms [215]. The trip times of remote dcCBs are illustrated in Table 4.1. The second method is an overcurrent protection scheme. The overcurrent thresholds are set to 3 kA for all lines.

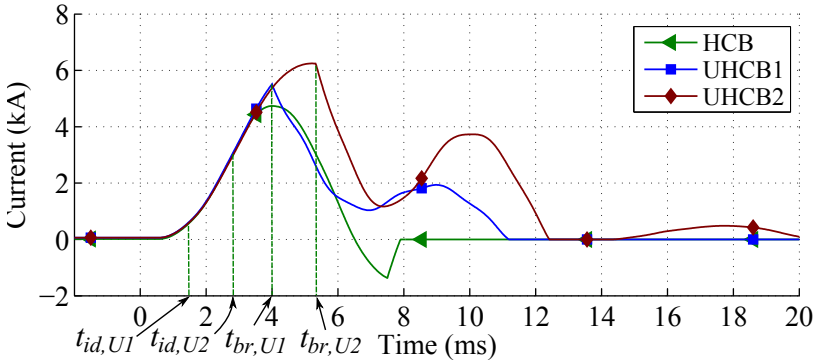
Figures 4.11, 4.12 and 4.13 show the currents in all dcCBs attached to the adjacent lines for three discussed protective schemes. In Figures 4.11, 4.12 and 4.13 HCB, UHCB1 and UHCB2 represent the bidirectional, communication-based and overcurrent-based unidirectional protective schemes, respectively. In addition, t_{id} and t_{br} represent fault identification and current interruption times for each protective scheme. Absorbed energy in the surge arrester of each dcCB is depicted in Figure 4.14(a)-(c).

As can been in Figures 4.11, 4.12 and 4.13, the current in CB_{21}, CB_{31} and CB_{41} reach higher values in overcurrent-based scheme as compared to the communication-based scheme. It can be seen in Figures 4.11(a), 4.12(a) and 4.13(a), the HCBs interrupt the bus fault current before reaching higher values. On the other hand, the remote UHCBs in the communication-based unidirectional protective scheme (UHCB1) also interrupt the bus fault current before reaching higher values. Due to the higher interrupted current and larger cable inductance in unidirectional protection strategy, UHCBs' surge arresters absorb more energy than the HCBs.

Figures 4.15(a), 4.16(a) and 4.17(a) show the MMC arm currents for healthy buses (MMC 2, 3 and 4) in presence of HCBs. In addition, the arm currents of MMC 2, 3 and 4 in presence of UHCBs for overcurrent-based scheme are depicted in Figures 4.15(b), 4.16(b) and 4.17(b). Also, the arm currents of mentioned MMCs in presence of UHCBs for communication-based scheme are illustrated in Figures 4.15(c), 4.16(c) and 4.17(c). The arm currents of MMC 1 are not included since this converter is isolated from the MT-HVdc grid due to converter station dcCB (CB_{11}) action during the dc bus fault.

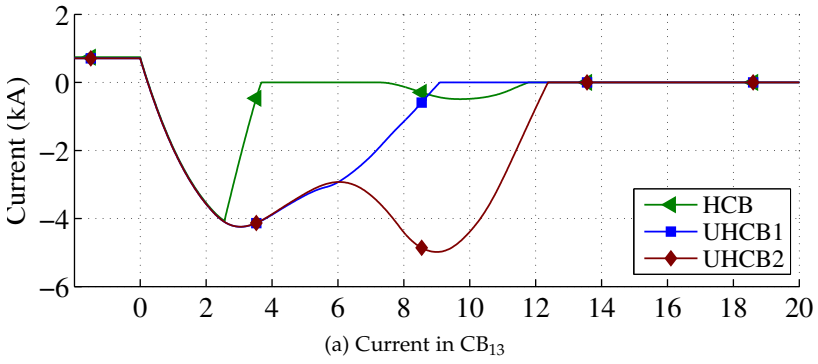


(a) Current in CB_{12}

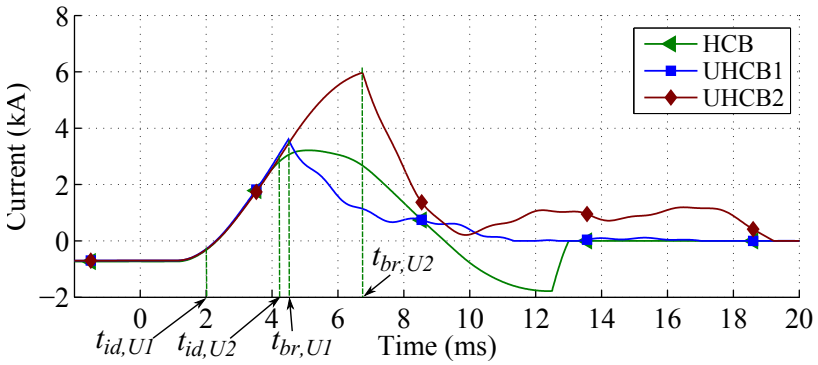


(b) Current in CB_{21}

Figure 4.11: Current in CB_{21} and CB_{12} during fault at dc bus B_1 for HCB based and two UHCB based protection schemes.



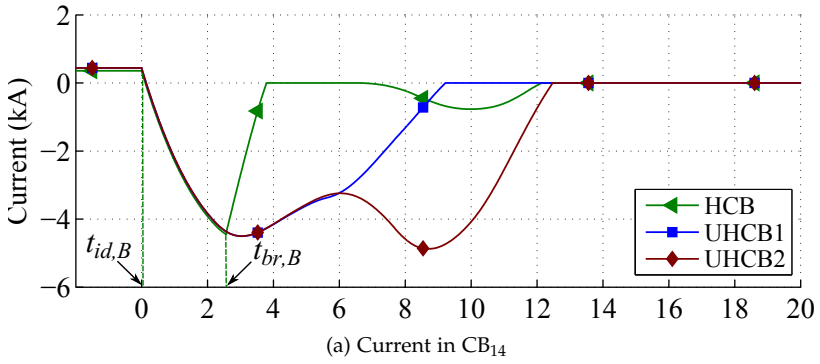
(a) Current in CB_{13}



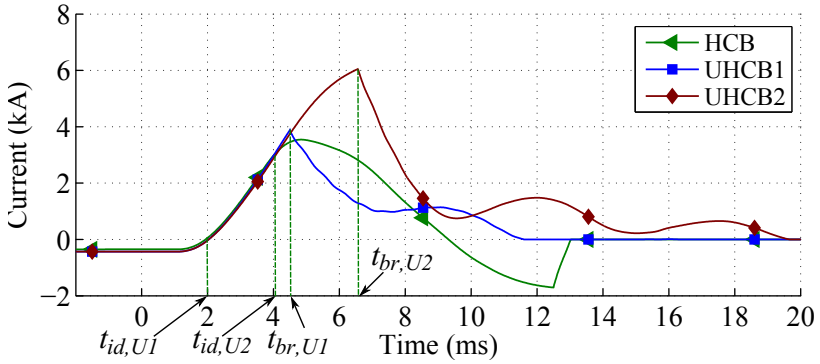
(b) Current in CB_{31}

Figure 4.12: Current in CB_{31} and CB_{13} during fault at dc bus B_1 for HCB based and two UHCB based protection schemes.

The self-blocking feature of the MMCs is de-activated in this study. As it is expected the arm currents in all the MMCs reach higher values in overcurrent based protection scheme. The arm currents in MMC 2 and 3 do not exceed 2.5 kA in communication-based and in presence



(a) Current in CB_{14}



(b) Current in CB_{41}

Figure 4.13: Current in CB_{31} and CB_{13} during fault at dc bus B_1 for HCB based and two UHCB based protection schemes.

of HCBs, which can be acceptable for setting the blocking threshold of the MMCs.

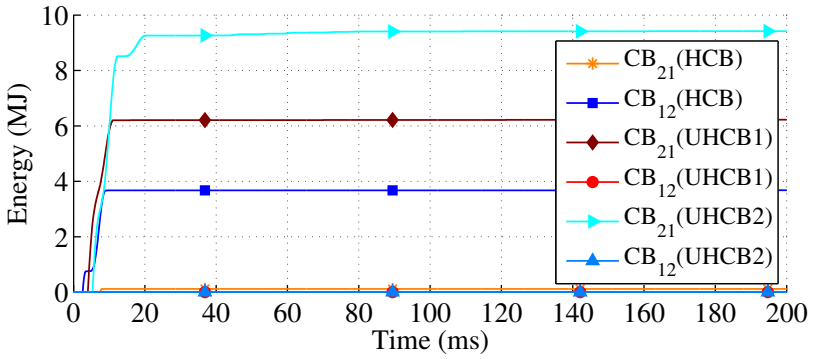
4.3.4 *Impact on the HCB Current Interruption Capability*

The maximum current in possible fault scenarios sets the requirements for dcCB current interruption rating.

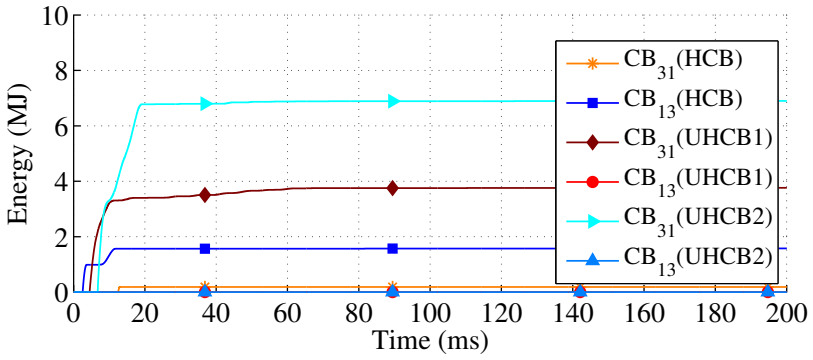
Communication-based Method

Due to the lower inductance of short transmission lines, rate of rise of fault current in short lines is higher as compared to the long lines. Hence, the remote dcCBs in short lines might be required to interrupt higher current as compared to long lines. For instance, as can be seen in Figure 4.11(b), the current in CB_{21} reaches almost 5.6 kA with unidirectional strategy while it does not exceed 3.9 kA in CB_{12} in the bidirectional strategy (see Figure 4.11(a)). Note that the length of line L_{12} is 100 km. On the other hand, for line L_{13} (200 km), the current in CB_{31} reaches almost 3.8 kA with unidirectional strategy and it reaches almost 4 kA in CB_{13} in the bidirectional strategy (see Figure 4.12(a) and (b)). The bus fault is cleared in longer time in communication-based unidirectional strategy as compared to the bidirectional strategy.

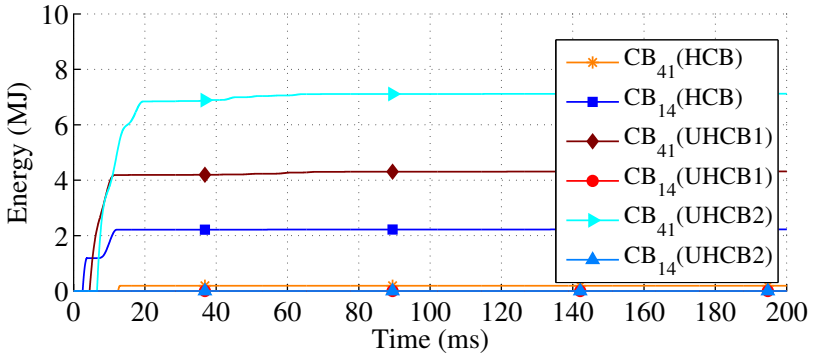
Figure 4.18(a) provides a comparison between the maximum interrupted current of different dcCBs during the dc bus and corresponding transmission line faults. As shown in the figure, the dcCBs are required to interrupt higher fault current during the line



(a) Absorbed energy in the surge arrester of CB_{12} and CB_{21}



(b) Absorbed energy in the surge arrester of CB_{13} and CB_{31}



(c) Absorbed energy in the surge arrester of CB_{14} and CB_{41}

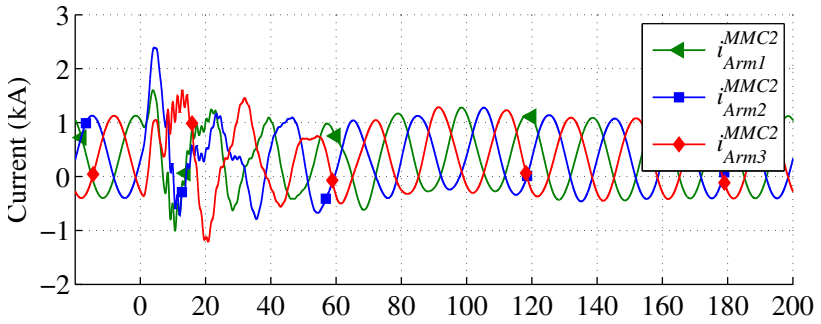
Figure 4.14: Absorbed energy in the surge arresters of corresponding dcCBs for a short circuit fault at dc bus 1 for HCB based and two UHCB based systems.

fault as compared to the dc bus fault in communication-based unidirectional protection strategy. Results of this study imply that the communication-based unidirectional scheme does not necessarily require dcCBs with higher current rating. Despite longer fault detection and trip times in the communication-based unidirectional scheme, the cable inductance and the dcCB current limiting inductor limit the rate of rise of fault current in the remote dcCB.

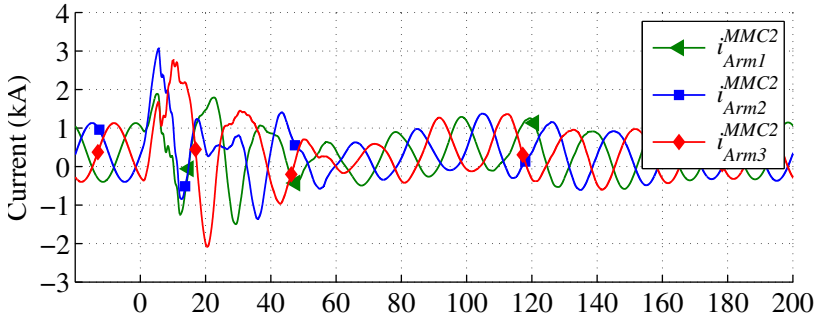
Overcurrent-based Method

As can be seen in Figures 4.11, 4.12 and 4.13, the current in CB_{21}, CB_{31} and CB_{41} reach higher value in overcurrent-based unidirectional scheme as compared to the current in CB_{12}, CB_{13} and CB_{14} in the bidirectional and the communication-based unidirectional schemes. The overcurrent protection threshold may be set to lower values in

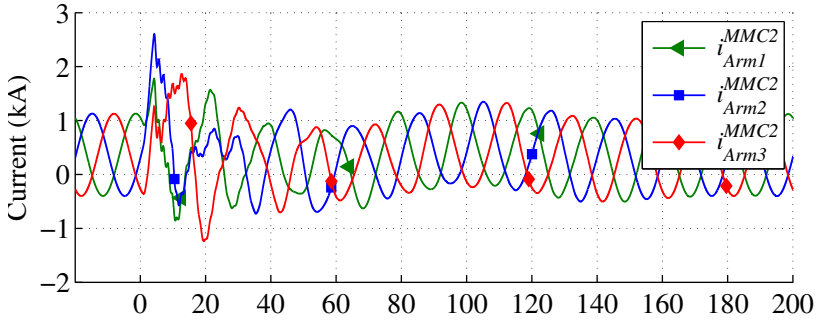
Figure 4.15: Arm currents of MMC 2 for three studied protection schemes.



(a) Arm currents of MMC 2 for typical protection scheme based on HCB



(b) Arm currents of MMC 2 for overcurrent based unidirectional protection scheme based on UHCB



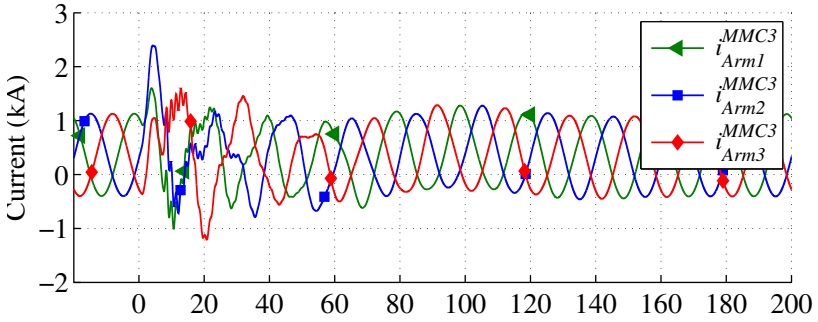
(c) Arm currents of MMC 2 for communication-based unidirectional protection scheme based on UHCB

order to shorten the fault identification time if it is coordinated with the non-unit protection scheme. As shown in Figure 4.18(a), the maximum interrupted current in CB_{31} and CB_{41} is slightly higher for the dc bus fault with overcurrent-based method as compared to the maximum interrupted current for corresponding transmission line faults. Hence, the UHCBs might be required to interrupt higher current as compared to the HCBs depending on the overcurrent protection parameters.

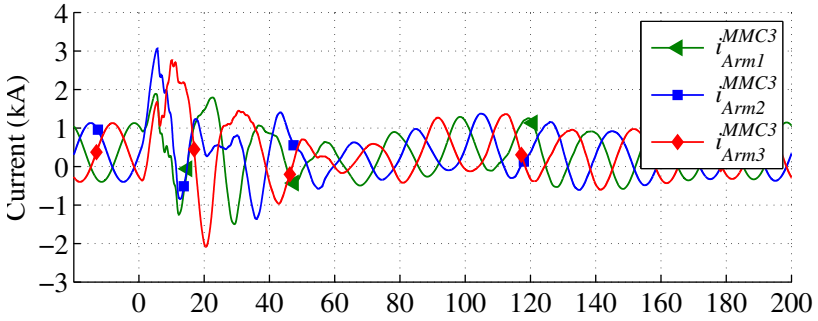
4.3.5 *Impact on the Surge Arrester Energy Rating*

Communication-based Method

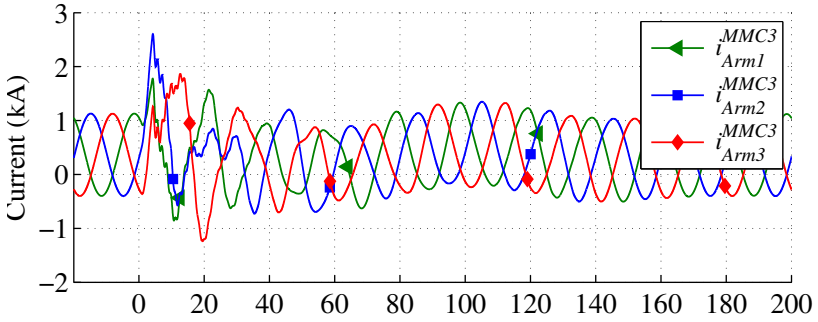
The amount of absorbed energy in the surge arrester of dcCB depends on the interrupted current value and the fault location distance from the dcCB. The magnitude of interrupted current has higher impact



(a) Arm currents of MMC 3 for typical protection scheme based on HCB



(b) Arm currents of MMC 3 for overcurrent based unidirectional protection scheme based on UHCB



(c) Arm currents of MMC 3 for communication-based unidirectional protection scheme based on UHCB

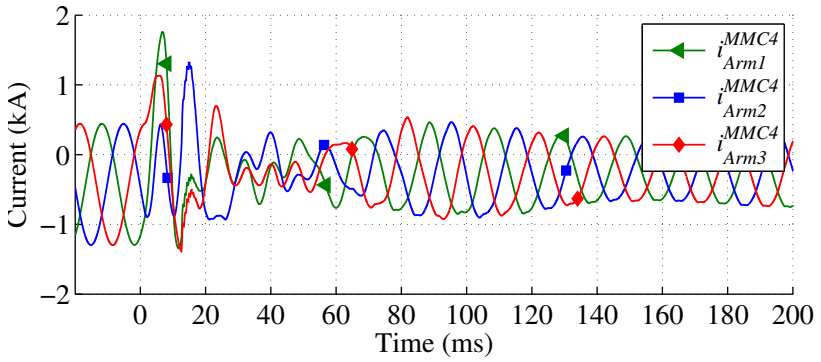
Figure 4.16: Arm currents of MMC 3 for three studied protection schemes.

on the amount of absorbed energy. The absorbed energy in surge arresters of dcCBs during the transmission line and the dc bus faults are compared in Figure 4.18(b). As can be seen, the surge arresters of UHCBs dissipate lower amount of energy during dc bus fault in communication-based unidirectional method as compared to corresponding transmission line fault. Note that the amount of absorbed energy in CB_{21} during bus fault is almost equal to the absorbed energy in CB_{12} during the line fault. These results imply that the energy rating of surge arresters for UHCBs with communication-based unidirectional strategy is not necessarily different than their energy rating for HCBs with the bidirectional strategy.

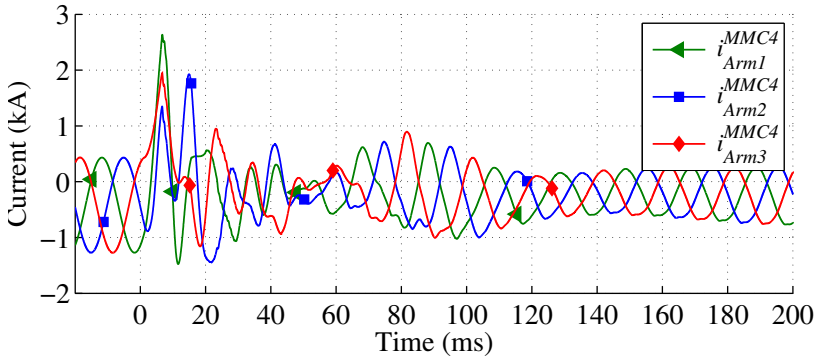
Overcurrent-based Method

Due to the higher fault current during the dc bus fault in overcurrent-based method, the surge arresters dissipate higher amount of energy

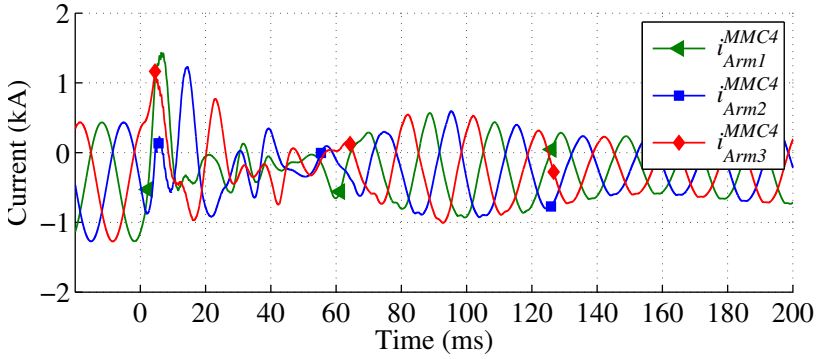
Figure 4.17: Arm currents of MMC 4 for three studied protection schemes.



(a) Arm currents of MMC 4 for typical protection scheme based on HCB



(b) Arm currents of MMC 4 for overcurrent based unidirectional protection scheme based on UHCB

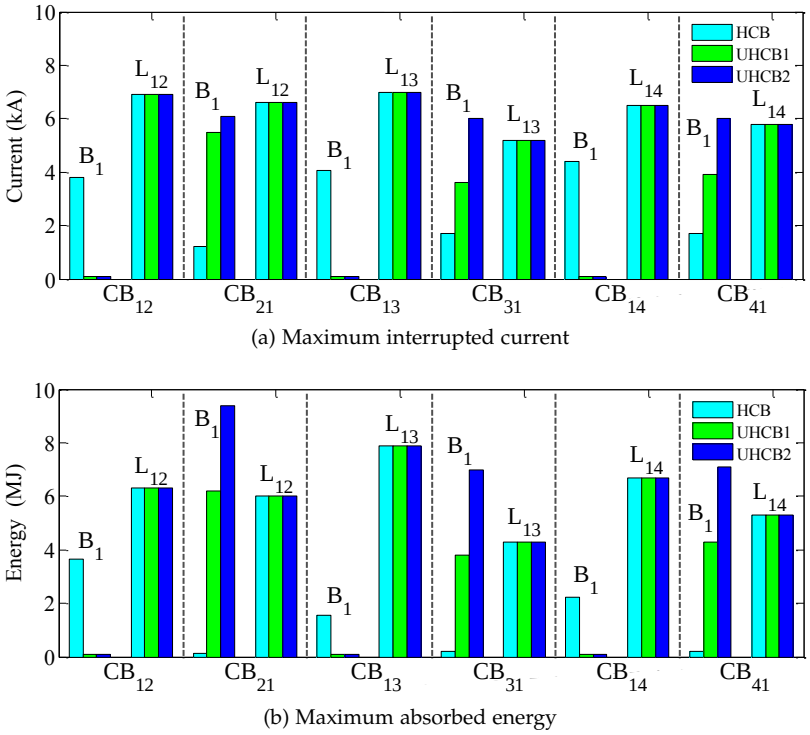


(c) Arm currents of MMC 4 for communication-based unidirectional protection scheme based on UHCB

as compared to the line fault conditions (see Figure 4.18(b)). Hence, the surge arresters in UHCBs with overcurrent-based method are required to be rated for higher energy absorption as compared to the HCBs with the typical strategy.

4.3.6 *Impact on the Converters*

As seen in Figures 4.15, 4.16 and 4.17, MMC 2 arm currents reach higher values as compared to the arm currents of other MMCs. MMC 2 is connected to the faulted bus (B_1) through a 100 km cable, which is shorter than other adjacent cables. Therefore, MMC 2 is more influenced by the fault transient as compared to the other MMCs. Furthermore, as can be seen in Figure 4.15(b), one of MMC 2 arm cur-



(a) Maximum interrupted current

(b) Maximum absorbed energy

Figure 4.18: Maximum interrupted current and absorbed energy in different dc circuit breakers during dc bus and line faults.

rents reaches almost 3 kA, which would be higher than self-protection threshold level of MMC. Although in this study MMC 2 is not blocked, the application of unidirectional protection strategy may cause blocking of the MMCs connected to the faulted bus by a short transmission line. This issue can be avoided by either slight increase in the inductance of dcCBs limiting inductor or using IGBTs with higher current capability in MMCs.

4.3.7 *Impact on the Number of Required Semiconductor Switches*

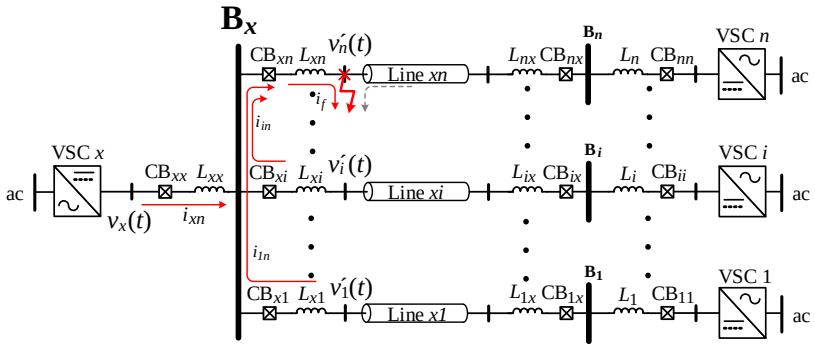
The MBU and LCS in the UHCB requires half the number of semiconductors as compared to the HCBs. For instance, an HCB with 320 kV and 9 kA voltage and current ratings requires 1416 IGBTs with 3.3 kV voltage rating in the MBU [162]. By applying unidirectional protection strategy this number can be reduced to 708 by mean of the UHCB. Due to the large number of required IGBTs by the HCB and considering the peripheral circuits and elements for each IGBT, this reduction can significantly decrease the initial investment for implementation of the HCBs.

4.4 *Application of CRCB in Protection of MT-HVdc Grid*

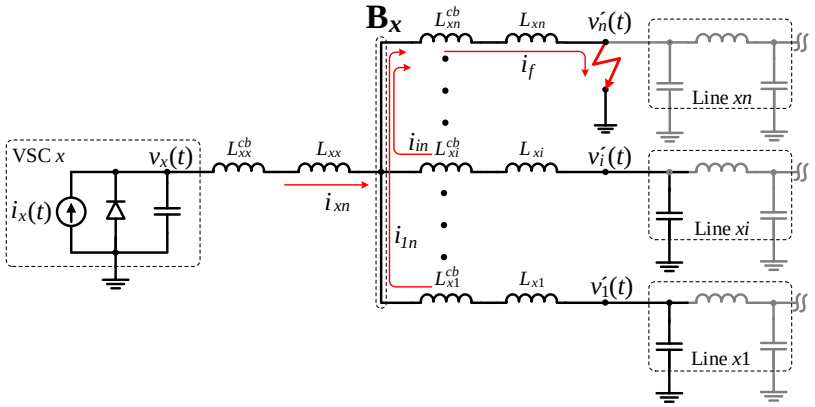
4.4.1 *The CRCB Integration into the MT-HVdc Grid*

The design procedure of the CRCB for a point-to-point HVdc system can be extended to meshed HVdc grids. The extended design procedure can be advanced by defining the value of short circuit current at the interruption instance for each CRCB in a meshed grid. The

Figure 4.19: UCBs arrangement and directions and fault current directions.



(a) Typical hybrid dc circuit breaker schematic



(b) Unidirectional hybrid dc circuit breaker schematic

value of fault current at the interruption instance depends on the pre-fault current value, fault identification delay, CRCB operation delay, size of current limiting inductor and fault distance from the corresponding CRCB. The most severe short circuit fault scenario sets the requirements for the CRCB. The fault identification delay (t_d), which depends on the fault distance from current sensors can be given by:

$$t_d\,(x) = t_t\,(x) + t_s + t_f + t_p \tag{4.6}$$

where $t_t\,(x)$ is the time required by traveling waves to reach the sensor associated with the relay. t_t depends on the distance between fault location and the sensor (x). t_s, t_f and t_p are measurement, signal conditioning circuits and relay processing delays, respectively.

Figure 4.19(a) shows a dc bus (B_x) connected to a VSC (VSC x) and also connected to n other VSCs through the transmission lines. CB_{xj} represents the CRCB attached to line L_{xj} and CB_{xx} represents the CRCB connected to VSC x. Different fault currents flowing from the converter station and the transmission lines are depicted in Figure 4.19(a) for a line fault at the end of line L_{xn} and close to the CB_{xn}. Figure 4.19(b) depicts a simplified equivalent circuit of the system shown in Figure 4.19(a). In Figure 4.19(b), the converter is replaced with a simplified model connected to the dc bus capacitor.

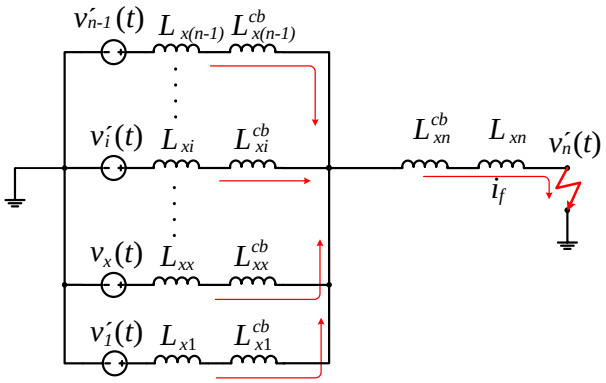


Figure 4.20: (a) Maximum interrupted current and (b) absorbed energy in different dc circuit breakers during dc bus and line faults.

The current limiting inductors of CRCBs are represented by $L_{cb,ij}$. The transmission lines are represented by simple line model and the line resistance is neglected. Fast protection algorithms are supposed to detect the line short circuit faults in range of milliseconds depending on the fault location. Hence, a fault close to the circuit breaker is detected in less than a millisecond. During this short fault detection time, the voltage of converter stations can be considered constant. Due to the presence of line current smoothing reactors and the dcCBs' limiting inductors the voltage of adjacent transmission lines can be assumed to be constant. $v'_n(t)$ is the voltage at fault location, which drops to zero immediately after fault inception. Thereafter, the equivalent circuit can be simplified even more for the short period of time after the fault inception. The second simplified equivalent circuit is shown in Figure 4.20. Although this circuit is valid until the adjacent lines voltage and the converter station voltage collapse, it is suitable to estimate the initial rate of rise of fault current in the grid.

The initial conditions of the circuit is given by:

$$\begin{aligned} &i_{f,xn}(0) = I^{xn}_{pre} \\ &v_x(0) = V_{dc} \\ &v'_n(0^+) = 0 \\ &v'_j(0^+) = V_{dc}, \quad j = 1, 2, ..., n-1 \end{aligned} \tag{4.7}$$

where $i_{f,xn}$ is the fault current in CB_{xn} and I^{xn}_{pre} is the pre-fault current of CB_{xn}. Considering the initial conditions of the equivalent circuit, the following equation holds:

$$V_{dc} = \left(\left(L'_{x1} \parallel L'_{x2} \parallel ... \parallel L'_{x(n-1)} \parallel ... \parallel L'_{xn}\right) + L'_{xn}\right) \frac{\mathrm{d}i_{f,xn}(0^+)}{\mathrm{d}t} \tag{4.8}$$

where L'_{xj} represents sum of the current limiting inductor of CB_{xj} and the current smoothing reactor of line L_{xj}. L'_{xx} represents the sum of current limiting inductor of CB_{xx} and the inductance of the dc bus filter associated with VSC x. Based on Equation 4.8, the initial rate of

rise of fault current in CB_{xn} can be approximated as:

$$\frac{\mathrm{d}i_{f,xn}\left(0^{+}\right)}{\mathrm{d}t}=\frac{V_{dc}\sum_{j=1}^{n-1}\frac{1}{L'_{xj}}}{1+L'_{xi}\sum_{j=1}^{n-1}\frac{1}{L'_{xj}}} \tag{4.9}$$

The obtained initial rate of rise of current is almost constant for the short period of time before fault detection. Hence, the fault current value at the interruption instance for any CRCB in the grid can be approximated by:

$$I_{f,xn}^{max}=\frac{V_{dc}\left(t_d+t_{cb}\right)\sum_{j=1}^{n-1}\frac{1}{L'_{xj}}}{1+L'_{xi}\sum_{j=1}^{n-1}\frac{1}{L'_{xj}}}+I_{xn}^{pre} \tag{4.10}$$

where $I_{f,xn}^{max}$ is the maximum fault current in CB_{xn} and V_{dc} is the system nominal voltage. t_{cb} is the CRCB operation delay time and I_{xn}^{pre} is the pre-fault current of CB_{xn}. The internal parameters of each CRCB can be calculated based on the following equations:

$$R_{cb,ij}<\frac{V_{dc}}{I_{f,ij}^{max}} \tag{4.11}$$

$$C_{cb,ij}>\frac{4\left(L_{ij}+L_{ij}^{cb}+L_{ij}+L_{ji}+L_{ji}^{cb}\right)}{\left(R_{cb,ij}+R_{L,ij}\right)^{2}} \tag{4.12}$$

where R_{ij}, $C_{cb,ij}$, $L_{L,ij}$ and $R_{L,ij}$ represent the internal resistor of CB_{ij}, internal capacitor of the CB_{ij}, stray inductance of the transmission line L_{ij} and resistance of the transmission line L_{ij}, respectively.

4.4.2 Models

Test System

The four-terminal meshed HVdc grid model from previous section is employed in this study. The MMC IGBTs are blocked when the arm current of the MMC exceeds 2.5 kA. All transmission lines are equipped with current smoothing reactor with inductance of 40 mH at both ends.

Circuit Breaker Models

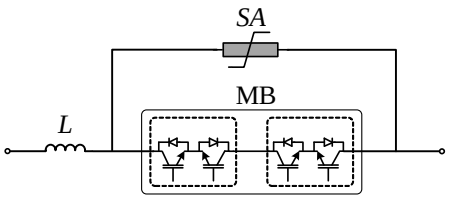


Figure 4.21: The topology of typical solid-state dc circuit breaker.

The models of two types of dcCBs including CRCB and typical SSCB are employed in this study. The detail model of CRCB from chapter 3 is used. The value of current limiting inductor of the CRCB is set to 10 mH.

The model of typical SSCB includes IGBTs with antiparallel diodes. As can be seen from Figure 4.21, configuration of IGBTs guarantees bidirectional current interruption and conduction. The operation delay of the SSCB is considered to be no more than 250 μs. Moreover,

the SSCB model contains a surge arrester (SA). The OVP voltage of surge arrester is set to 480 kV. The value of current limiting inductor in the SSCB is set to 10 mH.

4.4.3 Simulation Results

In symmetric monopole HVdc systems, the pole-to-ground faults do not lead to steady-state fault currents. A pole-to-pole dc short circuit fault is the most severe case for interruption in HVdc systems. In this study, dc line pole-to-pole short circuit faults and dc bus pole-to-pole faults are investigated. To compare the performance of CRCB and SSCB, different fault scenarios are studied. Similar to the previous subsection the studied dc fault is a low impedance fault with 100 mΩ resistance.

Transmission Line Fault

The dc pole-to-pole short circuit faults are applied into the all transmission lines of the system in different locations at $t = 0$ s. The trip time of all the dcCBs for various fault locations is illustrated in Figure 4.22. As can be seen in the figure, the fault identification and trip time for faults at the corresponding dcCB varies between 0.35 to 0.41 ms for different lines. The value of t_d in Equation 4.6 must be considered to be the maximum trip time for faults at dcCBs to calculate the maximum fault current for the corresponding dcCB. Furthermore, the trip time for faults with 200 km distance from the corresponding dcCBs is always less than 1.54 ms.

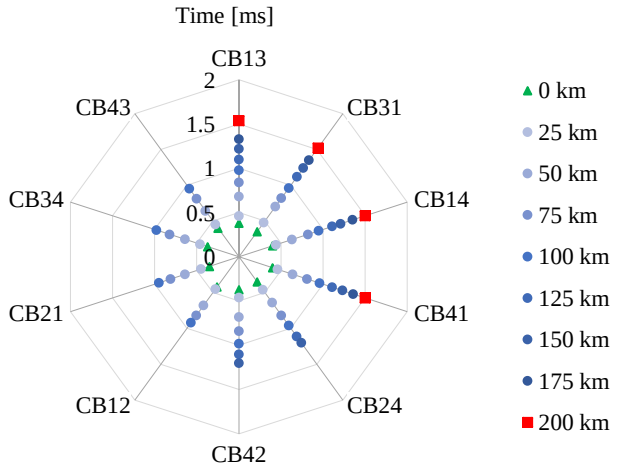
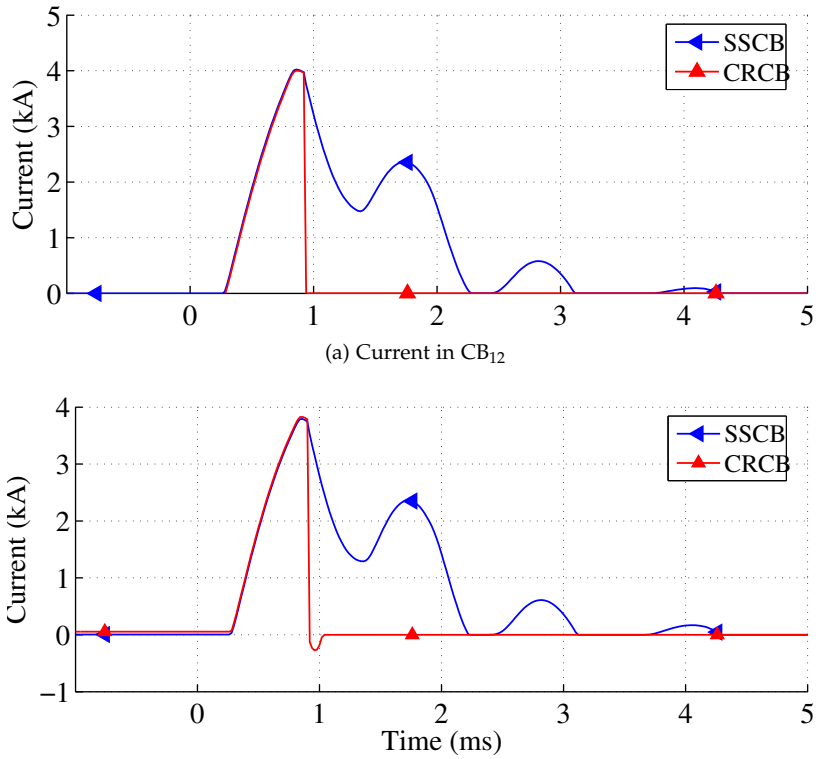


Figure 4.22: (a) Maximum interrupted current and (b) absorbed energy in different dc circuit breakers during dc bus and line faults.

The fault currents for the SSCB and CRCB during the fault on the line 12, 13 and 14 are shown in Figure 4.23, 4.24 and 4.25. The CRCB interrupts the fault current promptly due to its topological characteristics. The fault current in typical SSCB takes more time to become zero due to lower impedance of surge arrester during the fault interruption transient. Both types of dcCBs handle equal peak values of fault currents due to the identical fault identification and trip time of protection algorithm.

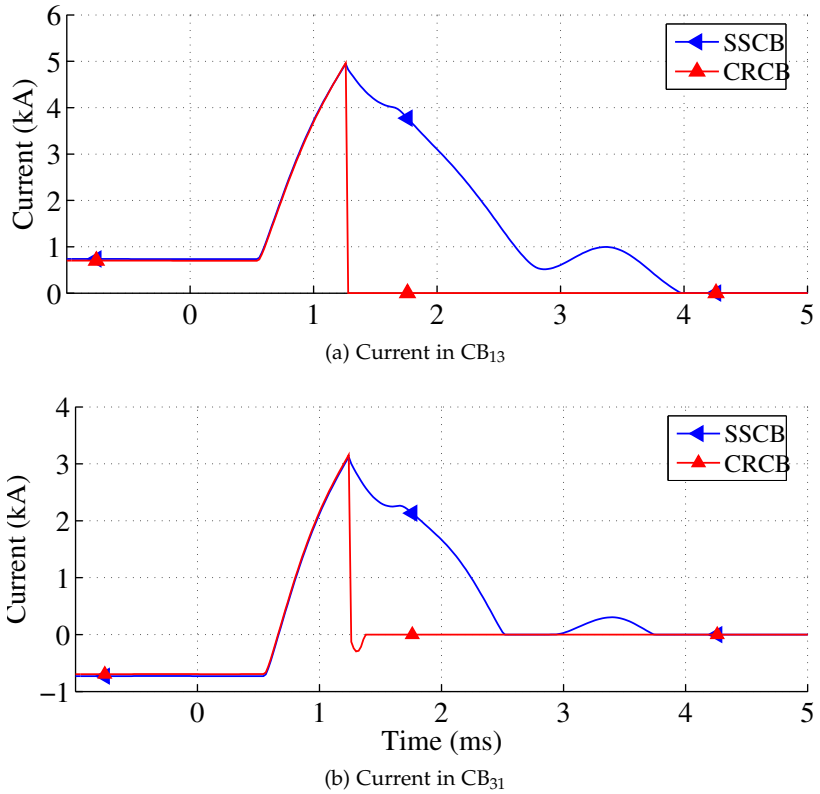
Figure 4.23: Current in CB_{21} and CB_{12} during fault on transmission line L_{14} for CRCB based and SSCB based systems.



(a) Current in CB_{12}

(b) Current in CB_{21}

Figure 4.24: Current in CB_{31} and CB_{13} during fault on transmission line L_{14} for CRCB based and SSCB based systems.

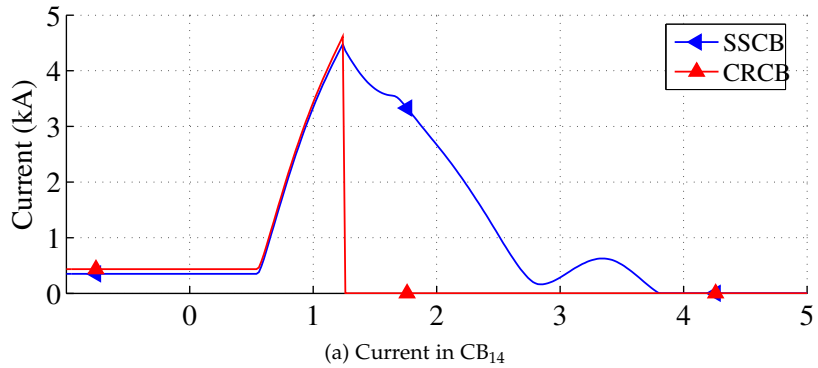


(a) Current in CB_{13}

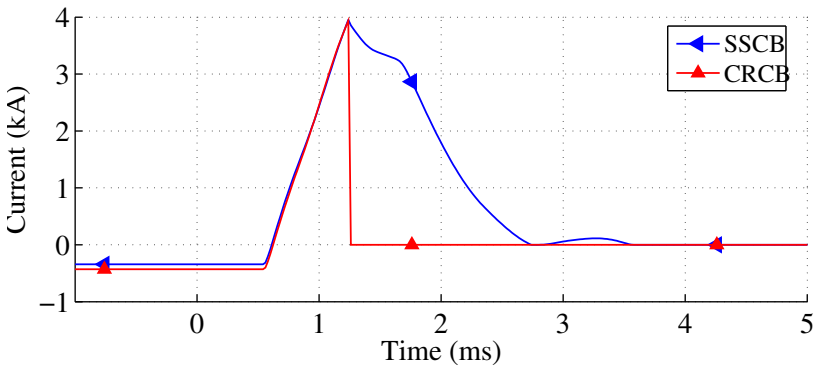
(b) Current in CB_{31}

dc Bus Fault

A dc bus fault is considered to be the most sever type of dc fault from converter point of view. Due to the absence of transmission



(a) Current in CB_{14}



(b) Current in CB_{41}

Figure 4.25: Current in CB_{31} and CB_{13} during fault on transmission line L_{14} for CRCB based and SSCB based systems.

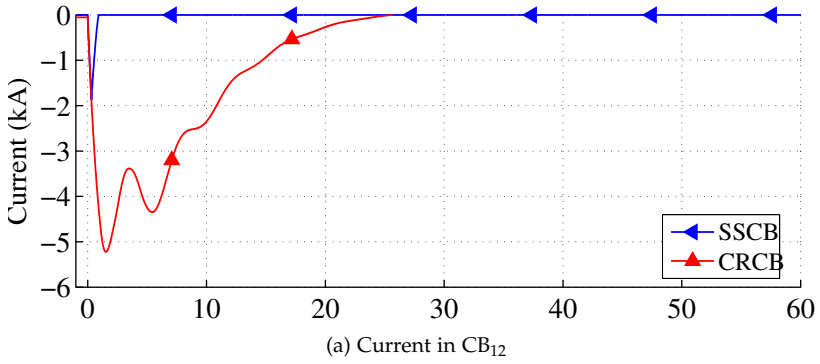
line inductance, the fault current quickly reaches high values if it is not promptly interrupted. Four dc bus short circuit fault scenarios including faults at buses B_1, B_2, B_3 and B_4 are studied in this section. The local protection algorithm generates the trip signal for the faults in different buses almost at the same time. The dc bus fault trip time is almost 0.2 ms for the applied protection algorithm. Hence, in case of BCBs, the dc bus fault can be cleared immediately after detection.

On the other hand, in the unidirectional protection strategy, only the converter station dcCB is able to promptly interrupt the current. The interruption of fault currents flowing from the adjacent lines takes longer due to delay in detection at the remote side of the transmission lines. The fault detection times for unidirectional protection strategy are illustrated in Table 4.2.

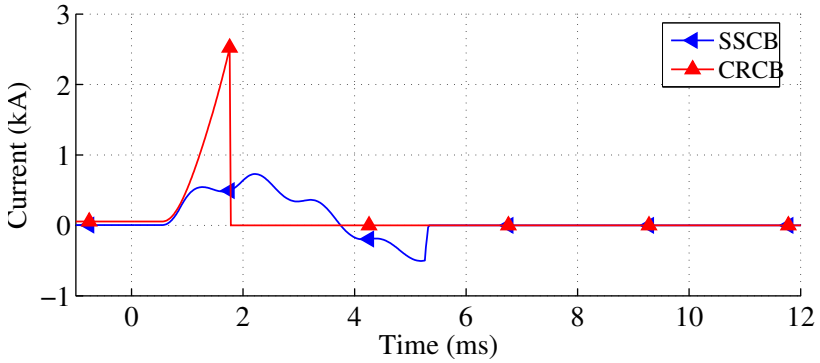
	Bus 1	**Bus 2**	**Bus 3**	**Bus 4**
CB_{21}	1.52 ms	-	-	-
CB_{31}	2.48 ms	-	-	-
CB_{41}	2.53 ms	-	-	-
CB_{12}	-	1.46 ms	-	-
CB_{42}	-	2.04 ms	-	-
CB_{13}	-	-	2.53 ms	-
CB_{43}	-	-	1.54 ms	-
CB_{14}	-	-	-	2.49 ms
CB_{24}	-	-	-	2.01 ms
CB_{34}	-	-	-	1.5 ms

Table 4.2: Fault detection times for unidirectional protection strategy.

Figure 4.26: Current in CB_{21} and CB_{12} during fault at dc bus B_1 for HCB based and two UHCB based protection schemes.

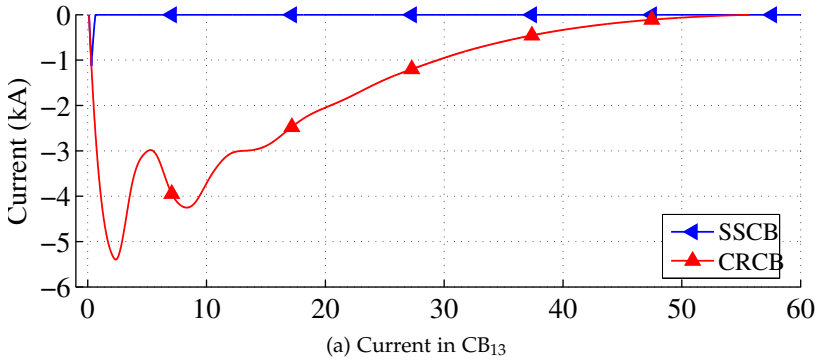


(a) Current in CB_{12}

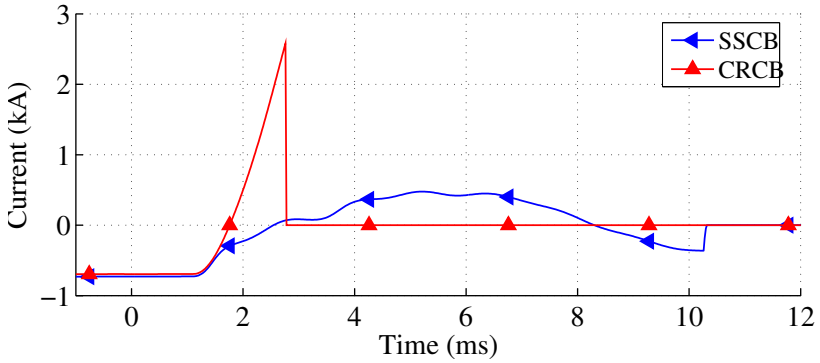


(b) Current in CB_{21}

Figure 4.27: Current in CB_{31} and CB_{13} during fault at dc bus B_1 for HCB based and two UHCB based protection schemes.

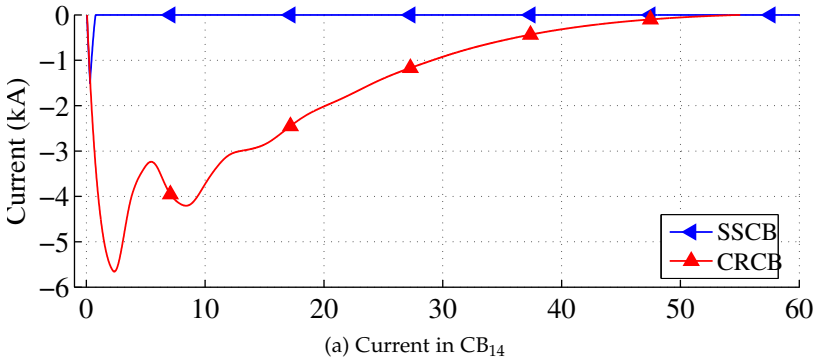


(a) Current in CB_{13}

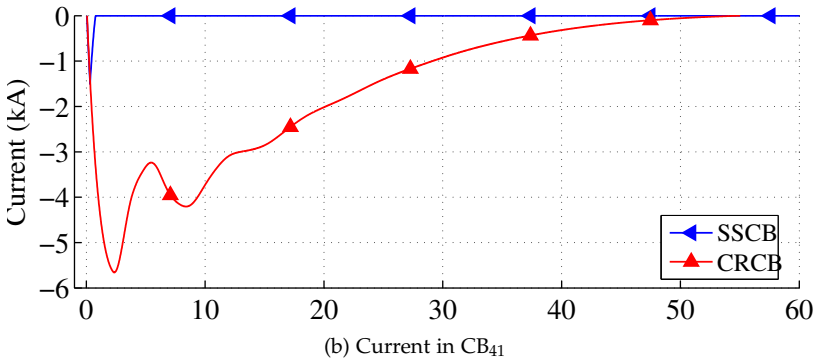


(b) Current in CB_{31}

The current waveforms for the fault at dc bus B_1 are presented in Figures 4.26, 4.27 and 4.28. Because of the similar performance of the dcCB of converter station in both bidirectional and unidirectional cases, their current waveforms are not presented. Since the fault



(a) Current in CB_{14}



(b) Current in CB_{41}

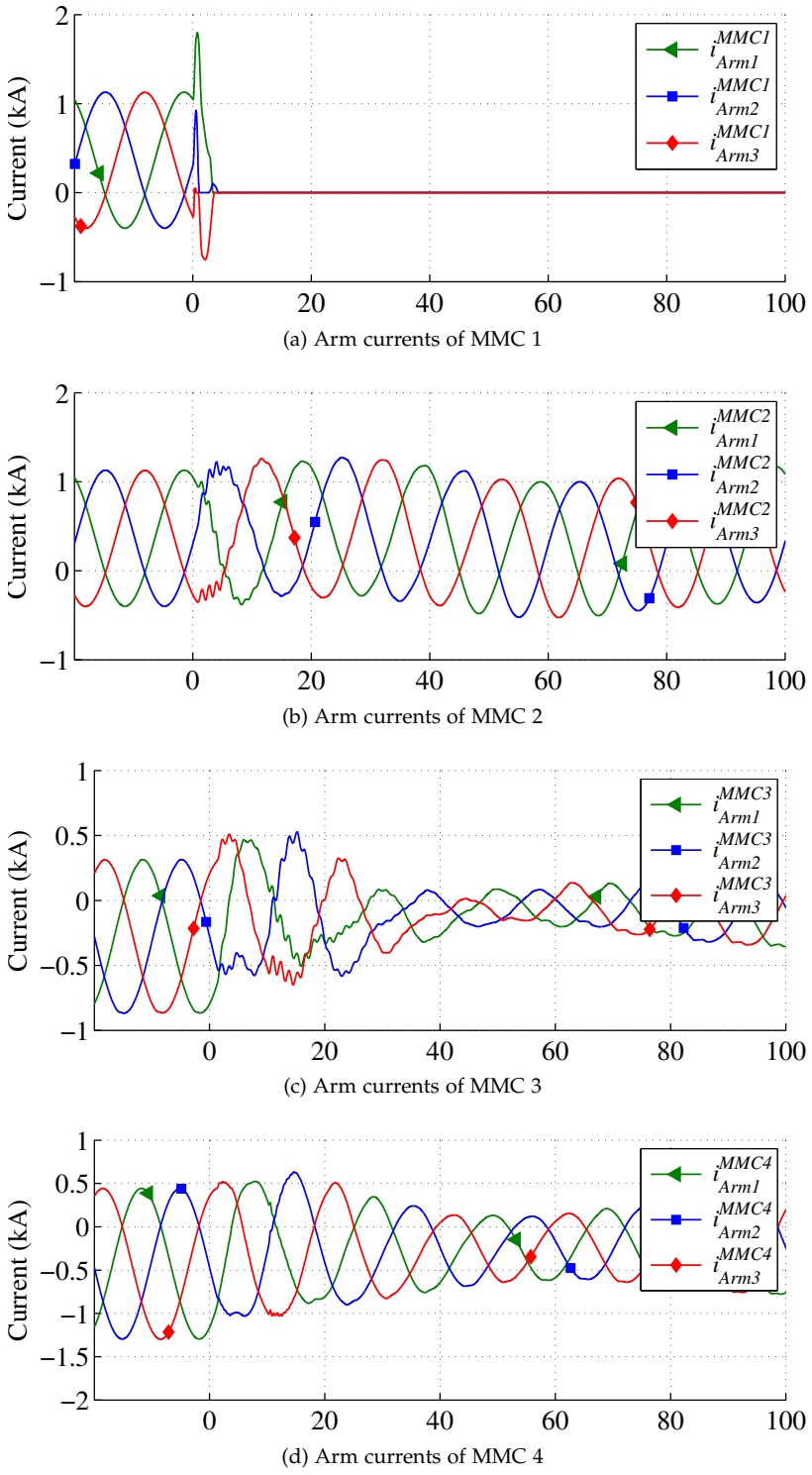
Figure 4.28: Current in CB_{31} and CB_{13} during fault at dc bus B_1 for HCB based and two UHCB based protection schemes.

is applied at bus B_1, the adjacent dcCBs (CB_{12}, CB_{13} and CB_{14}) are tripped by the local protection algorithm almost 0.2 ms after fault inception. Figures 4.26(a), 4.27(a) and 4.28(a) show that the fault currents flowing through CB_{12}, CB_{13} and CB_{14} are interrupted before reaching high values. In case of UCBs, the fault currents flow for a longer period until they are interrupted by the remote dcCBs (CB_{21}, CB_{31} and CB_{41}).

In unidirectional strategy, the absolute value of current through CB_{12}, CB_{13} and CB_{14} reaches 5.1, 5.3 and 5.6 kA, respectively. These fault currents flow in the backward directions of the mentioned UCBs and cannot be interrupted. These fault currents are detected by the protection relays at the remote ends of the adjacent transmission lines. Therefore, CB_{21}, CB_{31} and CB_{41} are tripped by their corresponding protection relays. Figures 4.26(b), 4.27(b) and 4.28(b) show the interrupted fault current through CB_{21}, CB_{31} and CB_{41}, respectively. The fault currents in CB_{21}, CB_{31} and CB_{41} reaches 2.5, 2.5 and 3 kA, respectively.

Figures 4.29(a)-(d) and 4.30(a)-(d)show the arm currents of MMC 1, 2, 3 and 4 for unidirectional and bidirectional protection strategies, respectively. Figures 4.29(a) and 4.29(a) show that due to operation of corresponding dcCBs during the fault at B_1, MMC 1 is isolated from the dc grid and its arm currents fall to zero. In both unidirectional and bidirectional strategies, the permanent dc bus fault causes discontinuity in the power and outage of adjacent lines. Figures 4.29(b)-(d) and 4.30(b)-(d) show the arm currents of converters associated with the non-faulted dc buses. Due to fast response of the protection system, the converters are not significantly stressed.

Figure 4.29: Arm currents of MMCs for CRCB based protection scheme.



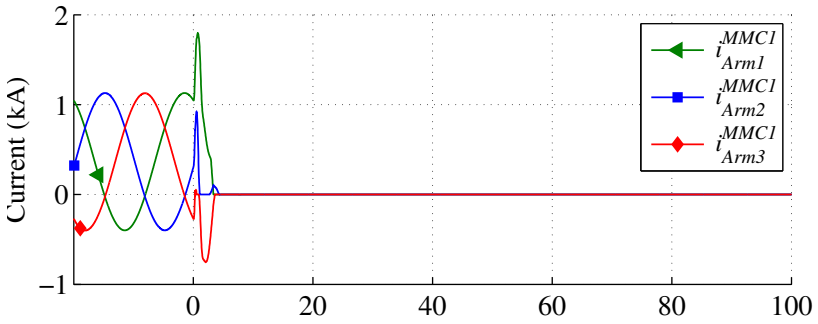
(a) Arm currents of MMC 1

(b) Arm currents of MMC 2

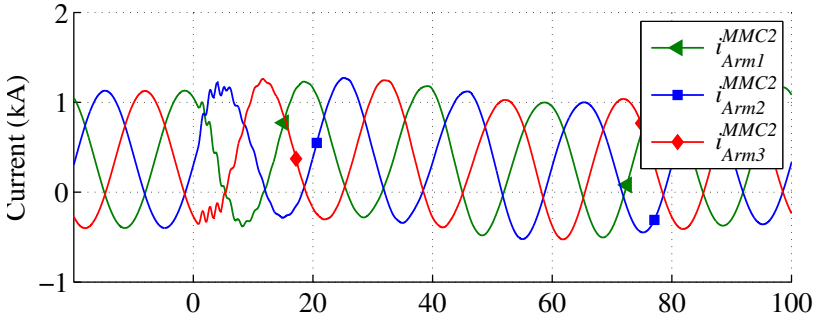
(c) Arm currents of MMC 3

(d) Arm currents of MMC 4

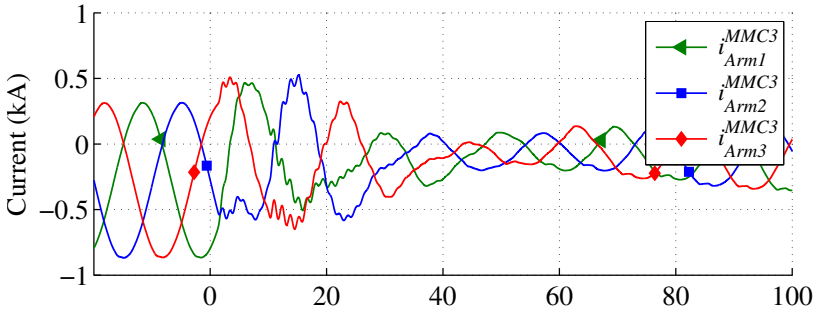
Figures 4.29(b), (c) and (d) show the arm currents of converters associated with the non-faulted dc buses for the unidirectional protection strategy. Compared to Figure 4.30(b), (c) and (d), the arm currents of converter are distorted more in the unidirectional protection scheme. The arm currents in the bidirectional scheme are not highly distorted from magnitude point of view. The main reason for the arm current distortion is the interaction between the CRCB



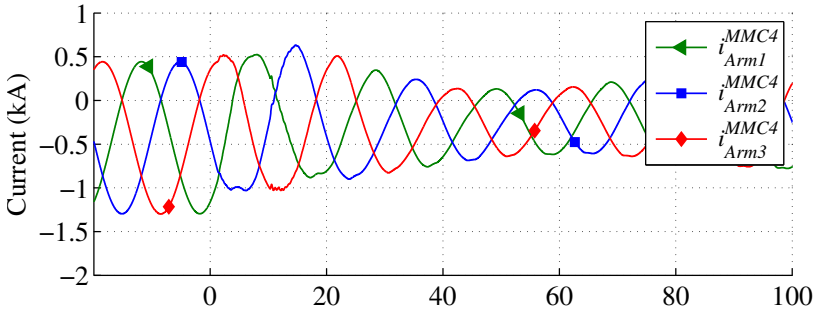
(a) Arm currents of MMC 1



(b) Arm currents of MMC 2



(c) Arm currents of MMC 3



(d) Arm currents of MMC 4

Figure 4.30: Arm currents of MMCs for SSCB based protection scheme.

and the converter dc side during fault interruption. The converters can recover and regulate the power based on the updated operating points after outage of MMC 1 in both protection strategies.

4.4.4 *Impact on the Current Interruption Capability*

The unidirectional protection scheme interrupts the dc bus fault currents with more delay as compared to the bidirectional one. Thus,

a comparison of dcCBs sizing (current breaking capability) in both cases is required to assess the feasibility of unidirectional protection strategy. To compare the dcCB interruption capability in both strategies, the maximum interrupted transmission line fault current in all dcCBs of the MT-HVdc grid for various fault locations are depicted in Figure 4.31.

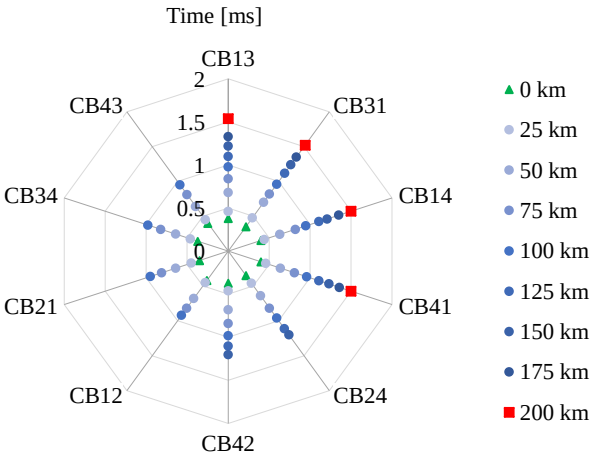
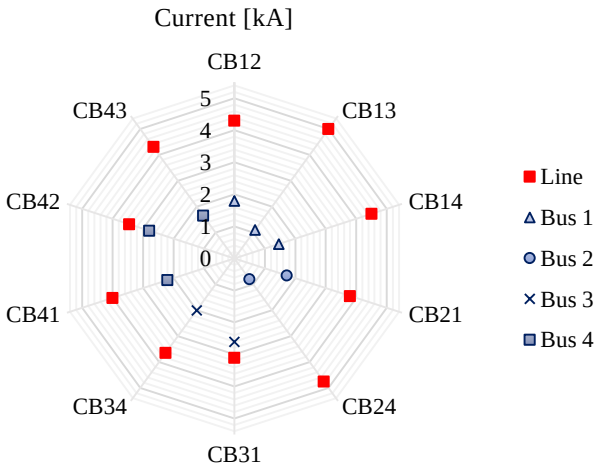
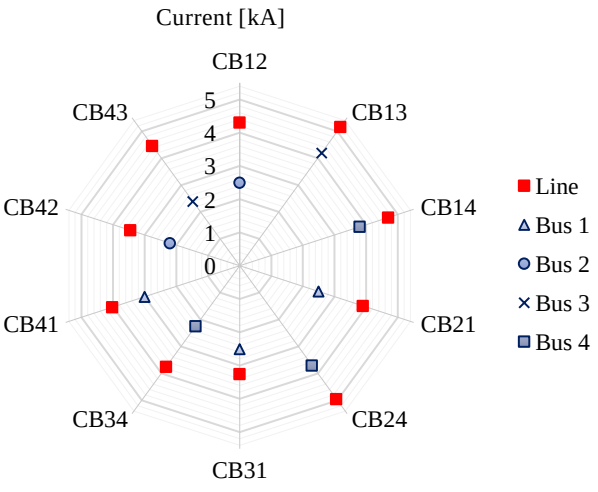


Figure 4.31: (a) Maximum interrupted current and (b) absorbed energy in different dc circuit breakers during dc bus and line faults.



(a) Typical hybrid dc circuit breaker schematic



(b) Unidirectional hybrid dc circuit breaker schematic

Figure 4.32: UCBs arrangement and directions and fault current directions.

Figure 4.31 shows that a fault at a location 75 km far from its corresponding dcCB reaches the highest value. This is due to the non-linear characteristic of the transmission line and its impact on the traveling wave propagation time together with the current limiting behavior of inductance of the cable and different tripping times. The highest value of interrupted fault current for various transmission line faults is shown in Figure 4.31.

Figure 4.32(a) and (b) show the required current interruption capability for all possible dc bus faults for BCBs and UCBs, respectively. Although the UCBs should interrupt higher level of fault current during bus fault as compared to the BCBs, their maximum interrupted current is still lower than that of the line fault with 75 km distance. These figures show that the maximum current interruption capability for both protection strategies are the same. Although dc bus fault currents are cleared later in the unidirectional protection strategy compared to the bidirectional strategy, the inductance of long transmission lines limits the rate of rise of current and prevent it from reaching higher values.

4.5 Conclusion

A unidirectional protection strategy for MT-HVdc grid is suggested in this chapter. The results of study confirm that the unidirectional protection strategy can be utilized for protection of the MT-HVdc grid. Four types of dcCBs are considered in this study including typical bidirectional HCB, unidirectional HCB, typical SSCB and the CRCB. The HCB based protection system is investigated though two methods for remote dcCB tripping. The considered methods include a communication-based method and an overcurrent-based method. The communication-based method shows better performance as compared to the the overcurrent-based method.

The results of comparison study for different parameters of HCB and UHCB imply that the current rating of HCB and the size of surge arresters are not necessarily different for the bidirectional and unidirectional strategies. However, the impact of suggested strategy on all converters of the grid, particularly the converters with shorter transmission line between them should be analyzed. In order to avoid blocking of the MMCs at healthy buses, slight increase in HCB limiting inductor size or current rating of MMC's IGBTs might be required.

The compatibility of fast local protection algorithms with UCBs and their ability in clearing dc bus faults are the main concerns regarding their application in MT-HVdc grids. The performance of a fast local protection algorithm together with UCBs in a four-terminal HVdc grid is also studied in this chapter.

The design procedure of the CRCB is extended to the multi-terminal HVdc grid and formulated. The internal parameters of CRCB are calculated based on the simplified design approach. The fault detection criteria of a current-based non-unit protection algorithm, which was originally developed for bidirectional protection strategies was adopted for a unidirectional protection strategy in MT-HVdc grid.

Both of the mentioned protection schemes show similar performances during dc transmission line faults. The highest transmission line fault currents are observed when the fault distance from the closest dcCB is around 75 km. This distance depends on the cable characteristics and the protection algorithm response time. The dc bus fault is detected locally by the differential protection algorithm in the bidirectional protection strategy and remotely as an endpoint transmission line fault when using the unidirectional protection strategy. The current interruption requirements of UCBs are identified to be similar to those of the BCBs.

This study suggest that, UCBs can protect MT-HVdc grids similar to the BCBs while using fewer semiconductor switches. The application of UCBs may reduce the implementation cost of the dcCBs for both SSCBs and HCBs. Moreover, the power losses of SSCBs can be reduced significantly by using UCBs, which would make SSCBs a suitable candidate for application in MT-HVdc grids.

Part III

Fault Current Limiting dc Circuit Breaker

5
Fault Current Limiting Hybrid dc Circuit Breaker

A. Mokhberdoran, A. Carvalho, N. Silva, H. Leite, A. Carrapatoso, "Application study of superconducting fault current limiters in meshed HVdc grids protected by fast protection relays," *Electric Power Systems Research Journal*, Volume 143, February 2017, Pages 292-302.

Words were not given to man in order to conceal his thoughts.
José Saramago, Portuguese Writer, 1922-2010

As discussed in chapter 2, the fault current in the MT-HVdc grids can reach large magnitudes. Therefore, the dcCBs are required to be designed for interruption of high current. The interruption of high current not only demands for greater number of semiconductor switches (due to the additional parallel branches in the MB unit structure in both SSCB and HCB), but also requires large surge arresters for interruption energy absorption. To prevent the dc fault current from reaching destructive values, superconducting fault current limiter (SFCL) has been considered as a solution in the literature. Based on the literature review in subsection 2.2.4, the application of SFCLs in the protection of point-to-point and MT-HVdc systems has been investigated in the literature

However, the current literature shows no study on application of SFCL in MT-HVdc grids considering the fast protection schemes. Furthermore, despite the wide application of variants of MMC in the modern HVdc projects, most of the studies in literature have been carried out based on the conventional VSCs.

This chapter attempts to analyze and asses the application of SFCL in the protection of meshed HVdc grids considering non-unit protective relaying schemes. Moreover, this chapter addresses the impact of SFCL integration on current limiting inductors, current stress on the HCB, surge arrester energy and the dc fault current characteristics. The present assessment is carried out by utilizing the behavioral model of the generic resistive type SFCL.

5.1 Fault Current Limiting Hybrid dc Circuit Breaker

A current limiting HCB can be resulted from integration of an SFCL module into the typical HCB. Figure 5.1 depicts the topology of a current limiting HCB. The SFCL position is illustrated in Figure 5.1 by dashed line block. The operation principles of the current limiting HCB is the same as those of typicality HCB as explained in chapter 2. It is clear that, the results of this study could be valid for all types of the hybrid dc circuit breakers operating based on the same concept.

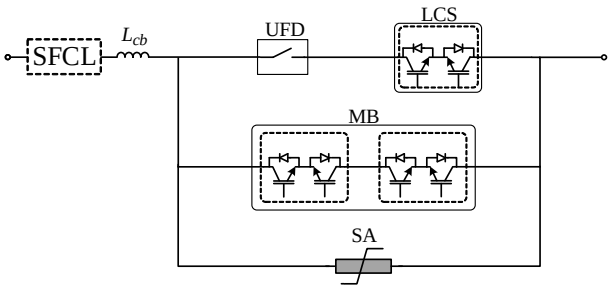


Figure 5.1: SFCL integration into the structure of hybrid dc circuit breaker.

5.2 Models

5.2.1 Test System

The test system is a four-terminal meshed HVdc grid model as detailed in appendix A. The cables are modeled using the frequency dependent modeling approach in the electromagnetic transient type software as explained in appendix A.

5.2.2 Superconducting Fault Current Limiter Model

Several types of SFCLs including the resistive and inductive ones exist [174,216]. Each type has been investigated for different applications in the literature. Generally, when the current density (J) in the high temperature SFCL exceeds the critical value, an electric field (E) develops across the device and its impedance increases. In order to identify the requirements of SFCL independently of its technology, a behavioral model of a generic resistive type SFCL is adopted based on modeling concept from [217]. The SFCL is modeled considering its main parameters. The SFCL's fundamental parameters can be listed as: transition time, maximum impedance, critical current, recovery time and normal condition impedance [182,217]. Below the critical current, the SFCL shows a very low resistance. As soon as the current exceeds the critical value, its impedance increases exponentially to the maximum impedance value within the transition time. After current falls below the triggering current the SFCL's impedance decreases to its minimum impedance within the recovery time [217]. The model of SFCL unit is developed as a time-dependent nonlinear resistor [217]. Figure 5.2 depicts the utilized SFCL model. The SFCL transition characteristics for maximum resistance of 20 Ω and four different

transition times are implemented in four lookup tables. The SFCLs transition curves for different transition times are plotted using the mentioned look up tables and are shown in Figure 5.3. The SFCLs should be connected in series to reach the higher SFCL resistances. Therefore, to reach resistance values of 30, 40, 50, 60 Ω, multiplication factors of 1.5, 2, 2.5, 3 are needed to be applied in R_{SFCL} block, respectively. The resistor has its minimum resistance (R_{min}) until the SFCL current reaches the critical value. At this instant, state of the controlled switch is changed and the resistance increases based on the lookup table values. The recovery time is implemented in the "Timing & Logic" block of the SFCL model.

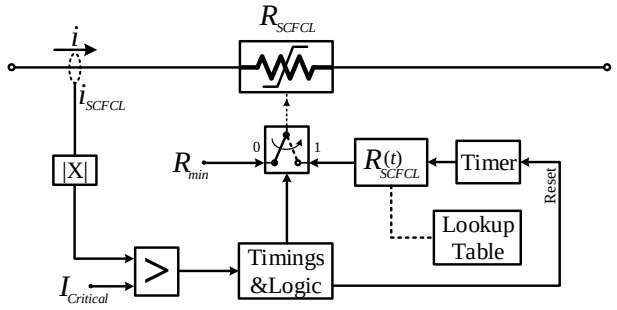


Figure 5.2: Utilized SFCL model.

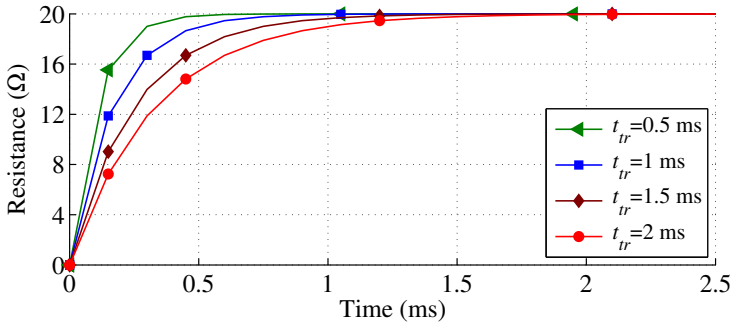


Figure 5.3: Generic SFCL characteristics plotted out of look up table.

5.2.3 *dc Circuit Breaker Model*

A detailed model of hybrid dc circuit breaker, which is depicted in Figure 5.1 is developed based on [134,138,140]. The turn-off delay of IGBTs of the LCS unit are set to 250 μs to model the commutation time [139] and the UFD action time is set to 2 ms [218]. The individual surge arresters of the IGBT positions are modeled as one surge arrester with the reference voltage of 480 kV [134,138,140]. The surge arrester is modeled employing the piecewise linear modeling approach using the curve shown in Figure 3.6 in PSCAD. The current limiting inductor of HCB is set to 100 mH to avoid the self-blocking of MMCs during the end-point line short circuit faults [21].

5.2.4 *Protection System Model*

The fault identification time can reach ten milliseconds in slow algorithms [184]. The meshed dc grid can be protected by low-speed

protection algorithms, only if the fault tolerant converter topologies or fault current limiters are employed. The non-unit protective schemes can identify the fault after inception in less than 2 ms in a line with 100 km length [184]. In the non-unit protection schemes each line is protected by two dcCBs at its ends, which receive the trip command from dc distance protective relays. For instance, in Figure 5.4, the line L_{mn} is protected by the circuit breakers CB_{mn} and CB_{nm}. The dc fault transient is in the range of millisecond dominated by traveling waves. The propagation velocity of these waves is dependent on the inductance and capacitance of the dc transmission line [184,219]. Since the details of the fault identification method in HVdc systems is not the subject of this study, a behavioral model of the protection relay is employed. The total fault identification delay time can be given by Equation 4.6, which was explained in chapter 4.

When the fault incepts at the midpoint of the transmission line, it is expected to be detected by the relays of both ends at the same time. The dc faults at endpoints of the line are detected faster by the closer relay than the farther one. Tt can be estimated by considering the traveling wave velocity using Equation 5.1 and line characteristics and fault distance using Equation 5.2.

$$v = \frac{1}{\sqrt{LC}} \tag{5.1}$$

$$t_d\,(d) = d\sqrt{LC} \tag{5.2}$$

In Equations 5.1 and 5.2, L and C are the inductance and capacitance of line per length unit, respectively and d is the fault distance. The developed model receives the fault distance as the input and generates the trip signal after required delay using Equation 4.6. Tt is calculated based on the lumped parameters of the XLPE cable. The time delay caused by the measurement devices, signal conditioning and processor ($t_s + t_f + t_p$) is assumed as 0.4 ms. The impact of delay caused by line inductances is also considered in the developed model. It is assumed that the protective relaying scheme operates properly without any malfunction.

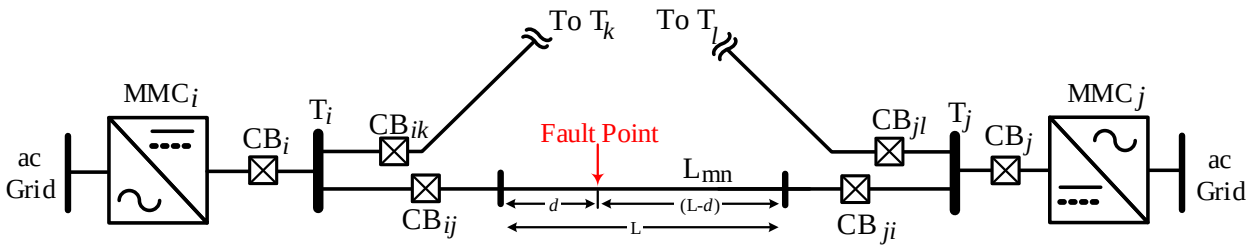
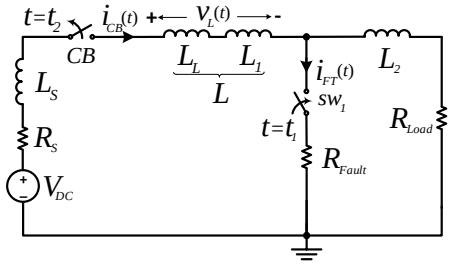


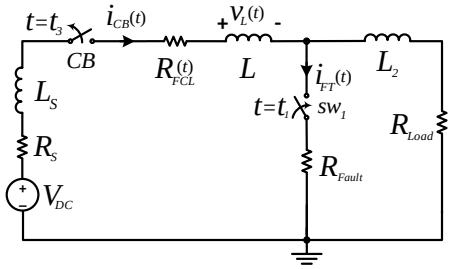
Figure 5.4: Non-unit protection of multi-terminal HVdc grids based on fast dcCBs.

5.3 *Analysis*

In order to analyze the circuit breaker current during the fault condition, the voltage source converter can be modeled as a dc voltage source and its Thevenin impedance supplying a constant load through a transmission line. Figure 5.5(a) depicts the simplified equivalent circuit of a VSC connected to a dc line and a dc circuit breaker. The transmission line resistance and capacitance are neglected. As it was mentioned in previous section, the system has two inductors including the smoothing reactor and the HCB current limiting inductor. As can be seen in Figure 5.5(a), the smoothing reactor and the current limiting inductor are shown by L_s and L_L, respectively. sw_1 represents the fault inception. R_{FCL}, R_{Fault} and R_{Load} are the SFCL, fault and load resistances, respectively. As can be seen in Figure 5.5(a), after fault incepts by closing sw_1, the transmission line inductance is divided in two sections (L_1 and L_2). The values of L_1 and L_2 depends on the fault location on the transmission line. If the fault occurs closer to the circuit breaker the value of L_1 will be smaller and can be zero if the fault happens at the beginning of the transmission line right after the circuit breaker. The line inductance between the dc source and the fault location (L_1) and the L_{cb} are added together and showed by L in Figure 5.5(b). It was mentioned that, the fault identification delay depends on the traveling wave speed, which is a function of system inductance as it is illustrated in Equation 5.1. Figure 5.5(b) depicts the simplified equivalent circuit in presence of SFCL. The SFCL can be modeled as a time-dependent resistance.



(a) Equivalent circuit without SFCL



(b) Equivalent circuit with SFCL

Figure 5.5: Simplified equivalent circuit.

Figure 5.6 shows the circuit breaker current without SFCL after a short circuit fault inception at $t = t_1$. The solid line shows the interrupted current waveform at $t = t_2$ while the dashed line represents the prospective fault current if circuit breaker does not act.

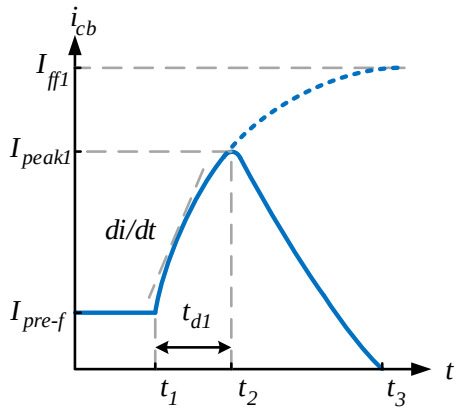


Figure 5.6: Circuit breaker current without SFCL.

The steady-state dc short circuit current for the system without SFCL (I_{ff1}) can be given by Equation 5.3.

$$I_{ff1} = \frac{V_{dc}}{R_s + R_F} \tag{5.3}$$

The steady-state dc short circuit current for a system with SFCL (I_{ff2}) is given by Equation 5.4.

$$I_{ff2} = \frac{V_{dc}}{R_s + R_F + R_{max}} \tag{5.4}$$

It is clear that the SFCL can reduce the steady-state dc short circuit current, but when the fast protection of dc grids is taken into account, the fault current at the interruption instant must be limited. After fault inception in a system without the SFCL, the current increases quickly. In MMC based systems, the initial rate of rise of dc fault current is limited by line current smoothing reactor, circuit breaker current limiting inductor and the transmission line inductance between the circuit breaker and the fault point. Although the main purpose of smoothing reactor installation is to reduce the system harmonics, they can also limit the rate of rise of fault current due to their inherent inductive characteristics. In case of the low impedance fault, the R_{Fault} is small enough to be neglected. Therefore, the dc fault current for the system without SFCL can be approximated by:

$$i_{f1}(t) = \frac{V_{dc}}{R_s}\left[1 - e^{\frac{-(t-t_1)(R_s)}{L_s+L}}\right] + i(t_1); \quad t_1 < t < t_2 \tag{5.5}$$

where $i(t_1)$ is the initial current of inductor and t_2 is the time when the circuit breaker interrupts the current. Considering the equivalent circuit in Figure 5.5(a), if the dc circuit breaker interrupts the current after a time delay, which is defined by t_{d1} and assuming the initial current equal to the system pre-fault current, the current value at the interruption instant (I_{peak1}) can be given by:

$$i_{peak1}(t) = \frac{V_{dc}}{R_s}\left[1 - e^{\frac{-t_{d1}R_s}{L_s+L}}\right] + I_{pre-f} \tag{5.6}$$

The SFCL integration into the hybrid circuit breaker may change the fault current shape in different ways. Similar to Equation 5.6, the fault current before reaching the SFCL critical current can be given by:

$$i_{f2}(t) = \frac{V_{dc}}{R_s}\left[1 - e^{\frac{-(t-t_1)(R_s)}{L_s+L}}\right] + I_{pre-f}; \quad t_1 < t < t_2 \tag{5.7}$$

Note that, in Equation 5.7, t_2 is the time when the current reaches the critical current of SFCL. In the second stage of the fault current, which can be defined between t_2 and t_3 the SFCL resistance changes and increases to reach its maximum value during the SFCL transition time (t_{tr}). Depending on the SFCL technology the system inductance also might change. Assuming the system inductance as a constant

value, the fault current in presence of SFCL can be given as:

$$i_{f2}(t) = \frac{V_{dc}}{R_s + R_{FCL}(t)} \left[1 - e^{\frac{-(t-t_2)(R_s+R_{FCL}(t))}{L_s+L}}\right] + I_{th}; \quad t_2 < t < t_3 \tag{5.8}$$

where I_{th} is the critical current of the SFCL and t_3 is the time when the current is interrupted by the HCB. Equation 5.8 illustrates that, due to the nonlinear impedance (R_{FCL}), during the transition time of the SFCL, the fault current may reach higher values than its final value. The fault current can be analyzed considering following assumption:

- Equal circuit breaker interruption time for systems with and without SFCL.
- Having less current limiting inductance with SFCL than in the system without SFCL. (Reduction in size of the current limiting inductors is one of expected improvement.)

Therefore, depending on the SFCL transition time and also its maximum impedance three different cases can be identified:

5.3.1 $t_{d2} < t_{tr}$ and $I_{ff2} < I_{peak1}$

Figure 5.7 shows the expected current waveform for this case. The SFCL transition time is longer than the circuit breaker interruption time and the fault steady-state current is lower than the peak of the current in SFCL-less system. Due to the longer time in reaching maximum impedance the dc circuit breaker might be exposed to higher current values. Due to the nonlinear increase in SFCL resistance after $t = t_2$, the $\left(\frac{di}{dt}\right)_2$ is less than the $\left(\frac{di}{dt}\right)_1$. The dashed waveform shows the prospective fault current if the circuit breaker does not trip.

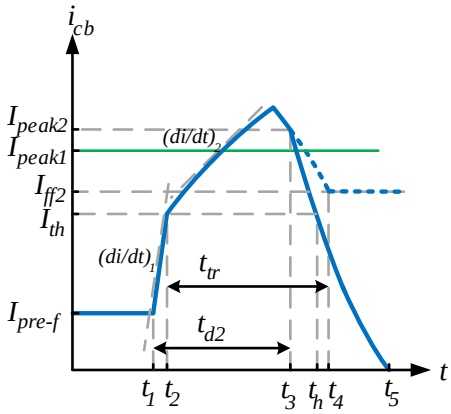


Figure 5.7: Circuit breaker current with SFCL when $t_{d2} < t_{tr}$ and $I_{ff2} < I_{peak1}$.

5.3.2 $t_{d2} > t_{tr}$ and $I_{ff2} > I_{peak1}$

The estimated current waveform is depicted in Figure 5.8 for these conditions. As can be seen, the SFCL transition time is short enough but due to its lower maximum impedance the dc circuit breaker has to interrupt higher fault currents than the normal case. It is clear that, the fault current reaches higher values than the normal case due to the lower inductance of system with SFCL.

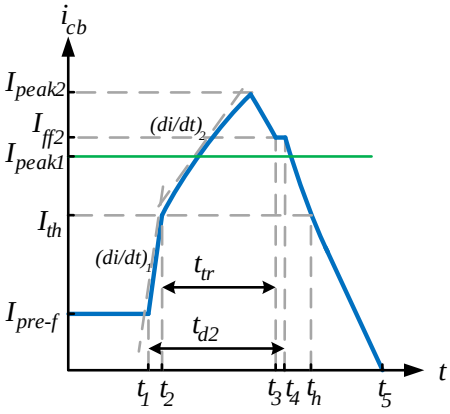


Figure 5.8: Circuit breaker current with SFCL when $t_{d2} > t_{tr}$ and $I_{ff2} > I_{peak1}$

5.3.3 $t_{d2} > t_{tr}$ and $I_{ff2} < I_{peak1}$

To guarantee the successful fault current limiting in presence of fast protective relaying schemes and fast dc circuit breakers, maximum impedance of the SFCL must be high enough to be able to limit the current below the normal interruption current. Additionally, the transition time has to be shorter than fault current interruption delay to avoid any unwanted current peak during quenching process. Figure 5.9 shows the expected fault current waveform applying mentioned conditions.

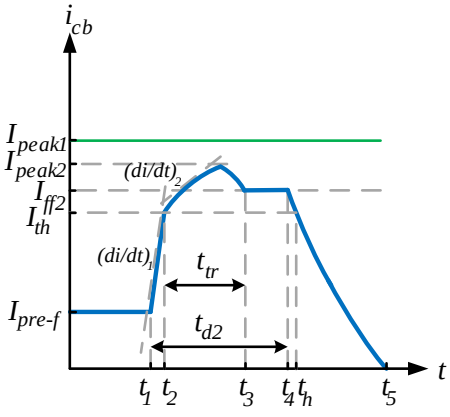


Figure 5.9: Circuit breaker current with SFCL when $t_{d2} > t_{tr}$ and $I_{ff2} < I_{peak1}$.

5.4 Simulation Results

In symmetric monopole HVdc systems the pole to ground faults do not lead to steady state fault currents. The pole-to-pole dc short circuit fault is the most severe case for interruption in HVdc systems.

In this study, the SFCL performance during dc line pole-to-pole short circuit faults are investigated. The fault location in dc transmission line has impact on the rate of rise of current. Typically, inception of dc fault close to the converter station is the most severe line fault conditions. Therefore, in addition to a short circuit fault at the middle of L_{13}, a short circuit fault at one end of this line, which is attached to MMC 1 is studied. Henceforth, the mentioned faults will be referred as the midpoint and endpoint faults in this chapter. The studied dc fault is a low impedance (100 mΩ) permanent fault.

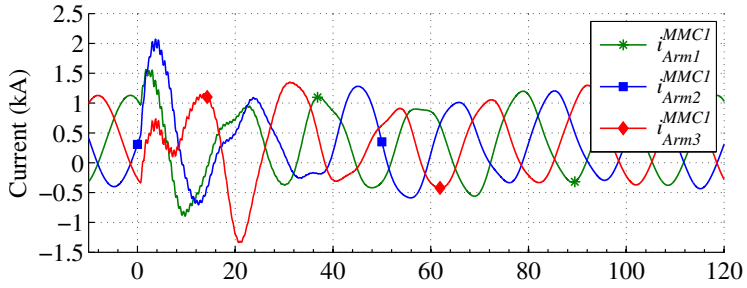
Firstly, the protection of meshed dc grid is tested without placing any SFCL. To meet the protection requirements of the grid and to prevent the MMCs from self-blocking during an endpoint fault a 100 mH current limiting inductor is necessary to be employed at each HCB. In both fault scenarios, a pole-to-pole fault is incepted at $t = 0.7$ s. Consequently, the protection relay model generates the trip command after the required time delay (t_d). The SFCL transition time is assumed to be 1 ms and its critical current is 3 kA. Also, minimum impedance of the SFCL is assumed as 1 mΩ. The system is investigated for different values of the SFCL maximum resistance. Due to the system symmetry only positive currents are presented.

5.4.1 System Without Superconducting Fault Current Limiter

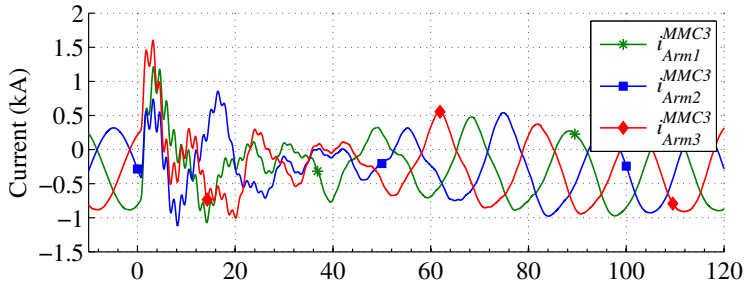
Figures 5.10, 5.11 shows the current and energy waveforms for the midpoint fault. The arm currents for both MMC 1 and MMC 3 are depicted in Figure 5.10(a) and (b). The converter dc side currents are shown in Figure 5.10(c). As can be seen, after the fault identification delay, CB_{13} and CB_{31} are tripped and opened. The converters are stressed by high fault current. Particularly, since the fault and pre-fault currents of the MMC 1 are in the same directions, it is more stressed. The current of MMC 1 reaches more than 4 kA, which is almost four times of its nominal current.

It can be seen from Figure 5.10(a) and (b), the arm currents of MMCs are less than the self-blocking level and the converters still operates within their safe operation area. Figure 5.10(d) presents the absorbed energy in the circuit breaker surge arresters. The surge arresters of CB_{13} and CB_{31} absorb 6.2 and 3.1 MJ, respectively. Since the fault and the pre-fault currents of CB13 are in the same directions, this circuit breaker needs to interrupt higher current than CB_{31}. Therefore, the surge arrester of CB_{13} absorbs more energy than that of CB_{31}.

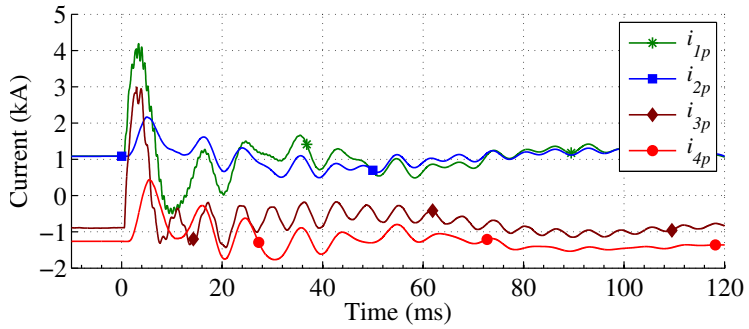
The current and energy waveforms for an endpoint fault in L_{13} is shown in Figures 5.12 and 5.13. Due to the closer distance of fault to the MMC 1, its arm and dc side currents reach higher values. It is clear that the presence of the current limiting inductor limits the



(a) Arm currents of MMC 1



(b) Arm currents of MMC 3



(c) dc side positive pole current of MMC 1

Figure 5.10: The MMCs arm currents during a midpoint fault on transmission line L_{13} without SFCL.

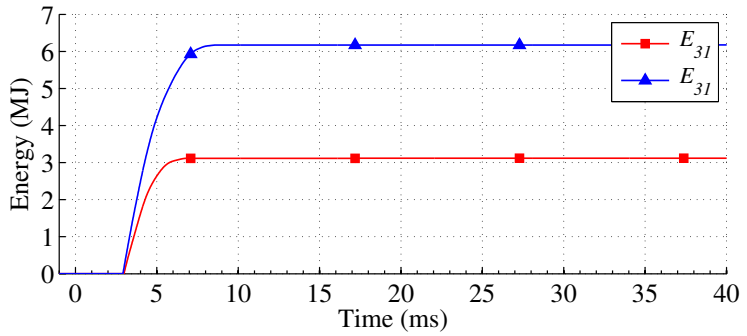


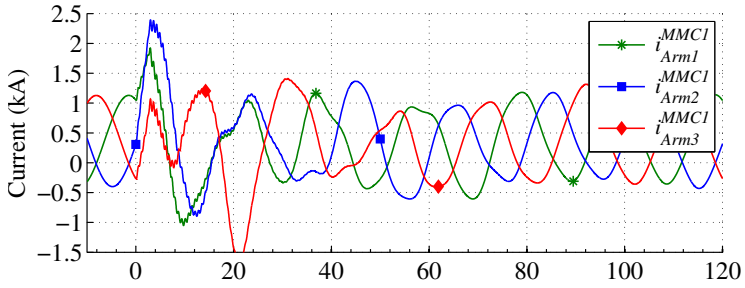
Figure 5.11: Absorbed energy in the surge arresters of corresponding dcCBs during a midpoint fault on transmission line L_{13} without SFCL.

current derivative and prevent the converters from blocking. The amounts of absorbed energy by surge arresters of CB_{13} and CB_{31} are 8.2 and 2.5 MJ, respectively.

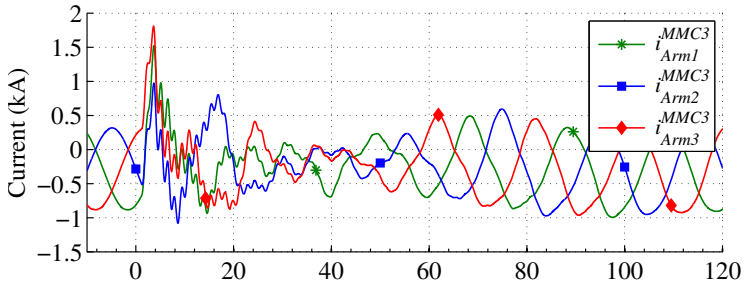
5.4.2 *System With Superconducting Fault Current Limiter*

The fault current analysis, verified by simulation, when the SFCL is placed between each HCB and the dc bus terminal is presented in this subsection. Figures 5.14(a)-(b), 5.16(a)-(b) and 5.18(a)-(b) depict CB_{13} and CB_{31} midpoint fault current waveforms for three line inductor

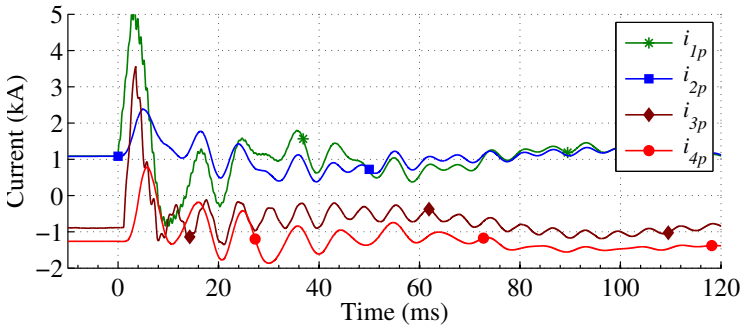
Figure 5.12: The MMCs arm currents during an endpoint fault on transmission line L_{13} without SFCL.



(a) Arm currents of MMC 1

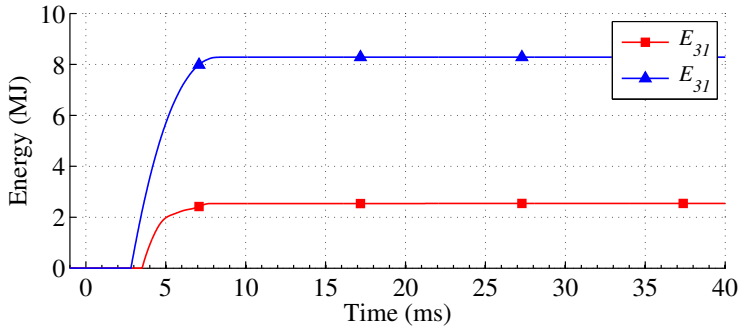


(b) Arm currents of MMC 3



(c) dc side positive pole current of MMC 1

Figure 5.13: Absorbed energy in the surge arresters of corresponding dcCBs during an endpoint fault on transmission line L_{13} without SFCL.



values and four maximum impedance values. CB_{13} and CB_{31} currents in the system without SFCL and with a current limiting inductor of 100 mH is shown in thick green line with the legend of 0 Ω. The presence of SFCL changes the current waveform.

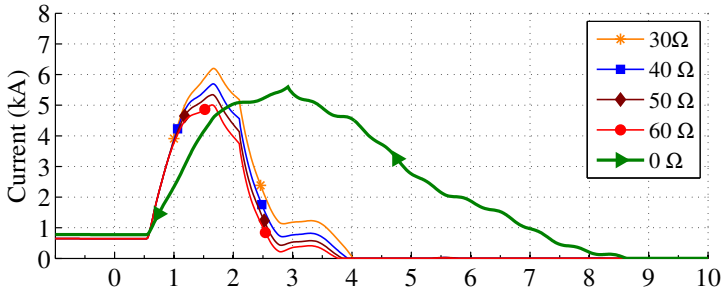
The impact of nonlinear behavior of the SFCL on the fault current before interruption can be seen from Figures 5.14(a) and (b). Two aforementioned stages of the fault current can be noticed from the mentioned figures. The initial rate of rise of current is higher than the normal case due to the lower inductance of system. In the second stage of the current waveform the SFCL is triggered and its impedance

rises exponentially and may reduce the rate of rise of fault current and its peak. For instance, for L_{cb}=40 mH and R_{max}=60 Ω in Figure 5.14(a), the peak of CB_{13} current can effectively be limited to less than 5 kA, which is almost 15% less than the SFCL-less case. Figure 5.14 also shows that by decreasing the value of line inductance value the fault current peak substantially increases for the lower SFCL impedance values.

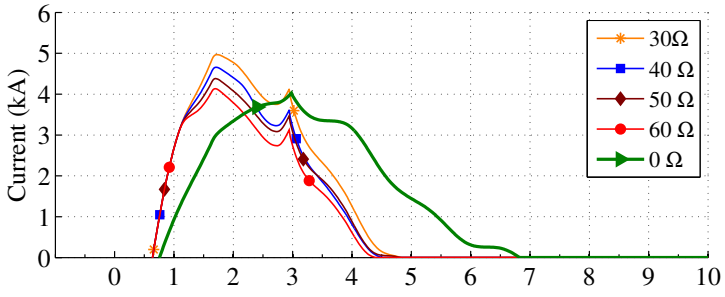
In contrast, for higher impedance values even with lower current limiting inductor values (for example, R_{max}=60 Ω, L_{cb}=10 mH in Figure 5.18) the currents of both CB_{13} and CB_{31} for the midpoint fault are still limited. The absorbed energy in surge arresters of the circuit breakers are also shown in Figures 5.14(c), 5.16(c) and 5.18(c). The absorbed energy in the surge arresters is dramatically reduced. The reduction in energy absorption is because of smaller current limiting inductance and also lower fault current at the interruption instant. Figures 5.15, 5.17 and 5.19 show the converter currents for the midpoint line fault. For R_{max}=30 and 40 Ω and L_{cb}=10 mH the converter currents become closer to the self-blocking conditions.

Figures 5.20(a)-(b), 5.22(a)-(b) and 5.24(a)-(b) shows the circuit breaker current for the endpoint fault. Considering the lowest current limiting inductor value (L_{cb}=10 mH) from the Figures 5.24(a)-(b), the maximum impedances more than 40 Ω allows effective fault current limiting in both dcCBs. Note that the endpoint fault is very close to CB_{13}. Hence, due to lower line inductance between the circuit breaker and the fault point, higher current peak can be seen in CB_{13}. The surge arrester energy waveforms are shown in Figures 5.20(c), 5.22(c) and 5.24(c). The absorbed energy in the surge arresters is notably decreased. It can also be seen from the Figures 5.21, 5.23 and 5.25 that the converters are not blocked.

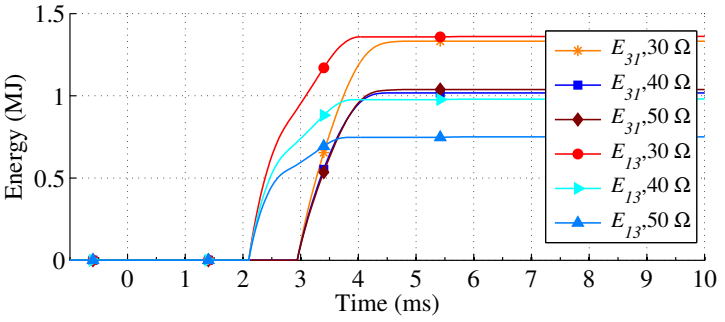
Figure 5.14: Circuit breaker current and the surge arrester absorbed energy for a midpoint fault on transmission line L_{13} for $L_{cb} = 40$ mH.



(a) The current in CB_{13}

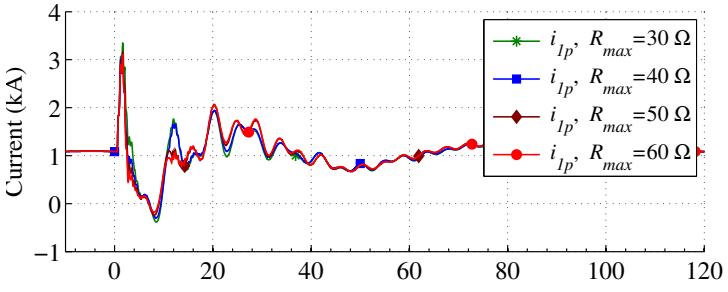


(b) The current in CB_{31}

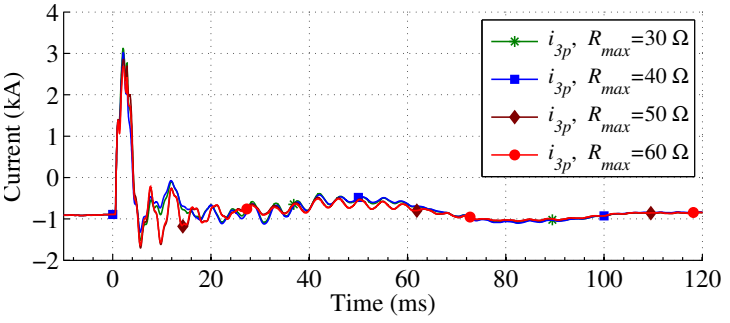


(c) The absorbed energy in the surge arresters

Figure 5.15: Converter dc side current for a midpoint fault on transmission line L_{13} for $L_{cb} = 40$ mH.

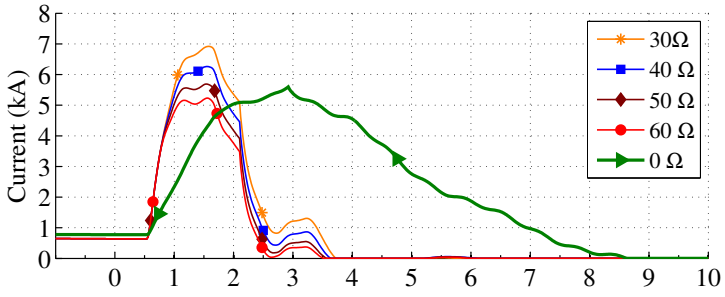


(a) dc side positive pole current of MMC 1

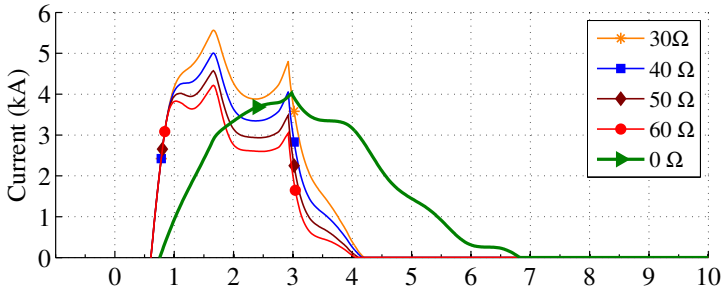


(b) dc side positive pole current of MMC 3

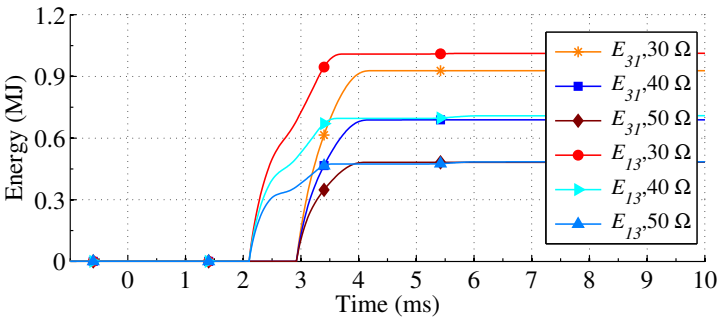
Figure 5.16: Circuit breaker current and the surge arrester absorbed energy for a midpoint fault on transmission line L_{13} for $L_{cb} = 20$ mH.



(a) The current in CB_{13}

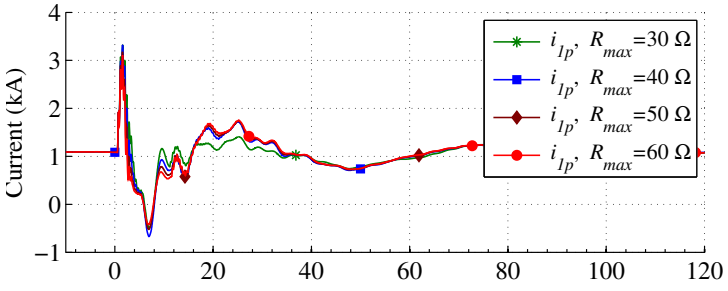


(b) The current in CB_{31}

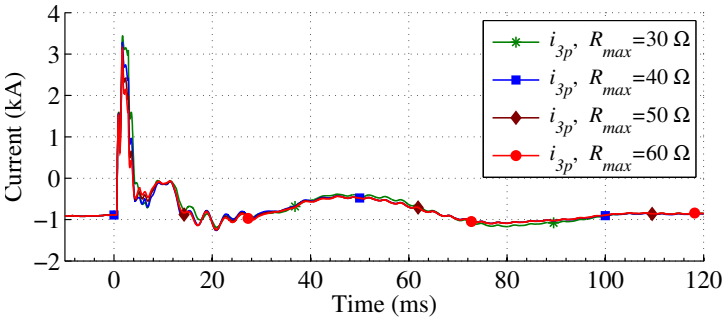


(c) The absorbed energy in the surge arresters

Figure 5.17: Converter dc side current for a midpoint fault on transmission line L_{13} for $L_{cb} = 20$ mH.

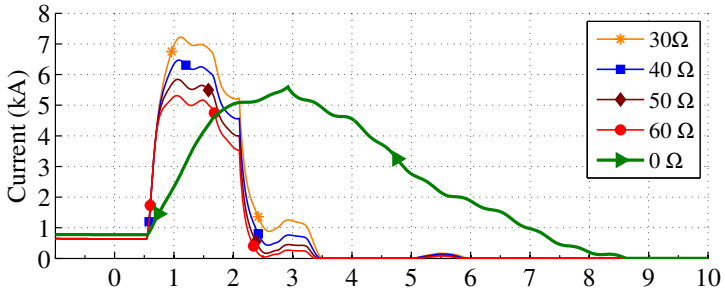


(a) dc side positive pole current of MMC 1

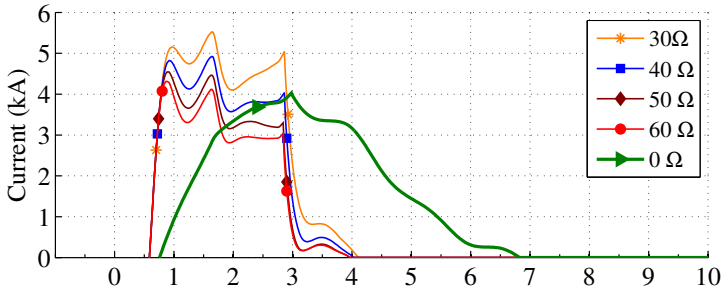


(b) dc side positive pole current of MMC 3

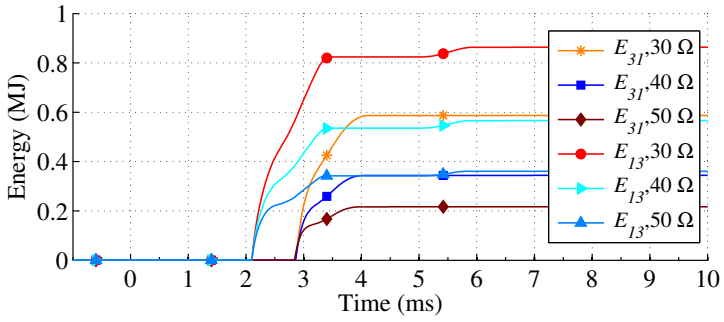
Figure 5.18: Circuit breaker current and the surge arrester absorbed energy for a midpoint fault on transmission line L_{13} for $L_{cb} = 10$ mH.



(a) The current in CB_{13}

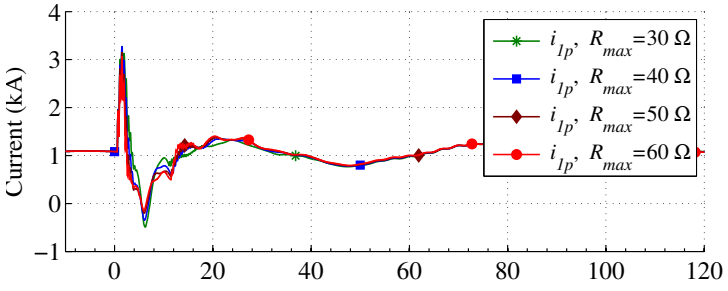


(b) The current in CB_{31}

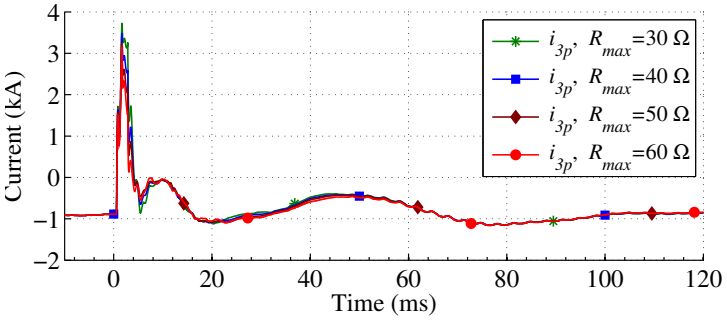


(c) The absorbed energy in the surge arresters

Figure 5.19: Converter dc side current for a midpoint fault on transmission line L_{13} for $L_{cb} = 10$ mH.

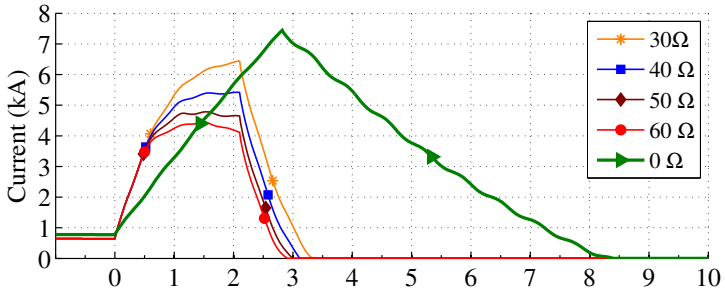


(a) dc side positive pole current of MMC 1

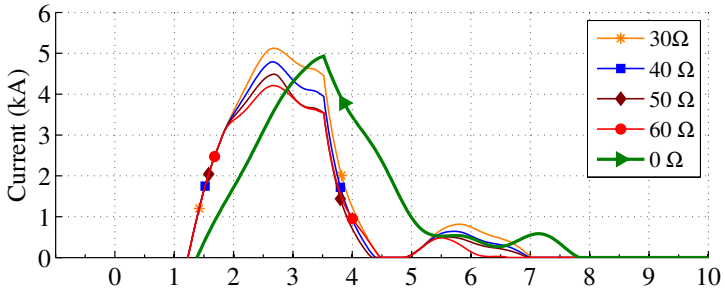


(b) dc side positive pole current of MMC 3

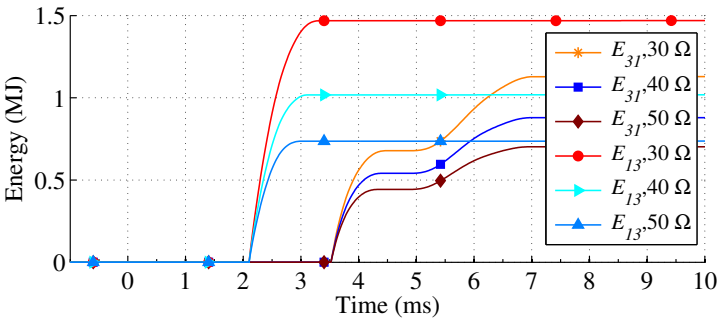
Figure 5.20: Circuit breaker current and the surge arrester absorbed energy for an endpoint fault on transmission line L_{13} for $L_{cb} = 40$ mH.



(a) The current in CB_{13}

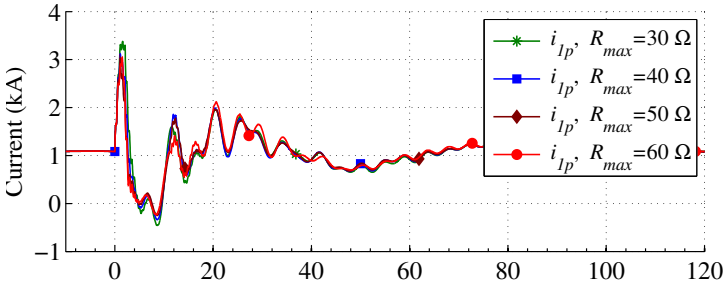


(b) The current in CB_{31}

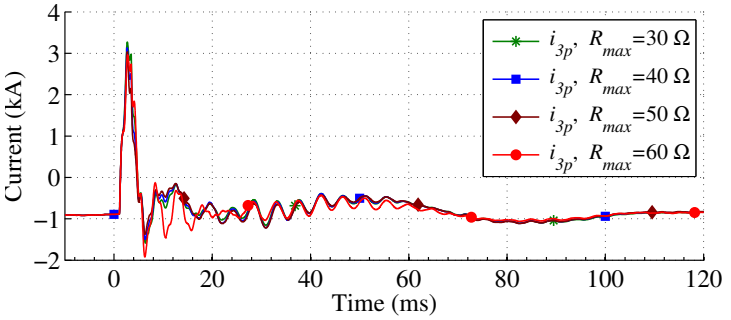


(c) The absorbed energy in the surge arresters

Figure 5.21: Converter dc side current for an endpoint fault on transmission line L_{13} for $L_{cb} = 40$ mH.

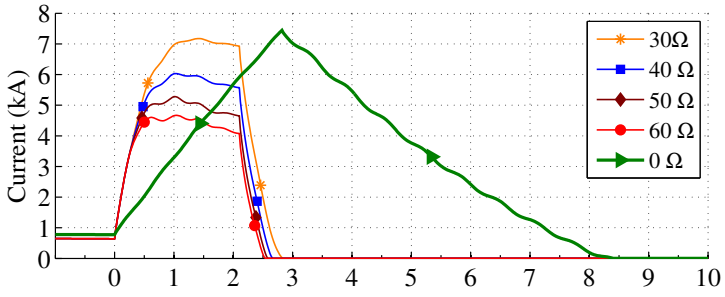


(a) dc side positive pole current of MMC 1

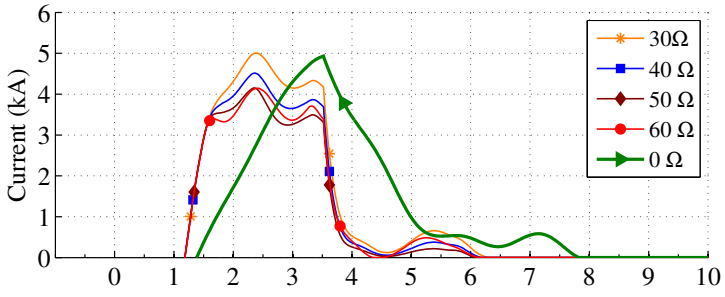


(b) dc side positive pole current of MMC 3

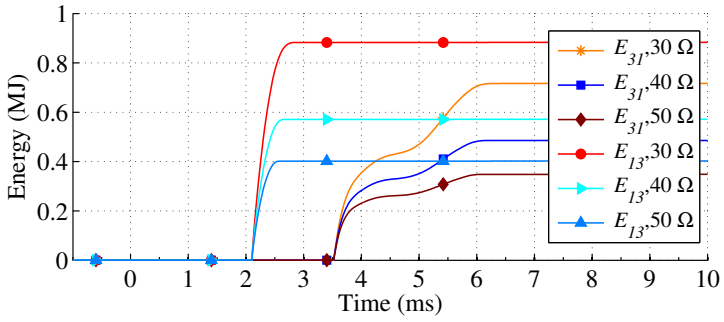
Figure 5.22: Circuit breaker current and the surge arrester absorbed energy for an endpoint fault on transmission line L_{13} for $L_{cb} = 20$ mH.



(a) The current in CB_{13}

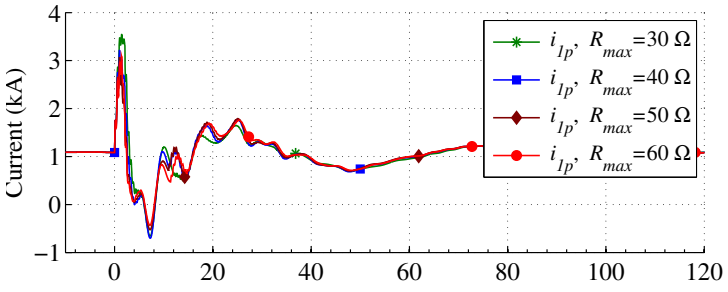


(b) The current in CB_{31}

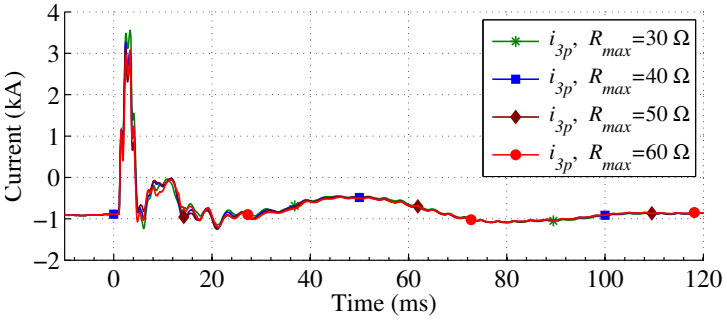


(c) The absorbed energy in the surge arresters

Figure 5.23: Converter dc side current for an endpoint fault on transmission line L_{13} for $L_{cb} = 20$ mH.

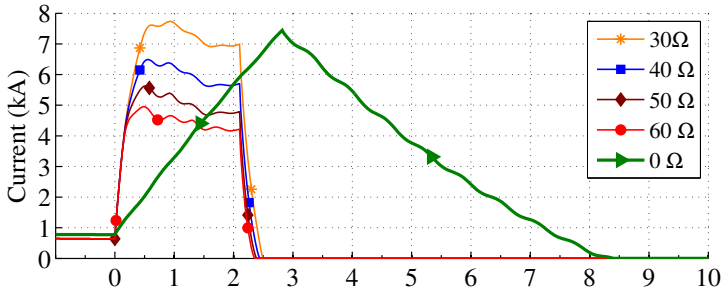


(a) dc side positive pole current of MMC 1

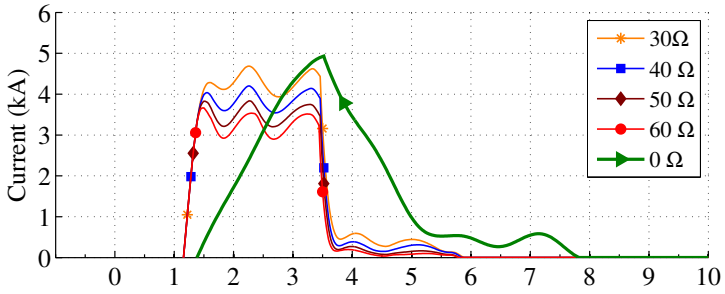


(b) dc side positive pole current of MMC 3

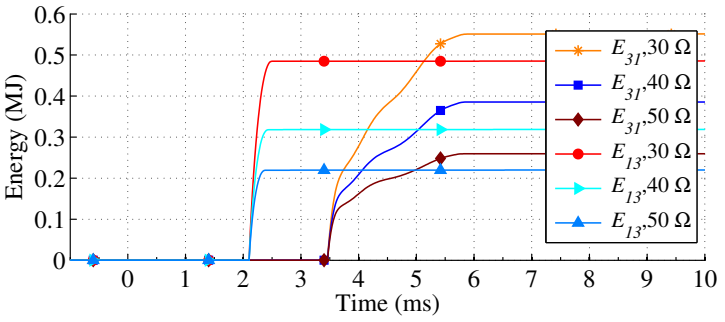
Figure 5.24: Circuit breaker current and the surge arrester absorbed energy for an endpoint fault on transmission line L_{13} for $L_{cb} = 10$ mH.



(a) The current in CB_{13}

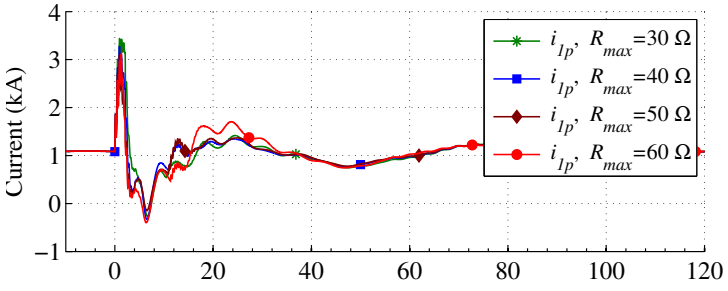


(b) The current in CB_{31}

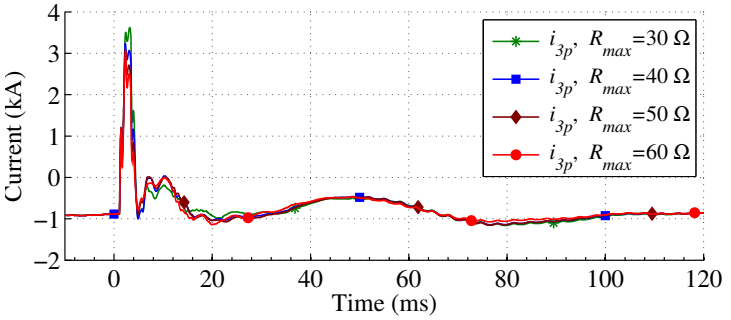


(c) The absorbed energy in the surge arresters

Figure 5.25: Converter dc side current for an endpoint fault on transmission line L_{13} for $L_{cb} = 10$ mH.



(a) dc side positive pole current of MMC 1



(b) dc side positive pole current of MMC 3

5.5 Remarks on Application

The results from the case studies confirm that the SFCL can decrease the fault current peak in presence of fast protection relays and the hybrid circuit breakers. Although the SFCL decreases the requirement for the current limiting inductor, it cannot eliminate the need for it. Reducing the size of limiting inductors more than specific value for a system may activate the converter self-protection system and block the MMC's IGBTs, which is not desirable. Additionally, the line inductors are also needed to form the borders between different protection zones in fast protection schemes for meshed dc grids. On the other hand, to limit the fault current peak with the lower line inductances, higher SFCL impedances are required. Therefore, the optimized parameters of the circuit breaker can be selected due to the trade-off between the current limiting inductor size and the maximum impedance of the SFCL. Application of the SFCL in HCB can reduce the energy rating of surge arresters, remarkably. The fault current peak can also be limited by suitable SFCLs and decrease the current ratings of the hybrid circuit breakers. The reduction in value of the current limiting inductor does not violate the harmonic requirements of system as the value of current smoothing reactors (10 mH) has not been changed. Table 5.1 shows a comparison between the parameters of systems with and without SFCL. Note that the data in Table 1 is derived for L_L=20 mH and R_{max}=60 Ω. The improvement of each parameter after applying the SFCL is also illustrated in percentage and SA_{mn} represents the surge arrester of CB_{mn}.

Table 5.1: Comparative results according the SFCL application.

Parameter	Midpoint fault			Endpoint fault		
	No FCL	**With FCL**	**Imp.***	**No FCL**	**With FCL**	**Imp.***
Total L (mH)	100	20	80%	100	20	80%
T_{id}, $Relay_{13}$ (ms)	0.9	0.8	11%	0.6	0.5	16%
T_{id}, $Relay_{31}$ (ms)	0.95	0.85	10%	2	1.52	24%
CB_{13} Current (kA)	5.78	5.09	12%	7.34	4.65	37%
CB_{31} Current (kA)	4.92	4.1	16%	4.92	4.13	16%
SA_{13} Energy (MJ)	6.2	0.35	94%	8.4	0.31	96%
SA_{31} Energy (MJ)	3.1	0.35	88%	2.5	0.47	81%

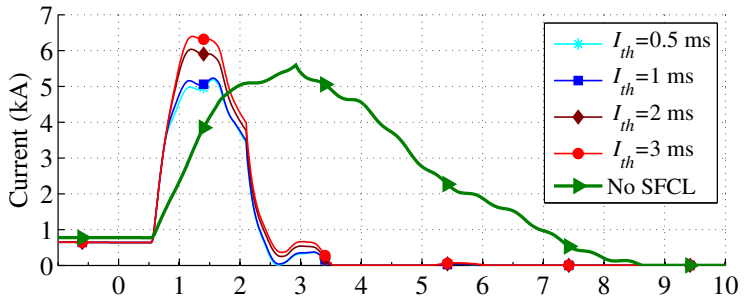
* Imp. :Improvement percentage

5.6 *Sensitivity Analysis*

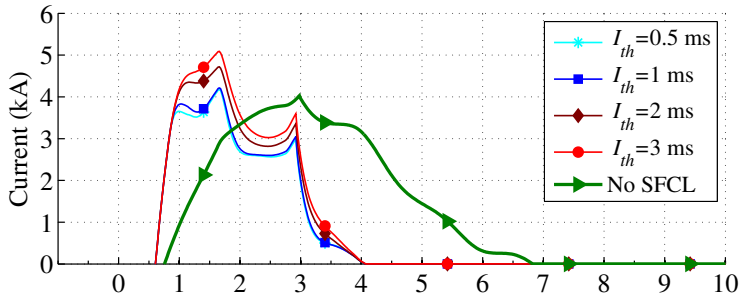
Impact of two parameters on the system performance are studied in this subsection. Considering the results from previous section, the maximum impedance and current limiting inductor values are set to 60 Ω and 20 mH, respectively.

5.6.1 *Superconducting Fault Current Limiter Transition Time*

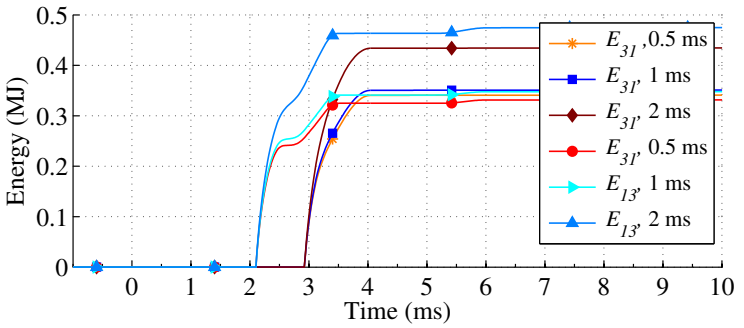
Figure 5.26(a) and (b) shows CB_{13} and CB_{31} while the transition time of SFCL varies between 0.5 and 3 ms. As it is expected the faster SFCLs can limit the fault current better than the slower ones. Increasing the transition time leads to higher peak in the fault current. The surge arrester waveforms are depicted in Figure 5.2616(c). Due to the higher current of slower SFCLs, the discharged energy in surge arrester is higher in comparison to the system with faster SFCLs.



(a) The current in CB_{13}



(b) The current in CB_{31}

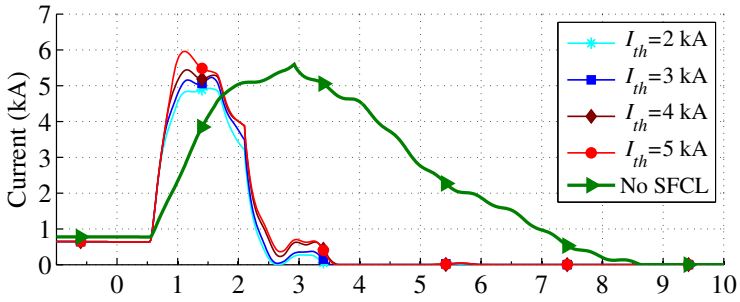


(c) Absorbed energy in the surge arresters of corresponding circuit breakers

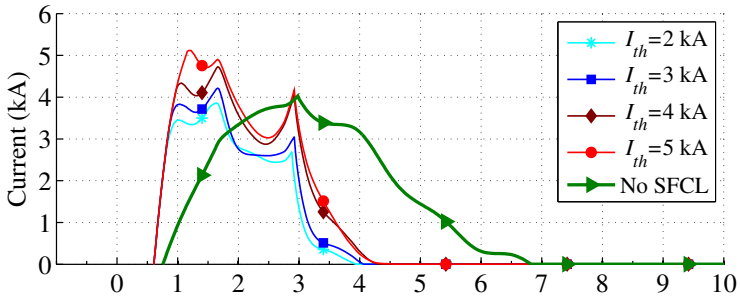
Figure 5.26: Circuit breakers current and absorbed energy waveforms for different transition times of SFCL.

5.6.2 *Superconducting Fault Current Limiter Critical Current*

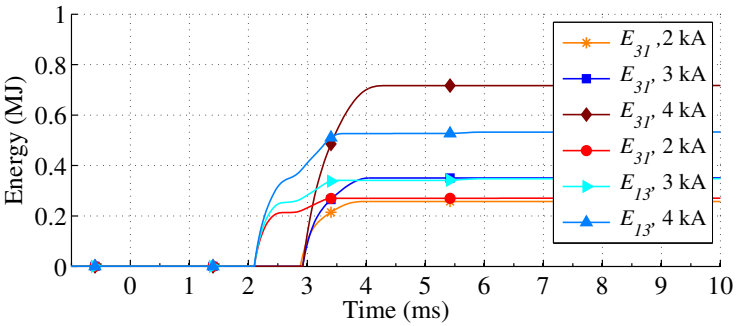
The circuit breakers currents for different values of the critical current of SFCL between 2 and 5 kA are shown in Figure 5.27(a) and (b). Decreasing the critical current of the SFCL causes reduction in peak of the fault current. Note that the lower critical currents of the SFCL may influence the fast relaying scheme and prevent the relay from fault discrimination. Hence, depending on the operation principles of fast protective relays, specific limitations should be defined. On the other hand, the protective relays can be adjusted considering the lower critical current of the SFCLs. The absorbed energy waveforms for different critical currents are shown in Figure 5.27(c). The lower triggering currents lead to lower energy absorption in surge arresters.



(a) The current in CB_{13}



(b) The current in CB_{31}



(c) Absorbed energy in the surge arresters of corresponding circuit breakers

Figure 5.27: Circuit breakers current and absorbed energy waveforms for different critical currents of SFCL.

5.7 Conclusion

The application of superconducting fault current limiters in the meshed HVdc grids considering the fast protection schemes is investigated in this chapter. Due to the nonlinear impedance characteristic of SFCL and depending on its transition time and also fault interruption delay, the current may reach higher values than SFCL limiting current, which is not desirable. Therefore, suitable SFCL have to be designed in coordination with the rate of rise of current, fault identification delay and steady-state fault current.

The system analysis implies that the successful fault current limiting in presence of fast protective relaying schemes and fast dc circuit breakers can be done when the maximum impedance of the SFCL is high enough to limit the fault current below the normal interruption current. Additionally, the transition time has to be shorter than fault current interruption delay to avoid any unwanted current peak during quenching process. In addition to reduction in fault current peak after applying the SFCL, the size of the current limiting inductor can also be decreased. The study shows that in spite of lower inductance of system, the MMCs operates without self-blocking even during the line endpoint faults. The lower fault current peak can reduce the current requirements of the main breaker unit of the HCB. The lower inductance and lower interrupted current values reduce the stored energy of the system. The results of this study show significant reduction in absorbed energy in the surge arresters of HCBs. Hence, the size of circuit breaker surge arrester will be remarkably smaller than the standard case. Moreover, due to the lower inductance of system, the traveling wave based fast protective relaying schemes identify the dc fault faster in presence of SFCL.

Impacts of transition time and critical current are also discussed through the sensitivity analysis. It is confirmed that decreasing the transition time of SFCL is always advantageous while the critical current of the SFCL should not be reduced more than specific values due to its influence on fast fault detection schemes. The results from present research work highlights that, the SFCLs, which meet the transition time, critical current and maximum impedance requirements can significantly improves the fast protection system performance, independently of their technology.

Part IV

Multi-port HVdc Circuit Breakers

6
Multi-port Hybrid dc Circuit Breaker

Mokhberdoran, A.; Van Hertem, D.; Silva, N. ; Leite, H., Carvalho, A., "Multi-port Hybrid HVdc Circuit Breaker", *IEEE Transaction on Industrial Electronics Journal*, Early Access, June 2017.

Only two things are infinite, the universe and human stupidity, and I'm not sure about the former.

Albert Einstein, Theoretical physicist, 1879-1955.

As discussed in chapter 2, the implementation cost of the HCBs for MT-HVdc applications is expected to be high. The HCB requires hundreds of semiconductor switches in its MB branch to tolerate the system and transient recovery voltage [162,220], hence its implementation cost is expected to be high. The number of required semiconductor switches for protection of a dc bus with two adjacent transmission lines would be comparable to that of an MMC station [162,221].

Several dcCB topologies have been introduced in the literature (see chapter 2) aiming to reduce the number of required components for realization of HCB and decreasing its implementation cost.

This chapter proposes a novel multi-port dc current interrupter device benefiting from the HCB core concept [138]. The proposed dcCB has n ports and can interrupt the current at each of its ports independent of other ports and irrespective of current direction. Therefore, it is called multi-port hybrid dc circuit breaker (Mp-HCB). The Mp-HCB requires fewer switches in the MB and also in the load commutation switch compared to the typical HCB. Furthermore, the size of surge arresters for energy absorption can be significantly decreased.

The topology of proposed Mp-HCB is presented in section 6.1 and its operation principles are detailed in section 6.2. The theoretic analysis is carried out in section 6.3. The performed analysis is validated through a simulation study using a three-terminal grid model in section 6.4. Moreover, the functionality of Mp-HCB is examined through simulation study of a detailed four-terminal MT-HVdc model with a state of the art protection scheme in section 6.4. A comparison between the HCB and the Mp-HCB has been carried out in section 6.5. Finally, the chapter is concluded in section 6.6.

6.1 Multi-port Hybrid dc Circuit Breaker

6.1.1 Basic Representation

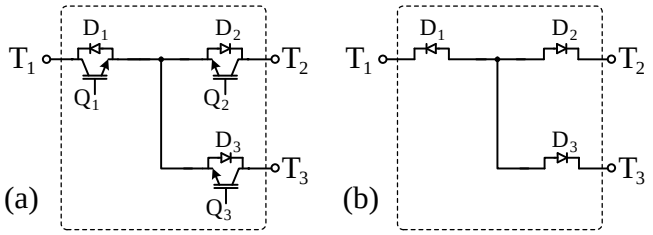


Figure 6.1: Basic block of Mp-HCB, (a) ON (close) state, (b) OFF (open) state.

The basic representation for a 3-port switch consists of three IGBTs with antiparallel diodes is shown in Figure 6.1(a). Although several states exist for the 3-port switch based on the states of IGBTs, only a couple of them are utilized for developing the proposed Mp-HCB. The first state of 3-port switch is the ON (close) state. In this state all the IGBTs are turned on and the 3-port switch has no impact on the current flow between the terminals (T_1-T_3). The second state of 3-port switch is the OFF (open) state and can be achieved by turning off all the IGBTs. As shown in Figure 6.1(b), due to the arrangement of D_1-D_3, all the terminals are disconnected from each other in open state. The 3-port switch concept can be generalized to an *n*-port switch.

6.1.2 Mp-HCB Topology

The topology of proposed Mp-HCB with *n* ports is depicted in Figure 6.2.

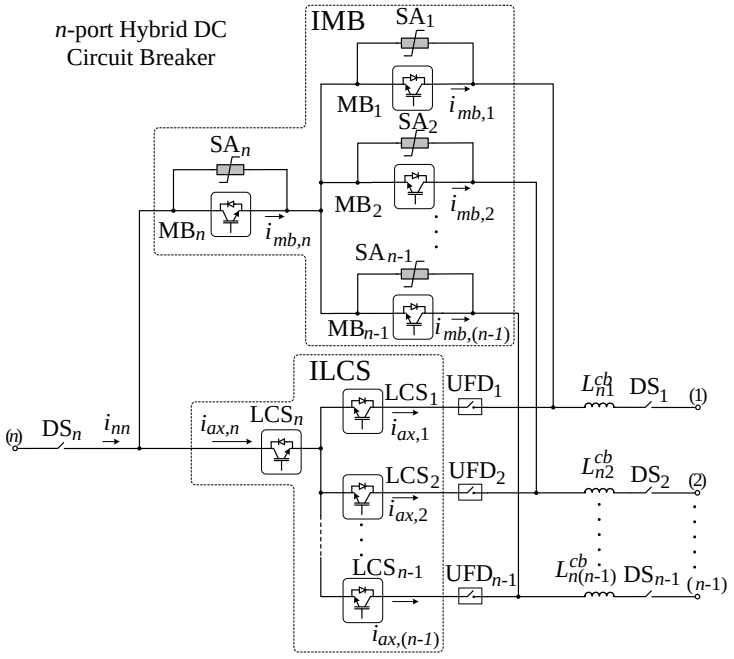
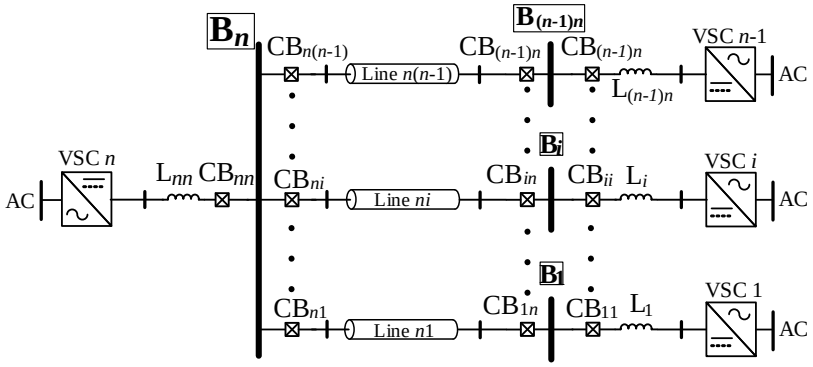


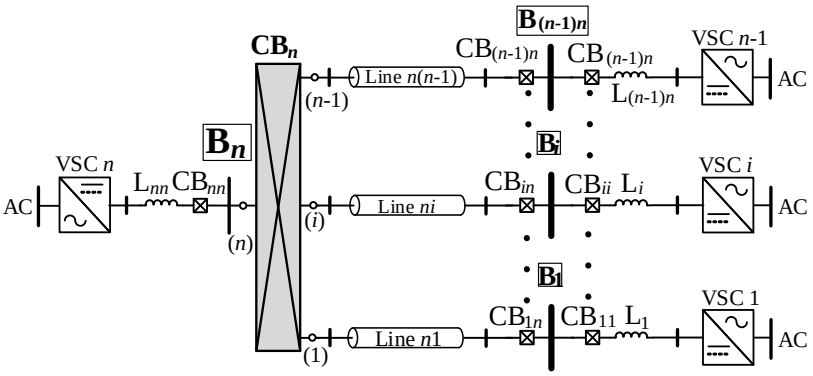
Figure 6.2: *n*-port hybrid dc circuit breaker topology.

The Mp-HCB is composed of an integrated main breaker (IMB), an

integrated load commutation switch (ILSC), ultra-fast disconnectors (UFD_i), current limiting inductors (L_i^{cb}), surge arresters (SA_i) and disconnectors (DS_i). Port n is assumed to be connected to a dc bus and ports 1 to $n-1$ are assumed to be connected to $n-1$ adjacent transmission lines. Figure 6.3(a) shows an n-terminal dc system protected by the HCBs. As shown in the figure, the HCBs are placed at ends of all transmission lines to achieve full protection selectivity. Although the number of dcCBs might be reduced based on the grid requirements, a fully protected grid is considered in this study [184]. Figure 6.3(b) depicts similar system when $n-1$ HCBs at dc bus n (B_n) are replaced by an n-port Mp-HCB. The SAs, UFDs and DSs are similar to the typical ones used in the HCBs [138].



(a) Multi-terminal dc grid protected by hybrid dc circuit breakers



(b) Multi-terminal dc grid protected by multi-port hybrid dc circuit breaker

Figure 6.3: Multi-terminal dc grid protected by hybrid dc circuit breakers and the proposed multi-port hybrid dc circuit breaker.

The Mp-HCB has two new integrated modules:

Integrated Main Breaker Unit (IMB)

As shown in Figure 6.2, the IMB unit consists of n MB subunits. The MB subunits consist of series connected IGBTs. Contrary to the MB unit of typical HCB, the MB subunits of Mp-HCB are not bidirectional switches. The unidirectional MB subunits are integrated together to form a multidirectional IMB unit. Similar to the n-port switch basic representation, the IMB has two states (ON and OFF) depending on the states of MB subunits.

Integrated Load Commutation Switch (ILCS)

The ILCS consists of n LCS subunits. The ILCS is in the ON state when all the LCS subunits are closed and is in the OFF state when the LCS subunits are opened. The LCS subunit can be realized by one IGBT or series connection of few IGBTs similar to the LCS of typical HCB due to reduced voltage requirements [138].

6.2 Operation Principles

The Mp-HCB operation principles can be separated in three modes: normal conduction, current interruption and reclosing.

6.2.1 Normal Conduction Mode

In the normal conduction mode, the ILCS together with the UFD_1 to UFD_{n-1} and DS_1 to DS_n are closed whereas the IMB is in the open state. The equivalent circuit of Mp-HCB in this mode is similar to Figure 6.4(a). Therefore, the power flow can be maintained between the dc bus and adjacent lines irrespective of its direction.

6.2.2 Fault Current Interruption Mode

The Mp-HCB can receive n independent trip commands. Upon receiving a trip command from a line or bus protection relay, the corresponding port(s) of Mp-HCB must interrupt(s) its(their) current(s).

6.2.3 Fault on Adjacent Transmission Line i (Port i)

Line i is connected to port i of the Mp-HCB where $i = 1, 2, ..., n-1$. Hence, to clear a permanent fault on line i, port i of the Mp-HCB should trip. It is assumed that the fault incepts at $t = 0$ s and the trip command for port i is received at time $t = t_{ax}$. Figure 6.4(a) depicts the equivalent circuit of Mp-HCB for $0 < t \leq t_{ax}$. The fault current flows through the ILCS during this time period. Upon receiving the trip command, the IMB is closed and then the ILCS is opened in order to commutate the currents into the IMB. Due to the fast turn-on and turn-off of IGBTs, the current commutation time is expected to be in the range of few tens of micro-seconds [139]. The rate of rise of current would slightly be reduced after current commutation is done due to the larger number of IGBTs in the IMB and its higher stray inductance compared to the ILCS. However, the variation is negligible and has no remarkable impact on the fault current. In order to ease the explanation of Mp-HCB operation, the current commutation is assumed to be done instantaneously.
After completion of the current commutation at t_{ax}, UFD_i should be opened. During UFD_i operation delay, the fault current flows through the MB subunits. Figure 6.4(b) shows the equivalent circuit for this stage. UFD_i operation is assumed to be accomplished at time t'_{ax} and thereafter the ILCS should be closed. This stage of the Mp-HCB

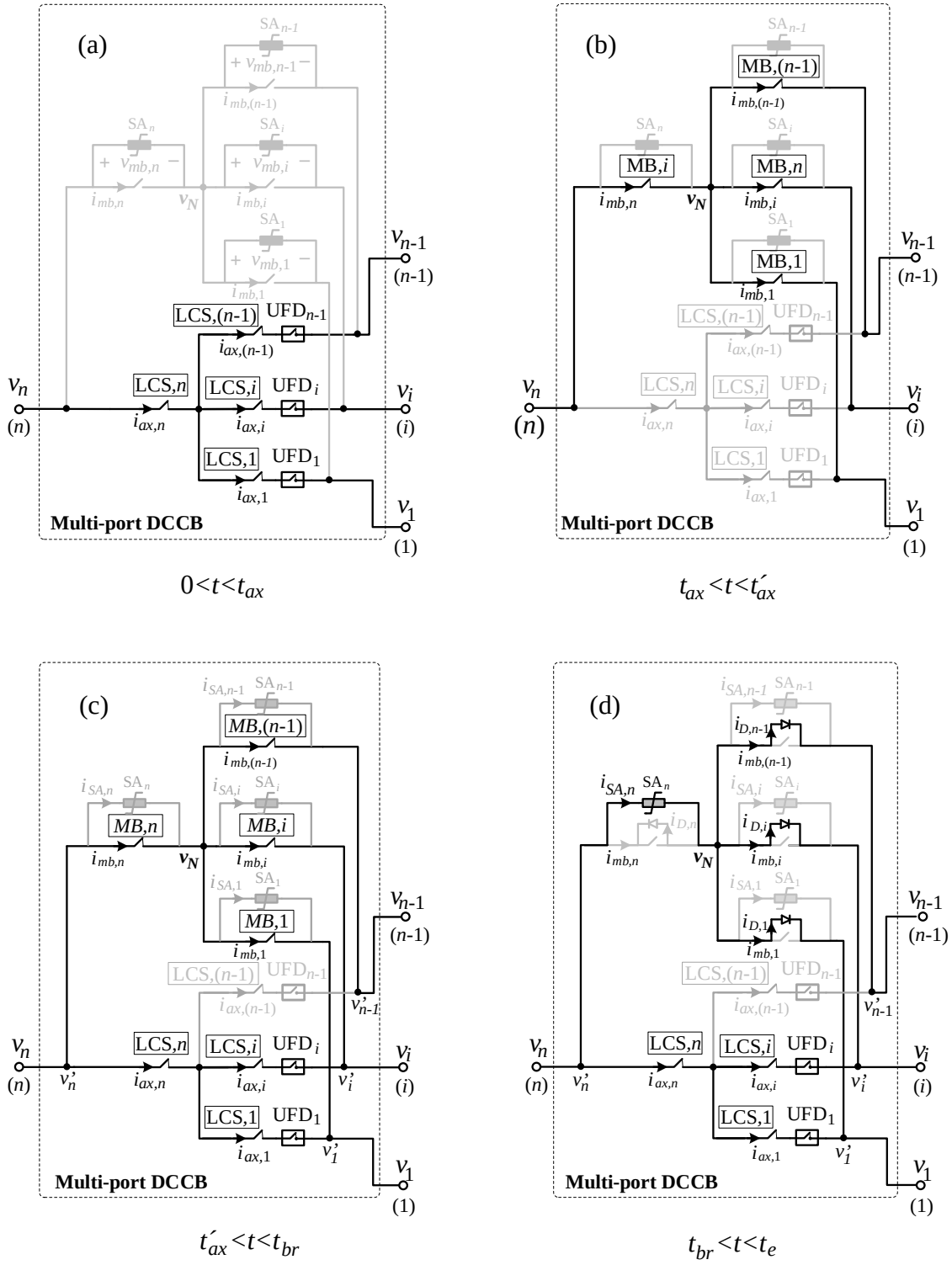
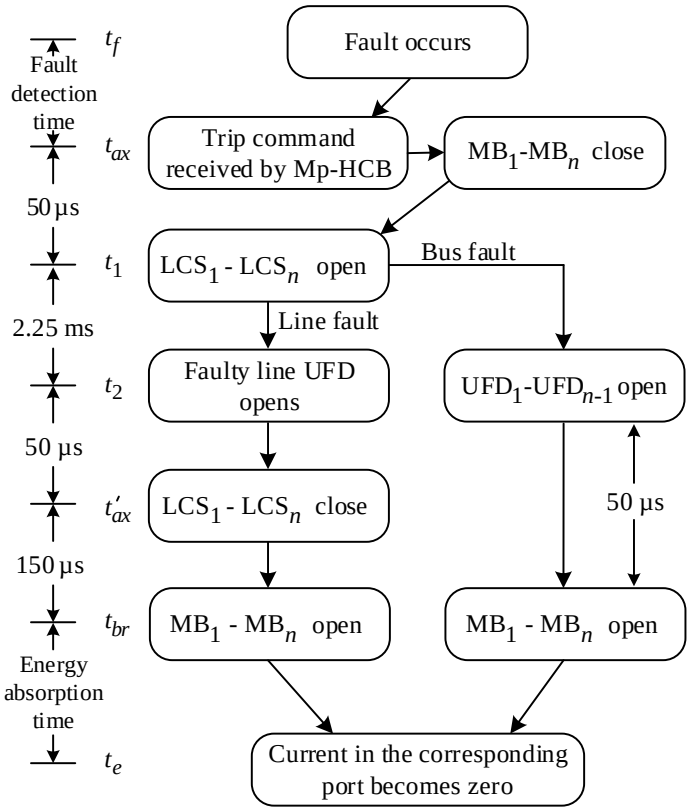


Figure 6.4: Operation stages of multi-port hybrid dc circuit breaker.

operation is depicted in Figure 6.4(c). When the ILCS is closed in this stage, some of the MB subunits share their current with some of the LCS subunits. This stage is named as current sharing stage. Although the ILCS is closed, the current cannot flow through LCS_i

Figure 6.5: Line and bus faults isolation process.



into the port i due to the open state of UFD_i. Nevertheless, the fault current can still flow into the faulty line via MB_i. Considering a fast fault current interruption strategy, after closing the ILCS, the IMB unit should be opened to interrupt the fault current. After opening the IMB at $t = t_{br}$, the currents of healthy lines can flow though the corresponding LCS subunits whereas the fault current is commutated into the surge arresters in the IMB unit as shown in Figure 6.4(d). Finally, the released energy is absorbed in SA_1 to SA_n by $t = t_e$. Note that due to the antiparallel diodes of MB_i the current cannot be redirected into SA_i. To provide electrical isolation DS_i can be opened. Figure 6.5 illustrates the line fault isolation process and related timings.

6.2.4 *Fault at dc Bus (port n)*

Upon detection of a permanent dc bus fault, all adjacent lines must be isolated from the dc bus. Therefore, after receiving dc bus fault trip command the IMB should be closed and the ILCS should be opened to commutate the current into the IMB (at $t = t_{ax}$). Following the current commutation completion, UFD_1 to UFD_{n-1} can be opened. Finally, the IMB should be opened (at $t = t_{br}$) and the currents will be redirected into the SAs. The electrical isolation can be provided by opening DS_n. The sequential bus fault interruption process is shown in Figure 6.5.

6.2.5 Recloser Mode

The reclosing mode might be required before completely opening of the Mp-HCB. The Mp-HCB can be reclosed by reclosing the IMB after opening the UFD_i. The equivalent circuits of reclosing mode are equal to Figure 6.4(c) and (d). Finally, in case of a non-permanent fault, the UFD_i can again be closed and the Mp-HCB shifts to its normal conduction state by closing the ILCS and opening the IMB.

6.3 Analysis

The internal operation of Mp-HCB is analyzed through the simplified model of dc system depicted in Figure 6.3. The analyzed network is an n-terminal grid where dc buses B_1 to B_{n-1} are connected through $n-1$ transmission lines to dc bus B_n. It is clear that the Mp-HCB operation does not depend on the grid topology. Although more complex networks could have been considered, it was found to be unnecessary considering the scope of chapter. In order to compare the proposed approach with the typical HCB, similar analysis has been carried out for the system based on the typical HCBs. To perform the analysis, the following aspects are considered:

- Simple (RL-equivalent) model of the transmission line is used in order to clarify the internal operation of the Mp-HCB and avoid variation in rate of rise of fault current.
- Detailed models of HCB [139] and Mp-HCB are used and the current limiting inductor is considered as a part of dcCB.
- The permanent dc fault and prompt fault interruption strategy are considered [184].
- Voltage at dc buses are assumed to be constant during the dcCB operation time [222].
- Transmission line and dc bus short circuit faults are modeled by a voltage source, whose value is equal to the system steady-state voltage value in normal conduction and it changes to 0 V as soon as a fault happens.

6.3.1 Transmission Line Fault F_1 and Mp-HCB

The equivalent circuit is depicted in Figure 6.6. A low impedance ($R_{fault} \approx 0\ \Omega$) pole-to-ground fault occurs on line $n-1$ at point F_1 at $t = 0$ s. The voltage at fault location (v_{F1}) becomes zero after fault occurs. The following equations can be given considering the initial conditions and assumptions:

$$\begin{aligned} &v_{F1}(0) = V_{dc}, \\ &v_{F1}\left(0^+\right) = 0, \\ &v_j(t) = V_{dc}; \quad 0 < t \leq t_{br}, \quad j = 1, ..., n, \\ &i_{cb,j}(0) = I_{pre,j}; \quad j = 1, ..., n. \end{aligned} \tag{6.1}$$

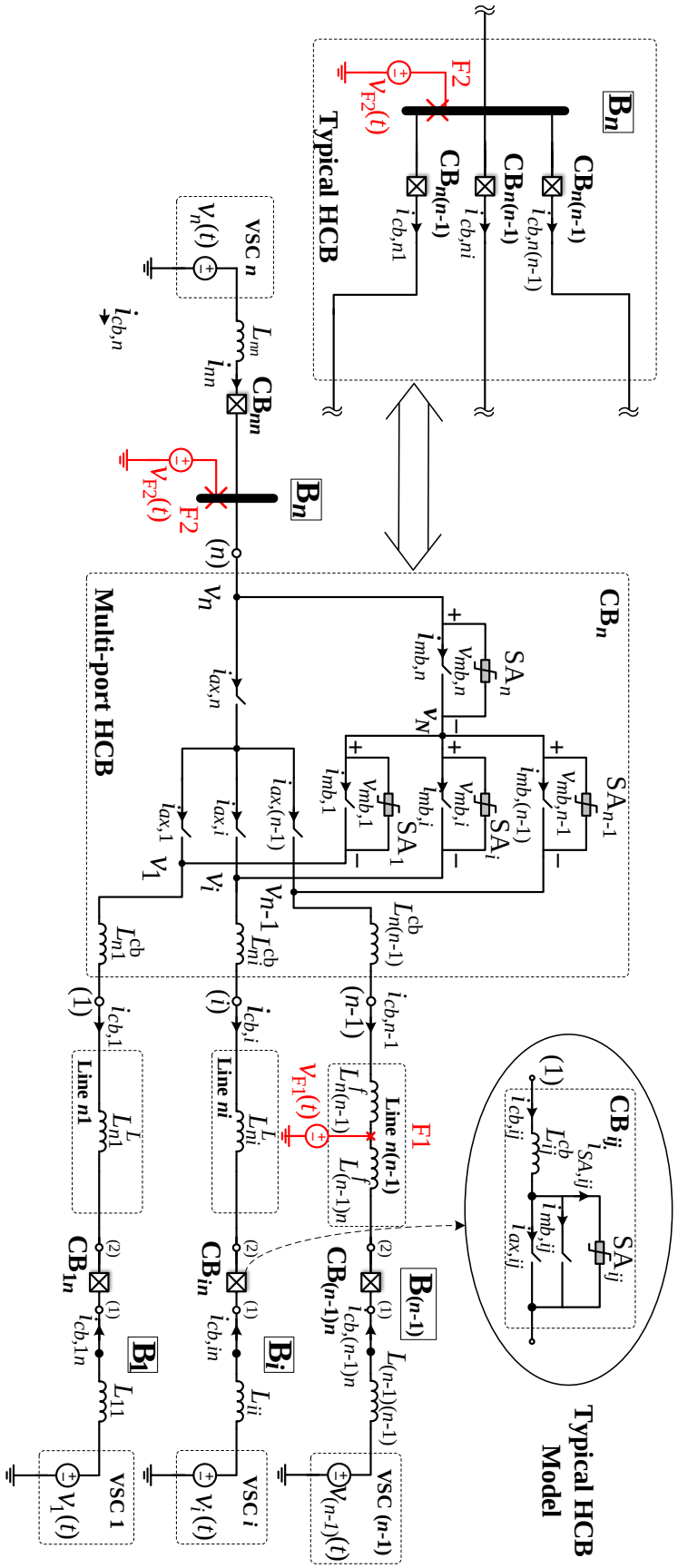


Figure 6.6: Equivalent circuit of test system in presence of Mp-HCB.

In (6.1) $v_{F1}(t)$, $v_j(t)$ and $I_{pre,j}$ represent the voltage at fault location, dc bus B_j voltage and pre-fault current in port j of the Mp-HCB. t_{br} represents the current interruption instant. The current at port j can be given as follows for $j = 1, ..., n-2, n$:

$$i_{cb,j}(t) = \begin{cases} i_{ax,j}(t), & 0 < t \leq t_{ax} \\ i_{mb,j}(t), & t_{ax} < t \leq t'_{ax} \\ i_{mb,j}(t) + i_{ax,j}(t), & t'_{ax} < t \leq t_{br} \\ i_{SA,j}(t) + i_{ax,j}(t), & t_{br} < t \leq t_e \end{cases}, \tag{6.2}$$

and for $j = n-1$:

$$i_{cb,j}(t) = \begin{cases} i_{ax,j}(t), & 0 < t \leq t_{ax} \\ i_{mb,j}(t), & t_{ax} < t \leq t'_{ax} \\ i_{mb,j}(t), & t'_{ax} < t \leq t_{br} \\ i_{mb,j}(t), & t_{br} < t \leq t_e \end{cases}, \tag{6.3}$$

We replace the sum of line jn inductance (L^L_{jn}), faulty line corresponding port current limiting inductor value (L^{cb}_{nj}), the remote end HCB limiting inductor (L^{cb}_{jn}) and the remote dc bus filter inductor (L_{jj}) by L'_{nj}:

$$\begin{aligned} L'_{nj} &= L^{cb}_{nj} + L^L_{jn} + L^{cb}_{jn} + L_{jj} \quad for \quad j = 1, ..., n, \\ L'_{nn} &= L_{nn} + L^{cb}_{nn}. \end{aligned} \tag{6.4}$$

Therefore, the following equation can be given for $t = 0^+$ when the transmission line resistance is neglected:

$$\begin{aligned} V_{dc} = \Big((L'_{n1} \parallel L'_{n2} \parallel ... \parallel L'_{n(n-2)} \parallel L'_{nn}) + \\ L^{cb}_{n(n-1)} + L^f_{n(n-1)} \Big) \frac{\mathrm{d}i_{cb,n-1}(0^+)}{\mathrm{d}t}, \end{aligned} \tag{6.5}$$

where $L^f_{n(n-1)}$ represents the inductance between port $n-1$ and the fault location. Hence, the rate of rise of current at port $n-1$, which is equal to that of fault current can be given by:

$$\frac{\mathrm{d}i_{cb,n-1}(0^+)}{\mathrm{d}t} = \frac{V_{dc}\left(\frac{1}{L'_{nn}} + \sum_{j=1}^{n-2} \frac{1}{L'_{nj}}\right)}{1 + \left(L^{cb}_{n(n-1)} + L^f_{n(n-1)}\right)\left(\frac{1}{L'_{nn}} + \sum_{j=1}^{n-2} \frac{1}{L'_{nj}}\right)} \tag{6.6}$$

The current derivative at the other ports of Mp-HCB for $i = 1, ..., n-2, n$ can be given as:

$$\frac{\mathrm{d}i_{cb,i}(0^+)}{\mathrm{d}t} = \frac{-V_{dc}}{L'_{ni}\left(1 + \left(L^{cb}_{n(n-1)} + L^f_{n(n-1)}\right)\left(\frac{1}{L'_{nn}} + \sum_{j=1}^{n-2} \frac{1}{L'_{nj}}\right)\right)} \tag{6.7}$$

The current in MB and LCS subunits can be obtained using (6.2), (6.3), (6.6) and (6.7). The maximum current at interruption instant set the current requirements of subunits.

Main Breaker (MB) Subunits

The IMB is in ON state when $t_{ax} < t < t_{br}$. Therefore, the current in MB subunits can be evaluated considering two time periods including $t_{ax} < t < t'_{ax}$ and $t'_{ax} < t < t_{br}$.

(6.2) and (6.3) illustrate that the current in MB subunits is equal to the current in the corresponding port for $t_{ax} < t < t'_{ax}$. Assuming instantaneous current commutation at $t = t_{ax}$ and using (6.6) and (6.7), the current in MB subunits for $i = 1, ..., n-2, n$ can be given as:

$$i_{mb,i}(t) = I_{pre,i} + \frac{sgn(i-n+1)V_{dc}t}{L'_{nn}\left[1+\left(L^{cb}_{n(n-1)}+L^{f}_{n(n-1)}\right)\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)\right]} \tag{6.8}$$

and for $i = n-1$:

$$i_{mb,i}(t) = I_{pre,i} + \frac{V_{dc}\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)t}{1+\left(L^{cb}_{n(n-1)}+L^{f}_{n(n-1)}\right)\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)} \tag{6.9}$$

In addition to the MB subunits, LCS_1-LCS_{n-2} and LCS_n conduct when $t'_{ax} < t < t_{br}$. LCS_{n-1} cannot conduct the current since DS_{n-1} is in open position. Figure 6.4(c) shows the equivalent circuit of the Mp-HCB for this time period. The MBs have several IGBTs in series whereas the LCSs have only few IGBTs. The on-state voltage drop on an MB can be hundred times larger than the on-state voltage drop of LCS. Hence, the voltage drop on LCSs can be neglected against that of MB subunits. Therefore, the following equation can be given considering Figure 6.4(c):

$$v'_1 \approx v'_2 \approx ... \approx v'_{n-2} \approx v'_n, \quad t'_{ax} < t \leq t_{br} \tag{6.10}$$

v'_1 - v'_n are illustrated in Figure 6.4(c). Based on (6.10), MB_1, MB_2, ..., MB_{n-2} and MB_n can be considered as parallel branches during the mentioned time period and their currents will be almost equal. The current in MB_j for $t'_{ax} < t < t_{br}$ can be given by: Therefore, the current in the mentioned MB subunits can be given by:

$$i_{mb,j}(t) = \frac{i_{mb,n-1}(t)}{n-1}, j = 1, 2, ..., n-2, n \tag{6.11}$$

The current in MB_{n-1} is equal to the current in its corresponding port and hold the same equation as (6.9).

Load Commutation Switch (LCS) Subunits

As was explained, the ILCS conducts the current in two periods of time. In the first stage (when $0 < t < t_{ax}$), the current in LCS_j holds the same equations as (6.8) and (6.9) and its maximum happens at $t = t_{ax}$. Considering (6.2) and Figure 6.4(c), the current in the LCS subunits for $t'_{ax} < t < t_{br}$ can be given as follows:

$$i_{ax,j}(t) = i_{cb,j}(t) - i_{mb,j}(t), \quad j = 1, 2, ..., n-2, n \tag{6.12}$$

The second maximum of current in the LCS subunits occurs at time t_{br}, which can be obtained by evaluating (6.12) at $t = t_{br}$.

Surge Arresters (SA)

Surge arresters have a non-linear current characteristic. Only for comparison purposes, SA's parameters are approximated by assuming its voltage to be constant until its current falls to zero for both proposed and typical schemes. Figure 3.5 in chapter 3 shows the voltage and current approximation method used for the SAs. It is assumed that the SA current reaches its maximum instantaneously and then decreases linearly. This method is used to identify the maximum possible energy absorption in the surge arresters. Neglecting the practical mismatch between $V-I$ characteristics of surge arresters, the current can be given as:

$$\begin{aligned} \left|i_{SA,j}\right| &= \left|\frac{i_{mb,n-1}}{n-1}\right|, \quad j=1,2,...,n-2,n \\ \left|i_{SA,n-1}\right| &= 0, \end{aligned} \tag{6.13}$$

The current in SA_{n-1} is zero due to conduction of antiparallel diodes of MB_{n-1}. Considering (6.10) it can be assumed that SA_1, SA_2, âĂę, SA_{n-2} and SA_n operate in parallel connection. The rated voltage of each surge arrester is assumed to be equal to V_r. The transient interruption voltage across MB_1 to MB_{n-2} and MB_n can be given by:

$$TIV = V_{dc} + \left(\frac{1}{\frac{1}{L'_{nn}} + \sum_{j=1}^{n-2} \frac{1}{L'_{nj}}} + L^{cb}_{n(n-1)} + L^{f}_{n(n-1)} \right) \frac{I^{mb,n-1}_{max}}{t_e - t_{br}} \tag{6.14}$$

The current in SA reaches zero when its voltage falls below its reference voltage. The range of $t_e - t_{br}$ can be given as:

$$(t_e - t_{br}) \leq \left(\frac{1}{\frac{1}{L'_{nn}} + \sum_{j=1}^{n-2} \frac{1}{L'_{nj}}} + L^{cb}_{n(n-1)} + L^{f}_{n(n-1)} \right) \frac{I^{mb,n-1}_{max}}{V_r - V_{dc}}, \tag{6.15}$$

where, V_r represents the rated voltage of surge arrester. The maximum total absorbed energy in all the surge arresters holds:

$$E_{SA,T} = \int_{t_{br}}^{t_e} V_r \cdot i_{cb,n-1}(t)\, dt \tag{6.16}$$

Consequently, the maximum absorbed energy in SA_j can be given as:

$$\begin{aligned} E_{SA,j} = \frac{V_r I^{cb,n-1}_{max}(t_e - t_{br})}{2(n-1)}; \quad j=1,...,n-2,n, \\ E_{SA,j} = 0; \quad j = n-1. \end{aligned} \tag{6.17}$$

6.3.2 *dc Bus Fault F_2 and Mp-HCB*

As shown in Figure 6.6, a low impedance pole-to-ground fault ($R_{fault} \approx 0\ \Omega$) occurs at dc bus n at time 0 s. The initial conditions and study assumptions are similar to (6.1) and also similar approach to subsection 6.3.1 is used for analysis. The current at port j for various time

periods can be given by:

$$i_{cb,j}(t) = \begin{cases} i_{ax,j}(t), & 0 < t \leq t_{ax} \\ i_{mb,j}(t), & t_{ax} < t \leq t_{br} \\ i_{SA,j}(t), & t_{br} < t \leq t_e \end{cases} \tag{6.18}$$

Using similar approach to section 6.3.1. the rate of rise of current at ports of Mp-HCB can be given as follows:

$$\begin{aligned} \frac{\mathrm{d}i_{cb,n}(0^+)}{\mathrm{d}x} &= V_{dc} \sum_{j=1}^{n-1} \frac{1}{L'_{nj}}; \quad i = n, \\ \left| \frac{\mathrm{d}i_{cb,i}(0^+)}{\mathrm{d}x} \right| &= \frac{V_{dc}}{L'_{ni}}; \quad i = 1, 2, ..., n-1. \end{aligned} \tag{6.19}$$

Main Breaker (MB) Subunits

The currents of MB subunits during $t_{ax} < t \leq t_{br}$ can be given as:

$$i_{mb,i}(t) = \begin{cases} I_{pre,i} - \frac{V_{dc}}{L'_{nj}} t; & i = 1, 2, ..., n-1 \\ I_{pre,i} - V_{dc} \sum_{j=1}^{n-1} \frac{1}{L'_{nj}} t; & i = n \end{cases} \tag{6.20}$$

The maximum current in MB_j ($I_{max}^{mb,j}$) is reached at $t = t_{br}$.

Load Commutation Switch (LCS) Subunits

Despite the line fault scenario, the current in LCS subunits has one maximum at $t = t_{ax}$ and can be given as:

$$I_{max}^{ax,i}(t) = \begin{cases} I_{pre,i} - \frac{V_{dc}}{L'_{nj}} t_{ax}; & i = 1, 2, ..., n-1 \\ I_{pre,i} - V_{dc} \sum_{j=1}^{n-1} \frac{1}{L'_{nj}} t_{ax}; & i = n \end{cases} \tag{6.21}$$

Surge Arresters (SA)

The SA current can be given as:

$$\begin{aligned} \left| i_{SA,j} \right| &= \left| \frac{i_{mb,n}}{n-1} \right|, \quad j = 1, 2, ..., n-2, n-1 \\ \left| i_{SA,n} \right| &= 0. \end{aligned} \tag{6.22}$$

Depending on the length of adjacent lines, the absorbed energy in the surge arresters of the Mp-HCB and also the energy absorption time ($t_{e,j} - t_{br}$) can be different for each surge arrester. The range of energy absorption time can be given as:

$$t_{e,j} - t_{br} \leq \frac{L'_{nj} I_{max}^{cb,i}}{V_r - V_{dc}}, \quad j = 1, 2, ..., n-1 \tag{6.23}$$

where $t_{e,j}$ is the time when the current in SA_j becomes zero. Due to conduction of antiparallel diode D_n, the current in SA_n remains zero and consequently the absorbed energy in SA_n is also zero. The maximum absorbed energy in SA_j can be given by:

$$E_{SA,j} = \frac{V_r I_{max}^{mb,j} \left(t_{e,j} - t_{br} \right)}{2}, \quad j = 1, 2, ..., n-1 \tag{6.24}$$

6.3.3 Transmission Line Fault and HCB

As shown in Figure 6.6, the Mp-HCB can be replaced by $n-1$ HCBs at B_n. A detailed schematic of the HCB is illustrated in the figure. Similar fault analysis to subsections 6.3.1 and 6.3.2 have been carried out. For sake of brevity, only the most relevant equations are included in this section.

Load Commutation Switch (LCS) Subunits

The LCS current in $CB_{n(n-1)}$ reaches its maximum at $t = t_{ax}$ whereas the current in LCS unit of CB_{ni} reaches its maximum at $t = t_{br}$. The maximum current in LCS unit of CB_{ni} for $n = 1, 2, ..., n-2, n$ can be given by:

$$I_{max}^{ax,i}(t) = I_{pre,i} + \frac{sgn(i-n+1)V_{dc}t_{br}}{1+\left(L_{n(n-1)}^{cb}+L_{n(n-1)}^{f}\right)\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)} \tag{6.25}$$

and for $i = n-1$:

$$I_{max}^{ax,i}(t) = I_{pre,i} - \frac{V_{dc}\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)t_{ax}}{1+\left(L_{n(n-1)}^{cb}+L_{n(n-1)}^{f}\right)\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)} \tag{6.26}$$

Main Breaker (MB) Subunits

It is assumed that only the MB unit of corresponding HCB of the faulty line is activated. Therefore, the current in MB units of other HCBs remain zero. The current in MB unit of $CB_{n(n-1)}$ for $t_{ax} < t \leq t_{br}$ can be given as:

$$i_{mb,n-1}(t) = I_{pre,n-1} - \frac{V_{dc}\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)t}{1+\left(L_{n(n-1)}^{cb}+L_{n(n-1)}^{f}\right)\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)} \tag{6.27}$$

The maximum current in the MB unit in $CB_{n(n-1)}$ ($I_{max}^{mb,n(n-1)}$) is reached at time t_{br}.

Surge Arresters (SA)

The currents in surge arresters of all the HCBs are zero except the faulty line HCB ($SA_{n(n-1)}$). The absorbed energy in the surge arrester can be given by:

$$E_{SA,n(n-1)} = \frac{V_r I_{max}^{mb,n(n-1)}\left(t_{e,j}-t_{br}\right)}{2} \tag{6.28}$$

6.3.4 dc Bus Fault and HCB

Load Commutation Switch (LCS) Subunits

During the bus fault, all the adjacent HCBs of the faulty dc bus are activated. The maximum current in the LCS unit of all adjacent HCBs ($I_{max}^{ax,ni}$) can be given as:

$$I_{max}^{ax,ni} = I_{pre,ni} - \frac{V_{dc}}{L'_{ni}}t; \quad i = 1, 2, ..., n-1 \tag{6.29}$$

Main Breaker (MB) Subunits

The currents of MB units for $0 < t \leq t_{br}$ can be given as:

$$i_{mb,ni}(t) = I_{pre,ni} - \frac{V_{dc}}{L'_n i}t; \quad i = 1, 2, ..., n-1 \tag{6.30}$$

The maximum current in the MB unit ($I_{max}^{mb,ni}$) is reached at $t = t_{br}$.

Surge Arresters (SA)

The absorbed energy in SA_{nj} can be given by (6.31).

$$E_{SA,j} = V_r I_{max}^{mb,j} \left(t_{e,j} - t_{br}\right), \quad j = 1, 2, ..., n-1 \tag{6.31}$$

6.4 Simulation Results

In this section the results of simulation for line and dc bus faults in a simplified model of a three-terminal grid and a detailed model of four-terminal grid are presented. The simulations are carried out using PSCAD.

6.4.1 Three-terminal Grid

The three-terminal grid model is shown in Figure 6.7. Two HCBs (CB_{31} and CB_{32}) at bus 3 are replaced by a 3-port Mp-HCB. The parameters of test system and also the internal parameters of both dcCBs are illustrated in Table 6.1 and 6.2, respectively. The transmission lines are protected by overcurrent protection scheme. The line fault trip command is sent to the corresponding dcCBs when the line current exceeds 2.8 kA. The dc buses of grid are protected by differential protection scheme. In this scheme, when the sum of incoming and outgoing currents at a dc bus becomes non-zero, the dc bus trip signal is activated. The dc bus fault measurement and identification delay is also considered and set to 1 ms.

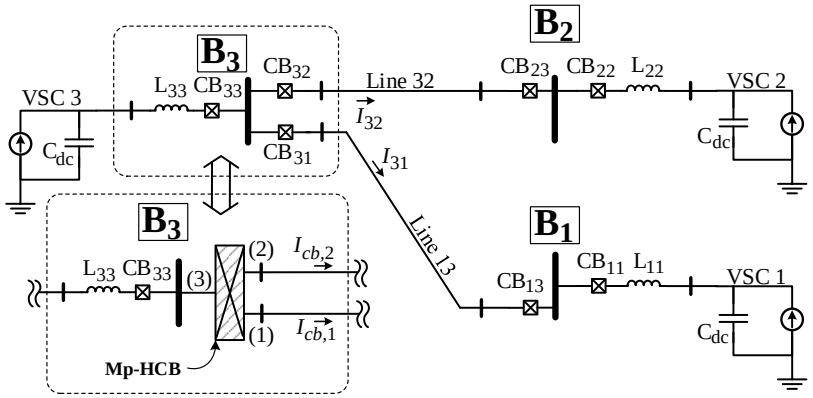


Figure 6.7: Mp-HCB and HCBs in the theee-terminal test grid.

Converter terminal parameters			
Parameter	**VSC 1**	**VSC 2**	**VSC 3**
Rated power [MVA]	300	150	150
dc bus capacitor [μF]	1000	1000	1000
dc bus voltage [kV]	320	320	320
Bus,filter reactor [mH]	10	10	10
Cable parameters			
Parameter	**Line 32**	**Line 13**	
Length,[km]	200	150	
Resistance,[Ω/km]	0.001	0.001	
Inductance,[mH/km]	2	2	

Table 6.1: Three-terminal HVdc system parameters.

Parameter	**HCB**	**Mp-HCB**
$t'_{ax} - t_{ax}$	-	2.25 ms
$t_{br} - t'_{ax}$	-	150 Âţs
$t_{br} - t_{ax}$	2.25 ms	2.4 ms
V_r (Surge arrester)	460 kV	460 kV
Limiting Inductor	50 mH	50 mH

Table 6.2: Mp-HCB and HCB simulation model parameters.

Transmission line Fault

A low impedance pole-to-ground fault (100 mΩ) is placed at the middle of line 32 at time 0 s. In HCB based protection CB_{32} and CB_{23} and in case of Mp-HCB based protection CB_{32} and port 2 of Mp-HCB should trip. Figure 6.8 and 6.9 show the waveforms for Mp-HCB and HCBs, respectively.

The important numerical values obtained from simulation and analysis are also illustrated in Table 6.3. Comparing Figure 6.8(a) and Figure 6.9(a) confirms that the behavior of typical and proposed dcCBs from grid point of view are similar. Slight difference (25 A) in the interrupted currents of HCB and Mp-HCB is observed due to the additional time, which is considered in the modeling of current sharing stage in Mp-HCB. Figure 6.8(b)-(d) depict the current in the subunits of Mp-HCB.

As can be seen in Figure 6.9(b) and (c) CB_{31} has no internal operation whereas the fault current is commutated into the MB unit in

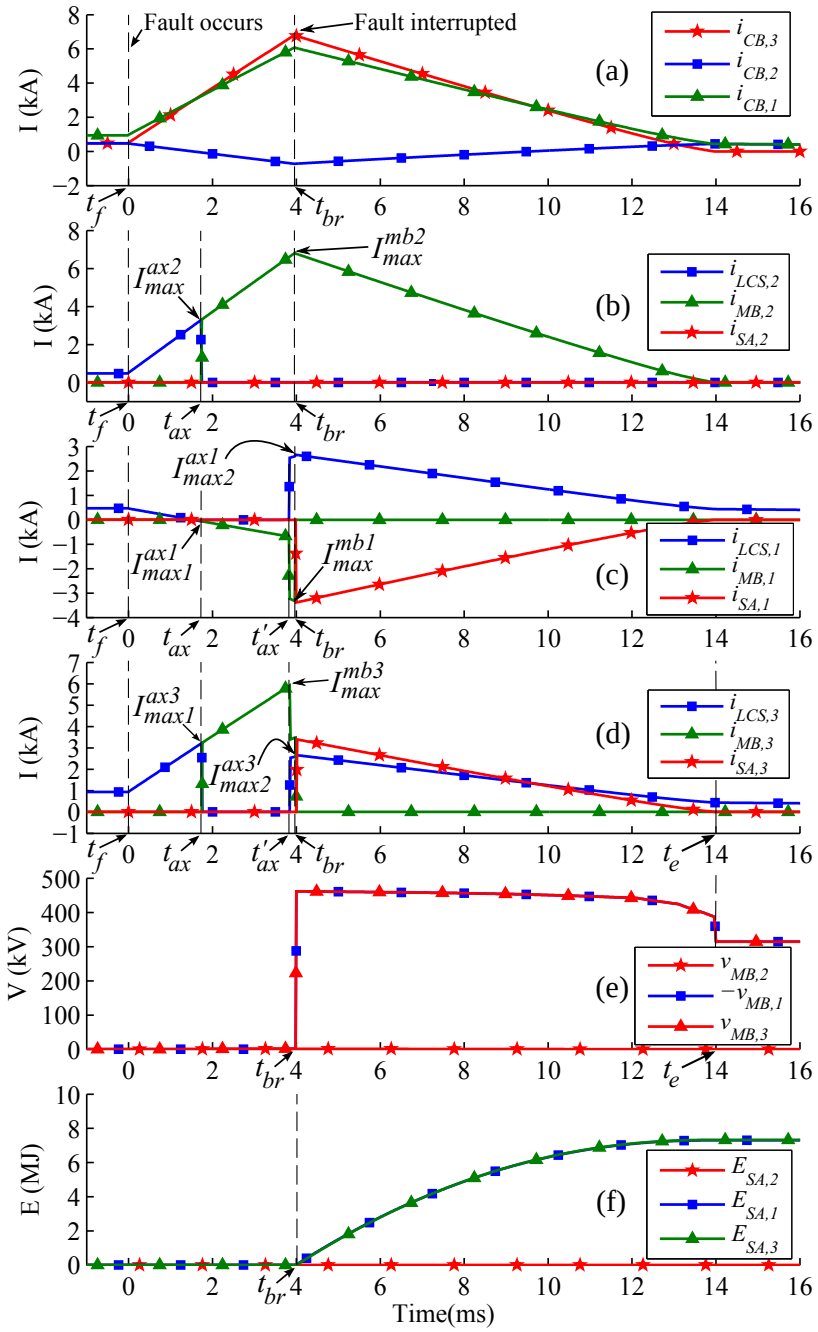


Figure 6.8: Mp-HCB during line fault at line 32 of three-terminal grid.

CB_{32}. Figure 6.8(b) and Figure 6.9(b) show that the trip command is received by the corresponding dcCBs at $t_{ax} = 1.7$ ms and then the current is commutated into the corresponding (I)MB unit. Table 6.3 illustrates that the simulation results are in agreement with the analysis in section 6.3.

It can be seen in Figure 6.8(f) and Figure 6.9(e), the absorbed energy in the surge arrester of HCB is almost equal to twice the absorbed energy in each surge arrester of Mp-HCB.

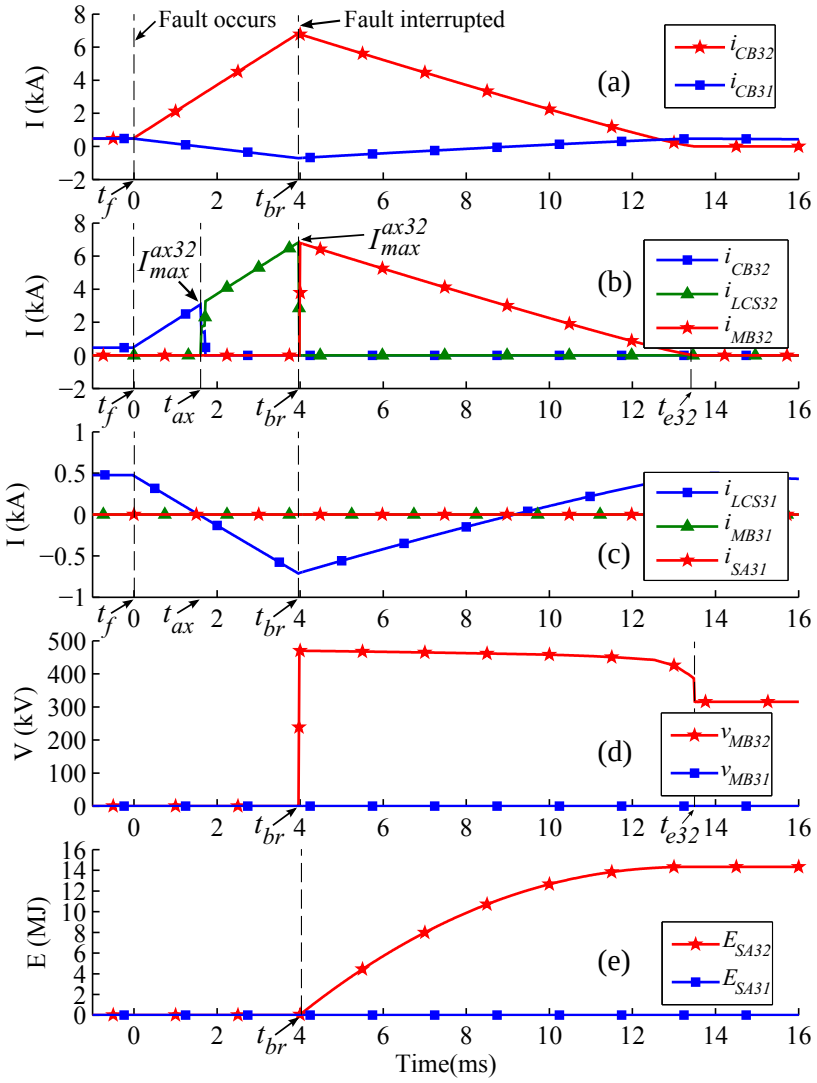


Figure 6.9: HCBs during line fault at line 32 of three-terminal grid.

Parameters	Mp-HCB		HCB	
Mp-HCB (HCB)	Analysis	Simulation	Analysis	Simulation
$I_{max1}^{ax,2}(I_{max}^{ax,2})[kA]$	3.198	3.190	3.198	3.190
$I_{max}^{mb,2}(I_{max}^{mb,2})[kA]$	6.84	6.83	6.82	6.81
$E_{SA,2}(E_{SA,32})[MJ]$	0	10^{-7}	14.844	14.340
$E_{SA,1}(E_{SA,31})[MJ]$	7.422	7.315	0	0
$E_{SA,3}[MJ]$	7.422	7.333	-	-

Table 6.3: Mp-HCB and HCB parameters during line fault.

dc Bus Fault

A low impedance pole-to-ground fault (100 mΩ) is placed at bus B_3. The differential protection relay activates the trip signal at almost $t = 1$ ms. In HCB based protection CB_{33}, CB_{31} and CB_{32} and in Mp-HCB based protection CB_{33} and all the ports of Mp-HCB should trip. Figure 6.10 and 6.11 depicts the waveforms of Mp-HCB and HCBs, respectively. It can be seen in Figure 6.10(b)-(d) that the fault current is commutated into MB subunit for all ports. In contrary with MB_1 and MB_2, the current in MB_3 does not redirected to the surge

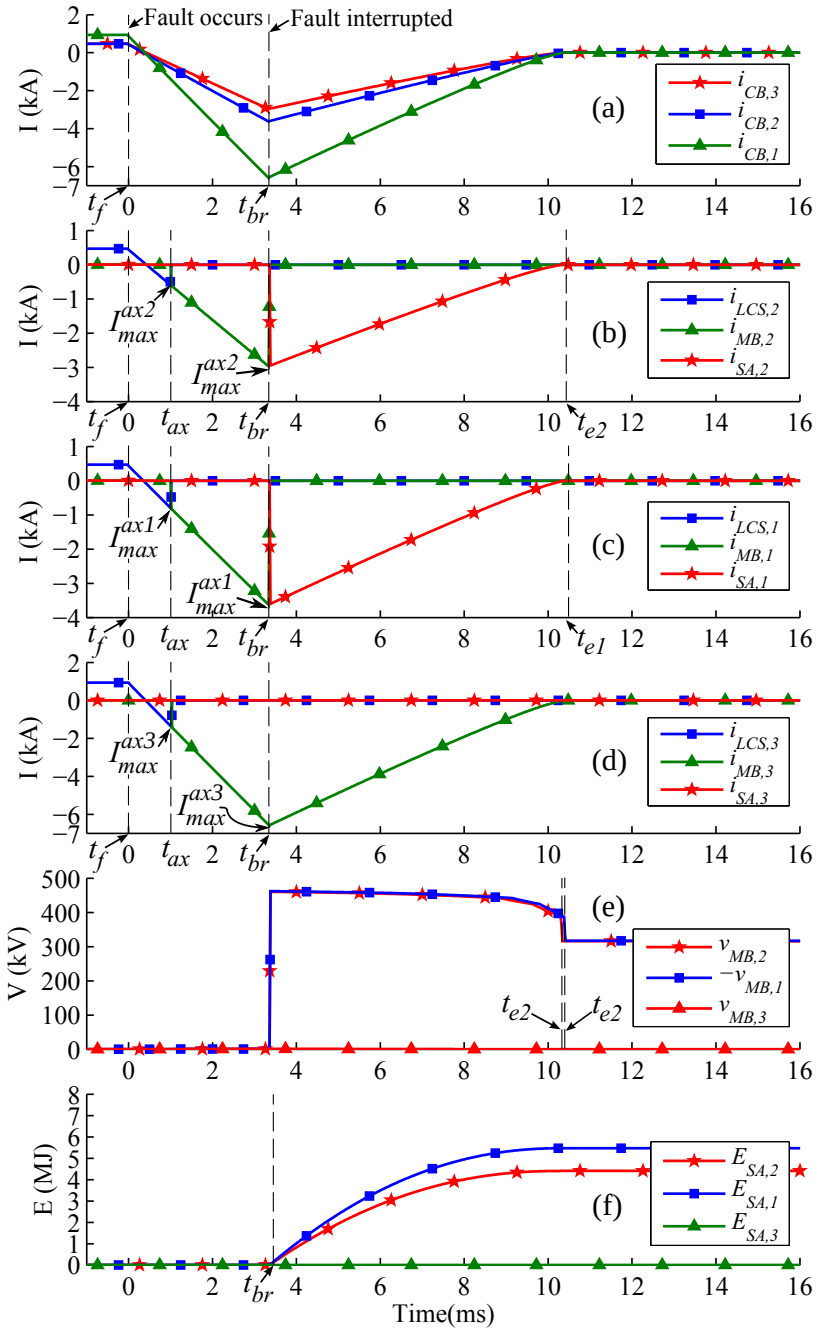


Figure 6.10: Mp-HCB during bus fault at bus 3 of three-terminal grid.

arrester due to the explained reason in section 6.3.

The most relevant numerical values obtained from analysis and simulation are illustrated in Table 6.4. The obtained approximated values from analysis are close to the values obtained from simulation of simplified model. The maximum current in MB_{31} and MB_1 and also in MB_{32} and MB_2 are equal. Moreover, the maximum current in LCS_{31} and LCS_1 and also in LCS_{32} and LCS_2 are equal. The current in MB_3 of Mp-HCB reaches 6.62 kA, which is higher than the currents of other subunits. However, this does not necessarily mean that the antiparallel diodes of MB_3 should be rated for higher current than

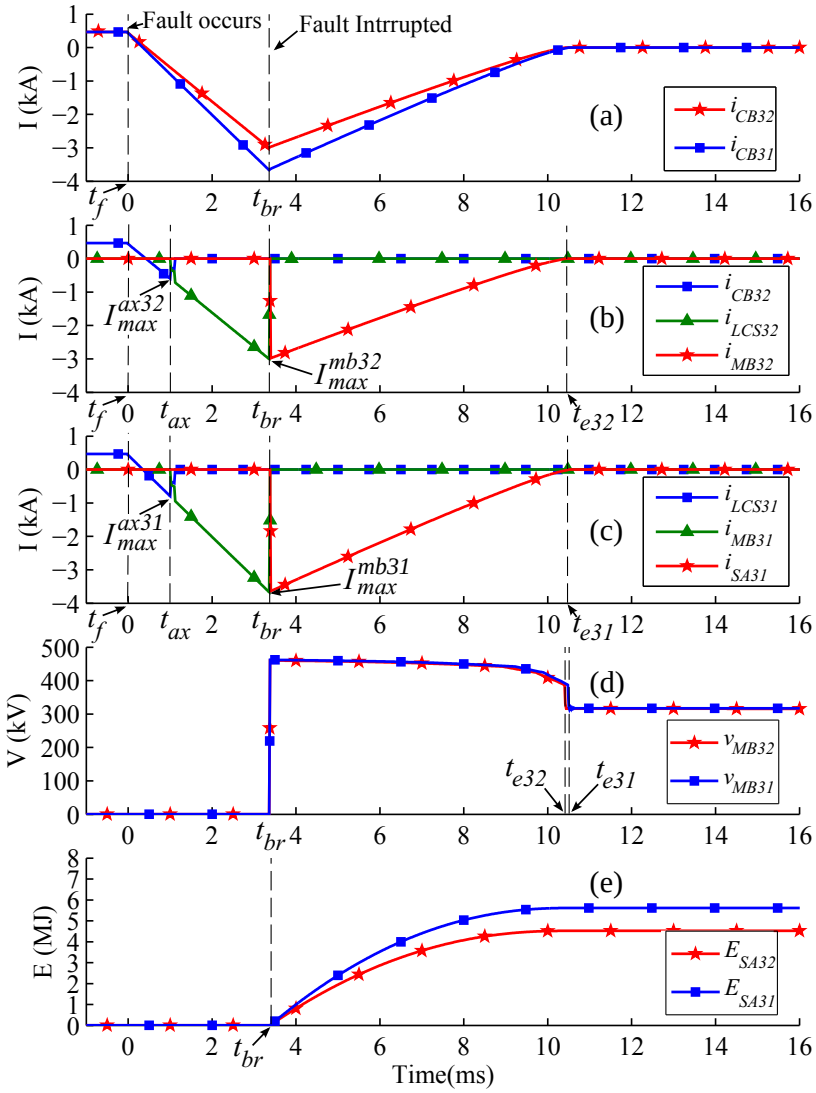


Figure 6.11: HCB during bus fault at bus 3 of three-terminal grid.

Parameters	Mp-HCB		HCB	
Mp-HCB (HCB)	Analysis	Simulation	Analysis	Simulation
$I_{max}^{ax,1}(I_{max}^{ax,31})$ [kA]	-0.76	-0.78	-0.76	-0.78
$I_{max}^{ax,2}(I_{max}^{ax,32})$ [kA]	-0.56	-0.54	-0.56	-0.54
$I_{max}^{ax,3}$ (-) [kA]	-1.32	-1.35	-	-
$I_{max}^{mb,1}(I_{max}^{mb,31})$ [kA]	-3.64	-3.62	-3.64	-3.62
$I_{max}^{mb,2}(I_{max}^{mb,32})$ [kA]	-2.97	-2.96	-2.97	-2.96
$I_{max}^{mb,3}$ (-) [kA]	-6.62	-6.59	-	-
$E_{SA,1}(E_{SA,31})$ [MJ]	5.661	5.478	5.661	5.472
$E_{SA,2}(E_{SA,32})$ [MJ]	4.492	4.415	4.492	4.411
$E_{SA,3}(-)$ [MJ]	0	2×10^{-6}	-	-

Table 6.4: Mp-HCB and HCB parameters during bus fault.

the antiparallel diodes of MB_1 and MB_2. In fact, MB_1 and MB_2 may be required to carry higher currents during a line fault and should be rated for that. Figure 6.10(e) and 6.11(d) illustrate that equal amount of absorbed energy in SA_1 and SA_{31} and also in SA_2 and SA_{32}.

Power Flow

The currents flowing from the dc bus and the transmission lines in presence of the Mp-HCB are depicted in Figure 6.12. Figure 6.12(a) and (b) depict the currents for dc bus B_3 and line 32 fault scenarios, respectively. Moreover, Figure 6.13 illustrates the currents flowing from the dc bus and the transmission lines in presence of the HCBs. Figure 6.13(a) and (b) depict the currents for dc bus B_3 and line 32 fault scenarios, respectively. In all scenarios, the fault happens at time $t = 0$ s. The behavior of Mp-HCB has been found out to be similar to the typical scheme during normal operation and fault condition from the grid point of view. Figure 6.12 shows that the Mp-HCB can clear a single line fault without tripping all its ports.

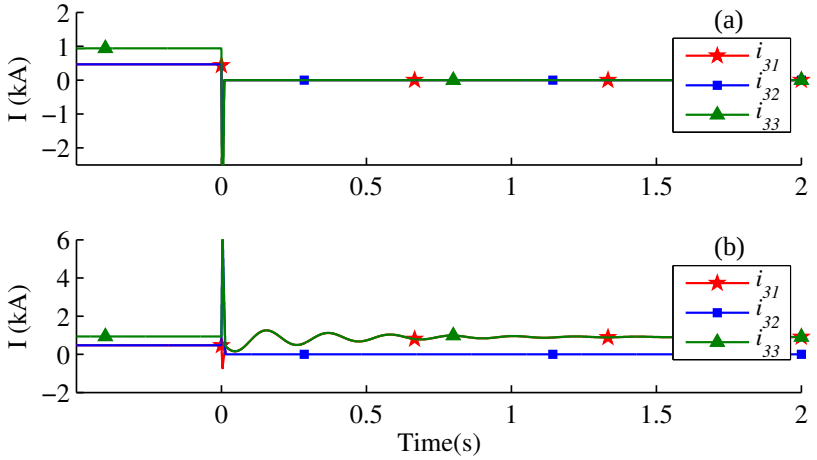


Figure 6.12: Transmission lines and dc bus currents in Mp-HCB based scheme during fault at: a) dc bus B_3, b) line 32.

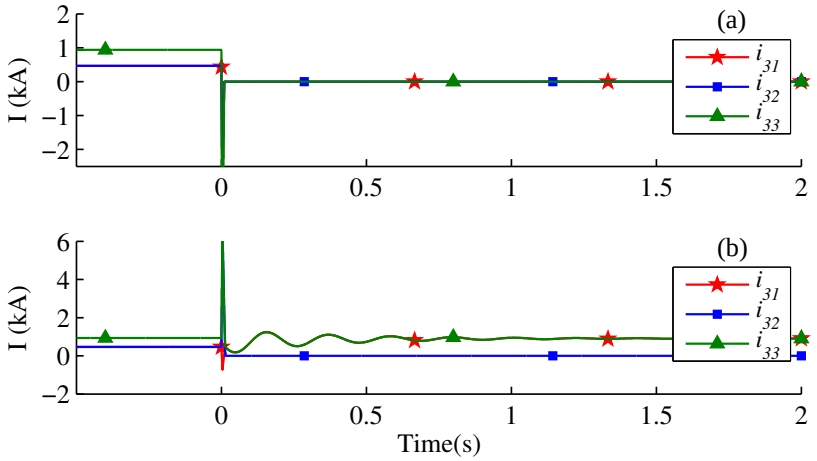


Figure 6.13: Transmission lines and dc bus currents in HCB based scheme during fault at: a) dc bus B_3, b) line 32.

6.4.2 *Four-terminal Grid*

The functionality of Mp-HCB is examined through the detailed model of four-terminal meshed HVdc grid explained in chapter A. The system configuration with typical HCBs and MP-HCBs is shown

in Figure 6.14. A state of art protection scheme [214] explained in chapter B is utilized to protect the multi-terminal grid against the line and dc bus faults.

The internal timing of HCB and Mp-HCB actions are provided in Table 6.2, whereas the value of rated voltage of surge arresters are set to 480 kV and the current limiting inductors of both HCB and Mp-HCB are set to 50 mH.

Transmission Line Fault

A low impedance pole-to-pole fault (100 mΩ) is placed at the middle of line 13 at $t = 0$ s. The trip command is generated by the protective relay at $t = 1.1$ ms. Figure 6.15(a) shows the current in corresponding HCB (CB_{31}) and port 2 of Mp-HCB.

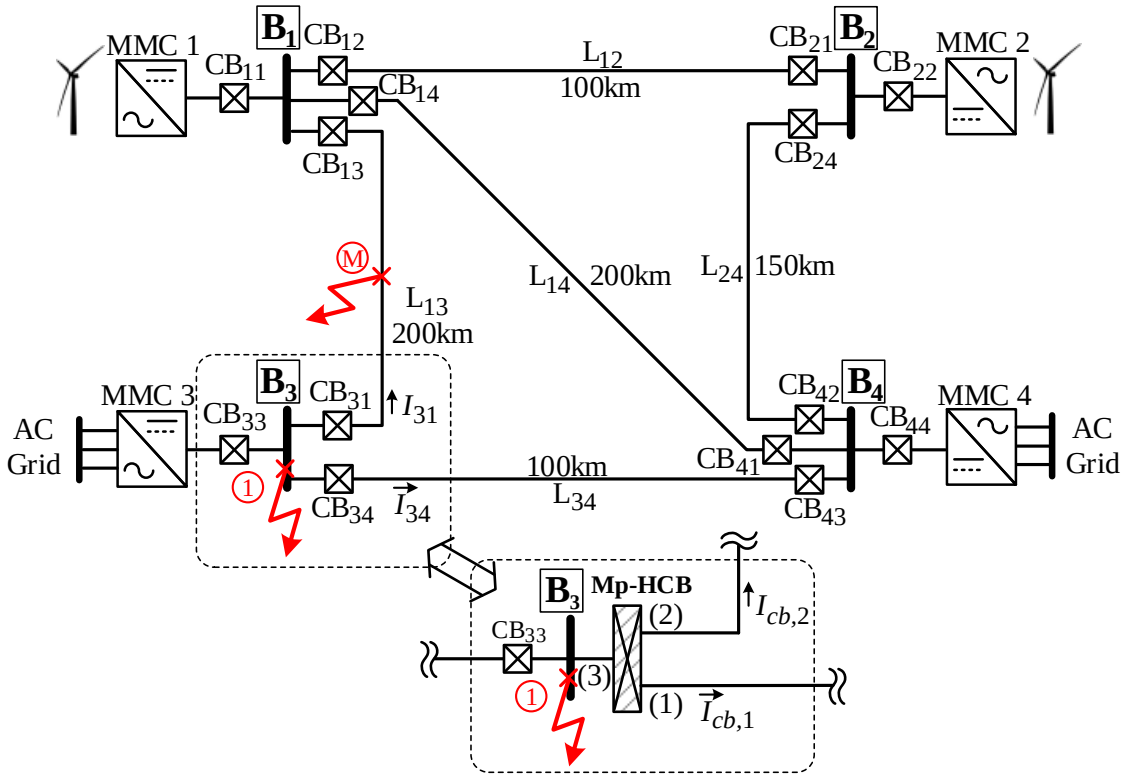


Figure 6.14: Four-terminal dc grid model.

Similar to the simplified model, the current in Mp-HCB reaches slightly higher value (30 A) due to the additional internal operation stage. The absorbed energy in both types of dcCBs are depicted in Figure 6.15(b). The absorbed energy in each surge arrester is in accordance with the analysis and aforementioned results.

dc Bus Fault

A low impedance pole-to-pole fault (100 mΩ) is placed at bus B_3 of the test grid. The protection relay activates the trip signal at $t = 0.4$ ms. The current in adjacent dcCBs of B_3 are shown in Figure 6.16(a) and (b). As it is expected the current waveforms of both dcCBs are almost the same. Slight difference is due to additional time period of

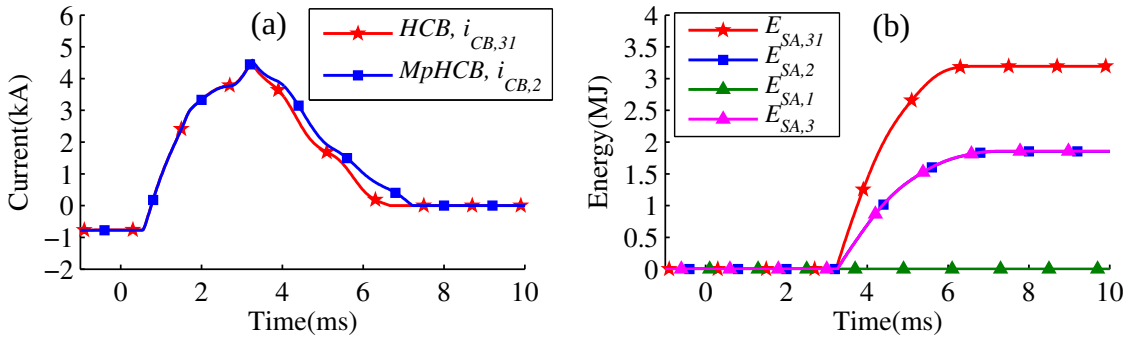


Figure 6.15: Mp-HCB and HCBs during fault on line 31 in the four-terminal grid.

current sharing stage in Mp-HCB. Therefore, it can be seen in Figure 6.16(c) and (d) that the surge arrestors in Mp-HCB are required to absorb higher amount of energy as compared to the HCBs. However, the amount of absorbed energy is not higher than the amount of absorbed energy in HCBs during the line fault (Figure 6.15(b)).

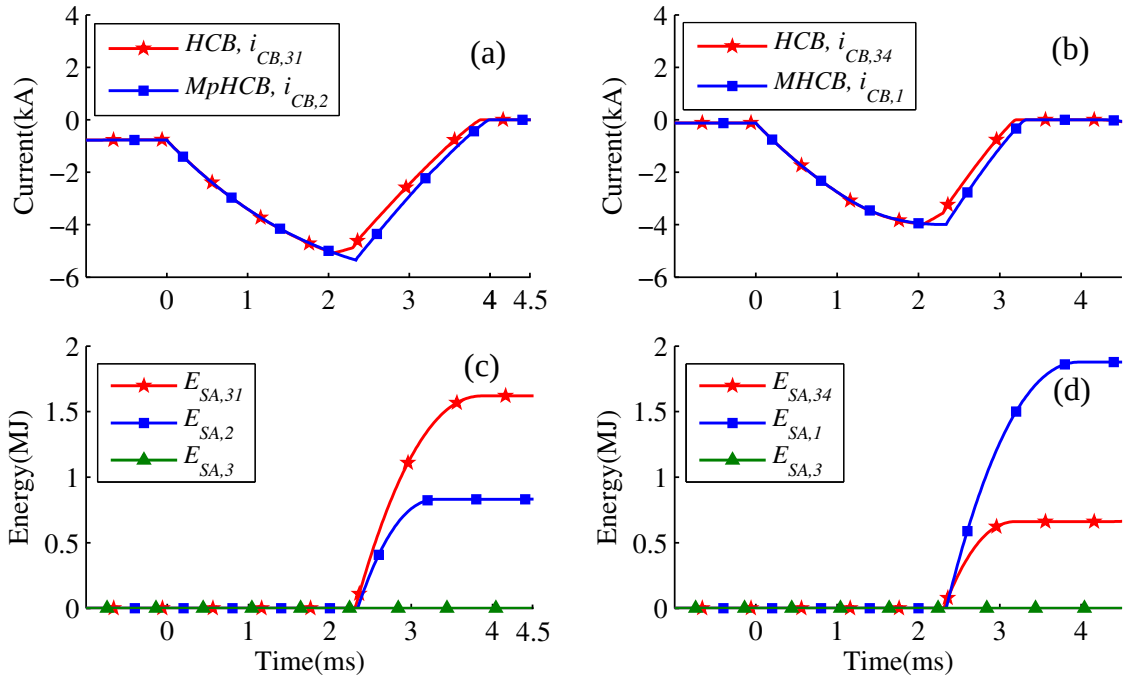


Figure 6.16: Mp-HCB and HCBs during fault at bus 3 in the four-terminal grid.

6.5 Comparison

The proposed Mp-HCB is compared to the typical HCB in this section. As seen in Figure 6.3(a), to protect a dc bus with $n-1$ adjacent lines and one converter station with an asymmetric monopole HVdc configuration, n HCBs are required. The number of HCBs can be doubled in symmetric monopole and bipole configurations. Although the comparison study is done for asymmetric monopole configuration, it is valid for other mentioned configurations. As shown in Figure 6.3(b), the HCBs can be replaced by an n-port Mp-HCB. The converter station HCB (CB_{nn}) will not be removed. Therefore, the requirements

of CB_{nn} in both cases are equal and will not be compared and included in calculations.

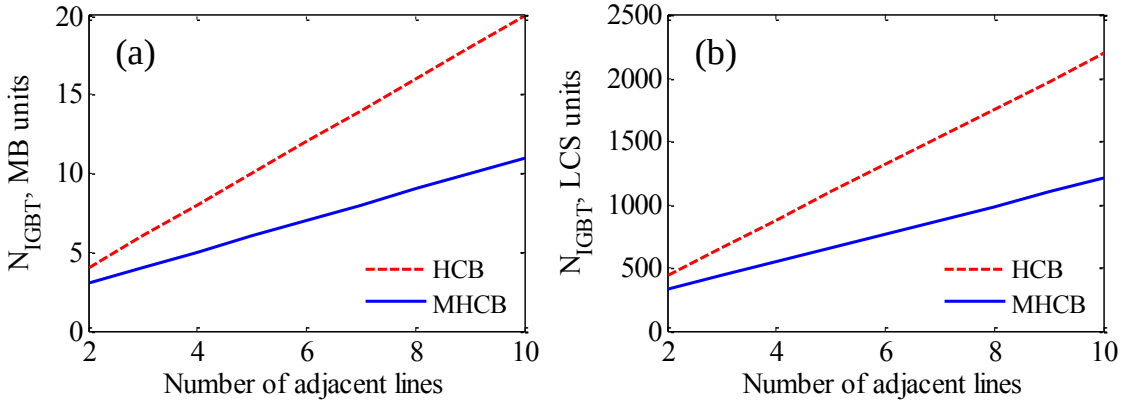


Figure 6.17: Number of IGBTs versus the number of adjacent lines (a) MB (b) LCS.

Table 6.5 compares different aspects of both the proposed and typical devices assuming $t'_{ax} \approx t_{br}$.

Table 6.5: Mp-HCB and HCB parameters comparison.

dc bus protection requirement with $n-1$ adjacent line			
Parameter	**Asymmetric Monopole**	**Symmetric Monopole**	**Bipole**
Mp-HCB	1	2	2
HCB	$n-1$	$2(n-1)$	$2(n-1)$
Internal parameters comparison (For dc bus with $n-1$ adjacent line)			
Parameter	**HCB**	**Mp-HCB**	
Number of UFDs	$n-1$	$n-1$	
Number of limiting ind.	$n-1$	$n-1$	
Number of surge arresters	$n-1$	n	
Surge arresters energy	E	$\frac{E}{n}$	
Surge arresters voltage	V_r	V_r	
Number of IGBTs in LCS	$2(n-1)$	n	
Number of IGBTs in MB	$\frac{(n-1)V_r}{V_{CES}}$	$\frac{nV_r}{V_{CES}}$	

6.5.1 *Load Commutation Switches*

The maximum current in LCS unit of HCB_{nj} is equal to the first maximum current in LCS_j in Mp-HCB for line fault scenario. Depending on the grid topology, the second maximum current in LCS units of Mp-HCB might be greater as compared to the typical HCB. During the dc bus fault condition the current in LCS_1 to LCS_{n-1} of Mp-HCB are equal to the current in LCS units of HCB_{n1} to $HCB_{n(n-1)}$. The current in LCS_n is equal to sum of currents in LCS_1 to LCS_{n-1} of Mp-HCB and therefore is higher than the currents in other subunits. Note that the current in LCS_n flows through the antiparallel diode D_n during the bus fault. However, considering the most severe power flow scenario in normal condition where the current flowing through LCS_n can be equal to the sum of currents flowing though LCS_1-LCS_{n-1}, LCS_n may require additional parallel branches. In the worst case, the number of parallel branches in LCS_n can be equal to the number of adjacent transmission lines when similar IGBTs are used for realization of all

LCS subunits. Hence, the current rating of the IGBTs are equal. Fig. 6.17(a) shows the total number of required IGBTs for LCS units of HCB and Mp-HCB for protecting a dc bus with $n-1$ adjacent lines. The figure is plotted using Table 6.5 and assuming V_{ovp}=460 kV and V_{CES}=4.5 kV. V_{CES} represents the collector-emitter voltage of IGBTs. It can be seen that in the worst case, the number of required IGBTs in LCS units of Mp-HCB based protection and the HCB based protection are identical.

6.5.2 Main Breaker Units

During the line fault the current in corresponding MB (sub)units of the Mp-HCB and HCB are equal. Similar to the previous subsection, the antiparallel diodes of subunit n of IMB in Mp-HCB may need to be able to carry higher current as compared to the other (sub)units depending on the fault identification time and the grid topology. The number of IGBTs are compared in Table 6.5. Figure 6.17(b) depicts the total number of IGBTs in MB (sub)units versus the number of adjacent lines. Figure 6.17(b) shows that the Mp-HCB requires significantly fewer IGBTs, especially when the number of adjacent lines increases.

6.5.3 Surge Arresters

Reference Voltage

The rated voltage for the surge arrester of the HCB would lie in range of $1.4V_{dc} - 1.5V_{dc}$ [138,162]. The rated voltage of surge arresters of Mp-HCB are also assumed to lie in the same range.

Discharge Current

(6.13) illustrates that the maximum discharge current in the surge arresters of the CFCCB in line fault scenario is smaller than the value of fault current at the interruption instance by a factor of $n-1$. However, the maximum discharge current in the surge arrester in typical HCB is almost equal to the interrupted current.

Energy

In HCB based protection and during the line fault, only the faulty line dcCB interrupts the current and its surge arrester absorbs the energy. When using the Mp-HCB the faulted line corresponding surge arrester does not absorb the energy and the energy absorption is shared between $n-1$ surge arresters. Using (6.17) and (6.28) the ratio of total absorbed energy in both dcCBs can be given as:

$$\frac{E_{SA,T}^{Mp-HCB}}{E_{SA,T}^{HCB}} = \frac{1}{n-1}, \tag{6.32}$$

where $E_{SA,T}^{Mp-HCB}$ and $E_{SA,T}^{HCB}$ represents the total absorbed energy in the surge arresters of Mp-HCB and HCB, respectively. (6.32) implies

that the energy rating of surge arresters in Mp-HCB is at least 50% smaller than that of HCB. The Mp-HCB performance during the dc bus fault was found to be similar to the HCB. Therefore, equal amount of energy is absorbed in the surge arresters of both devices.

6.5.4 Ultra-Fast Disconnector

Each HCB has an ultra-fast disconnector (UFD). As shown in Figure 6.2, the n-port Mp-HCB has $n-1$ UFDs. Therefore, there is no difference in number of required UFD units for both typical and proposed schemes.

6.5.5 Current Limiting Inductors

The number of current limiting inductors in both schemes are identical. Also, the inductances of current limiting inductors for the proposed and typical devices are equal.

6.5.6 Multiple Fault Handling

The average failure rate for all types of submarine power cables are 0.1114 faults/100 km/year [223] and it has been reducing since most new cables being buried to a depth of at least 0.5 m and have better route design. Considering that, the future MT-HVdc grid is expected to connect large wind farms and the cables will not be buried physically close together, the probability of faults in different cables are independent. Therefore, using the fault occurrence probability in single cable the multiple fault probability can be obtained by multiplication of single fault probabilities. For instance, the average failure rate for 2 cables at the same time for all types of submarine power cables can be obtained as 0.0124 faults/100 km/year. This means the average time for having faults on two cables simultaneously in 100 km is almost 80 years. This time range is even longer than the lifetime of offshore systems. Therefore, due to the proposed application for Mp-HCB, the multiple fault occurrence has not been considered in design of Mp-HCB.

However, in case that the proposed Mp-HCB is needed to be designed for systems with considerable multiple faults occurrence probability, the MB subunits may be required to be rated for higher currents depending on the number of ports (adjacent lines). The worst case happens when the system has two adjacent lines (3-port Mp-HCB). In this case, when two faults simultaneously happen, MB_n is required to carry sum of the fault currents. However, when the system has larger number of adjacent lines, when two faults happen, MB_n will carry only a portion of sum of fault currents as other healthy MB subunits will also carry some portion of sum of the fault currents. For instance, assume a system with 5 adjacent lines (6-port Mp-HCB). If two faults happen on adjacent lines connected to ports 1 and 2, the sum of fault currents will be shared between MB_3, MB_4, MB_5 and MB_6. Therefore, an increase in the rating of MB subunits is expected. Note

that the requirement for increase in the ratings of MB subunits will be decreased as the number of adjacent lines are increased. Moreover, when Mp-HCB is interrupting a fault current ($t_{ax} < t < t_{br}$), if it receives another trip command (due to another fault occurrence), it should restart the interruption process from $t = t_{ax}$ and open the required DS before opening MB units. This can lead to a delay in current interruption and consequently higher magnitude of fault current as it will be growing during the mentioned delay time, which can reach to 2.25 ms in the worst case.

6.6 Conclusion

The availability of an effective and reliable dc circuit breaker is one of the main prerequisites for the development of future large multi-terminal dc grids. Although, the HCB has been proposed as a solution for this problem, the implementation cost of a few HCBs would be comparable to that of a modern converter station.

In this chapter, a novel multi-port dc circuit breaker has been proposed and analyzed. Each port of Mp-HCB can interrupt the current, independent of the other ports. The proposed device has a similar time performance compared to the HCB. The analysis implies that the proposed Mp-HCB requires fewer IGBTs compared to the typical HCB. For a dc bus with two adjacent transmission lines, Mp-HCB needs 25% fewer IGBTs as compared to the HCB. As the number of adjacent lines increases the percentage of saved IGBTs approaches 50%.

Moreover, the proposed device requires smaller size surge arresters due to less discharge current energy absorption in its surge arresters as compared to the HCB. The results from this study confirms that the energy ratings of the surge arresters can be reduced by almost 50%. Considering the improvements by applying the proposed device, its implementation cost is expected to be remarkably lower than the cost of typical HCBs. The future work will concern with the cost-benefit and reliability studies of the proposed device.

7
Current Flow Controlling Hybrid dc Circuit Breaker

Mokhberdoran, A.; Gomis-Bellmunt O.; Silva, N., Carvalho, A., "Current Flow Controlling dc Circuit Breaker", *IEEE Transaction on Power Electronics Journal*, Early Access, March 2017.

Let the future tell the truth and evaluate each one according to his work and accomplishments. The present is theirs; the future, for which I really worked, is mine.

Nikola Tesla, Physicist, Inventor, and Electrical engineer, 1856-1943.

In addition to the protection problem, a meshed HVdc (M-HVdc) grid as a complex form of the MT-HVdc grid may face power flow control problems. Typically, the power flow in the M-HVdc grid is controlled by regulating the converters' dc side voltage considering the transmission line impedance. Due to the M-HVdc grid topology, there are multiple paths for the current to circulate between two different nodes. Consequently, some of the transmission lines can be overloaded because of their lower impedances [22].

Over the last decade, several current flow controller (CFC) devices have been introduced to solve the power flow problem in M-HVdc grid [224–229]. The series CFCs demonstrate less power losses and reduced cost due to their lower voltage requirement and hence the fewer number of switches. The interline dual H-bridge CFC with reduced number of switches can be considered as one of the most efficient CFCs [226].

The coordinated operation of HCBs and CFCs is expectable in the future M-HVdc grids. As an alternative solution, this chapter proposes a new device, which benefits from the core idea of typical HCB [134] and possesses an embedded CFC [226] and therefore can be named as current flow controlling circuit breaker (CFCCB). The CFCCB has three ports and can connect a dc bus to two adjacent transmission lines. The CFCCB can regulate the current in one of the adjacent lines and upon receiving a trip command can interrupt the fault current and isolate the faulty line from the dc bus. The

proposed approach requires fewer number of semiconductor switches as compared to the typical approach. Moreover, the ratings of required surge arresters in dcCB part can be reduced remarkably by employing the proposed device.

This chapter is organized as follows: the CFCCB topology and operation principles are detailed in sections 7.1 and 7.2, respectively. The case study model is explained in section 7.3 and section 7.4 provides the analysis of CFCCB operation. The analysis related to the typical scheme is included in section 7.5. The simulation results are presented and discussed in section 7.6. A comparison between the typical approach and the proposed CFCCB is included in section 7.7 and the chapter is concluded in section 7.8.

7.1 Current Flow Controlling dc Circuit Breaker

The topology of proposed CFCCB is shown in Figure 7.1. The CFCCB has three terminals and can connect a dc bus to two adjacent transmission lines. The CFCCB consists of main breaker (MB_i) units,

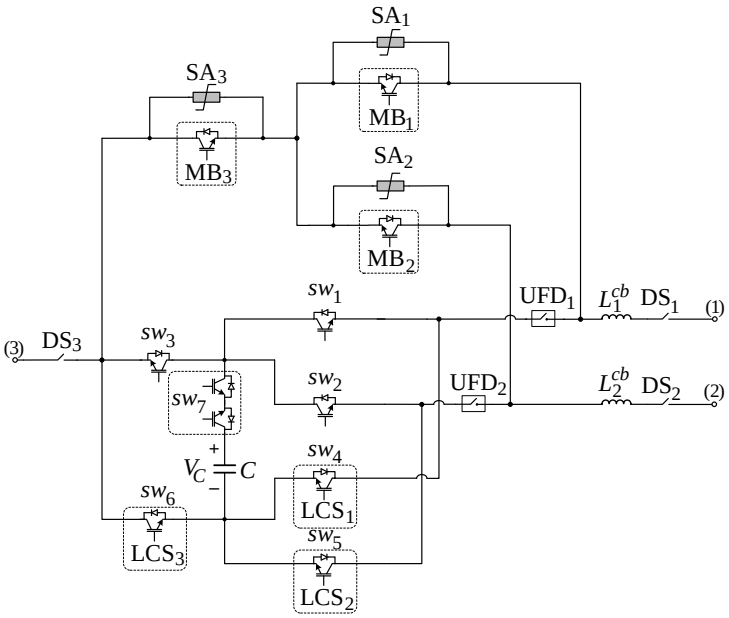


Figure 7.1: Current flow controlling dc circuit breaker topology.

ultra fast disconnectors (UFD_i), surge arresters (SA_i), disconnectors (DS_i), seven semiconductor valves and one capacitor. Moreover (L_1^{cb}) and (L_2^{cb}) are employed as current limiting inductors. The MB units consist of several semiconductor switches with antiparallel diodes in series connection. The semiconductor switches are connected in one direction and hence the MB units are unidirectional. UFD_1-UFD_3 are assumed to be similar to the UFDs in typical HCB [134]. DS_1-DS_3 are standard high voltage disconnectors to provide the electrical isolation after CFCCB action. As shown in Figure 7.1, sw_1-sw_6 together with capacitor C form an interline dual H-bridge CFC with reduced number of switches [226]. However, sw_4-sw_6 are also exploited as load commutation switches (LCSs). Therefore, sw_4-sw_6 are also referred as LCS_1-LCS_3 in this chapter.

7.2 CFCCB Operation Principles

7.2.1 CFC Bypassed Mode

In this mode, the CFCCB does not control the current and only maintain the power flow between the dc bus and the adjacent lines. The equivalent representation of CFCCB in the CFC bypassed mode is depicted in Figure 7.2(a). Note that the semiconductor switches are represented by ideal switches in Figure 7.2. In this mode, sw_1-sw_3 and sw_7 are opened whereas sw_4-sw_6 are closed. DS_1-DS_3 and UFD_1-UFD_2 are closed while MB_1-MB_3 are opened. Is can be seen in the figure, the current can flow between the terminals of CFCCB

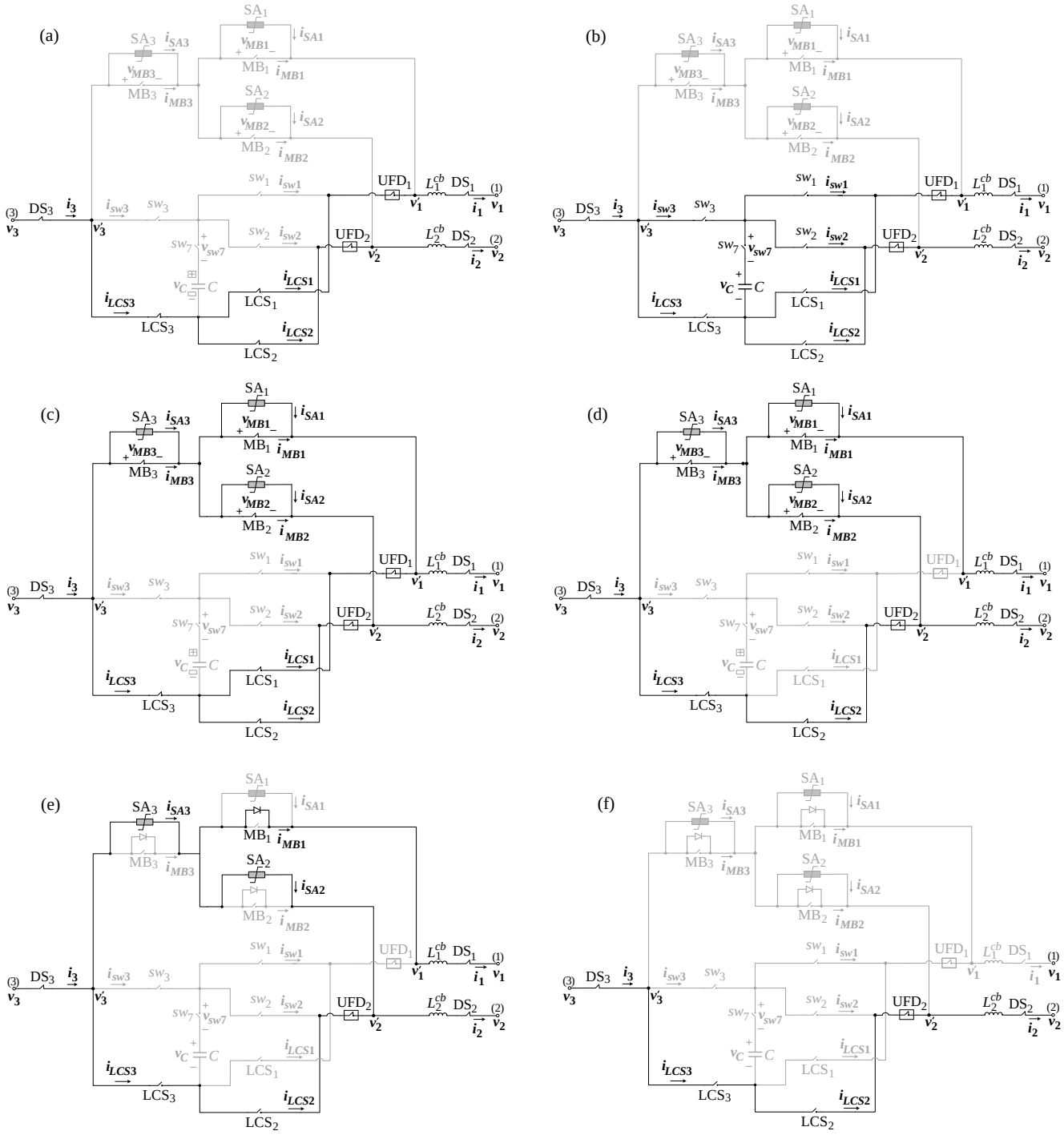


Figure 7.2: Operation stages of current flowing hybrid dc circuit breaker.

irrespective of its direction.

7.2.2 *Active CFC Mode*

The equivalent representation of CFCCB in the active CFC mode is depicted in Figure 7.2(b). In this mode the CFCCB controls the current in one of the adjacent lines by operating its embedded dual H-bridge

CFC. Depending on the current direction, the desired voltage can be generated by selecting a suitable set of states of switches. Table 7.1 illustrates the switching states for both negative and positive currents. The capacitor voltage is represented by V in Table 7.1. The current can be controlled using a PI and second order compensator. The linearized average model of the CFC represented by a couple of voltage sources can be used to design the current control system [22]. The embedded CFC operation modes and control scheme have been extensively investigated in [226] and [22]. As shown in Figure 7.2, i_1, i_2 and i_3 are the currents flowing through terminal 1, 2 and 3 of CFCCB, respectively. Based on the switching states in Table 7.1, i_2 can be controlled only by applying PWM signal to sw_6 assuming the following scenario:

- i_3 is incoming current into the CFCCB and i_2 and i_1 are outgoing currents.
- The currents are positive.

Positive currents						Negative currents					
Set	**sw_1**	**sw_6**	**sw_2**	**V_{31}**	**V_{32}**	**Set**	**sw_3**	**sw_4**	**sw_5**	**V_{31}**	**V_{32}**
1	0	0	0	$-V$	$-V$	**9**	0	0	0	$+V$	$+V$
2	0	0	1	$-V$	0	**10**	0	0	1	$+V$	0
3	0	1	0	0	$-V$	**11**	0	1	0	0	$+V$
4	0	1	1	0	0	**12**	0	1	1	0	0
5	1	0	0	0	0	**13**	1	0	0	0	0
6	1	0	1	0	$+V$	**14**	1	0	1	0	$-V$
7	1	1	0	$+V$	0	**15**	1	1	0	$-V$	0
8	1	1	1	$+V$	$+V$	**16**	1	1	1	$-V$	$-V$

Table 7.1: Switching states for positive and negative current scenarios.

7.2.3 *Fault Mode*

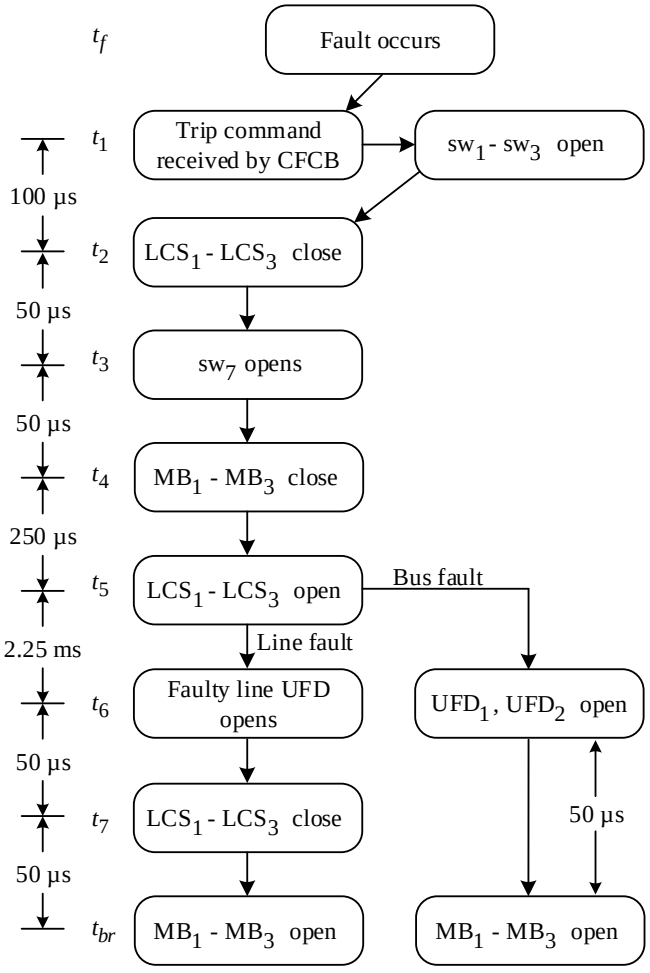
The CFCCB can receive three independent trip commands including two line faults and one dc bus fault trip commands. Upon receiving a trip command the corresponding terminal(s) of CFCCB must interrupt(s) its(their) current(s). Note that the CFCCB may enter to the fault mode either when it operates in the CFC bypassed or in the active CFC modes.

Fault on Adjacent Transmission Line

Assume a permanent short circuit fault happens on the line connected to the terminal 1 of CFCCB. Hence the terminal 1 of CFCCB should trip and interrupt the fault current. It is assumed that the fault incepts at time t_f and the trip command is received by the CFCCB at time t_1. At time t_1, sw_1-sw_3 should be opened and consequently sw_4-sw_6 must be closed at time t_2. This action redirects the fault current path into the LCS units and prevents the capacitor from charging or discharging by reducing its current to zero. Thereafter sw_7 can be opened at time t_3 in zero current to ensure that the capacitor is disconnected from the system. Upon opening of sw_7, MB_1-MB_3 must

be closed at time t_4. The equivalent representation of this stage is shown in Figure 7.2(c). As can be seen in the figure, the fault current is shared between MB and LCS units. At time t_5, sw_4-sw_6 should be opened and commutate the current into the MB units. At this stage, the current in UFD units is almost zero. Therefore, UFD_1 can be opened at time t_6 in order to isolate the terminal 1 of CFCCB (Faulty line corresponding terminal) from the dc bus and the other adjacent line. Consequently, sw_4-sw_6 should be closed at time t_7. Figure 7.2(d) shows the equivalent representation of CFCCB at time t_7. Note that, the current cannot flow through LCS_1 due to the open state of UFD_1. Finally, MB_1-MB_3 opens and redirect the currents into the SA_1-SA_3 at t_{br}. The time period between t_7 and t_{br} is named as current sharing stage. The current in SA_1 will be zero due to the conduction of antiparallel diodes of MB_1. Figure 7.3 illustrates the sequential operation of CFCCB in the line fault mode. The operation sequence for a fault on the line connected to terminal 2 of CFCCB are similar to the explained case. However, in the latter scenario UFD_2 must be opened instead of UFD_1. To provide the electrical isolation, the corresponding terminal disconnector (DS) can be opened.

Figure 7.3: Line and bus faults isolation process.



Fault at dc Bus

Upon detection of a permanent dc bus fault, all adjacent lines must be isolated from the dc bus. The operation sequence for a bus fault interruption is illustrated in Figure 7.3. As it is shown in the figure, the operation sequences for line and bus faults are the same until time t_5. To interrupt a dc bus fault, it is necessary to open both UFD_1 and UFD_2 at time t_6. For the bus fault interruption there is no current sharing stage and MB_1-MB_3 can be directly opened at time t_{br} to interrupt the fault current and redirect it into the surge arresters. Note that the current in SA_3 will be zero due the conduction of the antiparallel diodes of MB_3. The bus fault current interruption is expected to be faster than the line fault scenario due to the lack of current sharing stage. Finally, the electrical isolation can be provided by opening $DS_1 - DS_3$.

Recloser Mode

The recloser mode might be required before completely opening of the CFCCB. The CFCCB can be reclosed by reclosing MB_1-MB_3 after opening the faulty line corresponding UFD. The equivalent circuits of reclosing mode are equal to Figure 7.2(d) and (f). Finally, in case of a non-permanent fault, the faulty line corresponding UFD can be again closed and the CFCCB shifts to its normal conduction state by closing sw_4-sw_6 and opening MB_1-MB_3.

7.3 Case Study Model

The current interruption operation of CFCCB does not depend on the grid topology. Therefore, an average model of a three-terminal meshed grid is selected for performing the analysis and simulation. The three-terminal grid model is shown in Figure 7.4. The transmission lines are modeled using lumped T-equivalent model. The parameters of test system are illustrated in Table 7.2. The analysis and simulations are carried out for both proposed and typical schemes. As illustrated in Figure 7.4, in the typical scheme, a CFC is installed at bus B_1 to regulate the current in line 12. In addition, two HCBs are installed between two adjacent lines (12 and 13) and the CFC. In this study, the HCBs from [134] are considered. A detailed schematic of the HCB is illustrated in Figure 7.5. In the proposed scheme, the CFC and the HCBs are substituted by the CFCCB (see Figure 7.4). The CFC control system is designed based on [22] for both typical and proposed schemes. The parameters of CFC are the same for both mentioned schemes and are illustrated in Table 7.2.

7.4 Analysis

The operation of embedded CFC has been analyzed in [22,226]. Therefore, only the current interruption mode of CFCCB is considered in this section. In order to clarify the differences between the proposed

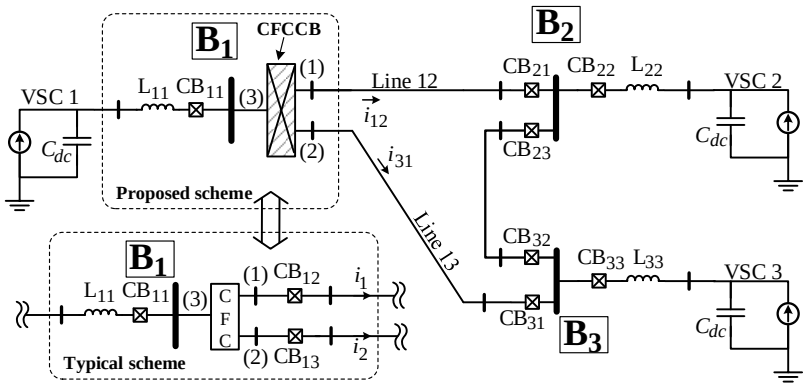


Figure 7.4: Average model of three-terminal grid.

and the typical methods the analysis are simplified by considering the following aspects:

- The permanent dc fault and prompt fault interruption strategy are considered [184,220].
- Voltage at dc buses are assumed to be constant during the dcCB operation time [222].
- Transmission line and dc bus short circuit faults are modeled by a voltage source, whose value is equal to the system steady-state voltage value in normal condition and it changes to 0 V as soon as a fault happens.

Considering the aforementioned assumptions, the grid model can be simplified by eliminating the connection between buses B_2 and B_3. The simplification can be done due to assumed constant dc bus voltage during the fault condition. The simplified model for analysis is depicted in Figure 7.5.

7.4.1 Impact of the Embedded CFC on the Fault Current

The embedded CFC is composed of six switches with their antiparallel diodes. Due to arrangement of the switches and the capacitor, the CFC cannot block the fault current until the capacitor is charged up to the nominal line voltage. The voltage rating of the capacitor lies in the range of few kilo volts. Therefore, the CFC capacitor must be disconnected from the fault current path to prevent it from being charged or discharged. The capacitor can be retained by opening sw_1-sw_3 while closing sw_4-sw_6 and then opening sw_7. Considering the embedded CFC structure, it can be found out that all the switching states may only change the fault current path inside the CFC and the fault current may charge or discharge the capacitor. Hence, during the fault clearing time period (which lies in range of few milliseconds) the CFC has almost no impact on the fault current. When $0 < t \leq t_2$, the current flows through sw_1-sw_7 depending on their state. Therefore considering the scope of chapter the analysis considers the current equations for $t_2 < t \leq t_{br}$.

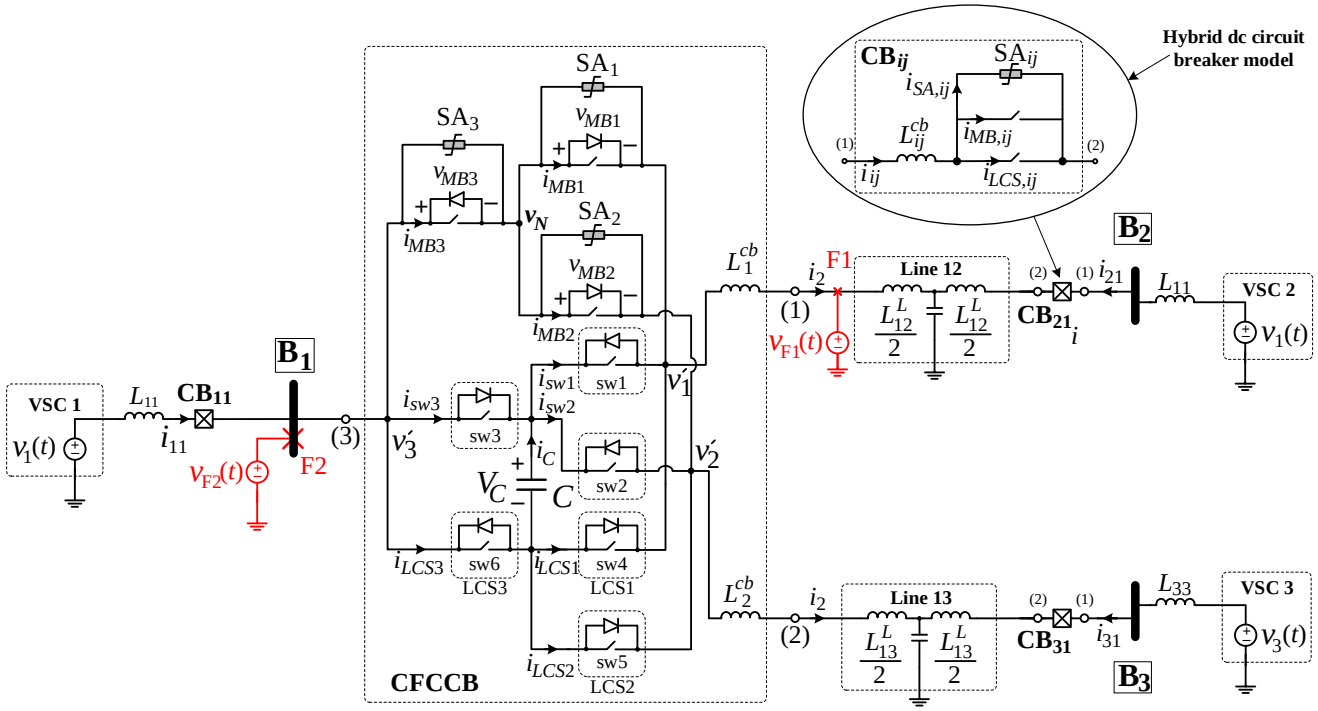


Figure 7.5: Equivalent circuit of test system in presence of CFCCB.

7.4.2 *Transmission Line Fault F_1 and CFCCB*

A low impedance ($R_{fault} \approx 0\,\Omega$) pole-to-ground fault occurs on line 12 at point F_1 at $t = 0$ s. The voltage at fault location (v_{F1}) becomes zero after fault occurs. The following equations can be given considering the initial conditions and assumptions:

$$\begin{aligned} &v_{F1}(0) = V_{dc}, \\ &v_{F1}(0^+) = 0, \\ &v_j(t) = V_{dc}; \quad 0 < t \leq t_{br}, \quad j = 1,2,3, \\ &i_j(0) = I_{pre,j}; \quad j = 1,2,3. \end{aligned} \tag{7.1}$$

In (7.1) $v_{F1}(t)$, $v_j(t)$ and $I_{pre,j}$ represent the voltage at fault location, dc bus B_j voltage and pre-fault current of port j of the CFCCB. t_{br} represents the current interruption instant. The current at port 3 can be given as follows:

$$i_3(t) = \begin{cases} i_{LCS3}(t), & t_2 < t \leq t_5 \\ i_{MB3}(t), & t_5 < t \leq t_7 \\ i_{MB3}(t) + i_{LCS3}(t), & t_7 < t \leq t_{br} \\ i_{SA3}(t) + i_{LCS3}(t), & t_{br} < t \leq t_e \end{cases}, \tag{7.2}$$

and for port 1:

$$i_1(t) = \begin{cases} i_{LCS1}(t), & t_2 < t \leq t_5 \\ i_{MB1}(t), & t_5 < t \leq t_7 \\ i_{MB1}(t), & t_7 < t \leq t_{br} \\ i_{SA1}(t), & t_{br} < t \leq t_e \end{cases}, \tag{7.3}$$

and for port 2:

$$i_2(t) = \begin{cases} i_{LCS2}(t), & t_2 < t \leq t_5 \\ i_{MB2}(t), & t_5 < t \leq t_7 \\ i_{MB2}(t) + i_{LCS2}(t), & t_7 < t \leq t_{br} \\ i_{SA2}(t) + i_{LCS2}(t), & t_{br} < t \leq t_e \end{cases}. \tag{7.4}$$

We replace the sum of half of line $1j$ inductance (L_{1j}^{L}) and corresponding port current limiting inductor value (L_{j-1}^{cb}) by L'_{1j}:

$$\begin{aligned} &L'_{1j} = L_{j-1}^{cb} + \frac{1}{2}L_{1j}^{L} \quad for \quad j = 1,2 \\ &L'_{11} = L_{11} + L_{11}^{cb}. \end{aligned} \tag{7.5}$$

Therefore, considering the impact of transmission line lumped T-equivalent model capacitance during the short fault clearing time period, the initial rate of rise of current at port 1, which is equal to that of fault current can be given by:

$$\frac{\mathrm{d}i_1(0^+)}{\mathrm{d}t} = \frac{V_{dc}}{\left((L'_{11} \parallel L'_{13}) + L_1^{cb} + L_{12}^{f}\right)} \tag{7.6}$$

where L_{12}^{f} represents the inductance between the CFCCB and the fault location. The current derivative at the other ports of CFCCB can be given as:

$$\begin{aligned} \left|\frac{\mathrm{d}i_2(0^+)}{\mathrm{d}t}\right| &= \frac{L'_{11}}{(L'_{11} + L'_{13})}\left|\frac{\mathrm{d}i_1(0^+)}{\mathrm{d}t}\right|, \\ \left|\frac{\mathrm{d}i_3(0^+)}{\mathrm{d}t}\right| &= \frac{L'_{13}}{(L'_{11} + L'_{13})}\left|\frac{\mathrm{d}i_1(0^+)}{\mathrm{d}t}\right|. \end{aligned} \tag{7.7}$$

The current in MB and LCS units can be obtained using (7.2)-(7.4), (7.6) and (7.7).

Main Breaker (MB) Units

When $t_4 < t < t_{br}$ MB_1-MB_3 are closed. Therefore, assuming instantaneous current commutation at $t = t_5$ the current in MB_1 can be given as:

$$i_{MB1}(t) = I_{pre,1} + \left|\frac{\mathrm{d}i_1(0^+)}{\mathrm{d}t}\right| t \tag{7.8}$$

The maximum current in MB_1 (I_{max}^{MB1}) happens at $t = t_{br}$. The current in MB_2 and MB_3 when $t_4 < t < t_7$ can be given by:

$$i_{MBi}(t) = I_{pre,i} + sgn(i - 2.5)\left|\frac{\mathrm{d}i_i(0^+)}{\mathrm{d}t}\right| t; \quad i = 2,3. \tag{7.9}$$

The maximum current in MB_2 and MB_3 is reached at $t = t_7$. When $t_7 < t < t_{br}$, the current is shared between two mentioned MBs and their current will be decreased.

Load Commutation Switch (LCS) Units

As was explained, the LCS switches conduct the current in two periods of time: i) $t_2 < t < t_5$ ii) $t_7 < t < t_{br}$. In the first stage (when $t_2 < t < t_5$), the current in LCS_j for $j = 1$ and for $j = 2, 3$ holds the same equations as (7.8) and (7.9), respectively. The maximum current in the first stage in the LCS units happens at $t = t_5$. The second maximum of current in the LCS units occurs at time t_{br}. Figure 7.2(d) shows the equivalent circuit of the CFCCB when $t_5 < t \leq t_{br}$. The MBs have several IGBTs in series whereas the LCSs have only few IGBTs. The on-state voltage drop on an MB can be hundred times larger than the on-state voltage drop of an LCS. Hence, the voltage drop on the LCSs can be neglected against that of MB units. Therefore, the following equation can be given considering Figure 7.2(d):

$$v_2' \approx v_3' \tag{7.10}$$

v_1'-v_3' are illustrated in Figure 7.2. Based on (7.10), MB_2, MB_3 can be considered as parallel branches during the mentioned time period and their currents will be almost equal. The absolute value of current in MB_j at $t = t_7^+$ can be given by:

$$\left|i_{MBj}\left(t_7^+\right)\right| = \frac{\left|i_{MB3}\left(t_7^-\right)\right| + \left|i_{MB2}\left(t_7^-\right)\right|}{2}; \quad j = 2, 3 \tag{7.11}$$

Using (7.2), the current in LCS_n can be given as follows:

$$i_{LCS3}\left(t_7^+\right) = i_{LCS1}\left(t_7^+\right) = \frac{\left|i_{MB3}\left(t_7^-\right)\right| - \left|i_{MB2}\left(t_7^-\right)\right|}{2} \tag{7.12}$$

The time $t_{br} - t_7$ lies in the range of tens of microseconds. However, using the obtained current derivative in (7.6), the second maximum of current in LCS_j for $j = 2, 3$ can be obtained as:

$$I_{max2}^{LCSj} = i_{LCSj}\left(t_7^+\right) + \frac{\mathrm{d}i_1\left(0^+\right)}{\mathrm{d}t} \cdot \frac{t_{br} - t_7}{2} \tag{7.13}$$

Surge Arresters (SA)

Similar to chapter 6 SA's parameters are approximated by assuming its voltage to be constant until its current falls to zero for both proposed and typical schemes. Neglecting the practical mismatch between $V - I$ characteristics of surge arresters, the current can be given as:

$$\begin{aligned} \left|i_{SAj}\right| &= \left|\frac{i_{MB1}}{2}\right|; \quad j = 2, 3 \\ \left|i_{SA1}\right| &= 0, \end{aligned} \tag{7.14}$$

The current in SA_1 is zero due to the conduction of antiparallel diodes in MB_1. Considering (7.10) it can be assumed that SA_2 and SA_3 operate in parallel connection. The rated voltage of each surge arrester is assumed to be equal to V_r. The transient interruption voltage across MB_2 and MB_3 can be given by:

$$TIV = V_{dc} + \left((L_{11}' \parallel L_{13}') + L_1^{cb} + L_{12}^{f}\right)\frac{I_{max}^{MB1}}{t_e - t_{br}} \tag{7.15}$$

The current in SA reaches zero when its voltage falls below its rated voltage. The maximum required time for SA current to fall to zero ($t_e - t_{br}$) can be given as:

$$(t_e - t_{br}) \leq \left((L'_{11} \parallel L'_{13}) + L_1^{cb} + L_{12}^{f} \right) \frac{I_{max}^{MB1}}{V_r - V_{dc}}, \tag{7.16}$$

The maximum absorbed energy in all the surge arresters holds:

$$E_{SA,T} = \int_{t_{br}}^{t_e} V_r \cdot i_1(t)\, dt \tag{7.17}$$

Consequently, the maximum absorbed energy in SA_j can be given as:

$$\begin{aligned} E_{SAj} &= \frac{V_r I_{max}^{MB1} (t_e - t_{br})}{4}; \quad j = 2,3, \\ E_{SA1} &= 0. \end{aligned} \tag{7.18}$$

7.4.3 dc Bus Fault F_2 and CFCCB

As shown in Figure 7.5, a low impedance pole-to-ground fault ($R_{fault} \approx 0\ \Omega$) occurs at dc bus B_1 at time 0 s. The initial conditions and study assumptions are similar to (7.1) and also similar approach to subsection 7.4.2 is used for analysis. The current at port j for various time periods can be given by:

$$i_j(t) = \begin{cases} i_{LCSj}(t), & t_2 < t \leq t_5 \\ i_{MBj}(t), & t_5 < t \leq t_{br} \\ i_{SAj}(t), & t_{br} < t \leq t_e \end{cases} \quad ; \quad j = 1,2,3 \tag{7.19}$$

The current derivative at ports of CFCCB can be given by:

$$\begin{aligned} \frac{\mathrm{d}i_3(0^+)}{\mathrm{d}t} &= V_{dc} \frac{L'_{12} + L'_{13}}{L'_{12} L'_{13}}, \\ \left| \frac{\mathrm{d}i_i(0^+)}{\mathrm{d}t} \right| &= \frac{V_{dc}}{L'_{1(i+1)}}; \quad i = 1,2. \end{aligned} \tag{7.20}$$

Main Breaker (MB) Units

The currents in MB units when $t_5 < t \leq t_{br}$ can be given as:

$$i_{MBi}(t) = \begin{cases} I_{pre,i} - \frac{V_{dc}}{L'_{1(i+1)}} t; & i = 1,2 \\ I_{pre,i} - V_{dc} \frac{L'_{12} + L'_{13}}{L'_{12} L'_{13}} t; & i = 3 \end{cases} \tag{7.21}$$

The maximum current in MB_j (I_{max}^{MBj}) is reached at $t = t_{br}$.

Load Commutation Switch (LCS) Units

Despite the line fault scenario, the current in LCS units has one maximum at $t = t_5$ and can be given as:

$$I_{max}^{LCSi}(t) = \begin{cases} I_{pre,i} - \frac{V_{dc}}{L'_{1(i+1)}} t_5; & i = 1,2 \\ I_{pre,i} - V_{dc} \frac{L'_{12} + L'_{13}}{L'_{12} L'_{13}} t_5; & i = 3 \end{cases} \tag{7.22}$$

Surge Arresters (SA)

The SA current can be given as:

$$\begin{aligned} |i_{SAj}| &= \left|\frac{i_{MB3}}{2}\right|, \quad j = 1,2 \\ |i_{SA3}| &= 0. \end{aligned} \tag{7.23}$$

Depending on the length of adjacent lines, the absorbed energy in the surge arresters of the CFCCB and also the energy absorption time ($t_{ej} - t_{br}$) can be different for each surge arrester. The range of energy absorption time can be given as:

$$t_{ej} - t_{br} \leq \frac{L'_{1(j+1)} I_{max}^{MBj}}{V_r - V_{dc}}, \quad j = 1,2 \tag{7.24}$$

where t_{ej} is the time when the current in SA_j becomes zero. Due to conduction of antiparallel diode D_3, the current in SA_3 remains zero and consequently the absorbed energy in SA_3 is also zero. The absorbed energy in SA_j can be given by:

$$E_{SAj} = \frac{V_r I_{max}^{MBj} \left(t_{ej} - t_{br}\right)}{2}, \quad j = 1,2 \tag{7.25}$$

7.5 Typical scheme

In the typical scheme, after receiving a trip command by the corresponding HCB at time t_1, its MB unit is closed. Thereafter, the LCS unit opens at time t_2 and consequently MB unit opens at time t_3 [139]. Similar line and bus fault scenarios to subsection 7.4.2 to subsections 7.4.2 and 7.4.3 are considered. For sake of brevity, only the most relevant equations are included in this section.

7.5.1 Transmission Line Fault and HCB

Load Commutation Switch (LCS) Units

The LCS current in CB_{12} reaches its maximum at $t = t_2$ whereas the current in LCS unit of CB_{13} reaches its maximum at $t = t_{br}$. The maximum current in LCS unit of CB_{12} can be given by:

$$I_{max}^{LCS12}(t) = I_{pre,12} + \left|\frac{\mathrm{d}i_{12}(0^+)}{\mathrm{d}t}\right| t_2 \tag{7.26}$$

and for LCS unit of CB_{13}:

$$I_{max}^{LCS13}(t) = I_{pre,13} - \left|\frac{\mathrm{d}i_{13}(0^+)}{\mathrm{d}t}\right| t_{br} \tag{7.27}$$

Main Breaker (MB) Units

It is assumed that only the MB unit of corresponding HCB of the faulty line is activated. Therefore, the current in MB units of other

HCBs remain zero. The current in MB unit of CB_{12} for $t_2 < t \leq t_{br}$ can be given as:

$$I_{max}^{MB12}(t) = I_{pre,12} + \left| \frac{\mathrm{d}i_{12}(0^+)}{\mathrm{d}t} \right| t \tag{7.28}$$

The maximum current in the MB unit in CB_{12} (I_{max}^{MB12}) is reached at time t_{br}.

Surge Arresters (SA)

The currents in surge arresters of all the HCBs are zero except the faulty line HCB (SA_{12}). The absorbed energy in the surge arrester can be given by:

$$E_{SA12} = \frac{V_r I_{max}^{MB12}(t_e - t_{br})}{2} \tag{7.29}$$

7.5.2 dc Bus Fault and HCB

Load Commutation Switch (LCS) Units

During the bus fault, all the adjacent HCBs of the faulty dc bus are activated. The maximum current in the LCS unit of all adjacent HCBs (I_{max}^{LCS1i}) can be given as:

$$I_{max}^{LCS1i} = I_{pre,1i} - \frac{V_{dc}}{L'_{1i}} t_2; \quad i = 2,3 \tag{7.30}$$

Main Breaker (MB) Units

The currents of MB units for $t_2 < t \leq t_{br}$ can be given as:

$$i_{MB1i}(t) = I_{pre,1i} - \frac{V_{dc}}{L'_{1i}} t; \quad i = 2,3 \tag{7.31}$$

The maximum current in the MB unit (I_{max}^{MB1i}) is reached at $t = t_{br}$.

Surge Arresters (SA)

The absorbed energy in SA_{1j} can be given by (7.32).

$$E_{SA1j} = V_r I_{max}^{MB1j}\left(t_{ej} - t_{br}\right), \quad j = 2,3 \tag{7.32}$$

7.6 Simulation Results

In this section the simulation results of the three-terminal grid (Figure 7.4) for line 12 and dc bus fault scenarios are presented and compared to the obtained numerical values from the analysis of simplified grid model in section 7.4. The simulations are carried out using PSCAD. The non-linear $V - I$ characteristic of surge arresters are also considered. The transmission lines are protected by standard overcurrent protection scheme. The line fault trip command is sent to the CFCCB or the corresponding HCB when the line current exceeds 2.8 kA. The dc buses are protected by the differential protection scheme. In this

Table 7.2: Three-terminal test grid and CFC parameters.

Transmission Lines Parameters			
Lumped T-model Parameters	R [Ω/km]	L [mH/km]	C [μF/km]
	0.01105	3.245	0.382
Length [km]	Line 12	Line 13	Line 23
	200	300	200
VSC Parameters			
Bus	**1**	**2**	**3**
Capacitance [μF]	1000	1000	1000
Power [MW]	600	-	-
V_i^* [kV]	-	300	300
Droop Constant k_i [A/V]	-	0.05	0.5
Voltage [kV]	320	320	320
Filter reactor [mH]	10	10	10
CFC Parameters			
Nominal Voltage [kV]	4		
Capacitor [mF]	10		
Switching Frequency [kHz]	2		
PI	$0.012 + \frac{0.398}{s}$		
Compensator	$\frac{0.3421s^2+1.2978s+21.5213}{s^2+120.5323s+3207.9071}$		
Filter	$\frac{1}{0.08s+1}$		

scheme, when the sum of incoming and outgoing currents at a dc bus becomes non-zero, the dc bus trip signal is activated. The parameters of three-terminal grid and CFC are illustrated in Table 7.2.

7.6.1 Power Flow

The currents flowing from the dc bus and the transmission lines in presence of the CFCCB are depicted in Figure 7.7. Figure 7.7(a), (b) and (c) depict the currents for dc bus B_1, line 13 and 12 fault scenarios, respectively. The CFCCB operates in CFC bypassed mode for $0 < t < 2$ s. Thereafter the CFCCB changes its operation mode to active CFC mode at time $t_{CFC} = 2$ s. The CFCCB regulates the current in line 12 and increases its flowing current from 1.125 kA to 1.416 kA. Consequently, the current in line 13 decreases to 443 A. In all scenarios, the fault happens at time $t_f = 5$ s. The behavior of CFCCB has been found out to be similar to the typical scheme during normal operation and fault condition from the grid point of view.

7.6.2 Transmission Line Fault

To consider the most sever scenario, a low impedance pole-to-ground fault (100 mΩ) is placed very close to the CFCCB (distance from CFCCB is equal to 0 km.) on line 12 at $t = 0$ s. In the typical approach CB_{12} and CB_{21} and in case of the proposed CFCCB, CB_{21} and port 1 of the CFCCB should trip. Figure 7.8 and Figure 7.9 show different waveforms for the proposed and typical schemes, respectively.

The important numerical values obtained from simulation and analysis are also illustrated in Table 7.3. The interrupted current in the CFCCB is almost 5% larger than the interrupted current in the typical scheme due to the additional time that is considered in the

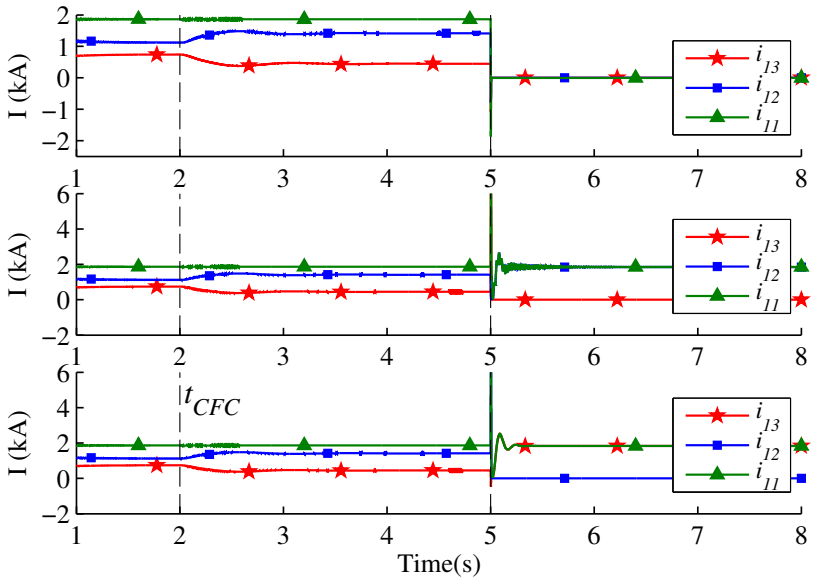


Figure 7.6: Transmission lines and dc bus currents in presence of HCB and dual H-bridge CFC during fault at: a) dc bus B_1, b) line 13, c) line 12.

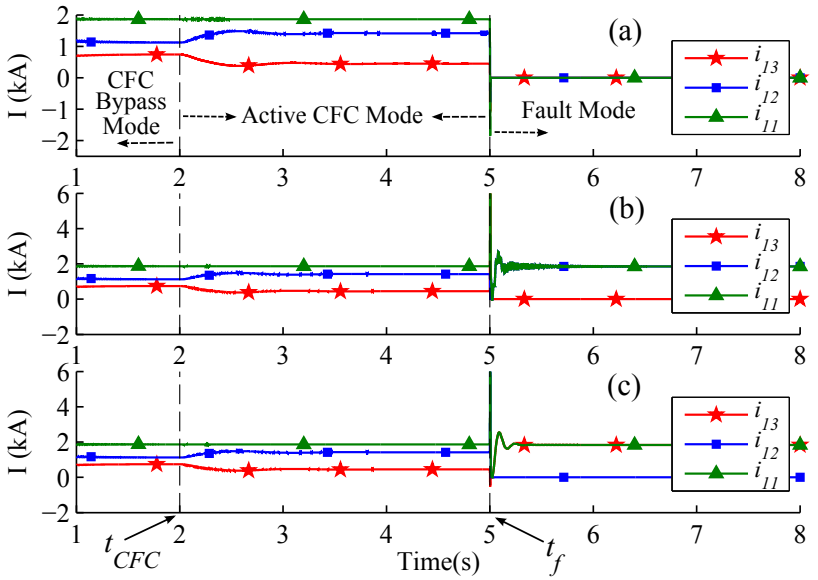


Figure 7.7: Transmission lines and dc bus currents in presence of CFCCB during fault at: a) dc bus B_1, b) line 13, c) line 12.

modeling of current sharing stage in the CFCCB. As shown in Figure 7.8(b) and Figure 7.9(b), the current in sw_1-sw_3 in both schemes are almost equal. However, a large difference in the current of sw_4-sw_6 can be observed in Figure 7.8(c) and Figure 7.9(c). The absolute value of current in sw_4 and sw_6 in the typical scheme reaches almost 10 kA whereas in sw_5 and sw_6 in the proposed scheme does not exceed 5 kA.

Figure 7.8(d) depicts the CFCCB capacitor voltage and current and also the voltage across sw_7. The absolute value of voltage across sw_7 does not exceed 2.5 kV. As shown in Figure 7.8(f) and Figure 7.9(f), the fault current is redirected into two surge arresters (SA_2 and SA_3) in CFCCB whereas it is handled by one surge arrester in the typical method.

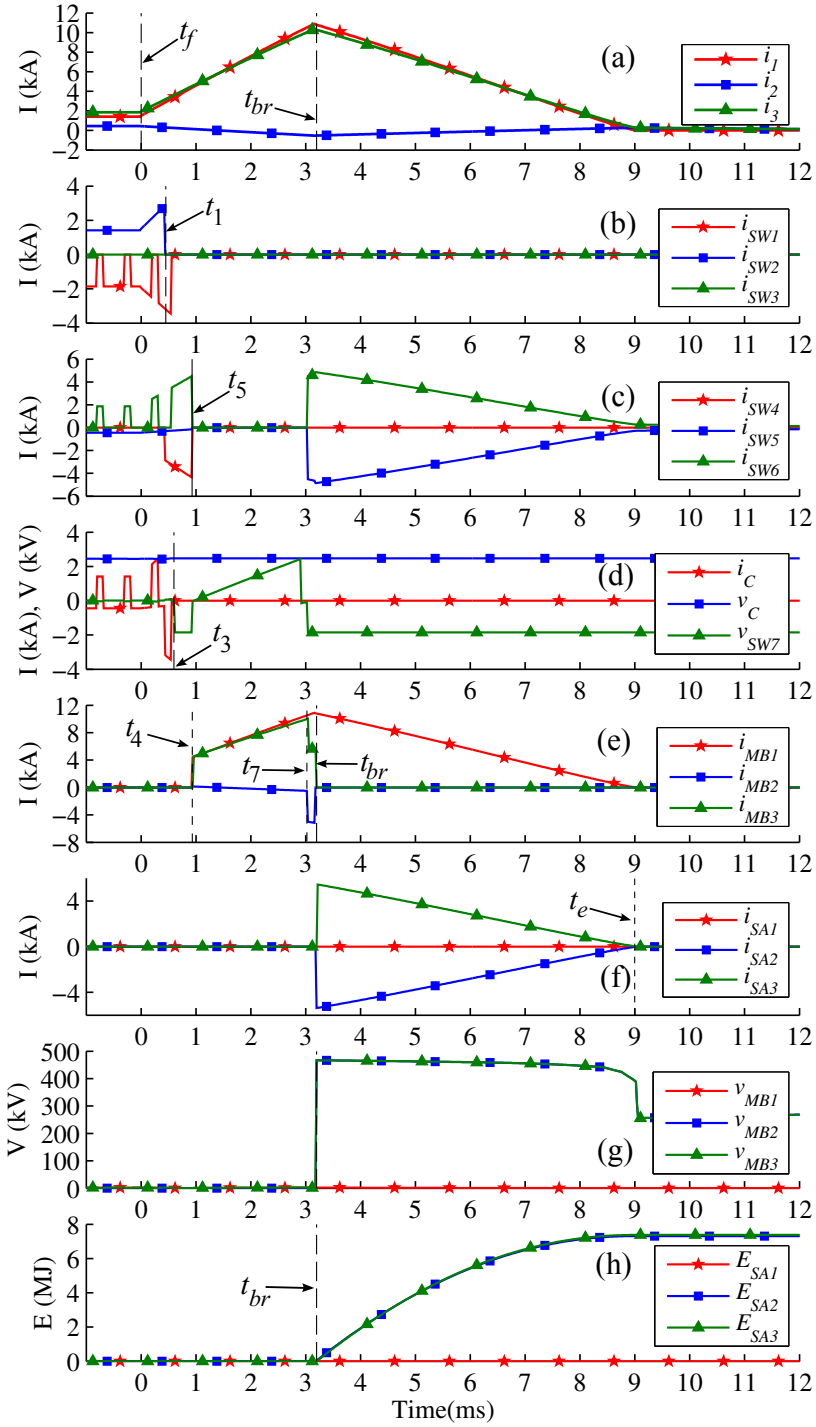


Figure 7.8: CFCCB waveforms for a permanent fault on line 12.

Since the rated voltage of surge arresters in CFCCB are equal to that of HCBs, the maximum voltage across MB units in both methods are equal (Figure 7.8(g) and Figure 7.9(g)). Figure 7.8(h) and Figure 7.9(h) show the absorbed energy in the surge arresters in both methods. The amount of absorbed energy in each surge arrester in the CFCCB reaches almost 7.2 MJ whereas it reaches approximately 14 MJ in the typical scheme.

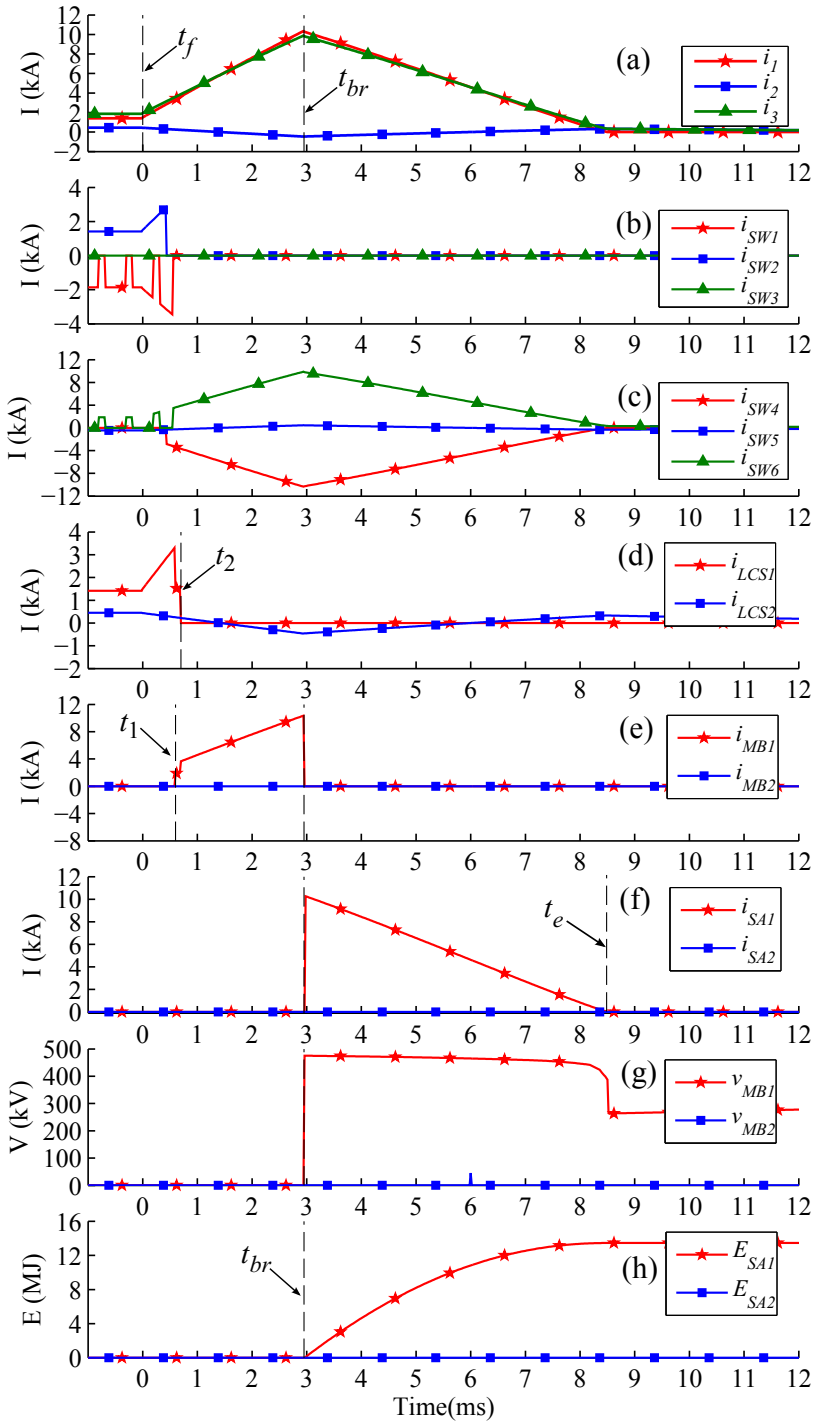


Figure 7.9: Typical scheme waveforms for a permanent fault on line 12.

Table 7.3: CFCCB and HCB parameters during line fault.

Parameters	CFCCB		HCB	
CFCCB (HCB)	Analysis	Simulation	Analysis	Simulation
$I_{max1}^{LCS1}(I_{max}^{LCS12})$ [kA]	4.18	4.28	3.20	3.28
I_{max2}^{LCS1}[kA]	4.48	4.62	-	-
$I_{max}^{MB1}(I_{max}^{MB12})$[kA]	11.10	10.9	10.43	10.33
$E_{SA1}(E_{SA12})$[MJ]	0	0	16.98	13.69
$E_{SA2}(E_{SA13})$[MJ]	8.99	7.31	0	0
E_{SA3}[MJ]	8.99	7.38	-	-

The results confirm that the absorbed energy in the surge arrester in the typical scheme is almost equal to twice the absorbed energy in each surge arrester in the proposed scheme.

7.6.3 *dc Bus Fault*

A low impedance pole-to-ground fault (100 mΩ) is placed at bus B_1. In the typical scheme CB_{11}, CB_{12} and CB_{13} and in the proposed scheme CB_{33} and all the ports of CFCCB should trip. Figure 7.10 and 7.11 depict the results for the proposed and the typical schemes, respectively.

The most relevant numerical values obtained from analysis and simulation are illustrated in Table 7.4. The obtained approximated values from analysis are close to the values obtained from simulation. Figure 7.10(a) and 7.11(a) show that the behavior of both schemes from system point of view are similar. As can be seen in Figure 7.10(b) and 7.11(b) the current in sw_1-sw_3 for both schemes are equal. Figure 7.10(c) and 7.11(c) show that the current in sw_4-sw_6 in the typical scheme may reach higher values as compared to the proposed scheme. The maximum current in MB_{12} and MB_1 and also in MB_{13} and MB_2 are equal (see Figure 7.10(e) and 7.11(e)).

The absolute value of current in MB_3 of CFCCB reaches almost 1.8 kA, which is higher than the current in MB units of CB_{12} and CB_{13}. However, this does not necessarily mean that the antiparallel diodes of MB_3 should to be rated for higher current than the antiparallel diodes of MB_1 and MB_2. In fact, MB_1 and MB_2 may be required to carry higher currents during a line fault and should be rated for that.

Figure 7.10(f) and 7.11(f) illustrate that the maximum current in the surge arresters of both schemes are equal. In contrary with MB_1 and MB_2, the current in MB_3 does not redirected to the surge arrester due to explained reason in section 7.4. The absorbed energy in the surge arresters in the CFCCB and the typical scheme are depicted in Figure 7.10(h) and 7.11(h), respectively.

Parameters	**CFCCB**		**HCB**	
CFCCB (HCB)	**Analysis**	**Simulation**	**Analysis**	**Simulation**
$I_{max}^{LCS1}(I_{max}^{LCS12})$ [kA]	-0.96	-0.98	-1.19	-1.24
$I_{max}^{LCS2}(I_{max}^{LCS13})$ [kA]	-0.133	-1.151	-0.29	-0.33
I_{max}^{LCS3} (-) [kA]	-1.103	-1.13	-	-
$I_{max}^{MB1}(I_{max}^{MB12})$ [kA]	-0.933	-0.81	-0.75	-0.78
$I_{max}^{MB2}(I_{max}^{MB13})$ [kA]	-1.19	-1.056	-1.059	-1.06
I_{max}^{MB3} (-) [kA]	-2.12	-1.84	-	-
$E_{SA1}(E_{SA12})$ [MJ]	0.534	0.442	0.452	0.406
$E_{SA2}(E_{SA13})$ [MJ]	1.249	0.995	1.056	0.941
E_{SA3} [MJ]	0	0	-	-

Table 7.4: CFCCB and HCB parameters during bus fault.

7.7 *Comparison*

The proposed scheme is compared to the typical scheme in this section. As shown in Figure 7.4, to fully protect a dc bus with 2

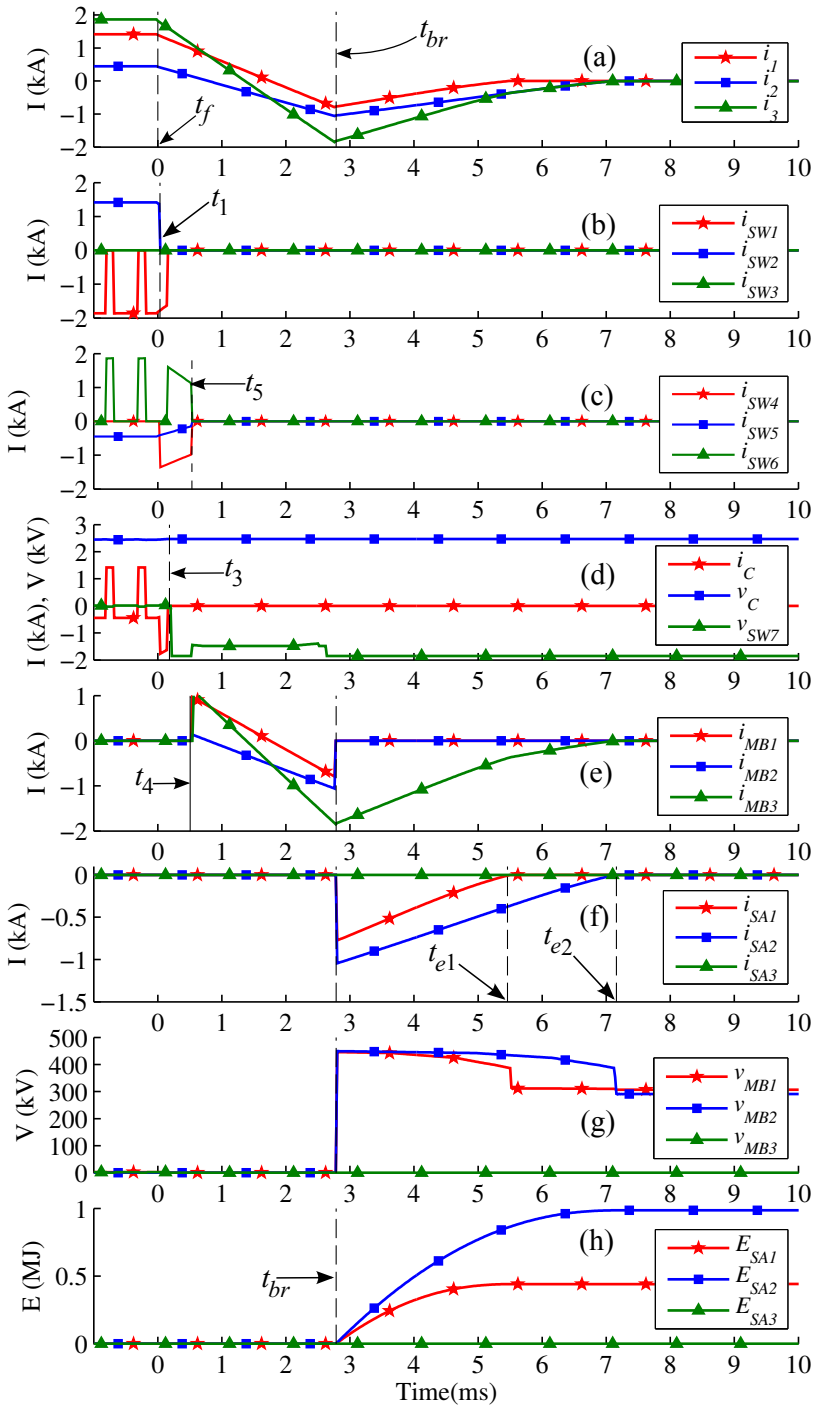


Figure 7.10: CFCCB waveforms for fault at bus B_1.

adjacent lines and one converter station with an asymmetric monopole HVdc configuration, 3 HCBs are required in the typical scheme. The number of HCBs can be doubled in symmetric monopole and bipole configurations.

Although the comparison study is done for asymmetric monopole configuration, it is valid for other mentioned configurations. The HCBs and the CFC can be replaced by the CFCCB. The converter station HCB (CB_{11}) will not be removed. Therefore, the requirements

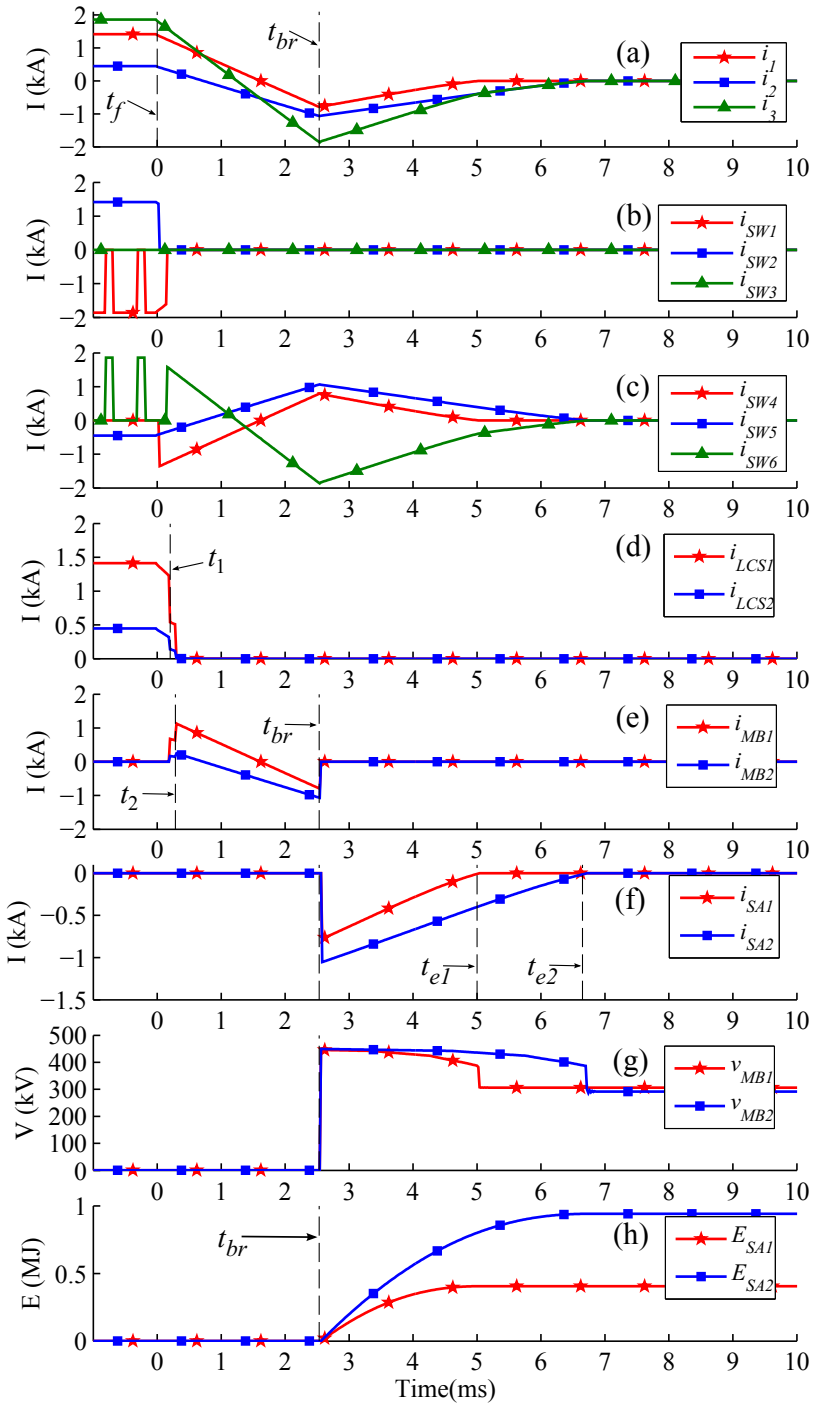


Figure 7.11: Typical scheme waveforms for fault at bus B_1.

of CB_{11} in both cases are equal and will not be compared and included in calculations. Table 7.5 compares different aspects of both the proposed and typical devices assuming $t_6 \approx t_{br}$.

7.7.1 CFC

The CFC can be bypassed during the fault either by the explained method in 7.4.1 or using bypass valves. Considering the method from 7.4.1 sw_4-sw_6 are required to carry the fault current till the

Table 7.5: CFCCB and HCB based Methods parameter comparison.

Parameter	HCB	CFCCB
Number of UFDs	2	2
Number of limiting ind.	2	2
Number of surge arresters	2	3
Surge arresters energy	E	$\frac{E}{2}$
Surge arresters voltage	V_r	V_r
Number of IGBTs in LCS	$2N_{LCS}$	0
Number of IGBTs in MB	$\frac{2V_r}{V_{CES}}$	$\frac{3V_r}{2V_{CES}}$

corresponding HCBs interrupt the fault (at time t_{br}). In contrary, the same switches in the embedded CFC of CFCCB are only required to carry the fault current till the the LCS units are opened (at time t_5). In addition, sw_4-sw_6 are closed at time t_7 and share the fault current with the MB units in the line fault scenario. Comparing (7.30) and (7.13) imply that sw_4-sw_6 should be rated for higher current in the typical scheme than the proposed scheme.

Load Commutation Switches

The CFCCB uses sw_4-sw_6 of the embedded CFC as the LCSs. In fact, CFCCB saves all the IGBTs, which are required for implementing the LCS units (N_{LCS}) in the HCBs. The maximum current in LCS unit of HCB_{1j} is equal to the first maximum current in LCS_j of CFCCB for the line fault scenario. Depending on the grid topology, the second maximum current in LCS units of CFCCB might be greater as compared to the typical HCB. During the dc bus fault condition the current in LCS_2 and LCS_3 of CFCCB are equal to the current in LCS units of HCB_{11} to HCB_{12}. The current in LCS_1 is equal to sum of currents in LCS_2 and LCS_3 of CFCCB and therefore is higher than the currents in other units. Note that the current in LCS_1 flows through its antiparallel diodes during the bus fault. Hence, the current rating of the IGBTs are equal.

Main Breaker Units

During the line fault the current in corresponding MB units of the CFCCB and HCB are equal. Similar to the previous subsection, the antiparallel diodes of MB_1 in CFCCB may need to be able to carry higher current as compared to the other units depending on the fault identification time and the grid topology. As it is illustrated in Table 7.5 the typical approach requires larger number of IGBTs in MB units of HCBs as compared to the proposed CFCCB. V_{CES} represents the collector-emitter blocking voltage of IGBTs in Table 7.5.

Surge Arresters

7.7.2 Rated Voltage

The rated voltage for the surge arrester of the HCB would lie in range of $1.4V_{dc} - 1.5V_{dc}$ [138,162]. The rated voltage of surge arresters of CFCCB are also assumed to lie in the same range.

7.7.3 Discharge Current

(7.14) illustrates that the maximum discharge current in the surge arresters of the CFCCB in line fault scenario is almost half of the fault current at the interruption instance. However, the maximum discharge current in the surge arrester in typical HCB is almost equal to the interrupted current. Therefore, the maximum discharge current in the surge arresters of the CFCCB is almost 50% smaller than that of the typical scheme.

7.7.4 Energy

Transmission Line Fault

In the typical scheme and during the line fault, only the faulty line HCB interrupts the current and its surge arrester absorbs the energy. When using the CFCCB the faulted line corresponding surge arrester does not absorb the energy and the energy absorption is shared between 2 surge arresters. Using (7.18) and (7.29) and assuming identical current at the interruption instant in both schemes the ratio of total absorbed energy in both schemes can be given as:

$$\frac{E_{SA,T}^{CFCCB}}{E_{SA,T}^{HCB}} = \frac{1}{2} \tag{7.33}$$

where $E_{SA,T}^{CFCCB}$ and $E_{SA,T}^{HCB}$ represents the total absorbed energy in the surge arresters of CFCCB and HCB, respectively. (7.33) implies that the energy rating of surge arresters in CFCCB is almost 50% smaller than that of HCB.

dc Bus Fault

The CFCCB performance during the dc bus fault was found to be similar to the typical method. Therefore, equal amount of energy is absorbed in the surge arresters in both schemes.

7.7.5 Ultra-Fast Disconnector

Each HCB has an ultra-fast disconnector (UFD). As shown in Figure 7.1, the CFCCB has 2 UFDs. Therefore, there is no difference in number of required UFD units for both typical and the proposed schemes.

7.7.6 Current Limiting Inductors

The number of current limiting inductors in both schemes are identical. Also, the inductances of current limiting inductors for the proposed and typical devices are equal.

7.8 Conclusion

In this chapter, a novel current flow controlling dc circuit breaker (CFCCB) has been proposed and analyzed. The proposed CFCCB has three ports and can connect a dc bus to two adjacent transmission lines. Each port of the CFCCB can interrupt its current, independent of the other ports and irrespective of the current direction. Furthermore, the proposed device possesses an embedded interline dual H-bridge current flow controller (CFC), which can regulate the current in one of the adjacent transmission lines.

While the proposed device shows similar behavior compared to the typical scheme from the system level view, it can reduce the requirements of different elements of system. The analysis and simulations imply that the proposed CFCCB requires fewer IGBTs compared to the typical approach. For a dc bus with two adjacent transmission lines, CFCCB needs at least 25% fewer IGBTs as compared to the typical scheme.

Moreover, the proposed device requires smaller size surge arresters due to the less energy absorption in its surge arresters. In addition, the maximum current discharge in the surge arresters in the proposed method is smaller that that of typical method. The results from this study confirm that the energy and discharge current ratings of the surge arresters can be reduced by almost 50%. Considering the improvements by applying the proposed device, its implementation cost is expected to be remarkably lower than the cost of typical scheme.

Part V

Conclusions & Future Work

8
Conclusions

Perhaps I shall survive, perhaps not. I have been known as the commander. Wherever I am present or am mentioned, I am the king.

Babak Khorramdin, Azarbaijani (Iranian) Revolutionary Leader, 795-838.

8.1 Surge-less dc Current Interruption

The interruption of dc current causes a large TIV across the current interrupter device due to the presence of inductive elements in the current path. The TIV can be clamped to almost 1.5 pu of the system nominal voltage. Therefore, the dcCB must be designed to withstand at least under the mentioned voltage level. For instance, in an HVdc system with voltage of +320 kV, the dcCB must be rated for 480 kV. The realization of MB unit of such an SSCB or HCB requires series connection of almost 192 IGBTs with $V_{CE,D} = 2.5kV$ in each direction.

A new SSCB topology has been proposed in chapter 3. The proposed topology is named as Current Releasing dc Circuit Breaker. The CRCB does not require surge arrester for limiting its TIV since it does not generate large TIV. Detailed theoretic and computational analysis show that the TIV across the CRCB can be limited below 1.15 in most severe fault current interruption scenarios. The TIV across the CRCB depends on the values of its internal resistor and capacitor. This approach can lead to almost 24% reduction in the TIV across the dcCB. For instance, the number of required IGBTs in the aforementioned dcCB example can be decreased to almsot 147 IGBTs.

In addition, the proposed dcCB is a unidirectional dcCB and employs semiconductor switches only in one direction. Hence, the number of required semiconductor can be halved as compared to the typical SSCB.

Despite expectation, the CRCB interrupt the fault current with lower TIV when the fault is located at the remote end of the transmission line. The results of this study point out that the increase in cable resistance due to the high frequency components of the dc fault current and the skin effect, has a strong impact on the magnitude of TIV across the CRCB. Therefore, the largest TIV across the CRCB is generated when the fault is very close to the CRCB. This is due to the

absence of cable frequency dependent resistance between the CRCB and the fault location.

The CRCB can still operate when its capacitor is 12% undercharged. The CRCB is not sensitive to the variation in the values of internal resistor and capacitor. The functionality of CRCB is examined and validated through implementing a lab-scale prototype. The short circuit test of the prototype confirms the surge-less operation of the CRCB.

Additional circuits with low voltage ratings are included in the CRCB configuration. These circuits guarantee the successful turn-off of the charging and discharging thyristor banks, which is essential in the real applications.

8.2 Unidirectional dc Circuit Breakers

The unidirectional SSCBs and HCBs are technically attractive since they only employ half the number of semiconductor switches required in the MB unit of the typical bidirectional SSCB and HCBs. In addition to the number of semiconductor switches, the number of gate driver circuits, static and dynamic voltage balancing components and snubber circuits can be reduced significantly by applying unidirectional dcCBs. Moreover, the size of cooling system and the complexity of signaling network can be lowered, notably.

However, the main concern regarding the application of unidirectional dcCBs is their inability in interrupting the fault currents in their backward direction as it can be required in a dc bus fault scenario. This thesis suggests a unidirectional protection strategy for MT-HVdc grid in chapter 4. The results of two sets of study on integration of the unidirectional dcCBs into the MT-HVdc grid using the proposed protection strategy confirm that the unidirectional protection strategy can be utilized for protection of the MT-HVdc grid.

Four types of dcCBs are considered in this study including typical bidirectional HCB, unidirectional HCB, typical SSCB and the CRCB. The design procedure of the CRCB is extended to the multi-terminal HVdc grid and formulated. The internal parameters of CRCB are calculated based on the simplified design approach. The HCB based protection system is investigated though two methods for remote dcCB tripping. The considered methods include a communication-based method and an overcurrent-based method. The communication-based method shows better performance as compared to the the overcurrent-based method.

The results of comparison study for different parameters of HCB and UHCB imply that the current rating of HCB and the size of surge arresters are not necessarily different for the bidirectional and unidirectional strategies. In order to avoid blocking of the MMCs at healthy buses, slight increase in HCB limiting inductor size or current rating of MMC's IGBTs might be required.

Both of the mentioned protection schemes show similar performances during dc transmission line faults. The highest transmission

line fault currents are observed when the fault distance from the closest dcCB is around 75 km. This distance depends on the cable characteristics and the protection algorithm response time. The current interruption requirements of UCBs are identified to be similar to those of the BCBs for interrupting possible dc bus fault scenarios.

8.3 Superconducting Fault Current Limiters

The application of superconducting fault current limiters in the meshed HVdc grids can reduce the magnitude of the interrupted current in the dcCBs. The combination of HCB and SFCL has been investigated in the literature considering the slow protection algorithms. However, considering the recent developments in the protection algorithms for the dc grids, the future MT-HVdc grids seems to rely on the fast protection schemes.

This thesis has investigated the application of SFCL in MT-HVdc grids protected by a fast protection scheme. Due to the nonlinear impedance characteristic of SFCL and depending on its transition time and also fault interruption delay, the current may reach higher values than SFCL limiting current, which is not desirable. Therefore, suitable SFCL have to be designed in coordination with the rate of rise of current, fault identification delay and steady-state fault current.

The system analysis implies that the successful fault current limiting in presence of fast protective relaying schemes and fast dc circuit breakers can be done when the maximum impedance of the SFCL is high enough to limit the fault current below the normal interruption current. Additionally, the transition time has to be shorter than the fault current interruption delay to avoid any unwanted current peak during quenching process.

The SFCL can reduce the fault current peak and the size of the current limiting inductor. The impact of reduction in the current limiting inductors on the MMCs have also been considered. The results confirm that the MMCs can operate without self-blocking even during the line endpoint faults.

The reduction in fault current peak and the size of current limiting inductor can reduce the current requirements of the MB unit of the HCB the energy absorption requirement of the surge arresters. The results obtained in chapter 5 show significant reduction in absorbed energy in the surge arresters of HCBs.

A sensitivity analysis has been carried out in order to assess the impacts of transition time and critical current on the performance of current limiting HCB. The sensitivity analysis confirm that decreasing the transition time of SFCL is always advantageous while the critical current of the SFCL should not be reduced more than specific values due to its influence on the fast fault detection scheme. The study in chapter 5 can be considered as requirement identification study for application of the SFCL in future MT-HVdc grids. The results demonstrate that, the SFCLs, which meet the transition time, critical current and maximum impedance requirements can significantly

improves the fast protection system performance, independently of their technology.

8.4 dc Current Interruption Using a Multi-port Device

Although the application of SFCL can reduce the current interruption requirement of the HCB in MT-HVdc grid, it can be still costly due to the additional cost of the SFCL. Therefore, the components requirement reduction studies must be focused on innovative solutions with lower demand for additional components.

As a novel solution, a multi-port dc circuit breaker has been proposed and analyzed in chapter 6 of this thesis. Despite the conventional concept of the circuit breakers, the proposed Mp-HCB has several ports and each port can interrupt the current, independent of the other ports. From operation time point of view, the proposed device has a similar performance compared to the HCB.

The required number of semiconductor switches in MB unit of the proposed Mp-HCB has been reduced significantly. For a dc bus with two adjacent transmission lines, Mp-HCB needs 25% fewer IGBTs as compared to the HCB. The reduction in number of IGBTs can be more notable when the number of adjacent transmission line increases As the number of adjacent lines increases the percentage of saved IGBTs approaches 50%.

Furthermore, the size of surge arresters can be reduced notably in the Mp-HCB due to the less discharge current and lower energy absorption in its surge arresters as compared to the HCB. The results obtained in this thesis confirm that the energy ratings of surge arresters can be reduced by almost 50%. Considering the improvements by applying the proposed device, its implementation cost is expected to be remarkably lower than the cost of typical HCBs.

8.5 dc Current Flow Control and Interruption

In addition to the previously proposed solutions, this thesis investigates the possibility of development of a novel three-port dcCB which can also control the power flow in one of the adjacent transmission lines. The proposed solution is called current flow controlling dc circuit breaker and has been analyzed in chapter 7.

Similar to the Mp-HCB, each port of the CFCCB can interrupt its current, independent of the other ports and irrespective of the current direction. Furthermore, the proposed device possesses an embedded interline dual H-bridge current flow controller, which can regulate the current in one of the adjacent transmission lines.

The CFCCB can reduce the requirements of different elements of system whereas it shows similar performance compared to the typical scheme from the system level view. The analysis and simulations confirm that the proposed CFCCB requires fewer IGBTs compared to the typical approach. For a dc bus with two adjacent transmission lines, CFCCB needs at least 25% fewer IGBTs as compared to the

typical scheme.

Moreover, the proposed device requires smaller size surge arresters due to the less energy absorption in its surge arresters. In addition, the maximum current discharge in the surge arresters in the proposed method is smaller that that of typical method. The results from this study confirm that the energy and discharge current ratings of the surge arresters can be reduced by almost 50%. Considering the improvements by applying the proposed device, its implementation cost is expected to be remarkably lower than the cost of typical scheme.

8.6 Future Work

The research works included in this thesis have paved the way for realization of more research works in the future. The medium voltage implementation of the CRCB proposed in chapter 3 is one of the future works. More details in design of CRCB including novel snubber and voltage balancing circuits and adaptive operation of CRCB for wide range of system parameters will be covered.

A research work considering the impacts of proposed unidirectional protection strategy on backup protection scheme in MT-HVdc grid is desirable. This study will consider different topologies of MT-HVdc grid and will assess the performance of unidirectional strategy in each case. The impacts on the backup protection of each grid topology will be classified and comparison study considering the typical protection strategy will be carried out.

The experimental implementation of Mp-HCB is also proposed as a strongly required future work. Several additional detail theoretic analysis on the current commutation process from ILCS unit into the IMB unit of Mp-HCB will be carried out. Detail prototype design will be done and a test setup representing a multi-terminal grid will be required. Furthermore, cost-benefit and reliability studies of the Mp-HCB will be carried out. The failure modes of Mp-HCB will be identified and an extensive study on multiple fault handling capability of the Mp-HCB will also be done.

Finally, the prototyping of proposed CFCCB is planned as a future work. The CFCCB with its distinguished technical features can be a real player in the future MT-HVdc grid. The implementation of CFCCB demands for a detail study on the current commutation process during the current interruption. The developed prototype can be tested in the prepared test setup for testing the Mp-HCB. In addition, the reliability study of the proposed CFCCB can be a timely study. The failure modes of CFCCB must be identified and its capability in handling simultaneous faults must be assessed.

Bibliography

[1] United States Environmental Protection Agency (EPA). (2017, January) Climate change: Basic information. [Online]. Available: https://www.epa.gov/climatechange/climate-change-basic-information

[2] K. Brysse, N. Oreskes, J. O'Reilly, and M. Oppenheimer, "Climate change prediction: Erring on the side of least drama?" *Global Environmental Change*, vol. 23, no. 1, pp. 327 – 337, 2013.

[3] H.-M. Groscurth, *Long-Term Integration of Renewable Energy Sources into the European Energy System*, 1st ed., ser. Environmental and Resource Economics. Physica-Verlag Heidelberg, 1998.

[4] P. T. Eggleton, *A Short Introduction to Climate Change*, 1st ed. Cambridge University Press, 2012.

[5] J. P. Holdren and P. R. Ehrlich, "Human population and the global environment: Population growth, rising per capita material consumption, and disruptive technologies have made civilization a global ecological force," *American Scientist*, vol. 62, no. 3, pp. 282–292, May 1974.

[6] C. Shuai, L. Shen, L. Jiao, Y. Wu, and Y. Tan, "Identifying key impact factors on carbon emission: Evidences from panel and time-series data of 125 countries from 1990 to 2011," *Applied Energy*, vol. 187, pp. 310 – 325, 2017.

[7] K. Jurczynska and B. Kuang, "Population growth," in *International Encyclopedia of Public Health (Second Edition)*, second edition ed., S. R. Quah, Ed. Oxford: Academic Press, 2017, pp. 533 – 540.

[8] United States National Library of Medicine National Institutes of Health. (2010, June) Population and climate change. [Online]. Available: https://www.ncbi.nlm.nih.gov/pubmed/21553595

[9] L. Li, X. Hong, D. Tang, and M. Na, "GHG emissions, economic growth and urbanization: A spatial approach," *Sustainability*, vol. 8, no. 5, 2016.

[10] United Nations Framework - Convention on Climate Change (UNFCCC) secretariat. (2015, December) Paris agreement, fccc/cp/2015/l.9/rev.1. [Online]. Available: http://unfccc.int/resource/docs/2015/cop21/eng/l09r01.pdf

[11] I. Campos, J. Guerra, J. F. Gomes, L. Schmidt, F. Alves, A. Vizinho, and G. P. Lopes, "Understanding climate change policy and action in portuguese municipalities: A survey," *Land Use Policy*, vol. 62, pp. 68 – 78, 2017.

[12] A. E. de Salamanca, R. Diaz-Sierra, R. M. Martin-Aranda, and M. J. Santos, "Environmental impacts of climate change adaptation," *Environmental Impact Assessment Review*, vol. 64, pp. 87 – 96, 2017.

[13] C. Teotonio, P. Fortes, P. Roebeling, M. Rodriguez, and M. Robaina-Alves, "Assessing the impacts of climate change on hydropower generation and the power sector in portugal: A partial equilibrium approach," *Renewable and Sustainable Energy Reviews*, vol. 74, pp. 788 – 799, 2017.

[14] R. K. de Richter, T. Ming, S. Caillol, and W. Liu, "Fighting global warming by GHG removal: Destroying cfcs and hcfcs in solar-wind power plant hybrids producing renewable energy with no-intermittency," *International Journal of Greenhouse Gas Control*, vol. 49, pp. 449 – 472, 2016.

[15] Working Group III, "Climate change 2014, mitigation of climate change," Intergovernmental Panel on Climate Change, The United States, Technical Report, 2014. [Online]. Available: http://www.ipcc.ch/report/ar5/wg3/

[16] C. Day and G. Day, "Climate change, fossil fuel prices and depletion: The rationale for a falling export tax," *Economic Modelling*, vol. 63, pp. 153 – 160, 2017.

[17] World Resources Institute. (2012) Top 10 emitters in 2012. [Online]. Available: http://www.wri.org/resources/charts-graphs/top-10-emitters-2012

[18] European Environment Agency, EEA. (2015, September) Total greenhouse gas (GHG) emission trends and projections. [Online]. Available: http://www.eea.europa.eu/data-and-maps/indicators/greenhouse-gas-emission-trends-5/assessment

[19] D. Van Hertem, O. Gomis-Bellmunt, and Jun Liang, *HVDC grids for transmission of electrical energy: offshore grids and a future supergrid*, 1st ed., ser. IEEE Press Series on Power Engineering. John Wiley, 2014.

[20] Wind Europe, "The european offshore wind industry - key trends and statistics 2016," Siemens AG, Germany, Technical Report, January 2017. [Online]. Available: https://windeurope.org/about-wind/statistics/offshore/european-offshore-wind-industry-key-trends-and-statistics-2016/

[21] N. Chaudhuri, B. Chaudhuri, R. Majumder, and A. Yazdani, *Multi-terminal direct-current grids: Modeling, analysis, and control*. John Wiley & Sons, 2014.

[22] J. Sau-Bassols, E. Prieto-Araujo, and O. Gomis-Bellmunt, "Modelling and control of an interline current flow controller for meshed HVDC grids," *IEEE Transactions on Power Delivery*, vol. PP, no. 99, pp. 1–1, 2016.

[23] A. Mokhberdoran, A. Carvalho, H. Leite, and N. Silva, "A review on HVDC circuit breakers," in *Renewable Power Generation Conference (RPG 2014), 3rd*, Sept 2014, pp. 1–6.

[24] C. M. Franck, "HVDC circuit breakers: A review identifying future research needs," *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 998–1007, April 2011.

[25] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, Jan 2015.

[26] Working Group B4-52, "HVDC grid feasibility study technical brochure, 2013," CIGRE, Technical Report, April 2013.

[27] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, Jan 2015.

[28] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37–53, Jan 2015.

[29] J. Yang, J. E. Fletcher, and J. O'Reilly, "Short-circuit and ground fault analyses and location in VSC-based DC network cables," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3827–3837, Oct 2012.

[30] J. Yang, J. E. Fletcher, and J. O'Reilly, "Multiterminal DC wind farm collection grid internal fault analysis and protection design," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2308–2318, Oct 2010.

[31] B. Chang, O. Cwikowski, M. Barnes, and R. Shuttleworth, "Multi-terminal VSC-HVDC pole-to-pole fault analysis and fault recovery study," in *11th IET International Conference on AC and DC Power Transmission*, Feb 2015, pp. 1–8.

[32] J. G. Lee, U. A. Khan, S. W. Lim, H. Y. Lee, B. W. Lee, Y. G. Kim, and J. W. Sim, "Fault current characteristics of multi-terminal HVDC system," in *2015 3rd International Conference on Electric Power Equipment; Switching Technology (ICEPE-ST)*, Oct 2015, pp. 566–569.

[33] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*. John Wiley & Sons, 2016.

[34] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, Sept 1981.

[35] H. Liu, Z. Xu, and Z. Gao, "A control strategy for three-level VSC-HVDC system," in *IEEE Power Engineering Society Summer Meeting,*, vol. 1, July 2002, pp. 480–485 vol.1.

[36] A. Yazdani and R. Iravani, "Dynamic model and control of the NPC-based back-to-back HVDC system," *IEEE Transactions on Power Delivery*, vol. 21, no. 1, pp. 414–424, Jan 2006.

[37] M. Beza and S. Norrga, "Three-level converters with selective harmonic elimination PWM for HVDC application," in *2010 IEEE Energy Conversion Congress and Exposition*, Sept 2010, pp. 3746–3753.

[38] M. Chaves, E. Margato, J. F. Silva, S. F. Pinto, and J. Santana, "Fast optimum-predictive control and capacitor voltage balancing strategy for bipolar back-to-back NPC converters in high-voltage direct current transmission systems," *IET Generation, Transmission Distribution*, vol. 5, no. 3, pp. 368–375, March 2011.

[39] I. G. Torres, H. Miranda, V. Cardenas, and R. A. Salas, "Gain scheduling scheme assisting the control strategy for three-level NPC VSC-HVDC transmission system," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, Oct 2014, pp. 4635–4641.

[40] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings,*, vol. 3, June 2003, p. 6 pp. Vol.3.

[41] R. Marquardt, A. Lesnicar, and J. Hildinger, "Modulares stromrichterkonzept fur netzkupplungsanwendung bei hohen spannungen," in *Proceedings of the ETG-Fachtagung, Bad Nauheim, Germany,*, 2002.

[42] Y. Wang and R. Marquardt, "Future HVDC-grids employing modular multilevel converters and hybrid DC-breakers," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, Sept 2013, pp. 1–8.

[43] A. Wasserrab and G. Balzer, "Determination of DC short-circuit currents of MMC-HVDC converters for DC circuit breaker dimensioning," in *11th IET International Conference on AC and DC Power Transmission*, Feb 2015, pp. 1–7.

[44] M. K. Bucher and C. M. Franck, "Analytic approximation of fault current contribution from ac networks to MTDC networks during pole-to-ground faults," *IEEE Transactions on Power Delivery*, vol. 31, no. 1, pp. 20–27, Feb 2016.

[45] W. Leterme, J. Beerten, and D. Van Hertem, "Equivalent circuit for half-bridge MMC dc fault current contribution," in *2016 IEEE International Energy Conference (ENERGYCON)*, April 2016, pp. 1–6.

[46] O. Cwikowski, B. Chang, M. Barnes, R. Shuttleworth, and A. Beddard, "Fault current testing envelopes for VSC HVDC circuit breakers," *IET Generation, Transmission Distribution*, vol. 10, no. 6, pp. 1393–1400, 2016.

[47] O. Cwikowski, A. Wood, A. Miller, M. Barnes, and R. Shuttleworth, "Operating DC circuit breakers with MMC," *IEEE Transactions on Power Delivery*, vol. PP, no. 99, pp. 1–1, 2017.

[48] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li, "Protection of nonpermanent faults on DC overhead lines in MMC-based HVDC systems," *IEEE Transactions on Power Delivery*, vol. 28, no. 1, pp. 483–490, Jan 2013.

[49] M. Spence, A. Plumpton, C. Rout, A. Millington, and R. Keyse, "Design and characterisation of optimised protective thyristors for VSC systems," in *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2016, pp. 1–8.

[50] A. A. Elserougi, A. S. Abdel-Khalik, A. M. Massoud, and S. Ahmed, "A new protection scheme for HVDC converters against dc-side faults with current suppression capability," *IEEE Transactions on Power Delivery*, vol. 29, no. 4, pp. 1569–1577, Aug 2014.

[51] A. Elserougi, S. Ahmed, and A. Massoud, "Half-bridge modular multilevel-based HVDC converters with external pre-charged capacitors for dc fault current suppression capability," in *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, April 2016, pp. 1–4.

[52] A. A. Elserougi, A. M. Massoud, and S. Ahmed, "Arrester-less DC fault current limiter based on pre-charged external capacitors for half-bridge modular multilevel converters," *IET Generation, Transmission Distribution*, vol. 11, no. 1, pp. 93–101, 2017.

[53] R. Marquardt, "Modular multilevel converter topologies with dc-short circuit current limitation," in *8th International Conference on Power Electronics - ECCE Asia*, May 2011, pp. 1425–1431.

[54] S. Cui, S. Kim, J. J. Jung, and S. K. Sul, "Principle, control and comparison of modular multilevel converters (MMCs) with DC short circuit fault ride-through capability," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, March 2014, pp. 610–616.

[55] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended dc-bus-applications," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, June 2010, pp. 502–507.

[56] J. Zhang and C. Zhao, "The research of SM topology with DC fault tolerance in MMC-HVDC," *IEEE Transactions on Power Delivery*, vol. 30, no. 3, pp. 1561–1568, June 2015.

[57] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 385–394, Feb 2015.

[58] G. P. Adam, I. Abdelsalam, J. E. Fletcher, G. M. Burt, D. Holliday, and S. J. Finney, "New efficient submodule for a modular multilevel converter in multiterminal HVDC networks," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4258–4278, June 2017.

[59] A. Nami, L. Wang, F. Dijkhuizen, and A. Shukla, "Five level cross connected cell for cascaded converters," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, Sept 2013, pp. 1–9.

[60] M. Sleiman, H. F. Blanchette, K. Al-Haddad, L. A. Gregoire, and H. Kanaan, "A new 7L-PUC multi-cells modular multilevel converter for AC-AC and AC-DC applications," in *2015 IEEE International Conference on Industrial Technology (ICIT)*, March 2015, pp. 2514–2519.

[61] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, D. R. Critchley, and R. W. Crookes, "A new hybrid multi-level voltage-source converter with DC fault blocking capability," in *9th IET International Conference on AC and DC Power Transmission (ACDC 2010)*, Oct 2010, pp. 1–5.

[62] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, and F. Hassan, "The alternate arm converter: A new hybrid multilevel converter with DC-fault blocking capability," *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 310–317, Feb 2014.

[63] A. N. Greenwood and T. H. Lee, "Theory and application of the commutation principle for HVDC circuit breakers," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-91, no. 4, pp. 1570–1574, July 1972.

[64] H. A. Darwish, M. A. Izzularab, and N. I. Elkalashy, "Enhanced commutation circuit design of HVDC circuit breaker using EMTP," in *2005/2006 IEEE/PES Transmission and Distribution Conference and Exhibition*, May 2006, pp. 978–985.

[65] H. Brumshagen, H. Hartel, and D. Kind, "New developments in design and testing of HVDC circuit breakers," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-93, no. 5, pp. 1353–1358, Sept 1974.

[66] S. Tokoyoda, M. Sato, K. Kamei, D. Yoshida, M. Miyashita, K. Kikuchi, and H. Ito, "High frequency interruption characteristics of VCB and its application to high voltage DC circuit breaker," in *2015 3rd International Conference on Electric Power Equipment; Switching Technology (ICEPE-ST)*, Oct 2015, pp. 117–121.

[67] G. A. Hofmann, G. L. L. Barbera, N. E. Reed, and L. A. Shillong, "A high speed HVDC circuit breaker with crossed-field interrupters," *IEEE Transactions on Power Apparatus and Systems*, vol. 95, no. 4, pp. 1182–1193, July 1976.

[68] G. A. Hofmann, G. L. LaBarbera, N. E. Reed, L. A. Shillong, W. F. Long, and D. J. Melvold, "Field test of HVDC circuit breaker: Load break and fault clearing on the pacific intertie," *IEEE Transactions on Power Apparatus and Systems*, vol. 95, no. 3, pp. 829–838, May 1976.

[69] D. J. Melvold, P. R. Shockley, W. F. Long, and N. G. Hingorani, "Three terminal operation of the pacific HVDC intertie for dc circuit breaker testing," *IEEE Transactions on Power Apparatus and Systems*, vol. 95, no. 4, pp. 1287–1296, July 1976.

[70] B. L. Damsky, I. Imam, and W. Premerlani, "A new HVDC circuit breaker system design for $\pm$400 kV," in *1979 7th IEEE/PES Transmission and Distribution Conference and Exposition*, Apr 1979, pp. 230–236.

[71] S. Yanabu, T. Tamagawa, S. Irokawa, T. Horiuchi, and S. Tomimuro, "Development of HVDC circuit breaker and its interrupting test," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-101, no. 7, pp. 1958–1965, July 1982.

[72] S. Yanabu, T. Tamagawa, S. Irokawa, T. Horiuchi, and S. Tomimuro, "Development of HVDC circuit breaker and its interrupting test," *IEEE Power Engineering Review*, vol. PER-2, no. 7, pp. 33–34, July 1982.

[73] T. Senda, T. Tamagawa, K. Higuchi, T. Horiuchi, and S. Yanabu, "Development of HVDC circuit breaker based on hybrid interruption scheme," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-103, no. 3, pp. 545–552, March 1984.

[74] D. Alferov, A. Budovsky, D. Evsin, V. Ivanov, V. Sidorov, and V. Yagnov, "DC vacuum circuit-breaker," in *2008 23rd International Symposium on Discharges and Electrical Insulation in Vacuum*, vol. 1, Sept 2008, pp. 173–176.

[75] K. Arimatsu, Y. Yoshioka, S. Tokuyama, Y. Kato, and K. Hirata, "Development and interrupting tests on 250kV 8kA HVDC circuit breaker," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-104, no. 9, pp. 2452–2459, Sept 1985.

[76] B. Bachmann, G. Mauthe, E. Ruoss, H. P. Lips, J. Porter, and J. Vithayathil, "Development of a 500kV airblast HVDC circuit breaker," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-104, no. 9, pp. 2460–2466, Sept 1985.

[77] B. Pauli, G. Mauthe, E. Ruoss, G. Ecklin, J. Porter, and J. Vithayathil, "Development of a high current HVDC circuit breaker with fast fault clearing capability," *IEEE Transactions on Power Delivery*, vol. 3, no. 4, pp. 2072–2080, Oct 1988.

[78] A. Lee, P. G. Slade, K. H. Yoon, J. Porter, and J. Vithayathil, "The development of a HVDC SF6 breaker," *IEEE Power Engineering Review*, vol. PER-5, no. 10, pp. 32–32, Oct 1985.

[79] J. J. Vithayathil, A. L. Courts, W. G. Peterson, N. G. Hingorani, S. Nilsson, and J. W. Porter, "HVDC circuit breaker development and field tests," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-104, no. 10, pp. 2692–2705, Oct 1985.

[80] R. Jungblut and R. Sittig, "Hybrid high-speed DC circuit breaker using charge-storage diode," in *1998 IEEE Industrial and Commercial Power Systems Technical Conference. Conference Record. Papers Presented at the 1998 Annual Meeting (Cat. No.98CH36202)*, May 1998, pp. 95–99.

[81] Z. Q. Shi, Y. K. Zhang, S. L. Jia, X. C. Song, L. J. Wang, and M. Chen, "Design and numerical investigation of a HVDC vacuum switch based on artificial current zero," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 22, no. 1, pp. 135–141, Feb 2015.

[82] Y. Zhang, Z. Shi, Q. Wang, Z. Gao, S. Jia, and L. Wang, "Experimental investigation on HVDC vacuum circuit breaker based on artificial current zero," in *2016 27th International Symposium on Discharges and Electrical Insulation in Vacuum (ISDEIV)*, vol. 2, Sept 2016, pp. 1–4.

[83] G. Ge, M. Liao, X. Duan, and J. Zou, "HVDC hybrid circuit breaker based on SF6 interrupter and vacuum interrupter in series," in *2013 2nd International Conference on Electric Power Equipment - Switching Technology (ICEPE-ST)*, Oct 2013, pp. 1–4.

[84] W. Lin, D. Jovcic, S. Nguefeu, and H. Saad, "Modelling of high power mechanical DC circuit breaker," in *2015 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Nov 2015, pp. 1–5.

[85] M. Bonkarev, N. K. Challagondla, and D. Thummapal, "Simulation-based performance evaluation of different current breaking techniques employed in mechanical HVDC circuit breakers," in *2016 IEEE International Conference on High Voltage Engineering and Application (ICHVE)*, Sept 2016, pp. 1–4.

[86] B. C. Kim, Y. H. Chung, H. D. Hwang, and H. S. Mok, "Comparison of inverse current injecting HVDC curcuit breaker," in *2015 3rd International Conference on Electric Power Equipment; Switching Technology (ICEPE-ST)*, Oct 2015, pp. 501–505.

[87] Y. Shan, T. C. Lim, B. W. Williams, and S. J. Finney, "Successful fault current interruption on DC circuit breaker," *IET Power Electronics*, vol. 9, no. 2, pp. 207–218, 2016.

[88] L. Angquist, S. Norrga, and T. Modeer, "A new dc breaker with reduced need for semiconductors," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–9.

[89] L. Angquist, S. Norrga, T. Modeer, and S. Nee, "Fast HVDC breaker using reduced-rating power electronics," in *13th IET International Conference on AC and DC Power Transmission (ACDC 2017)*, Feb 2017, pp. 1–6.

[90] L. Li, Y. Cheng, M. Peng, B. Yu, Y. Liu, Z. Yuan, and P. Yuan, "Nonlinear frequency characteristic of multiple series gaps with voltage-dividing network and its application in HVDC circuit breaker," *IEEE Transactions on Plasma Science*, vol. 44, no. 10, pp. 1989–1996, Oct 2016.

[91] L. Liu, M. van der Meijden, M. Popov, and V. Terzija, "The DC circuit breaker with necessary bidirectional interruption capability," in *2016 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Oct 2016, pp. 110–114.

[92] K. Tahata, S. Ka, S. Tokoyoda, K. Kamei, K. Kikuchi, D. Yoshida, Y. Kono, R. Yamamoto, and H. Ito, "HVDC circuit breakers for HVDC grid applications," in *AORC Technical meeting 2014*, May 2014, pp. 1–9.

[93] T. Schultz, V. Lenz, and C. M. Franck, "Circuit breakers for fault current interruption in HVDC grids," in *VDE High Voltage Technology 2016; ETG-Symposium*, Nov 2016, pp. 1–6.

[94] C. Meyer, M. Kowal, and R. W. D. Doncker, "Circuit breaker concepts for future high-power DC-applications," in *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, vol. 2, Oct 2005, pp. 860–866 Vol. 2.

[95] M. Kempkes, I. Roth, and M. Gaudreau, "Solid-state circuit breakers for medium voltage DC power," in *2011 IEEE Electric Ship Technologies Symposium*, April 2011, pp. 254–257.

[96] H. J. Jang, W. Y. Lee, S. h. Park, and J. K. Chong, "A configuration concept of solid state switch for 2kV class DC circuit breaker," in *2015 3rd International Conference on Electric Power Equipment; Switching Technology (ICEPE-ST)*, Oct 2015, pp. 435–437.

[97] K. Sano and M. Takasaki, "A surgeless solid-state DC circuit breaker for voltage-source-converter-based HVDC systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 4, pp. 2690–2699, July 2014.

[98] L. Feng, R. Gou, F. Zhuo, X. Yang, and F. Zhang, "Development of a 10kV solid-state DC circuit breaker based on press-pack IGBT for VSC-HVDC system," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 2371–2377.

[99] F. Zhang, X. Yang, Y. Ren, C. Li, and R. Gou, "Voltage balancing optimization of series-connected IGBTs in solid-state breaker by using driving signal adjustment technique," in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, Nov 2015, pp. 1–5.

[100] H. Li, J. Zhou, Z. Liu, and D. Xu, "Solid state DC circuit breaker for super uninterruptible power supply," in *2014 International Power Electronics and Application Conference and Exposition*, Nov 2014, pp. 1230–1235.

[101] S. Negari and D. Xu, "A new solid-state HVDC circuit breaker topology for offshore wind farms," in *2014 IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2014, pp. 1–5.

[102] J.-Y. Kim, S.-S. Choi, S.-M. Song, and I.-D. Kim, "New dc solid state circuit breaker with reclosing and rebreaking capabilities," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 3554–3558.

[103] J. Mu, L. Wang, and J. Hu, "Analysis and design of topological structure for DC solid-state circuit breaker," in *2009 World Non-Grid-Connected Wind Power and Energy Conference*, Sept 2009, pp. 1–5.

[104] F. Z. Peng, "Z-source inverter," *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504–510, Mar 2003.

[105] K. A. Corzine and R. W. Ashton, "A new z-source dc circuit breaker," in *2010 IEEE International Symposium on Industrial Electronics*, July 2010, pp. 585–590.

[106] K. A. Corzine and R. W. Ashton, "A new z-source DC circuit breaker," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2796–2804, June 2012.

[107] K. A. Corzine and R. W. Ashton, "Structure and analysis of the z-source MVDC breaker," in *2011 IEEE Electric Ship Technologies Symposium*, April 2011, pp. 334–338.

[108] P. Prempraneerach, M. G. Angle, J. L. Kirtley, G. E. Karniadakis, and C. Chryssostomidis, "Optimization of a z-source DC circuit breaker," in *2013 IEEE Electric Ship Technologies Symposium (ESTS)*, April 2013, pp. 480–486.

[109] A. Overstreet, A. Maqsood, and K. Corzine, "Modified z-source DC circuit breaker topologies," in *2014 Clemson University Power Systems Conference*, March 2014, pp. 1–6.

[110] A. Maqsood, A. Overstreet, and K. A. Corzine, "Modified z-source DC circuit breaker topologies," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7394–7403, Oct 2016.

[111] A. Maqsood and K. Corzine, "The z-source breaker for fault protection in ship power systems," in *2014 International Symposium on Power Electronics, Electrical Drives, Automation and Motion*, June 2014, pp. 307–312.

[112] A. Maqsood and K. A. Corzine, "The z-source breaker for ship power system protection," in *2015 IEEE Electric Ship Technologies Symposium (ESTS)*, June 2015, pp. 293–298.

[113] D. Keshavarzi, T. Ghanbari, and E. Farjah, "A z-source based bidirectional DC circuit breaker with fault current limitation and interruption capabilities," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2016.

[114] A. H. Chang, B. R. Sennett, A. T. Avestruz, S. B. Leeb, and J. L. Kirtley, "Analysis and design of DC system protection using z-source circuit breaker," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1036–1049, Feb 2016.

[115] A. Maqsood and K. A. Corzine, "Integration of z-source breakers into zonal DC ship power system microgrids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 269–277, March 2017.

[116] A. Hassanpoor, Y. j. HÃd'fner, A. Nami, and K. Vinothkumar, "Cost-effective solutions for handling dc faults in VSC HVDC transmission," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–7.

[117] A. Bindra, "Wide-bandgap-based power devices: Reshaping the power electronics landscape," *IEEE Power Electronics Magazine*, vol. 2, no. 1, pp. 42–47, March 2015.

[118] D. P. Urciuoli, D. Ibitayo, G. Koebke, G. Ovrebo, and R. Green, "A compact 100-A, 850-V, silicon carbide solid-state DC circuit breaker," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–5.

[119] X. SONG, A. Huang, M. C. Lee, and C. Peng, "Theoretical and experimental study of 22-kV SiC emitter turn-off (eto) thyristor," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2016.

[120] Y. Zhang and Y. C. Liang, "Over-current protection scheme for SiC power MOSFET DC circuit breaker," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 1967–1971.

[121] Z. Miao, G. Sabui, A. Moradkhani, J. Wang, Z. Shuai, and X. Yin, "A self-powered bidirectional DC solid state circuit breaker using two normally-on SiC JFETs," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 4119–4124.

[122] D. Jovcic and B. Wu, "Fast fault current interruption on high-power DC networks," in *IEEE PES General Meeting*, July 2010, pp. 1–6.

[123] D. Jovcic and B. T. Ooi, "Developing DC transmission networks using DC transformers," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2535–2543, Oct 2010.

[124] M. J. Carrizosa, J. Cortes, A. Benchaib, P. Alou, G. Damm, J. A. Cobos, and F. Lamnabhi-Lagarrigue, "DC/DC converters as DC circuit-breakers in HVDC networks operation," in *2014 16th European Conference on Power Electronics and Applications*, Aug 2014, pp. 1–10.

[125] P. Cairoli, I. Kondratiev, and R. A. Dougal, "Coordinated control of the bus tie switches and power supply converters for fault protection in DC microgrids," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 2037–2047, April 2013.

[126] L. Tang, B. Wu, V. Yaramasu, W. Chen, and H. S. Athab, "Fast acting DC circuit breaker for HVDC transmission line based on DC/DC chopper," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, May 2014, pp. 3695–3701.

[127] R. Sellick, M. Agamy, L. Hao, and K. Weeber, "A high-speed HVDC breaker topology with integral voltage-changing capability," in *2015 IEEE Electrical Insulation Conference (EIC)*, June 2015, pp. 123–126.

[128] Y. Liu, X. Wei, C. Gao, and J. Cao, "Topological analysis of HVDC circuit breaker with coupling transformer," in *2015 IEEE First International Conference on DC Microgrids (ICDCM)*, June 2015, pp. 129–134.

[129] A. Maqsood and K. Corzine, "Z-source dc circuit breakers with coupled inductors," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 1905–1909.

[130] K. A. Corzine, "A new-coupled-inductor circuit breaker for DC applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1411–1418, Feb 2017.

[131] P. van Gelder and J. A. Ferreira, "Zero volt switching hybrid DC circuit breakers," in *Conference Record of the 2000 IEEE Industry Applications Conference. Thirty-Fifth IAS Annual Meeting and World Conference on Industrial Applications of Electrical Energy (Cat. No.00CH37129)*, vol. 5, 2000, pp. 2923–2927 vol.5.

[132] D. Bosche, E. D. Wilkening, H. Kopf, and M. Kurrat, "Breaking performance investigation of hybrid DC circuit breakers: An experimental approach," in *2015 IEEE 61st Holm Conference on Electrical Contacts (Holm)*, Oct 2015, pp. 117–123.

[133] D. Bosche, E. D. Wilkening, H. Kopf, and M. Kurrat, "Hybrid DC circuit breaker feasibility study," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. PP, no. 99, pp. 1–9, 2016.

[134] J. Häfner and B. Jacobson, "Proactive hybrid HVDC breakers - a key innovation for reliable HVDC grids," in *Electric system of the future - Integrating supergrids and microgrids international symposium, Italy*, Sept 2011, pp. 1–8.

[135] J. Magnusson, A. Bissal, G. Engdahl, and J. A. Martinez-Velasco, "Design aspects of a medium voltage hybrid DC breaker," in *IEEE PES Innovative Smart Grid Technologies, Europe*, Oct 2014, pp. 1–6.

[136] K. Yasuoka, T. Yoshiki, T. Hayakawa, T. Oide, and N. Takeuchi, "A hybrid DC circuit breaker with vacuum contact and SiC-MOSFET for arcless commutation," in *2016 IEEE 62nd Holm Conference on Electrical Contacts (Holm)*, Oct 2016, pp. 45–48.

[137] L. Novello, F. Baldo, A. Ferro, A. Maistrello, and E. Gaio, "Development and testing of a 10-kA hybrid mechanical-static DC circuit breaker," *IEEE Transactions on Applied Superconductivity*, vol. 21, no. 6, pp. 3621–3627, Dec 2011.

[138] A. Hassanpoor, J. Häfner, and B. Jacobson, "Technical assessment of load commutation switch in hybrid HVDC breaker," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5393–5400, Oct 2015.

[139] W. Lin, D. Jovcic, S. Nguefeu, and H. Saad, "Modelling of high-power hybrid DC circuit breaker for grid-level studies," *IET Power Electronics*, vol. 9, no. 2, pp. 237–246, 2016.

[140] M. Callavik, A. Blomberg, J. Hafner, and B. Jacobson, "The hybrid HVDC breaker: An innovation breakthrough enabling reliable HVDC grids," ABB Grid Systems, Technical Report, Nov 2012. [Online]. Available: http://new.abb.com/docs/default-source/default-document-library/hybrid-hvdc-breaker---an-innovation-breakthrough-for-reliable-hvdc-gridsnov2012finmc20121210_clean.pdf?sfvrsn=2

[141] O. Cwikowski, M. Barnes, R. Shuttleworth, and B. Chang, "Analysis and simulation of the proactive hybrid circuit breaker," in *2015 IEEE 11th International Conference on Power Electronics and Drive Systems*, June 2015, pp. 4–11.

[142] C. Peng, A. Q. Huang, and X. Song, "Current commutation in a medium voltage hybrid DC circuit breaker using 15 kV vacuum switch and SiC devices," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 2244–2250.

[143] D. Schmitt, Y. Wang, T. Weyh, and R. Marquardt, "Dc-side fault current management in extended multiterminal-HVDC-grids," in *International Multi-Conference on Systems, Sygnals Devices*, March 2012, pp. 1–5.

[144] M. Hajian, D. Jovcic, and B. Wu, "Evaluation of semiconductor based methods for fault isolation on high voltage DC grids," *IEEE Transactions on Smart Grid*, vol. 4, no. 2, pp. 1171–1179, June 2013.

[145] R.Derakhshanfar, T.U.Jonsson, U.Steiger, and M.Habert, "Hybrid HVDC breaker - a solution for future HVDC system," in *CIGRE Session 2014*, August 2014, pp. 1–12.

[146] A. Yanushkevich, R. Scharrenberg, M. Kell, and R. P. P. Smeets, "Switching phenomena of HVDC circuit breaker in multi-terminal system," in *11th IET International Conference on AC and DC Power Transmission*, Feb 2015, pp. 1–6.

[147] Y. Li, X. Shi, F. Wang, L. M. Tolbert, and J. Liu, "Dc fault protection of multi-terminal VSC-HVDC system with hybrid dc circuit breaker," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–8.

[148] J. A. Martinez and J. Magnusson, "EMTP modeling of hybrid HVDC breakers," in *2015 IEEE Power Energy Society General Meeting*, July 2015, pp. 1–5.

[149] D. Peftitsis, A. Jehle, and J. Biela, "Design considerations and performance evaluation of hybrid DC circuit breakers for HVDC grids," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–11.

[150] X. Su, S. Fu, J. Hao, X. Kang, Z. Yu, and R. Yang, "Modeling DC circuit breaker in MTDC for wind farms based on delay slope method," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Oct 2016, pp. 6512–6515.

[151] N. Lin and V. Dinavahi, "Detailed device-level electro-thermal modeling of proactive hybrid HVDC breaker for real-time hardware-in-the-loop simulation of HVDC grids," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[152] F. B. Effah, A. J. Watson, C. Ji, E. Amankwah, C. M. Johnson, C. Davidson, and J. Clare, "Hybrid HVDC circuit breaker with self-powered gate drives," *IET Power Electronics*, vol. 9, no. 2, pp. 228–236, 2016.

[153] Y. Bingjian, G. Yang, W. Xiaoguang, H. Zhiyuan, C. Longlong, and S. Yunhai, "A hybrid circuit breaker for dc-application," in *2015 IEEE First International Conference on DC Microgrids (ICDCM)*, June 2015, pp. 187–192.

[154] C. C. Davidson, R. S. Whitehouse, C. D. Barker, J. P. Dupraz, and W. Grieshaber, "A new ultra-fast HVDC circuit breaker for meshed DC networks," in *11th IET International Conference on AC and DC Power Transmission*, Feb 2015, pp. 1–7.

[155] R. Sander, M. Suriyah, and T. Leibfried, "A novel current-injection based design for HVDC circuit breakers," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2015, pp. 1–7.

[156] W. Zhou, X. Wei, S. Zhang, G. Tang, Z. He, J. Zheng, Y. Dan, and C. Gao, "Development and test of a 200kV full-bridge based hybrid HVDC breaker," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sept 2015, pp. 1–7.

[157] Z. Jie, L. Haibin, X. Rui, L. Li, N. Wenhai, S. Kun, H. Feiyang, and L. Dapeng, "Research of DC circuit breaker applied on zhoushan multi-terminal VSC-HVDC project," in *2016 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Oct 2016, pp. 1636–1640.

[158] W. Wen, Y. Huang, T. Cheng, S. Gao, Z. Chen, X. Zhang, Z. Yu, R. Zeng, and W. Liu, "Research on a current commutation drive circuit for hybrid dc circuit breaker and its optimisation design," *IET Generation, Transmission Distribution*, vol. 10, no. 13, pp. 3119–3126, 2016.

[159] W. Wen, Y. Huang, Y. Sun, J. Wu, M. Al-Dweikat, and W. Liu, "Research on current commutation measures for hybrid DC circuit breakers," *IEEE Transactions on Power Delivery*, vol. 31, no. 4, pp. 1456–1463, Aug 2016.

[160] F. Xu, H. Yu, Y. Lu, P. Qiu, K. Tong, J. Xuan, Q. Chen, X. Huang, and D. Jiang, "Topology, control and fault analysis of a new type HVDC breaker for HVDC systems," in *2016 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Oct 2016, pp. 1959–1964.

[161] X. Song, C. Peng, and A. Q. Huang, "A medium-voltage hybrid DC circuit breaker, part i: Solid-state main breaker based on 15 kV SiC emitter turn-off thyristor," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 278–288, March 2017.

[162] G. Liu, F. Xu, Z. Xu, Z. Zhang, and G. Tang, "Assembly HVDC breaker for HVDC grids with modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2016.

[163] J. Liu, N. Tai, C. Fan, and S. Chen, "A hybrid current-limiting circuit for DC line fault in multi-terminal VSC-HVDC system," *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[164] M. Komatsu, "Approach and basic evaluation for the DC circuit breaker with fault current limiting feature," in *2016 IEEE International Telecommunications Energy Conference (INTELEC)*, Oct 2016, pp. 1–5.

[165] C. Zhou, P. Wang, and D. Jacobson, "The application of superconducting fault current limiters in manitoba hydro HVDC system," in *2013 IEEE Power Energy Society General Meeting*, July 2013, pp. 1–5.

[166] S. Roy, D. Kanabar, C. Dodiya, and S. Pradhan, "Development of a prototype hybrid DC circuit breaker for superconducting magnets quench protection," *IEEE Transactions on Applied Superconductivity*, vol. 24, no. 6, pp. 1–6, Dec 2014.

[167] S. Li, C. Zhao, and J. Xu, "A new topology for current-limiting solid-state HVDC circuit breaker," in *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, Dec 2016, pp. 1–5.

[168] S. Liang, Y. Tang, Z. Xia, L. Ren, L. Chen, Y. Xu, Z. Wang, and S. Yan, "Study on the current limiting performance of a novel SFCL in DC systems," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 4, pp. 1–6, June 2017.

[169] S. H. Lim, H. S. Choi, and B. S. Han, "Fault current limiting characteristics of DC dual reactor type SFCL using switching operation of HTSC elements," *IEEE Transactions on Applied Superconductivity*, vol. 16, no. 2, pp. 723–726, June 2006.

[170] J. Shi, Y. Tang, L. Chen, J. Wang, L. Ren, J. Li, L. Li, T. Peng, and S. Cheng, "The application of active superconducting DC fault current limiter in hybrid AC/DC power supply systems," *IEEE Transactions on Applied Superconductivity*, vol. 18, no. 2, pp. 672–675, June 2008.

[171] Y. Chen, X. Liu, J. Sheng, L. Cai, Z. Jin, J. Gu, Z. An, X. Yang, and Z. Hong, "Design and application of a superconducting fault current limiter in DC systems," *IEEE Transactions on Applied Superconductivity*, vol. 24, no. 3, pp. 1–5, June 2014.

[172] C. Peng, J. Wen, Y. Wang, J. Wu, and X. Chen, "Potential use of fault current limiter in VSC based DC transmission systems," in *2012 Asia-Pacific Power and Energy Engineering Conference*, March 2012, pp. 1–4.

[173] W. Ahmed and P. Manohar, "DC line protection for VSC-HVDC system," in *2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Dec 2012, pp. 1–6.

[174] J. Descloux, C. Gandioli, B. Raison, N. Hadjsaid, and P. Tixador, "Protection system for meshed HVDC network using superconducting fault current limiters," in *2013 IEEE Grenoble Conference*, June 2013, pp. 1–5.

[175] F. A. Mourinho, D. Motter, J. C. M. Vieira, R. M. Monaro, S. P. L. Blond, M. Zhang, and W. Yuan, "Modeling and analysis of superconducting fault current limiters applied in VSC-HVDC systems," in *2015 IEEE Power Energy Society General Meeting*, July 2015, pp. 1–5.

[176] B. Xiang, K. Yang, Y. Tan, Z. Liu, Y. Geng, J. Wang, and S. Yanabu, "DC-current-limiting characteristics of YBCO tapes for DC currents of 50 a to 10 kA," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 4, pp. 1–5, June 2017.

[177] J. G. Lee, U. A. Khan, H. Y. Lee, and B. W. Lee, "Impact of sfcl on the four types of HVDC circuit breakers by simulation," *IEEE Transactions on Applied Superconductivity*, vol. 26, no. 4, pp. 1–6, June 2016.

[178] B. Xiang, K. Yang, Y. Tan, L. Zhang, Z. Liu, Y. Geng, J. Wang, and S. Yanabu, "A DC circuit breaker based on superconducting current-limiting technology," in *2015 3rd International Conference on Electric Power Equipment; Switching Technology (ICEPE-ST)*, Oct 2015, pp. 257–260.

[179] X. Pei, A. C. Smith, and M. Barnes, "Superconducting interface for a DC circuit breaker," in *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, April 2016, pp. 1–6.

[180] B. Xiang, Z. Liu, Y. Geng, and S. Yanabu, "DC circuit breaker using superconductor for current limiting," *IEEE Transactions on Applied Superconductivity*, vol. 25, no. 2, pp. 1–7, April 2015.

[181] W. R. L. Garcia, A. Bertinato, P. Tixador, B. Raison, and B. Luscan, "Full-selective protection strategy for MTDC grids based on R-type superconducting FCLs and mechanical DC circuit breakers," in *5th IET International Conference on Renewable Power Generation (RPG) 2016*, Sept 2016, pp. 1–7.

[182] U. A. Khan, J. G. Lee, F. Amir, and B. W. Lee, "A novel model of HVDC hybrid-type superconducting circuit breaker and its performance analysis for limiting and breaking DC fault currents," *IEEE Transactions on Applied Superconductivity*, vol. 25, no. 6, pp. 1–9, Dec 2015.

[183] U. A. Khan, J.-G. Lee, I.-J. Seo, F. Amir, and B.-W. Lee, "Feasibility analysis of a novel hybrid-type superconducting circuit breaker in multi-terminal HVDC networks," *Physica C: Superconductivity and its Applications*, vol. 518, pp. 154 – 158, 2015.

[184] W. Leterme and D. Van Hertem, "Classification of fault clearing strategies for HVDC grids," in *Cigre Lund Symposium, Lund*, May 2015, pp. 1–10.

[185] B. Chang, O. Cwikowski, X. Pei, M. Barnes, R. Shuttleworth, and A. C. Smith, "Impact of fault current limiter on VSC-HVDC DC protection," in *12th IET International Conference on AC and DC Power Transmission (ACDC 2016)*, May 2016, pp. 1–6.

[186] Y. Zhang, Z. Shi, Q. Wang, S. Jia, and L. Wang, "Research on the experimental method for HVDC vacuum circuit breaker based on artificial current zero," in *2016 27th International Symposium on Discharges and Electrical Insulation in Vacuum (ISDEIV)*, vol. 2, Sept 2016, pp. 1–4.

[187] M. K. Bucher and C. M. Franck, "Analytic Approximation of Fault Current Contributions From Capacitive Components in HVDC Cable Networks," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 74–81, feb 2015.

[188] R. Sander and T. Leibfried, "Considerations on energy absorption of HVDC circuit breakers," in *2014 49th International Universities Power Engineering Conference (UPEC)*, sep 2014, pp. 1–6.

[189] G. L. Amicucci, B. D'Elia, and P. Gentile, "Mean time to failure of metal oxide varistors under lightning stress," in *2003 IEEE Bologna Power Tech Conference Proceedings,*, vol. 3, June 2003, pp. 6 pp. Vol.3–.

[190] J. L. He and J. Hu, "Discussions on nonuniformity of energy absorption capabilities of ZnO varistors," *IEEE Transactions on Power Delivery*, vol. 22, no. 3, pp. 1523–1532, July 2007.

[191] S. Nyati, S. R. Atmuri, D. L. Gordon, and V. Koschik, "Metal oxide varistor to limit dynamic overvoltages at the terminals of an HVDC converter," *IEEE Transactions on Power Delivery*, vol. 3, no. 2, pp. 819–827, apr 1988.

[192] Siemens AG, Energy Sector, "High-voltage surge arresters - Product guide," Siemens AG, Germany, Technical Report, 2014. [Online]. Available: http://www.siemens.com/about/sustainability/en/environmental-portfolio/products-solutions/power-transmission-distribution/high-voltage-direct-current-transmission.htm

[193] ABB Switzerland Ltd, "Application guidelines, Overvoltage protection," ABB, Switzerland, Technical Report, 2011. [Online]. Available: https://library.e.abb.com/public/70e9fd6933c8c644c12578d200333cb5/952_abb_awr_mittelspannung_E_low.pdf

[194] J. R. Lucas and P. G. McLaren, "An MOV model for series compensation studies," in *Proceedings of the 33rd Midwest Symposium on Circuits and Systems*, aug 1990, pp. 633–636 vol.2.

[195] F. B. Ajaei and R. Iravani, "Cable Surge Arrester Operation Due to Transient Overvoltages Under DC-Side Faults in the MMC-HVDC Link," *IEEE Transactions on Power Delivery*, vol. 31, no. 3, pp. 1213–1222, jun 2016.

[196] Siemens AG, Energy Sector, "High Voltage Direct Current Transmission - Proven Technology for Power Exchange," Siemens AG, Germany, Technical Report, 2011. [Online]. Available: http://www.energy.siemens.com/us/en/power-transmission/high-voltage-products/surge-arresters-limiters/high-voltage-station-arresters.htm

[197] R. Hong, L. Bing, X. Li, C. Zongyuan, and L. Li, "Development of 800kV UHVDC Transmission Technology in China," in *2008 International Conference on High Voltage Engineering and Application*, nov 2008, pp. 1–7.

[198] D. Zhang, M. Haeusler, H. Rao, C. Shang, and T. Shang, "Converter station design of the 800 kV UHVDC project Yunnan-Guangdong," in *The 17th Conference of Electric Power Supply Industry. Macau, China*, vol. 805, 2008.

[199] A. Mizukoshi, J. Ozawa, S. Shirakawa, and K. Nakano, "Influence of uniformity on energy absorption capabilities of zinc oxide elements as applied in arresters," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-102, no. 5, pp. 1384–1390, May 1983.

[200] M. Bartkowiak, M. G. Comber, and G. D. Mahan, "Failure modes and energy absorption capability of ZnO varistors," *IEEE Transactions on Power Delivery*, vol. 14, no. 1, pp. 152–162, Jan 1999.

[201] C. de Salles, M. L. B. Martinez, and . A. A. de Queiroz, "Ageing of metal oxide varistors due to surges," in *2011 International Symposium on Lightning Protection*, Oct 2011, pp. 171–176.

[202] C. de Salles, M. L. B. Martinez, and . A. A. de Queiroz, "Surge ageing of metal oxide varistors," in *2015 IEEE Electrical Insulation Conference (EIC)*, June 2015, pp. 137–140.

[203] C. A. Desoer and E. S. Kuh, *Basic Circuit Theory*. McGraw-Hill, 1969.

[204] A. Mokhberdoran and A. Ajami, "Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6712–6724, Dec 2014.

[205] D. Graovac and M. Purschel, "IGBT power losses calculation using the data-sheet parameters," Infineon Technologies AG, Germany, Germany, Technical Report, 2009. [Online]. Available: http://www.infineon.com

[206] Infineon, "Technische information: FZ750R65KE3," Infineon Technologies AG, Germany, Germany, Technical Report, 2014. [Online]. Available: http://www.infineon.com

[207] G. Breglio, A. Irace, E. Napoli, M. Riccio, and P. Spirito, "Experimental detection and numerical validation of different failure mechanisms in IGBTs during unclamped inductive switching," *IEEE Transactions on Electron Devices*, vol. 60, no. 2, pp. 563–570, Feb 2013.

[208] P. Ellerman, "Calculating reliability using FIT & MTTF: Arrhenius HTOL model," Microsemi, United States of America, Technical Report, 2014. [Online]. Available: https://www.microsemi.com/document-portal/doc_view/124041-calculating-reliability-using-fit-mttf-arrhenius-htol-model

[209] POWEREX, "Mitsubishi thyristor: Ft1500au-240," POWEREX, United States of America, Technical Report. [Online]. Available: http://www.pwrx.com/pwrx/docs/ft1500au2401.pdf

[210] A. Blicher, *Thyristor Physics*, 1st ed., ser. Applied Physics and Engineering 12. Springer-Verlag New York, 1976.

[211] ABB Switzerland Ltd, Semiconductors, "Phase control thyristor: 5STP 28L4200," ABB, Switzerland, Technical Report. [Online]. Available: http://www.abb.com/semiconductors

[212] F. Mura, C. Meyer, and R. W. D. Doncker, "Stability analysis of high-power DC grids," vol. 46, no. 2, March 2010, pp. 584–592.

[213] W. Leterme, N. Ahmed, J. Beerten, L. Angquist, D. V. Hertem, and S. Norrga, "A new HVDC grid test system for HVDC grid dynamics and protection studies in emt-type software," in *AC and DC Power Transmission, 11th IET International Conference on*, Feb 2015, pp. 1–7.

[214] S. P. Azad and D. Van Hertem, "A fast local bus current-based primary relaying algorithm for HVDC grids," *IEEE Transactions on Power Delivery*, vol. 32, no. 1, pp. 193–202, Feb 2017.

[215] S. C. F. Behrouz A. Forouzan, *Data Communications and Networking*. McGraw-Hill Forouzan Networking, 2007.

[216] A. Morandi, "State of the art of superconducting fault current limiters and their application to the electric power system," *Physica C: Superconductivity*, vol. 484, pp. 242 – 247, 2013, proceedings of the 24th International Symposium on Superconductivity (ISS2011).

[217] L. Ye and K. P. Juengst, "Modeling and simulation of high temperature resistive superconducting fault current limiters," *IEEE Transactions on Applied Superconductivity*, vol. 14, no. 2, pp. 839–842, June 2004.

[218] P. Skarby and U. Steiger, "An ultra-fast disconnecting switch for a hybrid HVDC breaker - a technical breakthrough," in *2013 CIGRE Canada Conference, Calgary, Alberta, September 9-11, 2013*, September 2013, pp. 1–9.

[219] W. Leterme, J. Beerten, and D. Van Hertem, "Nonunit protection of HVDC grids with inductive DC cable termination," *IEEE Transactions on Power Delivery*, vol. 31, no. 2, pp. 820–828, April 2016.

[220] A. Mokhberdoran, A. Carvalho, N. Silva, H. Leite, and A. Carrapatoso, "Application study of superconducting fault current limiters in meshed HVDC grids protected by fast protection relays," *Electric Power Systems Research*, vol. 143, pp. 292 – 302, 2017.

[221] A. Mokhberdoran, N. Silva, H. Leite, and A. Carvalho, "Unidirectional Protection Strategy for Multi-terminal HVDC Grids," *Transactions on Environment and Electrical Engineering*, vol. 1, no. 4, pp. 58–65, 2016.

[222] D. Jovcic and K. Ahmed, *High Voltage Direct Current Transmission: Converters, System and DC Grid*. John Wiley & Sons, Inc., 2015.

[223] The Crown Estate, "PFOW Enabling Actions Project: Sub-sea Cable Lifecycle Study," The Crown Estate, United Kingdom, Technical Report, 2015. [Online]. Available: http://new.abb.com/semiconductors/stakpak

[224] C. D. Barker and R. S. Whitehouse, "A current flow controller for use in HVDC grids," in *AC and DC Power Transmission (ACDC 2012), 10th IET International Conference on*, Dec 2012, pp. 1–5.

[225] D. Jovcic, M. Hajian, H. Zhang, and G. Asplund, "Power flow control in DC transmission grids using mechanical and semiconductor based DC/DC devices," in *AC and DC Power Transmission (ACDC 2012), 10th IET International Conference on*, Dec 2012, pp. 1–6.

[226] S. Balasubramaniam, J. Liang, and C. E. UgaldeLoo, "Control, dynamics and operation of a dual H-bridge current flow controller," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 2386–2393.

[227] V. Hofmann, A. Schon, and M. M. Bakran, "A modular and scalable HVDC current flow controller," in *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, Sept 2015, pp. 1–9.

[228] M. Ranjram and P. W. Lehn, "A multiport power-flow controller for DC transmission grids," *IEEE Transactions on Power Delivery*, vol. 31, no. 1, pp. 389–396, Feb 2016.

[229] W. Chen, X. Zhu, L. Yao, G. Ning, Y. Li, Z. Wang, W. Gu, and X. Qu, "A novel interline DC power-flow controller (IDCPFC) for meshed HVDC grids," *IEEE Transactions on Power Delivery*, vol. 31, no. 4, pp. 1719–1727, Aug 2016.

Part VI

Appendixes

A
4-Terminal HVdc Grid Model

I can calculate the motion of heavenly bodies, but not the madness of people.
Isaac Newton, Mathematician, Astronomer, and Physicist, 1643-1727

A.1 HVdc System Model

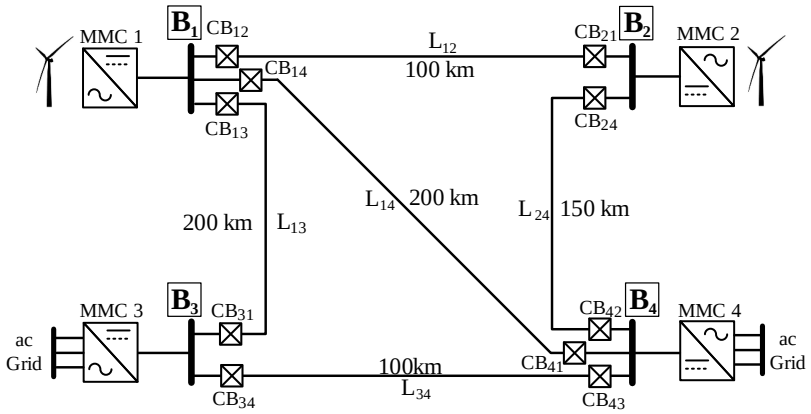


Figure A.1: Test multi-terminal HVdc grid.

A four-terminal meshed HVdc grid model, which was proposed in [213] is used in this thesis. The system configuration is shown in Figure A.1. The studied model represents a cable-based meshed HVdc grid. The investigated system has a symmetric monopole HVdc configuration and includes four half-bridge MMCs. The MMCs are modeled by a continuous modeling approach with antiparallel diodes representing the blocking capability of the MMCs [213].
In the normal condition, MMCs 1 and 2 inject almost 700 MW into the grid and MMCs 3 and 4 absorb 600 and 800 MW, respectively. The blocking current threshold of MMCs is set to 3.2 kA in order to observe the MMC behavior without blocking during sever fault conditions. The parameters of four-terminal grid are illustrated in Table A.1.

Table A.1: Four-terminal HVdc system parameters [213].

Parameter	Converter 1, 2, 3	Converter 4
Rated power	900 MVA	1200 MVA
acgrid voltage	400 kV	400 kV
Converter acvoltage	380 kV	380 kV
Transformer, u_k	0.15 pu	0.15 pu
Arm capacitance C_{arm}	29.3 μF	39 μF
Arm reactor L_{arm}	84.8 mH	63.6 mH
Arm,resistance R_{arm}	0.885 Ω	0.67 Ω
dc Bus capacitor L_s	10 μF	10 μF
Bus filter reactor L_s	10 mH	10 mH

A.2 HVdc Cable Model

HVdc transmission lines are modeled based on the XLPE insulated cable using frequency dependent modeling approach. The cable consists of central copper conductor with an XLPE insulation, sheath made of lead and armor made of steel, coaxially surrounding the main core. The cable cross-sections and properties of material are illustrated in Figure A.2 and Table A.2, respectively [212]

Figure A.2: HVdc cable cross-section and arrangement.

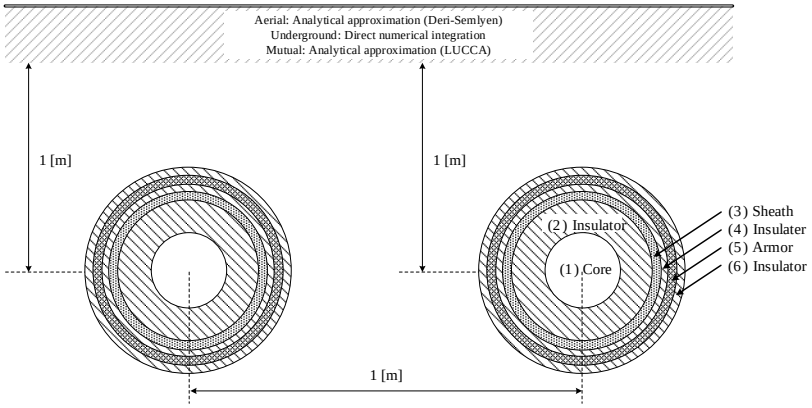


Table A.2: dc cable data [212].

Layer	Radius (mm)	Resistivity (Ωm)	Rel. permeability	Rel. permittivity
(1) Core	25.2	1.72×10^{-8}	1	1
(2) Insulator	40.2	-	1	2.3
(3) Sheath	43.0	2.20×10^{-7}	1	1
(4) Insulator	48.0	-	1	2.3
(5) Armor	53.0	1.80×10^{-7}	10	1
(6) Insulator	57.0	-	1	2.1

B
Fault Identification Schemes

The weak can never forgive. Forgiveness is the attribute of the strong.
Mahatma Gandhi, Leader of the Indian Independence Movement, 1869-1948

B.1 Employed Non-unit Fast Protection Scheme

The detailed description of the considered relaying algorithm is given in [214]. In this section only a brief introduction to the current-based relaying algorithm is provided. The employed relaying algorithm is based on local measurements and only uses current sensor readings to detect and identify faults. Moreover, it can promptly detect faults before the fault current reaches high values. This algorithm can be applied to various grid configurations. Furthermore, the employed relaying algorithm is not sensitive to measurement noise and can distinguish between faults and other system transients.

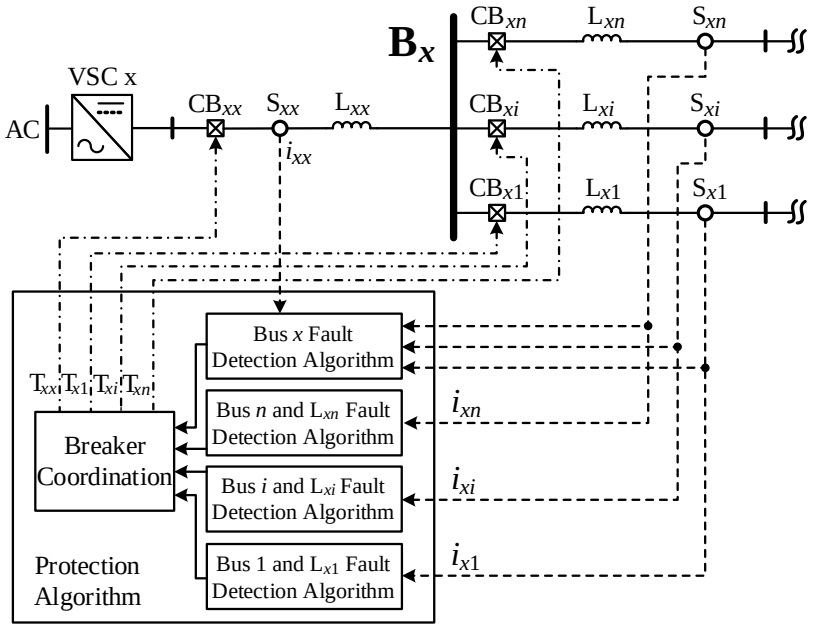


Figure B.1: dc bus x layout and its associated FDI unit

As it is explained in [214], one fault detection and identification

(FDI) unit is associated with each dc bus terminal. Figure B.1 shows the dc bus x layout and its associated FDI unit. The inputs to this FDI unit are provided by sensors S_j and S_{xj} ($j \in C_x$ where C_x corresponds to the set of all the lines connected to bus x). Trip signals T_{xx} and T_xj are the outputs of the FDI unit associated with dc bus x. Since each FDI unit only uses the current measurements at its associated bus level, its relaying algorithm is considered to be a local one.

Each FDI unit includes three types of modules:

- dc bus fault detection
- Transmission line fault detection
- Breaker coordination

Each FDI unit includes one bus fault detection module, one breaker coordination module and n line fault detection modules, where n is the number of transmission lines connected to the associated dc bus terminal.

B.2 Bus Fault Detection Module

The bus fault detection module uses a different algorithm than that of the line fault detection module to detect the faults at dc bus terminals and, consequently, distinguishes between bus and line faults. Distinguishing between bus and line faults is particularly essential for cases where a line fault occurs at a location close to a bus terminal. If bus faults are not explicitly detected, such fault scenarios might be misidentified as bus faults and might result in erroneous trip signals. The inputs to the bus fault detection module x are the measurements i_xx and i_{xj} from all sensors associated with bus x. In the bus fault detection module, the sum of all the inputs is compared with a threshold TH_B. A near-zero value can be selected for TH_B to properly detect bus faults while accounting for measurement noise. If the sum is greater than the threshold, a bus fault is detected and the trip signal T_{xx} becomes one and remains one until the fault is cleared [214].

In the bidirectional protection strategy, all the dcCBs associated with B_x are tripped and the bus fault is cleared quickly. In the unidirectional protection scheme, the trip signals are sent to all associated dcCBs but only CB_{xx} is able to interrupt the current. Therefore, the fault current flowing from the converter is interrupted while fault currents in adjacent transmission lines keep flowing in the backward direction of corresponding dcCBs (CB_{xj}). Thereafter, these fault currents (i_{xj}) are detected and interrupted by the remote dcCBs of adjacent transmission lines (CB_{jx}).

B.3 Line Fault Detection Module

The inputs to line L_{xj} fault detection module of FDI unit x is the current measurement of sensor S_{xj}, Figure B.1. In this module, fault

detection is carried out using a signal derived from the current measurement i_{xj}. This signal is the deviation of the last current sample from its moving average with a window size of 20 samples. Figure B.2 shows the three criteria evaluated in the line fault detection module, i.e., potential fault detection, selectivity, and reliability.

The potential fault detection criterion identifies any disturbances in the measured signals by detecting a local maximum in the signal. The reliability criterion distinguishes between transients caused by faults on the associated transmission lines and other system disturbances, e.g., trip of dcCBs, faults on other transmission lines, line outage, or operating point variations. In this criterion, the value of i_{xj} at the instant that the local maximum of is detected, is compared against its maximum value. When both potential fault and reliability criteria are satisfied, the selectivity criterion is evaluated. The selectivity criterion ensures that a breaker only trips if a fault occurs on the line where it is located. In this criterion, the signal is compared against a threshold TH_L. The threshold value can be selected as any values between the minimum of for faults on L_{xj} and the maximum of for faults on lines adjacent to L_{xj}. If the selectivity criterion is satisfied, an actual line fault is detected.

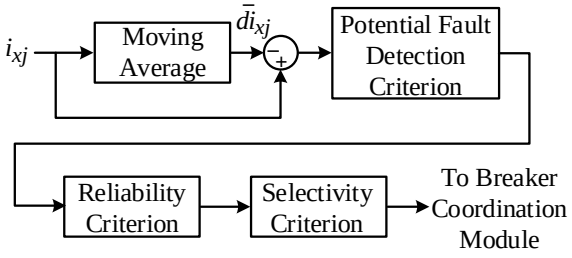


Figure B.2: Line L_{xj} fault detection module of FDI unit x

B.4 Breaker Coordination Module

In the breaker coordination module, based on the outputs of all the line fault detection modules and the bus fault detection module, the trip signals for the responsible breakers are generated. The trip signals generation relies on three principles:

- If a bus fault is detected, the trip signals T_xj for all breakers located at the lines connected to the faulted bus become one.
- If a line L_{xj} fault is detected, T_xj becomes one unless the trip signal for an adjacent breaker is already one.
- If neither a bus fault, nor an actual line fault are detected, normal condition is declared.

Abbreviations

AAC Alternate-Arm Converter

ac Alternating Current

ACSR Aluminium-Conductor Steel-Reinforced

ADS Accessory Discharging Switch

ANPC Active Neutral Point Clamped

ASCB Active Short Circuit Breaker

BCB Bidirectional dc Circuit Breaker

BS Bypass Switch

CB Circuit Breaker

CC Commutating Circuit

CEPRI China Electric Power Research Institute

CFCCB Current Flow Controlling dc Circuit Breaker

CFI Crossed Field Interrupt

CRCB Current releasing dc Circuit Breaker

CS Closing Switch

CSC Current-Source Converter

CWT Continuous Wavelet Transform

dc Direct Current

dcCB Direct Current Circuit Breaker

DS Disconnector

EMTP Electro Magnetic Transients Program

ETO Emitter Turn Off

EU European Union

FACTS Flexible AC Transmission Systems

FCC Forced Current Commutation

FCL Fault Current Limitter

FDI Fault Detection and Identification

GDP Gross Domestic Product

GHG Greenhouse Gases

GTO Gate Turn-Off Thyristor

HCB Hybrid dc Circuit Breaker

HTSC High Temperature Superconducting

HVac High-Voltage Alternating Current

HVdc High-Voltage Direct Current

IEA International Energy Agency

IGBT Insulated-Gate Bipolar Transistor

IGCT Integrated Gate-Commutated Thyristors

ILCS Integrated Load Commutating Switch

IMB Integrated Main Breaker

IPCC Intergovernmental Panel on Climate Change

JFET Junction Gate Field-Effect Transistor

KIF Key Impact Factor

KVL Kirchhoff's Voltage Law

LCC Line-Commutated Converter

LCS Load Commutating Switch

MB Main Breaker

MCB Elctro-Mechanical dc Circuit Breaker

M-HVdc Meshed High-Voltage Direct Current

MMC Modular Multilevel Converter

MOV Metal-Oxide Varistor

Mp-HCB Multi-port Hybrid dc Circuit Breaker

MSG Multiple Series Gaps

MT-HVdc Multi-Terminal High-Voltage Direct Current

MVdc Medium-Voltage Direct Current

NBS Neutral Bus Switch

NPC Neutral Point Clamped

OHL Overhead lines

OVP Over Voltage Protection

PCC Point of Common Coupling

p-ETO p-Type Emitter Turn Off

PI Proportional-integral

pu Per Unit

PUC Packed U-Cell

PWM Pulse-Width Modulation

SA Surge Arrester

SCR Silicon-Controlled Rectifier

SFCL Superconducting Fault Current Limiter

SHE Selective Harmonic Elimination

SM Submdule

SSCB Solid-state dc Circuit Breaker

STATCOM Static Synchronous Compensator

TIV Transient Interruption Voltage

TRV Transient Recovery Voltage

UFD Ultra-Fast Mechanical Disconnectror

UN United Nations

UNFCCC United Nations Framework Convention on Climate Change

US The United States

UCB Unidirectional dc Circuit Breaker

UCB Unidirectional Hybrid dc Circuit Breaker

US EPA United States Environmental Protection Agency

VI Vacuum Interrupter

VSC Voltage-Source Converter

WBG Wide Band Gap

YBCO Yttrium Barium Copper Oxygen

List of Patents and Publications

Journal Publications

1. **Mokhberdoran, A.**; Van Hertem, D.; Silva, N. ; Leite, H., Carvalho, A., "Multi-port Hybrid HVDC Circuit Breaker" ***IEEE Transactions on Industrial Electronics Journal***, June 2017 doi: 10.1109/TIE.2017.2719608

2. **Mokhberdoran, A.**; Carvalho, A.; Leite, H.; Silva, N., Carrapatoso, A., "Design and implementation of a Surge-less DC Circuit Breaker" ***Electric Power System Research Journal***, Elsevier, Volume 151, October 2017, doi: 10.1016/j.epsr.2017.05.032

3. **Mokhberdoran, A.**; Gomis-Bellmunt O.; Silva, N., Carvalho, A., "Current Flow Controlling Hybrid DC Circuit Breaker", ***IEEE Transactions on Power Electronics Journal***, Early Access, March 2017, doi: 10.1109/TPEL.2017.2688412

4. **Mokhberdoran, A.**; Carvalho, A.; Silva, ; N. Leite, H., Carrapatoso, A., "Application Study of Superconducting Fault Current Limiters in Meshed HVDC Grids Protected by Fast Protection Relays," ***Electric Power Systems Research Journal***, Volume 143, February 2017, Pages 292-302, doi: dx.doi.org/10.1016/j.epsr.2016.09.008

5. **Mokhberdoran, A.**; Silva, ; N. Leite, H.; Carvalho, A., "Unidirectional Protection Strategy for Multi-terminal HVDC Grids," ***Transactions on Environment and Electrical Engineering Journal***, Volume 1, Issue 4, November 2016, Pages 58-65, dio: http://dx.doi.org/10.1016/j.epsr.2016.09.008

6. Ajabi Farshbaf A.; Azizian, M.; Shazdeh, S.; **Mokhberdoran, A.**, "Modeling of a New Configuration for DFIGs Using T-type Converters and a Predictive Control Strategy in Wind Energy Conversion Systems," ***Journal of Renewable Energy Research (IJRER)***, Volume 6, Issue 3, June 2016, [Online] http://www.ijrer.org/ijrer/index.php/ijrer/article/view/4013

7. **Mokhberdoran, A.**; Sau-Bassols J.; Prieto-Araujo E.; Gomis-Bellmunt O.; Silva, N., Carvalho, A., "Fault Mode Operation Strategies for Current Flow Controller in Meshed HVDC Grid" In the Second Round of Review at ***Electric Power System Research Journal***, Elsevier, Submitted in January 2017

Patents

8. **A. Mokhberdoran**, N. Silva, A. Carrapatoso, A. Carvalho, H. Leite, "Fault current managing branch for surge-less current interruption in dc system," Patent No. WO2017025927 A1, International Application No. PCT/IB2016/054850, Filing date Aug 11, 2016, Publication date Feb 16, 2017.

International Conference Publications

9. **Mokhberdoran, A.**; Pirooz Azad, S.; Van Hertem, D.; Silva, N., Carvalho, A., "Unidirectional Protection of HVDC Grids Using Fast DC Circuit Breakers and Local Protection Algorithm," ***The 13***th ***IET international conference on AC and DC Power Transmission***, Manchester, UK, February 2017, pp. 1-6, doi: 10.1049/cp.2017.0011

10. **Mokhberdoran**, A.; Silva, N., Leite, H.; A.; Carvalho, "A Directional Protection Strategy for Multiterminal VSC-HVDC Grids," ***The 16***th ***IEEE International Conference on Environment and Electrical Engineering (EEEIC)***, Florence, Italy, July 2016, dio: 2016 10.1109/EEEIC.2016.7555819

11. **Mokhberdoran**, A.; Silva, N., Leite, H.; A.; Carvalho, "Surge-less Fast dc Solid-state Circuit Breaker," Poster at ***ENERGYCON 2016 IEEE international energy conference***, Leuven, Belgium, April 2016

12. **Mokhberdoran**, A.; Carvalho, A.; Leite, H.; Silva, N., Carrapatoso, A., "A New Topology of Fast Solid-state HVDC Circuit Breaker for Offshore Wind Integration Applications," ***The 17***th***European Power Electronics Conference (EPE)***, 9-10 September. 2015, doi: 10.1109/EPE.2015.7309270

13. **Mokhberdoran, A.**; Carvalho, A.; Leite, H.; Silva, N., "A review on HVDC circuit breakers," ***The 3***rd ***Renewable Power Generation Conference (RPG2014)***, 24-25 September. 2014, doi: 10.1049/cp.2014.0859

Acknowledgements

Be slow to fall into friendship; but when thou art in, continue firm and constant.

Socrates, Greek philosopher, 470-399 BC.

My passion and enthusiasm to learn more forced me to leave my job and my home country in 2013. Although these three years and half had several sadnesses[1] and happinesses[2] for me, I am quite happy with my decision to take this challenge. I believe that the past three years and half are among the most fruitful years of my life. I met many people from different countries and I made friendship with several people from different cultures. I believe that several persons helped me in accomplishing this intensive PhD work in various technical and non-technical ways.

First of all, I would like to thank my beloved wife Fatemeh[3]. My dear Fatemeh, you supported me with your endless patience and belief during this challenging trip. Without you and your backing this trip would not have started and would not have finished. You are the most invaluable person that I have had in my life! Thank you sweetheart!

My mother Naiemeh and my father Rahim have had the most strongest impact on my personality. I have learned to work hard toward my goals from my father and my mother thought me how to be consistent and hopeful in my life. Dear *Baba*[4], solving complex geometry problems with your help and guidance and learning technical stuffs from you formed a large portion of my pleasant memories from my school time when I was a teenager. My lovely *Maman*[5], your endless love and sympathy to me and my siblings has smoothen and polished my soul and gifted me peace in life. I am sure that I cannot thank you enough even if I spend all my life appreciating you both!

The presence of my lovely sister and my brother beside my parents has been a great source of reliance for me while I have been far away from home. Dear Mehdi and Paria, your presence is extremely important and valuable for me. Thank you both! Moreover, I would like to thank *Mama*[6] for her nice and kind wishes over our skype conversations.

This PhD thesis[7] was supported by the MEDOW[8] project with eleven partners in six countries. The project provided me with the opportunity of meeting knowledgeable people from all over the world. I would like to express my gratitude to all MEDOW project col-

[1] I have lost few family members and friends during these years which made me quite sad. Particularly, death of my grandmother *Aba* was one of the hardest things that I had to deal with that. Rest in peace my darling *Aba*, the woman of strength, kindness and love.

[2] We had many happy moments during these years. Particularly, the birth of my nephew *Nil*, made me extremely happy. Moreover, I and my wife together with our families are enjoying extremely special moments of our lives while we are waiting for our lovely daughter *Tamay*, to be born that we see and touch her and look to her beautiful eyes.

[3] My beloved Fatemeh, you have been beside me during the most challenging times of our life. You have been encouraging and supportive all the time! That's why I have to state that Çox sağ ol sevgilim! Sensiz bu iş ne başlanıb ne de sona ererdi!

[4] Baba means dad and it is common in both Azerbaijani and Farsi languages.

[5] Maman means mum and it is common in both Azerbaijani and Farsi languages.

[6] My mother in law.

[7] The research leading to these results has received funding from the People Programme (Marie Curie Actions) of the European Union's Seventh Framework Programme (FP7/2007-2013) under REA grant n° 317221.

[8] Multi-terminal dc Grid for Offshore Wind

laborators including ESRs[9], ERs[10], supervisors and staffs for their constructive collaboration during theses years. However, I would like to highlight my gratitudes to Jun Liang the MEDOW project coordinator and also to Dirk Van Hertem and Oriol Gomis-Bellmunt my supervisors during my placements in Leuven and Barcelona for their kind hospitalities.

Many friends have helped me in different ways during these years. It is not possible to include all the names in this limited space. However, I would like to highlight a few of them. I would like to thank Rui Brito[11], Alexandre Silveira[12] and Elias Yousefi Rezaii for their great accompany during these years. Rui and Alexandre helped me a lot in dealing with different administrative situations when a perfect level of Portuguese language was required! Thank you both again specially Rui who prepared the *Sumário* of this thesis! I would also like to thank Rodrigo Teixeira Pinto for his kind support regarding the format of thesis when I was starting to prepare this thesis.

I would like to thank my co-supervisor Helder Leite for being the first person who welcomed me when I arrived for the first time in Porto and also for his supports during my PhD program. I would like to express my gratitude to Nuno Silva, my supervisor at Efacec[13] for being a great support and encourager for my work. Nuno facilitated my training process in the initial stages of my study by supporting my attendance in different training events. I would like to thank António Carrapatoso for his wise comments on my work during our technical meetings.

Last but not least, I would also like to express my highest regard, deepest respect and sincere gratitude to my promoter Prof. Adriano Carvalho. Prof. Adriano, with you I learned many great technical deals in control and power electronics. Furthermore, I learned a lot about Portuguese geography, culture and history from you! I enjoyed a lot when we were talking about football[14]! I will never forget our early morning meetings while drinking the tasty *café*! The most important thing that I have learned from you is how to be tolerant and patient with different people! Dear Prof. Adriano, thank you for all these things!

[9] Early Stage Researchers

[10] Experienced Researchers

[11] Rui, thank you for the time that you took in many cases that I needed your help from writing an official letter to taking my car to mechanic! Thank you for introducing several nice friends to me during these years. Thank you for *Pão d'avó* that you bring us when coming back from *Castelo Branco*!

[12] Alexandre, you have always been a source of energy and happiness for me. I have learned a great deal in practical Portuguese language from you! Thank you for all these and also thank you for *Pasteis de Vouzela* that you bring us!

[13] Efacec was my host company in MEDOW project for three years. I have been associated with the automation and switchgear unit of Efacec.

[14] Needless to mention that watching the match between FC Porto and Benfica at *Estádio do Dragão* together with you has been one of my greatest memories during these years!

Curriculum Vitae

Ataollah Mokhberdoran was born in Tabriz, Iran, in 1983. He received his high school and pre-university diploma in Mathematics and Physics from the school of National Organization for Development of Exceptional Talents (NODET) in Tabriz. Thereafter, he received his Bachelor's degree [15] from the Electrical Engineering Faculty of Iran University of Science and Technology in 2006. He also received the Master's degree [16] from the Engineering Faculty of Azarbaijan University in Iran since 2010.

He worked as developer, designer and R&D engineer in Electronic Research Center Iran University of Science and Technology and Asian Sayar Sanat Ltd where he involved in several research and development projects related to the industrial and mining automation, energy conversion and embedded systems between 2005 and 2013. He was also associated with the Power Electronics and FACTS research Lab at Electrical Engineering Department of Azarbaijan University where he has done significant amount of research [17] on multilevel converters for application in renewable energy systems and FACTS. Moreover, he lectured several undergraduate courses in Electrical Power Engineering in three universities in Iran between 2010 and 2013.

In 2013, he was granted the prestigious and competitive Marie Skłodowska-Curie Research Fellowship withing the framework of Multi-terminal dc Grid for Offshore Wind (MEDOW) project funded by Seventh Framework Programme (FP7) of the European Union. In December 2013, he joined Efacec Energia Company in Porto, Portugal as his project host. He has been associated with the automation and switchgear unit of Efacec for three years.

Prior to his PhD public defense, Ata has been collaborating with the Power Electronics Lab at Electrical and Computer Engineering Department of Engineering Faculty of University of Porto as an R&D Engineer.

Currently, he works as a Power Electronics Engineer at Vestas Wind Systems A/S, Engineering Design Center in Porto.

His research interests include wind energy systems, multi-terminal HVdc grid, fast dc circuit breakers, dc grid protection, renewable energy integration to grid and power converters.

[15] The title of Bachelor thesis is *Effect of Distributed Generation in Reliability of Electrical Grid and Optimum Distributed Generation Allocation*. In this project, the optimization of distributed generations considering the system reliability factors using the genetic algorithm has been investigated.

[16] Ata's Master thesis title is *Design and Implementation of a Multilevel Inverter for Use in D-Statcom*. In this thesis a 13-level diode-clamped converter for D-Statcom application has been designed. A Lab-scale prototype of system has also been implemented.

[17] Ata has authored and co-authored over 10 articles in leading journals and IEEE Transactions during this period.