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Integrity checking of 1149.4 extensions to 1149.1

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***Abstract*—The IEEE 1149.4 Standard for a Mixed-Signal (MS) Test Bus proposes an extension to the well-accepted IEEE 1149.1 boundary-scan test architecture, with the objective of facilitating interconnect, parametric and internal testing of MS circuits. An Analog Test Access Port (ATAP) comprising two pins called AT1 and AT2, and an internal analog bus (AB) comprising two lines (AB1, AB2), enable analog test stimulae and responses to be routed to any pin possessing an Analog Boundary Module (ABMs replace the IEEE 1149.1 test cells in the case of analog pins). A Test Bus Interface Circuit (TBIC) comprising ten analog switches defines how the ATAP and the internal analog bus are (dis)connected, and the six analog switches in each ABM define what connections should be established between the pin, the core circuitry, and the internal analog bus. The large number of analog switches in the 1149.4 test architecture may raise concerns about their integrity, particularly when they are used frequently, as would be the case in an 1149.4-based MS debug strategy. This paper proposes a set of integrity check procedures that address only the 1149.4 extensions: ATAP, TBIC, AB lines, ABMs.**

***Index Terms*—IEEE1149.4, integrity, verification.**

I. Introduction

Approved in 1990, the IEEE 1149.1 boundary-scan test (BST) standard [1] was quickly adopted by a wide spectrum of industry players, ranging from semiconductor manufacturers, to equipment and software industry and vendors. The narrow application domain of BST (structural testing of digital printed circuit boards) and the increasing importance of MS designs, led to the development of an extension of this test standard, able to deal with MS circuits. The IEEE 1149.4 Standard for a MS Test Bus was approved in 1999 [2], but its market acceptance has been slow to take off, largely because the overhead of the test architecture is much higher than in the case of 1149.1. The development of alternative application domains, going beyond production test, may contribute to promote the acceptance of this test standard, much as it did in the case of 1149.1, which is nowadays used in pre- and post-production scenarios (e.g. prototype debugging, programmable hardware reconfiguration, real-time monitoring, etc.).

This paper proposes a quick integrity check procedure which addresses only the 1149.4 extensions: the 4 pins in the ATAP, the TBIC, the internal AB lines and the ABMs. It is important to understand that the proposed procedure *is not* an integrity check of the board-level 1149.4 infrastructure, neither a standard-compliance check. An integrity check of the 1149.1 TAP interconnections has already been proposed long ago [3], and 1149.1-compliance methods are also available in the literature since the early stages of the standard development process [4]. The procedures presented in the following sections may contribute to an 1149.4 board-level integrity check, as well as to an 1149.4 compliance verification method, but the scope of the integrity tests described is restricted to the 1149.4 extensions to 1149.1.

The following section recalls the switching and control structures of the TBIC and the ABMs, which together with the ATAP and the AB lines, comprise the 1149.4 extensions (to 1149.1) that enable MS circuit testing. Section 3 presents the adopted fault model and section 4 describes the integrity check test configurations. Section 5 presents the experimental work carried out with an 1149.4 chip, and the following section concludes the paper.

II. 1149.4 extensions to 1149.1

The 1149.4 test architecture is represented in figure 1 and adds the following elements to the 1149.1 test circuitry:

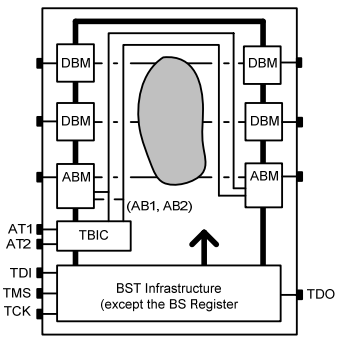


Fig. 1. A simplified representation of the 1149.4 test architecture.

- An ABM in each analog functional pin (and eventually on digital functional pins as well)

- An ATAP comprising two pins: AT1, normally used to drive an analog test stimulus, and AT2, normally used to observe the test response
- An internal AB comprising two lines, AB1 and AB2
- A TBIC that defines how the ATAP and the internal AB lines are to be connected (or disconnected)

Both the TBIC and the ABMs possess a switching structure (containing all analog switches and comparators) and a control structure, as represented in figures 2 and 3.

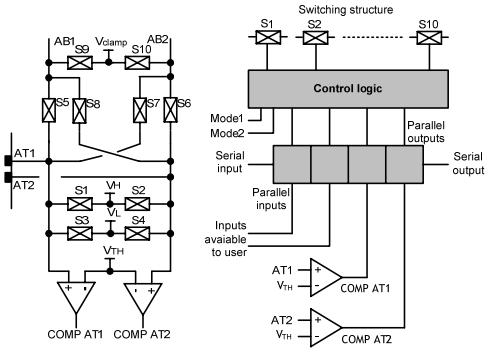


Fig. 2. TBIC switching structure and control structure.

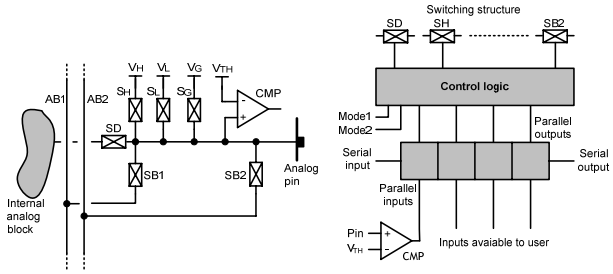


Fig. 3. ABMs switching structure and control structure.

The switching structure of the TBIC comprises two groups of switches: S1 to S4, which support ATAP interconnect fault detection (shorts and opens among ATAP pins), and S5-S10, which are essentially related to parametric test operations. This switching structure also includes two comparators, which are used to check if the voltage levels in the ATAP pins are above or below the threshold voltage V_{TH}. The TBIC comparator output is read via the boundary-scan (BS) register, as indicated in the respective control structure representation of figure 2, and enables the detection of shorts and opens in the ATAP interconnections.

The switching structure of the ABMs comprises six switches. Besides switch SD, which is responsible for determining if the ABM is in *test* (SD open) or *mission* (SD closed) modes, the remaining switches support two types of test operations. SH and SL enable the application of a HIGH or LOW voltage to the pin and are used to detect interconnect short or open faults (the voltage arriving at the input of the comparator is read via the ABM control structure, which is part of the BS register). SG, SB1 and SB2 are used for parametric test operations, e.g. for determining the value of one resistor placed between pin and ground or between two pins.

III. 1149.4 EXTENSIONS FAULT MODEL

The nature of the test architecture extensions defined in the IEEE 1149.4 standard recommends the adoption of a hybrid fault model, able to encompass the malfunctioning of various types of devices. We adopted a *single fault* model with the following characteristics:

ATAP: opens/shorts, and s@0/s@1. The ATAP (AT1, AT2) is the only 1149.4 extension element that is located outside the chip. Normally AT1 and AT2 will be connected in parallel in all 1149.4 chips in the same board, although it is possible to have as many separate ATAPs as chips (at the cost of extra pins in the board test connector). In line with the traditional fault model considered for board-level interconnect testing, we considered that AT1 and AT2 may malfunction due to open or short-circuit faults, and also to stuck-at faults.

Analog switches: s@op (always open) / s@cl (always closed). The analog switches present in the TBIC and in the ABMs are responsible for a large part of the silicon area required to implement the 1149.4 test architecture. Our proposed fault model considers that the switches may be stuck in the open or closed state.

Comparators (output): s@0/s@1. There is one comparator in each ABM, and two comparators in the TBIC. Primarily used for interconnect testing, all these comparators have one input connected to an internal threshold voltage V_{TH}, and the other input connected to a pin (AT1, AT2 in the case of the TBIC, a functional pin of the chip in the case of the ABMs). To conclude if the voltage level at the pins are above or below V_{TH}, each comparator output is captured into a corresponding bit of the BS register. A malfunctioning comparator is represented by a stuck-at fault in its output.

AB lines: opens/shorts. The internal AB lines route the ATAP (via the TBIC) to any functional pin that has an ABM. Our adopted fault model assumes that these two lines may be open or shorted.

Control structure logic: s@0/s@1. The control logic comprises four cells that belong to the BS register, and a combinational decoding block that controls the analog switches, as a function of i) the 4-bit word loaded into this control structure and ii) the current instruction.

In order to restrict the complexity of the integrity check tests, only *single faults* were considered. With the exception of the control structure test logic, our objective was to achieve 100% fault coverage. In the case of the control structure, we assume that the implicit tests applied when setting up the required switching patterns constitute a guarantee of fault-free operation. This assumption is reinforced by the higher reliability of this type of digital circuitry, and is also assumed in the 1149.1 board-level integrity check method that was referred earlier [3].

IV. INTEGRITY CHECK PROCEDURES

Our integrity check method starts from the ATAP+TBIC and proceeds to the other blocks, as successive tests indicate that an increasing part of the 1149.4 extensions operate properly.

All test setups, addressing the operating condition of specific elements (e.g. switches, comparators, etc.), are presented in the form of integrity check configurations (ICC). The presentation of each set of ICCs is accompanied by a table that indicates which elements are tested. An outline of the corresponding SVF (Serial Vector Format [9]) test code is presented at the end of this section, and may be used to estimate the number of test clock cycles required to complete an integrity check, as a function of BS register length.

A. ATAP + TBIC

The ATAP pins and the TBIC switches and comparators are checked using eight ICCs that are presented in table I.

TABLE I
ICCS USED TO CHECK THE ATAP AND TBIC

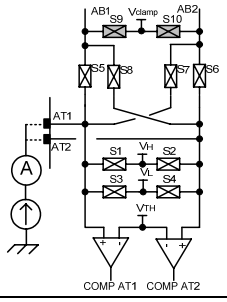
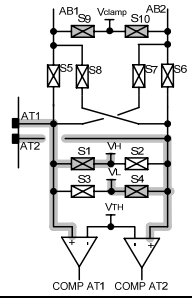
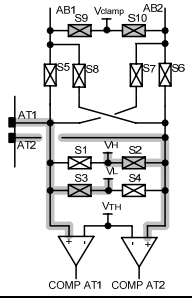
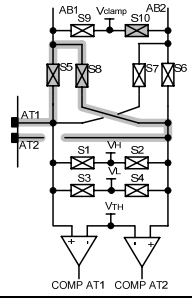
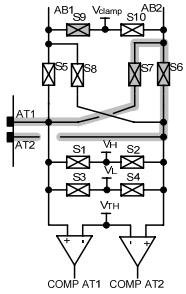
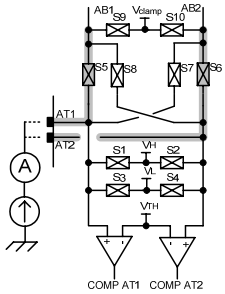
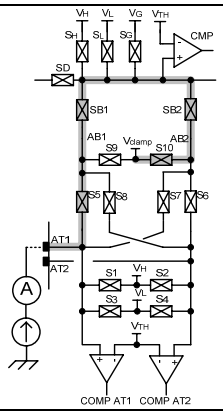
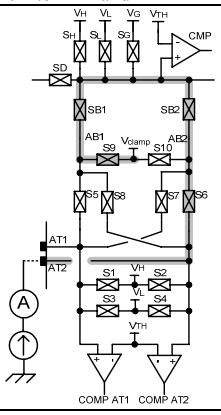
	
ICC#1 setup ABMs: all switches open. TBIC: S9, S10 closed. If $V_{Clamp} \neq 0$ and $V_L \neq 0$ Then Observe AT1, AT2. Else Try drive (source and/or sink) a known current into AT1 and AT2.	**ICC#2 setup** ABMs: all switches open. TBIC: S1, S4, S9, S10 closed. Observe AT1, AT2, Comp AT1, Comp AT2. **Remarks**: Open circuits detected: AT1-S1, AT1-CompAT1, AT2-S4, AT2-CompAT2.
	
ICC#3 setup ABMs: all switches open. TBIC: S2, S3, S9, S10 closed. Observe AT1, AT2, Comp AT1, Comp AT2. **Remarks**: Open circuits detected: AT1-S3, AT2-S2.	**ICC#4 setup** ABMs: all switches open. TBIC: S5, S8, S10 closed. Apply V_H in AT1, observe AT2. **Remarks**: Open circuits detected: AT1-S5, AT2-S8, S5-S8.

TABLE I
(CONT.)

	
ICC#5 setup ABMs: all switches open. TBIC: S6, S7, S9 closed. Apply V_H in AT1, observe AT2. **Remarks**: Open circuits detected: AT2-S6, AT1-S7, S6-S7.	**ICC#6 setup** ABMs: all switches open. TBIC: S5, S6 closed. If $V_{Clamp} \neq 0$ Then Observe AT1, AT2 Else Try drive (source or sink) a known current into AT1 and AT2
	
ICC#7 setup ABMs: SB1, SB2 closed in all ABMs. TBIC: S5, S10 closed. If $V_{Clamp} \neq 0$ Then Observe AT1 Else Try drive (source or sink) a known current into AT1.	**ICC#8 setup** ABMs: SB1, SB2 closed in all ABMs. TBIC: S6, S9 closed. If $V_{Clamp} \neq 0$ Then Observe AT2 Else Try drive (source or sink) a known current into AT2.

All s@0 / s@1, open / short, and s@op / s@cl faults considered in each block are detected. Some of these faults are detected by more than one ICC, as represented in table II.

TABLE II
FAULT COVERAGE SUMMARY FOR THE ATAP AND TBIC (LIST OF ICCS THAT DETECT EACH FAULT)

	AT1	AT2	Comp AT1	Comp AT2
s@0	2	3	2	3
s@1	3	2	3	2
open	2, 3, 4, 5	2, 3, 4, 5		
short	2, 3			

	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
s@op	2	3	3	2	4	5	5	4	8	7
s@cl	1	1	1	1	1	1	1	1	6	6

B. ABx lines + ABMs

The AB lines and the ABM switches and comparators are checked using seven ICCs, as summarised in table III.

TABLE III
ICCS USED TO CHECK AB LINES AND ABMS

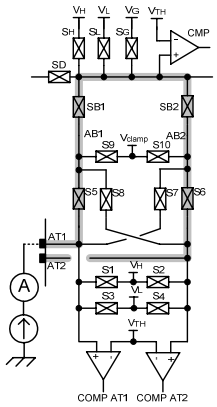
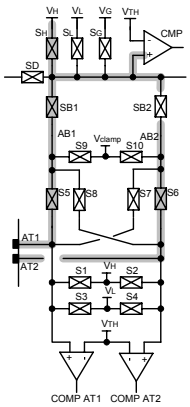
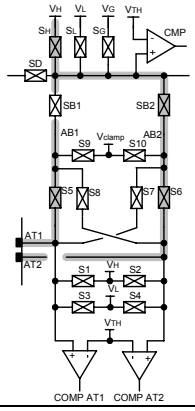
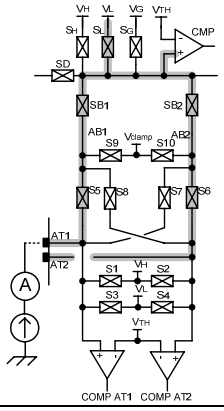
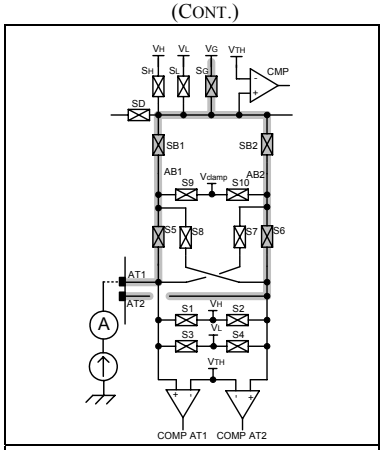
	
ICC setup for #9, #10, #11 ABMs: SB1, SB2 closed in each ABM at time; all switches open in the remaining ABMs. TBIC: S5, S6 closed. ICC #9: Apply V_H in AT1, observe AT2. ICC #10: Apply V_L in AT1, observe AT2. ICC #11: If $V_G \neq 0$ and $V_L \neq 0$ Then Observe AT2. Else Try drive (source and sink) a known current into AT1.	**ICC#12 setup** ABMs: SB1, SH closed in each ABM at time; all switches open in the remaining ABMs. TBIC: S5, S6 closed. Observe AT1, AT2, ABM Comp.
	
ICC#13 setup ABMs: SB2, SH closed in each ABM at time; all switches open in the remaining ABMs. TBIC: S5, S6 closed. Observe AT1, AT2.	**ICC#14 setup** ABMs: SB1, SB2, SL closed in each ABM at time; all switches open in the remaining ABMs. TBIC: S5, S6 closed. Observe ABM Comp. If $V_L \neq 0$ Then Observe AT2. Else Try drive (sink) a known current into AT1.

TABLE III
(CONT.)


ICC#15 setup ABMs: SB1, SB2, SG closed in each ABM at time; all switches open in the remaining ABMs. TBIC: S6, S10 closed. If $V_G \neq 0$ Then Observe AT2. Else Try drive (source or sink) a known current into AT1.

With the exception of s@op / s@cl faults in the ABM SD switches, all remaining faults considered for each block are detected. Each fault is detected by a single ICC, as represented in table IV.

TABLE IV
FAULT COVERAGE SUMMARY FOR AB LINES AND ABMS (ICCS THAT DETECT EACH FAULT)

	AB1	AB2	Comp
s@0	9	9	12
s@1	10	10	14
open	9	9	
short	12,13		

	SB1	SB2	SH	SL	SG	SD
s@open	9	9	12	14	15	-
s@close	13	12	11	11	11	-

C. SVF code outline

Each ICC corresponds to a combination of switching patterns (TBIC, ABMs), which are imposed by the 4-bit words shifted into the respective control structures. Since most of the ICCs represented in the preceding sections are intrusive, the EXTEST instruction must be loaded into the instruction register of the 1149.4 devices. The SVF program will therefore start by sending in the all-0 instruction code and checking that the sequences captured / shifted-from the device instruction registers will start by the binary sequence 10…, as defined in the IEEE standard (the bit closest to TDO must be 1, the following bit 0):

```
SIR XX TDI (... all-0s ...) TDO (0...01) MASK (0...03);
! XX: Length of the instruction registers
```

To set up each successive ICC, the corresponding 4-bit words will be shifted into the control structures of the TBIC and ABMs:

```
SDR YY TDI (...);
! YY: Length of the boundary-scan registers
```

Each ICC may be followed by an ATAP operation, requiring observation of AT2 and eventually control of AT1. The ATAP operations must be synchronised with the 1149.1 test controller, to ensure that the required ICC is stable while AT1 is driven / AT2 is observed.

Additionally, the output of the TBIC or ABM comparators must be observed in the case of ICCs #2, #3, #12, and #13. When this is the case, the *following* ICC must be set up using the following SVF expression:

```
SDR YY TDI (...) TDO (...) MASK (...);
! YY: Length of the boundary-scan registers
```

This SVF expression specifies the expected responses in those bit positions that capture the TBIC or ABM comparator outputs (the execution time is the same).

V. CASE STUDY

The National Semiconductor STA400 (dual 2:1 analog mux with IEEE 1149.4) chip was used to illustrate the application of our proposed method [5, 6, 7]. The 1149.4 test architecture of this device includes 11 ABMs, as represented in figure 4. Notice that all functional pins (either digital or analog) have an associated ABM, so there is a total of 48 bits (11 x 4 bits for the ABMs + 4 bits for the TBIC) in the BS register.

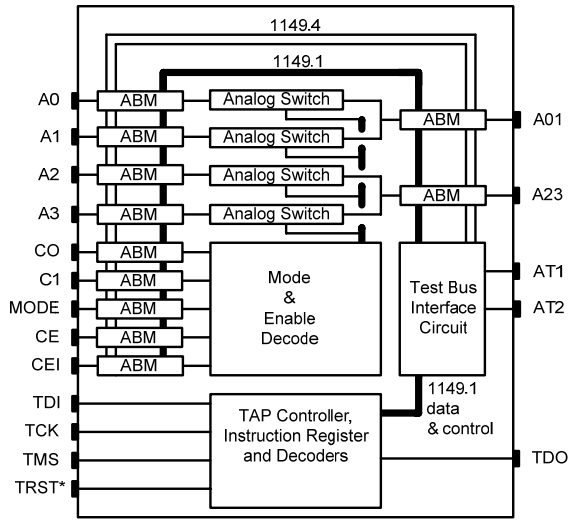


Fig. 4. National Semiconductor's STA 400 1149.4 chip.

The total number of TCK cycles required by our proposed method may be represented by the following expression:

$$13 + 2 \cdot \#bitsIR + [\,(\#ABMs \cdot 5)+8\,] \cdot (\#\,bitsBSR+5)$$

Where:

#bitsIR: Number of bits in the device's instruction register

#bitsBSR: Number of bits in the device's boundary-scan register

#ABMs: Number of ABMs

In the case of the STA400, we have #bitsIR=20, #bitsBSR=48 and #ABMs=11. Consequently, 3.392 TCK cycles are required to complete the proposed integrity check. For a TCK frequency of 20 MHz, the total integrity check test time is approximately 170 µs. The main sections of the SVF code for this experiment may be represented as follows:

```
TRST ON;
TRST OFF;
STATE IDLE;
!  Load Sample/Preload; Length of the STA400 instruction register: 20
SIR 20 TDI (7FFF8) TDO (00001) MASK (00003);

! ICC #1 – TBIC: S9, S10 closed; all ABM switches open
!  Length of the STA400 BS register: 20+24+4=48
HDR 20 TDI (00000);
TDR 24 TDI (000000);
SDR 4 TDI (0);
! Load Extest
SIR 20 TDI (0);
! Pause SVF, observe AT1 and AT2, continue SVF

! ICC #2 – TBIC: S1, S4, S9, S10 closed; all ABM switches open; capture
output of TBIC comps
SDR 4 TDI (6);
! Pause SVF, observe AT1, AT2, continue SVF

! ICC #3 – TBIC: S2, S3, S9, S10 closed; all ABM switches open; capture
output of TBIC comps
SDR 4 TDI (A) TDO (4) MASK (C);
! Pause SVF; observe AT1, AT2, AT1 Comp, AT2 Comp, continue SVF

! ICC #4 – TBIC: S5, S8, S10 closed; all ABM switches open
SDR 4 TDI (5) TDO (8) MASK (C);
! Pause SVF, apply VH in AT1, observe AT2, AT1 Comp, AT2 Comp,
continue SVF

! ICC #5 – TBIC: S6, S7, S9 closed; all ABM switches open
SDR 4 TDI (1);
! Pause SVF, apply VH in AT1, observe AT2, continue SVF

! ICC #6 – TBIC: S5, S6 closed; all ABM switches open
SDR 48 TDI (C);
! Pause SVF, observe AT1 and AT2, continue SVF

! ICC #7 – TBIC: S5, S10 closed; all ABM switches SB1 and SB2 closed
HDR 20 TDI (33333);
TDR 24 TDI (333333);
SDR 4 TDI (4);
! Pause SVF, observe AT1, continue SVF

! ICC #8 – TBIC: S6, S9 closed; all ABM switches SB1 and SB2 closed
SDR 4 TDI (8);
! Pause SVF, observe AT2, continue SVF

HDR 0;
TDR 0;

! ICC #9, ICC #10, and ICC #11 – TBIC: S5, S6 closed; ABM [A0]: SB1, SB2
closed
SDR 48 TDI (300000C00000);
! ICC #9 Pause SVF, apply VH in AT1, observe AT2, continue SVF
! ICC #10 Pause SVF, Apply VL in AT1, observe AT2, continue SVF
! ICC #11 Pause SVF, Observe AT1 and AT2, continue SVF
```

```
! Repeat the SVF commands for ICCs #9, #10, and #11 for each remaining
ABM
(...)

! ICC #12 – TBIC: S5, S6 closed; ABM[A0]: SB1, SH closed
SDR 48 TDI (D00000C00000);
! Pause SVF, Observe AT1 and AT2, continue SVF

! ICC #12 – TBIC: S5, S6 closed; ABM[A2]: SB1, SH closed
! Check the output of the comparator in the ABM
SDR 48 TDI (0D0000C00000) TDO (800000000000) MASK
(800000000000);
! Pause SVF, Observe AT1 and AT2, AT1 Comp, AT2 Comp, continue SVF
! Repeat the previous SVF command for each remaining ABM
(...)

! ICC #13 – TBIC: S5, S6 closed; ABM[A0]: SB2, SH closed
! Check the output of the comparator in the ABM
SDR 48 TDI (E00000C00000) TDO (000000000008) MASK
(000000000008);
! Pause SVF, Observe AT1 and AT2, AT1 Comp, AT2 Comp, continue SVF
! ICC #13 – TBIC: S5, S6 closed; ABM[A2]: SB2, SH closed
SDR 48 TDI (0E0000C00000);
! Pause SVF, Observe AT1 and AT2, continue SVF
! Repeat the previous SVF command for each remaining ABM
(...)

! ICC #14 – TBIC: S5, S6 closed; ABM[A0]: SB1, SB2, SL closed
SDR 48 TDI (700000C00000);
! Pause SVF, Observe AT2, continue SVF
! ICC #14 – TBIC: S5, S6 closed; ABM[A2]: SB1, SB2, SL closed
! Check the output of the comparator in the ABM
SDR 48 TDI (070000C00000) TDO (000000000000) MASK (800000000000);
! Pause SVF, Observe AT2, AT1 Comp, AT2 Comp, continue SVF
! Repeat the previous SVF command for each remaining ABM
(...)

! ICC #15 – TBIC: S5, S6 closed; ABM[A0]: SB1, SB2, SG closed
! Check the output of the comparator in the ABM
SDR 48 TDI (B00000C00000) TDO (000000000000) MASK
(000000000008);
! Pause SVF, Observe AT2, AT1 Comp, AT2 Comp, continue SVF
! ICC #15 – TBIC: S5, S6 closed; ABM[A2]: SB1, SB2, SG closed
SDR 48 TDI (0B0000C00000);
! Pause SVF, Observe AT2, continue SVF
! Repeat the previous SVF command for each remaining ABM
(...)
```

Notice that various SVF commands are accompanied by a comment indicating that ATAP operations are required before proceeding to the following command. This happens whenever it is required to drive / observe analog stimulae in the ATAP pins, for any given ICC (our SVF interpreter allowed single-command execution, so the synchronisation between the TAP controller and ATAP equipment was established manually).

VI. Conclusion

The work described in this paper addressed the development of an integrity check method for those test blocks that were added by 1149.4 to the 1149.1 test architecture (ATAP, TBIC, AB lines, ABMs). The nature of these blocks dictated the use of a hybrid fault model, comprising single faults of three types: s@0 / s@1, s@op / s@cl, and opens / shorts. The proposed integrity check procedures ensure nearly 100% fault coverage, leaving only the ABMs' SD switch untested. The test speed, measured in number of TCK cycles, was presented, and a validation case study was described based on the well-known 1149.4 STA400 chip from National Semiconductor.

The proposed method is independent of the board-level test infrastructure topology. It is possible to have one or more 1149.1 TAPs at board-level, and the ATAP interconnections may range from a single ATAP to as many ATAPs as there are 1149.4 chips. The assumption of single faults and the complete coverage of open, short and ss@ faults in each ATAP, make the proposed integrity check procedures independent of the TDO-TDI and AT1/AT2 interconnect scheme.

Our proposed solution was implemented for the STA400 1149.4 chip manufactured by National Semiconductor. The TAP controller was implemented in the form of an SVF interpreter developed in LabView, and used a Göpel Electronic GmbH 1149.1 controller board. The results of this work are particularly important in the case of 1149.4-based debug strategies for MS circuits, a pre-production test scenario where the 1149.4 extensions play a main role. The limitations of the proposed integrity check method are essentially related to the typical ABM topology, which places the SD switch out of reach in the general case (except in the case of analog output pins associated with a core circuitry that enables the propagation of known test signals). However, and since our main operating scenarios may benefit from improved ABM topologies, it becomes possible to achieve 100% fault coverage by redesigning the ABM switching structures as proposed in [9]. Future work includes the development of additional test configurations that will enable 1149.4 board-level integrity check (TAP + ATAP only), and 1149.4-compliance checking for ASIC designs.

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