FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

A Study on Digitally Controlled Oscillators for All-Digital Phase-Locked Loops

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October 15, 2015

U.PORTO
FEUP FACULDADE DE ENGENHARIA UNIVERSIDADE DO PORTO

MIEEC - MESTRADO INTEGRADO EM ENGENHARIA ELETROTÉCNICA E DE COMPUTADORES | **2014/2015**

A Dissertação intitulada

"A Study on Digitally Controlled Oscillators for All-Digital Phase-Locked Loops"

foi aprovada em provas realizadas em 15-10-2015

o júri

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Abstract

The "Phase Locked Loop" (PLL) primary uses are in clock recovery and frequency synthesis applications, being present in several technological devices. The interest relatively to the "All-Digital PLL" (AD-PLL) type of architecture has been growing due to the benefits that these present over its analog counterparts, such as lower power consumption, less area, lower phase noise, better testability and stability.

The digitally controlled oscillator (DCO) is the block that dominates the overall performance of the AD-PLL. It is the responsible for most of the power consumption and it is extremely susceptible to process, supply voltage and temperature (PVT).

In this work it is studied and presented a new DCO implementation technique with the purpose of producing an extended and linear frequency range, and with that accomplish an high level of PVT immunity when compared with other approaches. It was projected a pseudo differential DCO, respective digital control circuit and buffer recurring to CMOS 130nm process with Radio Frequency (RF) transistors.The frequency range goes from 3.89 GHz to 5GHz for extreme PVT, with power consumption of 17.5 and 18.03mW respectively.

Resumo

As "Phase Locked Loop" (PLL) são utilizadas principalmente em aplicações de recuperação de relógio e síntese de frequências, estando presentes nos mais variados dispositivos tecnológicos. O interesse relativamente ao tipo de arquitetura "All-Digital PLL" (AD-PLL) tem vindo a aumentar devido aos benefícios que estas apresentam face às suas congéneres analógicas, nomeadamente no menor consumo de potência, menor área, menor ruído de fase, melhor testabilidade e estabilidade.

O oscilador controlado digitalmente (DCO, de "Digitally Controlled Oscillator") é o bloco que mais condiciona o desempenho da AD-PLL. É o responsável pela maior parte do consumo de potência e é extremamente susceptível a variações de processo, tensão de alimentação e temperatura (PVT).

Neste trabalho é estudada e apresentada uma nova técnica de implementação de um DCO com o objetivo de síntese de frequência de operação extensa, linear, sendo demonstrado um elevado grau de imunidade a variação de condições PVT quando comparado com outras abordagens. Foi projectado um DCO pseudo diferencial, respetivo circuito de controlo digital e "buffer" em processo CMOS 130nm com transístores com modelos de rádio frequência. A gama de frequências de operação é 3.89GHz a 5GHz para variações extremas de PVT, sendo o consumo de potência respectivamente entre 17.5 e 18.03mW na referida gama de frequência.

Acknowledgements

I would like to express my gratitude to:

My family, especially to my mother, father, sister and brother, that supported me throughout my academic life, in its downs and highs.

My friends with whom I studied: Bruno Teixeira, Pedro Brito, Diogo Guimarães and José Sá. It was always a pleasure to study and spend time complaining about school with all of you.

My friends with whom I lived with: João Bernado Oliveira and Henrique Lopes. Above all, friends for live.

My FEUP supervisor, Cândido Duarte, that even when everything seemed lost, always tried to see the bright side, and keep the work on track. His contribution made it possible for me to be writing this document right now.

My supervisor at Synopsis, Joaquim Machado, that always gave his total collaboration, even when the schedule was tight.

And finally to FEUP, that gave me a lot of headaches in these past 5 years.

João Cruz

"Never take anything for granted.
If you do so, the disappointment will be greater than ever."

João Cruz

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Abbreviations and Acronyms

ADPLL	ALL Digital Phase Locked Loop
DCC	Digitally Controlled Capacitor
DCDE	Digitally Controlled Delay Element
DCO	Digitally Controlled Oscillator
DCV	Digitally Controlled Varactor
DLF	Digital Loop Filter
DRO	Differential Ring Oscillator
EMI	Electro Magnetic Interference
FD	Frequency Divider
HDC	Hysteresis Delay Cell
ISF	Impulse Sensitivity Function
PLL	Phase Locked Loop
P2D	Phase Detector
PVT	Process, Voltage,Temperature
RF	Radio Frequency
SD	Spectral Density
SERO	Single Ended Ring Oscillator
SSB	Single Side Band
VCO	Voltage Controlled Oscillator
XCP	Cross Coupled Pair

Chapter 1

Introduction

1.1 Motivation

This dissertation was proposed with the intent to develop a digitally controlled oscillator (DCO) for all digital phase locked loops (AD-PLL). But, what is a phase locked loop (PLL) to begin with? What are its uses? According to [1], "a PLL is a feedback system that has the purpose to replicate and track the frequency and phase at the input when in lock", and its primary uses are in clock and data recovery and in frequency synthesis. PLL are present on a wide range of devices such as computers, cellular phones, televisions, radios, motor speed controllers, etc.

There are different types of PLLs, and although they have the same functionality, they differ significantly. In general, the PLL can be categorized as shown in Table 1.1.

Table 1.1: PLL types.

PLL	Phase Detector	Loop Filter	Controlled Oscillator
Analog or Linear PLL	Analog	Analog	Analog
Digital PLL	Digital	Analog	Analog
All Digital PLL	Digital	Digital	Digital

The AD-PLL importance has been rising in the last few years due to the expansion and development of nanometric CMOS technologies. The truth is that these kind of PLL consume less power, can be easily scaled down to another technology, do not need off-chip components such as capacitors and resistors, cover less area, possess lower phase noise, provide a faster lock-in time, better testability, stability, and portability over different processes [2].

As shown in Fig. 1.1, the AD-PLL is constituted by four major blocks: phase-to-digital converter (P2D), digital loop filter (DLF), DCO and frequency divider (FD). The P2D senses the phase difference between the reference clock F_{REF} and F_{CKV}, and converts it to a digital format. This control code is filtered by the LF and then is used to control the DCO, which generates an output frequency accordingly [3].

The DCO is the called "heart" of the AD-PLL and is appointed has the block that dominates its overall performance, since it is reported that 50–70% of the power consumption comes from it.

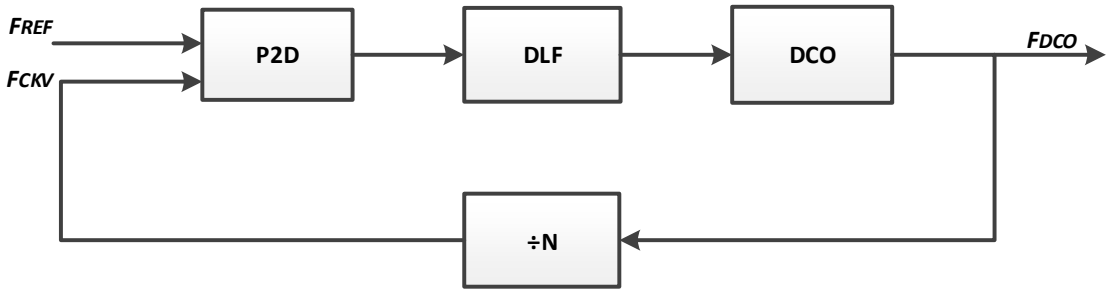


Figure 1.1: AD-PLL design according to [3].

This emphasizes the notoriety of the DCO and constitutes a motivation for the development of the present dissertation.

1.2 Dissertation Objectives

As previously mentioned, the performance of the DCO dictates the overall performance of the AD-PLL. Virtually all DCO circuits tend to be very susceptible to PVT variations, and even a single frequency oscillator is very difficult to compensate. The present dissertation particularly addresses this issue by proposing a technique to reduce the sensitivity to PVT effects in a target frequency range. The objectives of this Dissertation are the following:

- develop a DCO that possesses a large linear frequency range;
- assure that a well defined frequency range is obtainable, even under PVT variations.

1.3 Document Structure

The present document has the following structure:

- ***Chapter 2,"Background"*:** in this chapter are introduced some theoretical concepts regarding oscillators, so the reader is able to better understand the contents that are presented throughout the document. Some topics are introduced such as: oscillation creation, major oscillator topologies, frequency control, power consumption, phase noise and jitter;
- ***Chapter 3,"Bibliographic review"*:** in this chapter are introduced several controlled oscillator implementations that constitute a sample of the state of the art;
- ***Chapter 4,"Preliminary Study"*:** in this chapter are presented and studied in detail two oscillator implementations that served as foundation to the development of the proposed DCO. The performance of these topologies is evaluated under CMOS corners, some data is provided regarding power consumption, and it is given some information about their supply and temperature variation susceptibility;

- ***Chapter 5,"Proposed DCO"*:** introduces the major blocks of the proposed DCO and presents the results for process corners and PVT simulations that help to characterize the circuit performance;

- ***Chapter 6,"Conclusion"*:** it is made a critical review on the work developed and on the obtained results. Some proposals for future work are also presented.

Chapter 2

Background

In this chapter are going to be introduced several important concepts regarding oscillators, so the reader is able to better understand the contents that are going to be presented throughout the document.

The chapter is organised as follows: at first, are presented the conditions that an oscillator must satisfy in order to effectively produce a sustainable oscillation. Then, are explored and explained the major topologies employed in the development of controlled oscillators, being presented their principles of operation, advantages and disadvantages. Next, are introduced the concepts of phase noise and jitter, noise sources, and different jitter metrics. To conclude it is made a small theoretical comparison between the introduced topologies.

2.1 Barkhausen's Criteria

An oscillator is a feedback system that produces a continuous periodic output wave when excited by a DC input supply voltage [4] [5]. However, in order to actually do so, it must satisfy certain conditions that are known as the Barkhausen's criteria. On Fig. 2.1, it is presented a block representation of a negative feedback system, where $H(jw)$ is the amplifier open loop transfer function, with which is possible to calculate the closed loop transfer function $\frac{V_{in}(jw)}{V_{out}(jw)} = \frac{H(jw)}{1+H(jw)}$.

Oscillation can only be achieved once the system becomes unstable, something that happens when the denominator of $V_{in}(jw)/V_{out}(jw)$ is 0. With this, is possible to conclude that it only happens when $|H(jw)|$=1 and $\angle H(jw)$=180^o, conditions that are known as the Barkhausen's criteria. This criteria demands a 360^o phase shift around the loop, something that is achieved by the addition to the 180^o phase shift provided by the dc inversion, of a frequency-dependent 180^o phase shift given by the negative feedback [6]. To note that on the case of a positive feedback system (Fig. 2.2), $H(jw)$ must be able to generate the necessary 360^o phase shift by itself [6].

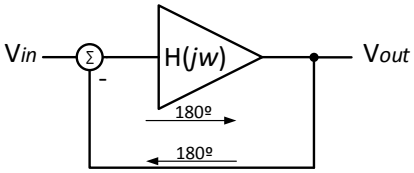


Figure 2.1: Negative feedback system.

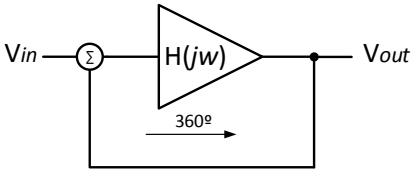


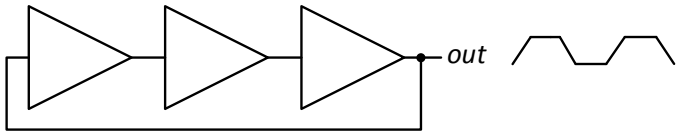
Figure 2.2: Positive feedback system.

2.2 Oscillator Topologies

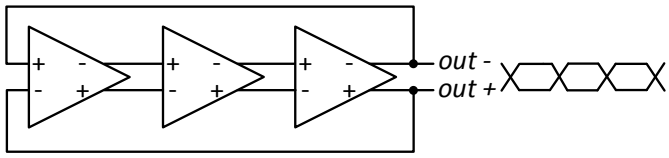
There are many different oscillator topologies such as the ring, quadrature, Colpitts, Hartley, crystal and LC tank oscillator. However, the ring and LC tank are the ones that are more highly used in controlled (digitally, current or voltage) oscillators, since they are especially suited for integration [5]. So, and since different oscillator implementations based on these topologies are going to be presented and studied throughout the Chapter 3, it is now made a small brief introduction on these two major topologies.

2.2.1 Ring Oscillator

The ring oscillator topology name literally represents what it is, i.e a group of inverter delay cells with their inputs connected to the outputs of the immediately previous cell, or by other words, in loop. This topology can be divided in two categories according to the type of signal in the ring: the single-ended ring oscillator (SERO) – Fig. 2.3a – and the differential ring oscillator (DRO) – Fig. 2.3b, which can be subdivided in fully and pseudo differential.



(a)



(b)

Figure 2.3: (a) Single-ended , and (b) differential implementations.

- ***Single-ended ring oscillator (SERO)***

The SERO implementation is composed by a ring with an odd number of stages constituted by inverter delay cells that can go from a simple common inverter, in the most basic case, to more complex cells, depending on the adopted frequency control strategy.

The ring oscillator topology is a positive feedback system, so its stages must provide the 360º phase shift on every loop to meet the Barkhausen's criteria. For this to happen, the dc inversion (180º) and the frequency-dependent phase shift must add up to 360º. Since the single pole of each stage transfer function can only deliver a maximum of 90º phase shift, it becomes clear that this approach can only be implemented with an odd number of stages equal or higher than 3.

The SERO implementation is power efficient, since the power dissipation occurs mostly during signal transitions. It is also capable of producing an output signal with full rail-to-rail voltage swing. On the other hand, there is some susceptibility to supply/substrate interference, and the constrain on the number of stages that, as previously explained must be odd, turns it undesirable for applications that require even multiphase outputs, like quadrature [7].

- ***Differential ring oscillator (DRO)***

The DRO implementation is composed by a ring with an even or odd number of stages formed by differential delay cells and can be divided, as previously stated, in two types: fully and pseudo differential. The fact that this implementation outputs are differential makes it possible to have an even number of stages, being only needed to cross the ring outputs to be able to create the 180º phase shift from dc inversion (Fig. 2.4).

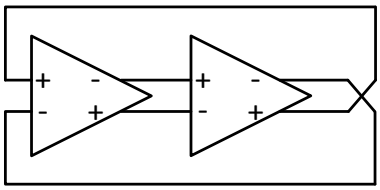


Figure 2.4: Two stages DRO.

The differences between a fully and a pseudo differential delay cell are quite small: the fully differential configuration is based on a differential pair, and the pseudo differential configuration is based on two independent inverters without the tail current transistor [8]. Yet, there are different benefits and drawbacks that characterize them.

According to [7], the fully differential implementation advantages are the possibility of using an odd or even number of stages and a massive interference rejection. On the other hand it has a lower signal swing than the SERO implementation.

The pseudo differential implementation has the ability to provide a signal swing close to the SERO implementation and provides some interference rejection, although not at the same extent has the fully differential approach [7].

- ***Ring oscillator frequency control***

To comprehend any DCO implementation, it is necessary to understand the principles behind frequency control. So, in order to help in this matter, they are now discussed below.

The oscillation frequency for a ring oscillator with equal stages is given by $f_{osc} = \frac{1}{2NT_p}$, where N is the number of stages and T_p the propagation delay of each cell, which shows that the values of N or T_p must be manipulated in order to control the frequency of oscillation.

A higher number of stages provides a larger quantity of possible outputs, but difficulties the production of higher frequencies, increases the area and the global capacitance of the circuit. Such also leads to higher power consumption, making the selection of the number of stages an important step in ring oscillators design.

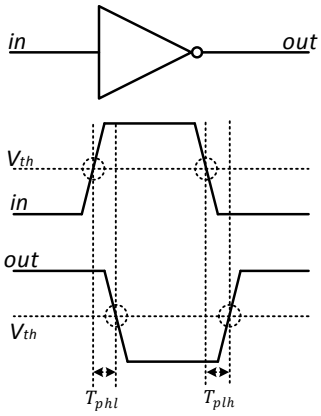


Figure 2.5: T_{phl} and T_{plh} representation.

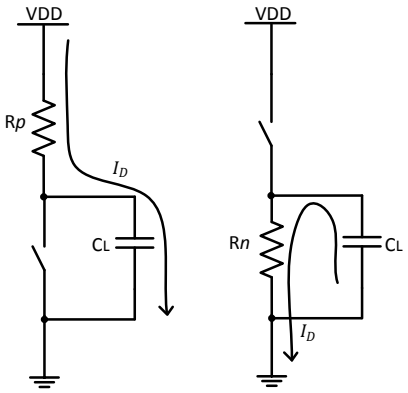


Figure 2.6: Common inverter operation.

Since in most cases the number of stages of a ring oscillator is fixed after its design, the best solution to control the output frequency is by manipulating T_p.

The propagation delay is given by $T_p = \frac{T_{plh}+T_{phl}}{2}$, where T_{phl} is the delay of an high to low (*H to L*) signal transition and T_{plh} the delay of a low to high (*L to H*) signal transition (Fig. 2.5). These propagation delays (always $\neq 0$) vary with the capacity of the driving current (I_D), to charge/discharge the load capacitance (C_L) – See Fig 2.6. With this in mind it is possible to introduce another manner of expressing the propagation delay: $T_p = C_L \cdot \Delta V / I_D$, where ΔV represents the voltage swing between the H and L states.

It is now possible to conclude that the control of T_p can be done with the manipulation of C_L or/and I_D.

2.2.2 LC Tank Oscillator

The LC tank oscillator is mainly composed by a capacitor, an inductor, and a cross coupled pair (XCP). The oscillation frequency is created by the relationship between the charge and discharge of the capacitor and with the variation of the magnetic field in the inductor. Initially, the fully charged capacitor starts discharging, causing the appearance of a magnetic field in the inductor. Once the capacitor is discharged, the magnetic field hits its peak and the polarity changes. The capacitor is then charged in the opposite direction until the magnetic field collapses completely. The cycle repeats itself giving birth to the pretended oscillation (Fig. 2.7) .

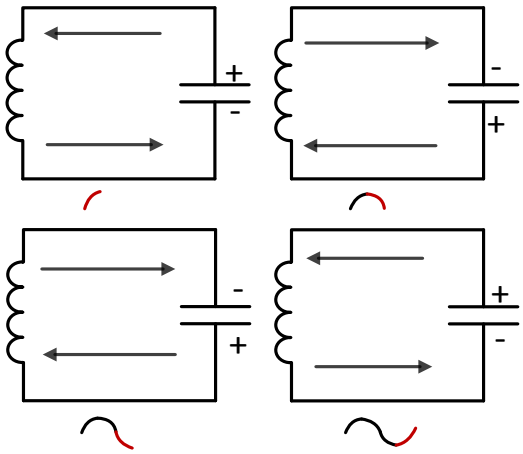


Figure 2.7: LC basics.

A simplified representation of a LC tank oscillator is shown in Fig. 2.8. The cross coupled pair (XCP) is represented by a negative resistance helps to compensate the LC losses and with that create a sustainable oscillation.

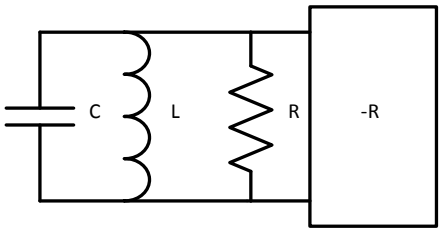


Figure 2.8: LC Tank basic representation.

The oscillation frequency is given by $F_o = \frac{1}{2\pi\sqrt{LC}}$, and as it can be seen there are two possible options to control the frequency: manipulate L or C. Since manipulating the value of L introduces Q factor (ratio of inductive reactance to its resistance at a given frequency) degradation, the manipulation of C became preferable.

- ***CMOS power consumption***

The awareness concerning power consumption has been growing in the past few years, since high power consumption poses a major obstacle in integration and downscaling. It is important then, to take a look at its various components and causes.

Power consumption is given by $P_{TOTAL} = P_{switch} + P_{short} + P_{leak}$ [9], where P_{TOTAL} represents the total power consumption, P_{switch} the switching power, P_{short} the short circuit power and P_{leak} the leakage power.

- **Pswitch:** caused by the charge and discharge of the load capacitance and given by $P = N \cdot C_L V_{\mathrm{DD}}^2 f$, where N represents the number of stages, C_L the load capacitance, V_{DD} the

supply voltage, and f the switching frequency. One way to reduce this parcel is to reduce V_{DD} and/or C_L;

- **Pshort:** due to non-zero rise/fall times; depends on V_{DD} and transition times. By minimizing P_{switch}, it is also reduced;

- **Pleak:** due to leakage currents of transistors in OFF state; depends on the technology (PMOS/NMOS). Becomes highly important with the decrease of the transistors size, and it is proportional to the number of transistors [9].

2.3 Phase Noise and Jitter

According to [10], phase noise can be described as "short-term random frequency fluctuations of a signal, and is measured in the frequency domain being expressed as a ratio of signal power to noise power measured in a 1 Hz bandwidth at a given offset from the desired signal".

Jitter is the time-domain effective measurement of phase noise and represents the undesired deviation from true periodicity of an assumed periodic signal (expressed in $\pm$ ps), which can occur on either the rising edge or the falling edge of a signal, and is not uniform over all frequencies [2].

Noise sources alter the frequency spectrum and the desired transition intervals of the output waves produced by the oscillator and in general can be classified in two groups: deterministic noise and random noise. Deterministic noise sources are: crosstalk between adjacent signal traces, electro magnetic interference (EMI) radiation on a sensitive signal path, noise from power layers of a multilayer substrate and simultaneous switching of multiple gates to the same logic value. Random noise sources are: thermal noise (associated with electron flow in conductors), shot noise (due to potential barrier in semiconductors) and flicker or $\frac{1}{f}$ noise (associated with crystal surface defects in semiconductors) [11]. The output of a practical stable oscillator is given by (2.1)

$$V_{out}(t) \quad = \quad V_o(1+\alpha(t)) \cdot \sin(2\pi f_o + \phi(t)) \tag{2.1}$$

where α and ϕ are function of time and represent respectively the amplitude and phase perturbations caused by noise. Two measurements of the phase noise are common, the spectral density (SD) of phase fluctuations and the single side band (SSB) phase noise. Since SD is twice of SSB it is presented only the SSB expression here for white noise

$$L(f_{off}) \quad = \quad \frac{\Gamma_{rms}^2}{8\pi^2 f_{off}^2} \cdot \frac{i_n^2}{\Delta f \cdot q_{max}^2} \tag{2.2}$$

where Γ_{rms} represents the rms value of the impulse sensitivity function (function that measures the sensitivity of every point in the wave form to perturbations), $\frac{i_n^2}{\Delta f}$ is the single sideband power spectral density of noise current source and f_{off} is the offset frequency from the carrier (see Fig. 2.9). Below the corner frequency the flicker noise has dominance over the white noise, which with the decrease of size of transistors in CMOS processes poses a major problem since these transistors

have higher corner frequencies. In addition, this noise is not only limited to low frequencies but it tends to be up converted to high frequencies [12].

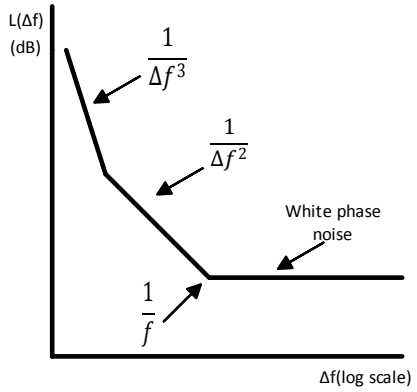


Figure 2.9: Phase noise with offset frequency.

In oscillators, jitter can be expressed by 3 different metrics. They are now stated below:

- **Cycle-to-cycle jitter:** variation of the output signal transition in relation to the one in the immediately previous cycle;
- **Period jitter:** maximum variation of the output signal transition from its ideal position;
- **Long-term jitter:** maximum variation of the output signal transition from its ideal position, over a large number of cycles.

2.4 Topologies Resume

To sum up and to provide an easy overview between the strengths and the weaknesses of both topologies, is now made a brief comparison between the ring and LC tank oscillator topologies.

Ring oscillators are generally characterized by having a small area, achieving oscillation at a low voltage, providing high frequencies at low power, having a wide tuning range and the possibility of delivering multiphase outputs. Nevertheless, its phase noise performance is poor and is very affected by PVT variations [11] [13].

LC tank oscillators, on the other hand, are best suited for radio frequency (RF) applications, because possess the best phase noise performance. However, this topology features an higher power consumption and area, as well as a lower tuning range [13] [14].

Chapter 3

Bibliographic Review

The last chapter gave a brief introduction about several aspects concerning oscillators with the intent to help to easily understand some concepts that are going to be explored in this and in the following chapters, but it did not give a look into the present state of art of DCOs. So, this chapter introduces several DCO implementations, shedding light into this matter.

The studied implementations are based on the previously introduced topologies SERO and DRO, using different digitally controlled delay elements (DCDE), and on the LC tank topology. In each implementation are presented the technology, supply voltage and the N-length digital input control word $D = D_{N-1} \cdots D_1 D_0$, as well as a small brief explanation on the tuning method and the results obtained by the authors. In the end it is made a small summary where are put up together the different specifications of every implementation.

3.1 Ring Oscillator With Tristate Delay Cells

The DCO presented on Fig. 3.1 was developed using TSMC 0.18um CMOS process with a supply voltage of 1.8 V, and is controlled by an 8 bit binary code word D[0:7] [15]. The oscillator is composed by 8 binary weighted rings connected in parallel, each one with 3 equal stages formed by the proposed tristate delay cells.

As it can be seen on Fig. 3.1, the nodes A, B and C are common to all the rings, making C_L equal for every cell. The value of D defines if there is signal propagation from *In* to *out* by controlling the transmission gates connected to the inputs of the inverter. With this, it is possible to control the rings that are enabled, regulating the amount of current that charge/discharge C_L, effectively controlling the propagation time, and therefore the output frequency.

This implementation has a frequency range that goes from 316 MHz to 1165 MHz (Fig. 3.2), with a power consumption of 4mW to 28mW, and presents a phase noise of 114 dBc/Hz @ 1 MHz offset of the frequency of 1GHz.

Due to the fact that this oscillator is composed by 8 parallel binary weighted rings, its use is not recommended when area is a constraint. Also the power consumption is not very attractive since

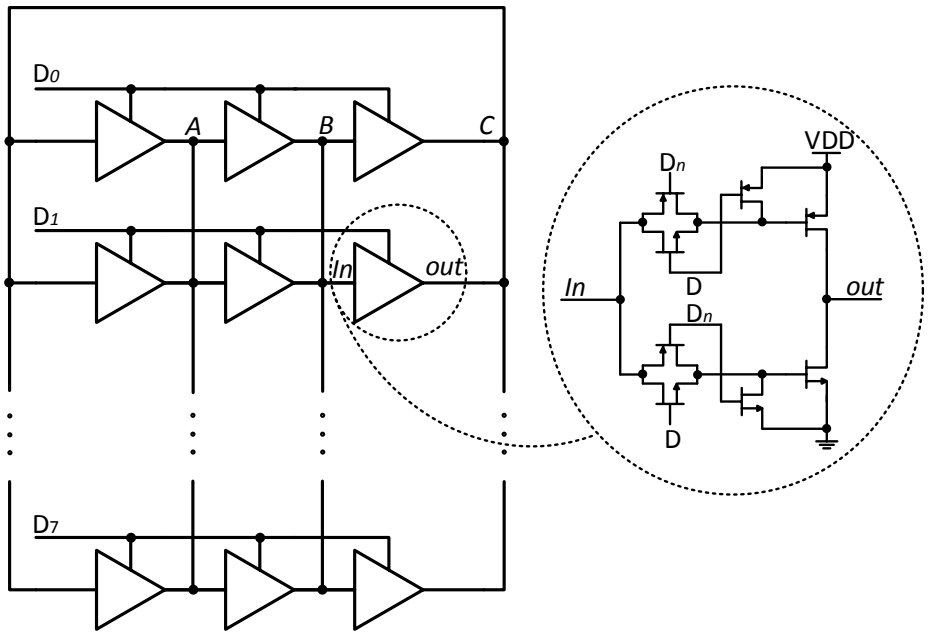


Figure 3.1: DCO with tristate delay cells proposed in [15].

it is very high for frequencies that at best go slightly above 1 GHz. On the other hand, the phase noise performance is very good and the voltage output swing comes very close to full rail-to-rail.

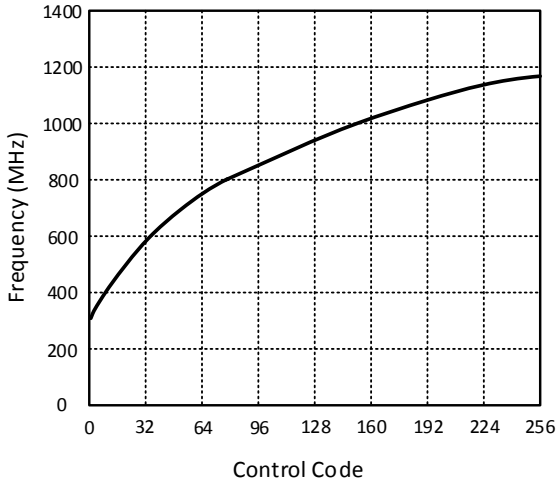


Figure 3.2: Frequency versus control code characteristic.

From simulations of a non-optimized implementation of this oscillator is it possible to refer that in presence of a proper transistor sizing, it is possible to achieve a highly linear frequency characteristic and a duty cycle very close to 50%.

3.2 Ring Oscillator With Fine and Coarse Tuning Stages

The DCO present in Fig. 3.3 was developed using 32nm PTM technology with a supply voltage of 0.9V, and is controlled by a 12 bit code word D[0:11] [16]. It is composed by two coarse tuning stages controlled by D[0:5], by one fine tuning stage controlled by D[6:11], and by an AND logic gate that acts like a circuit enable, all connected in a ring topology [16].

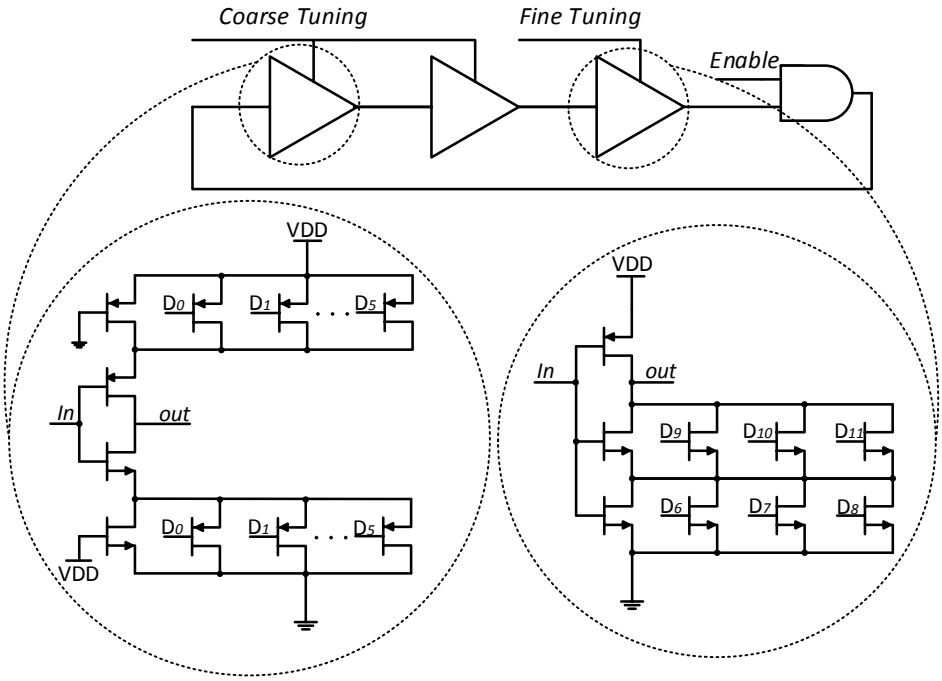


Figure 3.3: DCO with coarse and fine tuning proposed in [16].

The coarse stage cell is formed by an inverter with a dual PMOS network (Fig. 3.3). By enabling the different PMOS transistors of the networks, it is possible to manipulate the total current that charge/discharge the load capacitance, and therefore control T_P. The fine stage cell operation is very similar, but on this case is only possible to control the discharge current.

The oscillator possesses a rather small frequency range that goes from 570 MHz to 800 MHz with a power consumption that varies from 3.4 mW to 3.8 mW. From simulations of a non-optimized implementation of this oscillator it is possible to say that it possesses a very linear frequency characteristic and due to the use of the dual network, instead of a single one like in [17], it is possible to achieve duty cycles very close to 50%. However, the linearity of this characteristic degrades with the increase of the tuning range and the use of the fine delay cell becomes fruitless, because it starts to be very difficult to properly interlink the frequency steps given by the coarse and fine tuning stages.

3.3 Multiple Fine Tuning Stages DCO

The DCO shown in Fig. 3.4 was developed based on TSMC 180nm technology with a 1.8V supply voltage, controlled by a 15 bit binary code word D[0:14], where D[0:9] controls the fine stage and D[10:14] the coarse stage [18]. However, the actual oscillator control is done by several thermometer code words that are created by extra logical circuits that have D as input.

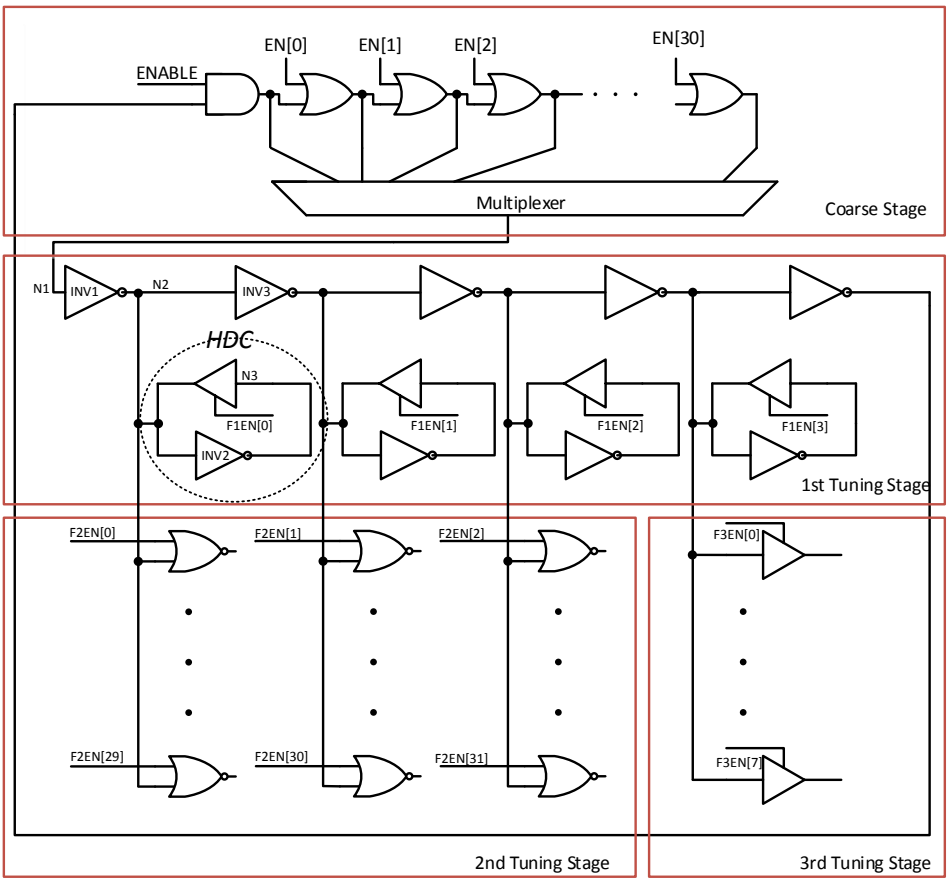


Figure 3.4: DCO with multiple fine stages proposed in [18].

As it can be seen in Fig. 3.4, the coarse tuning stage is formed by a delay line made of 31 OR gates and a 32-1 multiplexer (built with transmission gates), allowing to select 1 of 32 different delay paths. Since the path chosen varies according to the desired frequency, there are some redundant OR gates that are disabled to save power ($EN = 1 \Rightarrow disabled / EN = 0 \Rightarrow enabled$).

The fine tuning stage is divided in 3 sub stages that provide different decreasingly delay steps from stages 1 to 3. The first sub stage is composed by 4 hysteresis delay cells (HDC), the second by a 32 two–input NOR digitally controlled varactor (DCV) and the third by a 8 tri-state inverter DCV.

The logic behind the coarse stage is quite simple: by increasing the path length, the propagation time increases and a lower output frequency is generated. On the other hand, the logic behind

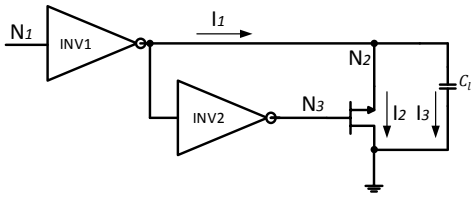


Figure 3.5: HDC operation in *H-L* transition.

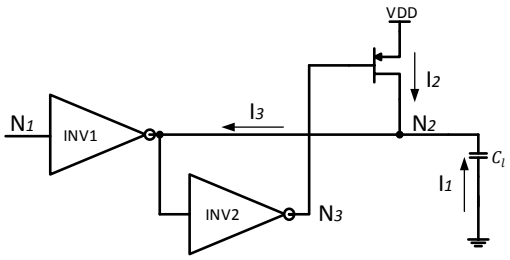


Figure 3.6: HDC operation in *L-H* transition.

the fine stage is not that straightforward. The second and third fine tuning sub stages purpose is to control C_L. By setting the control signals (F2EN[0]:F2EN[31]) and (F3EN[0]:F3EN[7]) to 1 or 0, it is possible to achieve a different gate capacitance [19].

The operation of the first fine tuning sub stage is a little bit more complex and it is now explained with the help of Figs. 3.5 and 3.6. To note that it is assumed that the HDC is enabled.

When the signal in the node N_1 makes a *H-L* transition, the propagation delay introduced by the inverter INV2 makes the signal in the node N_3 to stay in high level for a while, keeping the NMOS of the tristate conducting. With this, part of the current I_1 that would charge C_L is sunk (I_2), being C_L charged only by $I_3 = I_1 - I_2$ (Fig. 3.5). On the other hand, when the node N_1 makes a *L-H* transition, the PMOS of the tristate keeps charging C_L (I_2) , being C_L discharged only by $I_3 = I_1 - I_2$ (Fig. 3.6) [20].

Table 3.1: Steps and range of stages.

	Coarse-Tuning	1^{st} Fine-Tuning	2^{nd} Fine-Tuning	3^{rd} Fine-Tuning
Range (ps)	3780	135.3	83.2	7.6
Step (ps)	120.12	38.4	3.18	0.95

This implementation frequency range goes from 205MHz to 925MHz and has a power consumption of 255 μW at 205 MHz, which is very low. It may seem counter intuitive, but in this implementation, the power consumption increases with the decrease in the frequency. When the oscillator generates the 205MHz frequency, the varactors are "applying" more load on the nodes and more importantly the HDC are active, resulting on higher power consumption.

From the data in Table 3.1 it is easy to see that the coarse and fine tuning stages of this oscillator give it a very good step resolution. But, on the other hand, there is a large amount of extra complex control circuits that must be implemented in order to effectively create the necessary control signals to all of these stages.

From simulations of a non-optimized implementation of this oscillator it is possible to say that it possesses a very linear frequency characteristic. Anyway, several changes could be made. The use of the logic gate varactors does not pay off either in area or power consumption in relation to the use of controlled capacitors made by connecting the source and drain of a transistor together. Another possible variation would be replacing the HDCs for a larger number of varactor elements, but this would depend on the objectives, since the use of HDCs reduces the size of the varactors to a third but at the cost of higher power consumption.

3.4 Differential Ring Oscillator With Control Network

The DCO shown in Fig. 3.7 was developed using UMC 130nm process with a 1.2V supply voltage, and is controlled by a 3 bit binary code word D[0:2] [21]. The oscillator is a two stage DRO with fully differential delay cells controlled by a digitally programmable resistor that regulates the tail current and with that controls T_p.

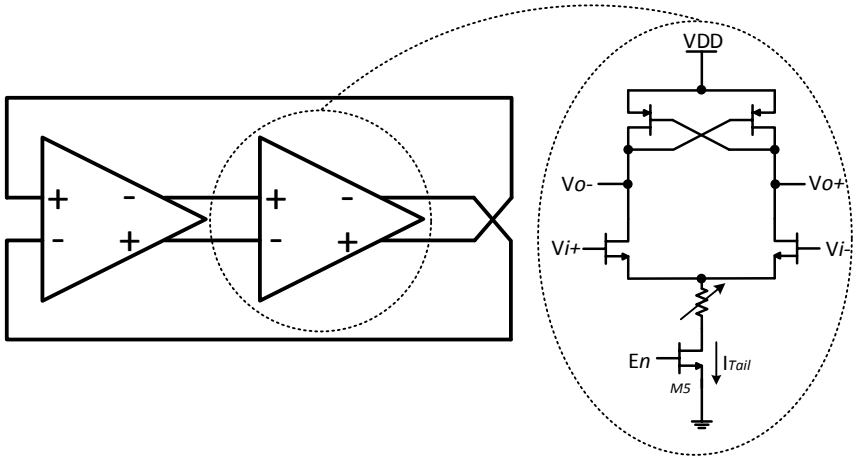


Figure 3.7: Differential DCO proposed in [21].

This implementation has a wide frequency range that goes from 1.8GHz to 9GHz (Fig. 3.8) with a power consumption no higher than 5mW. Also it presents a very good phase noise performance with -121.7 dBc/Hz @ 10MHz offset from the frequency of 5.6GHz.

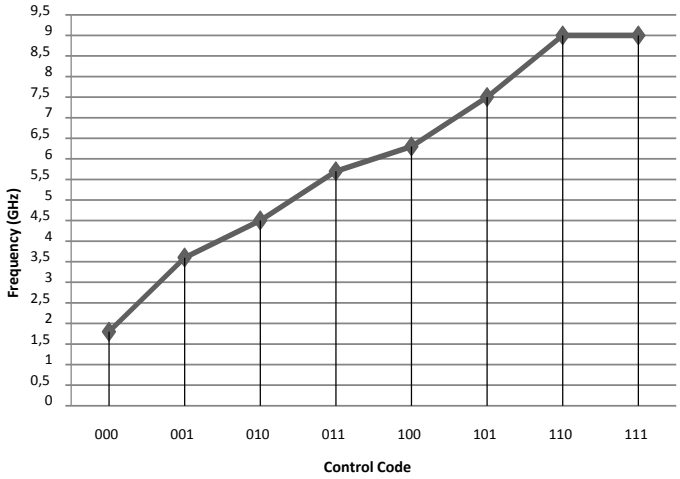


Figure 3.8: Frequency versus control code.

From a quick study of this oscillator it is possible to say that its output voltage swing is not as higher as the implementations discussed until now, something that it is not unexpected since it makes use of fully differential cells. The programmable resistor in [21] is done by using actual

resistors, but for study effects, it was also tested another implementation using only transistors. With the first is possible to achieve a much better power consumption performance and frequency characteristic linearity, but with the cost of a larger area. So it is up to the designer to choose according to the project objectives.

3.5 Differential Ring Oscillator With Maneatis Loads

The oscillator shown in Fig. 3.9 is not actually a DCO but in fact a voltage controlled oscillator (VCO) and was developed using UMC 0.13um technology. It is based on a two stage DRO with fully-differential delay cells and is controlled by varying the supply voltage from 0.58V to 1.6V [22]. The delay cell possesses two PMOS symmetric loads, called Maneatis loads, which are used to cancel resistive effects [8] and to speed up the signal transitions, simultaneously maximizing the voltage swing at the output [13].

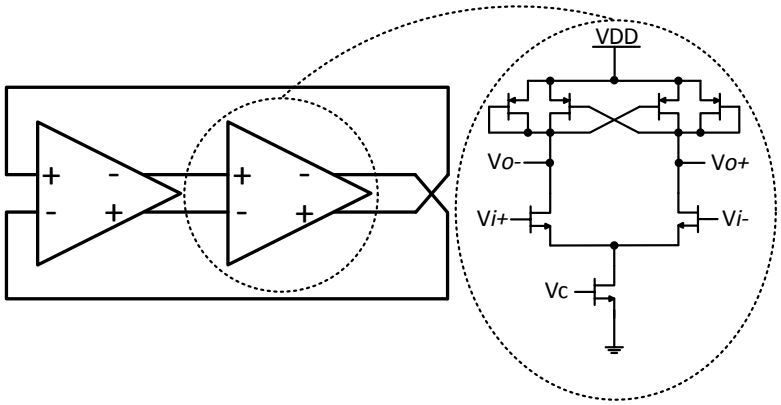


Figure 3.9: VCO with Maneatis loads proposed in [22].

This implementation has a frequency range that goes from 1 GHz to 9.4 GHz with a power consumption no higher than 6 mW. Also it presents a good phase noise of -112.3dBc/Hz @ 10 MHz offset from the frequency of 6GHz.

3.6 Differential Ring Oscillator With Latch Control

In this section are presented two different oscillator implementations that are also not actually DCOs but in fact VCOs.

The first implementation (Fig. 3.10) was developed using 0.6um CMOS technology with a supply voltage of 3V and is based on a 3 stage DRO with pseudo-differential delay cells [23].

The NMOS transistors M3 and M4 control the maximum voltage present on the gates of the latch transistors M1 and M2, controlling by this way the driving current that charges C_L. When V_{ctr} is low, the strength of the latch gets weaker and the driving current increases, increasing the frequency. When V_{ctr} is high the exact opposite happens.

This implementation has a tuning range that goes from 0.75 GHz to 1.2 GHz with a maximum power consumption of 30 mW and a phase noise of 101 dBc/Hz @ 100 kHz offset from the frequency of 900MHz.

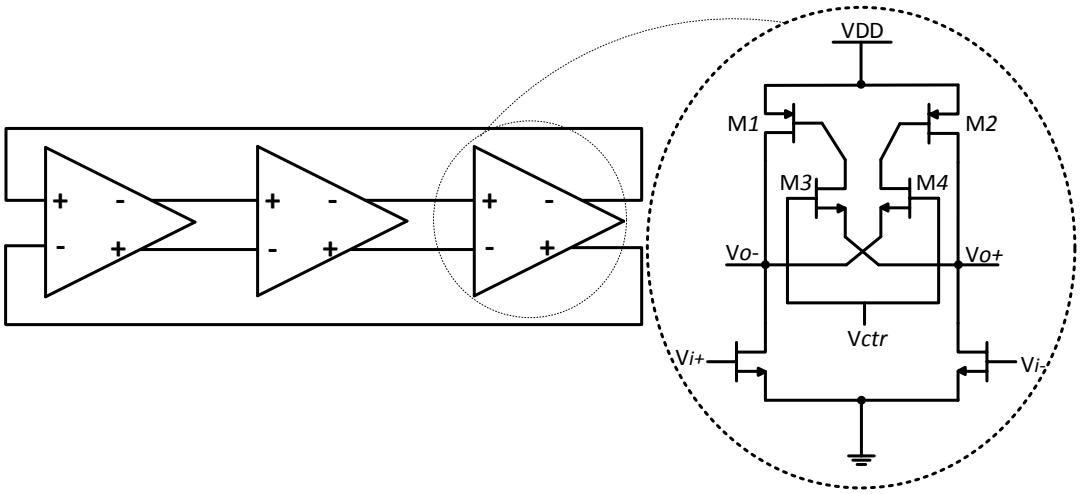


Figure 3.10: VCO with latch control proposed in [23].

The second configuration is a dual-loop implementation of the previous one and was developed using TSMC 0.18um technology with a supply voltage of 1.8V [24].

As it can be seen on Fig. 3.11, it was added the transistor pair $M_{5,6}$ that act like another set of inputs. These receive the signal from the output of previous stages and with this the output nodes of the cells are pre charged, diminishing the charging time [23–25]. This implementation has a tuning range that goes from 5.18 GHz to 6.11 GHz and possesses a phase noise of -99.5dBc/Hz @ 1 MHz offset from the frequency of 5.79GHz.

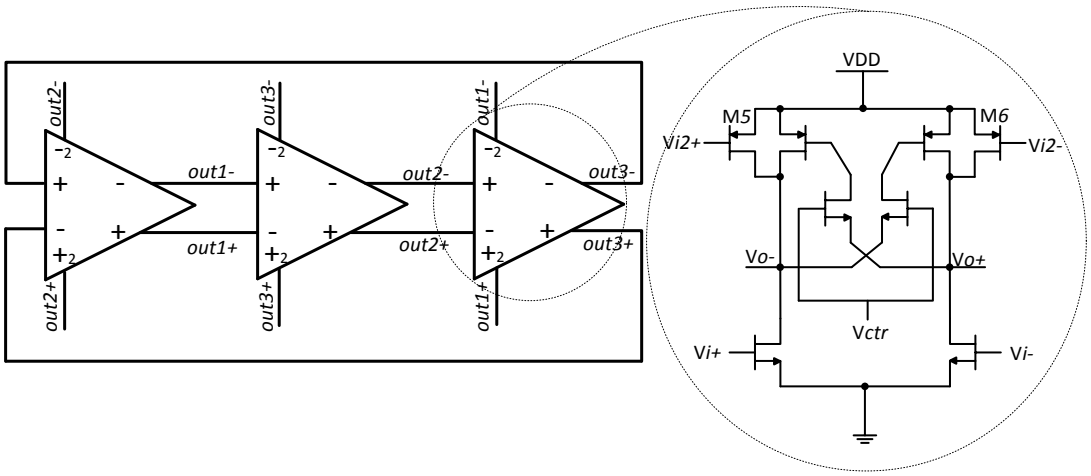


Figure 3.11: Dual loop VCO proposed in [23], and also developed in [24, 25].

From a quick simulation of these oscillators one can concludes that is possible to achieve a fairly higher frequency range than the ones of the articles [23–25] with a good degree of linearity.

With this kind of control it is only possible to use a part of the complete frequency characteristic, since for some V_{ctr} values it becomes erratic and non linear. So during the development, the designer must choose a V_{ctr} interval with which is possible to effectively obtain a proper frequency characteristic.

3.7 LC Tank Oscillator

The DCO shown in Fig. 3.12 is a 11 bit LC tank oscillator developed in 90nm technology with a supply voltage of 1.2V. The oscillator is composed by capacitor DCVs, an inductor and by a cross coupled PMOS/NMOS transistors that form a negative resistance [26].

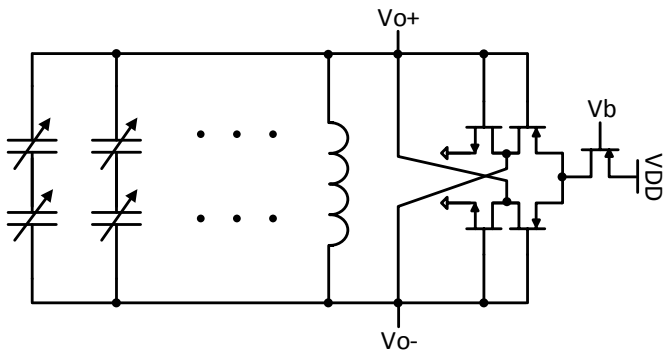


Figure 3.12: LC DCO proposed in [26].

As previously stated in Section 2.2.2, this kind of oscillator produces an output frequency given by $F_o = \frac{1}{2\pi\sqrt{LC}}$, which can be controlled by manipulating C. In order to do so, are used DCVs that allow to produce different C values by setting the capacitors in one of two levels: C_{ON}, higher capacitance, or C_{OFF}, lower capacitance ($\neq 0$). The capacitance tuning units are performed by PMOS transistors with their drain/source tied together.

The 11 bits are divided to be applied in a 5 bit fine tuning bank and in 6 bit coarse tuning bank giving this way 32 tuning levels for the fine tuning stage and 64 for the coarse tuning producing 2048 tuning levels. It is relevant to mention that, the tuning range of the fine bank was dimensioned so it is approximately equal to the coarse bank step.

This DCO is reported to have a capacitance range from 2 to 3 pF with a step size of 10aF, providing by this way, using a 1.8nH inductor, a tuning range from 3.05 to 3.65 GHz with an average step size of 4.5KHz. For 3.058GHz carrier frequency, the phase noise was measured as -118dBc/Hz @ 1MHz frequency offset. Although this implementation possesses a very good frequency step and phase noise, the use of an inductor increases the area greatly.

3.8 Chapter Summary

Table 3.2 summarizes the most important parameters: technology, number of bits, power supply, power consumption, phase noise and the topology – to help the reader to get a broader and easier global view of the implementations characteristics.

Table 3.2: Summary of presented implementations.

Design	$L_{\text{feat.}}$ (μm)	V_{dd} (V)	Bit word	Δf (GHz)	P_{diss} (mW)	Phase noise (dBc/Hz)	Topology
3.1	0.18	1.8	8	0.316 – 1.165	4 – 28	-114 @ 1MHz	SERO
3.2	0.032	0.9	12	0.57 – 0.8	3.4 – 3.8	—	SERO
3.3	0.18	1.8	15	0.205 – 0.925	255 @ 205MHz	—	SERO
3.4	0.13	1.2	3	1.8 – 9	5 @ 9GHz	-121.7 @ 10MHz	DRO
3.5	0.13	0.58 – 1.6	V_{ctr}	1 – 9.4	6 @ 9.4GHz	-112.3 @ 10MHz	DRO
3.6 (SL)	0.6	3	V_{ctr}	0.75 – 1.2	30 @ 1.2GHz	-101 @ 100kHz	DRO
3.6 (DL)	0.18	1.8	V_{ctr}	5.18 – 6.11	—	-99.5 @ 1MHz	DRO
3.7	0.09	1.2	11	3.05 – 3.65	—	-118 @ 1MHz	LC Tank

Chapter 4

Preliminary Study

From the preliminary results, gathered during the simulation of non-optimized implementations of the several oscillators introduced in Chapter 3, it was possible to choose two solution to be studied in detail: the single and dual loop implementations of a three stages differential ring oscillator with latch control (Section 3.6). The frequency range was in the GHz scale, the power consumption was not extremely high, the phase noise at the center frequency was above -100 dBc/Hz @10MHz, they possessed a fairly linear frequency characteristic and an acceptable system complexity. Based on this, it was decided that these were the implementations to be more thoroughly studied, as they posed to be, excellent candidates to be chosen to be developed in this dissertation. With that in mind they were dimensioned and subjected to corner simulations to determine their viability.

The chapter is organized as follows: at first, are given some extra details about the implementations operation and are presented the goals that conditioned the design. Next, are presented and discussed the frequency versus V_{ctr} characteristics obtained for each corner, and the correspondent power consumption for maximum and minimum frequencies. Then, are briefly discussed some results concerning performance under supply voltage and temperature variations and phase noise. To wrap it up are presented the conclusions.

4.1 Single Loop Implementation

The schematic of the 3 stage differential ring oscillator with latch control in a single-loop configuration, was already introduced in the last chapter on Fig. 3.10. Nevertheless, to provide an easier reading, the delay cell is presented once again on Fig. 4.2 and it is introduced a different view of the complete schematic on Fig. 4.1. To note, that the latch control, GND and VDD were suppressed on Fig. 4.1 in order to facilitate the comprehension and present the schematic in a more compact disposition.

As previously stated, this delay cell is pseudo differential and do not possess the tail transistor, reducing the $1/f$ noise [23]. It is composed by a XCP ($M_{1,2}$) that forms a regenerative latch, by

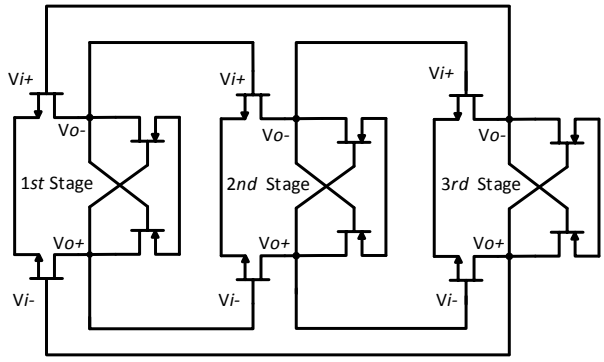


Figure 4.1: Alternative view of single loop configuration.

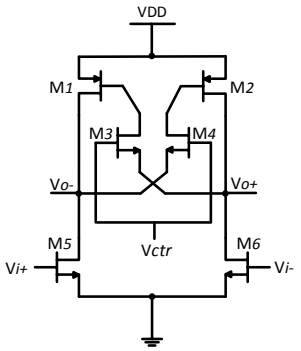


Figure 4.2: Differential cell with latch control.

the control pair $M_{3,4}$, and by the input pair $M_{5,6}$, that set the output state according to the input signal.

Lets assume an initial state where V_{i+} is low and V_{i-} is high for some time. The outputs V_{o-} and V_{o+} are high and low, respectively. When the input signals shift, M_5 "fights" to overcome M_1 and starts to discharge the load capacitance. At a certain point, M_2 starts to conduct and when V_{o+} reaches an high state, M_1 shuts down and the outputs state is shifted [27]. The speed of this operation can be controlled by the transistor pair $M_{3,4}$ that is able to regulate the maximum voltage present at the gates of the XCP transistors, which ultimately sets the maximum driving current. When V_{ctr} is low the driving current is higher, resulting in a lower propagation time. When V_{ctr} is high, the exact opposite happens.

The frequency versus V_{ctr} characteristic is very far from linear, in fact, it is very erratic, with only some interval(s) that can truly be utilized. In addition to that, small changes in the transistors $\frac{W}{L}$ ratio revealed major differences in the total frequency characteristic and it was nearly impossible to come to any conclusion on the effects that any change would result on.

Since one of the objectives was to develop an oscillator with the largest linear range as possible, it was created a Ocean script that would automatically simulate the schematic for different transistor $\frac{W}{L}$ ratios and sweep the control voltage for the interval between 0.5V and 1.2V, since it was the one that showed to accommodate the vast majority of linear frequency intervals during previous simulations. To note that the simulations were made assuming a temperature of 27°C, typical condition and an invariant supply voltage of 1.2V. Then a Matlab script was devised with the intention of processing the raw data and produce a set of possible linear intervals with $r^2 > 0.97$ (r^2 being the coefficient of determination), each one associated with a correspondent transistor sizing, which could be viable to be chosen.

On Fig. 4.3 are shown the frequency versus V_{ctr} characteristics obtained for the different corners: tt, fs, ss, ff, sf.

Looking at the frequency characteristic in the typical condition, it can be seen that it possesses a fairly good linearity and that has a frequency range that goes from 1.56 GHz to 4.34 GHz with control voltages of 1.2V and 0.8V, respectively.

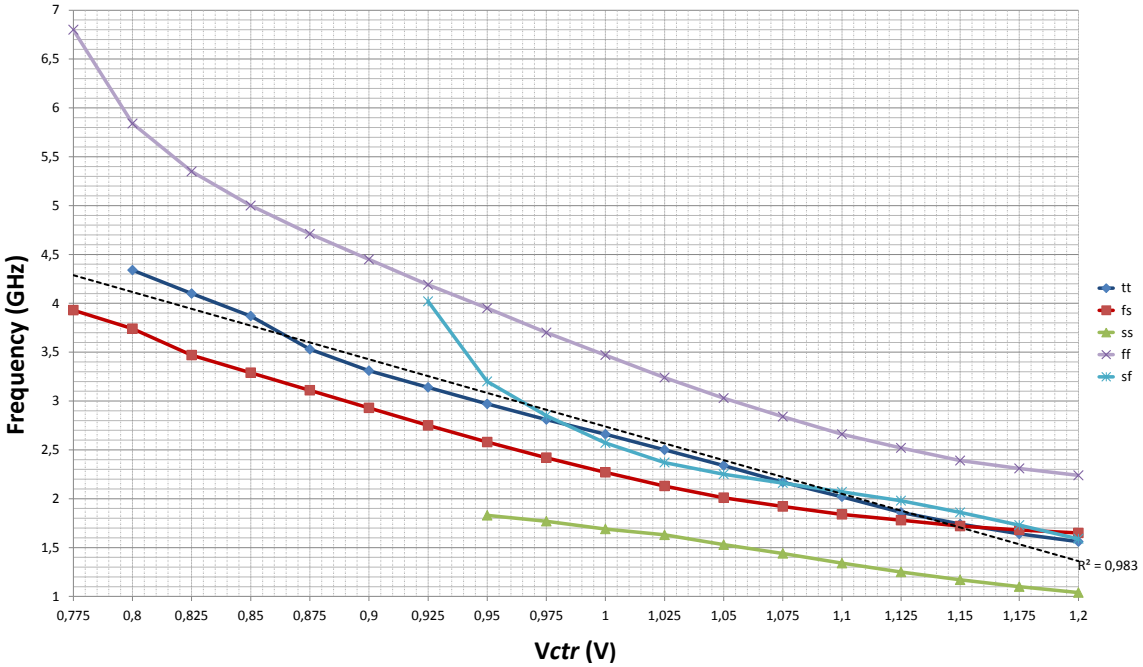


Figure 4.3: Frequency versus V_{ctr} characteristics for different corners.

The frequency characteristics have different ranges and the same control voltage produce distinct frequencies for the various corners. Although the control voltage was supposed to be in the interval mentioned before, it was extended in the case of the ff and fs corners in order to increase their range in the hope of maximizing the convergence between all corners. On the other hand, in the case of the ss and sf corners, the frequencies for control voltages smaller than 0.925 are unusable since they become erratic.

Since one of the primary objectives is that the oscillator possess a good frequency linearity and that the primary objective of this dissertation is that it must be digitally controlled, the frequency characteristics for the different corners were artificially linearised for a set of 8 values (to be controlled by 3 bits), Fig. 4.4. To note that the voltage control for the same point may be different for the several corners.

Table 4.1: Power consumption with corner.

Corner	$P_{\text{diss}Min}$ (mW)	$P_{\text{diss}Max}$ (mW)
tt	4.2	7.6
fs	4.3	7.1
ss	3.12	4.1
ff	5.3	9.87
sf	4.4	6.84

Unfortunately as it can be seen from Figs. 4.3 and 4.4, this implementation is not viable, since there are no common frequency values between the corners, not being possible to ensure, which independently of the corner, this oscillator could produce for sure a well defined range of frequencies. Also due to the bad performance in the ss and sf conditions, it would be very difficult

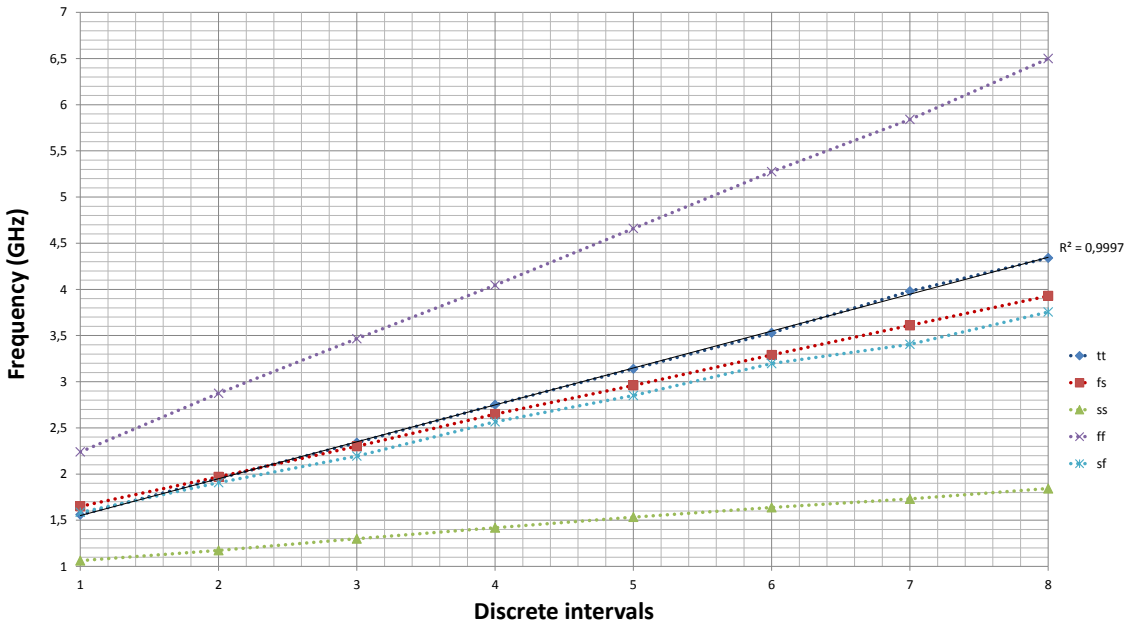


Figure 4.4: Linearised frequency characteristics.

to actually compensate a digital control network so it could effectively be able to control properly the oscillator in these corners.

It is now shown on Table 4.1 the maximum and minimum power consumptions for each corner.

On a curiosity note and to give some more information about the circuit performance under supply voltage and temperature variations, is now shown on Table 4.2 the frequency variation for temperature sweep from 0ºC to 100ºC and a $\pm$ 5% supply voltage variation. It is used the control voltage (0.95V) that produces the center frequency in the typical condition. As it can be seen, the frequency decreases with the increase in the temperature, due to the fact that the resistive effects increase with the temperature. Also, higher supply voltage leads to higher frequencies due to the increase in the driving current.

Table 4.2: Supply and temperature variation.

Temperature (ºC)	Supply Voltage (V)		
	1.14	1.2	1.26
0	2.73 G	3.34 G	4.04 G
20	2.56 G	3.11 G	3.76 G
40	2.41 G	2.91 G	3.50 G
60	2.27 G	2.75 G	3.28 G
80	2.15 G	2.59 G	3.07 G
100	2.02 G	2.45 G	2.87 G

The phase noise simulated for this implementation was -86.27 @1MHz offset and -112.7 @10MHz from a 3.1GHz center frequency in typical condition.

4.2 Dual Loop Implementation

The schematic of the differential cell with latch control in a double loop configuration was already introduced in the last chapter on Fig. 3.11, but for an easier reading and better comprehension it is now introduced once again in a different but complementary view. The latch control, *GND* and *VDD* were suppressed in order to facilitate the comprehension and for the schematic to be presented in a more compact disposition.

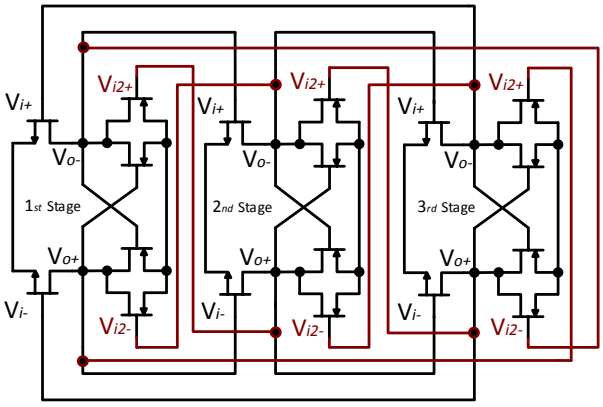


Figure 4.5: Alternative view of dual loop configuration.

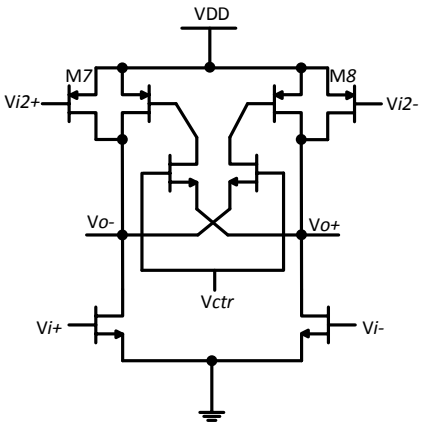


Figure 4.6: Differential cell with secondary inputs.

The operation is pretty much the same as in the single loop implementation. In fact, the only difference are the secondary inputs V_{i2+} and V_{i2-} ($M_{7,8}$), which receive the signal from the outputs of the delay cell two stages prior to the current one, pre-charging the outputs and achieving a faster rise time. On Fig. 4.5 it is possible to see the dual path. The black connections represent the normal signal path and the red ones the secondary path that feeds the extra pair of inputs. With this technique it is possible to increase not only the frequencies but also its range [23].

On Fig. 4.7 are shown the frequency characteristics obtained for the different corners. Looking at the frequency characteristic in the typical condition it can be seen that it possesses a fairly good linearity and that has a frequency range that goes from 7.9 GHz to 14.5 GHz with a voltage control of 1.2V and 0.65V respectively. Like in the single loop approach, the frequency characteristics have different ranges and the same control voltage produce distinct frequencies for the various corners, but the discrepancy between corners is lower.

The frequency characteristics were also linearised, but this time with 16 points (4 bits), since the range is approximately the double of the range of the single loop.

Unfortunately, as it can be seen from Figs. 4.7 and 4.8, there are no common frequency values between the corners, not being possible to ensure that this oscillator could produce for certain a defined range of frequencies.

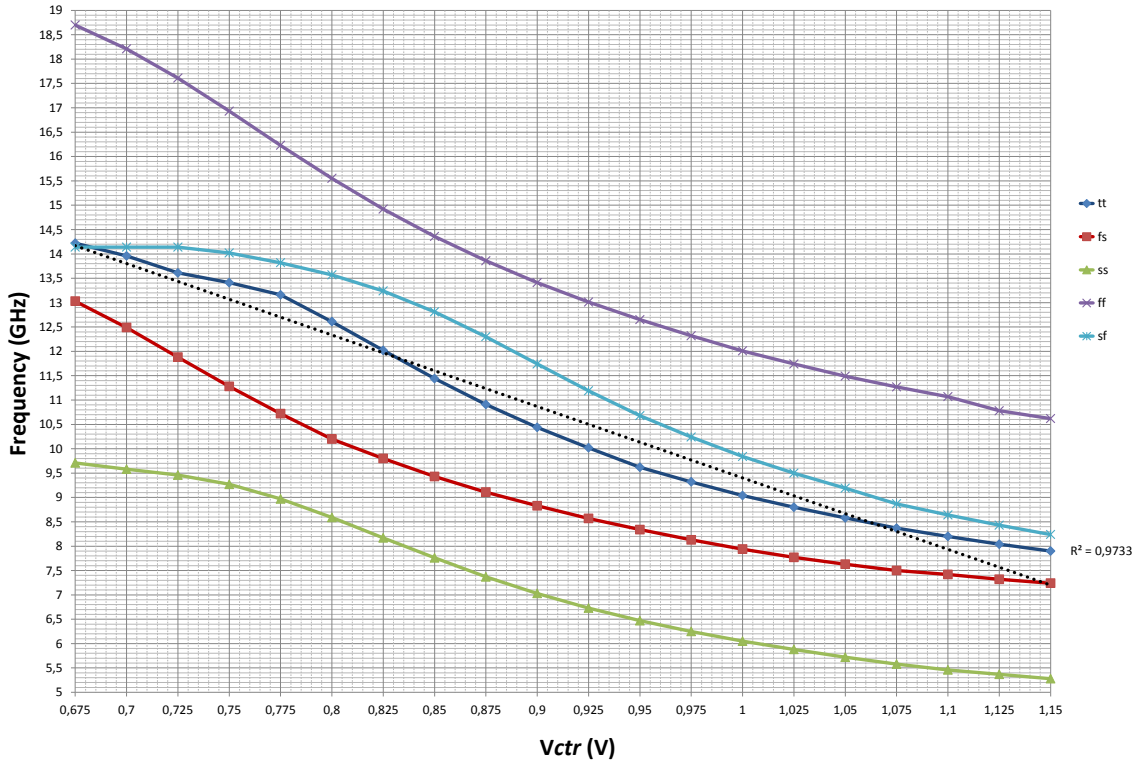


Figure 4.7: Frequency versus V_{ctr} for different corners.

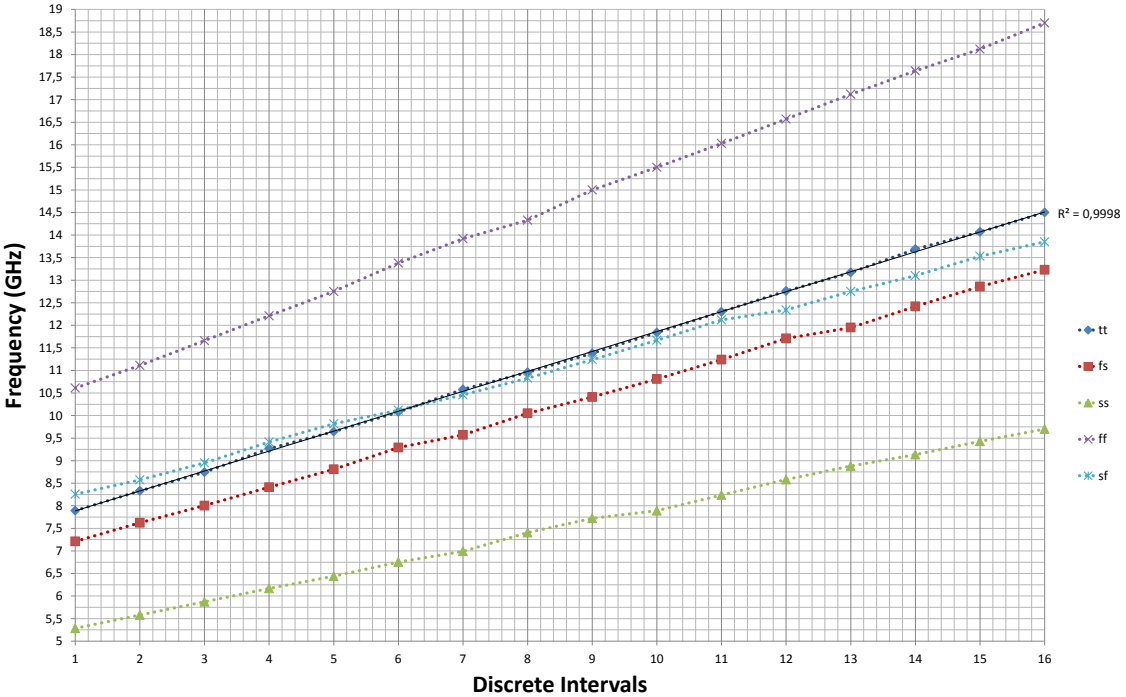


Figure 4.8: Linearised frequency characteristics.

Table 4.3: Power consumption with corner.

Corner	$P_{\text{diss}Min}$ (mW)	$P_{\text{diss}Max}$ (mW)
tt	9.36	12.24
fs	8.37	11.20
ss	6.57	8.75
ff	12.2	15.74
sf	9.93	12.16

As before, are presented on Table 4.3 the power consumption for the different corners. On a curiosity note and to give some more information about the circuit performance under supply voltage and temperature variations, it is now shown on Table 4.4 the frequency variation for temperature sweep from 0°C to 100°C and a $\pm$ 5% supply voltage variation. It is used the control voltage (0.875V) that produces the center frequency in the typical condition.

Table 4.4: supply and temperature variation.

Temperature (°C)	Supply Voltage (V)		
	1.14	1.2	1.26
0	9.94 G	11.48 G	13.08 G
20	9.62 G	11.10 G	12.61 G
40	9.35 G	10.76 G	12.25 G
60	9.1 G	10.45 G	11.87 G
80	8.87 G	10.22 G	11.49 G
100	8.71 G	9.88 G	11.20 G

The phase noise simulated for this implementation was -86.27 @1MHz offset and -112.7 @10MHz from a 11.1GHz center frequency in typical condition.

4.3 Chapter Conclusion

From the results achieved from the corner analysis is possible to conclude that neither the single or dual loop implementations designed as they were, are viable. The fact is that is impossible to ensure that there is a well defined frequency range common to all the corners that can be guaranteed. However, this dissertation proposes a new solution. The solution consists on merging the two implementations in one, making a hybrid pseudo differential delay cell that can accommodate the two loop modes and with that extend the range, improving the possibilities of frequency convergence between corners.

Chapter 5

Proposed DCO

This chapter comes in the follow up of the previous one and introduces the proposed DCO that is able to accommodate both single and dual loop modes and with it increase the frequency range and improve the results in the presence of process variation. The oscillator is divided in three major components: input stage, DCO core and output stage that are going to be individually presented and explained (Fig. 5.1).

Figure 5.1: DCO block diagram.

The chapter is organised as follows: at first, it is introduced the DCO core, being explained its operation, presented its performance under process variation and, to further characterize it, its performance under PVT variations. Next, are introduced the different blocks that constitute the input stage, and its overall performance under process and PVT variations. Then, the output stage is briefly explained and to end, are presented and discussed the overall results achieved for the complete DCO structure.

5.1 DCO Core

The DCO core is formed by a three stages DRO with newly proposed pseudo differential delay cells that are able to operate in both single and dual loop modes (Fig. 5.2). Since the purpose of such implementation was to join the frequency ranges of both modes, it was necessary to add another NMOS pair $M_{3,4}$ to , when in dual loop mode, increase the minimum frequency achieved, enhancing a better fit between the two ranges.

When D is 0, all of the transmission gates are disabled, and the "known state" (KS) transistors, force a signal at the gates of the secondary inputs $M_{1,2}$ and at the gates of the extra NMOS pair

$M_{3,4}$ that disables them. The cell now operates in the single loop mode. When D is 1, all of the transmission gates are enabled and the KS transistors are disabled, an so $M_{1,2}$ and $M_{3,4}$ are active. The cell now operates in the dual loop mode.

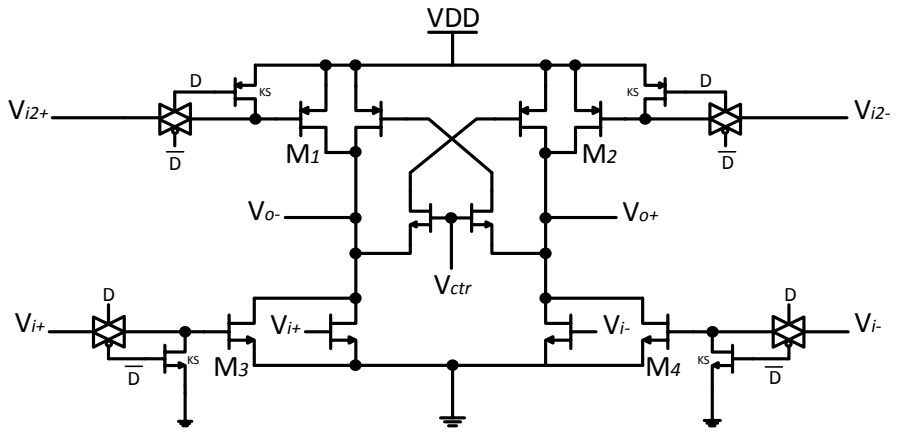


Figure 5.2: Proposed pseudo differential delay cell.

The design of the circuit was done having in mind the same premisses that were already introduced in the last chapter: achieve the maximum frequency range as possible with a fairly good linearity ($r^2 > 0.97$).

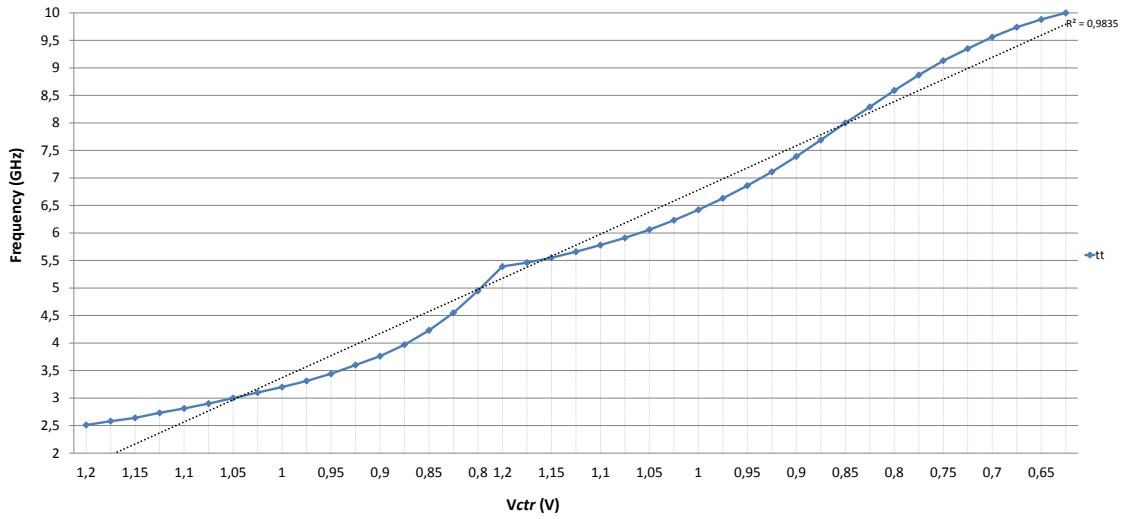


Figure 5.3: Frequency versus V_{ctr} characteristic.

On Fig. 5.3 can be seen the frequency versus V_{ctr} characteristic obtained in typical condition with a supply voltage of 1.2V and temperature of 27°C. As it can be seen, the X axis can be divided in two parts: the first, that goes from 1.2V to 0.8V and represents the control voltages for single loop mode, where the frequency goes from 2.51GHz to 4.95GHz; and the second, that goes from 1.2V to 0.625V and represents the control voltages for dual-loop mode operation, where

frequency goes from 5.35GHz to 10GHz. So, in these conditions, the oscillator is capable of producing frequencies from 2.51GHz to 10GHz, in a total of a 7.5GHz frequency range.

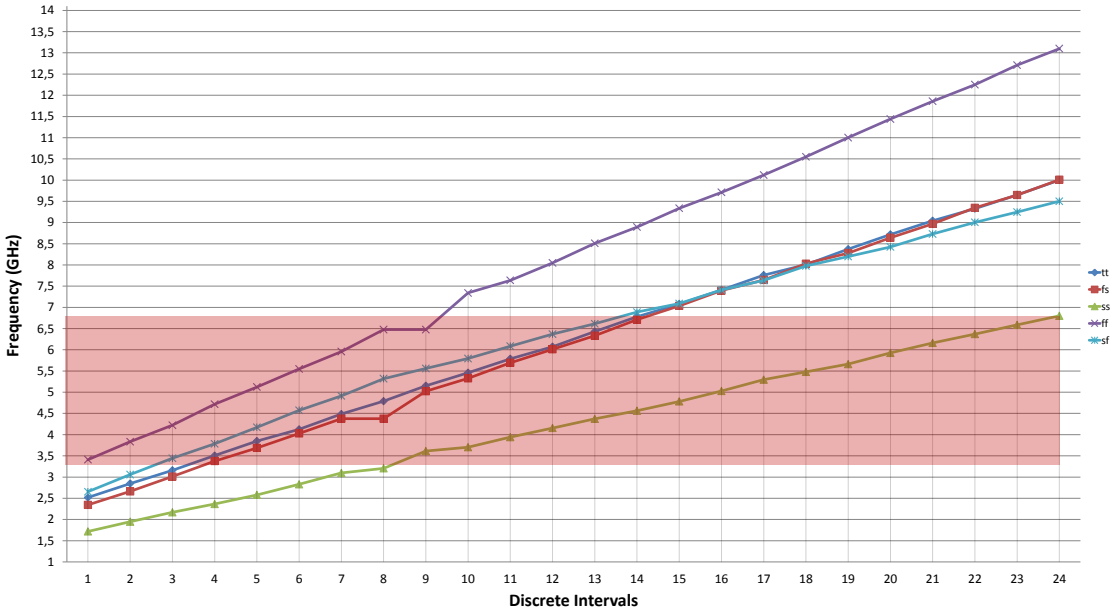


Figure 5.4: Linearised frequency characteristics for different corners.

As it was already possible to see from Figs. 4.3 and 4.7, the frequency versus V_{ctr} characteristics for the different process conditions do not possess the same V_{ctr} values for the first or the last points. This also happens here, since for some corners, it is necessary to manipulate the V_{ctr} intervals of the single and/or dual loop modes, to be possible to join the two individual characteristics. With this, it is impossible to present them here in a single graph, since they each possess their own X axis values. Either way, just like in Chapter 4, they are now presented linearised on Fig. 5.4, where the first 8 points represent frequencies generated in single loop, and the next 16 in dual loop. To remind once again that each point may represent a different V_{ctr} value for each corner.

As expected, the frequency characteristics for the ss and the ff corners are the ones that show higher deviation from the ideal (tt), since the transitions occur slower and faster respectively, due to the changes in the driving current I_d. By inspection, it is possible to see that the theory that led to this DCO implementation is correct. As it was anticipated, the range extension specifically in the ss and ff case, allows now to have a well defined frequency range common to all corners, that goes from 3.41GHz to 6.8GHz (area in red).

To find out the true extent of the proposed oscillator performance, were also made complete PVT variations, adding to the process corners already presented, $\pm 5\%$ variation in supply voltage and a temperature sweep from 0^{o}C to 100^{o}C.

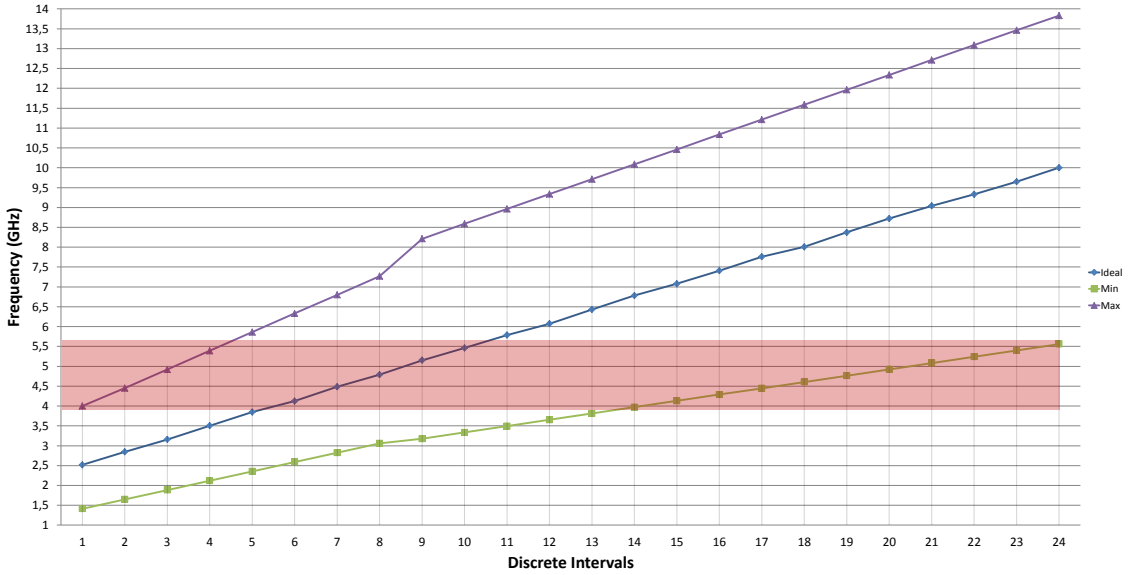


Figure 5.5: Linearised frequency characteristics for PVT extreme conditions.

On Fig. 5.5 are presented the ideal case (typical 1.2V 27°C), and the most extreme cases, where *MIN* represents ss at 100°C with 1.14V supply, and *MAX* represents ff at 0°C with 1.26V supply. These results are not surprising, since as already seen before on Fig. 5.4, the worst performances were obtained with ss and ff. To add to that, the resistance increases with the increase in temperature and the driving current decreases with lower supply voltages, which lowers and increases even more the frequencies obtained when in ss and ff, respectively. Even though, it continues to be possible to achieve a common frequency range, which as it can be seen on Fig. 5.5 goes from 4GHz to 5.56GHz (area in red).

5.2 Input Stage

The input stage main purpose is to generate and deliver to the DCO core, a control voltage $\Rightarrow V_{ctr}$ and a "loop decider" flag $\Rightarrow D$, according to the input code words Sm[0:2], Dm[0:3], F1[0:3] and F2[0:3]. As it can be seen on Fig. 5.6, this stage can be divided in three blocks: input buffer, binary to thermometer converter and voltage generator; each one with a different purpose. These blocks are now presented and thoroughly explained in the next few sections in the following order: voltage generator, input buffer and binary to thermometer converter.

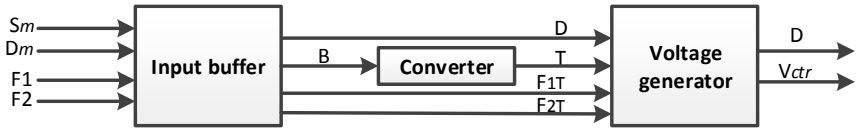


Figure 5.6: Input stage block diagram.

5.2.1 Voltage Generator

Since the oscillator core is controlled by V_{ctr}, and the purpose of this dissertation is to develop a DCO, it was needed to create a structure that would be able to generate an output voltage from a set of digital input signals. The proposed structure, that can be seen on Fig. 5.7, is based on strategies already discussed in Sections 3.2 and 3.4. Basically, the PMOS transistors behave like a current source and the NMOS network like a variable resistor. By enabling or disabling the NMOS transistors it is possible to regulate the total resistance and with this create the desired voltage.

Since the oscillator possesses two distinct operation modes, it was necessary to create not one, but two transistor networks to effectively produce the control voltage. Due to the fact that the control voltages for the linearised frequency characteristics are non linear, it was needed to control the transistor networks with a thermometer code word T where each bit has a different weight.

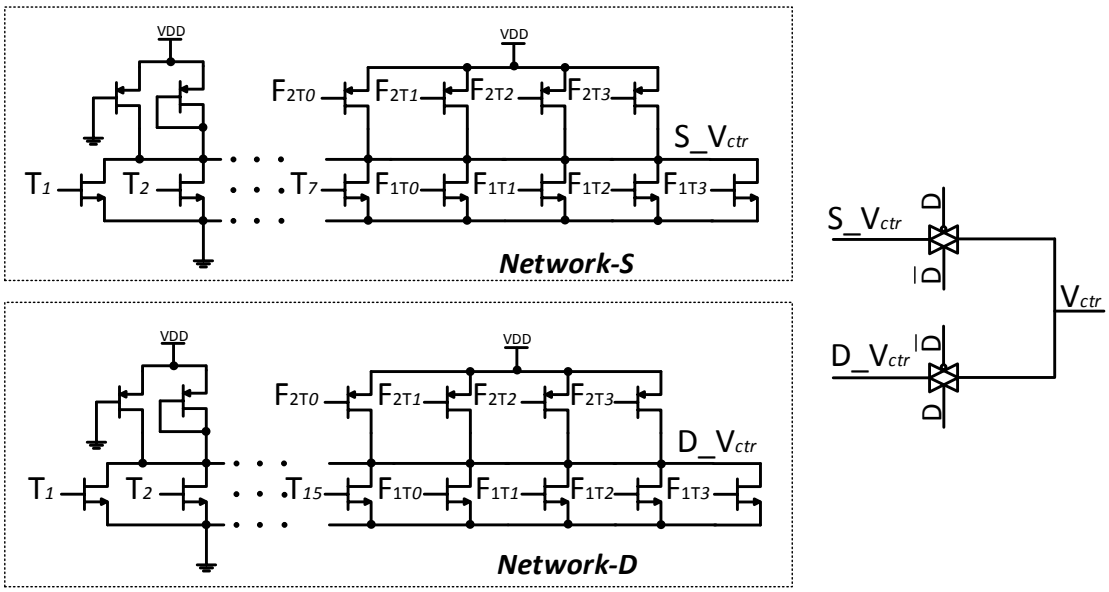


Figure 5.7: Voltage generator structure.

The Network-S is controlled by the first 7 bits of code word T ($T_1 ... T_7$) and the Network-D is controlled by the complete code word T ($T_1 ... T_{15}$). This decision of making the first 7 bits common for both networks was taken in order to reduce the total DCO area and the number of actual inputs, and is going to be better understood within the next section. To choose from which network V_{ctr} is generated, were added two transmission gates that are controlled by D. So when D is 0, V_{ctr} is generated by the Network-S and when D is 1 it is generated by Network-D.

In order to compensate for process variations, it was added on each network a PMOS transistor connected in diode. Also, it were added 4 extra PMOS controlled by F_{2T} and 4 extra NMOS controlled by F_{1T}, all thermometer weighted, so they could not only improve the performance of

the networks when under process variations, but also to help to better achieve the control voltages for the different frequency characteristics ($\neq$ process corner) that the oscillator core can create.

5.2.2 Input Buffer

The input buffer helps not only to isolate the inputs from the inner circuit, but also to index them to the supply voltage, something that is accomplished by the two stages inverter chain on each input, Fig. 5.8. As it was already explained, the transistor networks are controlled by the code words T and $F_{1,2T}$, that are thermometer code words. If each control signal were to be an input, it would not be very reasonable since the number of input pins to be created would be very high. With that in mind, was decided that the actual control would be done using binary words: Sm[0:2] $\Rightarrow$ single loop; Dm[0:3] $\Rightarrow$ dual loop.

If this was to be done as it is, it would be needed to create two binary to thermometer converters, one 3:7 and one 4:15, which would be not very elegant and would lead to an unnecessary increase in the occupied area. So, making the signals T_1 to T_7 common to both networks, as it was already said before, allows to use only one converter of 4:15. If D is 0, the 4 bit binary code word fed into the binary to thermometer converter (B) is going to be a code word formed by the concatenation of 0 in the MSB and the code word Sm. If D is 1, the 4 bit binary code word fed to the converter is Dm itself. To note, that D is 1 when any of the bits of Dm is one.

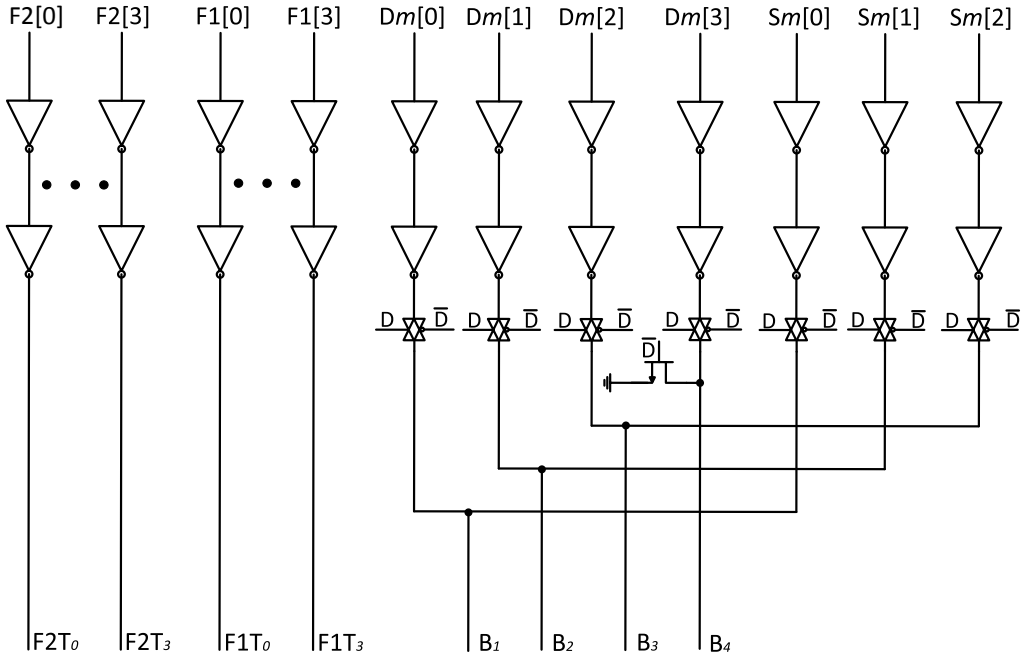


Figure 5.8: Input buffer.

5.2.3 Binary to Thermometer Converter

For further comprehension of the operation of the binary to thermometer converter [28] are now presented its schematic on Fig. 5.9, and the logical expressions with which is possible to calculate the output code word T[1:15] according to the input B[1:4].

$$T_1 = B_1 + B_2 + B_3 + B_4 \quad (5.1)$$

$$T_2 = B_2 + B_3 + B_4 \quad (5.2)$$

$$T_3 = B_3 + B_4 + (B_1 * B_2) \quad (5.3)$$

$$T_4 = B_3 + B_4 \quad (5.4)$$

$$T_5 = B_4 + B_3 * (B_1 + B_2) \quad (5.5)$$

$$T_6 = B_4 + (B_2 * B_3) \quad (5.6)$$

$$T_7 = B_4 + (B_1 * B_2 * B_3) \quad (5.7)$$

$$T_8 = B_4 \quad (5.8)$$

$$T_9 = B_4 * (B_1 + B_2 + B_3) \quad (5.9)$$

$$T_{10} = B_4 * (B_2 + B_3) \quad (5.10)$$

$$T_{11} = B_4 * (B_3 + (B_1 * B_2)) \quad (5.11)$$

$$T_{12} = B_4 * B_3 \quad (5.12)$$

$$T_{13} = B_4 * B_3 * (B_1 + B_2) \quad (5.13)$$

$$T_{14} = B_4 * B_3 * B_2 \quad (5.14)$$

$$T_{15} = B_4 * B_3 * B_2 * B_1 \quad (5.15)$$

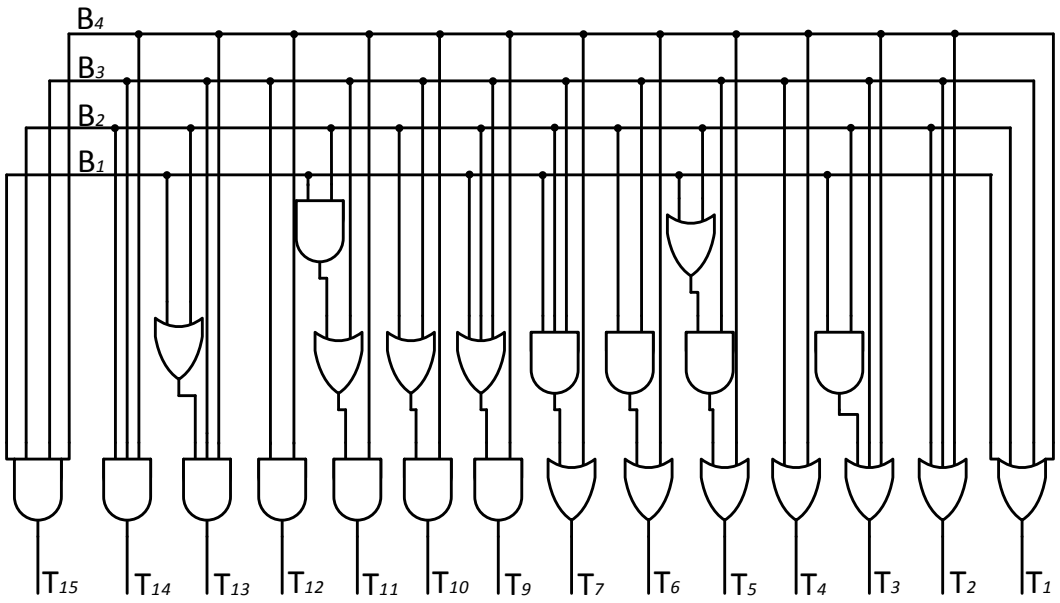


Figure 5.9: Binary to Thermometer converter presented in [28].

5.2.4 Input Stage Overall Performance

Like the DCO core, the input stage was also submitted to process variation simulations in order to evaluate its performance. Due to the fact that there are two different networks, the results were divided in two graphics, where the one on Fig. 5.10 represents the results obtained for the binary code word S*m*[0:2], and the 5.12 the results for D*m*[0:3].

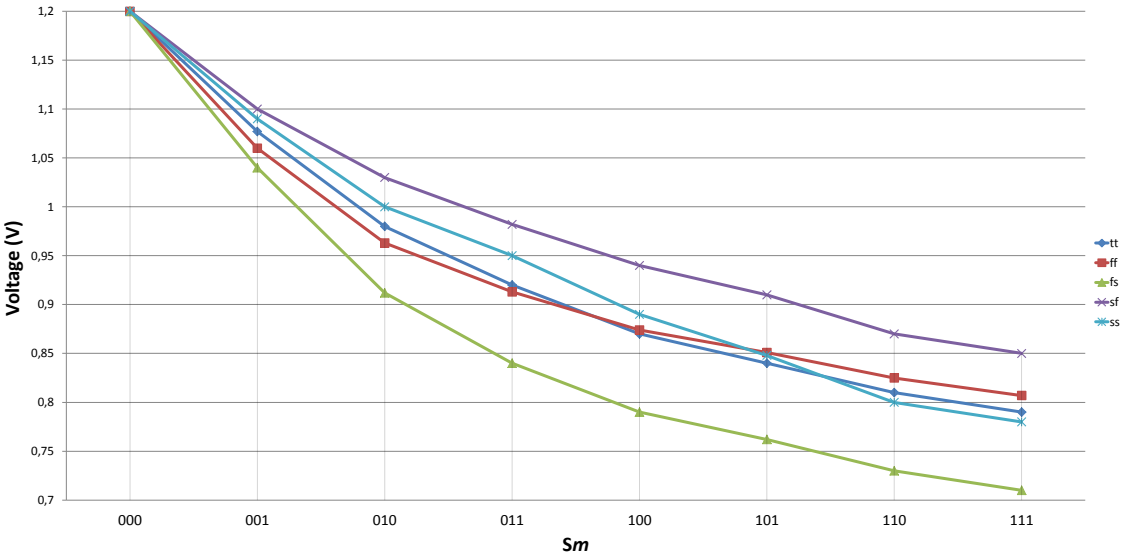


Figure 5.10: V_{ctr} versus Sm for different corners.

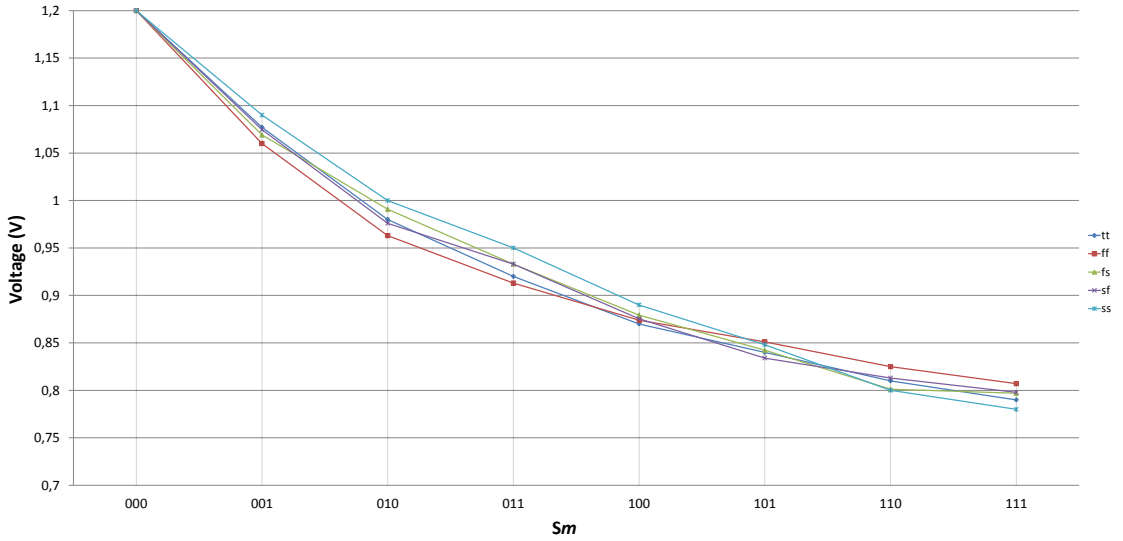


Figure 5.11: V_{ctr} versus Sm compensated for different corners.

The highest deviations from the ideal values happen in the sf and fs corners. In the sf corner, the NMOS network possesses an higher resistance and the driving current is higher, resulting in V_{ctr} values higher than desired. In the fs corner, the exact same opposite happens. The NMOS network possesses a lower resistance and the driving current is lower, resulting in V_{ctr} values lower than desired. On the other corners, the control voltage values are very similar to the ideal.

As it was already said before, the function of the extra set o PMOS and NMOS transistors, serves not only to help to produce the control voltages needed to obtain the possible frequency characteristics that the DCO core is capable of achieving, but also to help to compensate the input stage own process deviation and maintain the characteristic as close to the ideal as possible. On Figs. 5.11 and 5.13, are represented the compensated V_{ctr} versus code word characteristics, for the

S*m* and D*m* code words, respectively.

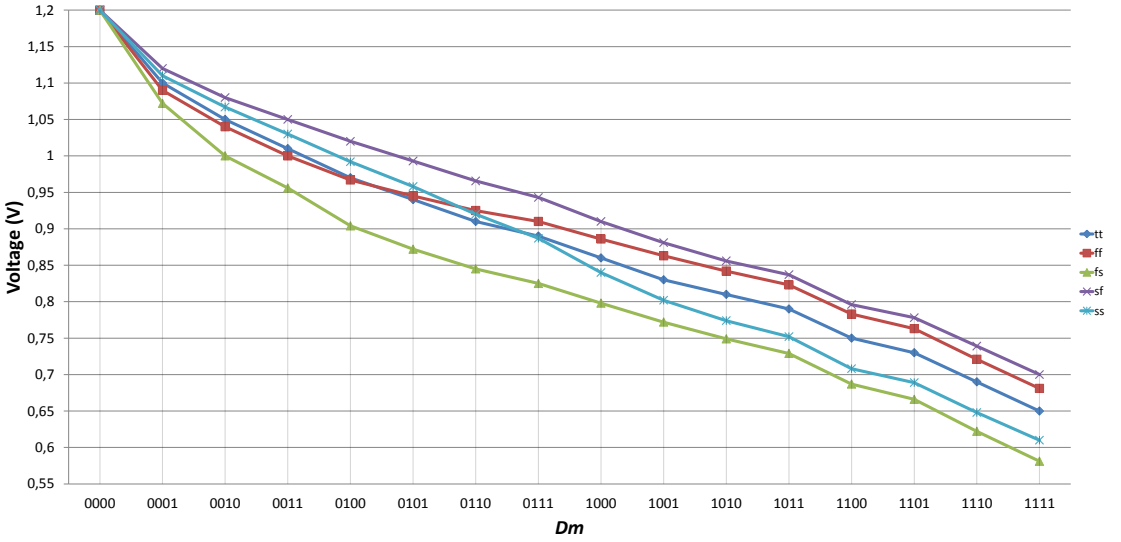


Figure 5.12: V_{ctr} versus D*m* for different corners.

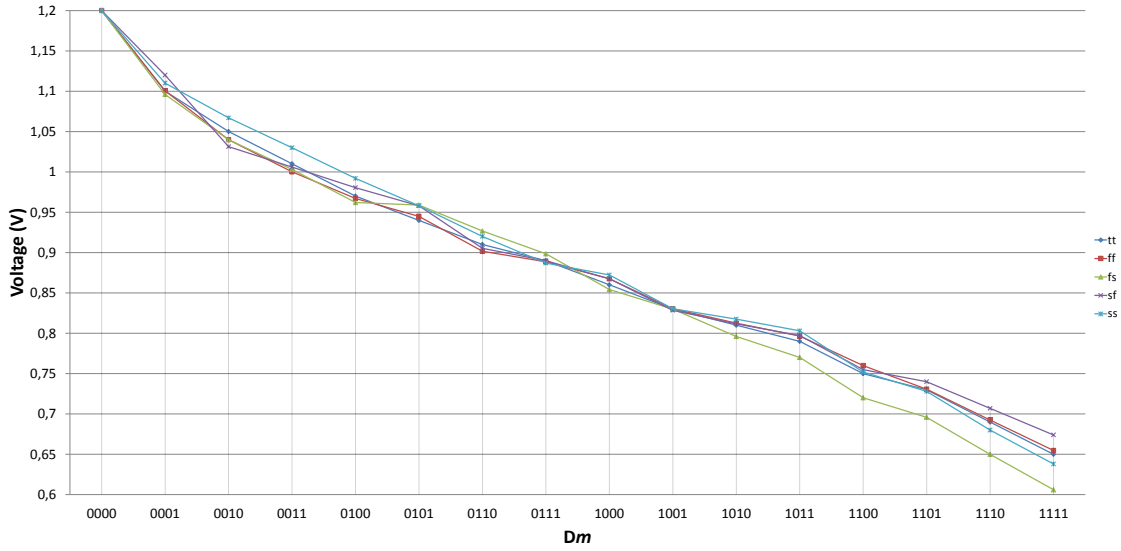


Figure 5.13: V_{ctr} versus D*m* compensated for different corners.

5.3 Output Stage

Since there were no specifications relatively to the output signal type, differential or single ended, it was decided to use a differential to single ended converter to reduce the outputs from 2 to 1, and with that reduce the number of output buffers, reducing the power consumption and the occupied area. With this, the output stage is then formed by a differential to single ended converter and an output buffer.

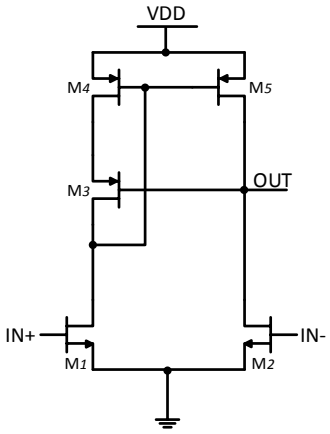


Figure 5.14: Differential to single ended converter.

Regarding the differential to single ended converter, lets assume that OUT is initially at low level and that IN+ is low and IN- is high level. The input signals start to shift and the transistor M_1 starts to conduct. At a certain point, the value at the gates of the mirror pair gets close to zero and they start to conduct. Since M_2 is shut, the output begins to rise to high level. When this happens, and to prevent the formation of a direct path between VDD to GND, the transistor M_3 shuts down.The process repeats it self, converting a differential signal into a single ended one.

The output of the converter feeds the input of a 6 stages tapered buffer that drives a load of 100fF, Fig. 5.15. With this, the inner circuit is isolated from load variations if the total load does not exceed 100fF. Each inverter is slightly bigger than the previous, keeping the first inverter to a minimal size and affecting the less possible the frequency generated by the oscillator core.

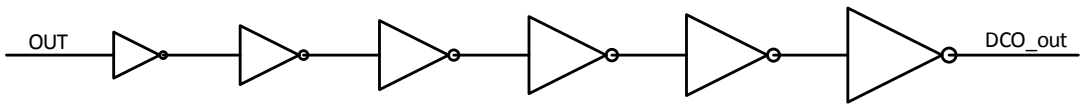


Figure 5.15: Output buffer.

5.4 Overall Performance

After presenting the individual performance of the DCO core and of the input stage, it is now time to present the overall results obtained for the complete DCO.

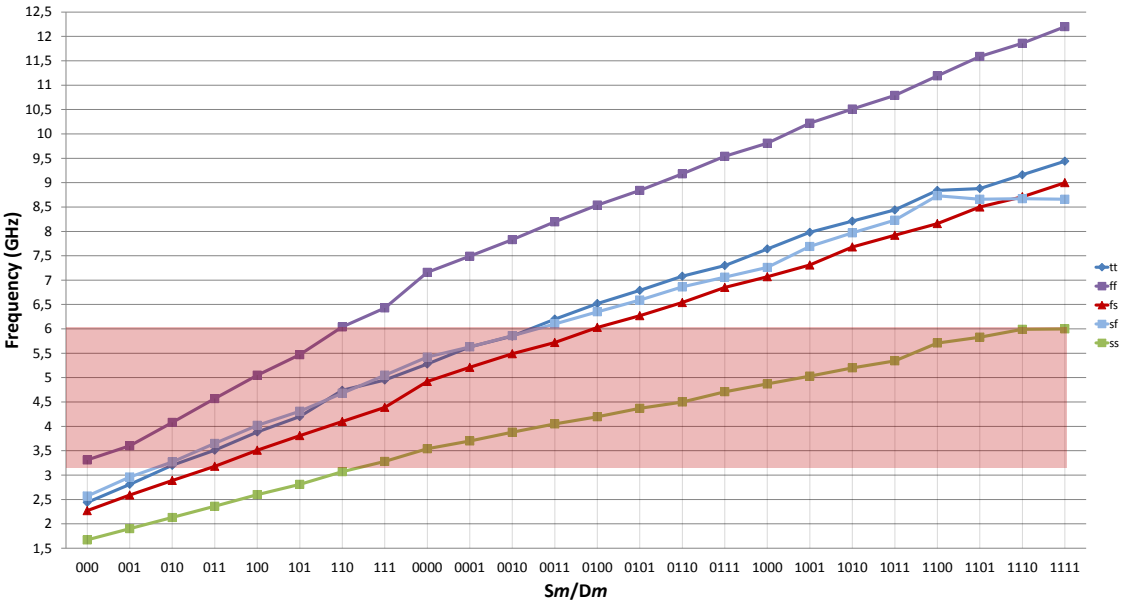


Figure 5.16: DCO frequency versus code word for different corners.

On Fig. 5.16 it is presented the frequency versus code word characteristics for all the process corners. All of the characteristics except for the tt were linearised using the extra thermometer code word F_{1T} and F_{2T}.

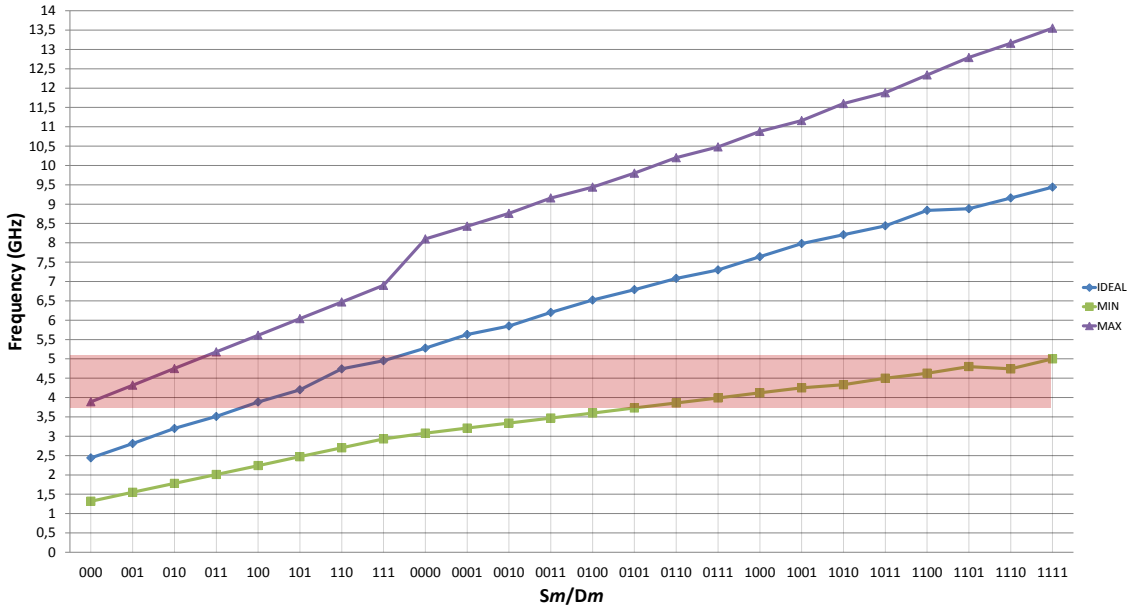


Figure 5.17: DCO linearised frequency characteristics for PVT extreme conditions.

As it is possible to see, the ranges suffered a little loss due to the introduction of the output stage, fact that is easily explained due to the load increase at the output of the DCO core. Nevertheless, in typical condition it is yet possible to achieve frequencies that goes from 2.44GHz to

9.44GHz, which gives a total frequency range of 7GHz. The frequency range common to all of the corners also decreased, but it is yet possible to achieve common frequencies for 3.13GHz to 6GHz, in a total of 2.87GHz of common range.

Table 5.1: DCO power consumption for different corners.

Corner	P_{diss} *Total* (mW)		P_{diss} *Input stage* (mW)		P_{diss} *DCO core* (mW)		P_{diss} *Output stage* (mW)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tt	10.64	31.64	$\simeq 0$	2.4	7.14	16.54	3.5	12.7
ff	13.53	39.73	$\simeq 0$	2.3	9.13	21.43	4.4	16
fs	9.69	29.48	$\simeq 0$	2.35	6.4	15.13	3.29	12
sf	11.21	30.72	$\simeq 0$	2.12	7.57	16.4	3.64	12.2
ss	7.59	22.28	$\simeq 0$	2.03	5.15	11.45	2.44	8.8
MIN	5.84	18.03	$\simeq 0$	2.5	3.94	8.83	1.9	6.7
MAX	17.5	47.2	0.5	2.13	11.24	26.07	5.76	19

On Fig. 5.17 are presented the results when DCO operates in the most extreme cases of PVT variation, where *MIN* represents ss at 100ºC with 1.14V supply, and *MAX* represents ff at 0ºC with 1.26V supply. For the reasons already explained, there is a little decrease in the common frequency range, yet it is still possible to achieve common frequencies from 3.89GHz to 5GHz.

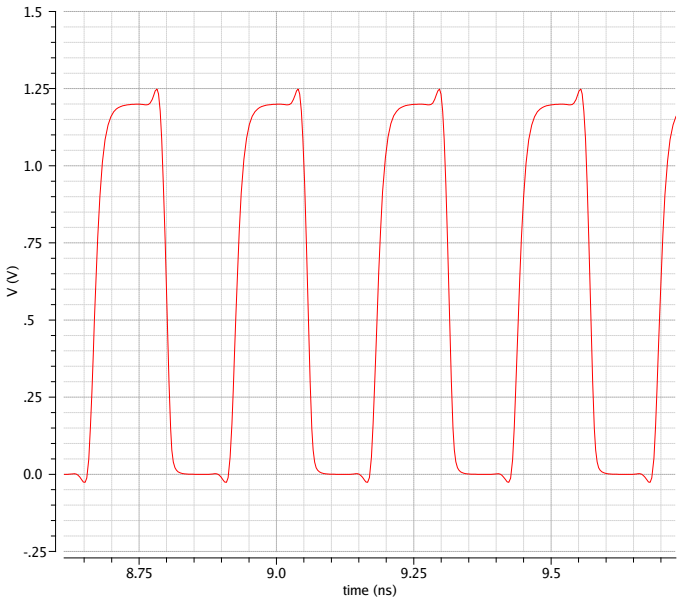


Figure 5.18: Output wave for control code 100.

On Table 5.1 are presented the values for the maximum and minimum power consumption that are achieve for the highest and lowest frequencies that are possible to be achieved in each corner. To note that the power dissipation of the output stage poses a big parcel in the total power consumption.

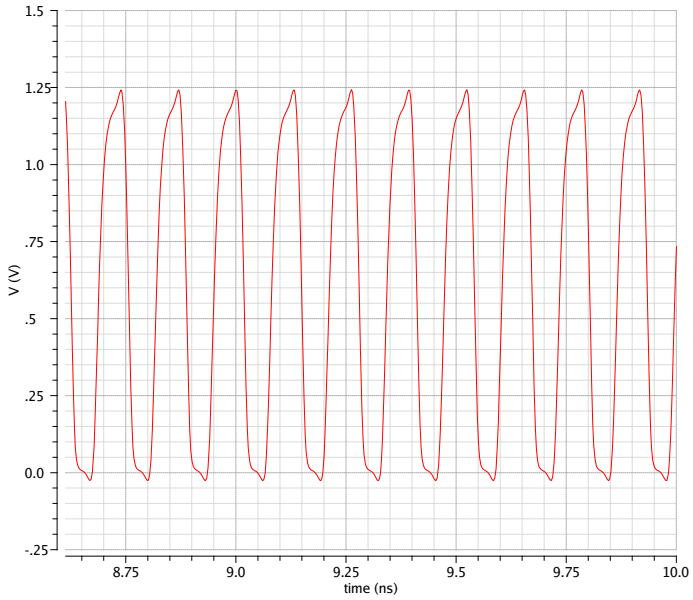


Figure 5.19: Output wave for control code 1000.

On Figs. 5.18 and 5.19 it is possible to see the output wave forms for control codes 100 and 1000 in the typical condition. They both possess a voltage swing rail-to-rail, and duty cycles in the order of 51%.

The simulated phase noise is of -85.77dBc/Hz @ 1MHz and of -109.2dBc/Hz @ 10MHz from 3.8GHz frequency (control code 100), and of -83.9dBc/Hz @ 1MHz and of -110.1dBc/Hz @ 10 MHz from 7.65GHz frequency (control code 1000).

Chapter 6

Conclusion

This dissertation was focused in the development of a DCO, the called heart of the AD-PLL, and the block whose performance more intimately affects the AD-PLL performance.

The initial objectives were to develop a DCO with a large linear frequency range that would be capable of producing a well defined frequency range even under PVT variations.

To begin with, were studied and implemented several oscillators designs that were researched during the quest to get more knowledge on the topic of DCOs. This allowed a better understanding of the presented frequency control techniques, as well as the acquisition of a very much needed experience on the simulation environment, that at first revealed itself to be very difficult to acquire, leading to delays in the work plan.

After this "small" study, it was done a more serious one on the implementations that seemed to be more suitable to eventually produce the results that were able to meet the primary objectives. Unfortunately they were not, since it was not possible to generate a well defined range of frequencies under PVT variations. However, the results achieved allowed to formulate the hypothesis that led to the development of the proposed DCO. The truth is that its performance met all the objectives, being possible to produce a frequency range from 3.13GHz to 6GHz under process variation, and a frequency range from 3.89GHz to 5GHz, when in the presence of the extreme PVT conditions.

The power consumption goes from 17.5mW to 18.03mW in the frequency interval of 3.89GHz to 5Ghz, but ultimately it may vary from 5.84mW to 47.2mW if the lowest and highest possibly achieved frequencies are taken into account.

The duty cycle is very close to 50%. and the voltage swing rail-to-rail.

6.1 Future Work

There are always new ways to improve past works. In this work particularly, there may be different strategies of digital to V_{ctr} conversion that may prove themselves more accurate. Also, as it could be seen, a great parcel of the total power consumption was associated with the buffer. So the study of different buffer implementations is recommended.

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