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DC/DC Converter with Transparent Electronics for Application on Photovoltaic Panels

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Sumário

A eletrónica transparente é uma tecnologia emergente que pode proporcionar sistemas de baixo custo dada a possibilidade de fabricação de dispositivos a baixa temperatura. A sua aplicação pode ser útil em vários domínios como indumentária eletrónica e sensores de monitorização de saúde. Com a implementação de conversores DC/DC em eletrónica transparente, as aplicações poderiam extender-se para dispositivos com fonte de bateria ou painéis fotovoltáicos.

A tecnologia transparente é baseada em transístores de filme fino (TFT) com semicondutores a-IGZO, material que emergiu nos últimos anos. Os transístores podem ser utilizados para a criação do Conversor DC/DC desejado, o qual pode ser depositado do vidro dos painéis, reduzindo os custos de montagem e conceção de todo o sistema.

Esta dissertação tem como principal objetivo o projeto e desenvolvimento para construção de uma topologia de conversor DC/DC com eletrónica transparente para aplicação em painéis fotovoltáicos. Inclui o estudo de elementos passivos, como bobinas e condensadores, e a sua possibilidade de utilização. A construção e melhoria do conversor DC/DC inclui o desenvolvimento de um regulador para estabilização da tensão de saída.

O trabalho tem a colaboração do grupo CENIMAT da Universidade Nova de Lisboa. Nesse local será construído o conversor DC/DC e os circuitos desenvolvidos nesta dissertação.

Abstract

Transparent electronics is a forthcoming technology, which allows for low-cost systems with devices fabricated at low temperatures. Its application may be useful in various domains, such as wearable electronics and sensors for health monitoring. Designing DC/DC converters with transparent technology could extend its application to battery operated devices or photovoltaic panels.

Transparent technology, in this work, is based on thin-film transistors (TFT) with a-IGZO semiconductors, material that has emerged in recent years. Their effectiveness for designing DC/DC converters will be assessed. Such converter could eventually be deposited on the glass casing of photovoltaic panels, reducing installation and designing costs of the whole system.

This dissertation has in its main objective the development, design and fabrication of a DC/DC converter topology with transparent electronics, for application in photovoltaic panels. It includes the study of some passive elements, such as inductors and capacitors, and their effectiveness for a possible use. The improvement of the DC/DC converter includes the design of a regulator to stabilize the output signal.

The work is developed in collaboration with the CENIMAT group at UNL, where the developed circuits and DC/DC converter will be fabricated.

Acknowledgments

I would like to thank my family for always support me during this master, to believe in my capability and effort to achieve this important objective in my life.

I thank my friends, Bruno Silva e Henrique Martins, for the support in all the challenges that this master created. All the study meetings before exams were very important to a successful accomplishment of the course.

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Romano Jorge de Sousa Torres

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Abreviaturas e Símbolos

a-IGZO	amorphous Indium Gallium Zinc Oxide
DC	Direct current
FEUP	Faculdade de Engenharia da Universidade do Porto
ITO	Indium Tin Oxide
LCD	Liquid-Crystal Display
LPF	Low-Pass Filter
MPDV	Multiphase voltage doubler
PWM	Pulse-Width Modulation
PCB	Printed Circuit Board
TFT	Thin-Film Transistor
TPVD	Two-phase voltage doubler
UNL	Universidade Nova de Lisboa
UV	Ultra-violet

Chapter 1

Introduction

1.1 The World of TFTs and Motivation

The industry of integrated circuits design is always searching new ways to improve the performance of the electronic devices. During the last century, electronic technology has emerged in such scale, appearing more and more devices that change the global life style and push the humanity towards new targets previously unreachable.

Thin Film Transistors are electronic devices that have been studied in recent years due to their low-cost fabrication, which can decrease the cost of application in various domains such as military, radio-frequency, sensors in health monitoring, wearable electronics and much more. The most common application of TFT is the liquid-crystal display technology (LCD). In this situation, TFT can reduce the crosstalk between the pixels, providing a better control of each pixel and improving the image quality in displays.

TFT's are field effect type, and are structurally built from deposition of thin-films on a non-conductive substrate, like glass or ceramic, which have good electrical isolation properties and reduce the parasitic capacitance comparing with monolithic circuits. A semiconductor layer and a dielectric layer are deposited between two metal contacts that represent the source and drain. Besides the improvement of this technology, transparent conducting oxides have been tested to use in TFT's, in order to create full transparent electronic devices. One of the most used material in recent years is the amorphous Indium Gallium Zinc Oxide (a-IGZO), which various reports suggest a better performance when compared to Zinc Oxide (ZnO).

The main focus of this thesis is the study and implementation of DC/DC converters with transparent electronics. The possibility of fabrication processes at low temperature allows the development of TFT on flexible substrates at an evermore low cost. The transparent DC/DC converters could be used on photovoltaic panels by deposition on glass substrate, possibly raising its cost effectiveness.

Today, there are many studies concerning climate changes that result from the burning of non-renewable energy sources, causing emissions of carbon dioxide to atmosphere and developing greenhouse effect. Due to an increasing world population, the energy demand rises, depleting

petroleum and other non-renewable energy sources. The research on alternative and renewable energy sources is then of outmost importance. Photovoltaic energy is one possibility.

Photovoltaic panels often use DC/DC Converters. They are mainly electronic circuits that change the voltage value from input to output, working with direct currents (DC). Their application extend to battery supplied devices, like mobile phones, laptops, typically to increase the voltage provided. Converters are used also on photovoltaic panels. In this case, the converter produces a regulated output voltage from energy temporarily saved, releasing it on a different voltage value, with increasing efficiency.

Now-a-days, the inclusion of photovoltaic panels on daily life is possible, by either using the roofs of buildings or large fields, but the creation of transparent devices can be considered as a possibility of embodying the electronics with panels. Such approach could effectively down-size the overall cost of the electronics (low-temperature fabrication) and of assembly (deposition of electronic system on the glass casing). This is the main motivation behind the present proposal for dissertation.

1.2 Generic Proposed Solution

The most common DC/DC Converters use inductors as a passive element to store energy, to increase or decrease the voltage level at the output. Due to the fact that transparent materials have lower conductance than metals, there is a large parasitic resistance associated to them. The creation of a high performance inductor, where the coil needed for magnetic field forces it to have a long path, is expected to be a challenging task. The longer the path is, lower is the quality factor of the inductor. To overcome this problem, other different electronic topologies can be used to increase an input voltage with DC current, such as charge pumps and voltage doublers. These devices have the same purpose as the standard ones, but due to their non-inductive behaviour, they can have more undesirable drawbacks. One of them is the increased voltage ripple, that reduce the precision of voltage level at the output.

Another limitation is the lack of p-type devices, due to the undesirable levels of carrier concentration, mobility and band-gap that this type of transparent materials have. Only n-type transistors can be used in transparent circuits designed, that forces to a different implementation of the circuits.

The lack of investigation in this field is another limitation. The most common studies of transparent electronics are focused on TFT parameters, which the first report is from Nomura et al. in 2004 [16]. Therefore, new electronic topologies will be needed for the design of a DC/DC converter with transparent electronics.

The proposal described in this report, for a positive DC/DC converter topology to be implemented with transparent electronics, uses switched-capacitor concepts to circumvent the need for inductive elements. However, there are other issues that need to be taking into account. In chapter 4 is presented the proposal of DC/DC converter and a method to regulate the output voltage, with the study of the respective parameters and behaviours that results from that design.

1.3 Structure of the Document

Besides the introduction, this report has 4 more chapters.

Chapter 2 discusses the fundamentals and theory behind the construction of DC/DC converters with transparent electronics and their regulation.

Chapter 3 presents the state of the art, where various studies, closely related to the goal of this dissertation, are exposed.

Chapter 4 presents the schematic and the layout of the final proposal for the transparent DC/DC converter and the regulation method, with a deep study of the results obtained with the circuit designed.

Chapter 5 presents the conclusions and the future work that can be made regarding DC/DC converters with this technology.

Chapter 2

Background

2.1 Transparent electronic devices

Standard DC/DC converters use various components such as resistors, capacitors, diodes and inductors. Regarding the goal of designing such device with transparent electronics, a study about transparency and its effect on the behaviour of passive devices is very important, to analyse how worth is the usage of each component.

To create transparent devices, different materials should be combined to perform the same functions of non-transparent devices. The efficiency of new devices created should be, as possible, equal or better to the existing ones. However, the characteristics of transparent electronic materials comparing with the others, like smaller conductivity, decrease their efficiency.

There have been many studies to create high performance devices. They focus on the layout of materials, and the results are sometimes very different from what could be expected with non-transparency.

2.1.1 Resistors

A good performance resistor should fulfil the characteristic defined by Ohm's law; it should have a linear behaviour according to this law. Parasitic capacitance is undesirable, therefore those should be fabricated on insulating substrates.

Taking advantage of the smaller conductivity of transparent materials, resistors are created with a long path between two contacts. The layout can be seen in figures 2.1 and 2.2.

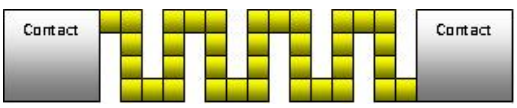


Figure 2.1: Transparent resistor from a planar view [1]

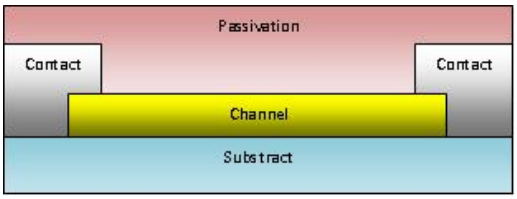


Figure 2.2: Transparent resistor from cross-sectional view [1]

The passivation layer is created to protect the resistor physically and chemically. The resistance value depends of the parameters from the equation:

$$R = \frac{\rho L}{Wt} \tag{2.1}$$

where ρ is the resistivity of the material, L is the path length, W is the path width and t is the path thickness. The resistance value is proportional to the resistivity of material and the path length. It is inversely proportional to the width and the thickness. To reduce the area of the resistor and obtain the maximum resistance, a rectangular zigzag shape is normally adopted along the resistor length 2.1.

2.1.2 Capacitors

Capacitors should have a linear current-voltage derivative characteristic. They are created to store energy in an electric field form. A transparent capacitor can be achieved with a transparent electric insulator between two contacts. The layout can be seen in figures 2.3 and 2.4.

Figure 2.3: Transparent capacitor from plan view [1]

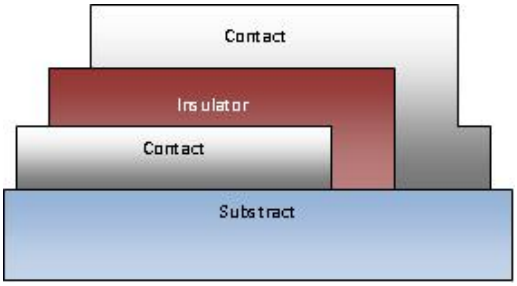


Figure 2.4: Transparent capacitor from cross-sectional view [1]

The capacitance value depends of the parameters from the equation:

$$C = \frac{\varepsilon LW}{d} \tag{2.2}$$

where ε is the insulator dielectric constant, L is the length and W is the width of the overlapping area, and d is the dielectric thickness. The capacitance is proportional to the insulator dielectric constant and the plates area. It is inversely proportional to the insulator thickness.

2.1.3 Inductors

Inductors store energy in a magnetic field, but due to poor conductance and consequently high parasitic resistance of transparent materials, it is difficult to create these devices with linear voltage-current derivative as expected.

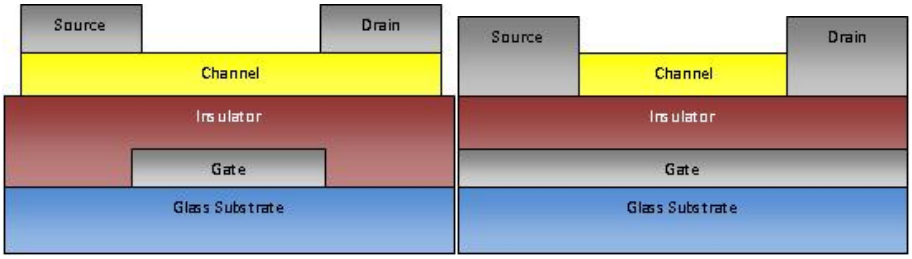
In fact, the resistance related to the transparent material is so high, that the large number of turns needed for inductor increases the length of material and consequently the parasitic resistance [1]. With high parasitic resistance, the quality factor of inductor will be low. Therefore, other ways to create DC/DC converters need to be studied. One possible solution can be voltage multipliers, referred in the next section.

2.1.4 Thin-film transistors (TFT)

TFT's use the principle of insulated-gate field-effect, which work with similar principals of the MOSFET transitor. The differences between the two devices are the properties of the materials, their fabrication and the smaller thickness of the semiconductor. In fact, the TFT's are fabricated on the top of an insulating substrate, as opposed to MOSFET technology, that uses the semiconductor as substrate. This difference reduces the parasitic capacitance associated to diffusions that occur in monolithic circuits.

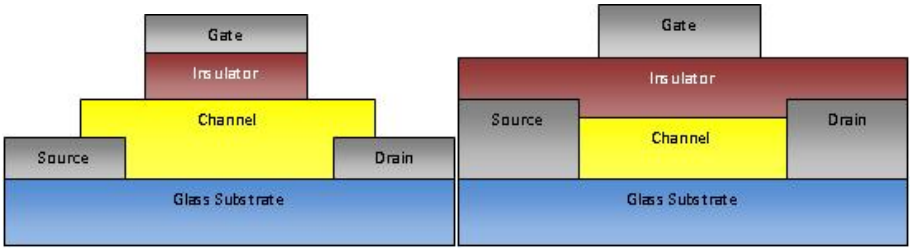
The basic function of these devices is to control the current between drain and source with an input voltage at the gate (to the source). Due to their characteristics, transistors can be used as a switch or even as a diode. The ability to set the device in multiple operation modes makes them the core of electronics. Different structures of the device are possible and various technological parameters can change their characteristics. There are four different structures of TFTs studied, the staggered bottom-gate, staggered top-gate, co-planar bottom-gate and co-planar top-gate structures. The different layouts can be observed in figures 2.5 and 2.6.

Classification differs with the relative positions of the channel (semiconductor), insulator, gate, source and drain. If the contacts are at the same level as the channel, it is a co-planar structure, otherwise it is staggered. The designation of top-gate and bottom-gate differs on the gate position as the name suggests.



(a) Staggered bottom-gate structure (b) Co-planar bottom-gate structure

Figure 2.5: Bottom-gate TFT Device Structures



(a) Staggered top-gate structure (b) Co-planar top-gate structure

Figure 2.6: Top-gate TFT Device Structures

2.1.4.1 Materials used for transparent TFT

Research have been made during the years for the creation of transparent TFTs. Results have been more successful with n-type semiconductors. There are no solutions yet about high performance p-type transistors, because the mobility, carrier concentrations, and band gaps of this type of semiconductors are not reliable to realize [1]. Therefore, the materials presented for channel layer are typically solely n-type, and transparent circuits have to take into account this limitation.

The first transparent thin-film transistors created were reported in 2003 [17] [18] [19]. They used a ZnO channel layer in a staggered bottom-gate structure. Improvements have been made, and K. Nomura [16] in 2004 presented a transparent TFT using amorphous Indium-Gallium-Zinc Oxide (a-IGZO) with mobility exceeding $10 cm^2/V.s$.

Gate dielectrics are very important because it impacts on the number of interface states, should show high dielectric constant and low leakage current. Al_2O_3, Y_2O_3 and Sc_2O_3 are materials that present good performance as dielectric [1]. Drain-source contacts should have low resistance. P.Barquinha et al. [20] suggests the usage of molybdenum (Mo) or Ti/Au contacts due to their good characteristics.

2.1.4.2 Transparent TFT ideal operation mode

Transparent TFT ideal behaviour is very similar to the common MOSFET. The difference between gate and source voltage, V_{GS} value, determines the mode in which the TFT is operating. With the ground connected to the source and a positive voltage connected to the drain, if gate-source voltage

V_{GS} is smaller than a threshold voltage V_{th}, there is no current through the channel and transistor is in cut-off mode. This mode can be seen in figure 2.7. The formula of current in this operation mode is:

$$I_{DS} = 0 \tag{2.3}$$

Figure 2.7: Transparent TFT in cut-off mode (no current flow)

If V_{GS} is greater than V_{th}, an uniform electron accumulation layer at the interface channel-insulator is formed, and current can flow from the source to the drain. When the V_{GS} value increases, the electron layer and the current flow increases. This is the pre-saturation mode. This mode can be seen in figure 2.8. The formula for the current in this operation mode is [1]:

$$I_{DS} = \frac{W}{L}\mu C_G[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}] \tag{2.4}$$

Figure 2.8: Transparent TFT in linear mode

where W is the gate width (μm), L is the gate length (μm), μ is the channel mobility ($cm^2/V.s$), C_G is the gate capacitance density (F/cm^2), V_{GS} is the gate-source voltage (V), V_{th} is threshold voltage (V) and V_{DS} is drain-source voltage (V).

The current value does not increase to infinite with bigger V_{GS}. There is a maximum value, called saturation current, where the current stabilizes despite an increasing V_{DS}. This mode can be seen in figure 2.9, where it is visible a depletion of electrons near the drain. The effect of the channel modulation, due to the decreased channel length with high drain voltage, can also increase the current by a λ parameter. The formula of current in this operation mode is:

$$I_{DS} = \frac{W}{2L}\mu C_G(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{2.5}$$

Figure 2.9: Transparent TFT in saturation mode

2.1.4.3 Transparent TFT non-ideal characteristics

The material used for transparent TFT present worse characteristics, and causes more detrimental behaviour than MOSFET's counterparts. The main issues are threshold voltage shift and source-drain contact resistance.

The main cause for threshold voltage shift is the charge trapping in the channel-dielectric interface. A. Suresh and J. Muth [21] report the occurrence of positive gate bias stress due to negative charge trapped between these two layers, resulting on smaller current flowing through the channel. Therefore, larger gate-source voltage is needed to overcome the reduction of free carriers in the channel.

Some reports [22] [23] rises concern on the instability of threshold voltage with water vapour exposure and describe the effects of environment conditions on the TFT operation and characteristic. Under positive gate voltage stress, oxygen is absorbed on IGZO, capturing an electron from the conduction band and decreasing the accumulated electrons density, thus increasing threshold voltage. However, water vapour exposure gives an electron, decreasing threshold voltage value.

Different proposals have been reported to improve this behaviour. Annealing of channel layer makes a better performance in this characteristic, resulting on more stable threshold voltage [16]. Passivation also avoids a large influence of atmospheric conditions, protecting the channel with a diffusion barrier layer and decreasing the threshold voltage shift [23].

Some studies are also concerned with the effects of temperature and light on threshold voltage shift, which is very important to refer due to the specific application in question — photovoltaic panels. S. Kuk et al. [24] report an increase from 0.89 V to 4.35 V as light temperature increases from 30ºC to 90ºC, explaining the donation of electrons to the conduction band as reason for so large increase. Light illumination enhances the charge trapping.

S. Lee et al. [25] refer a threshold voltage shift in 7000 seconds by less than 1 V in dark state, but an 8.7 V shift with 400 nm light and intensity of $0.025 mW/cm^2$, when a negative bias stress is applied. However, they also report a saturation value for the shift, caused by the filling of the available charge-trapping states to the full.

Threshold voltage shift is an increasing problem if the transistor is conducting for a long time. DC/DC converters use clock signals to open or close the transistor as a switch, so the transistor will not have a large time of conduction and threshold voltage shift will not be the main problem to concern. However, for the regulation of the output voltage of the DC/DC converters, it is necessary

to create an amplifier that requires specific values of threshold voltage for its TFT's, otherwise it is unstable. For this reason, this is an issue that concerns more when the regulator is designed.

Another possible reason of concern with TFTs is the source-drain contact resistance. According to P. Barquinha et al. [20], source-drain contact resistance is a phenomenon that affects the performance of thin-film transistor, mainly the mobility of short channel devices, because the overlap between contacts and the channel may not be negligible when compared to the length of the channel. They report higher maximum current in linear and saturation modes with molybdenum (Mo) or Ti/Au contacts. They also refer an improvement on maximum current and field-effect mobility with annealing after placing source-drain contacts. Source-drain contact resistance can decrease the current flowing through a closed transistor, creating a voltage drop. For a boost converter, a high voltage drop can result in a low voltage level at the output.

2.1.4.4 Transparent TFT as a switch

In order to use transparent TFT to implement a switch, it is important to study the behaviour of the transistors in this situation. Speed and voltage precision are issues that should be referred in detail.

B. Razavi [2] studied the behaviour of the transistor as a switch with a circuit described in figure 2.10.

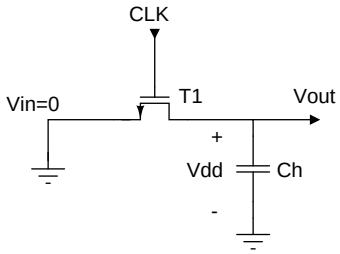


Figure 2.10: Switch mode transistor with capacitor at the drain [2]

Suppose that the drain of the transistor is connected to a charged capacitor with an initial voltage of V_{DD}. If $CLK = V_{DD}$ at initial time, the transistor operates in saturation and the capacitor is discharged, decreasing the value of V_{out}. When $V_{out} = V_{DD} - V_{th}$, the transistor operates at the triode region. The capacitor continues to discharge until zero voltage. In the case of figure 2.11, where the capacitor is connected to the source, V_{in} charges the capacitor when $CLK = V_{DD}$.

If the gate has a voltage level of V_{DD}, the transistors conducts current in both directions to have the same voltage at both sides. The author determines the output voltage level depending on time (t) as:

$$V_{out} = V_{DD} - V_{th} - \frac{1}{\frac{1}{2}\mu\frac{C_G}{C_H}t + \frac{1}{V_{DD}-V_{th}}} \tag{2.6}$$

Analysing this formula, it can be assumed that the voltage at the output will never be higher than $V_{DD} - V_{th}$, and the lower mobility of the transistor can decrease this voltage to very low values.

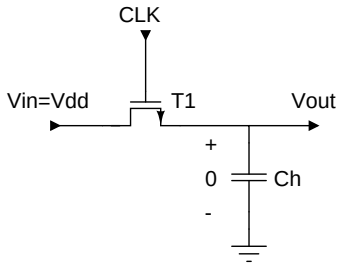


Figure 2.11: Switch mode transistor with capacitor at the source [2]

That suggests the effect of on-resistance will have a large effect on the output voltage level. The on-resistance can be determined by:

$$R_{on} = \frac{1}{\mu C_G \frac{W}{L}(V_{DD} - V_{in} - V_{th})} \tag{2.7}$$

The input voltage has also an effect on this resistance, increasing it if the voltage level is higher. Another consideration to take into account is the speed. The factors that influence the time response is the on-resistance of the transistor and the capacitance used. Those create a time constant $\tau = R_{on}C_H$ associated, that increases as higher the value of resistance and capacitance is. Due to the effect of the input voltage on the on-resistance, the voltage level can increase the time constant as well. One common problem associated to the utilization of a transistor as a switch and its effect on precision is the charge that is accumulated in its channel during the on-time. This charge can be calculated as:

$$Q_{ch} = WLC_G(V_{DD} - V_{in} - V_{th}) \tag{2.8}$$

When the transistor turns off, this charge exits from drain and source, half for each other, giving some current that should not exist. This phenomenon is called charge injection and creates an undesired ripple, DC offsets and non-linearity if the body-effect is taken into account. The voltage error level associated to charge injection on each side is calculated by:

$$\Delta V = \frac{WLC_G}{C_H}(V_{DD} - V_{in} - V_{th}) \tag{2.9}$$

Another consideration for voltage precision is the clock feedthrough, which results from parasitic capacitances coupling between gate-source and gate-drain. Considering C_{ov} the overlap capacitance per unit width, the error can be expressed as:

$$\Delta V = V_{CLK}\frac{WC_{ov}}{WC_{ov} + C_H} \tag{2.10}$$

Analysing carefully the formulas of speed (time constant) and voltage precision associated to charge injection, it can be concluded that there is a trade-off on choosing the value of the sampling capacitor and the width of transistors. If the transistors are larger, it reduces the on-resistance and

improves the speed, but it increases the error level. If the sampling capacitor is larger, it reduces the speed and also the error level. Notice that the mobility and length of the transistor do not influence the voltage, and the input voltage does not influence the clock feedthrough unlike the voltage level at the gate.

2.1.5 Fabrication processes

Since the appearance of transparent thin-film transistors that research is made to improve the fabrication processes. The goal is to achieve more precision and control of thickness and layout, when the thin-film is created. The fabrication processes of transparent devices include pulsed laser deposition, photolithography, etching, chemical layer deposition, atomic layer deposition and physical vapour deposition.

2.1.5.1 Pulsed laser deposition

K. Nomura et al. [16] report this technique in the first TFT created. It is used for deposition of indium gallium zinc oxide (IGZO) and indium tin oxide (ITO) thin films. Inside a vacuum chamber, a high and short energy laser pulses collide on a solid target, typically ceramic. The laser pulse beam creates a phenomenon of vaporization of the target. The vapour condenses, and generates a thin film on the substrate.

2.1.5.2 Photolithography

It is the process of transferring images from the computer database to the wafer. Initially, it is used a computer-aided design system to draw the layer. Then, a photoresist is exposed to ultraviolet light, which make its material characteristics to be altered. A photomask is used to create the pattern where it is opaque or transparent to UV light.

2.1.5.3 Etching

This process removes the exposed material created on photolithography to refine the desired pattern. This can be achieved by wet etching, where acids are used to remove the material depending on the time and temperature it is exposed, and dry etching, where the material is exposed to a bombardment of ions, and portions of material are removed selectively.

2.1.5.4 Chemical layer deposition

Technique obtained by the introduction of chemical gases on a chamber, which reacts with the wafer in order to design the thin film. This makes a flow system, where reactant gases flow into the substrate and products are removed from it.

2.1.5.5 Atomic layer deposition

The thin-film layers are obtained from a sequential exposure of precursors, or chemical gases, reacting with the substrate. It is a self-limiting process, which enables a control on growth deposition and uniformity even on large areas, and it differentiates from chemical layer deposition due to the separation of precursors by inert gas during reaction.

2.1.5.6 Physical vapour deposition

These processes create deposition of atoms from a source onto a substrate. The two mainly processes of this type are evaporation and sputtering. In the first, it is created by a resistive heating with electric current. While the material is melting and evaporating, the vapour material condenses, creating the thin film. The second one, sputtering, uses the collision of gaseous ions to dislodge atoms while thin film is deposited. It is a very controllable technique in terms of thickness of the film, and very used nowadays. CENIMAT, a Portuguese scientific research centre, uses the RF sputtering technique [26]. It utilizes energy from radio waves to ionize the gas atoms. Further, the ions get in contact with the substrate, creating the film.

2.2 Voltage Multipliers

Voltage multipliers or charge-pumps use capacitors and switches or diodes to achieve a different output voltage. The principle of operation is to store energy in capacitors, charging and discharging, transferring it to the output load [5]. The study of these devices can be important for the implementation of transparent DC/DC converter, because it could enable the desired functionalities of a normal DC/DC converter without using inductors, avoiding the problems referred to the construction of a transparent inductor, such as the low quality factor.

2.2.1 Output Voltage and Load Current

In order to build a background on specific parameters, behaviour of the charge-pumps and to understand the principles of functioning that exist in these devices, some of the initial charge-pump topologies created will be presented. The first voltage boosting circuit designed was the Cockcroft-Walton [3], presented in figure 2.12.

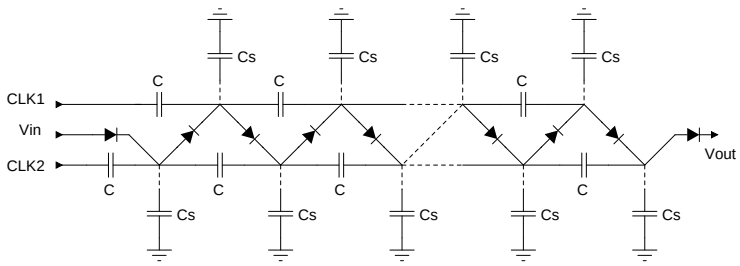


Figure 2.12: Cockcroft-Walton configuration [3]

This circuit uses n-stage diodes connected to coupling capacitors that are charged by the clock signals with the same voltage level as V_{in}, and provide this charge to the output stage. With N stages, the output voltage expected would be $(N+1)V_{in}$ if the non-ideal characteristics are not taken into account.

In a way of improving, J. Dickson [4] modified the circuit, connecting each of the coupling capacitors directly to the clock inputs, designing the capacitors in parallel. The circuit is presented in figure 2.13.

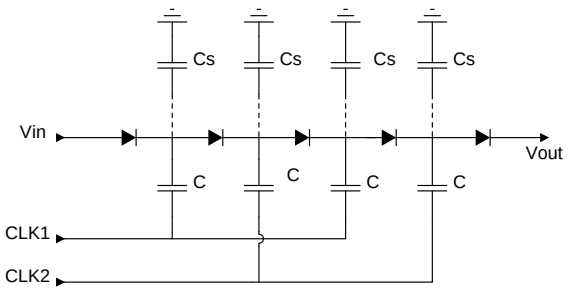


Figure 2.13: Dickson charge pump [4]

The increased voltage in each stage is given by:

$$V_N - V_{in} = V_C - V_D - V_L \tag{2.11}$$

where V_C is the voltage level due to the coupling capacitors, given by the ratio $V_C = \frac{C}{C+C_S}V_{CLK}$, V_D is the voltage drop in each diode and V_L is the voltage that the capacitors charge and discharge with a load current at the output given by $I_{out} = f(C+C_S)V_L$ (f is the clock frequency). The final expression for N stages is given by:

$$V_N - V_{in} = N[(\frac{C}{C+C_S})V_{CLK} - V_D - \frac{I_{out}}{(C+C_S)f}] \tag{2.12}$$

The maximum output resistance of a charge-pump with N stages depends of the frequency and the pumping capacitors by:

$$R_{out} = \frac{N}{fC_{CLK}} \tag{2.13}$$

An important theoretical analysis of the charge-pumps is made by R. Perigny [27]. This author calculates the output voltage level of one stage of a charge-pump with an inclusion of ripple maximum and minimum level. In the load capacitor, the charge Q_{load} accumulated when the lower voltage V_{low} is applied to the terminals is:

$$Q_{load} = C_{load}V_{low} \tag{2.14}$$

When the boosting capacitor C_a is charged to V_{DD}, the charge is expressed as:

$$Q_a = C_a V_{DD} \tag{2.15}$$

When C_a connects to C_{load}, it is applied the voltage V_{high}, and the charge at the load Q_{load2} is:

$$Q_{load2} = C_{load} V_{high} \tag{2.16}$$

At this time, the charge stored in the boosting capacitor is:

$$Q_{a2} = C_a(V_{high} - V_{DD} \tag{2.17}$$

The principle of conservation requires that:

$$Q_a + Q_{load} = Q_{a2} + Q_{load2} \tag{2.18}$$

The slope at the output is given by $I_{out}/(C_{load} + C_a$, and it decreases in half clock period, so:

$$V_{high} = V_{low} + \frac{I_{out}}{2 f_{clk}(C_a + C_{load}} \tag{2.19}$$

Combining the two equations and simplifying, the lower voltage is given by:

$$V_{low} = 2V_{DD} - \frac{I_{out}}{2 f_{clk} C_a} \tag{2.20}$$

With no load current, the output voltage is estimated by $2V_{DD}$, but this level changes when it is applied a load resistance at the output, creating a load current. Therefore, there is a decrease of I_o/C_a on the output voltage, where C_a is the pumping capacitance, so the voltage difference between maximum and minimum, with a clock frequency of f_{clk}, is:

$$\Delta V_{out} = \frac{I_o}{2 f_{clk} C_a} \tag{2.21}$$

If a load capacitor C_x is added to the output, the voltage ripple is not so large, due to the slower transition of voltage level. The slope can be calculated by:

$$\Delta V_{out} = \frac{I_o}{2 f_{clk}(C_a + C_x)} \tag{2.22}$$

With the voltage ripple calculated, the minimum voltage level is the difference between $2V_{DD}$ and ΔV_{out} without the load capacitor. Notice that the load capacitor is used only to reduce the maximum voltage V_{high}, and it does not have influence on the V_{low}. The maximum voltage is:

$$V_{high} = V_{low} + \frac{I_o}{2 f_{clk}(C_a + C_x)} = 2V_{DD} - \frac{I_o}{2 f_{clk}(C_a + C_x)} + \frac{I_o}{2 f_{clk}(C_a + C_x)} \tag{2.23}$$

This expression does not take into account the on-resistance of the diodes, that reduce the output voltage as higher as the resistance is. In chapter 3 will be presented and discussed newer and improved topologies, which reduce some constrains that exist in these circuits.

2.2.2 Power and Efficiency

Efficiency is an important parameter to study when DC/DC converters and charge-pumps are designed. D. Baderna et al. [28] calculate the efficiency by the relation between the power at input and output. The power at the input is equal to the sum of power at the output, added by the resistive and dynamic losses, so the efficiency is:

$$\eta = \frac{V_{out}I_{out}}{V_{out}I_{out} + P_{res} + P_{dyn}} = \frac{V_{out}I_{out}}{V_{out}I_{out} + R_{out,id}I_{out}^2 + kNfC_{par}V_{DD}^2} \tag{2.24}$$

where k is a coefficient of proportionality and C_{par} is the equivalent parasitic capacitance in each stage. The author divides the parasitic capacitance in two parts, C_{top} and C_{bot}. The first component is more dependent of the topology, because it is created by the design of wider transistors and the voltage level that the transistors have in their terminals. If C represents the value of the pumping capacitors in each stage, the output voltage of the both devices can be calculated as:

$$V_{out} = \frac{C}{C + C_{top}}[(N + 1 + \beta)V_{DD} - R_{out,id}I_{out}] \tag{2.25}$$

The effective output resistance is $R_{out} = \frac{C}{C+C_{top}}R_{out,id}$, and the maximum load current that the devices can deliver is $I_{out,max} = \frac{NV_{DD}}{R_{out,id}} = fCV_{DD}$, so the efficiency can be estimated as:

$$\eta = \frac{V_{DD}I_{out}(N + 1 + \beta - R_{out,id}I_{out}^2}{V_{DD}I_{out}(N + 1 + \beta) + (\alpha + \beta)(1 + \beta)NfCV_{DD}^2} \tag{2.26}$$

The conclusion is that the efficiency η decreases as higher as β is.

J. Starzyk [5] compare different charge-pump designs on the boosting energy required. Since the load resistance is not infinite, the circuits do not present a perfect behaviour, such as $V_{out}/V_{in} = 0.5$ in step-down and $V_{out}/V_{in} = 2$ in step-up converter. The output voltage is as lower as the load resistance is.

The author [5] present a two-phase voltage doubler (TPVD) with the design in figure 2.14. The doublers can be used in cascade as represented in figure 2.15.

Removing the second capacitor in each doubler, J. Starzyk [5] presents a multiphase voltage doubler (MPVD), which need half of the capacitors for the same output/input voltage ratio. The circuit is shown in figure 2.16.

Starzyk compares the improved charge-pumps to the standard one from Dickson in figure 2.17. Some of the Starzyk's conclusions [5] are that the number of stages used does not affect the output power. It depends on the load resistance, capacitors and clock frequency. When the value

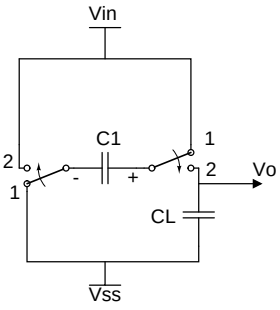


Figure 2.14: Voltage doubler [5]

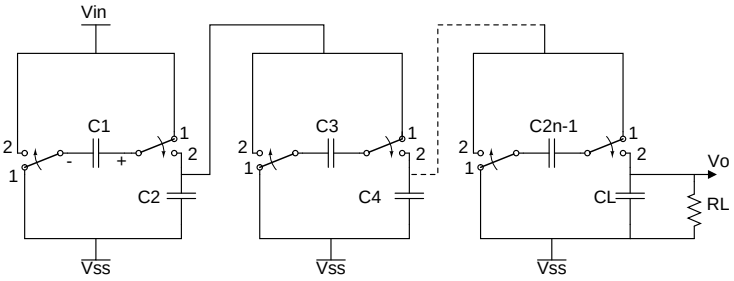


Figure 2.15: Simply cascade voltage doublers [5]

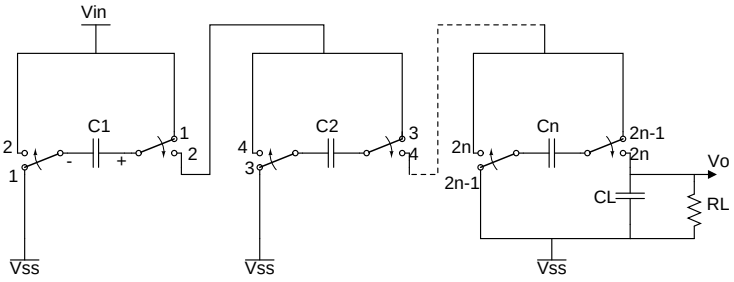


Figure 2.16: Multiphase voltage doublers [5]

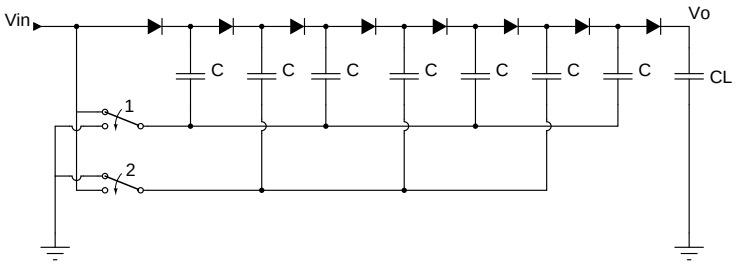


Figure 2.17: Dickson charge pump [5]

of capacitors increase, power increases. The author estimates the boosting energy for Dickson

charge pump as:

$$W_D = \frac{(N+1)(N+2)}{12} A V_{in}^2 \tag{2.27}$$

where A is the designed area with equal capacitors and N is the ratio V_{out}/V_{in}. The TPVD's topology has a boosting energy of:

$$W_{tp} = \frac{5(N^2-1)A}{12 log_2 N} V_{in}^2 \tag{2.28}$$

and for MPVD's topology:

$$W_{mp} = \frac{(4N^2-1)A}{6 log_2 N} V_{in}^2 \tag{2.29}$$

The results show that for TPVD's and MPVD's energy depends less than quadratically with voltage gain [5]. For Dickson's charge pump, the dependency is higher. In fact, the output power for the same load resistance is higher on Dickson's charge pump and lower on TPVD's. TPVD's presents also lower rise times than MPVD's.

2.2.3 Step-Up and Step-Down - a question of design

M. Wens and M. Steyaert [6] presented another example of charge-pump step-up DC-DC converter based on charge-pump, as shown in figure 2.18, studying its output voltage level and efficiency expected.

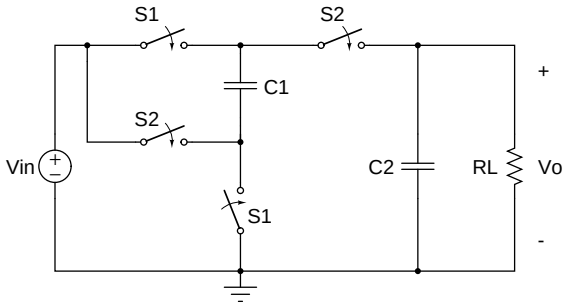


Figure 2.18: Charge-Pump Step-Up Converter [6]

When the switches are at position 1, the voltage source charges capacitor C_1. C_L discharges to R_L. When the switches are at position 2, the lower terminal of C_1 connects in series with the voltage source, and C_L and R_L receive charge from the both. Hence, the output voltage is higher than the input. Makowski in [5] refers that the V_{out}/V_{in} ratio is limited by 2^n, where n is the number of capacitors used.

M. Wens and M.Steyaert [6] estimate the output voltage for ideal converter by:

$$V_{out} = R_L I_{out} = R_L f_{SW} \Delta Q_{SW} = R_L f_{SW} C_1 \Delta V_{C_1} = R_L f_{SW} C_1 (2V_{in} - V_{out}) \tag{2.30}$$

$$V_{out} = \frac{R_L f_{SW} C1 Vin}{1 + R_L f_{SW} C1} \tag{2.31}$$

where f_{SW} is the switching frequency, ΔQ_{SW} is the amount of charge being transferred to the output in each switching cycle and ΔV_{C_1} is the difference of voltage level between switching state 1 and 2.

The efficiency of the converter is divided by the two stages of switching. The efficiency on first stage is calculated by the energy in C_1 divided by the energy transferred to the capacitor:

$$\eta_{\Phi_1} = \frac{E_{C_1}}{E_{V_{in} \to C_1}} = \frac{V_{out}}{2V_{in}} \tag{2.32}$$

When C_1 is discharged, the efficiency is estimated with the energy in C_2 divided by the energy transferred from source and C_1 to C_2:

$$\eta_{\Phi_2} = \frac{E_{C_2}}{E_{V_{in} C_1 \to C_2}} = \frac{2C_1V_{in} + C_1V_{out} + 2C_2V_{out}}{4C_1V_{in} + 2C_2V_{in} + C_2V_{out}} \tag{2.33}$$

The resulting efficiency of the circuit is:

$$\eta_{up} = \eta_{\Phi_1}\eta_{\Phi_2} = \frac{V_{out}(2C_2V_{out} + C_1(2V_{in} + V_{out}))}{2V_{in}(4C_1V_{in} + C_2(2V_{in} + V_{out}))} \tag{2.34}$$

The authors in [6] estimate an efficiency between 35% if $V_{out}/V_{in} = 1$ and 100% if $V_{out}/V_{in} = 2$. This circuit has some issues due to the large number of switches comparing with pumping capacitors. For the transparent technology, the switch is substituted by a TFT with larger on-resistance. The voltage level is reduced if there are many transistors used on the converter main path. Besides, there is no full time boosting to the output, because it is used an output capacitor to hold the voltage level at good level. However, a large ripple at the output is not avoided.

Beyond the analysis of a step-up charge-pump, there is also the possibility to create a step-down circuit. This one returns a lower voltage at the output than the applied at the input. M. Wens and M. Steyaert [6] present an example of charge-pump step-down DC-DC Converter based on voltage doubler in figure 2.19.

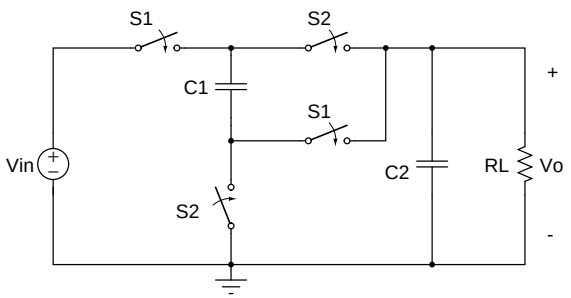


Figure 2.19: Charge-Pump Step-Down Converter [6]

When the switches are at position 1, capacitors C_1 and C_2 are charged by the connection in series with the voltage source. A portion of current goes also through R_L. With switches at position 2, there is no connection with the source, C_1 discharges its energy to C_2 and R_L. With this principle of switching, V_{out} will be, ideally, $V_{in}/2$. Physically, the authors [6] estimate the output voltage using the same fundamentals as with the step-up converter:

$$V_{out} = R_L I_{out} = R_L f_{SW} \Delta Q_{SW} = R_L f_{SW} C_1 \Delta V_{C_1} = R_L f_{SW} C_1 (V_{in} - 2V_{out}) \tag{2.35}$$

$$V_{out} = \frac{R_L f_{SW} C_1 V_{in}}{1 + 2R_L f_{SW} C_1} \tag{2.36}$$

To estimate efficiency, on the first switching position, the energy in C_1 and C_2 is divided by the energy transferred from voltage source to these capacitors:

$$\eta_{\Phi_1} = \frac{E_{C_1 C_2}}{E_{V_{in} \to C_1 C_2}} = \frac{V_{in} + 2V_{out}}{2V_{in}} \tag{2.37}$$

On the second switching mode, efficiency is calculated by the ratio between the energy in C_2 and the energy transferred from C_1 to C_2:

$$\eta_{\Phi_2} = \frac{E_{C_2}}{E_{C_1 \to C_2}} = \frac{C_1 V_{in} + 2C_2 V_{out}}{V_{in}(2C_1 + C_2) - 2C_1 V_{out}} \tag{2.38}$$

Total efficiency of the circuit is obtained multiplying both values:

$$\eta_{up} = \eta_{\Phi_1} \eta_{\Phi_2} = \frac{(C_1 V_{in} + 2C_2 V_{out})(\frac{V_{in} + 2V_{out}}{2V_{in}})}{C_2 V_{in} + 2C_1 (V_{in} - V_{out})} \tag{2.39}$$

The same authors [6] estimate an efficiency of 100% if $V_{out}/V_{in} = 0.5$. This value decreases with lower values of V_{out}/V_{in}.

Analysing the step-up and step-down circuits, there can be concluded that the difference between a step-up and step-down converter is the position of first capacitor, namely, the flying capacitor C_1. As referred in last subsections, on the second switching position, step-up converters have this capacitor connected in series with R_L and the input source. In fact, the voltage source is never disconnected from the rest of the circuit, in contrast to step-down converters. Therefore, step-down converters have the flying capacitor always connected to output, in opposition to the step-up that has it always connected to the input.

The adaptation of the converter for a desired output voltage is achieved with a different schematic of the circuit. The position of capacitors influences the output voltage level, so the design of circuit must take into account what is expected.

2.3 Operational Amplifiers with transparent TFT's

The questions of transparency changes not only the design of DC/DC Converters, but also the limitations of an operational amplifier. In fact, the most important difference that exist between

a non-transparent and transparent amplifier is the lack of p-type transistor devices. This section presents the different existing stages and factors that must be taken into account when an Op-Amp with only n-type transistors is designed.

2.3.1 Single-Stage Amplifiers

2.3.1.1 Common-Source Stage

The common-source stage is one of the most common stages in an Op-Amp. The configuration is presented in figure 2.20

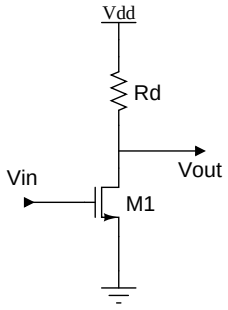


Figure 2.20: Common-source stage

One of the most important characteristic that this topology presents is the small-signal gain presented by:

$$A_v = -g_m(R_D||r_o) \tag{2.40}$$

Analysing this configuration, this stage can be used to invert the signal due to the negative gain. It can be well used to increase the small-signal gain, if a correct combination of the transistor output resistance r_o, and the load resistance R_D. To have higher values of gain, the resistances should be similar to have a high value of equivalent resistance. The voltage gain of this topology has a high dependence on the intrinsic parameters of the transistor, which can be prevented with a common-source stage with source degeneration, presented in figure 2.21.

If a resistance is applied to the source of the input transistor and the expression of small-signal gain is:

$$A_v = \frac{-g_m R_D}{1 + g_m R_s} \tag{2.41}$$

And the equivalent output impedance is:

$$R_{out} = R_D||r_o \tag{2.42}$$

If $g_m R_s >> 1$, the gain expression is more dependent of the resistance ratio $A_v = -\frac{R_D}{R_s}$.

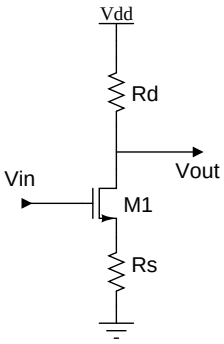


Figure 2.21: Common-source stage with source degeneration

2.3.1.2 Source-Follower Stage

This stage is mostly used to connect high load impedance stages to low impedance stages, operating as a voltage buffer. The schematic is presented in figure 2.22.

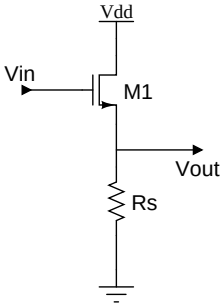


Figure 2.22: Source-follower stage

The small-signal gain for this stage is:

$$A_v = \frac{g_m(R_s||r_o)}{1+g_m(R_s||r_o)} \tag{2.43}$$

With the gm in this expression, the gain begins from zero with $V_{in} = V_{th}$, and increases with higher values of V_{in}, with a approximation to 1. To have a lower dependence of the current to the input voltage level, a transistor operating in saturation region can replace the resistor R_s. This transistor will work as a current source. The output impedance is estimated by:

$$R_{out} = (1/g_m)||R_s||r_o \tag{2.44}$$

Comparing with common-source stage, source-follower presents a lower output resistance, due to the low values of $\frac{1}{g_m}$.

2.3.1.3 Common-Gate Stage

This stage presents the input voltage applied to the source of the transistor. The gate of the transistor is biased with a DC voltage to operate in the saturation region. The schematic of this stage is presented in figure 2.23.

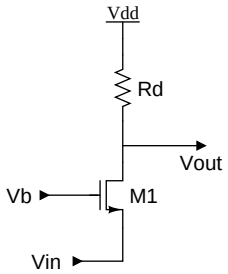


Figure 2.23: Common-gate stage

Analysing the small-signal gain, it can be estimated by:

$$A_v = g_m(R_D||r_o) \tag{2.45}$$

This stage does not invert the signal and it has very low input impedance, due to the applied input at the source. The input impedance is estimated by:

$$R_{in} = \frac{1}{g_m} \tag{2.46}$$

In multi-stage amplifiers, the low input impedance of this stage decreases the voltage gain of the previous stage. Besides, the saturation of the transistors is also necessary, so the biased transistor, due to its low impedance, has a low value of V_{gs}. Those are the disadvantages of this configuration.

2.3.1.4 Cascode Stage

Comparing with common-source, cascode stage uses a biased transistor between the input transistor and the output. This stage uses the same principles of common-gate stage with a current source, instead of a voltage, applied to the source of the biased transistor, using an input transistor. However, this stage has the disadvantage that the voltage level applied to the drain of the biased transistor must be enough to have the both transistors in saturation. This limits the value of R_D, and the small-signal gain. The schematic of this stage is presented in figure 2.24.

The small-signal gain can be estimated by:

$$A_v = -\frac{g_{m1}}{g_{m2}} g_{m2}(R_D||r_o) \tag{2.47}$$

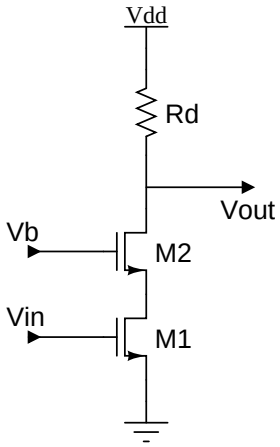


Figure 2.24: Cascode stage

The expression of the gain is the same as the common-source small-signal gain. As the common-source stage, this configuration inverts the signal applied. The advantages of this configuration is the very high output impedance, due to the large number of transistors. The output resistance is estimated by:

$$R_{out} = [1 + g_{m2} r_{o2}] r_{o1} + r_{o2} \tag{2.48}$$

The main effect that this stage has is the elimination of Miller effect on the input transistor, increasing the bandwidth response.

2.3.2 Differential Pair

This configuration is one of the most important because it receives the two differential inputs of the amplifier. The schematic of this configuration is presented in figure 2.25.

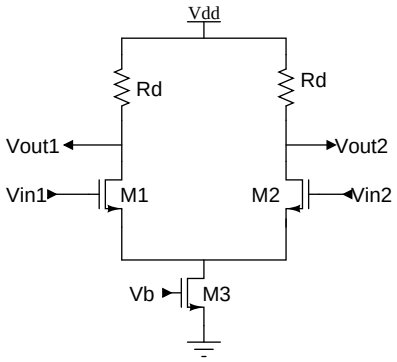


Figure 2.25: Differential pair

To analyse the differential pair theoretically, it can be assumed that the relation $V_{in1} - V_{in2}$ varies from $-\infty$ to $+\infty$. At initial stage, the voltage V_{in1} is more negative than the voltage V_{in2},

so the transistor M_1 is off, so $V_{out1} = V_{DD}$ and M_2 is on, so $V_{out2} = V_{DD} - R_D I_{SS}$. If the difference between $V_{in1} - V_{in2}$ becomes smaller, the output voltage tends to be $V_{out1} = V_{out2} = V_{DD} - \frac{R_D I_{SS}}{2}$. If $V_{in1} - V_{in2}$ becomes positive, the output voltages change in a symmetrical way. This is how the amplifier regulates the output voltage depending of the values at the input. The differential gain of this configuration take into account the two inputs, which have two components each, the differential and the common-mode. They are defined as:

$$V_{in1} = \frac{V_{in1} - V_{in2}}{2} + \frac{V_{in1} + V_{in2}}{2} \tag{2.49}$$

$$V_{in2} = \frac{V_{in2} - V_{in1}}{2} + \frac{V_{in1} + V_{in2}}{2} \tag{2.50}$$

To calculate the differential gain, there is only the differential component that is defined as input, as if there was applied a virtual ground between the sources of M_1 and M_2, so the output voltages are:

$$V_{out1} = -g_m(R_D||r_{o1})\frac{V_{in1} - V_{in2}}{2} \tag{2.51}$$

$$V_{out2} = -g_m(R_D||r_{o2})\frac{V_{in1} - V_{in2}}{2} \tag{2.52}$$

Considering that there is no common-mode component, the differential gain is expected to be:

$$A_d = V_{out1} - V_{out2} = -g_m(R_D||r_o)(V_{in1} - V_{in2}) \tag{2.53}$$

The differential pair should eliminate the effect of common-mode perturbations, but in reality the circuit is not fully symmetric due to the fabrication and the output impedance of M_3 is not infinite. Because of these facts, the common-mode variation exists, and its gain, considering a fully symmetric circuit and a finite output impedance of M_3, is estimated as:

$$A_{v,CM} = \frac{V_{out}}{V_{in,CM}} = -\frac{R_D/2}{(1/2g_m) + r_{o3}} \tag{2.54}$$

This component of gain can disturb the bias point and limit the output voltage swing. Besides, the non-symmetrical circuits create a difference on the currents between each side, increasing the issues mentioned. For all these reasons, the common-mode effect should be suppressed as much as possible, to have a very high common-mode rejection ration determined by:

$$CMRR = 20log_{10}(\frac{A_d}{|A_{CM}|}) \tag{2.55}$$

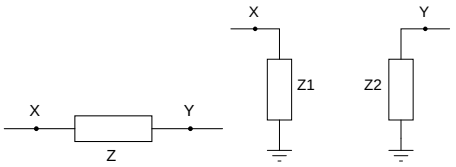
so it is the ratio between the differential and the common-mode gain.

2.3.3 Multi-Stage Amplifiers

In order to have high gain amplifiers with low output impedance, single-stage amplifiers are not enough, so there should be used multiple stages. However, with more stages used, there are applied more poles, and zeros in some cases, due to the resistances and capacitances added. This fact can produce an unstable behaviour of the amplifier under feedback, if there are dominant poles applied at high frequencies, decreasing the phase margin. To understand the principles of stability and frequency response of the amplifier, it is necessary to know in which way the poles and zeros are introduced in the phase, their origins and how to compensate their drawbacks.

2.3.3.1 Miller Effect

Miller's theorem describes one of the most important effects in analog circuits. It is related with the amplifier and the introduction of poles and phase response. This theorem states that a circuit presented in figure 2.26a can be converted in the circuit of figure 2.26b if $Z_1 = Z/(1-A_v)$ and $Z_2 = Z/(1-A_v^-1)$, where $A_v = V_y/V_x$.



(a) (a) (b) (b)

Figure 2.26: Application of Miller effect to a floating impedance

The importance of this theorem in amplifiers can be presented with the circuit in figure 2.27, that represents a common-source stage with the equivalent parasitic capacitances of a TFT, C_{GS} and C_{GD}. The equivalent capacitances connected to the ground, with a equivalent impedance of the capacitor of $Z_C = 1/(sC)$, for the node A is $C_A = C_{GS} + (1-A_v)C_{GD}$ and for the node B is $C_B = (1-A_v^-1)C_{GD}$. Due to the gain of the common-source stage $A_v = -g_m R_D$ is larger that unity, analysing the two nodes capacitances, it is considered that the capacitance at the input of the stage is higher than in the output, due to the Miller multiplication factor of C_{GD}. Therefore, the pole associated to the input is at lower frequencies.

2.3.3.2 Stability and Frequency Compensation

The capacitances and resistances associated to the amplifier have an important role on the stability and frequency response of the circuit. In fact, as non-dominant poles at higher frequencies worsens the phase responses, due to the lower phase margin introduced by a phase shift at high frequencies. That influences critically the stability of the amplifier under feedback. Frequency Compensation is the method to have better frequency responses. The frequency compensation can be made with additional capacitors or resistors in the circuit nodes where there are dominant poles, in order to

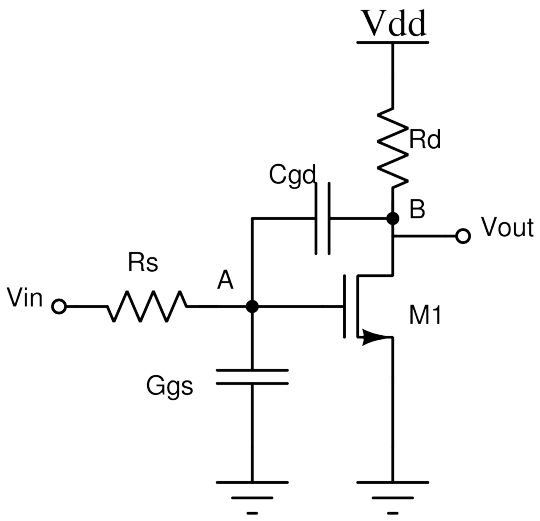


Figure 2.27: Common-source stage with parasitic capacitances

pull it into lower frequencies, resulting in higher phase margin. This technique is better explained in the chapter 4, where the frequency compensation of the proposed regulator is described.

Chapter 3

Bibliographic Review

There is not that many reports on transparent DC/DC Converters, but the ones that exist, invariably use voltage multipliers topologies instead of inductors. Besides, they use different switching modes. In transparent electronics, switches or diodes may be created with transistors. Therefore, the study of TFT is also very important to refer. This chapter starts with a review of research made for transparent TFTs with a-IGZO, with a historical perspective. Then, it is presented an overview of DC/DC converter proposals made until now. The initial topologies presented in charge-pumps section are not designed with transparent electronics, but they represent a step-forward to an efficient design of a switched-capacitor DC/DC converter. The next section presents the topologies that have been designed to regulate DC/DC converters. Last sections present an overview of the improved characteristics and a conclusion for the proposal presented in this report.

3.1 Thin-Film Transistors using a-IGZO

The production of transparent thin-film transistors have improved during the years with well-performed researches. This section does not intend to present an exhaustive report on all successful studies made with transparent TFT. However, a historical perspective on the basic behaviour improvements of these devices, with examples of some articles from different years, will be discussed.

The first TFT using a-IGZO in channel layer was reported by K. Nomura et al. [16] in 2004. It is a n-type TFT, where a-IGZO was deposited at room temperature by pulsed laser deposition on polyethylene terephthalate substract, creating a staggered top-gate structure. Insulator is 140 nm thick and the channel with a length of $50\mu m$ and a width of $200\mu m$. The estimation for saturation mobility is $8.3cm^2/V.s$ with a drain-source current of $0.02mA$, $V_{GS} = 5V$ and a leakage current of $10^{-10}A$. Field effect mobility is $5.6cm^2/V.s$.

P. Barquinha et al. [20] in 2008 reported an a-IGZO TFT with saturation mobility of $18.7cm^2/V.s$,

field-effect mobility of $24.5cm^2/V.s$, maximum drain-source current of $0.08mA$ and threshold voltage $V_{th} = 12.8V$. The transistor was created in a staggered bottom-gate structure with a 100 nm thick SiO_2 gate dieletric, a Ti/Au contacts with 15 nm and 135 nm of thickness, respectively, and 50 nm-thick a-IGZO layer deposited by RF sputtering. Annealing was performed after all depositions.

In 2009, K. Nomura et al. [29] reported a bottom-gate TFT with saturation mobility of $12.6cm^2/V.s$ and a threshold voltage between 1.4 V and 1.8 V. TFT's were created on SiO_2 substrate. A 40 nm-thick a-IGZO was deposited by pulsed laser deposition with oxygen partial pressure and a width and length of 300 and 50 μm, respectively. The device was subjected to annealing with water vapour at partial pressure, and Ti/Au were used for source/drain contacts.

A. Suresh et al. [30] in 2010 created an a-IGZO TFT using staggered bottom-gate structure. Gate dielectric was deposited with 120 nm-thick Al_2O_3 with atomic layer deposition. A 40 nm-thick a-IGZO layer and 200 nm-thick indium tin oxide were created by physical vapour deposition. No annealing steps were employed. The authors present a threshold voltage of 3.5 V and saturation field effect mobility of $15cm^2/V.s$ with $V_{DS} = 20V$. There was reported a leakage current of $1pA$.

S. Hong et al. [10] use in their transparent DC/DC converters a-IGZO TFT with co-planar top-gate structure. As source-drain material, there is deposited by sputtering indium-tin oxide. For the insulator there was used Al_2O_3 deposited by atomic layer deposition at 150^oC The results present a threshold voltage of -0.8V to reach a drain current of 100pA, $20.6cm^2/(V.s)$ of field effect mobility and a subthreshold slope of 0.2 V/dec at room temperature.

D. Kang et al. [31] created in 2011 a TFT using co-planar top-gate structure. On 200 nm-thick glass substrate, a 20 nm-thick a-IGZO layer was deposited using sputtering. For insulator, the authors used 200 nm-thick SiO_2 and patterned molybdenum for gate electrodes. After patterning a-IGZO and etched SiO_2, a 400 nm-thick SiN_x layer was deposited. Then, a 200 nm-thick molybdenum was deposited for source-drain contacts. With $V_G = 20V$, field-effect mobility is $24.7cm^2/V.s$ in saturation mode and $21cm^2/V.s$ in linear mode. Threshold voltage is around 3.6 V.

The different studies made suggests a improvement on TFT behaviour, with better field-effect mobility, lower threshold voltage and lower resistance. During the years, various materials for insulators and source-drain contacts were tested and results were compared. For channel layer, a-IGZO is actually the material with best performance. For the source-drain contacts, the main materials reported with better results are Ti/Au and molybdenum. Analysing the performance of the TFT depending of the structure used, the recent reports suggest better results of mobility with a top-gate structure, due to the better isolation of the channel to external factors. The transparent TFT fabricated in CENIMAT use the staggered bottom-gate structure, so the performance of the transistor in terms of mobility is not expected to be higher than $20cm^2/(V.s)$. The effects of

high on-resistance in charge-pumps and DC/DC converters using switched-capacitor stages were discussed in chapter 2.

3.2 Charge-Pumps

This section presents the charge-pumps designed during the years. Initially, there is considered the first topologies in non-transparent electronics. Later, the configurations designed with transparent TFT's.

3.2.1 Non-transparent designs

3.2.1.1 Initial Configurations

The first charge-pump reported are dated from 1932, with the Cockcroft-Walton multiplier [3]. As mentioned in the last chapter, it used clock signals to charge the capacitors and diodes through the main path, increasing the voltage in the output to an expected voltage of $2V_{DD}$. However, the circuit has some constrains. One of them is that the coupling capacitors C must have a much larger value of capacitance than the stray capacitances C_s, to have an efficient voltage increase. Due to the high values of stray capacitance in the substrate of monolithic circuits, the circuit has limitations on efficient voltage multiplication. Besides, the voltage drop associated to the diodes limits the output voltage level even with a large number of stages. With transparent technology, diodes are replaced by TFT's, which several constrains were discussed such as the on-resistance and voltage drop.

Another initial configuration referred in the last chapter is the Dickson's charge-pump dated from 1976 [4]. This is a improve of the Cockcroft-Walton configuration, due to the connected pump capacitors directly to the ground. According to the author, this enables a smaller difference between the coupling and stray capacitances, in order to have efficient multiplication of voltage. Although the problem with stray capacitances is reduced, the voltage drop across the diodes is not avoided. Furthermore, there is a high threshold voltage needed for the transistors, due to the differentiation between switching stages, and a large voltage drop across the transistor when the following capacitor is transferring its charge. These facts increase the parasitic capacitances associated to the circuit, according to Baderna [28]. These capacitances reduce the time response of the circuit and the maximum frequency allowed, resulting in worse response of the circuit to the load currents.

3.2.1.2 Cross-connected Configuration

P. Favrat et al. [7] proposed a new voltage doubler with cross-connected transistors to reduce the parasitic capacitances, improving the charge-pump cell from Y. Nakagome et al. [32] with a double series switch of p-type transistors. The circuit is presented in figure 3.1.

With the two series p-type transistors added, the author refer that the load capacitor have not to be very high, without affecting the charge-pump efficiency. The cross-connection reduces

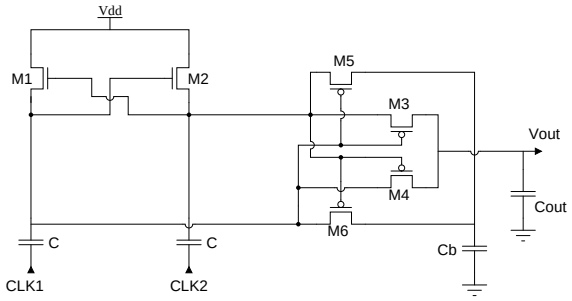


Figure 3.1: Cross-connected configuration from P. Favrat et al. [7]

the voltage drop on the transistors to a value lower than V_{DD}, because when one capacitor is discharging, the opposite side is charging, creating a full reverse bias of the junctions. The on-resistance is also lower, due to the synchronization of boosting on gate transistors.

The Favrat voltage doubler, with a cross-connected topology, has transistors with lower parasitic capacitance than the first topology, increasing the efficiency. Theoretically, Baderna [28] estimates the Dickson's charge-pump efficiency as 44.8%, and 56% for the Favrat's doubler efficiency. The p-type transistors can be substituted by a diode-connected TFT's, to answer to the transparent constrains.

3.2.1.3 Switch Bootstrapping Technique

The parasitic capacitance and output voltage level are two of the main concerns when a DC/DC converter using charge pumps topology is created. According to Y. Allasasmeh and S. Gregori [8], the usage of bootstrapping switches prevents short-circuit losses, due to the precision in controlling the switching times, and enables good efficiency with low supply voltage, due to a lower switch on resistance and lower power losses. The schematic of bootstrapping topology for a voltage doubler is presented in figure 3.2.

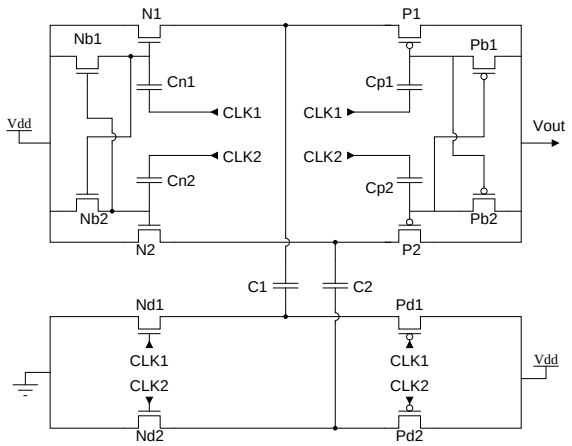


Figure 3.2: Bootstrapping configuration of charge-pump from Allasasmeh and Gregori [8]

Due to the added transistors and capacitances are not in the main current path between V_{DD} and V_{out}, the authors [8] refer that their area can be reduced, decreasing the parasitic capacitances. This phenomenon is helped with the fact that the gates of the first transistors are not connected to the main current path. They also report a higher output voltage in 1.5% due to this fact.

3.2.1.4 Switched-Capacitor based Embedded DC-DC Buck Converter

B. Maity and P. Mandal [9] present a non-transparent device that uses switched-capacitors to create a step-down DC/DC converter. The importance of this reference is the use of concepts that can be applied on the desired transparent DC/DC converter. The design is presented in figure 3.3.

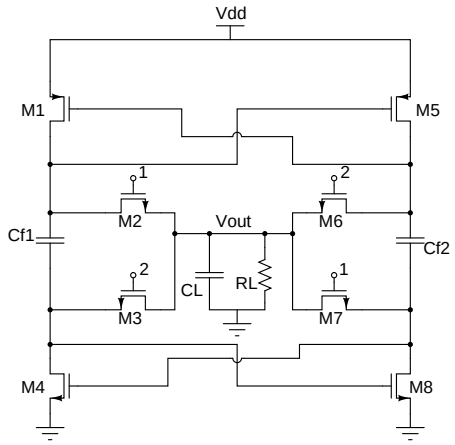


Figure 3.3: Switched Capacitor based Buck Converter [9]

Internal signals are used to control half of the switches, in order to reduce switching power loss and output ripple noise. The circuit shown in figure 3.3 is repeated 11 times and their output connects together with load capacitor and current source.

For a 10 mA current, results present a 1.35 V, with an input voltage range between 2.9 V and 3.8 V. For this voltage level, and a 25 mA load current, output ripple is 8 mV. Efficiency established on 79.5% for a load current between 1 mA and 25.5 mA. When the output voltage increases to 1.55 V, with load current from 1 mA to 7 mA, a peak power efficiency of 87% is achieved. This proposal uses p-type transistors, which can easily be replaced by n-type.

3.2.2 Configurations with TFT's

3.2.2.1 DC/DC Converters using Indium Gallium Zinc Oxide Thin-Film Transistors

S. Hong et al. [10] present the most close device to what we need to achieved. The proposed positive DC/DC Converter is presented in figure 3.4.

It has eight n-type IGZO TFT's, four pumping capacitors and two storage capacitors. When $CLK = 1$, the voltage level of node D is $2V_{DD}$ because it receives the energy stored on capacitor C_1. Node C has a voltage level of $2V_{DD} - V_{th}$ due to voltage drop across transistor N3. Therefore, node

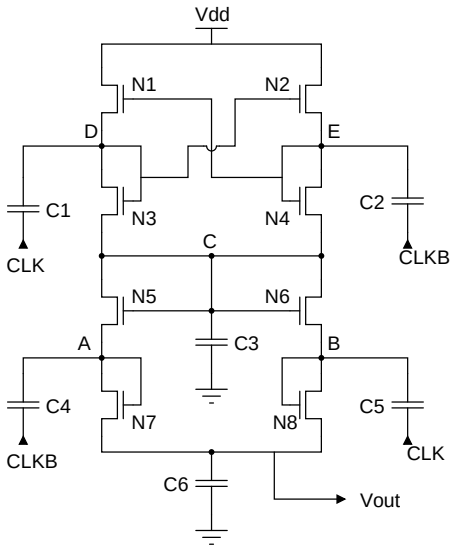


Figure 3.4: Transparent Step-Up DC/DC Converter [10]

B will receive the energy stored in capacitor C_5, so its voltage level becomes $3V_{DD} - 2V_{th}$. With the voltage drop in transistor N8, output voltage level is $3V_{DD} - 3V_{th}$. The same sequence happens in complementary nodes with $CLKB = 1$. As $V_{th} << V_{DD}$, the output voltage level is higher than the input voltage level.

The authors [10] compared the behaviour of positive circuit design proposed with Dickson's charge pump and positive cross-coupled DC/DC converter using n-type TFT's, presented in figures 3.5 and 3.6.

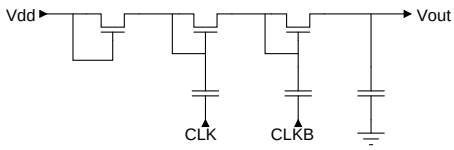


Figure 3.5: Dickson charge-pump [10]

With a supply voltage of 10 V and no load current, positive DC/DC converter presents an output voltage level of 25 V. On other hand, Dickson's charge pump presents 25.5 V and positive cross-coupled DC/DC converter presents 19.5 V.

With a load current of $250\mu A$, output voltage levels are 21.3 V, 20.4 V and 16.1 V respectively. In this case, the power efficiencies measured are 69.5%, 58.4% and 77.3%. The values show that Dickson's charge pump has a good output voltage level, but its efficiency is much lower than the other circuits. Cross-coupled DC/DC converter has good power efficiency, but its output voltage level is lower than the others. The authors explain this fact with low driving capability of n-type TFT's on source follower structure during pull-up.

The proposed positive DC/DC converter has also a better behaviour with load current. Its

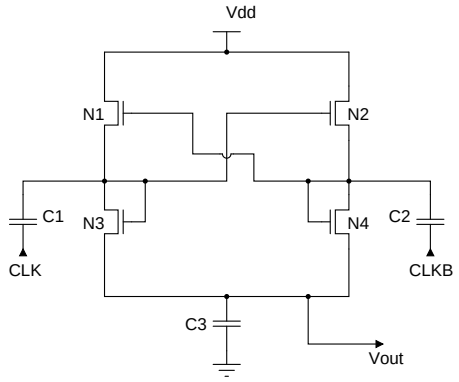


Figure 3.6: Cross-coupled DC/DC converter [10]

output voltage decreases less than others, and power efficiency approaches the values of cross-coupled design.

S. Hong et al. [10] also proposes a negative DC/DC Converter with six n-type IGZO TFT's, four pumping capacitors and one storage capacitor. The layout is presented on figure 3.7.

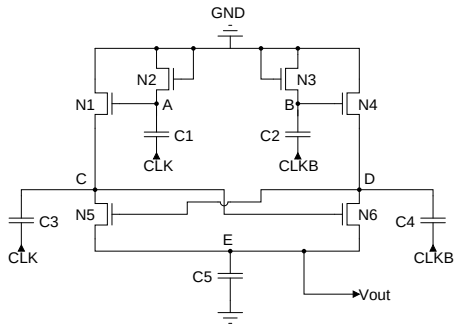


Figure 3.7: Transparent step-down DC/DC converter [10]

With $CLK = 1$, node C connects with the ground, so its voltage level is 0. The energy stored in capacitor C_4 turns the voltage level of node D to $-V_{DD}$. The output voltage level is $-V_{DD}$ because the transistor is turned on. As in positive converter, the same sequence happens in complementary nodes with $CLKB = 1$. So the output voltage, on ideal behaviour, will always be $-V_{DD}$.

The authors [10] compare the behaviours of negative circuit design proposed with Dickson's negative charge pump and negative cross-coupled DC/DC converter, shown in table 3.1.

	Cross-coupled DC/DC converter	Dickson's charge pump	Proposed DC/DC converter
Output Voltage (V)	-4.5	-3.8	-5.1
Power Efficiency (%)	47.1	45.2	56.1

Table 3.1: Simulated results of negative DC/DC converters with load current

The proposed negative DC/DC converter presents a lower output voltage level and better power efficiency. The results for both proposals suggests a good efficiency and constant output voltage, which allows an increasing knowledge on how to reduce undesired behaviours, such as parasitic capacitance and resistance.

3.2.2.2 DC/DC Converters in Organic Thin-Film Transistor Technology

H. Marien et al. [11] propose a DC/DC converter using organic thin-film transistors with a modified Dickson's charge pump. Organic technology only uses p-type transistors in contrast to transparent TFTs. The authors report some advantages of this technology, as the production at low-temperatures, reduced complexity and cost of the process. However, low mobility, transistor parameters variations and influence of oxygen and water, like transparent technology, are real limitations. The schematic is shown in figure 3.8.

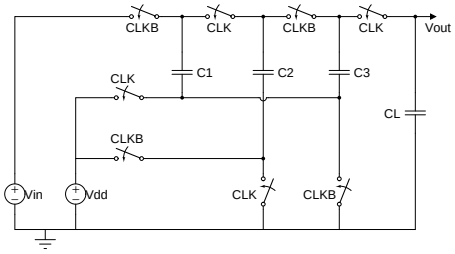


Figure 3.8: DC/DC converter design in organic technology [11]

The authors [11] describe the ideal output voltage with the following formula:

$$V_{out} = V_{in} + N(V_{dd} - \frac{I_{out}}{fC_D}) \tag{3.1}$$

N is the number of stages of charge pump, I_{out} is the output current, f is the clock frequency and C_D the capacitor value for each stage. Internal leakage current is estimated with and without $10\mu A$ load current by:

$$I_{int} = 10\mu A \frac{4V_{dd} - V_{out1}}{V_{out1} - V_{out2}} \tag{3.2}$$

where V_{out1} is the output voltage with $I_{out} = 0$ and V_{out2} is with a current of $10\mu A$ at the output. The power efficiency follows the equation:

$$\eta_{power} = \frac{10\mu A}{I_{int} + 10\mu A} \tag{3.3}$$

Simulation shows an output voltage level around 75 V with a voltage source of 25 V and no load current. With $10\mu A$ load current, output voltage is more than 10 V lower. It is very unstable, with a visible difference. Efficiency achieved is around 48%, which is relatively small. Authors in [11] explain it with leakage in capacitors. This proposal use a design based on Dickson's charge pump. It uses a large number of capacitors and transistors, increasing the problems referred in

chapter 2 with large use of these devices. Dickson's charge pump was compared with other topologies in [10] and [5], with worse results for the first one.

3.3 Regulators

To have a constant output voltage level at the output of the DC/DC converters, several regulation topologies have been presented. The regulation can be achieved by linear or pulse-width modulation. This section presents the state-of-the-art for regulation of DC/DC converters.

3.3.1 Linear Regulation

In 2009, K. Bhattacharyya et al. [12] presented a linear regulator with a differential pair amplifier and a current mirror configuration, to control the load current and reduce the voltage ripple of the DC/DC Converter designed. The schematic of the linear regulator amplifier is presented in figure 3.9.

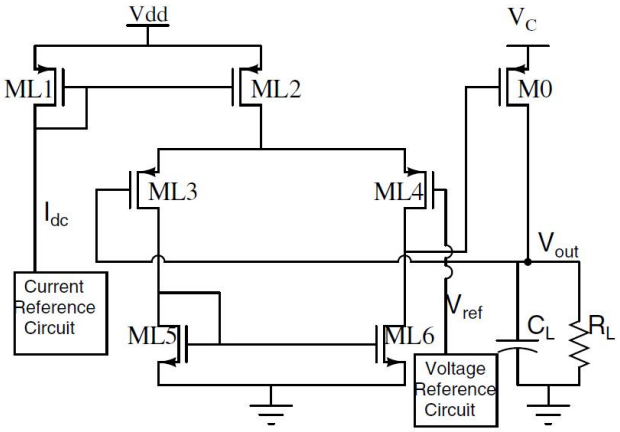


Figure 3.9: Proposal of linear regulator from Bhattacharyya et al.. Image obtained in [12]

It is used in the DC/DC converter configuration as shown in figure 3.10.

The current mirror introduce a reference current on the differential pair stage. The input voltages are applied on the p-type transistors. The n-type transistors are used to introduce the same current at the both sides of the differential pair, as a second current mirror. The differential pair compares the voltage received in the inputs, applying an output voltage as mentioned in last chapter.

In 2010, B. Maity et al. [13] designed a regulator with a push-pull structure for feedback loop, as presented in figure 3.11.

The output of the regulator is applied to the input of the DC/DC converter. A dual push-pool is introduced to increase the bandwidth and to have faster response during transient. The configuration is presented in figure 3.12.

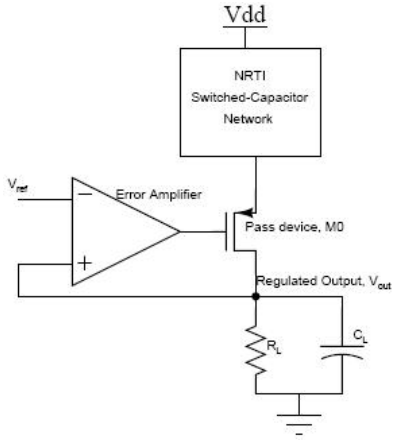


Figure 3.10: Schematic of regulation from Bhattacharyya et al. [12]. Image obtained from [12]

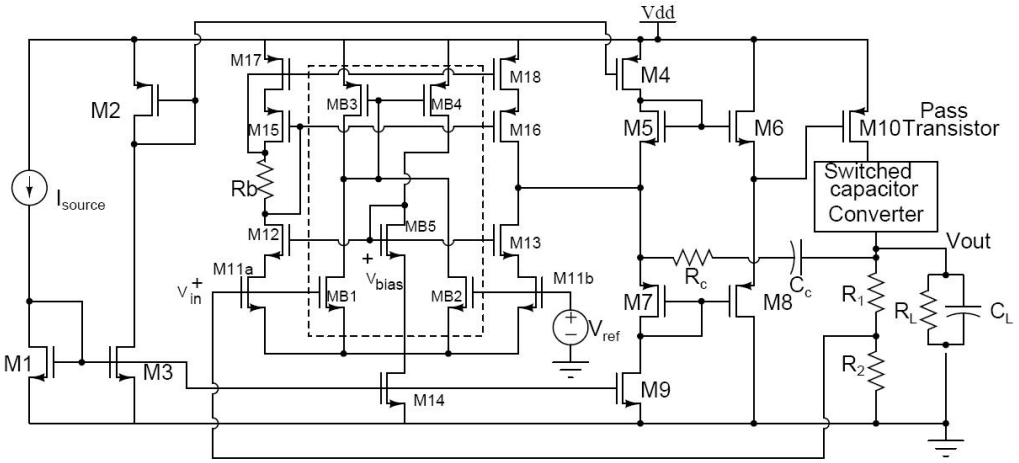


Figure 3.11: Proposal of linear regulator from B. Maity et al. [13]. Image obtained from [13]

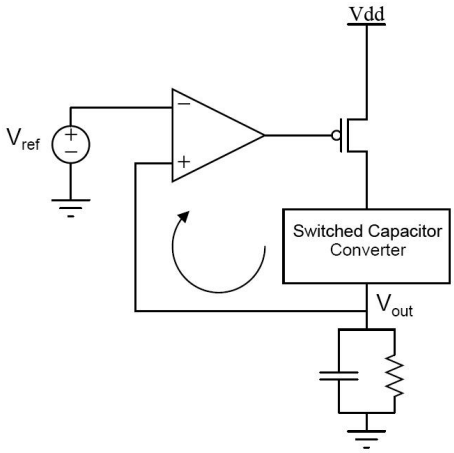


Figure 3.12: Schematic diagram of regulation from B. Maity et al. [13]. Image obtained from [13]

The frequency stability of the amplifier is ensured with a RC compensation to increase the frequency stability, that would decrease by the influence of three poles, the one at the output of the error amplifier, the one at the input of the pass transistor and the one associated to the load, with a value of $1/R_C C_C$. The comparison is made with two differential pairs, one of them with a telescopic cascode stage to increase gain. Results show a peak output voltage of 117% of the steady state voltage and a dip voltage of 81.4% of the stead-state.

In 2011, Maity et al. [14] added a differential current starved inverter to have good levels of efficiency independent of the load current required. The inverter changes the levels of frequency depending of the current that goes through each side. The inverter controls the voltage control oscillator to give a lower frequency with lower load currents, reducing the switching losses. The schematic of the inverter and the circuit where it is used is presented in figure 3.13.

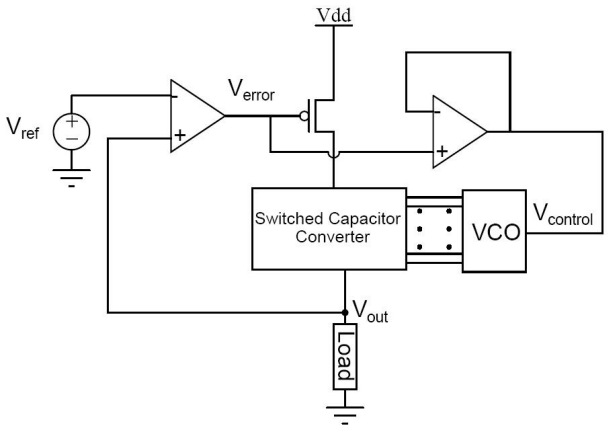


Figure 3.13: Schematic diagram of regulation with inverter from B. Maity et al. [14]. Image obtained from [14]

The results reported introduce a larger range of load current that can be applied, due to the optimization of the circuit to the changes of this parameter. Without the inverter, the output voltage level of the circuit has a large decrease above 25mA of load current. With the inverter, the output voltage becomes more stable even with an increasing load current.

3.3.2 Pulse-Width Modulation

The pulse-width modulation (PWM) is another technique to regulate the output of DC/DC converters. This technique was used by several authors not only for the regulation of the output voltage and compensation to have the desired voltage level, but for the stability of the voltage multipliers against load variations as well. Although the various authors use different voltage multiplier topologies, the main idea behind the PWM regulation is basically the same. In figure 3.14, it is presented the configuration of PWM controller presented by Y. Chang [15].

The load current of the charge-pump enters in a low-pass filter (LPF) to the high-frequencies rejection. Then, the current is compared with I_{ref} using a high-gain amplifier, in order to have the

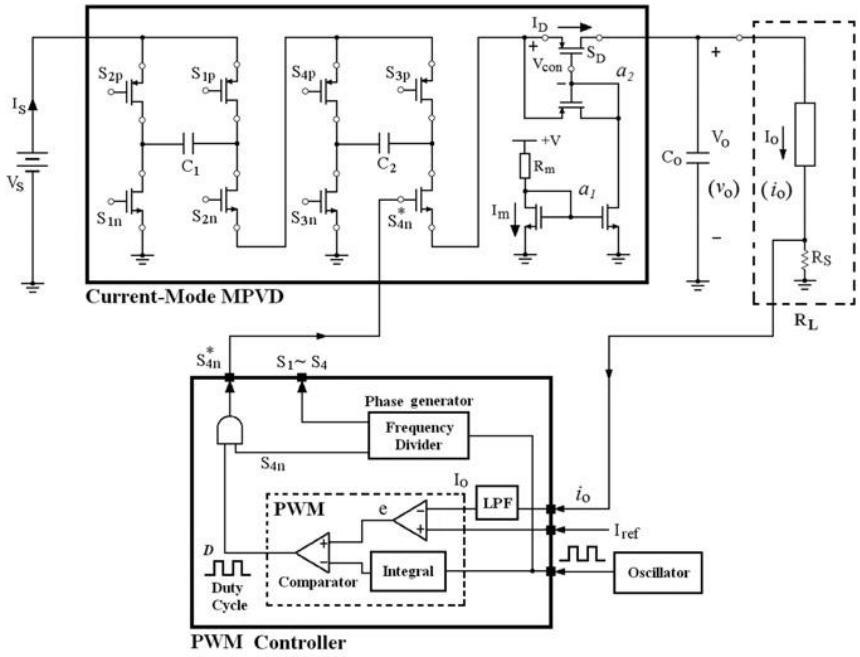


Figure 3.14: Configuration of charge-pump with PWM regulation proposed by Y. Chang [15]. Image obtained from [15]

same current at the output of the charge-pump. Therefore, a comparator is used to produce the necessary duty-cycle by a pulsed wave oscillator. The duty-cycle is divided in different phases by a frequency divider, to use the correspondent duty cycle in transistors S_1 to S_4. The results obtained present a lower ripple with the PWM regulation, 0.276% instead of the 0.4% without PWM.

Other authors from earlier studies [33] and the same in further reports [34] use the output voltage for comparison instead of the current. Usually, with PWM technique is achieved better results than with linear regulation, due to its precision in controlling the duty-cycle of DC/DC converters, changing the time of charge and discharge of the boosting capacitors, which is a very initial stage of the boosting process.

3.4 Critical Analysis

Analysing the improve of DC/DC converters using the charge-pump structure, it can be concluded that since the Cockcroft-Walton multiplier configuration [3] there was a concern of improving parameters such as the parasitic capacitance and the power efficiency. The changes made by Favrat [7] with the cross-connected configuration is one of the techniques used to reduce the overlapping of clock stages, which could increase the voltage ripple at the output and the efficiency. Another important improve made is the usage of bootstrapping topology, that reduce the short switching losses and where the transistors of smaller width can be used, due to the bootstrapping circuit it is not in the main path of the configuration.

Hong et al. [10] prevented the parasitic capacitances with another technique of separation between two boosting stages, which does not apply to a large difference of voltage in diode connected transistors.

In regulation, the efforts have been made to increase the gain of the amplifier, to have a more constant regulated voltage level. Thus, the number of amplifier stages are increased, which decreases its frequency stability. With the compensation technique, the phase margin can have values into a good stability. Another possibility is the usage of PWM regulation, which controls the duty-cycle applied to the DC/DC converter after a comparison of output and reference voltage or current.

3.5 Conclusion for the Proposal

The bibliographic review was very helpful to know and define the techniques used to improve a DC/DC converter using switched capacitors. For the creation of the new proposal presented in this report, these articles reviewed represented the initial step.

Various techniques presented in this chapter for the DC/DC converter, such as the bootstrapping configuration, the separation of different boosting stages and the cross-connected transistors can be used to have a better response of the DC/DC converter in terms of output voltage. However, the major concern using the transparent technology is the parasitic resistance of the transistors, which reduce the voltage as many transistors are used in the main path. As referred in the state-of-the-art of the transparent TFT, the latest reports suggest better results with the top-gate structure, which is not used in CENIMAT, and that can reduce the performance of the proposed topology. Some configurations presented used p-type transistors, but they can be well-substituted by n-type changing the nodes which the gates are connected.

Regarding the regulation, it was presented some topologies of regulator amplifiers, but there was not any proposal with transparent electronics. This is a major difference, due to the non-existing transparent p-type TFT's. This fact changes the standard view of amplifier stages, and influence the intrinsic parameters and behaviour of the amplifier.

Chapter 4

Proposed Configuration

The circuit proposed in this chapter intends to achieve the objectives for this dissertation, in order to have a topology using transparent electronics that has at the output a voltage level as higher as possible than the input voltage level, in direct current and as stable as possible. To achieve that, it was studied and designed the DC/DC converter with better performance in terms of output voltage level, ripple, efficiency and stability with load currents.

In chapter 2, it was mentioned that standard DC/DC converters use inductors to boost the voltage level. In order to explain how the inductors are problematic in transparent electronics, it was tested in a simulator the behaviour of this device with the conductivity of a transparent conductor. The parameters used to simulated the inductor are presented in 4.1.

Distance between turns	$40\mu m$
Number of turns	5
Path width	$15\mu m$
Thickness	$2\mu m$
Radius	$200\mu m$

Table 4.1: Parameters of the inductor simulated

The results of inductance and quality factor for the inductance simulated are presented in figures 4.1 and 4.2.

The figures obtained suggest a very low quality factor of 0.001 and a negative inductance for a frequency of 1MHz, which results in a non-inductive but capacitive response. Therefore, the proposed DC/DC converter with transparent electronics use switched-capacitors instead of inductors to increase the voltage level.

Besides the configuration of the DC/DC converter, it was also designed a regulator to get a better response of the output voltage with lower values of ripple, which increases the stability of the voltage level even with variations of load parameters.

This chapter presents the configuration of DC/DC converter and regulation with the transparent electronics developed. It has 3 sections, the first one about the DC/DC converter itself, the second

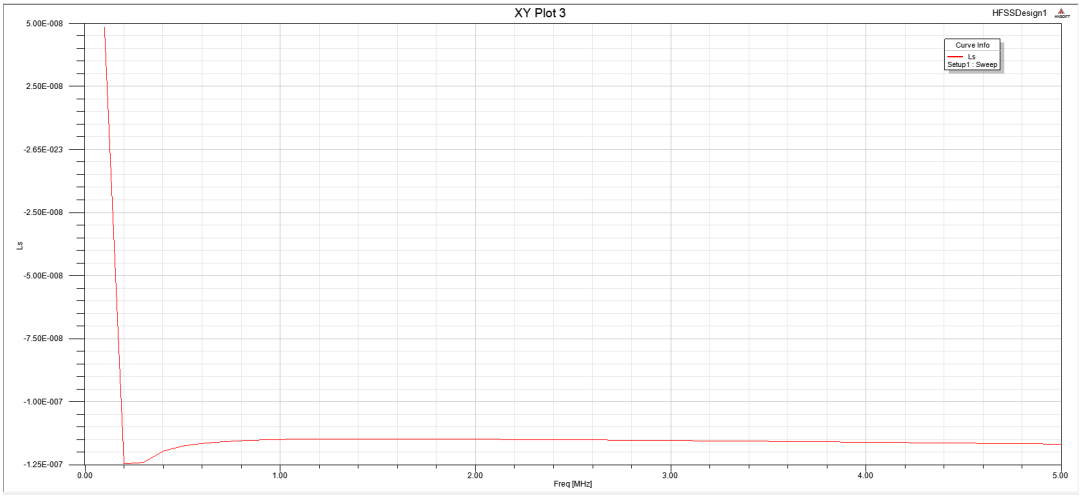


Figure 4.1: Inductance response depending of frequency

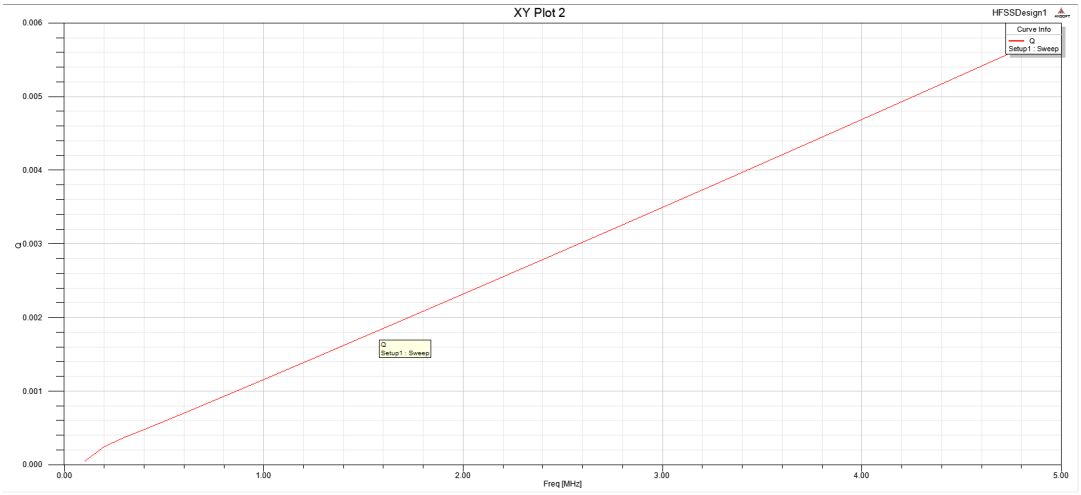


Figure 4.2: Quality factor depending of frequency

about the amplifier and the third about the regulator.

4.1 DC/DC converter

4.1.1 Design

Various techniques to improve the parameters of the DC/DC converters have been studied. For the configuration developed some of them were used. Basically, it was used a combination of the improves made by Y. Allasasmeh and S. Gragori [8] with the bootstrapping stage for voltage multipliers, which prevents short-circuit losses, and the improves from S. Hong et al. [10], with the voltage boosting stages to increase the output voltage and the separation between stages to

reduce clock feedthrough effects by the parasitic capacitances and stabilize the voltage level at the output of each stage. The schematic of the final proposal is presented in figure 4.3.

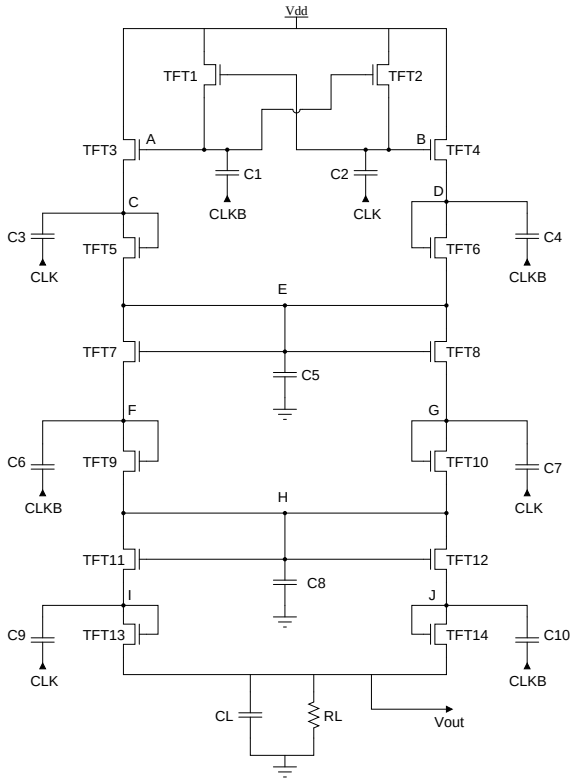


Figure 4.3: Proposal of DC/DC converter

At the initial stage, a bootstrapping configuration was employed to prevent the short-circuit losses by controlling the switching stages. When CLKB is on, TFT3 and TFT2 are on, so C2 is charging. The charge introduced in C1 in the previous half-clock cycle creates a voltage of V_{DD} in the terminals of this capacitor. By addition of the clock signal, the voltage applied to the gate of the TFT3 is $2V_{DD}$, and it is created a path between V_{DD} and node C, charging the capacitor C3. The complementary transitions applied to the TFT's enables a good separation of switching times. It increases the power efficiency due to the lower power losses. The cross-connected transistors also help on these parameters.

The clock signals were applied directly to the boosting capacitors, in order to increase the voltage level at the node C and D by addition of the charge from V_{DD}, saved in the capacitor, and the charge from the clock signal. The diode-connected TFT5 and TFT6 enable a transfer of charge from the node C/D to E when the voltage at C or D is $2V_{DD}$.

A separation stage was designed to prevent a high parasitic capacitance associated to the TFT5 and TFT6, which could exist with a large voltage difference between source and gate. This separation, although their voltage decrease in the diode-connected transistor, decrease the switching losses and parasitic capacitances. If this stage would not exist, node F/G would be the same as node E, so when the clock signal were applied to the capacitor C6/7, the voltage at node E would

be very high, causing a high difference of voltage level between source and gate of transistor TFT5/6. Two more boosting stages and one separation stage were designed to increase the output voltage level.

In a way to reduce the on-resistance of the TFT's, were designed four transistor of $320\mu m$ in parallel for each diode or switch connection, except on the bootstrapping stage in TFT1 and TFT2, because they are not in the main path between the input and the output. The overall resistance of the DC/DC converter only considers the main path of the circuit between input and output. A high TFT on-resistance decreases the voltage level between drain and source, and can increase the time response of the circuit, by an increasing time constant RC. Thus, the boosting capacitors does not have enough time to charge, resulting in a lower output voltage level. However, the large TFT's used can increase the parasitic capacitances associated and the charge injection effect, and the efficiency drops.

The sizing of the boosting capacitances was made by analysing the time constant, ripple and load current. The size of each capacitor is presented in table 4.2.

Capacitor	C1 and C2	C3 and C4	C5 and C8	C6 and C7	C9 and C10
Size (pF)	100	200	100	400	500

Table 4.2: Sizing of the capacitors for the proposed DC/DC converter

The amplifier created for regulation needs around $100\mu A$ of current, so the DC/DC converter should present a load current of $200\mu A$ if the case of using the DC/DC converter connected to other circuits is considered. The ripple voltage on a boosting stage can be calculated by R. Perigny [27] analysis:

$$\Delta V = \frac{I_o}{2 f_{clk} C_a} \tag{4.1}$$

With a switching frequency of 1MHZ, for a 100pF boosting capacitor, the voltage ripple is 1 V. With 500pF, it is 0.2 V. The output voltage depends of boosting capacitance C_b in each stage by replacing V_{high} and V_{low} calculated in the analysis by R. Perigny [27]:

$$V_{out} = 2V_{DD} - \frac{I_o}{2 f_{clk} C_b} + \frac{I_o}{2 f_{clk} (C_b + C_{load})} \tag{4.2}$$

Analysing the equation, if a load capacitance is used, the output voltage has reasonable values with boosting capacitances above 50pF. The capacitors should not be very large to not exceed area constrains, so depending on the efficiency, time response and ripple voltage desired, the values of capacitance are chosen. Another detail to be considered is the level of approximation to the output. If the larger capacitors are closer to the output, the ripple is lower with the correction of ripple created by the initial stages. This fact explains the different values of boosting capacitors for the proposal designed.

The load devices are designed depending of output voltage, current and frequency used. If the DC/DC converter returns 16 V at the output, to achieve a current of 200μ it is necessary a load resistor of $100k\Omega$. The load capacitor is used to reduce the ripple by the last equation.

To estimate the expression of the output voltage for the designed configuration, there is considered also the voltage drop in the transistors due to their on-resistance considered by B. Razavi [2]. There are 6 TFT in the main path between V_{DD} and V_{out}, so the overall expression is:

$$V_{out} = 4V_{DD} - 3[\frac{I_o}{2f_{clk}C_b} - \frac{I_o}{2f_{clk}(C_b + C_{load})}] - 6[V_{th} + \frac{1}{\frac{1}{2}\mu_n \frac{C_G}{C_H}\frac{W}{L}\frac{1}{f_{CLK}} + \frac{1}{V_{DD}-V_{th}}}] \tag{4.3}$$

This expression explains the usage of 4 large TFT in parallel at each transistor designed in the main path. As larger the transistor is, lower is the voltage drop across it. The expression also suggests better results if there are used DC/DC converters in parallel, due to the lower equivalent resistance of the block.

The layout of the single DC/DC converter is presented in figure 4.4.

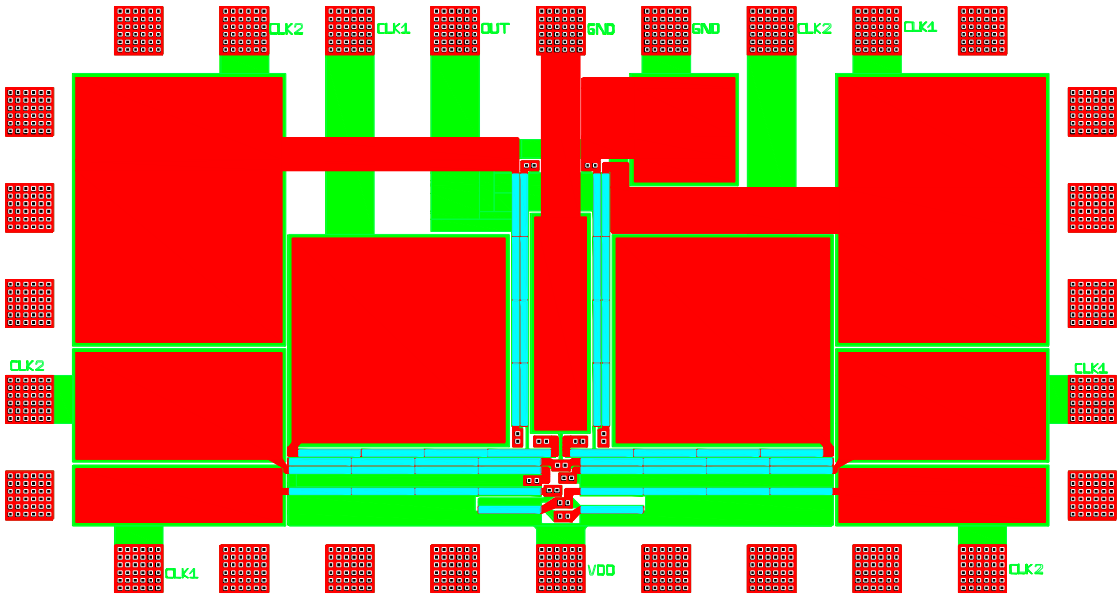


Figure 4.4: Designed layout of the single DC/DC converter

The red colour represent the gate material, which last reports of fabrication refer the usage of Indium Tin Oxide (ITO). The green colour represent the source/drain material, which Ti/Au

is commonly used. The blue colour represent the semi-conductor of the TFT (a-IGZO). The squares pads and rectangular vias use small squared metal inside, which is represented in white. To calculate the area of the capacitors, it was used a value of relative dielectric permittivity of 10.5 and a dielectric thickness of 275nm. For the designed values of capacitance, the area obtained is presented in table 4.3.

Capacitance values	Area (μm^2)	Capacitor associated
500pF	1.479	C9 and C10
400pf	1.183	C6 and C7
200pF	0.5916	C3 and C4
100pF	0.2958	C1, C2, C5 and C8

Table 4.3: Area of each capacitor designed

To get a lower parasitic resistance associated, wider connections were designed and with as many as possible source-drain material (Ti/Au), which has better parasitic parameters in comparison to gate material (ITO). There was also the concern to avoid the usage of a large number of vias, which can increase the parasitic capacitances. About the behaviour of the circuit, a trade-off exists between the area used and the parasitic parameters associated. However, a small-sized and efficient circuit can be obtained if the overlap between the 2 materials is avoided and the distances of the connections are not so large. The load capacitor and resistor were not designed in the layout due to external testing with PCB. The designed layout of the single DC/DC converter has 5793.55μm of length and 3058.55μm of width.

4.1.2 Simulation

Using the verilog-A TFT model for simulation, the topology presented has an output voltage of 16.37 V with 10 V of V_{DD} and clock voltage, and 162uA of load current. The frequency used is 1 MHz. The plot of the increasing voltage during the time is presented in figure 4.5.

Comparing with the simulation of the same topology with NMOS, which has 23.17V and 203μA at the output, the simulation with TFT's have lower output voltage due to the higher on-resistance of the transistors.

Using the TFT model of simulation, the bootstrapping stage on the single DC/DC converter represents an increment of only 0.04V, but the circuit is faster to achieve the final voltage level. This fact is very important for a fast start of the amplifier, which expects a high supply voltage. The comparison of the output voltage response with and without the bootstrapping stage is presented in figure 4.6.

The additional stage designed at the output represents an increment of 2.9V for the simulation with the NMOS. However, with the TFT's simulation, that only represents an increasing of 0.6V. Despite the low increasing, the second stage was used due to a necessary high voltage in the

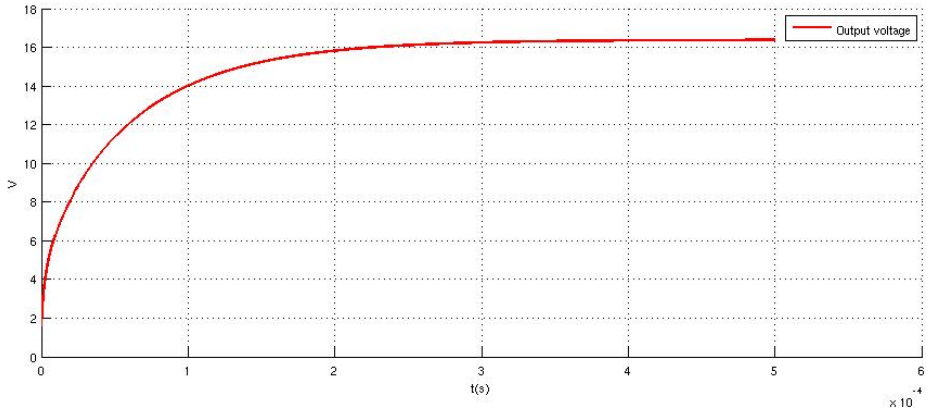


Figure 4.5: Output voltage of the single DC/DC converter during the time

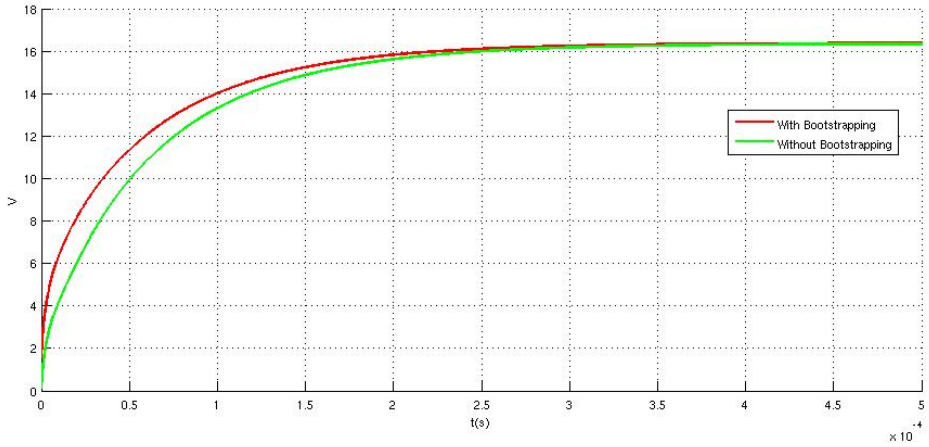


Figure 4.6: Comparison of output voltage during the time with and without bootstrapping stage

input of the regulator, and there are better results when this stage is used with more converters in parallel. In fact, to have a higher output voltage, it was used the same topology repeated 10 times in parallel, which will be explained later.

The results of the simulation with the TFT model for the proposed single DC/DC converter with different values of load resistance are presented in table 4.4.

Load resistance	$60k\Omega$	$80k\Omega$	$100k\Omega$	$120k\Omega$	$140k\Omega$
Output voltage	$13.43V$	$15.1V$	$16.37V$	$17.39V$	$18.24V$
Load current	$223.2\mu A$	$188\mu A$	$165.5\mu A$	$145\mu A$	130μ

Table 4.4: Output voltage and current for different values of load resistance for the proposed DC/DC converter

Analysing the table, as the load resistance is, the higher is the load current and voltage. The load current has a huge impact on DC/DC converter output voltage.

Another important parameter to refer is the dimensions of the transistors. As explained before, four TFTs of $320\mu m$ in parallel were designed to reduce the on-resistance, with exception of the bootstrapping stage. The voltage level simulated without the designed transistors in parallel, so just one transistor of $320\mu m$ in each position, is 8.42V and the correspondent load current is $84.7\mu A$, values much lower than with the final transistors.

The dimensions of the capacitors change the voltage level and ripple at the output of the DC/DC converter. For the simulation of such changes, the DC/DC converter was tested only with 100pF capacitors. The output voltage is 16.25V, lower than before, and the ripple is higher, around 5mV, comparing with the $860\mu V$ of the final proposal.

The circuit proposed use 10 DC/DC converters in parallel to increase the voltage level and the load current. The increasing voltage during the time is presented in figure 4.7.

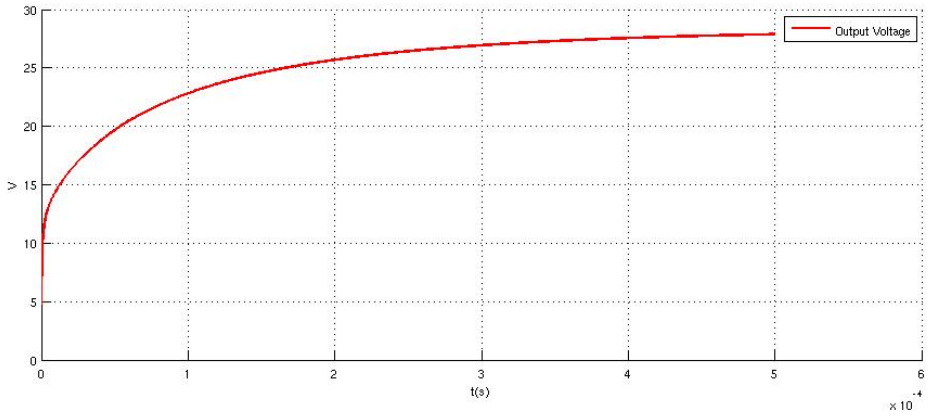


Figure 4.7: Output voltage of 10 DC/DC converter in parallel during the time

Output voltage is 27.8V and the current is $277\mu A$ with the same load devices. By comparison, ten converters without the last boosting stage have an output voltage of 20.05V, which is not enough to feed the regulator with a 24V expected. Notice that, although the difference of output voltage for one converter is not so large, for ten converters in parallel it is larger than 4 V. This fact is explained by the reduction of the equivalent resistance of the converter block. The resistance of each DC/DC converter is higher than the overall equivalent resistance, so the additional stage does not represent an increase of this parameter in all the circuit as much as with only one converter.

4.2 Amplifier

4.2.1 Design

The regulation is achieved with a high-gain amplifier using a differential pair with a positive feedback at the load, to increase the voltage gain. The amplifier was designed to receive a supply

voltage V_{DD} of 24V from the output of DC/DC converters. The final proposal for the amplifier is presented in figure 4.8.

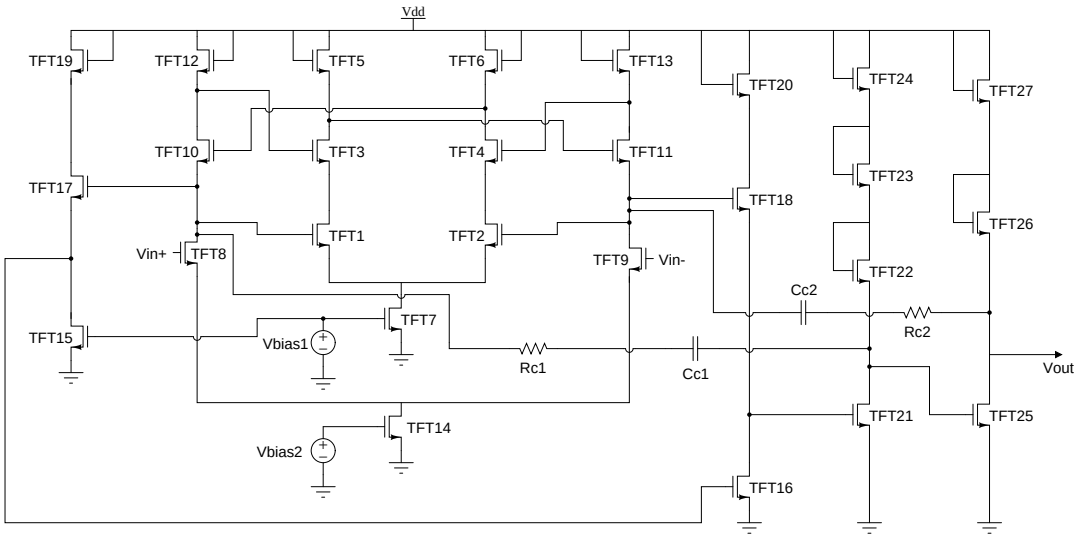


Figure 4.8: Proposal of regulator

The differential pair is the stage that compares the two input voltages for the regulation of the output. Additionally, two source followers were added to decrease the output resistance, and two common-source stages to increase the gain.

The positive feedback connected to the differential pair is used to increase the gain by increasing the load resistance. Due to the difficulty that exists with the lack of p-type transistor in increasing the load resistance to achieve a high gain, positive feedback can be used as with TFT1 to TFT6 presented in figure, which equivalent load resistance is found to be:

$$R_L = r_{o2} || \frac{1}{g_{m2}(1 - A_f)} \tag{4.4}$$

where A_f is the feedback gain. Therefore, the voltage gain of the common-source stage is:

$$A_v = -g_{m1}[\frac{1}{g_{m2}(1 - A_f)} || r_{o2} || r_{o1}] \tag{4.5}$$

With a feedback gain close to 1, the voltage gain is approximately $-g_{m1}(r_{o1}||r_{o2})$. With a feedback gain higher than 1, instability is created in the amplifier, which is undesirable. The feedback gain in the proposal presented is calculated by:

$$A_f = g_{m2}(\frac{1}{g_{m6}} || r_{o6} || r_{o2}) \tag{4.6}$$

Theoretically, the gain A_f is 0.8572. A higher feedback gain could increase the overall gain, but if in theory the feedback had a gain very close to 1, due to errors in fabrication, the maximum value could be exceeded, just with some difference on TFT's width.

The topology proposed of positive feedback uses a cascode stage instead of common-source, due to a high V_{DD} expected. Three TFT's in this stage decreases the V_{DS} and the V_{GS} applied in each transistor, which enables a efficient operation of transparent TFT's. Notice that the values of V_{GS} should be between 5 and 7 Volts, to prevent lower or higher levels of voltage applied to the TFT than those that are expected by analysis of the background.

The dimensions of the transistors for feedback topology are presented in the table 4.5.

	Width	Length
TFT 1 and 2	$75\mu m$	$20\mu m$
TFT 3 and 4	$75\mu m$	$20\mu m$
TFT 5 and 6	$80\mu m$	$20\mu m$
TFT 7	$160\mu m$	$20\mu m$

Table 4.5: Dimensions of TFT for the feedback stage

In the differential pair, a diode-connected transistor is used, that in addition to the decrease of voltage applied in the transistor, which was explained before, it increases the voltage gain due to a higher load resistance. Therefore, the voltage gain of the differential pair with the feedback stage is:

$$A_v = -g_{m8}[(\frac{1}{g_{m12}}||r_{o12}) + (\frac{1}{g_{m10}(1-A_f)}||r_{o10})||r_{o8}] \tag{4.7}$$

The dimensions of the transistors take into account two factors, the need to have all transistors in saturation and the voltage gain, by increasing the load resistance using narrow dimensions on TFT's 10, 11, 12 and 13. The dimensions used are presented in table 4.6.

	Width	Length
TFT 8 and 9	$80\mu m$	$20\mu m$
TFT 10 and 11	$80\mu m$	$20\mu m$
TFT 12 and 13	$160\mu m$	$20\mu m$
TFT 14	$160\mu m$	$20\mu m$

Table 4.6: Dimensions of TFT for the differential pair

The high impedance and the high output voltage level of the differential pair is decreased by using a source-follower stage. Despite its unitary gain, it is very useful for the addition of the two out-of-phase input signal voltages. Notice that the TFT16, to be in saturation, needs a low gate voltage due to the low voltage applied to the drain. It is also important to refer that the TFT15 receives a bias voltage at the gate instead of being connect directly to the gate of TFT16, which could create a negative gain at this stage. If the gate and drain of TFT15 were connected, the source resistance would be $1/g_{m15}$, resulting in a very low source resistance applied to the source-follower. That would decrease the value of $g_{m17}R_s$, which should be much higher than one to do not result in a negative gain.

The voltage gain of the source-follower stages and the common source applied to TFT16 is:

$$A_{vSF17} = \frac{g_{m17}[[(\frac{1}{g_{m17}}||r_{o17}) + (\frac{1}{g_{m15}}||r_{o15})]||r_{o15}]}{1 + g_{m17}[[(\frac{1}{g_{m17}}||r_{o17}) + (\frac{1}{g_{m15}}||r_{o15})]||r_{o15}]} \tag{4.8}$$

$$A_{vSF18} = \frac{g_{m18}[[(\frac{1}{g_{m18}}||r_{o18}) + (\frac{1}{g_{m20}}||r_{o20})]||r_{o16}]}{1 + g_{m18}[[(\frac{1}{g_{m18}}||r_{o18}) + (\frac{1}{g_{m20}}||r_{o20})]||r_{o16}]} \tag{4.9}$$

$$A_{vCS16} = g_{m16}[[(\frac{1}{g_{m18}}||r_{o18}) + (\frac{1}{g_{m20}}||r_{o20})]||r_{o16}] \tag{4.10}$$

The dimensions of the TFT are presented in the table 4.7.

	Width	Length
TFT 15 and 16	$80\mu m$	$20\mu m$
TFT 17 and 18	$80\mu m$	$20\mu m$
TFT 19 and 20	$80\mu m$	$20\mu m$

Table 4.7: Dimensions of TFT for the source-follower stages

In order to increase the voltage gain of the amplifier, two common-source stages were designed at the output. It was used diode-connected TFT's for the same reasons explained with the differential pair, increasing the gain and decreasing V_{GS}. The transistors that determine the load resistance should be as narrow as possible, to get lower values of g_m. The load transistors use the same width, so the voltage gain of each stage can be calculated as:

$$Av_{CStft21} = -g_{m21}[\frac{3}{g_{m22}}] \tag{4.11}$$

$$Av_{CStft25} = -g_{m25}[\frac{2}{g_{m26}}] \tag{4.12}$$

The dimensions of the transistors are presented in table 4.8.

	Width	Length
TFT 21 and 25	$80\mu m$	$20\mu m$
TFT 22, 23 and 24	$70\mu m$	$20\mu m$
TFT 26 and 27	$50\mu m$	$20\mu m$

Table 4.8: Dimensions of TFT for the common-source stages

The voltage gain of the amplifier can be estimated by analysis of each stage and then for all. Notice that the voltage gain of the source-follower stages is around 1. Therefore, the voltage gain

for the amplifier is estimated as:

$$A_{vop-amp} = -g_{m9}[(\frac{1}{g_{m13}}||r_{o13}) + (\frac{1}{g_{m11}(1-A_f)}||r_{o11})||r_{o9}][-g_{m21}(\frac{3}{g_{m22}})][-g_{m25}(\frac{2}{g_{m26}})] \quad (4.13)$$

In order to achieve a high phase-margin, frequency compensation is needed. To determine how to use the compensation technique, it is estimated the node where the dominant pole is located. Due to the positive feedback stage, which creates a very high load resistance, the impedance at the output node of the differential pair is very high, creating the dominant pole. A capacitor connected to this node move it into the lower frequencies, increasing the phase margin.

For an efficient compensation, the capacitor should be high to ensure that the pole is at lower frequencies. With a multi-stage amplifier, it is possible to use the properties of the Miller effect to have a high capacitance associated to the node without using a large capacitor, which would increase the necessary area of the circuit.

In addition to the effect of a dominant pole in the phase margin, there is also the effect of a zero. The zero is created by the signal path between the compensation capacitor nodes. This zero degrades the phase margin because is located at the right side of the S plane, creating a decrease of phase at lower frequencies. It also slows down the decreasing curve of the magnitude, moving the point of zero magnitude into higher frequencies. These two facts are responsible to the degradation of the phase margin and the stability. The technique used to eliminate the zero effect is by the additional resistor R_c added. The zero introduced by the compensation is:

$$w_z = \frac{1}{C_c(\frac{1}{g_{m18}} - R_c)} \quad (4.14)$$

With a $R_c \geq 1/g_{m18}$, $w_z \leq 0$, the resistance should be higher enough so to move the zero to the left half plane and cancel the first non-dominant pole, if possible. By an iterative mode, the resistance and capacitance value were obtained when the phase margin ensured a good stability of the amplifier.

For the layout design, the same care was considered as it was for the DC/DC converter. However, this circuit is pad-limited, the large number of pads determines the area that can be used. The layout of the proposed regulator amplifier is presented in figure 4.9.

The layout designed does not have the compensation resistors and capacitors, due to a following testing of those values using the PCB. The dimensions of the designed layout are $2383.8\mu m$ on the vertical axis of the figure presented and $2450\mu m$ at the horizontal axis.

4.2.2 Simulation

For the simulation of the amplifier, it was considered parasitic capacitances with values of $C_{GD} = 1pF$ and $C_{GS} = 5pF$. The voltage gain of the amplifier is 36.7dB and the phase margin is 83.79 degrees. The plot of voltage gain and phase is presented in figures 4.10 and 4.11.

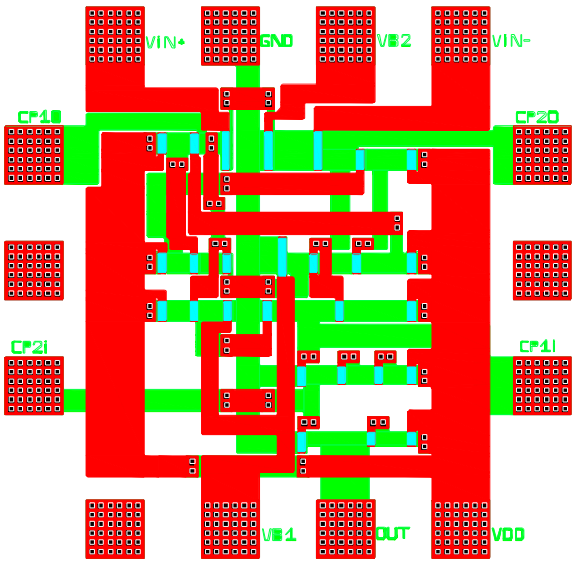


Figure 4.9: Designed layout of the proposed regulator amplifier

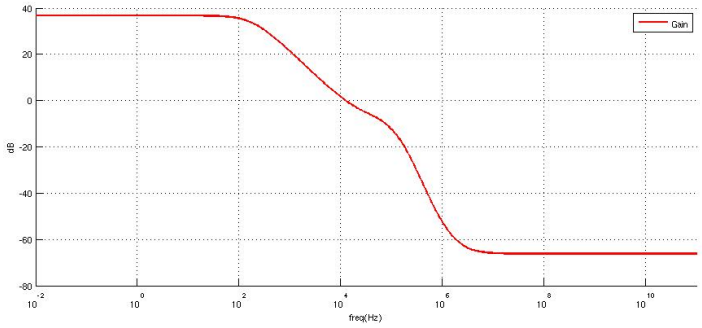


Figure 4.10: Voltage gain of the amplifier for a logarithmic frequency scale

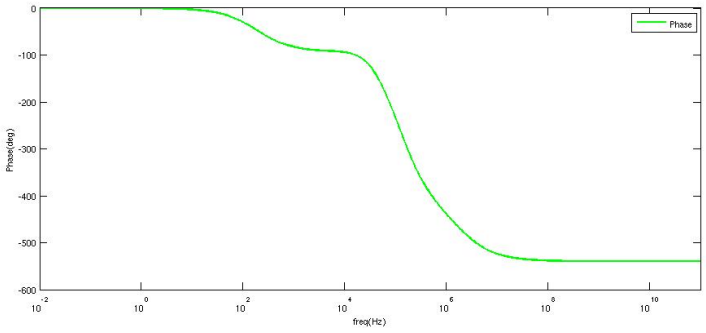


Figure 4.11: Phase response of the amplifier for a logarithmic frequency scale

The voltage gain for each stage is presented in table 4.9. With compensation, the phase margin increased to 131.31 degrees.

Stage	Voltage gain (dB)
Positive feedback	-1.3
Differential pair	23.34
Source-follower	-0.156
1st Common-Source	4.85
2nd Common-Source	6.19
3rd Common-Source	8.5

Table 4.9: Voltage gain for each stage of the amplifier

4.3 Regulator

The DC/DC converter and regulator are connected to achieve lower ripple at the output. The schematic of the final circuit is presented in figure 4.12.

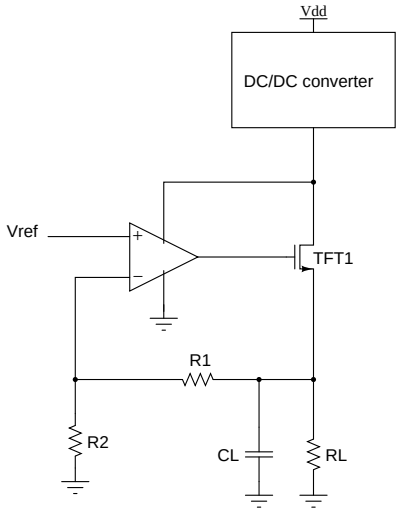


Figure 4.12: Final circuit

A transistor of 320μ at the output of the amplifier controls the current to the load depending on the voltage level applied to the gate. The resistors R1 and R2 are chosen according to the expected regulated voltage, according to:

$$V_{out} = (1 + \frac{R_1}{R_2})V_{ref} \tag{4.15}$$

Both resistors used have a value of $100k\Omega$.

For simulation, it was designed at the load an ideal switch with a 10V clock voltage with a period of 500μ connected to a resistor of $100k\Omega$ for testing the ripple behaviour and comparison between regulated and non-regulated voltage with changes in the load resistance. Therefore, because R_L has a value of $100k\Omega$ and C_L has a value of $1nF$, the load resistance has a variation between $100k\Omega$ and $200k\Omega$ depending of the position of the switch. The reference voltage level V_{ref} used is 10V. It is important to refer that in simulation it was used a NMOS instead of a TFT, due to convergence problems with the TFT model when the DC/DC converters and the regulator were simulated together. However, it is not expected to have a large difference in experimental analysis with this fact, because the transistor is only used to pass up more or less current depending on the output voltage of the amplifier. Nevertheless, the TFT main issues are not without significance, such us the threshold voltage shift, that should have a large influence in a TFT with this function. The output voltages during time are presented in figure 4.13.

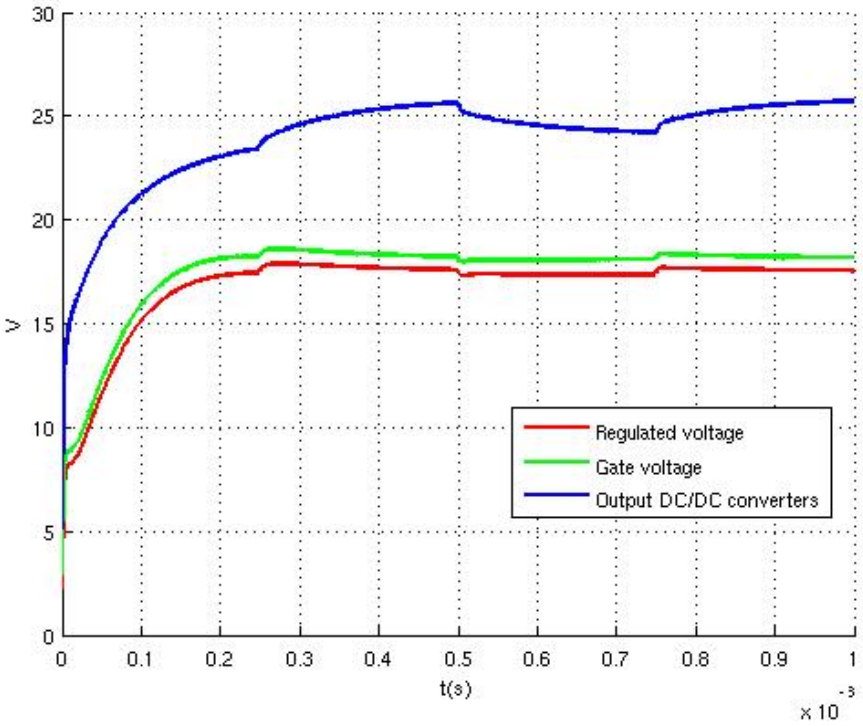


Figure 4.13: Voltage level during the time for different nodes of the circuit

The voltage levels at each node of the circuit are presented in table 4.10.

The circuit proposed presents an output voltage level of 17.65V in direct current with a V_{DD} of 10V. Comparing the ripple voltage for the output of DC/DC converters node and the regulated voltage node, it is easy to analyse from figure 4.13 that the regulated voltage has much lower ripple. In fact, the higher voltage of the first node is 25.7V and the lowest is 24.19V, in opposition to the higher voltage of 17.68V and the lower of 17.37V for the second node. The ripple of the regulated voltage is 80% lower than in the output of DC/DC converters.

Node	Voltage level (V)
DC/DC converters output	24.5
Voltage applied to the gate	18.34
Regulated voltage	17.65

Table 4.10: Voltage level for each node of the circuit

It is important to refer that the voltage level of the DC/DC converters output is lower than the level presented without the regulation, due to an increase of the load resistance, the lower gain of the amplifier and the on-resistance of the transistor used. The amplifier added to the circuit needs a current of $178.86\mu A$, which results in a decreasing of the voltage level at DC/DC converters output. Thus, this level is around 24V, which makes it able to supply the amplifier designed to receive that voltage.

To simulate with a TFT transistor at the output of the amplifier and verify if it in fact works, it was necessary to use a DC voltage source of 25V instead of the DC/DC converter. The results of voltage levels for this simulation are presented in figure 4.14.

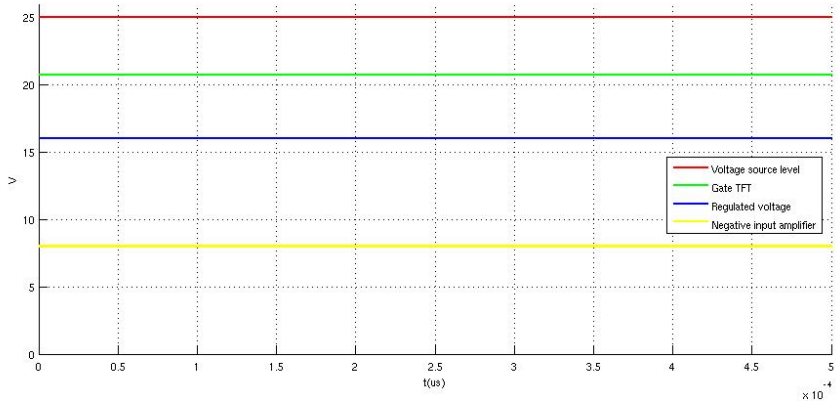


Figure 4.14: Results for the simulation with voltage source

The regulated voltage for this simulation is 16.05V, with 20.76V at the gate of the TFT. This voltage drop is also explained with the low gain of the amplifier and the high on-resistance of the TFTs. In fact, to reduce this on-resistance, 4 TFTs were placed in parallel. With a single TFT, the regulated voltage level would be smaller. The current through these TFT is 168.45μ. With this simulation is not possible to measure the difference on the voltage ripple, because the ideal voltage source does not create that ripple in opposition to DC/DC converters. This simulation was created due to convergence problems with the analysis of DC/DC converter together with the amplifier and with a TFT at its gate. Two different simulations were realized.

The layout of all circuit is presented in figure 4.15.

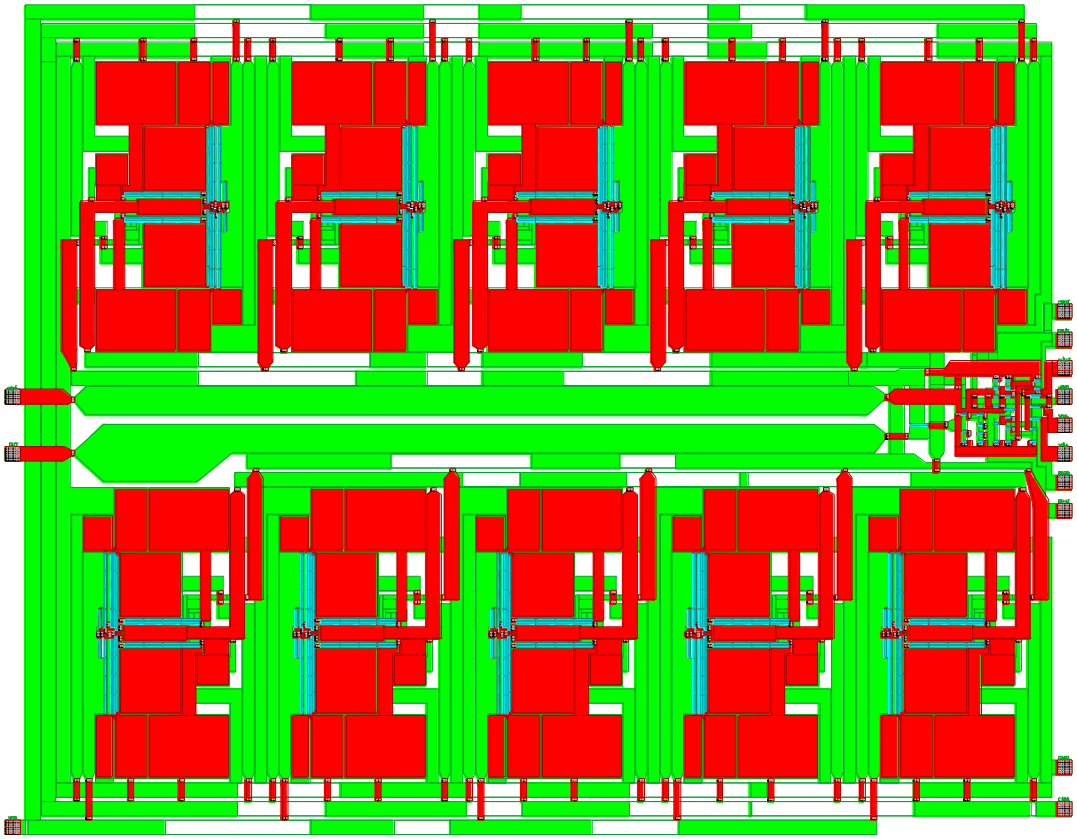


Figure 4.15: Designed layout of the all circuit

Due to the large extension of the connections between the different DC/DC converters, the source/drain material (Ti/Au) with a large width was used, to reduce the parasitic resistance associated. The dimensions of the circuit are 18709.55μm at the horizontal axis and 14557.1μm at the vertical axis.

Chapter 5

Conclusions and Future Work

Regarding the design and fabrication of a DC/DC converter using transparent electronics, this thesis has initialized with a study of the background and a bibliographic review of the work done in this field until now. Then, it was studied and simulated different topologies in order to design the DC/DC converter with the best performance. The steps to improve such performance have resulted in a design of 10 DC/DC converters in parallel and a regulator to reduce the voltage ripple at the output. At the final stage, the layout of the circuits was designed.

Analysing the accomplishment of the objectives, it is presented that the majority of them were successfully realized, with the design of an improved topology DC/DC converter using transparent TFTs and the design of a method for regulation. A study about the behaviour of the inductors was also realized. The study of the resistor and the capacitor is realized with the fabrication of the circuits in CENIMAT, because in the chip a set of these passive elements were designed. However, this was not yet realized, which has been a limitation to the accomplishment of this work.

The circuit proposed in this report includes a block of 10 DC/DC converters with 27.8V at the output voltage if a 10V input voltage is applied. A single DC/DC converter has an output voltage of 16.37V in the same conditions. The circuit also includes an amplifier with a voltage gain of 36.7dB and 83.79 degrees of phase margin. The regulator designed in the final circuit proposes a decrease of 80% in voltage ripple.

The usage of transparent electronics was the major barrier beyond the design of the proposed circuits, due to their intrinsic limitations such as the resistivity of the materials. This technology is not well developed yet, which is another difficulty because some parameters are not well-known and could be detrimental for a successfully circuit performance.

5.1 Future Work

Regarding the possible future work, the time available to develop this research and the limitations of the technology resulted in some ways to fulfill the objectives totally. One is the design of a higher-gain amplifier, to increase the low gain of 36.7dB achieved. Another possible way that was not considered in this work is the usage of PWM regulation. It is an improved method of

regulation that can achieve better results and better performance due to the direct regulation of the duty-cycle for the DC/DC converter. The circuit presented in this report only regulates the voltage level according to the output of the DC/DC converters with some error. In relation to the technology, the possibility of using p-type a-IGZO TFTs could be another step to improve the integrated circuits designed with transparent electronics.

Although much work still needs to be done, this report presents a step forward in the transparent electronics, that can have a promising future in the next few years.

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