Debugging mixed-signal circuits via the IEEE1149.4 Std. - analysis of limitations and requirements

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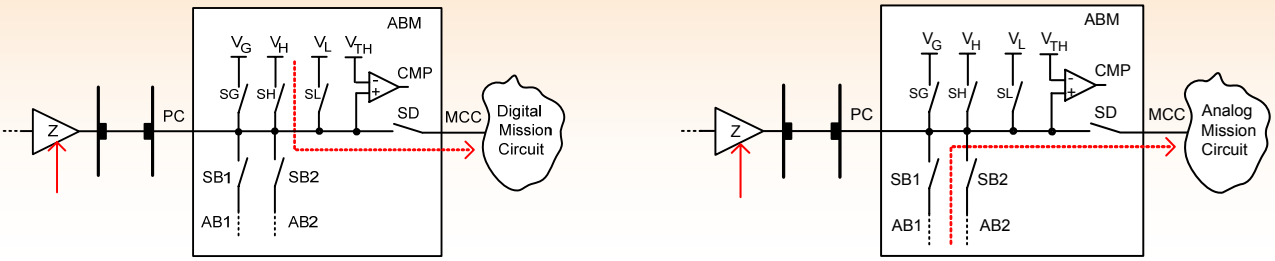
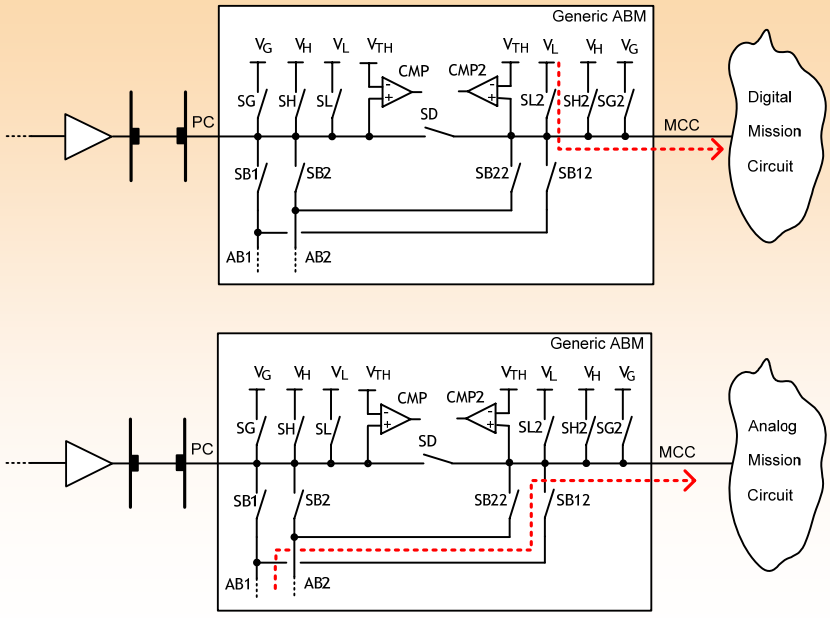
Motivation: To reuse the IEEE1149.4 infrastructure to support debug operations in mixed-signal circuits.

The problem: The analog or digital signal in the Mission Circuit Connection (MCC) will be controllable together with the Pin Connection (PC) only if all outputs connected to the associated pin have high-impedance capability.



The solution: The proposed generic ABM structure always allows the analog and digital controllability of the MCC. 1



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Abstract

Debugging mixed-signal circuits is traditionally seen as a complex task due to the presence of an analog part and the necessary interaction with a digital part. The use of debug tools that require physical access suffers from the same restrictions that led to the use of debug tools based on electronic access to digital circuits. While the IEEE1149.4 test infrastructure enables the structural and parametric test of mixed-signal boards, through electronic access, its use for debug purposes is still far from reaching a wide acceptance, namely due to the lack of a debug methodology. This work analyses several access mechanisms for Controllability, Observability and Verification operations via the IEEE1149.4 infrastructure, with an emphasis on the analysis of its limitations and requirements.

1. Introduction

Mixed-signal (MS) circuits include an analog part and a digital part with an interaction between them. These circuits are rising in importance on the last years as shown by a study from IBS Corp., which estimates that 73 percent of all design start-ups will include one or more MS blocks by 2006 [1]. According to information from leading semiconductor manufacturers, the analog circuitry in MS Systems-on-a-Chip (SoC) are estimated to account for just two percent of the total number of transistors, while at the same time representing 20 percent of the total area, 40 percent of the total design effort, and 50 percent of the total number of re-spins. Analog circuit design is much more sensitive to implementation details and silicon process variations than its digital counterpart, therefore any critical analog circuitry tends to be a bottleneck for design implementation, verification, and migration to manufacturing for the overall MS design [2]. The action of debugging MS circuits intends to detect, locate and diagnose all sorts of errors and it usually includes some sort of Controllability, Observability and Verification (COV) operations. Although these operations are very important, especially during the prototype validation phase, circuit miniaturization is constraining the use of debug tools that rely on physical access to implement them. MS circuits have analog and digital inputs/outputs so electronic access is needed in both domains. However, this is much less of a problem in the digital domain. The IEEE1149.1 [3] test infrastructure was developed to support the structural testing of digital boards. This restricted objective has facilitated the acceptance of this standard and enabled its use for many other purposes, like debugging, for instance. As a result, the IEEE1149.1 infrastructure is currently working together with the NEXUS infrastructure for debugging operations in microprocessor-based circuits. In the analog domain, electronic access strategies are still in their infancy. Since the IEEE1149.1 is a well accepted mechanism to access digital nodes, and considering that 1149.4 [4] is an extension of 1149.1, it is worth analyzing if a combined 1149.1 / 1149.4 test infrastructure may be effectively used as a platform to debug MS circuits.

This work analyses the access mechanisms for COV operations via the IEEE1149.4 test infrastructure. Chapter two analyzes the COV operations and extends the digital debug model into the MS arena. Chapter three analyzes several access means that may be used to achieve COV. Chapter four identifies a controllability insufficiency of the IEEE1149.4 infrastructure and presents a generic ABM block to overcome this limitation. Chapter five concludes this paper.

2. Debugging digital and MS circuits

Debugging digital circuits through COV operations usually requires a collection of tools based on some

type of access. Some tools are specific of microprocessor systems e.g. In-Circuit Emulators (ICE), while others remain generic (logic analyzers, oscilloscopes, multimeters). Each tool can perform a large number of different operations, although all of them belong to a small number of debug operation types. According to the basic debug model presented in Figure 1, any debug operation fits into one of four debug operation types [5, 6], namely:

- COV of the circuit state
- Breakpoints/Watchpoints
- Single Stepping
- Real-time Analysis

The Breakpoint, the Single Stepping and the Real-time Analysis are used to control/observe/verify the operation of the circuit in the temporal domain, while the COV operations are used to control/observe/verify the circuit state.

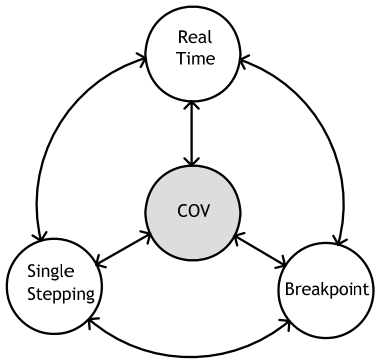

Figure 1. Basic debug model

As an example, suppose that we want to verify if a specific data value appears in a certain memory position, when the content of the program counter reaches a certain value. The correspondent flow of debug comprises the following steps: first, clear the defined memory position via a Control Operation; second, place the circuit in normal operation mode and then stop it when the program counter reaches the value specified by a Breakpoint Operation; third, read the specified memory position via an Observation Operation; and four, verify if the observed data matches the expected value via a Verification Operation. These same debug operation types can be used in the remaining digital circuits. For instance, the Breakpoint concept can be applied in a sequential circuit, by stopping the clock signal when some condition is validated and forcing the circuit to memorize the actual state, and then using the COV operations to monitor and verify the actual values of that circuit state. The Single Stepping operation can be used in the same circuit to control the clock signal and use the COV operations to monitor and verify every single state. In practice, these very same types of debug operations, as shown in Figure 1, can be extended to MS circuits. As an example, imagine we want to memorize the circuit state when a specific analog voltage surpasses a predefined limit that corresponds to a Breakpoint operation, or that we want to observe in real-time the voltage present at a certain circuit node; or, in a Single Stepping scenario, that we want to determine the cut-off frequency in a digitally programmable filter by, step-by-step, applying several input analog signals with different frequencies and then observing the corresponding analog output values.

These few examples illustrate the idea that the basic debug model, presented in Figure 1, can be extended to MS circuits. The referred operations are used to COV the circuit in the temporal domain; then it is also necessary to examine the circuit state through COV operations (e.g. after and/or before a Breakpoint operation) using one or more debug tools based on some type of access. Having in mind that physical access is increasingly compromised, electronic access becomes the preferred (and eventually only) solution.

In an MS scenario the problem is partially solved for the digital input/output nodes by using the IEEE1149.1 Test Access Port (TAP) and embedded test infrastructure. However, this type of electronic access to analog input/output nodes for COV operations, in a debug scenario, is not yet fully exploited in the current literature.

3. COV operations via DBMs and ABMs in MS circuits

The alternatives available to realize the COV operations are called Access Types and are divided as follows:

- Direct/physical Access
- Direct/electronic Access
- Indirect Access

Direct/physical Accesses are the primary input/output nodes and test points where it is possible to connect the probes of an Automatic Test Equipment (ATE) or other test instruments. **Direct/electronic** Access is performed through electronic access means such as scan chains or dedicated access blocks. **Indirect** Access is accomplished by propagating signals through intermediate circuit blocks. The IEEE1149.1 and the IEEE1149.4 infrastructures are used in the case of direct/electronic access.

3.1. Direct/physical access

The direct/physical access means are the primary input/output nodes and test points in the circuit where it is physically possible to connect the debug probes. The COV operations in this case are the following:

A1 – Control- *The primary input nodes of the circuit are directly controllable by physical probes. Controlling other circuit nodes may be difficult or impossible to achieve due to physical access restrictions. Even when physical access is possible, controllability may be prevented due to backdriving restrictions.*

A2 – Observation- *All such nodes (I/O nodes, test points) are directly observable by physical probes.*

A3 - Verification- *Verification requires an observed signal, a window to define an acceptable deviation, and a comparison mask. When the mask is active, the comparison result is true if the observed signal is within the window limits and false otherwise. Comparison is not performed if the mask is inactive.*

3.2. Direct/electronic access: IEEE1149.1

Direct/electronic access is performed through electronic access means such as scan chains or dedicated access blocks. The IEEE1149.1 infrastructure belongs to this category. Each 1149.1 test cell comprises several elements, but for the sake of simplicity it will be represented here by a single block with just one Parallel Input (PI) and one Parallel Output (PO), as shown in Figure 2.

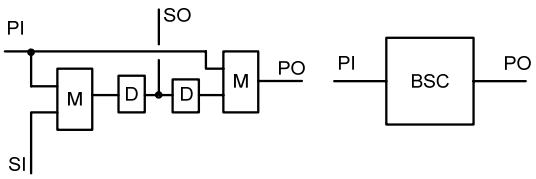

Figure 2. The 1149.1 test cell and its simplified representation

The Boundary Scan Register (BSR) is formed by a chain of Boundary Scan Cells (BSC). Each cell is associated with a (digital) functional device pin or with an internal digital node located on the interface between the Digital Mission Circuit (DMC) and the Analog Mission Circuit (AMC), as shown in Figure 3.

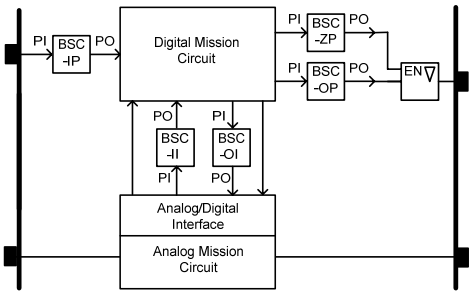

Figure 3. Type of BSCs according to their location in the circuit

According to their location in the circuit, each cell is designated as follows:

- BSC-IP: input pin
- BSC-OP: output pin
- BSC-ZP: controlling the high-impedance condition of an output pin
- BSC-II: input node on the interface between the analog and digital mission circuits
- BSC-OI: output node on the interface between the analog and digital mission circuits

The COV operations through this access type are the following:

A4 - Control*- The logic level in the parallel output of any BSC is always controllable (intrusively).*

A5 - Observation*- The logic level in the parallel input of any BSC is always observable (non-intrusively). The logic level in the parallel output will be observable only if the component supports an optional instruction to enable this operation.*

A6 – Verification

As described in A3.

3.3. Direct/electronic access: IEEE1149.4

The IEEE1149.4 infrastructure provides direct/electronic access means for MS circuits in the form of test cells associated with analog functional pins — Analog Boundary Modules (ABM) — and test cells associated with digital functional pins — Digital Boundary Modules (DBM). DBMs and ABMs will be represented as simple blocks with two connections as shown in Figure 4. DBMs have a Parallel Input (PI) and a Parallel Output (PO), and their orientation follows the digital signal flow (i.e. the PO side is connected to an output pin or to an input node of the mission circuit). ABMs have a Pin Connection (PC) and a Mission Circuit Connection (MCC).

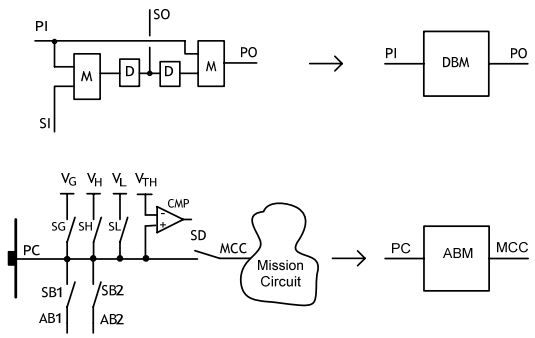

Figure 4. DBM / ABM blocks and their simplified representations

The PC is always connected to a pin and the MCC is always connected to a mission circuit node. ABMs are normally associated with analog input/output pins, but they can also be associated with digital input/output pins. DBMs are associated with digital input/output pins and optionally with the digital nodes located on the interface between the analog and digital mission circuits (mandatory if the test infrastructure supports the *INTEST* instruction), as shown in Figure 5.

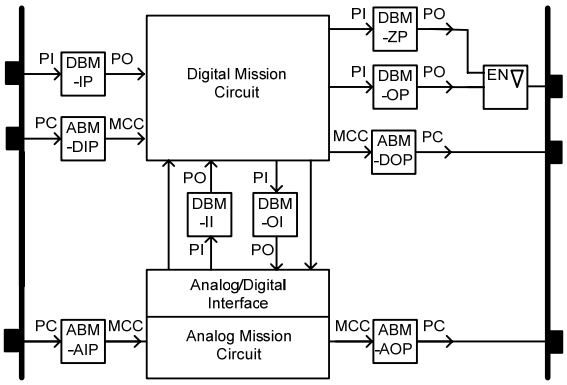

Figure 5. Types of DBMs and ABMs according to their location in the circuit

According to their location in the circuit, ABMs and DBMs will be designated as follows:

- ABM-AIP: analog input pin
- ABM-AOP: analog output pin
- ABM-DIP or DBM-IP: digital input pin
- ABM-DOP or DBM-OP/ZP: digital output pin
- DBM-II: input interface node (from the digital mission circuit point of view).
- DBM-OI: output interface node (from the digital mission circuit point of view).

The COV operations through this type of access are as follows:

A7 - Digital control

DBM - The logic level in the parallel output of any DBM is always controllable (intrusively).

ABM-DIP – The logic level in the pin connection is always controllable (intrusively). The logic level in the mission circuit connection will be controllable together with the pin connection if all the outputs connected to the associated pin have high-impedance capability.

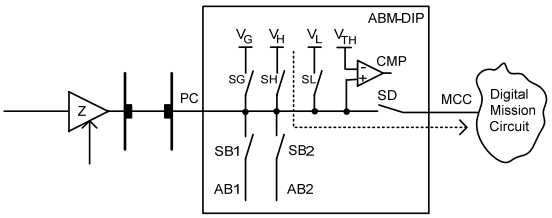

Figure 6. Digital control operation through the ABM-DIP

As seen in Figure 6, the ABM-DIP is able to control the digital input of the mission circuit if its driver has high-impedance capability.

ABM-DOP – The logic level in the pin connection is always controllable (intrusively).

A8 - Analog control

ABM-AIP – The analog signal in the pin connection is always controllable via AT1 or AT2 (intrusively). The analog signal in the mission circuit connection will be controllable together with the pin connection if all outputs connected to the associated pin have high-impedance capability (intrusively).

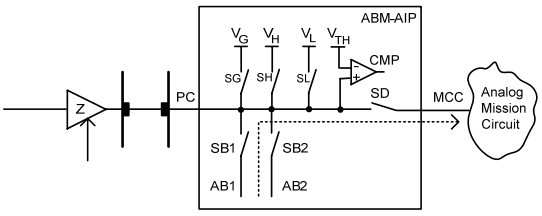

Figure 7. Analog control operation via an ABM-AIP

Figure 7 shows that the ABM-AIP has the means to control the analog input of the mission circuit if its driver has high-impedance capability.

ABM-AOP - The analog signal in the pin connection is always controllable (intrusively).

A9 - Digital observation

DBM - The logic level in the parallel input of any DBM is always observable (non-intrusively). The logic

level in the parallel output will be observable only if the test infrastructure supports an optional instruction to enable this operation.

ABM-DIP/DOP – The logic level in the pin connection is always observable through the scan chain. The logic level in the mission circuit connection will be observable in the same manner if it is possible to close the SD switch during this operation. The logic signal in the pin connection is always observable in real-time via AT1 or AT2. The logic signal in the mission circuit connection will be observable in the same manner if it is possible to close the SD switch during this operation.

A10 - Analog observation

ABM-AIP/AOP - The analog signal in the pin connection is always observable via AT1 or AT2. The analog signal in the mission circuit connection will be observed in the same manner if it is possible to close the SD switch during this operation.

A11 – Verification

As described in A3.

3.4. Indirect access (propagation)

Indirect access relies exclusively on propagation to realise the COV operations:

A12 - Controllability- *The signal present in a given node will be controlled by propagation only if an appropriate influence cone is available.*

A13 -Observability- *The signal present in a given node is observable if it is possible to propagate that signal to a node that is directly observable.*

A14 -Verification

As described in A3.

4. Future research

The IEEE1149.4 Std. defines an infrastructure with a high potential for COV operations even while the circuit is working at its nominal speed. The possibility to use ABMs in both analog and digital pins enables their use for COV operations on both domains. Since the ABM is primarily oriented to support operations related to pin connections, the opposite end (i. e. operations related to the mission circuit connection) is still lacking the same type and coverage of operations. In fact, to control a mission circuit connection via an associated ABM, its driver stage must support a high impedance mode (see A7 and A8). The IEEE1149.4 Std. defines some basic functional requirements for the ABMs and furthermore it allows the introduction of specific features to achieve other functionalities. Since the ABM does not have a fixed orientation in terms of signal flow, its COV potential (*in both connection sides)* requires a generic structure such as the one presented in Figure 8.

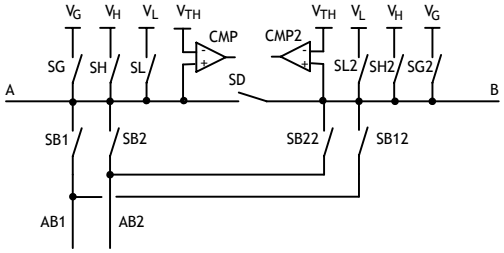

Figure 8. Generic ABM structure for debugging purposes

This configuration covers all the debug operations in both analog and digital nodes, inputs and outputs, pins and internal nodes. Its obvious disadvantage is the higher overhead, but the current trend is to integrate into the device the necessary means to support COV operations. Although this configuration includes more switches, increasing the total number of combinations (i.e. 2^{2x5} possible combinations instead of 2^5 combinations in the 'standard' ABM), many are 'not relevant' since the same ABM terminal cannot be connected to different voltages, and also because controllability requirements normally address a single ABM terminal. From this generic ABM we can derive simpler configurations that cover COV needs for specific circuit nodes, such as what happens in the case of the IEEE1149.1 Std., where several BSC types are presented.

5. Conclusion

This paper presented an extension of the digital COV operations and analysed its applicability in MS circuits. Implementation of those operations via several access means was also analysed and led to the identification of limitations imposed by the "standard" ABM structure. To overcome such limitations we proposed an enhanced and generic ABM structure, from where simpler ABM configurations may be derived to meet specific COV requirements.

Acknowledgement

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