BOARD-LEVEL BIST BASED ON THE 1149.1 STANDARD

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The progress in the fields of miniaturisation (surface mount technology, large pin count ICs, etc.) and integration density (due to feature size reduction, and exploited by the availability of highly sophisticated CAD design tools) has made it possible to design very complex Printed Circuit Boards (PCBs), which present very high testability requirements. Boundary Scan design and test is now largely accepted as one of the most promising solutions for this challenge, with an increasing number of off-the-shelf BST components becoming available, and easy-to-use software tools which automate the development of the boundary scan infrastructure for ASIC design.

Board-level test, which was the main driving force behind the development of the BST standard, is however still waiting for an integrated family of components able to address three main requirements: the test of non-BST clusters, analog I/O interface, and board-level BIST capability. Proposed solutions for these problems have been published and some components are available, but a much large offer for board-level designers is still required.

This paper proposes a board-level BIST strategy based on three types of testability building blocks: the interface to non-BS digital I/O nodes, the interface to analog I/O nodes, and a dedicated test processor providing the board-level test capability. It is shown that, by following careful design rules, it is possible to implement all the proposed building blocks in medium-complexity programmable logic devices (PLDs) widely available, therefore providing a low-cost and maximum-flexibility solution for board-level BIST. Moreover, and since these testability blocks were implemented using a simple and powerful hardware design language (HDL), any changes due to specific board requirements can easily be made.

J.M. Martins ferreira

20th CAVE Workshop
Dresden/Holzhau
Germany
May 1993

CAVE

TIMETABLE & PROGRAMME

Sunday, 16 May 1993

19:00	Ist bus departs from Dresden airport
20:30	Registration
21:00	Dinner
23:00	2nd bus departs from Dresden airport

Monday, 17 May 1993

07:45	Breakfast
08:15	Registration for late arrivals
08:45	Workshop start • Introduction Karl-Heinz Diener (Local Organizer) • Opening Address Birger Schneider (Workshop Chairman)
09:00	**Tony Sauer**, Chairman JESSI Application Board "JESSI–Status and Future Directions"

09:30 **Session 1: "Hardware/Software Codesign"**

Chairman: **Wolfgang Rosenstiel**, Univ. Tübingen, D
Coordinator: **Ulrich Lauther**, Siemens, D

Speakers:

Manfred Glesner, TH Darmstadt, D
"Experience with Hardware/Software Codesign for Mechatronic Applications"

L. Spaanenburg, Univ. Groningen, NL
"A Migration Architecture for Intelligent Control Applications: A Simple Example of Codesign"

Klaus Buchenrieder, Siemens, D
"HW/SW Codesign for Time Discrete and Time Continuous Systems"

Wolfgang Rosenstiel, Univ. Tübingen, D
"Hardware/Software Partitioning with UNITY"

Posters:

Paolo Prinetto, Politechnico de Torino, I
"A Methodology for System Level Design for Verifiability"

Carlos Beltran Almeida, INESC, Lisboa, P
"SEMCI - An Emulation System"

12:30 **Group photograph**

12:40 **Lunch**

14:00 **Session 2: "VHDL in Real Industrial Environments"**

Chairman:
Coordinator: **Gordon Adshaed**, Manchester Design Technology, UK

Speakers:

Lars Lindqvist, NKT Elektronik, DK
"Evaluating the Applicability of Current VHDL Synthesis Tools to an Industrial Top-Down Development Procedure"

Francesco Sforza, SGS-Thomson, I
"UNICAD_VHDL: A VHDL Oriented Design Environment"

Duncan Kitchen, BNR, UK
"VHDL-Based Design Experience at BNR Europe"

Wolfgang Rosentiel, Peter Thole, Univ. Tübingen, D
"Synthesis of a CAN Controller Part Employing CALLAS and Mentor Autologic"

Posters:

Jap Smit, Twente Univ., NL
"VLSI System Design under Power Dissipation Constraints: Theory, Methods and Tools"

Jörgen Sturm, Thesys, Erfurt, D
"Chip Design by CASE"

17:15 Session 2 ends

17:30 **Session 3: Working Session "Technology Trends"**

Coordinators:	**Jean Pierre Tual,**	Bull, F
	Gordon Adshead,	MDK, UK
Discussion Leaders:	**Massiomo Vanzi,**	IST, I
	Peter van Staa,	R. Bosch, D

Posters:

Carlos Lopez Barrio, TID, E
"Technology Requirements for the 2000's TELECOM SYSTEMS"

19:30 Session 3 ends

19:30 **Technical Committee Meeting**

20:30 **Dinner**

Tuesday, 18 May 1993

07:30 Breakfest

08:30 **Session 4: "Simulation: Mixed Mode, Multi Level"**

Chairman: **Jochen Jess**, Uni Eindhoven, NL
Coordinator: **Ludwig D.J.Eggermont,**

Speakers:

Jean Michel Bergé, CNET/CIT, F
"VHDL Analog Extensions (1076.1)"

Peter Schwarz, FhG-IIS/EAS, D
"Application of and Experiences with Multi-Level, Mixed-Mode Simulation"

Hazem El Tahawy, Anacad, F
"Mixed Signal Simulation with ELDO"

Louis Stroucken, Philips ED&T, NL
"Mixed Signal Simulation: Experiences with Miles"

Posters:

Ole Olesen, Univ. Lyngby, DK
"Automatic Design Tools Using Cadence SKILL"

Gareth Watts, Analogy Inc., UK
"VHDL in a Multi-Level, Mixed-Mode Simulation Environment"

Jochen Jess, Eindhoven Univ. of Techn., NL
"ESCAPE: A Flexible Integrated Specification and Simulation Environment"

Hans-Joachim Jentschel, TU Dresden, D
"Design Modelling and Simulation of Signal Processing Systems"

12:00 **Session 3: Continuation of Working Session on: "Technology Trends"**

13:00 Session 3 end

13:00 **Lunch**

14:15 **Social Event: Visit to Historic Dresden**

20:00 **Return to hotel**

20:15 **Technical Committee Meeting**

21:00 **Gala Dinner**

Wednesday, 19 May 1993

07:30 Breakfast

08:30 **Session 5: Built-in Self Test (BIST) for Digital/Analog"**

Chairman: **Frans de Jong**, Philips, NL
Coordinators: **Birger Schneider**, microLEXSystems, DK
Carlos Beltran Almeida, INESC, P

Speakers:

Ian Bell, University of Hull, UK
"Self Testing Switched Current Circuits"

Taco Zwemstra, Philips, NL
"On-Chip Signal Generation Using Sigma-Delta Modulation"

Miguel Miranda, Univ. Politec. de Madrid, I
"Generation of Optimised Single Distributions of Weights for VLSI Built-In Self-Test"

José Manuel Martins Ferreira, INESC, P
"Board Level BIST Based on the 1149.1 Standard"

Posters:

Birger Schneider, microLEX Systems, DK
"P1149.5 Module Test and Maintenance Bus"

Raimund Ubar, Tall. TU, Estonia
"Alternative Graphs and Testpattern Design in Digital Systems"

Christian Sebeke, Univ. Hannover, D
"Analog Fault Simulation"

11:45 Session 5 ends

11:45 **Workshop close: Birger Schneider**

12:00 **Lunch**

12:50 **Bus departs for Dresden airport**

Posters of Attendees

from Central and Eastern European countries (EEMCN)

and

Eastern part of Germany

Norbert Fristacky, TU Bratislava, Slov.

"R & D in Digital System Design in the Department of Computer Sciences and Engineering"

Guntis Fricnovichs, Latv. Acad. of Science, Riga, Est.

"R & D Activities of the Institute of Electronics and Computer Science" (preliminary title)

Elena Gramatová and Milan Duda, Slovak Acad. of Science, Bratislava, Slov.

"Activities of the Institute of Computer Systems in EEMCN"

Günter Elst, FhG-IIS/EAS, Dresden, D

"R & D Activities of the Department for Design Automation for Integrated Circuits and Systems" (preliminary title)

Dimiter Jossifow, IME, Ltd, Sofia, BG

"Microelectronics - IME"

Wolfgang Hecker, MAZet, Erfurt, D

"MAZet - R & D activities"