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Analog Circuit Design with Transparent Electronics

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Mestrado Integrado em Engenharia Eletrotécnica e de Computadores

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July 26, 2013

A Dissertação intitulada

“Analog Circuit Design with Transparent Electronics”

foi aprovada em provas realizadas em 19-07-2013

o júri

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Resumo

O domínio da eletrônica transparente tem tido um grande desenvolvimento na última década, com o aparecimento e desenvolvimento de transístores transparentes baseados em tecnologias de filme fino. Várias tecnologias estão atualmente sob estudo e todos os anos são publicados diversos artigos sobre novas descobertas realizadas na área. A investigação deste tema tem se concentrado tanto ao nível da descoberta de novos materiais e melhoria dos processos de fabrico, como do aprofundamento da compreensão dos mecanismos físicos que ditam as características funcionamento destes dispositivos. Atualmente a principal aplicação deste tipo de transístor é a construção de FPDs (*Flat Panel Display*). No entanto a possibilidade de realizar circuitos analógicos e digitais totalmente transparentes tem também vindo a ser estudada.

Uma das tecnologias de TTFT (Transparent Thin-Film Transistor) mais promissoras é a tecnologia a-GIZO. Esta tecnologia apresenta interessantes características elétricas e é fabricada a baixas temperaturas, o que representa uma vantagem significativa relativamente aos processos de fabrico de circuitos integrados convencionais. Esta última característica permite a integração destes TTFTs em substratos transparentes e flexíveis originando uma redução dos custos de fabrico. Esta dissertação nasce da necessidade do projeto de circuitos eletrónicos em a-GIZO TFT com vista a permitir o desenvolvimento futuro de sistemas *on-chip*, integrando num mesmo substrato sensores e sistemas de condicionamento e processamento de sinal, todos implementados na mesma tecnologia. Para possibilitar este tipo de aplicações é necessário o desenvolvimento de circuitos de processamento de sinal como amplificadores, filtros e conversores. Com esta necessidade em mente, a presente dissertação tem como objetivo o desenvolvimento e projeto para fabricação de um dos principais circuitos necessários para a realização de processamento de sinal, o amplificador operacional.

Como resultado deste trabalho apresentam-se dois novos amplificadores operacionais implementados em TFTs a-GIZO. Uma destas topologias é um amplificador operacional comutado, uma técnica que é utilizada em circuitos de baixa potência no domínio de capacidades comutadas. No entanto esta técnica é aqui utilizada para reduzir o efeito da variação, ao longo do tempo, da tensão de limiar nos TFTs a-GIZO quando estes estão continuamente em condução. Incluída nestes amplificadores operacionais, apresenta-se uma nova topologia de andar diferencial de alto ganho com apenas transístores de enriquecimento do tipo n. Este andar permite obter o maior ganho de tensão entre todos os andares que usam realimentação positiva para aumentar a resistência de carga e que conseguem amplificar sinais dc. No entanto, o aumento do ganho é conseguido à custa de uma redução da gama dinâmica e largura de banda. Finalmente, um circuito Sample-and-Hold é implementado usando o amplificador operacional comutado proposto. Para a realização de simulações dos circuitos projetados, foi utilizado um modelo de tecnologia previamente construído com base num sistema de rede neuronal. Sendo que o processo de projeto de circuitos neste tipo de tecnologia é análogo ao utilizado em tecnologias convencionais.

Este trabalho é realizado em colaboração com o grupo CENIMAT da UNL, que fabricará o amplificador operacional e circuitos auxiliares produzidos durante a realização da dissertação.

Abstract

The area of transparent electronics has had a great development in the last decade, with the emergence and development of transparent transistors based on thin-film technologies - TTFTs. Several technologies are presently under study and every year numerous articles are published regarding new advances made in this area. Directions have been focusing both in the discovery of new materials and improvement of manufacturing processes, and in deepening the understanding of the physical mechanisms that dictate the electrical characteristics of these devices. Currently TTFTs find its main application in the construction of FPDs (Flat Panel Display). However, the possibility of realizing analog and digital circuits, with fully transparent electronics, has also been studied.

One of the most promising TTFT technologies is a-GIZO (amorphous Gallium-Indium-Zinc-Oxide). This technology presents interesting electrical characteristics and can be manufactured at low temperatures. It represents a significant advantage over the manufacturing processes of conventional integrated circuits. This feature allows the integration of the TTFTs on transparent and flexible substrates and also enables a reduction in manufacturing costs.

This dissertation stems from the need to design electronic circuits that enable the development of future *systems-on-chip*, integrating on a single substrate sensors and signal processing systems. To make such application possible with a-GIZO, the development of analog processing and conditioning circuits, such as amplifiers, filters and converters, is required. Having this need in background, the present dissertation fosters its main goal in the development, design and fabrication of one of the most important circuits needed to perform signal processing, the operational amplifier.

Two novel operational amplifier topologies result from this work. One is a switched operational amplifier, a technique that is used in low-power design for switched-capacitor circuits. Here however, this technique is introduced to reduce the shift in the threshold voltage of a-GIZO TFTs under stress. Included in the operational amplifier, a novel topology for a differential high-gain stage, with only n-type enhancement transistors, is also proposed. This stage gives the highest voltage gain, amongst all of the stages that use positive feedback to increase the load resistance, while still being able to amplify dc signals. Nevertheless, the higher gain is achieved at the cost of a reduction in dynamic range and bandwidth. Finally, a Sample-and-Hold circuit is implemented using the proposed switched operational amplifier. For electric simulation, a previously designed behavioural model was used. The rest of the design process follows a similar track to that of conventional technologies, namely CMOS.

This work is conducted in collaboration with the CENIMAT group at UNL, which will manufacture the operational amplifier and auxiliary circuits produced during the course of the Master Thesis.

Acknowledgements

I begin by thanking my parents and my brother who always supported me in all of my decisions and gave me the strength to go after my objectives. My parents also sacrificed a lot so that I could have a good education and without them I wouldn't be where I am today and for this I am very grateful.

I also want to extend my thanks to my best friends Henrique Martins and Romano Torres with whom I have shared this five year journey at FEUP. We have been through a lot together and helped each other surpass many obstacles along the way. Without them all those hours studying for exams and spent in front of a computer screen developing the projects that were done throughout the course would have been much more difficult to pass.

Before concluding I would also like to thank Ganga Bahubalindrani for her support and help during these last few months in the development of the master thesis. Even though she was busy she would always find time to help solve some of the problems that occurred during the development of my work and she shared all of her finds and knowledge on thin-film transistors with me. Without her work the work developed would not be possible because it was she who paved the way in the design, simulation and testing of circuits with a-GIZO TFT in FEUP.

In the same regard I want to thank Nuno Cardoso for all the help he gave on how to work with the tools he developed for Layout design in a-GIZO TFT technology.

I would also like to thank Prof. Dr. Pedro Barquinha of CENIMAT for all of the help with the layout design and fabrication of masks for the fabrication process and with the fabrication of the produced circuits themselves.

Finally, I thank Prof. Dr. Vítor Grade Tavares for all the advice and ideas he gave me during my work and for all of the support he gave during the elaboration of documents. His advice played a great part in the work that was ultimately developed and helped solve numerous problems found along the way. And maybe the most amazing thing is that sometimes 5 minutes talking with him could help solve a multitude of problems.

Bruno Silva

“Life is and will ever remain an equation incapable of solution, but it contains certain known factors.”

Nikola Tesla

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Abbreviations, Acronyms and Symbols

ADC	Analog-to-digital converter
a-GIZO	Amorphous Gallium-Indium-Zinc-Oxide
a-Si:H	Hydrogenated Amorphous Silicon
AOS	Amorphous oxide semiconductor
CAD	Computer-aided design
CM	Common-mode
CMFB	Common-mode feedback
CMOS	Complementary metal-oxide-semiconductor
CMRR	Common-mode rejection ratio
DAC	Digital-to-Analog Converter
FPD	Flat-panel display
GBW	Gain-bandwidth product
IC	Integrated Circuit
MOSFET	Metal-oxide-semiconductor field-effect transistor
NMOS	N-type metal-oxide-semiconductor
OTFT	Organic Thin-film transistor
Opamp	Operational Amplifier
PSRR	Power supply rejection ratio
RF	Radio frequency
RO	Ring-oscillator
SCCMFB	Switched Capacitor Common-mode feedback
SFDR	Spurious-free dynamic range
S/H	Sample and Hold
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static random-access memory
TAOS	Transparent amorphous oxide semiconductor
TFT	Thin-film transistor
THD	Total Harmonic Distortion
TTFT	Transparent thin-film transistor
ZnO	Zinc-Oxide
dB	decibel
g _{ds}	Drain to source transconductance
g _m	transconductance
Hz	Hertz
V _{th}	threshold voltage
r _o	Intrinsic output resistance of a transistor
μ _n	Mobility of charge carriers in the channel of an n-type transistor

Chapter 1

Introduction

Transparent electronics is a rapidly growing field that has garnered a lot of interest from researchers around the world, especially in the last decade. This interest was mainly fuelled by the first reports on transparent thin-film transistors published in 2003 [13, 14, 15], all of which used a ZnO as the channel layer material. In the following year Nomura et al. reported the successful fabrication at room-temperature of transparent and flexible TFTs in polyethylene terephthalate substrates using an amorphous oxide semiconductor, a-GIZO, as the active layer material [16]. This active layer material is also optically transparent, allows low-temperature processing and presents higher carrier mobility than other amorphous semiconductors used in TFTs, namely a-Si:H which is widely used in the flat panel display industry.

Various researches have been carried out in recent years concerning the physical characteristics and the limitations of a-GIZO TFTs. This is so because they are seen as viable candidates to substitute a-Si:H TFTs in the production of the next generation of flat panel display technologies, and in the fabrication of flexible displays. Due to these researches work, considerable advances have been made in the fabrication process of these devices, resulting in the compensation of some performance limitations presented by the technology, especially in terms of electrical characteristics and semiconductor stability. Still, this technology is not yet matured and as of the moment of the writing of this document, various improvement proposals are being conducted on this subject.

This work aims to show that it is already possible to implement operational amplifiers with significant voltage gain in a-GIZO TFTs as well as in other technologies that only have available a single type of device. We propose two operational amplifiers that include a novel high-gain topology intended for technologies with only n-type enhancement devices. Both of the proposed topologies have the same signal path but have different schemes of countering the effect of the shift in the threshold voltage of a-GIZO TFTs under stress. In the continuous time version of the amplifier, the threshold voltage shift is mainly countered by means of common-mode feedback, while in the switched operational amplifier the transistors are periodically cut-off. An actual pulsed biasing scheme is then implemented to minimize transistor stress. Such technique has been previously demonstrated with digital circuits to decrease the threshold voltage shift and consequently increase the lifetime of circuits in a-GIZO TFTs [17].

1.1 Problem Presentation and Challenges

In spite of all the interesting characteristics that this technology presents one must still take into account that it is a fairly recent technology and therefore it is not yet reached a state of maturity. Because of this, the development process becomes much more complicated and time consuming than in conventional integrated-circuit design carried out in well developed silicon based technologies. The major difference is the fact that unlike MOS technologies which have detailed libraries and accurate simulation models, for a-GIZO TFTs these do not exist at this time. The non-existence of accurate a-GIZO TFT device models for simulation stems from the fact that some physical processes associated with the operation of the device are not yet fully understood. Nonetheless, a verilog-A model has been developed at FEUP allowing circuit simulation with these TFTs. However, this model does not include the parasitic capacitances for these transistors as it has not yet been possible to characterize these capacitances. Besides the lack of accurate simulation models, this technology also presents several other limitations when compared to the traditional CMOS technologies and, to this day, there are no operational amplifiers implemented with this transistor. Still, some implementations of opamps do exist in other TFT technologies that present similar characteristics, such as the case of a-Si:H TFT and pentacene based OTFTs.

Of the aforementioned limitations one very important is the low carrier mobility that is some orders of magnitude inferior to that of a MOS transistor. The low carrier mobility results in low transconductance values and consequently in lower intrinsic gain when compared to their NMOS counterparts. Another limitation is the lack of useful complementary devices. Therefore, only n-type transistors are available when constructing circuits and since the fabrication of depletion type devices would require an extra mask, which consequently increases fabrication costs, only enhancement type devices were considered. The use of only n-type enhancement devices calls for the use of bootstrapping or positive feedback techniques to achieve significant values of load resistance when implementing gain stages with active loads. These techniques, however, lead to circuits with lower bandwidth and with more transistors than those designed with traditional CMOS. Nonetheless, the main challenge of designing analog circuits with a-GIZO TFTs is the fact that when subject to constant biasing the transistor's threshold voltage tends to shift over time. In practical applications this will ultimately result in at least one of the transistors in the circuit entering the cut-off region and thus ending the normal operation of the circuit. If this limitation is not taken into account in the design process, the resulting circuits will present a very short lifetime, making them only suitable for a very limited set of applications.

In short, the challenge was to develop a topology for a high-gain operational amplifier in a technology that has low transconductance, a threshold voltage that shifts over time when the transistors are constantly biased, in which there are no complementary devices and also taking into account that only n-type enhancement mode transistors must be used to reduce the fabrication costs.

1.2 Motivation

With the technology presenting a considerable amount of drawbacks it becomes paramount to explain the motivation associated with trying to develop circuits with it so early in its development stage. To start explaining the motivation it is important to understand that TFTs, and more specifically a-GIZO TFTs, must not be viewed as replacements for CMOS technology. In reality, as semiconductors the former present worse characteristics than the latter and have the considerable drawback of not possessing a complementary device, which hinders the design of analog circuits. The purpose of the TFT technology can be viewed as specific. It opens the opportunity for a whole new range of applications due to its particular features, namely transparency, low-cost fabrication and the possibility of an easy integration with flexible and transparent substrates. A panoply of applications have not yet been possible to realize until recent years because the existing technologies did not in fact possess these required characteristics. Of such applications the ones that stand out the most are the system on panel or system on glass. An example is the possibility of providing flat panel displays that incorporate in the same substrate, electronic circuits, such as pixel drivers and analog signal-conditioning blocks along with the TFT arrays that constitute the display, all of which made with the same technology, allowing for reduction of fabrication costs and integration efforts. In order to build the referred signal-conditioning circuits, and thus make possible an implementation of the system-on-panel concept described above, the development of an operational amplifier becomes imperative to allow signal amplification and thus the implementation of active filters and converters.

Also, to date no operational amplifier has been presented with this technology, although some other types of analog circuits have already been reported. So, the proposed amplifier aims to be the first operational amplifier built solely with a-GIZO TFTs.

1.3 Objectives

In terms of the definition of the objectives, both the limitations of the technology, and the state of technology design kit being developed at FEUP, at the time the work on the thesis started, were taken into account. From the analysis of the previous factors the following objectives were defined:

- Develop, simulate and produce the respective layout of an operational amplifier with only n-type enhancement mode a-GIZO TFTs, for applications in switched-capacitor circuits.
- The developed amplifier must present values for open-loop gain and gain bandwidth as high as possible taking into account the limitations of the technology and the characteristics of the current devices that can be constructed at CENIMAT.
- Develop a topology able of reducing the effects of the threshold voltage shift in a-GIZO TFTs due to constant biasing.

1.4 Structure of the Document

This document presents the following structure:

- Chapter 2 provides a theoretical background regarding the subjects of a-GIZO semiconductor operation, design of amplifier topologies with only n-type enhancement devices, design and frequency compensation of operational amplifiers as well as an introduction to the concept of switched operational amplifiers. All of these concepts are introduced in this chapter in order to familiarize the reader to some of the specific topics that were involved in the work carried out.
- Chapter 3 presents a bibliographic review on operational amplifiers with only n-type transistors, operational amplifiers designed in TFT technologies with similar limitations to those presented by the a-GZIO TFT technology and on switched operational amplifiers.
- In Chapter 4 the methodology behind the design process of the amplifier is presented along with the detailed analysis of the various stages that constitute the novel operational amplifier topology designed, the layouts produced for the developed circuits and the results obtained in simulation.
- Chapter 5 presents the adaptation of the topology for the linear amplifier into a novel switched operational amplifier with a-GIZO TFTs and the application of this circuit in a sample-and-hold configuration. As in the previous chapter, the layouts produced for these circuits are also presented along with the results obtained in simulation.
- Chapter 6, which is the final chapter of this document, presents the conclusions obtained from the work developed along with proposals for future improvement of the proposed topologies and potential applications that may be constituted using the produced op amp.

Chapter 2

Background

In this chapter some important concepts regarding the a-GIZO TFT technology and analog circuit design are presented so that the contents presented in later chapters can be better understood. A special focus is given to the concepts of common-mode feedback and switched operational amplifiers because both concepts were applied in the topologies developed in this work.

The chapter is organized as follows: first, the characteristics of materials in which a-GIZO is included, the TAOS (Transparent Amorphous Oxide Semiconductor), are presented. These materials are used to produce a large part of the existing technologies of transparent transistors. The common a-GIZO TFT device structures are presented next, followed by an overview of the materials and techniques that influence the performance of a-GIZO TFTs. Then the TFT device operation is explained, together with the problems and limitations that affect a-GIZO TFTs. After this the design of high-gain amplifier stages with only n-type transistors is introduced followed by an overview on the characteristics and performance goals involved in the design of both single-ended and fully differential operational amplifiers. Finally, the concept of a switched capacitor operational amplifier, which has been applied to one of the novel topologies developed, is introduced as it is a technique that is not employed in typical IC design.

Appendix B presents a generic overview on the implementation of typical single-stage amplifiers, which has been left out of this chapter so as not to make it significantly long. Nevertheless it has been included in the document because it may facilitate the understanding of some of the other concepts addressed in this report.

2.1 Transparent Amorphous Oxide Semiconductors (TAOS)

The interest raised on TAOS for TFT active layers has started originally with a proposal by Nomura et al. [16] on using a-GIZO material (Amorphous Gallium-Indium-Zinc-Oxide) for the semiconductor (transistor channel) layer. These TFTs exhibited a higher performance than those that use binary oxides such as ZnO. It should also be noted that the materials were deposited at room temperature on plastic substrates. These materials derived from an earlier work presented by Hosono et al. demonstrating that it was possible to produce transparent conductive oxides using heavy

metal cations [18]. TAOS exhibit various advantages regarding other types of materials used in TFT active layers, for instance their amorphous structure eliminates the effects of grain boundaries, a major limitation in devices using polycrystalline materials that negatively affect its characteristic [19, p. 67]. Furthermore, due to the fact that free carriers in n-type TAOS are electrons in the s orbitals of cations, the overlap of these electrons is dimly influenced by the bonding structure of the material [20]. This property along with the lower density of carrier traps relatively to other AOS (Amorphous Oxide Semiconductor) contributes to a wide conduction band resulting in higher field-effect mobility in these materials. As an example, an a-GIZO TFT shows typical values of $\mu_{fe} > 10\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ while an a-Si:H TFT typical values are in the order of $\mu_{fe} = 1\text{cm}^2\text{V}^{-1}\text{s}^{-1}$. TAOS TFTs can be deposited at room temperature as referred earlier, allowing an integration of devices in substrates such as plastic or glass, which are widely used in the industry of flat panel displays. Finally, the most important characteristic of these materials is their wide-band gap, making them transparent to visible light and giving rise to a very low density of holes in n-type TAOS TFTs, which leads to small off-currents and small short-channel effects.

2.2 a-GIZO TFT device structures

The main structural difference between TFT devices and MOSFET resides on the fact that in TFTs the substrate has no electric properties and therefore does not play a role in the device operation. Also, the channel material is not embedded in the substrate as in MOSFET devices, being formed instead in the semiconductor material that is deposited on top of the substrate.

In terms of device structure TFTs are commonly classified according to the stacking order of the gate, channel layer and source/drain which leads to designations of top/bottom-gate devices and top/bottom-contact devices. There is also another characterization that is related to the source/drain contacts being or not in the same plane of the channel layer. If the source and drain contacts are placed in the same plane as the channel, the structure is classified as co-planar, otherwise the structure is designated as staggered. As result, four of the most common TFT structure configurations are staggered bottom-gate, staggered top-gate, co-planar bottom-gate and co-planar top-gate. In the present work, the devices will have a bottom-gate staggered configuration, the most commonly used in academic research. Nevertheless, recent studies [21] propose a top-gate self aligned structure that presents a possible solution to the high parasitic capacitances that are obtained in devices using a bottom-gate topology.

2.3 Overview of the materials and processes that influence the performance of a-GIZO TFTs

The device structure of the TFT has impact in its performance as stated before, but it is of course not the only factor that influences the characteristics of the transistor. In fact the materials used to define the different layers of the TFT and the process used to deposit each layer play a huge role on the final characteristics of the device. For this reason the fabrication process of a-GIZO

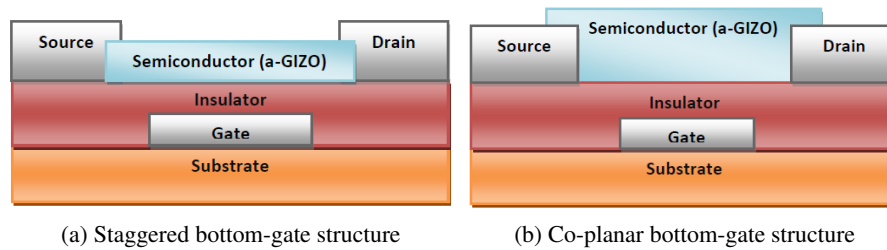


Figure 2.1: Bottom-gate a-GIZO TFT Device Structures

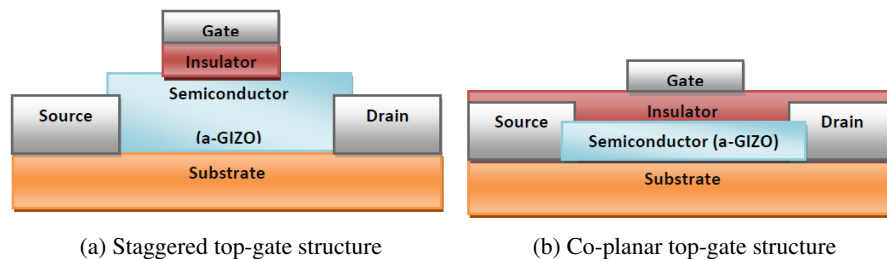


Figure 2.2: Top-gate a-GIZO TFT Device Structures

TFTs and the materials used for its layers have been extensively studied during the last few years, mainly because the technology shows great promise regarding commercial applications for the near future, especially in flat-panel displays. Consequently, today we have fabrication processes that are capable of improving the device characteristics and that are able to reduce the effects of some major setbacks that are inherent to the technology. Such advances have not just been concerned with the methods and techniques used to deposit the different layers, they have also been focused on the relative proportions of the materials that compose the semiconductor, on the thickness of the semiconductor layer, on the TFT device structure, on source/drain electrode materials and in the materials used to define the dielectric layer, all of which have an impact on the overall performance of the transistor [22].

2.3.1 Characteristics of the channel layer material

The semiconductor layer of this TFT is made of a multicomponent amorphous oxide semiconductor based on the combination of metallic cations of Gallium, Indium and Zinc. The relative concentration ratios of Ga, In and Zn, used to produce the semiconductor, impact the performance of the transistor. It has been shown that one way to increase the device's μ_{fe} (mobility) is through the manipulation of the thin-film composition [22, 23]. It has also been demonstrated that the thickness of the semiconductor layer impacts the performance of the semiconductor in terms of its switching behaviour and of the device's threshold voltage [22].

2.3.2 Materials used in a-GIZO TFT Source/Drain electrodes

The source/drain electrode composition has a significant impact on device performance, consequent of its high-resistivity contact values. This problem affects the carriers mobility and therefore the device transconductance, hindering its application in amplifier circuits. The topic of contact resistance will be revisited and further explored later in 2.5.4. Other parameters of a-GIZO TFT performance that have shown alterations with different source/drain materials are the threshold voltage, V_{ON} and the ratio between on and off currents [24]. Among others ITO, Ti/Au and Mo are currently being used for source/drain electrodes. The devices using Au/Ti electrodes demonstrate better performance, however, lack of transparency is a major drawback associated with this material. On the other hand, ITO electrodes are transparent but TFTs with such electrodes present significantly reduced performances in comparison to those using Ti/Au [24].

2.3.3 Other techniques used to improve performance of the a-GIZO TFT

The studies on the fabrication process of this type of TFT have also led to the utilization of techniques that increase the devices performance without changing, directly, the materials that constitute the semiconductor layer and the source/drain electrodes. One of these techniques is annealing. This process can be done after the deposition of the semiconductor layer and before source/drain electrode deposition, or it can be done after the deposition of both. In either case, annealed devices show better performance in terms of channel mobility, sub-threshold voltage swing, on/off current ratio and they present decreased shifts in the threshold voltage due to biasing stress. Still, if the annealing process is done after the deposition of source/drain electrodes the performance of the device is further augmented [24]. Another technique that has been used to improve the performance of a-GIZO TFTs is passivation. This technique turns the surface of the device less reactive to the environment reducing the negative effects that occur in devices presenting a bottom-gate configuration when the semiconductor layer is in contact with the atmosphere.

2.4 a-GIZO TFT Operation Principle

As previously introduced, some of the physical aspects of the device are still not fully understood. Still TFTs are field-effect transistors and the I-V characteristics indicate that the equations that describe the operation principle of a MOSFET provide a reasonable approximation to the characteristic of an a-GIZO TFT. However, this approximation is not very accurate due to the difference among semiconductor materials, mainly because of the amorphous nature of the a-GIZO semiconductor. More accurate models of operation for these devices have been proposed recently [25, 26].

2.4.1 Ideal TTFT Operation

With n-type TTFTs the biasing of the gate, by a positive voltage, attracts electrons, creating an accumulation layer at the surface of the semiconductor close to the gate dielectric. This accumulation layer provides a conductive channel from the source to the drain of the device. To explain how

the conduction of current happens in these devices, consider a TTFT with its source grounded and biased by a positive voltage at the gate electrode, ensuring that a conductive channel is formed. If under these conditions a positive voltage is applied to the drain electrode, a positive V_{DS} is achieved and electrons will be injected from the source to the channel layer and then extracted at the drain electrode. The transportation of negative charge from source to drain through the channel layer generates a flow of current in the opposite direction which is denominated as drain current, I_{DS} . As can be concluded from previous explanation, there will only be current flow between source and drain if there is a conductive channel formed between these contacts. From this last fact, we can extract the conditions that define the first operation mode of the device denominated as cut-off mode. In this mode the device is considered as being *off* because there is no significant current flow between the source and drain contacts due to lack of a conductive channel between them, as depicted in figure 2.3. To define the conditions on which this mode is reached, it is important to define the parameter V_{ON} . This parameter corresponds to the minimal source to drain voltage that guarantees that an electron accumulation channel is formed in the device. With this parameter defined, the condition on which the transistor is defined to be in cut-off mode can be determined as $V_{GS} < V_{ON}$.

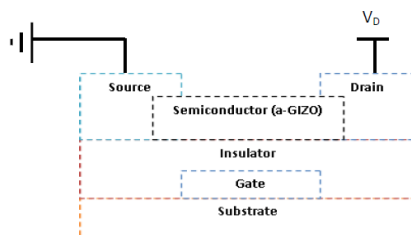


Figure 2.3: TTFT in Cut-off mode

Now, if we analyse the behaviour of the device when current is flowing between source and drain, which corresponds to $V_{GS} > V_{ON}$ (reasonably higher) and $V_{DS} > 0$, like with a MOSFET, we can define two different regions of operation: the linear mode, or pre-pinch-off in which $V_{DS} < V_{GS} - V_{th}$ and the saturation mode, or post-pinch-off in which $V_{DS} \geq V_{GS} - V_{th}$.

Before beginning to explain and characterize both of these modes of operation it is important to explain the difference between the concepts of V_{ON} and V_{th} in terms of what they represent in this technology. In a MOSFET the parameter that is defined as the threshold voltage, normally referred as V_{th} , corresponds to minimum value of V_{GS} necessary to induce an inversion layer in the interface between the gate dielectric and the substrate of the device, to a level of charge concentration equal to that of the substrate. In a n-type TTFTs V_{ON} is the minimal voltage necessary to ensure an electron accumulation layer in the interface between the semiconductor and the gate insulator. This parameter is extracted from heuristic measures of the devices characteristics. The threshold voltage, V_{th} in TTFTs has no actual physical meaning, it is a pseudo-constant that is defined for analysis purposes because in these devices the current I_{DS} measured when $V_{GS} = V_{ON}$ is relatively small. V_{th} is defined as the intersection with the x-axis of the linear part of the transfer curve of

$I_{ds}^{1/2}$ for various values of V_{GS} . This parameter defines the minimum voltage for which the drain current characteristic is approximately proportional to the square of V_{GS} . Figure 2.4 shows the i_{DS} characteristic of one of the a-GIZO TFTs previously characterized at CENIMAT, here both V_{on} and the reduced sub-threshold swing of these transistors are clearly visible.

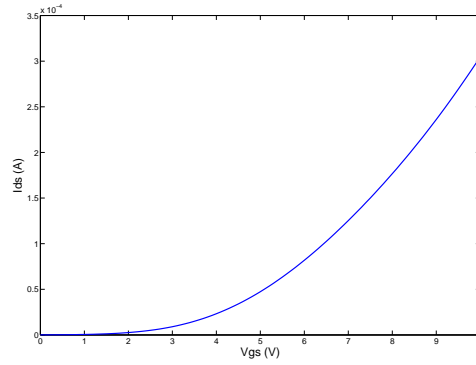


Figure 2.4: I_{DS} of an a-GIZO TFT biased with constant V_{DS}

Hoping that the disambiguation between those two parameters has been settled, it is possible to proceed with analysis of TFT operation when the device is in linear mode. In this mode the device shows an $I_{DS} - V_{DS}$ characteristic that is approximately linear and the value of the drain current is approximately given by

$$I_{DS} = \mu \frac{W}{L} C_G [(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}], \quad (2.1)$$

where C_G is the gate capacitance per unit area, μ is the mobility of the electrons in the channel, W and L are, respectively, the width and length of the channel. respectively.

In this mode of operation there is a continuous conductive channel that connects the source and drain, as represented in figure 2.5. TFTs biased in linear region can be used to implement small value active resistors suitable for switching.

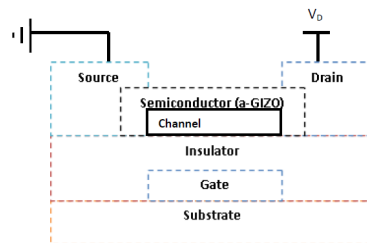


Figure 2.5: TFT in Linear mode

The last mode of operation is saturation. In this mode, the drain voltage rises above the gate voltage. As that voltage rises, the channel close to the drain becomes depleted of carriers. The local potential difference, between the channel and the insulator, is not high enough to keep an inversion layer. Under this condition the channel is *pinched-off*, as represented in figure 2.6, and

the I_{DS} current becomes constant, as it no longer increases with the increase of V_{DS} . This is better explained if we consider that charge density at a generic distance from the source x in the channel is given by [27, p. 20]

$$Q_d(x) = C_G[V_{GS} - V(x) - V_{th}] \quad (2.2)$$

At the drain where $x=L$ the charge density in the channel becomes

$$Q_d(L) = C_G[V_{GS} - V_{DS} - V_{th}] = 0 \quad (2.3)$$

In this operation mode the drain current is given by

$$I_{DS} = \mu \frac{W}{2L} C_G (V_{GS} - V_{th})^2 \quad (2.4)$$

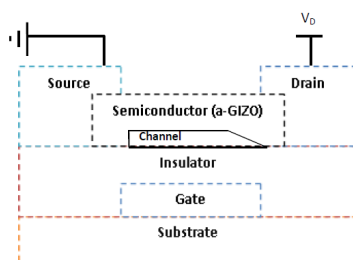


Figure 2.6: TTFT in Saturation mode

In a final comparison between the physical operation of TFT devices and the MOSFET it is important to reference that since the substrate of TFTs does not influence their operation, TFTs do not suffer from body effect.

2.4.2 Channel length modulation in TTFTs

In an ideal representation of a TTFT operation, the current in saturation was described as being constant. For this to be true the output resistance of the device would have to be infinite and this is not verified when extracting the device's I-V characteristic. Therefore, it is crucial to explain why there is a finite output resistance and how it can be characterized. This parameter is very important to determine the intrinsic gain of the transistor, given by:

$$A_{int} = -gm \cdot r_o \quad (2.5)$$

Returning to equation (2.2), it can be easily concluded that if V_{DS} continues to increase, relatively to V_{GS} , the pinch-off point will start moving towards the source because $V(x)$ will be equal to V_{GS} at a point $x < L$, thus reducing the effective length of the channel.

Re-examining I_{DS} in saturation (2.4), if the length of the channel is reduced the drain current is increased, given the fact that the drain current is inversely proportional to the effective length

of the channel. Then, the characteristic of the drain current in saturation is better approximated if we replace L by $L - \Delta L$, where ΔL is the difference between the length of the channel and the distance between the source and the point where the channel is pinched-off. After substituting the value of the channel length in the equation, and after a few mathematical manipulations, I_{DS} in the saturation region can be expressed by,

$$I_{DS} = \mu \frac{W}{2L} C_G (V_{GS} - V_{th})^2 \left(1 + \frac{\Delta L}{L}\right), \quad (2.6)$$

considering that the position of the pinch-off point, and therefore ΔL , is approximately proportional to the V_{DS} , we can define

$$\frac{\Delta L}{L} = \lambda V_{DS} \quad (2.7)$$

combining (2.6) and (2.7) we can express I_{DS} as

$$I_{DS} = \mu \frac{W}{2L} C_G (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}), \quad (2.8)$$

where λ is a proportionality constant, expressed in V^{-1} .

The above equation (2.8) shows that I_{DS} for the saturation region is not constant, opposed to and ideal operation model, but linearly proportional to V_{DS} , thus explaining the finite value of the output resistance presented by a-GIZO TFTs in saturation.

As with MOSFET, the Early voltage, V_A , is defined by the point, in the negative axis, where the straight-line formed from current characteristics in saturation regime, for different V_{DS} values, converge. It represents the voltage at which I_{DS} would be zero if the transistor always operated in saturation, independently of the value of V_{GS} . This parameter can also be determined as being equal to $1/\lambda$. The output resistance of the device can then be estimated by

$$r_o = \frac{V_A}{I_{DS}} \quad (2.9)$$

2.5 Limitations of the technology

An important part of trying to implement analogue or digital circuits with a-GIZO TFTs passes through the understanding of the limitations imposed by the technology. The importance of this step is crucial because the TFT represents the main building block and if the limitations it presents are not understood, it is not possible to explore the full potential of the technology when implementing electronic circuits. On the other hand, such limitations may lead to the conclusion that for now it is not possible to implement a specific type of circuit, or that the final implementation does not present the necessary performance that the circuit designer set out to achieve at the beginning of the design process. This is a consequence of the fact the technology is still in the early stages of its development which is of course a big limitation but does not mean that it is impossible at this point to start implementing some types of electronic applications with it. Backing up this theory

is the fact that some limitations presented by this technology can be circumvented using specific techniques when designing circuits. This shows that the maturing process depends not only on the improvement of the physical properties of the devices, but also on the development and improvement of circuit design techniques aimed specifically for the characteristics of the a-GIZO TFT technology.

In this section the most relevant limitations of the a-GIZO TFT technology, regarding the design of amplifying stages, are addressed in order to set up the background for the design of an operational amplifier, which is the main goal of the work carried out in the Master Thesis.

2.5.1 Carrier mobility

The first technological limitation to be considered, when designing amplifying stages with a-GIZO TFT, is the field effect mobility of n-type devices in a staggered bottom-gate structure. For these devices the carrier mobility has typical values around $10\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, attained in the earlier stages of development, and $73.9\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ reported on a more recent study [22]. Comparing these values with the ones of an n-type a-Si:H TFTs, which are typically $1\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, it is easy to realize that, at least in this aspect, a-GIZO TFTs are superior, but when compared with the field effect mobility values of polycrystalline TFTs, and of MOSFET devices, the field effect mobility of a-GIZO TFTs is inferior by some orders of magnitude.

The mobility values affect the transconductance of the transistors in saturation given by

$$gm = \left(\frac{dI_{DS}}{dV_{GS}} \right)_{V_{DS, const}} \quad (2.10a)$$

$$= \mu C_G \frac{W}{L} (V_{GS} - V_{th}) \quad (2.10b)$$

The above equation implies that gm increases with the increase of the intrinsic mobility of carriers in the device, μ . So a-GIZO TFTs will have transconductance values superior to the ones of a-Si:H TFTs but inferior to the transconductance values of polycrystalline TFTs and MOSFETs, considering of course that all devices present the same aspect ratio. From the above analysis and from (2.5), it is also demonstrated that the intrinsic gain values of a-GIZO TFTs are superior to those of a-Si:H TFTs but also inferior to the ones from polycrystalline TFTs and of MOSFETs. This in turn implies that for the same amplifying stage topology and the same load resistance, a common-source stage using a NMOS transistor for the drive will have a much superior gain to that of one using an a-GIZO TFT with the same aspect ratio.

2.5.2 Complementary devices

Another limitation that is directly related to the difficulty of implementing high-gain stages, with these transistors, is the lack, at this time, of p-type transistors for this technology. The existing p-type devices present poor characteristics which make them inappropriate for circuit application, mainly due to extremely low hole mobility.

As introduced before in chapter 1, without complementary type transistors there are only two options available to the circuit designer regarding the transistor to be employed as an active load. The first option, which is to use a depletion type transistor seems to be the more logical one because we could achieve a higher load resistance with only one transistor, but to fabricate these type of transistors an extra mask would be necessary increasing the overall fabrication cost. With the possibility of low fabrication costs being one of the main advantages of this technology, this option becomes somewhat counter-productive. Thus the best option really seems to be the implementation of electronic circuits with only n-type enhancement a-GIZO TFTs. This of course has a very big impact on the gain values achievable in high-gain stages such as the simple common-source stage.

Consider a common-source stage using a complementary device as an active load, as depicted in figure 2.7 the gain of this stage is given by,

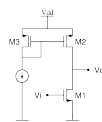


Figure 2.7: Generic Common-source amplifier with complementary active load

$$A_v = -gm \cdot (r_{oN} || r_{oP}), \quad (2.11)$$

if r_o is the same in both the driver and the load transistors, the gain becomes equal to

$$A_v = -gm \cdot \frac{r_{oN}}{2}, \quad (2.12)$$

which is half of the intrinsic gain of the drive transistor. Considering now the same topology but implemented with only n-type enhancement transistors, as represented in figure 2.8. The gain of this stage now is given by

$$A_v \approx -gm_1 \frac{1}{gm_2} \quad (2.13)$$

Since gm is directly proportional to the aspect ratio of the transistors (2.10), the gain of this stage is given by the relation of the aspect ratios of the drive and load transistors. In this configuration, to achieve, for example, a 20dB gain, the gate of the driver transistor would have to be approximately 10 times wider than the gate of the load transistor, considering that both transistors have the same gate length. This leads to circuits with a large area, poor performance because of the large gate capacitance associated to the driver transistor and the use of higher supply voltages.

Unlike the low-carrier mobility, the non-existence, at this time, of viable complementary devices can be compensated if positive feedback is used in the active load. This topic will be explored in section 2.6.2.

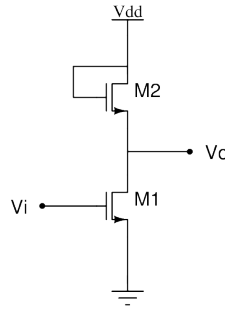


Figure 2.8: Generic Common-source amplifier with diode connected enhancement load

2.5.3 Gate-bias Stress

Of all the limitations currently presented by this technology the one that is probably the biggest obstacle to the development of electronic circuits and specifically analog circuits is the existence of gate-bias stress. This phenomenon corresponds to the change, over time, of a transistor's threshold voltage, V_{th} , due to constant biasing. This effect has been also verified in other TFT technologies, such as a-Si:H, and impacts the behaviour of amplifying stages in a significant manner. Consider the simple common-source with only n-type enhancement transistors stage previously presented in 2.8. If we take into account that due to constant positive biasing of the transistors their threshold voltages will increase as time passes, eventually at least one transistor in the circuit will get out of the saturation region and will go into cut-off as $V_{th} > V_{GS}$, and the circuit will stop working. Since this effect can become quite significant in short periods of time, variable according to the fabrication processes, ranging from some minutes to a few hours, the produced circuits will have low lifetimes. But, at least for the most part, when the circuits are turned off the effect is also reversible, although it can take hours or even a few days [28]. The cause of this effect has been attributed to a trapping of charge carriers in defects that exist in the dielectric and at the interface between the semiconductor and the dielectric [29]. These defects generate extra electron states that can be occupied due to stress.

The V_{th} shift with time, due to biasing, can be expressed by [1, 30, 31],

$$\Delta V_{th} = V_{th0} (1 - e^{-\frac{t}{\tau} \beta}), \quad (2.14)$$

where τ is a characteristic time constant, β is the stretched-exponential exponent, and ΔV_{th0} is the device threshold voltage shift as time goes to infinite.

The annealing of a-GIZO devices, introduced in section 2.3.3, reduces the effects of the shift in the threshold voltage [31].

Gate-bias stress is not the only phenomenon with impact on the stability of a-GIZO TFTs. It has also been demonstrated that the device characteristics are sensitive to light, exposure to water vapour and to temperature variations [32]. Nonetheless, for the purpose of designing amplifying

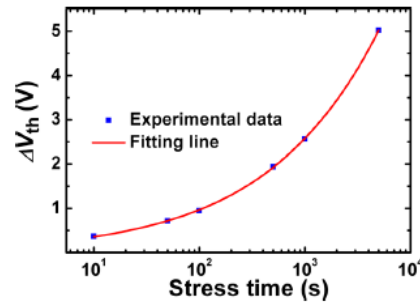


Figure 2.9: Time dependence of ΔV_{th} for gate bias stresses, reprinted from [1]

stages the most relevant cause of device instability is the shift over time in the V_{th} , in consequence of the constant biasing of the gate.

2.5.4 Contact Resistance

As introduced earlier in section 2.3.2, the materials employed for source and drain contacts also influence the overall performance of the a-GIZO TFT because of possible high values of contact resistance that can be attained. High values of contact resistance at the source/drain electrodes cause an effect of current crowding that negatively affects various electrical characteristics of the device, such as the threshold voltage, the mobility of carriers in the channel, the ratio between on and off currents and the subthreshold voltage swing [33].

Barquinha et al. reported a study of a-GIZO TFT characteristics for different source/drain materials, IZO, Ti, Mo, Ti/Au with the annealing process done both before and after the deposition of the materials [24]. This study concluded that of these materials Ti/Au was the one who led to a higher μ_{fe} and that there was a significant reduction in this parameter for devices with lower values of L, which was attributed to a higher influence of contact resistance in the total resistance of short-channel devices. It was also concluded that if the device was annealed after the deposition of source/drain electrodes, the electric characteristics achieved were improved. In terms of the design of amplifier stages, the impact of this issue is again related to decreased values of the mobility of carriers in the channel, which leads to a lower intrinsic gain of the transistors.

2.5.5 Gate Capacitance

Devices built in bottom-gate staggered configuration present an additional limitation, which is the large value associated with the parasitic gate capacitance. The high gate capacitance value is the result of a significant overlap between the source/drain electrodes and the gate. As in a MOSFET device, the overlap is increased with an increase in the dimensions of W and L. The total gate

capacitance can be approximated by the sum of the channel and overlap capacitances, assuming that these capacitors are linear.

$$C_{Channel} = C_G \times W \times L \quad (2.15)$$

$$C_{Overlap} = C_G \times W \times L_{overlap} \quad (2.16)$$

$$C_{Gate} = C_{Channel} + C_{Overlap} \quad (2.17)$$

From this model it can be verified that if the length of the overlap between the source/drain electrodes and the gate is significant, relatively to the effective channel length, the overall gate capacitance of the transistor will be increased significantly. In terms of amplifying stages, high values of gate capacitance lead to potential low-frequency poles, affecting the overall frequency response and bandwidth of the circuits.

2.6 Operational Amplifier Design

After going through the analysis of the limitations posed by the transistor that was used in this work it is important to also have knowledge about the various steps that are involved in the design of an operational amplifier. In this section some background information regarding the design of opamps, such as the definition of target parameters and the analysis of topologies with more than one stage are presented so that the reader may better understand the work presented in later chapters. The concept of positive feedback applied in the increase of load resistances is also introduced because this technique played an important role on the amplifier topologies that were developed.

To start, it is important to state the importance of Operational Amplifiers (opamp). These electronic circuits are an essential part of modern day electronics and are of vital importance in mixed signal circuits where they find a wide application spectrum, both in linear (e.g. amplification and filtering) and nonlinear applications (e.g. comparator).

The application of opamps in microelectronics is very diverse and the design of operational amplifiers is often more oriented for specific applications than for generic purposes. For this reason the design of operational amplifiers follows different objectives than those that are intended to achieve amplifiers with characteristics similar to those of the an Ideal opamp, namely high open-loop gain, very high-input resistance and a low-output impedance. This change in paradigm occurred due to the existence of other characteristics associated with the performance of opamps besides these last three and because there are trade-offs between some of these characteristics. Therefore, it is necessary to design these circuits considering that there are many variables associated with this process and knowing that by trying to maximize a certain characteristic, such as

open loop gain, other parameters that may also be important for a specific application, maybe be compromised.

With this last concept in mind the following list with some of the main performance parameters associated with the design of op amps is presented [27, chap. 9]:

- Open-Loop Gain
- Small-Signal Bandwidth
- Large-signal Bandwidth
- Output Voltage Swing
- Linearity
- Sensitivity to Noise
- Sensitivity to Offsets in the input
- Power Supply Rejection

In the end it is up to the designer of the opamp to carefully select the topologies and techniques to be used, so that the final design meets all the constraints imposed by the application. However, the technology used must also be taken into account when defining performance goals, a notion that becomes very important when working with technologies such as the ones based on thin film semiconductors.

After the definition of a preliminary set of performance parameters, the designer must define the topology for the opamp itself and for this step he must have knowledge of the small-signal behaviour of the transistor he is going to use.

2.6.1 a-GIZO TFT small-signal model

To analyse amplifier stages using a-GIZO TFT, a small-signal model is necessary in order to estimate the gain, values of the input and output impedance and the frequency behaviour of each topology.

As presented in section 2.4, the a-GIZO TFT is a field effect transistor and its ideal operational principle is in many ways similar to that of a MOSFET. Based on such similarity, the small-signal equivalent circuit, of an ideal n-type a-GIZO TTFT, is derived from the small-signal equivalent circuit of an NMOS device. The only difference, presented in figure 2.10, resides on the fact that in an NMOS model an additional component is needed to account for the body effect. In a-GIZO TFT no body effect is accounted for because the substrate does not have an electrical influence on the device operation.

Keep in mind that this model is a mere approximation for the intrinsic operation of the TFT and that many assumptions associated with it are not very accurate. For example the parasitic capacitances included in this model, which are depicted as being fixed, in reality are non-linear

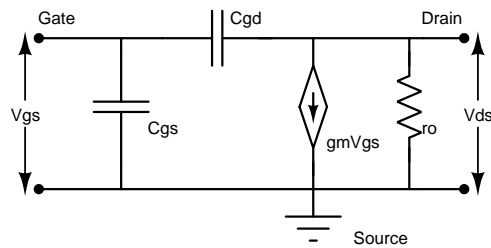


Figure 2.10: Small-Signal Model of an ideal a-GIZO TFT

because their values depend on the magnitude of V_{GS} and V_{DS} . However, as long as the signal is kept small, the linear approximation is valid.

A more accurate small-signal model of TTFTs using the staggered bottom-gate structure, seen in figure 2.11, is presented in [19, p. 136].

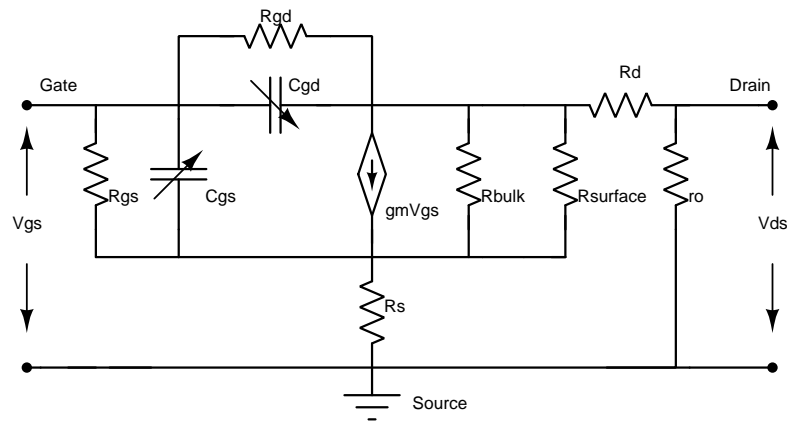


Figure 2.11: Small-Signal Model of a non-ideal TTFT

In this model, besides the representation of the devices parasitic capacitances as being variable, many other non-idealities associated with these devices are represented such as the contact resistance, expressed by the resistors R_S , R_D , R_{GS} and R_{DS} , the resistance of the conductive channel, R_{bulk} , and the residual drain current due to an electron accumulation layer at the interface between the semiconductor and a passivation layer, $R_{surface}$.

2.6.2 Designing High-Gain Amplifying stages with only n-type enhancement transistors

Considering that the simplified small-signal model of an a-GIZO TFT is similar to that of a MOSFET, in great part due to the fact that these transistor are of field effect type, we can expect the common amplifier stages used in typical analogue IC design will have similar behaviour with this technology. Still, if stages capable of achieving non-negligible voltage gain are considered, such as the common-source, common-gate or cascode configuration, it is found that the value of the

gain always depends on the transconductance and output resistance of the drive transistor, but also on the load resistance. Of these three parameters two are more technology dependent, g_m and r_o , and the other one is mostly dependent on the topology used to implement the load. Although the load could be directly implemented through a passive resistor, it would not be a very viable option due to area concerns because the load resistances may be required to present a magnitude of few mega Ohms in order to achieve significant voltage gain. Therefore, in typical opamp design, load resistances are implemented with transistors and are designated as active loads. In high-gain stages, active loads are usually implemented with complementary devices, which are not available when designing circuits with a-GIZO TFTs, as introduced before in section 2.5.2.

Using only n-type it is, however, possible to increase the load resistance using an enhancement n-type transistor with positive feedback between its source and gate terminals, as depicted in figure 2.12 for a common-source stage.

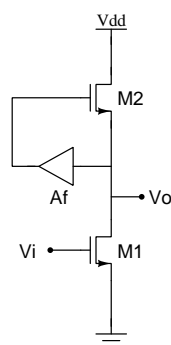


Figure 2.12: Common-source stage with positive feedback in the active load

In this configuration the load resistance is found to be

$$R_L = r_{o2} \parallel \frac{1}{g_{m2} \cdot (1 - A_f)} \quad (2.18)$$

From the later equation it is verified that if $A_f = 1$ the load resistance will be equal to r_{o2} , and this topology will present the same gain as a common-source stage with an active complementary load, previously presented in figure 2.7, and equal to

$$A_v = -g_m \cdot (r_{o1} \parallel r_{o2}) \quad (2.19)$$

It is also possible to have $A_f > 1$ but this situation leads to instability which is undesirable.

The problem then becomes the implementation of the feedback network. This can be accomplished in one of two ways. One is ac bootstrapping and the other consists in the usage of a buffer to feedback the output signal in order to implement dc bootstrapping.

The use of a buffer, depicted in figure 2.13, is very easy to comprehend and when implemented it requires the designer to ensure that the gain of the buffer will not be superior to 1, for stability

purposes. The principle of ac bootstrapping, represented in figure 2.14, will always ensure that the feedback factor is never superior to one, but since it uses a high-pass filter, formed by C and M3 to feedback the signal, the configuration will not be able to amplify dc signals. The operation principle of this topology is simple. For dc signals the capacitor acts as an infinite impedance and the biasing for the gate of the load transistor is provided by T3, which is cut-off, but for small-signal the output is fed back with the feedback factor depending of the capacitive divider between C and the equivalent capacitance seen at the gate of the load transistor.

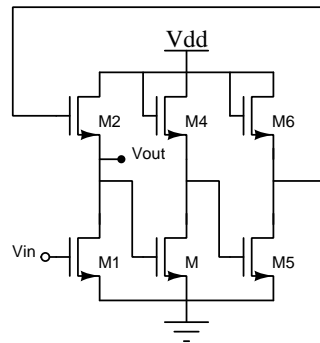


Figure 2.13: Active load positive feedback loop implemented with a buffer

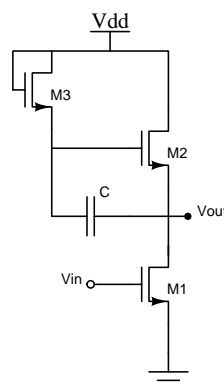


Figure 2.14: Active load positive feedback loop implemented with capacitive bootstrapping

2.6.3 Multi-stage Amplifiers

To satisfy the performance constraints required for some applications it may be necessary to use more than one amplifying stage when designing an operational amplifier. For example, in an application that requires high-gain and a low-output impedance, a simple solution would be to use a differential pair with a high small-signal resistance at the load to obtain a high-voltage gain. Then, connect the output to a source follower with an approximately unity gain, maintaining almost all of the gain of the previous stage and lowering the amplifiers output impedance. However, when the design of an opamp in technologies based in thin-film is considered, the necessity of using

more than one stage can become unavoidable because the gain that can be obtained, even with positive feedback, is reduced when compared to typical CMOS technologies due to low mobility values.

Still, the use of multiple stages does not come without a cost because the more stages that are used the more poles, and potentially zeros, are introduced in the system thus complicating compensation. Therefore, when designing multi-stage topologies it is important to meet the performance requirements that were set with the lowest amount of poles possible, which in turn means that the designer should try to use the least amount of stages possible.

2.6.3.1 Miller Effect

A very important concept associated with the analysis of the frequency response of amplifier stages is the concept of Miller Effect. Miller's Theorem states that if a circuit like the one depicted in figure 2.15a can be converted to that of figure 2.15b, then $Z1 = Z/(1 - A_v)$ and $Z2 = Z/(1 - A_v^{-1})$, where A_v is the voltage gain between nodes A and B.

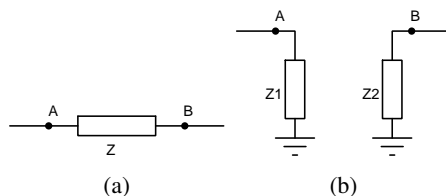


Figure 2.15: Miller Effect applied to a floating impedance

To show how this effect is important in frequency analysis of amplifying stages, consider the common-source stage represented in 2.16. In this figure the intrinsic capacitors of the TFT are represented. Solely C_{GS} and C_{GD} are represented because in TFTs there is no C_{DB} or C_{SB} , which must be considered when implementing circuits with MOSFETs. From the analysis of this figure it is immediately verified that C_{GD} connects the input and output nodes and therefore can be converted into an equivalent capacitor at both of these nodes, using Miller's theorem.

Recalling that a capacitor can be expressed as an impedance $Z = \frac{1}{C.S}$, the total capacitance connected between node A and ground is $C_A = C_{GS} + (1 - A_v)C_{GD}$ and the total capacitance seen between node B and ground is $(1 - A_v^{-1})C_{GD}$. Because $A_v = -gm.R_D$ is generally much bigger than unity, the capacitance seen at the input node of the common-source amplifier is superior to the one seen at the output, due to the Miller multiplication of C_{GD} . Thus, the pole associated with the input node will occur at lower frequencies than the one associated with the output node.

The possibility of Miller multiplication of capacitors must always be accounted for when characterizing the total capacitance connected between a node and ground. These capacitance values can be used to determine an estimation of the time constants associated with each node of the circuit, in order to have an estimate of the frequency response of the opamp.

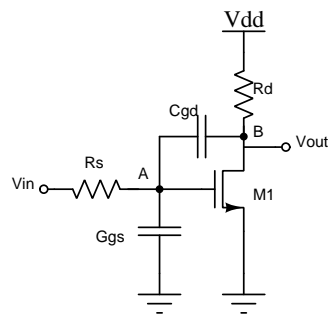


Figure 2.16: Common-source stage with parasitic capacitances

2.6.3.2 Frequency Compensation of Two-Stage Operational Amplifiers

The frequency compensation of a multi-stage op amp begins with the identification of all the poles associated with the various stages that constitute it. Considering the two-stage opamp presented in figure 2.17, it is possible to identify 3 poles, a pole per each output node of the gain stages, and an extra pole associated with the current mirror. The frequency of each pole can be approximately estimated by the RC time constant associated with each node, which is given by the equivalent resistance associated to the respective node and the capacitors connected from that node to ground.

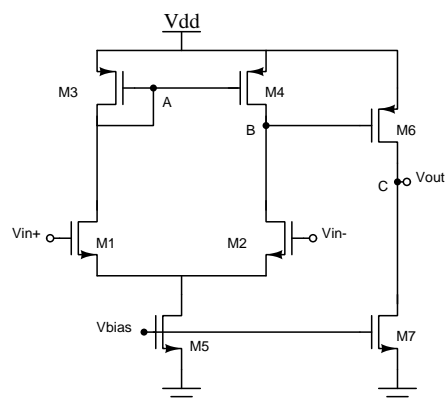


Figure 2.17: 2-stage Miller Opamp

The overall capacitors connected between the aforementioned nodes and ground and the small-signal resistances at each node, assuming that the transistors do not have body-to-drain parasitic

capacities, are given by,

$$C_A = C_{GS3} + C_{GS4} \quad (2.20a)$$

$$R_{eqA} = r_{o1} || r_{o3} || \frac{1}{gm_3} \quad (2.20b)$$

$$C_B = C_{GS6} + C_{GD6}(1 - A) \quad (2.20c)$$

$$R_{eqB} = r_{o2} || r_{o4} \quad (2.20d)$$

$$C_C = C_{load} + C_{GD7} \quad (2.20e)$$

$$R_{eqC} = r_{o6} || r_{o7} \quad (2.20f)$$

From this analysis it is possible to verify that if $1/gm_3 \ll r_{o1} || r_{o2}$, the pole associated with node A will be at high frequencies and the dominant poles of the amplifier will be the ones associated with nodes B and C, due to the large capacitor value at node B, originated by the Miller multiplication of C_{GD6} and the potentially high values of C_{load} that may be connected to node C.

Due to the relative difference in the frequency domain between the two dominant poles and the third pole, the negative phase shift due to the effect of the dominant poles may possibly lower the phase margin in such a way that it comes close to zero, making the system potentially unstable. The principle of frequency compensation for this topology is to move the dominant pole of the system towards lower frequencies. Considering the pole associated with node B to be the dominant before compensation, one way of lowering its frequency is by using a capacitor connected between nodes B and C. This capacitance will be multiplied by Miller effect, introducing a very-large capacitance at node B and moving the pole associated with this node closer to the origin. As an additional effect of adding the compensation capacitor, the pole associated with node C is moved away from the origin [27, p. 363] (pole splitting).

A drawback associated with this method is the possibility of C_{Load} being unknown or variable, which degrades the phase margin of the op amp if the non-dominant pole, associated with the output, is moved closer to the dominant pole due to a high output capacitance. The use of a compensation capacitor also introduces a right-half plane zero at low frequencies, which contributes to a degradation of 90° in the phase of the opamp, further reducing the phase margin of the system and potentially turning it unstable. This right-half plane zero derives from the feedforward formed by the compensation capacitor. Considering the topology in 2.17, the right-half plane zero can be moved to very high frequencies if the compensation capacitor only conducts current from the output to node B but not in the opposite direction [27, p. 369]. This behaviour can be imposed by using a source-follower in series with the compensation capacitor, as seen in figure 2.18, if the gate-source capacitance of this transistor has a value much inferior to that of the compensation capacitor.

Another possibility for removing the right-half plane zero is to move it in frequency and ideally make it so that it goes to a frequency in the left-half plane. In this case it can be used to cancel one of the non-dominant poles of the opamp. One way of doing this is by placing a resistor in

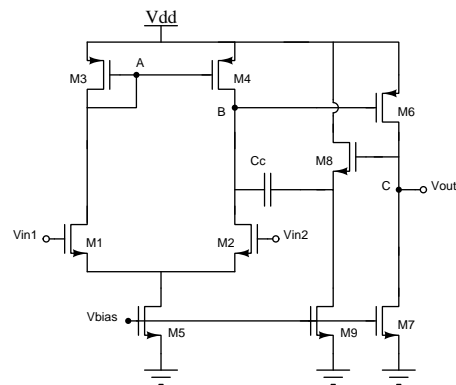


Figure 2.18: 2-stage Miller Opamp with a source follower in series with the compensation capacitor

series with the compensation capacitor, usually implemented by a transistor in the triode region as depicted in 2.19. In this case the frequency of the zero will be approximately given by

$$\omega_z = \frac{1}{C_c \left(\frac{1}{gm_6} - R_c \right)} \quad (2.21)$$

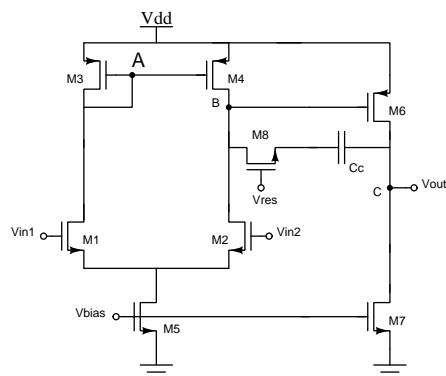


Figure 2.19: 2-stage Miller Opamp with transistor in triode in series with the compensation capacitor

2.6.4 Single-ended Amplifiers vs Fully-differential Amplifiers

Another important analysis to be done, during the design of operational amplifiers, is to decide if the configuration at the output should be single-ended or differential. As referred earlier, the input stage of an operational amplifier is always a differential pair and this stage possesses two outputs that have the same magnitude but a 180° phase difference between them, under the assumption that the differential stage is completely symmetrical. In spite of this, the most common operational amplifier topologies are single-ended, presenting a differential input and a single-ended output. A symbol representation of this topology can be seen in figure 2.20.

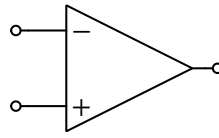


Figure 2.20: Symbol representation of a single-ended opamp

The use of opamps with differential outputs, figure 2.21, brings, however, advantages when compared with single-ended topologies. Some of these advantages concern the avoidance of mirror poles that are introduced by differential to single-ended conversion, leading to higher closed-loop speed, greater swings at the output of the differential pair and the cancellation of even-order harmonics [27, chap. 9]. A disadvantage is the need for common-mode feedback in high-gain fully-differential amplifiers when using technologies with complementary transistors. The output common-mode level in these topologies is sensitive to the properties of the transistors and possible mismatches, and cannot be resolved by the negative differential feedback.

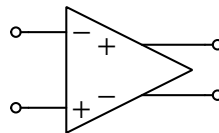


Figure 2.21: Symbol representation of a fully-differential opamp

2.6.4.1 Common-Mode Feedback

The purpose of common-mode feedback is to sense the common-mode levels of the two outputs of a fully differential amplifier and adjust the bias currents of the differential stage in order to control the common-mode level of the outputs, so that none of stages of the amplifier saturates when negative differential feedback is applied to the circuit. A generic scheme of a common-mode feedback network is presented in figure 2.22.

The task of CMFB can be divided in three operations:

- sensing of the common-mode level at the differential outputs
- comparison with a reference
- feedback of the error to the amplifiers biasing network

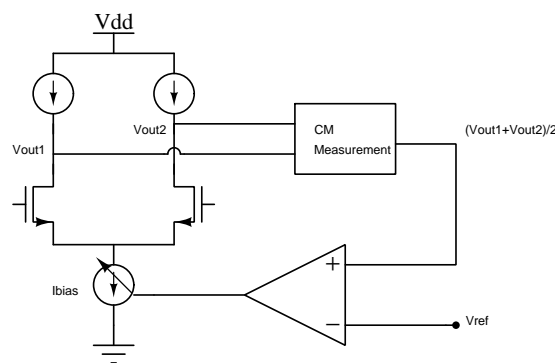


Figure 2.22: Generic representation of a CMFB topology

There are various ways of sensing the common-mode (CM) level at the outputs and of carrying out the comparison of this level with a reference. It is up to the circuit designer to define and employ a CMFB topology that can better suit the configuration of the differential amplifier used and of course the circuit in which the amplifier is to be applied.

In particular, the CM sensing method has a great influence on the performance of the amplifier's differential loop because the sensing scheme loads the output of the stage at which the CM level is being measured. Typically the sensing of the CM level is done with:

- Resistors
- Transistors in triode
- Source-followers
- Capacitors

Simple examples for these sensing schemes are shown in figure 2.23.

Analysing the different topologies presented above the following conclusions can be taken:

- Using resistors the load impedance of the differential amplifier is altered and the differential gain is potentially hindered.
- The use of transistors in triode introduce non-linearity because their *on* resistance depends on the mobility of charge carriers in the channel.
- Employing source followers also affects the linearity of the CMFB network and introduces extra poles in the system.
- Sensing the common-mode level through capacitors does not affect the differential gain but lowers the frequency of the poles present at the output node. Still, it is a highly linear method and in regular IC design the capacitors can be fabricated with great accuracy, leading to low matching errors.

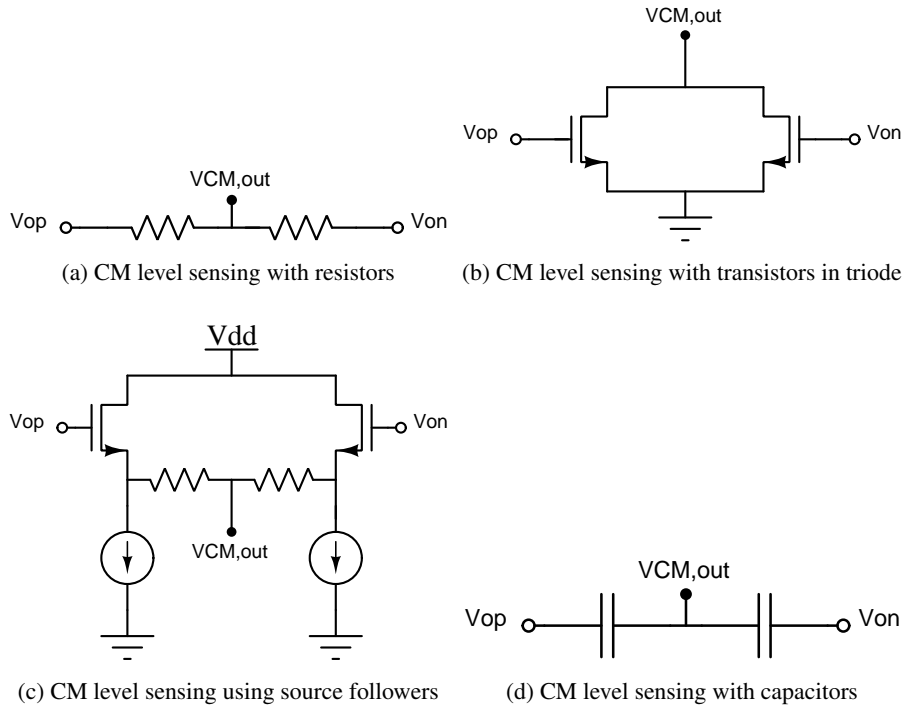


Figure 2.23: Common configurations used to sense the CM level at the output of a fully-differential amplifier

It is important to emphasize that there are two types of common-mode feedback networks, switched or continuous. Switched CMFB networks use capacitors to sense the CM level and are typically employed in switched capacitor circuits. Continuous networks are typically employed in continuous applications and tend to use the other sensing methods referred.

Regarding the operation of the two different types of networks it is easy to deduce that in the case of a continuous network the measurement of the CM level is carried out continuously. The principle of the switched-capacitor networks is however partially different. This is so because in these types of networks the sensing of the CM level and respective comparison to a reference voltage are implemented only through the use of sensing capacitors which are precharged to a reference voltage [34].

This principle can be demonstrated by the following example. Consider the simple capacitor sensing pair depicted in figure 2.23d. In one clock phase both capacitors will be precharged to a reference voltage, V_{ref} . An illustration of the state of the system in this clock phase is shown in figure 2.24a. In the other phase of the clock the CM level will be sensed by the capacitors that are connected to nodes V_{op} and V_{on} , which represent the differential outputs of the opamp. Then, voltage V_b , which represents the output of the common-mode feedback circuit and also the bias voltage to be applied to the biasing network of the opamp, is obtained by:

$$V_b = \frac{C_1 V_{C1} + C_2 V_{C2}}{C_1 + C_2} \quad (2.22)$$

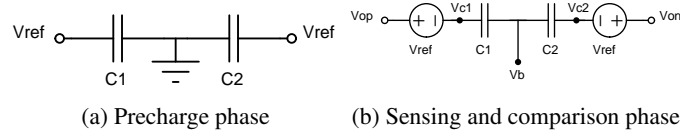


Figure 2.24: Operation principle of a switched-capacitor CMFB network

Considering that in this last clock phase the voltages V_{C1} and V_{C2} correspond respectively to the voltages V_{op} and V_{on} level-shifted by V_{ref} , determined as $V_{C1} = V_{op} - V_{ref}$ and $V_{C2} = V_{on} - V_{ref}$, equation 2.22 then becomes:

$$V_b = \frac{V_{op} + V_{on}}{2} - V_{ref} \quad (2.23)$$

Looking closely at the previous equation we see that the term $(V_{op} + V_{on})/2$ corresponds to the common-mode voltage at the output of the opamp and that it is being compared to the reference voltage. Thus, if the reference voltage is correctly defined as $V_{cmref} - V_{bias}$, where V_{cmref} is the desired common-mode voltage at the output, and V_{bias} is the voltage that when applied to the biasing network guarantees the desired common-mode level at the output, the switched-capacitor CMFB network will function as expected and will impose the desired CM voltage at the output when it reaches steady-state.

2.6.5 Switched Operational Amplifier

The final concept summarized in this theoretical background is the switched opamp technique, which is employed in one of the novel topologies proposed in this work. Being first introduced by Crols and Steyaert in 1994 [8], this technique is mainly used in low-power IC design. As the name might already imply, a switched operational amplifier is in short an operational amplifier in which at least part of the circuit is switched off in one of the clock phases. For this reason, it is exclusively employed in switched capacitor configurations. The motivation behind the proposal of this technique was the need for circuits that could operate at very low supply voltages and that would also decrease overall power consumption. Until the proposal of this technique there were only two ways of implementing switched-capacitor IC's with very low supply voltages, either through the use of transistors with low threshold voltage or with on-chip voltage boosters. The former option is expensive [9] and the latter may cause reliability problems in the long run because of the maximum allowed voltage being exceeded [35].

In terms of implementation a switched opamp is in its core a regular opamp with the addition of internal switches that are used to turn-off all or some of the biasing currents in the circuit during the clock phase where the amplifier is not required. It is important to note that the output stage must always be turned off during this phase to put the output in a high impedance state and therefore avoid the discharge of capacitors connected to this node. The number of stages disabled during the off-phase, the levels of voltage imposed at the output when the amplifier is turned off and the

switching schemes employed are determined in CMOS by the minimum turn-on speed desired, power-consumption requirements and by the topology employed in the core amplifier itself.

An example of an application where this technique can be employed is the Sample-and-Hold because the opamp is only required during the holding phase and can be partially or completely turned-off during the sampling phase.

2.7 Summary

In this chapter an overview was given on the characteristics of the a-GIZO TFT from the materials to its internal characteristics and limitations when compared to well know silicon based technologies. This overview is instrumental in the comprehension of many of the topologies used throughout this work, as the design of the topologies presented in chapters 4 and 5 is greatly conditioned by the specific characteristics of the a-GIZO TFT technology used.

Along with an overview on a-GIZO TFT a set of concepts regarding the design of operational amplifiers is also given. These concepts are intended to help the understanding of developed topologies, as some of them are not commonly used in typical operational amplifier designs. For this reason, relevance is given to the concepts of fully-differential opamps, common-mode feedback, design of high-gain stages with only n-type enhancement transistors and switched operational amplifiers, all of which play an important part on the opamp topologies presented in later chapters of this document.

Chapter 3

Bibliographic Review

In this chapter an assessment on the current state of operational amplifiers with single type transistors on TFT technologies, with characteristics similar to the ones of a-GIZO, is presented, along with the review of some old articles related to the design of high-gain operational amplifiers in technologies with only n-type transistors. Finally, the state of the art regarding switch operational amplifiers is summarised.

The atypical structure of this bibliographic review is justified by the fact that although a non negligible number of circuit implementations, with a-GIZO TFTs, does exist, these implementations are mainly for digital circuits. Also, to the knowledge of the author, to date no operational amplifier has ever been built with a-GIZO TFTs. This fact, plus the limitations associated with a-GIZO TFT technology, presented in 2.5, motivates a review on amplifier design with solely n-type transistors. The exploration of this subject was done mainly during the 70's because CMOS technology was not yet fully matured as it is today. Although some of these techniques are now obsolete for MOSFET technologies, they are of great importance to the design of opamps with a-GIZO TFTs, because for now p-type devices are not yet viable for circuit implementation. The state of the art on switched opamps is presented because one of the topologies developed is of this kind.

The state of the art in circuits with a-GIZO TFT is however included in appendix F to give the reader an overview on the circuits implemented to date with this technology even if it is not directly related with the work presented in this Thesis.

3.1 High gain Operational Amplifier Implementations with only n-type enhancement transistors

The research in the design of operational amplifiers with only n-type enhancement transistors was explored in the 70's and in the 80's for NMOS. Along this period, several different techniques of achieving high gain and of realizing frequency compensation in opamps with only n-type enhancement transistors were proposed. Facing the limitation of not possessing complementary devices in a-GIZO TFT technology, it is important now to analyse the work done previously in the field

of n-type amplifiers, in order to be able to establish a background for opamp design with a-GIZO TFTs.

In 1976 Tsividis and Gray [2] reported an NMOS operational amplifier designed to drive capacitive loads of 50pF, with fast settling. A block diagram and the complete schematic of this amplifier are presented in figures 3.1 and 3.2, respectively. In the reported operational amplifier, the voltage gain is achieved by making the drive transistors much wider than the diode connected n-type enhancement mode transistors used as active loads, which leads to a bigger area consumption, bigger input capacitances in the drive transistors and does not give a very significant gain per stage. Nonetheless, voltage gain was not the main objective in this design but rather the settling time of the circuit when driving capacitive loads. Many techniques were employed to improve the amplifiers frequency response. The first of which is the cascode stage that is connected to the output of the differential to single-ended converter stage in order to decrease the load capacitance seen by this stage, which otherwise would be big due to Miller effect and would degrade the overall frequency response of the opamp. Other examples of design techniques used to improve the frequency response of this circuit are the source follower applied to drive the output stage, which isolates the input capacitance of the output stage from the cascode stage, and the shunt-shunt feedback topology used at the output stage to reduce the overall output resistance of the amplifier, with the purpose of increasing the frequency of the pole associated with the output when driving capacitive loads. The most relevant frequency compensation technique employed in this opamp was, however, the compensation capacitor applied between the output of the differential to single-ended converter stage, and the output of the cascode formed by M20 and M19. This capacitor is multiplied by Miller effect to set the dominant pole of the opamp. Another interesting aspect of this compensation scheme is the source-follower M13 that is connected in series between the output of the cascode stage and the compensation capacitor. This source follower is used to shift the right-half plane zero introduced by the compensation capacitor, to high frequencies, since the capacitance at the gate of the source follower is expected to be much smaller than that of the compensation capacitor. If this right-half plane zero was not shifted to high frequencies, the phase of the amplifier would be decreased by 90° affecting the phase margin of the system. The proposed amplifier is reported as having a 51 dB low-frequency gain, a 70 dB CMRR and a unity-gain frequency of 5MHz.

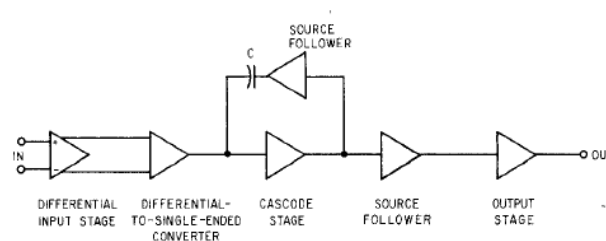


Figure 3.1: Block diagram of the internally compensated NMOS opamp reported by Tsividis and Gray in 1976, reprinted from [2]

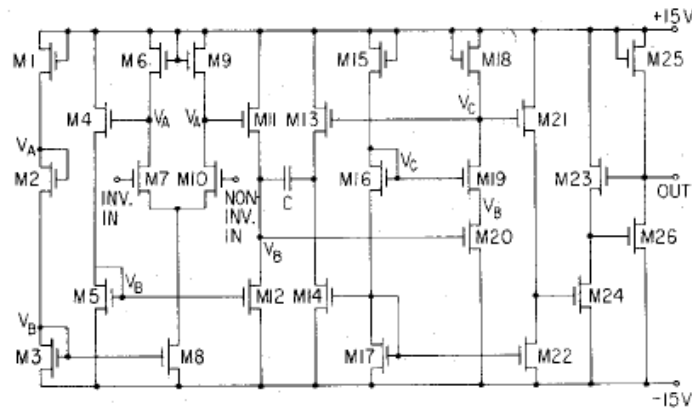


Figure 3.2: Complete schematic of the internally compensated NMOS opamp reported by Tsividis and Gray in 1976, reprinted from [2]

In 1979 Young [3] presented another operational amplifier with only n-type enhancement type NMOS transistors. A block diagram and the complete schematic of this amplifier are presented in figures 3.3 and 3.4, respectively. The topology proposed in this work was similar in many aspects to the one presented previously by Tsividis and Gray [2]. The gain stages were also implemented with enhancement mode transistors, using the differences in the relative dimensions of W and L for the drive and load transistors to determine the voltage gain of the stages, with the topology of the output stage being the same as well. However, in this topology the frequency compensation scheme was implemented in a different way. This compensation scheme starts at the output nodes of the differential stage, the positive output is fed to a source follower, M9, and then to a high-gain stage that also inverts the signal. On the other hand, the negative output of the differential stage is applied to a source follower, M11, and then summed in phase to the other differential component in the output of the high-gain stage composed by transistors M12 and M11. Between the input and the output of this stage, a compensation capacitor is connected, which introduces a high capacitance at the gate of M12 due to Miller effect, determining the dominant pole of the amplifier and also introducing a right-half plane zero in the system. Each of the source followers used introduce a zero and a pole in the system as well. From this analysis, the author implemented a frequency compensation scheme by defining a value for the dominant pole associated with the compensation capacitor and for the V_{GS} voltages of the source followers M9 and M11 that try to place all the zeros of the system that occur below the unity gain crossover frequency, close to their matching pole in order to ensure pole-zero cancellation. For this amplifier, a low-frequency voltage gain of 66.84dB is reported, along with a CMRR of 72dB and a unity-gain frequency of 3MHz, achieved through the additional use of two-bypass capacitors in the source follower signal paths used to move the dominant zero, introduced by the compensation capacitor, to a frequency close to that of the second dominant pole. The reported low-frequency gain of this topology was very high but at the cost of area because it was achieved through manipulation of the aspect ratios of drive and load transistors in the gain stages. In addition, the frequency compensation scheme required the

use of extra capacitors and achieved a lower unity-frequency gain than the compensation scheme used by Tsividis and Gray, which was also considerably simpler.

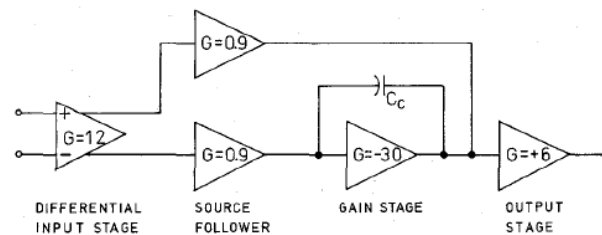


Figure 3.3: Block diagram of the NMOS opamp reported by Young in 1979, reprinted from [3]

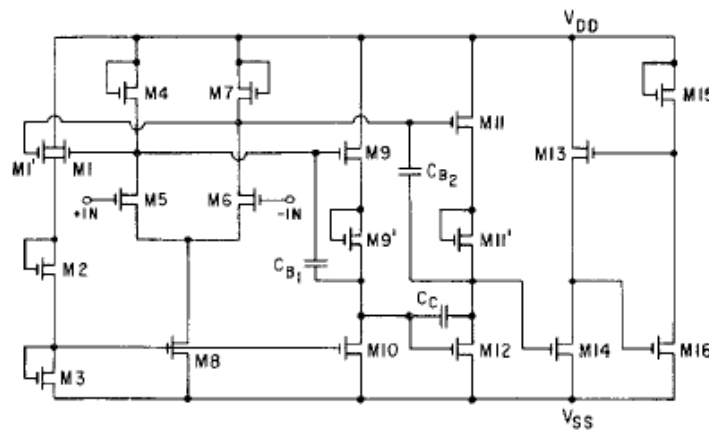


Figure 3.4: Complete schematic of the NMOS opamp reported by Young in 1979, reprinted from [3]

In the same year, Calzolari et al. [4] reported a high gain operational amplifier with only enhancement mode NMOS transistors that employed a new topology to achieve high gain based on the use of positive feedback at the load transistor of the gain stage. A complete schematic of this opamp is presented in figure 3.5. The high small-signal resistance is achieved in this topology by driving the gate of the enhancement mode load transistor with a bias voltage that has the signal at the source of the device superimposed. This way, the V_{GS} of this transistor is kept constant and the output impedance of the load is increased, becoming approximately equal to the transistor's intrinsic output resistance, as previously presented in 2.6.2. This concept is easy to implement in a differential pair because the outputs of this stage are 180° out of phase and each can be summed to the gate of the load transistor, of the opposite output, after being inverted through common-source amplifying stage with a gain magnitude of approximately one. The following stages of the amplifier were simply aimed at the differential to single ended conversion of the outputs of the differential stage, and to the reduction of the output resistance of the opamp. This work introduced a new way of achieving high gain with only n-type enhancement mode transistors without using the

manipulation of the aspect ratios between the drive and load devices in the amplifying stage. The proposed technique, however, leads to a dominant pole at the output of the differential pair due to the high small-signal resistance and the elevated capacitance in the node due to the feedback stage. This dominant pole was only compensated by connecting capacitances to these nodes in order to lower the frequency of the dominant pole. The reported low-frequency gain for this amplifier was 52dB which is very similar to the gain presented by the topology reported Tsividis and Gray in 1976 [2]. On the other hand, because the frequency compensation of the amplifier was not a main objective in this work, the unity-gain frequency achieved by the topology was considerably lower than the ones presented in the previous reports of NMOS amplifiers and therefore another compensation scheme would be required in order to increase the unity-gain frequency of this topology.

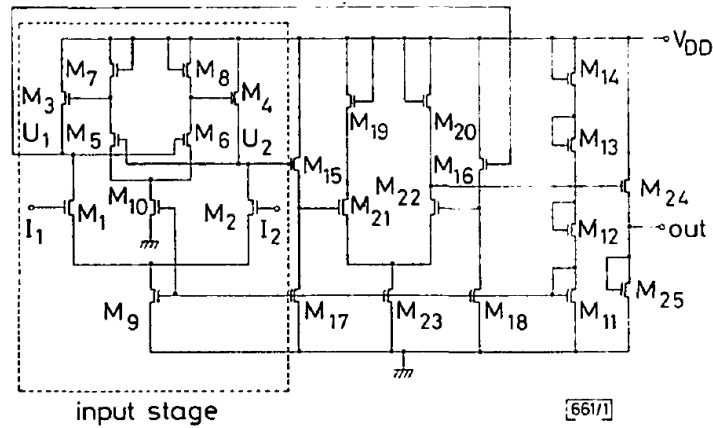


Figure 3.5: Complete schematic of the NMOS opamp reported by Calzolari et al. in 1979, reprinted from [4]

Since these proposals in the 70's the work in high-gain amplifier stages with only n-type enhancement transistors has not seen many developments, mainly due to the fact that they do not find much application in standard technology due to the superior performance of topologies implemented with complementary devices. However, because there are no complementary devices for TFT technologies, such as a-GIZO TFT, the development of high-gain topologies with a single type of transistor is again being researched. As a result of this, in the current year a new single-stage high-gain stage for technologies with only n-type enhancement transistors has been proposed by Bahubalindrani et al. [5]. Depicted in 3.6, the topology presented in this work is an improvement of the ac bootstrap inverter, previously discussed in 2.6.2. However here the ac bootstrapping technique is applied to a cascade configuration with the objective of further increasing the load impedance of the amplifier stage which for this topology can be estimated by

$$R_{load} = \frac{1}{gm(1 - Af) + \frac{2 \cdot (1 - Af) \cdot gm + gds}{gm} \cdot gds}, \quad (3.1)$$

where A_f is the gain of the feedback network.

The former equation considers that both of the transistors used in the load are biased in the same conditions, therefore presenting the same value for g_m and g_{ds} , and that both of the feedback networks have the same voltage gain.

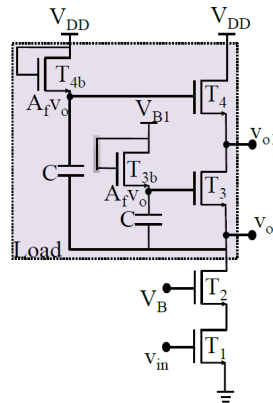


Figure 3.6: Schematic of the novel high-gain common-source stage with only n-type enhancement transistors proposed in 2013 by Bahubalindrani et al., reprinted from [5]

Here the positive feedback is introduced by the capacitors C that are connected between the gates of transistors T_3 and T_4 , respectively, and the output node. The biasing of these transistors being provided by T_{3b} and T_{4b} . As with the regular ac bootstrapped load, the load impedance will be higher for values of the capacitance C that are significantly higher to those of the parasitic capacitances of the transistors. The topology will be always stable because the gain of the network is always inferior to 1 and the amplification of dc components is not possible because of the high-pass filter used to implement bootstrapping.

The results obtained using a BSIM3V3 model for a $0.35\mu m$ NMOS technology show that this topology assures higher voltage when compared to the ones presented in 2.6.2 and that it has lower power consumption and a higher bandwidth when compared with the positive feedback topology in which the signal is fed back through a buffer.

3.2 Operational Amplifier Implementations in TFT technologies with characteristics similar to a-GIZO

The design of mixed signal electronics in TFT technologies has been one of the main objectives since these technologies first appeared, especially for the integration *on chip* of sensors with signal processing electronics. This necessity has already led to the development of a few operational amplifier topologies in other TFT technologies such as a-Si:H TFT and pentacene-based dual-gate organic TFT, both of which also present characteristics and limitations that are to some extent

similar to the ones of a-GIZO TFT, making the analysis of these topologies important for the work of this dissertation.

In 2010 Tarn et al. [6] reported an a-Si:H Operational Amplifier designed with only n-type enhancement TFTs that was used in a unity-gain buffer for a 4-bit DAC by short circuiting the opamp's output to its negative input. Just like a-GIZO TFT, a-Si:H TFT also possesses an amorphous structure in the semiconductor layer and presents a shift over time in the threshold voltage, when a constant bias is applied to its gate. In this technology there are no p-type devices as with the a-GIZO TFT technology. The proposed amplifier uses exactly the same topology in the input stage as the topology presented by Calzolari et al. [4] in 1979 for a high-gain NMOS operational amplifier, in which positive feedback is used to increase the impedance of the enhancement mode device used as an active load in the differential stage. The overall amplifier topology is relatively simple and beyond the differential stage at the input, and the feedback stage used to increase the equivalent load resistance of the former stage, only a simple differential-to-single ended stage is used to sum both of the differential components and to serve as the output stage of the opamp. However, a new concept is introduced in this work related to a design technique aimed at increasing the operational lifetime of the amplifiers using n-type transistors that exhibit a shift in V_{th} . The proposed approach consists in dimensioning the biasing transistor, M10, of the differential pair that constitutes the feedback network, so that it is approximately 2 times wider than the diode connected enhancement TFTs, M8 and M9, that serve as active loads for the feedback stage. This way, the shift in the threshold voltages of the biasing TFT and of each of the load TFTs can approximately cancel each other. For example, considering node V_P on the schematic presented in 3.7, if all transistors are assumed as biased in saturation and if the channel modulation of the transistors is neglected, the voltage shift in this node due to the shift of the V_{th} of both M8 and M10, which are biased by a constant gate voltage, is given by

$$\Delta V_P = -\sqrt{\frac{\left(\frac{W_{10}}{L_{10}}\right)}{2\left(\frac{W_8}{L_8}\right)}} \cdot \Delta V_{th10} + \Delta V_{th8} \quad (3.2)$$

From this last equation it's possible to conclude that if $W_{10} = 2W_8$, with both TFTs having the same channel length and a similar variation in V_{th} , the shifts in the threshold voltages will cancel each other.

This amplifier had a reported gain of 42.5dB and a unity-gain frequency of 30kHz. The former parameter is significant considering the low transconductance of a-Si:H TFTs and the utilization of only two gain stages. The later can be explained by the small-frequency pole associated to the outputs of the differential stage, because of the extra capacitances introduced by the feedback network, and the increased small-signal resistance achieved through the use of the feedback topology on the load TFT.

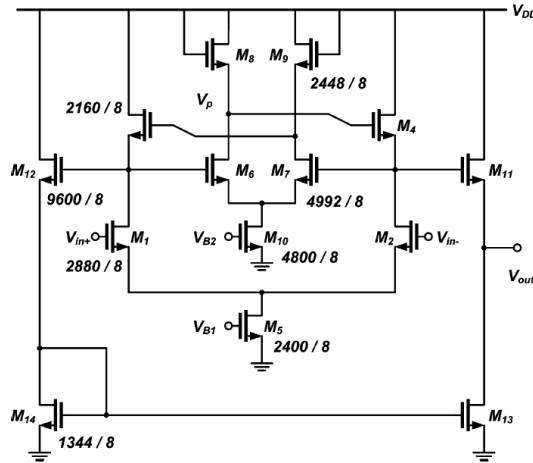


Figure 3.7: Complete schematic of the a-Si:H NTFT Operational Amplifier proposed by Tarn et al. in 2010, reprinted from [6]

In 2011 Marien et al. [7] proposed a single stage fully-differential opamp in p-type pentacene-based dual-gate organic thin-film transistors, using bootstrapped gain-enhancement. This technology can also be implemented in flexible substrates, for the time being no complementary devices are available, so the circuits implemented only use p-type TFTs that have hole mobilities in the range of 0.1 to $1\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, similar to the electron mobilities of n-type a-Si:H TFTs, and the devices also present a shift in the threshold voltage due to carrier trapping in the interface between the gate dielectric and the semiconductor. A schematic of the proposed operational amplifier is presented in figure 3.8. The proposed opamp was designed with high-gain as its main goal, and with the reduction of the V_{th} sensitivity as the secondary objective. In order to achieve high gain, positive feedback is introduced in the load TFTs through the use of high-pass filter with very low 3 dB frequency from source to gate. This filter is composed by a capacitor in series with a resistor implemented by the M5 TFT, which is in deep cut-off region. This topology leads to an increase in the gain of the configuration by increasing the load impedance of the differential stage. In terms of the reducing insensitivity to V_{th} , the transistors that do not influence the low-frequency gain are biased in saturation, with high $V_{sg} - V_{th}$, but the same technique cannot be used in the M3 transistors that are the drive transistors of the input stage. These transistors require a small $V_{sg} - V_{th}$ in order to maximize their gm/I_{DS} ratio and consequently maximize the voltage gain of the differential stage. The compensation technique used for these transistors assumes that both of the transistors M3 suffer the same shift in V_{th} . The resulting effect is equivalent to a shift in the common-mode voltage and therefore can be compensated through the use of common-mode feedback, which is done with transistors M1 both operated in the linear region and with M2 that is used to give a slight increase in the CMFB loop gain. The reported values of small-signal gain and unity-gain frequency for this topology are respectively 15dB and 10kHz for OTFTs using a dual-gate structure. These values are conditioned by both the transconductance and parasitic

capacitance of the transistors used.

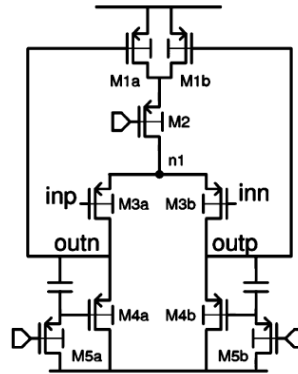


Figure 3.8: Complete schematic of the single stage opamp in p-type pentacene-based dual-gate organic thin-film transistors using bootstrapped gain-enhancement, proposed by Marien et al. in 2011, reprinted from [7]

3.3 Switched Operational Amplifiers

The use of switched operational amplifiers was first introduced in the mid-nineties and since then has been applied in various structures of operational amplifier with the most common of these structures being the two-stage Miller opamp. Today this type of opamp is still widely used due to the constant scaling-down of the semiconductor technologies and the necessity of using ever-decreasing supply voltages.

It is important to note however that, at least to the authors knowledge, there are no implementations of switched opamps in TFT technologies that only have a single type of device. Therefore all of the work revised in this section was implemented in CMOS technologies being presented to offer a more detailed context on how switched opamps are implemented in commonly used analog IC design technologies.

The precursors of the entire switched opamp concept were Crols and Steyart who introduced the first implementation of a switched opamp amplifier in 1994 [8]. The topology presented in this work, depicted in figure 3.9, was applied to a single-ended two-stage Miller opamp where in the turn-off phase all of the stages are disabled.

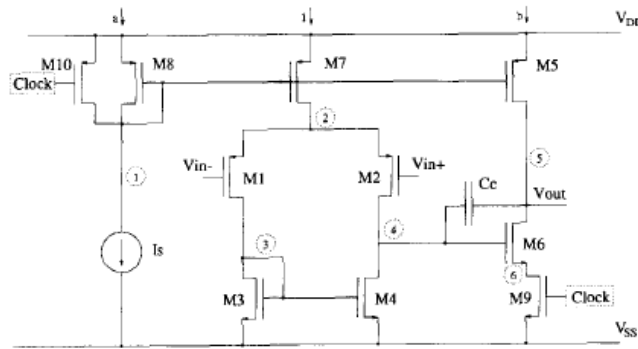


Figure 3.9: Complete schematic of the Switched opamp presented by Crols and Steyaert in 1994, reprinted from [8]

The proposed topology worked with a power supply voltage of 1.5V with the input and output common-mode levels equal and defined as 0.425V and with it a low-Q biquad filter, shown in figure was implemented. The implemented filter was shown to have a total harmonic distortion of -64dB for a output swing of $550mV_{pp}$. Also as an additional performance advantage it is stated that the overall power consumption was reduce to 75% when compare to the one attained if the amplifier were to be always active.

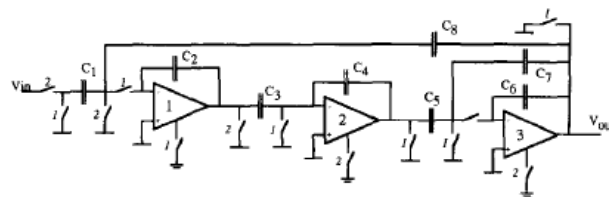


Figure 3.10: Schematic of the low-Q biquad filter with switched opamp presented by Crols and Steyaert in 1994, reprinted from [8]

As precursors of switched opamp techniques, the authors also established many principles that still serve to this day as the foundations of the entire switched opamp theory. Of these concepts the most important is maybe the one that states that a switched opamp technique can be applied in every switched capacitor circuit in which every switch is connected either to the output of the OTA (operational transconductance amplifier) or to a reference voltage. This property showed that the switched opamp could have a wide range of applications because it means that good number of switched capacitor circuits can be adapted into an equivalent circuit that uses an opamp of this type.

Three years later, in 1997, Baschirotto and Castello proposed a different approached for the realization of a switched opamp. The main difference between this topology and the one previously presented is the use of a fully-differential output and of a common-mode feedback circuit, which is necessary since the opamp was implemented in CMOS. Other alterations proposed in this

work were aimed at the increase of swing levels and at the reduction of the turn on-time of the circuit. The swing levels were increased using different common-mode voltages for the input and output, which were set at Gnd and $V_{dd}/2$ and lead to a lower minimum supply voltage than the one attained in the previous work, while enabling at the same time a rail-to-rail output swing when combined with the use of a folded structure at the input stage. The reduction in turn-on time was achieved by only turning-off the output stage and by opening the connection of the compensation capacitors to the input stage during the turn-off phase so as to keep these capacitors charged. An image of the complete topology proposed in this work can be seen in figure 3.11.

With this amplifier a switched-capacitor filter using a 1V supply was implemented in a $0.5\mu\text{m}$ CMOS topology, presenting a power consumption of $160\mu\text{W}$. This filter could be operated with a 1.8MHz frequency and according to the authors it would still be operational with supply voltages as low as 0.9V.

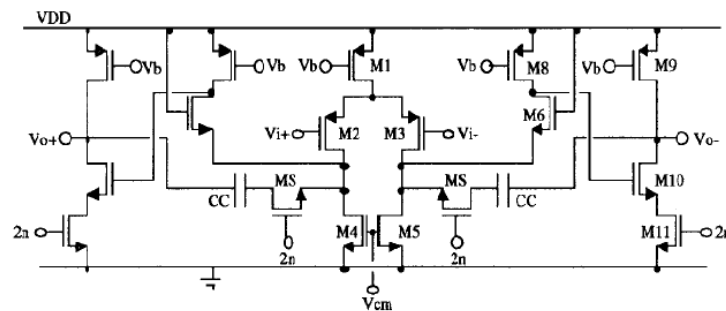


Figure 3.11: Complete schematic of the switched opamp proposed in 1997 by Baschirotto and Castello, reprinted from [9]

In the following year Waltari and Halonen introduced in switched opamps the concept of using the common-mode feedback network to also speed up the turn-on of the operational amplifier as well as setting the CM-level at the output [10]. Another interesting characteristic of this topology is the use of a cross-couple load in the input stage, which eliminates the necessity of including another CMFB circuit for the first stage of the amplifier. The cross-coupled load presents a high resistance for differential signals but a low resistance for common-mode components, which guarantees for this topology that the rejection of common-mode disturbances will be considerable in the input stage. The authors used this property to apply CMFB only to the output stage which makes the CM loop simpler and with lesser poles leading to a faster settling of the CM-level at the output of the opamp. In this way the need for signal inversion in the CM loop is also avoided making the implementation of this network with passive components possible.

The complete amplifier topology is presented in figure 3.12. From the analysis of the remaining topology it is possible to see that, apart from the details discussed above, this topology has many common aspects with that proposed by Baschirotto and Castello 3.11. A folded cascode structure is also used in the input stage, only the output stage is turned-off and the compensation

capacitor has a series switch to ensure that it stays charged during the phase where the amplifier is turned-off, which, as seen in the previous work, is a way of increasing the overall turn-on speed of the circuit.

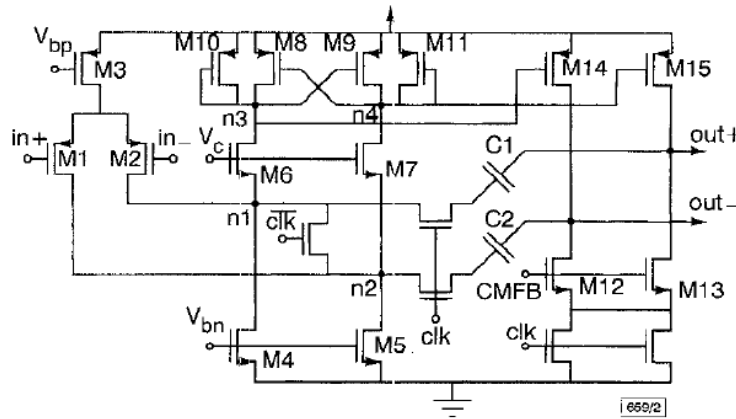


Figure 3.12: Complete schematic of the switched opamp proposed in 1998 by Waltari and Halonen, reprinted from [10]

The common-mode circuit proposed in this work is depicted in figure 3.13. This circuit as four capacitors C1-4, three of which, C1-3, must be of the same value for proper functioning of the circuit because these are the capacitors involved in the measurement and comparison to the reference level of the CM voltage at the outputs. The sensing and comparison operation for the CM level can be summarized in the following way. During the amplifier's off phase C1 and C2 are charged to Vdd because the output of the opamp is railed to this level and n0 is pulled to ground using a switch. In the same phase C3 is reset as both of its terminal are connected to ground. When the amplifier is turned on C3's top plate will be connected to Vdd and the top plates of C1 and C2, which remain connected to the differential outputs of the amplifier, will tend towards Vdd/2. Therefore when steady state is reached the voltage at node n0 will be ideally equal to ground as half of the charge stored in C1 and C2 during the off-phase is used in the on phase to charge C3 to Vdd. The remaining capacitor, C4, is used as a level shifter in order to apply a voltage with an adequate dc level to the active load of the output stage, which is implemented with a NMOS transistor. This level shift capacitor is precharged during the amplifiers off phase using a replica of the current source present in the amplifiers output stage. So, when steady state is reached the voltage applied to the active loads of the output stage is equal to the reference voltage at which C4 was precharged, which means that the circuit maintains the same operation principle of a switched capacitor CMFB network, previously presented in 2.6.4.1 but adapted into the specific context of switched opamps.

In terms of measured characteristics it is only mentioned that the opamp can work with a 1V supply. However the specific technology used for the implementation is not stated.

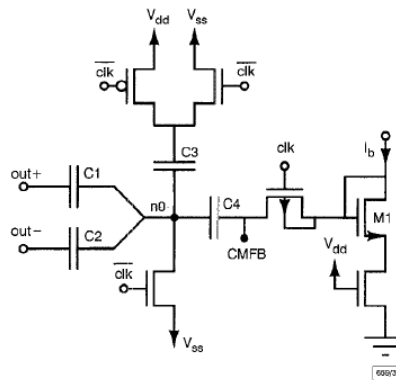


Figure 3.13: Schematic of the SCCMFB network proposed in 1998 by Waltari and Halonen for their switched opamp, reprinted from [10]

More recently, in 2008, Qin et al. presented an improvement proposal for the switched opamp presented above [11].

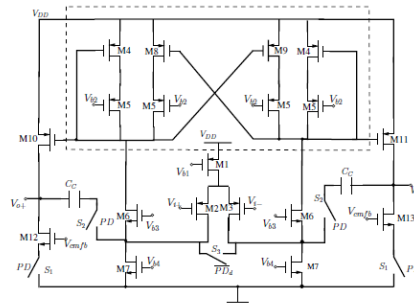


Figure 3.14: Schematic of the switched opamp proposed in 2008 by Qin et al., reprinted from [11]

Depicted in figure 3.14, this topology employs most of the characteristics that had been introduced in the fully-differential switched opamps presented in [9] and in [10], such as the use of different common-mode voltages for the input and output of the circuit, set as ground and $V_{dd}/2$ respectively, the switch in series with the compensation capacitor and the use of a folded cascode structure in the input stage with a cross-coupled load, albeit this time presenting a cascode structure. However, as a distinctive feature, this topology used a revised version of the CMFB circuit proposed in the work of Watari and Halonen. This CMFB circuit, depicted in figure 3.15, is based on the previous implementation proposed by the other authors but with the addition of an extra nonlinear amplifier to the loop. This extra component increases the voltage gain in the CMFB loop and provides a larger discharge current for the output stage of the amplifier during turn-on, consequently reducing the overall turn-on time of the opamp.

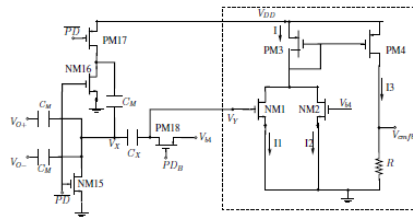


Figure 3.15: Schematic of the CMFB loop proposed by Qin et al. for their switched opamp, reprinted from [11]

With this opamp a sample-and-hold operating at 1V was implemented in a $0.18\mu\text{m}$ CMOS technology. This circuit is said to achieve 50MSPS (mega samples per second) with a THD (total harmonic distortion) of -76dB and a SFDR (spurious-free dynamic range) of 76dB over the entire Nyquist Rate. The topology for the sample-and-hold is presented in figure 3.16 and as it can be seen that the output of the circuit is not taken at the output of the amplifier but in the opposite plate of the feedback capacitor. The selection of this point for the output is justified by the fact that in this way a loading free architecture can be implemented using the feedback capacitor of the sample-and-hold to serve as the input capacitor for another circuit. An approach that makes perfect sense considering that a sample-and-hold is always used as a part of a larger signal processing chain like, for example, an ADC (analog-to-digital converter).

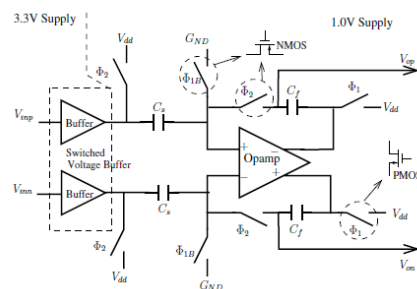


Figure 3.16: Schematic of the sample and hold implemented by Qin et al. using their switched opamp, reprinted from [11]

In terms of its operation the circuit is configured to accommodate the existence of different common-mode voltages at the input and output of the amplifier during its active phase as well as the setting of the voltages in these terminals to Gnd and Vdd, respectively, during turn-off. The opamp is turned-off during the sampling phase because in the holding phase the amplifier must be active for there to be transfer of charge from the sampling to the hold capacitor. The equations for

the charge and holding phases are respectively

$$Q_S = (V_{in} - gnd).C_s + (V_{dd} - gnd).C_f \quad (3.3a)$$

$$Q_H = (V_{dd} - gnd).C_s + (V_{out} - gnd).C_f \quad (3.3b)$$

Since the input signal and the output voltage of the amplifier in the holding are defined as $V_{in} = V_{dd}/2 + v_{signal}$ and $V_{out} = V_{dd}/2 + v_{signal}$, Q_S and Q_H will be equal ensuring the correct operation of the sample and hold configuration.

3.4 Summary

In this chapter a review of the state of the art is given for opamps with only n-type enhancement transistors, opamps with TFT technologies that have a single type of transistor and switched operational amplifiers. No review is given on previous opamps with a-GIZO TFTs as there are none reported to this date, which also constitutes the reason for the review of operational amplifiers in technologies with similar characteristics. The bibliographic review on switched opamps is presented to better contextualize the introduction of this concept to the design of operational amplifiers with a-GIZO TFTs presented in chapter 5, as although the developed switched opamp is fairly different to those that currently exist for CMOS, many of concepts presented in work here reviewed were employed or adapted in the work carried out in the present thesis.

Chapter 4

Development of the a-GIZO TFT Operational Amplifier

This chapter presents the detailed description of the design of the a-GIZO TFT operational amplifier and the respective results obtained from the simulation of the proposed topology.

Before detailing the design process of the operational amplifier it is very important to highlight both the methodology and performance goals that were defined for this work. These two steps are of paramount importance because the overall approach taken in the design process helps contextualize the majority of the decisions taken.

4.1 Methodology

To define the methodology the first thing that needs to be kept in mind is that working with a technology that is still in a research phase will always result in a great component of exploratory work. This last fact becomes even more apparent when all the limitations associated with the technology are considered, especially due to the fact that the simulation model used for the TFT is itself still not a completed work, as it does not characterize the intrinsic capacitances of a-GIZO TFTs. For this reason great care was taken in the definition of the methodology in order to ensure that results and conclusions could already be taken from simulation, at least to some extent. In this way the work developed could be partially validated through simulation instead of becoming exclusivity dependent on the results taken from fabricated circuits.

Taking these factors into account the decision was made on using both the a-GIZO TFT model and that of a commercial NMOS technology. Therefore all of the topologies developed were also implemented and simulated using a BSIM3V3 model in $0.35\mu\text{m}$ technology. An accurate model for MOSFET simulation can be used to validate the developed topologies since in terms of operation principle our device is also a field effect transistor and has been proven to present a drain current characteristic that can be approximated with a reasonable accuracy using the level 1 MOSFET equations. Still, in order to try and replicate the behaviour of circuits with a-GIZO

TFTs, the following precautions were taken in order to ensure that the circuits implemented in NMOS operate under similar conditions:

- Only n-type enhancement transistors were used because this is the only type available in the a-GIZO TFT technology.
- The body-effect was mitigated by connecting the body to the source in all NMOS transistors as there is no body effect in TFTs.
- Wide transistors were used to avoid narrow and short channel effects.

The rest of the design methodology was similar to that of a typical IC design and involved the conceptual study of the topologies employed, performing appropriate simulations for the developed circuits, optimization of these circuits according to a set of performance goals and finally the production of their layout so that they could be fabricated and validated through physical characterization.

After this process the next step taken was the definition of the preliminary performance goals for the amplifier. This process took into account the objectives of the Master Thesis but also the limitations of the technology that were known at the beginning of the design process so that the objectives defined could be met.

4.2 Performance Goals

The first step in this stage was to select the context in which the amplifier was to be applied. A first decision was then made to have generic switched capacitor circuits as the target application for the opamp because in a-GIZO TFTs the ratio between g_{ds} and g_m is much smaller than the one typically encountered in MOSFETs. This implies that even a topology with an output impedance of $1/g_m$ would present significant output impedance. In fact, from the simulations performed, the typical g_m values for the a-GIZO TFTs used were found to be in the order of some tens of $\mu A/V$. Consequently $1/g_m$ would easily reach several tens of $k\Omega$ which in practical terms translates in a necessity of using very high values of resistors in the feedback network so as not to significantly diminish to open loop gain of the opamp. In switched capacitor circuits however, there is no resistive loading of the amplifier which makes them a more suitable application for an opamp designed in this technology due to the limitations regarding the implementation of gain stages. Still, the capacitors in the feedback network will provide capacitive loading at the output which must be taken into account in the stability analysis of the opamp.

With the selection of switched capacitor circuits as the target application a generic analysis regarding these circuits was made in order to identify the common performance goals that should be met by an opamp employed in these types of circuits.

In switched capacitor applications speed and accuracy are two very important performance parameters. Both of which are affected by characteristics of the opamp used, namely its voltage gain and gain–bandwidth product. The latter characteristic influences the settling time of a switched

capacitor circuit, which will tend to be smaller for higher values of gain-bandwidth product. On the other hand, the voltage gain of the opamp is directly related to the accuracy of the steady state value. To comprehend this effect let us briefly analyse the static error that occurs when a voltage step with amplitude V_{step} is applied to the input of the opamp. In a real opamp with finite voltage gain, A_{ol} , the static error will be given by

$$\epsilon_s = \frac{V_{step}/\beta - V_{out}}{V_{step}/\beta} = 1 - \frac{\beta A_{ol}}{1 + \beta A_{ol}}, \quad (4.1)$$

where β is the feedback factor and A_{ol} is the amplifier's open loop gain. Assuming that $\beta A_{ol} \gg 1$ the previous expression can be further simplified to

$$\epsilon_s = \frac{1}{\beta A_{ol}} \quad (4.2)$$

Ultimately the maximum acceptable tolerance in the static error determines the minimum open loop gain required for the op amp which is directly obtained by manipulating equation 4.2.

$$A_{ol} = \frac{1}{\beta \epsilon_s} \quad (4.3)$$

In terms of the impact of the gain-bandwidth product on the settling time for a switched capacitor circuit, the following approximation for the closed loop gain of an opamp is considered [36, p. 852].

$$A_{Cl} = \frac{1/\beta}{1 + j \frac{f}{f_{un}\beta}}, \quad (4.4)$$

where f_{un} is the gain-bandwidth product calculated as $f_{3dB} \cdot A_{ol}(0)$. In the previous assumption the system possess a single pole, which is a valid approximation if the dominant pole occurs at much lower frequencies than the first non-dominant pole.

From equation 4.4 the closed loop time constant can be obtained as

$$\tau = \frac{1}{2\pi f_{un}\beta} \quad (4.5)$$

If slew rate limitations are neglected, the output voltage of the circuit in response to a voltage step input can be approximated by using the simple equation for capacitor charging

$$V_{out}(t) = V_0(1 - e^{-t/\tau}) \quad (4.6)$$

If for example a 1% settling is required at least 5τ seconds are needed, so it is important to have a unity gain frequency as high as possible so as to reduce the time constant and consequently increase the speed and the maximum switching frequency of a switched capacitor circuit. In a more simplified analysis an estimate for the settling time can be obtained as a rule-of-thumb by $1/(f_{un}\beta)$ [36, p. 853].

After the former analysis the problem seems to have a simple solution, if the objective is to design an opamp for switched capacitor circuits the adopted topology must have a high dc gain and gain-bandwidth product. Yet, achieving this is not easy because there are trade-offs between both of these characteristics, trade-offs which become even more significant when using a-GIZO TFTs. The current lack of complementary devices makes it difficult to achieve high values of dc gain in a-GIZO amplifying stages. It imposes wide driver transistors and multiple gain stages to achieve significant voltage gains. This in turn degrades the frequency response of the amplifier because wider transistors result in higher parasitic capacitances and multiple stages result in additional poles introduced in the system.

In the definition of the performance goals an additional limitation was taken into account besides the ones already presented in section 2.5. This extra additional limitation stems from tests carried out in transistors previously fabricated at CENIMAT which, have shown that the devices tend to be damaged for V_{GS} values superior to about 7V. This further restricts the options available during the design phase especially considering these transistors can stand up to 20V for V_{DS} .

Finally, after balancing all the factors presented above, the following performance goals were set for the amplifier:

- Voltage gain as close as possible to 60dB to have a static error close to 0.1
- At least 60° of phase margin
- No transistor in the opamp must present a V_{GS} value that exceeds 7V.
- Techniques to increase the lifetime of the topology must be implemented.

In terms of gain-bandwidth product no specific goal was set regarding speed, because this matter is still an ongoing research at the present stage of the work.

4.3 Simulation model for a-GIZO TFTs

Another important study that was executed before starting to develop the topology for the operational amplifier was that of the simulation model for the a-GIZO TFT. The model used reproduces the static behaviour of an a-GIZO TFT through an artificial neural approximator. This approach was employed to avoid complex physical models while still achieving a high level of accuracy. It was previously developed at FEUP by Bahubalindrani et al. being reported in [37] and because of its implementation in verilog-A, it is compatible with the circuit simulator used, which was Cadence Spectre.

In terms of aspect ratio, the transistors that can be simulated with this model must have a channel length of $20\mu m$ with the width of channel being between 40 and $320\mu m$. The reason for this is that the I-V characteristics used to build the model were taken from devices with aspect ratios within this range.

As referred earlier, the device's intrinsic capacitors were not yet characterized. Consequently, intrinsic capacitors are not yet taken into account in the present model. However, it is extremely

important at least to infer the frequency behaviour of the proposed circuits. For that reason, a Meyer Capacitance Model [38] was developed during this thesis. To the authors knowledge this approach has not been used before for a-GIZO TFTs but a recent study suggests that Meyer's capacitance model may be valid for the charge storage effect in pentacene-based OTFTs [39]. This technology is in many ways similar to the a-GIZO, both in terms of device structure, operation principle and limitations. Therefore, this model was used to attain estimates of C_{GS} and C_{GD} in simulation, although no information exists yet as to the accuracy of this approximation.

In the implementation of Meyer's Model for our simulation model the following parameters were used:

- ϵ_r : 10.5
- Thickness of the dielectric (t_{ox}): 250nm
- Overlap between gate and source/drain material (x_d): $5\mu m$

These parameters are up to date with the materials, processes and structures used in the circuits currently fabricated at CENIMAT.

Then according to the capacitance model the estimates for C_{GS} and C_{GD} in saturation were respectively calculated as

$$C_{GS} = W.C_{ov} + \frac{2}{3}W.Leff.C_{ox} \quad (4.7a)$$

$$C_{GD} = W.C_{ov}, \quad (4.7b)$$

where W is the width of the channel, $Leff$ is the effective length of the channel, C_{ox} is the equivalent capacitance per area and C_{ov} is the capacitance associated with the overlap between gate and source/drain material.

The remaining two parameters, C_{ox} and C_{ov} , are calculated as

$$C_{ox} = \frac{\epsilon_r \cdot \epsilon_0}{t_{ox}} \quad (4.8a)$$

$$C_{ov} = x_d \cdot C_{ox}, \quad (4.8b)$$

where ϵ_0 is the permittivity of free space which is approximately equal to $8.85 \times 10^{-12} F/m$.

The lack of information on parasitic capacitances is the biggest limitation of our technology model but other considerations were taken into account during the simulations of the developed circuits. One of these considerations is the possibility of having in some conditions a negative gds for an a-GIZO TFT, an effect that typically happens in devices with V_{DS} levels superior to 6V. The negative gds values for these transistors, which have not been reported in literature, can be verified in measurements. This effect, in principle, is not expected and for that matter it was assumed an always-positive gds value. This imposition was accomplished mainly through manipulation of

bias voltages, avoiding points in the characteristic that exhibited negative g_{ds} . Such measure is crucial because negative g_{ds} in some circuit configurations, may result in unrealistic voltage gain values during simulation.

Convergence problems also occurred during simulations, especially if the transistor was used as a switch. These problems resulted from the existence of non-negligible leakage currents when V_{GS} is equal to zero and could sometimes be resolved through the connection of big resistances and small capacitances to certain critical nodes.

As a final note concerning the simulation model for the a-GIZO TFT it is important to emphasize that it is yet not possible to estimate in simulation the shift of the threshold voltage over time. This means that the analysis of any measure implemented to reduce this effect can only be characterized by results taken from fabricated circuits.

4.4 Design of the Operational Amplifier

In this section the development process of the opamp is presented using a stage-by-stage approach in order to justify the decisions that were made regarding the proposed topology. The most important results associated with the proposed topology are also presented and critically analysed taking into account the results obtained from the simulations performed in both NMOS and a-GIZO TFT.

The design process started with the definition of a fully differential output for the amplifier. This decision is justified by the fact that right from the beginning it was known that it would be very difficult to implement the operational amplifier with a single stage. Therefore, the output was set as fully differential to avoid the extra mirror pole that would be inserted by a fully-differential to single-ended conversion stage. The use of this output structure also presents an extra advantage in the context of switched capacitor circuits because constant offsets like the ones introduced by clock feedthrough effects have less impact.

In the following stage-by-stage presentation of the proposed topology a superior emphasis is given to the input stage because it is the most complex part of the opamp.

4.4.1 Input Stage

For the selection of the topology to be employed in the differential input an analysis of all the configurations previously reported for high-gain stages, with only n-type enhancement transistors, was made. All of the stages analysed are capable of achieving high-gain without the need of using transistors at the drive that are much wider than the ones used as active loads. The aforementioned process was performed in the context of the differential pair stage because the input stage was defined as the main gain stage for the opamp. Also included in the analysis is a novel topology developed during the Master Thesis.

All the topologies analysed can be seen in figures 4.1 and 4.2.

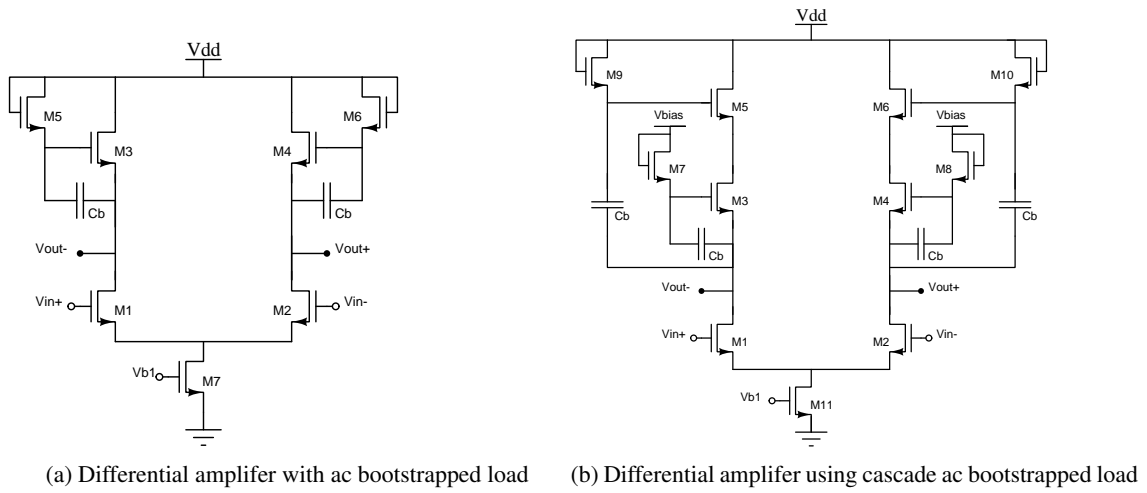


Figure 4.1: High-gain single-stage differential amplifiers using ac bootstrapping

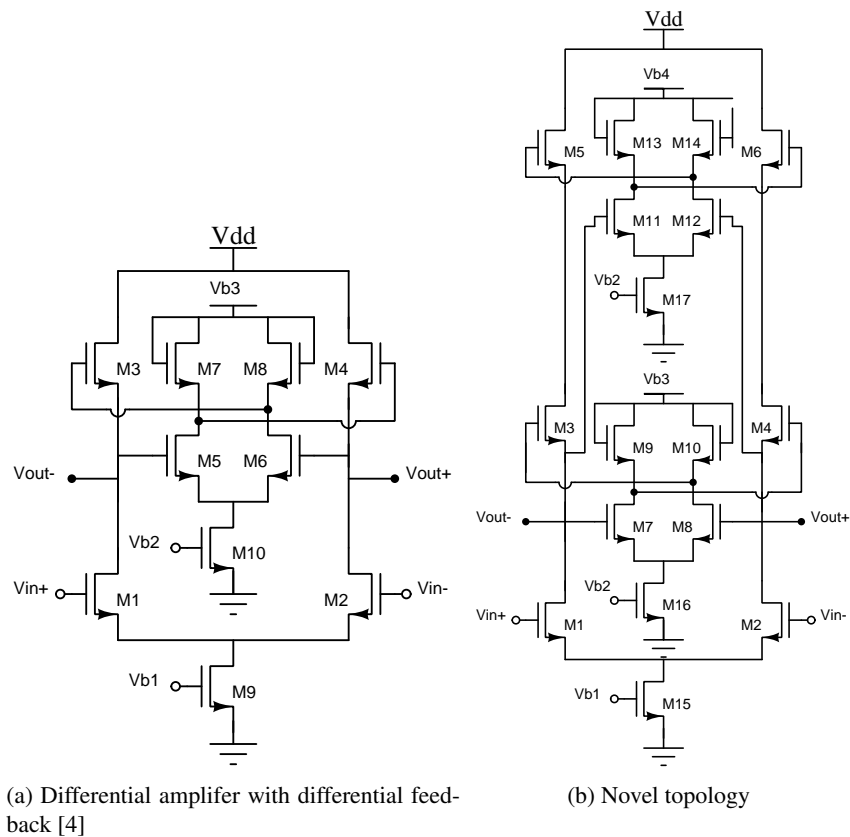


Figure 4.2: High-gain single-stage differential amplifiers using a differential amplifier to implement positive feedback

However, before the results obtained in the comparative analysis are presented it is important

to present the operation principle and characteristics of the novel topology. This topology combines the principle of using a cascade of transistors for the load, which had been introduced in [5] with the implementation of positive feedback network through the use of a differential amplifier, a technique previously presented in [4]. This last technique reduces the necessary number of transistor required for the implementation of the feedback networks. This reduction becomes evident if the single-stage implementation of the topology is considered (figure 4.3). If the differential version of the topology was implemented using the single-ended version in each side a total of 20 transistors would be necessary for the active load. Using a differential stage in the feedback networks, only 14 transistors are necessary considering that each differential pair has one biasing transistor.

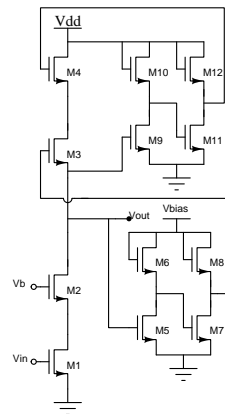


Figure 4.3: Single-stage version of the novel topology for high-gain with only n-type enhancement transistors

In terms of operation principle, the proposed topology is very similar to that of figure 4.1b. The output signal is fed back to the gate of both the transistors in the cascade load and an extra bias voltage is necessary for the feedback network of the bottom transistor of the cascade. Still there are two major differences between these configurations, in the novel topology the amplification of dc signals is possible but, unlike the cascade load implemented with capacitive bootstrapping, the feedback factor is not guaranteed to be always below one, which means that care is needed during design to ensure stability.

To estimate the behaviour of this new topology, a detailed small-signal analysis was carried out. Figure 4.4 depicts a simplified single-ended version of the novel gain stage and its respective small signal equivalent, corresponding to a cascode configuration.

The equations for voltage gain and equivalent load impedance have been calculated from the small-signal model and are presented in 4.9.

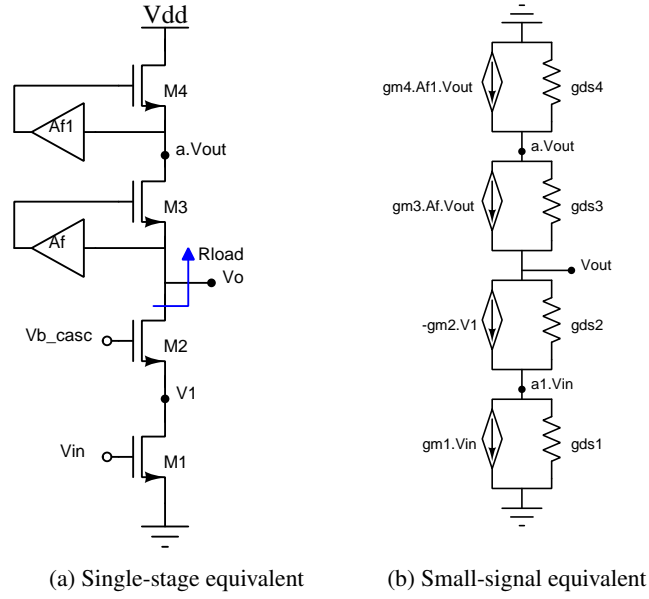


Figure 4.4: Simplified models of the proposed topology

$$A_{ol} = \frac{V_{out}}{V_{in}} = \frac{gm_1 \cdot gm_2 + gm_1 \cdot gds_2}{(Af - 1) \cdot gm_3 \cdot (gds_1 + gds_2 + gm_2) + (a - 1) \cdot gds_3 \cdot (gds_1 + gds_2 + gm_2) - gds_1 \cdot gds_2} \quad (4.9a)$$

$$R_{load} = \frac{r_{o3}}{1 - a - gm_3 \cdot (Af - 1) \cdot r_{o3}} \quad (4.9b)$$

$$a = \frac{gm_4 \cdot Af1 - gm_3 \cdot Af + gm_3 + gds_3}{gm_4 + gds_3 + gds_4} \quad (4.9c)$$

Where Af and $Af1$ are the feedback factors of the bottom and top feedback networks and a is the voltage gain between the output and the node in the middle of the cascade load. In this analyses the parasitic capacitances of the devices were not taken into account. For the detailed deduction of the former equations consult sections A.1.1 and A.1.2 of appendix A.

To simplify the analysis somewhat and promptly test in simulation that the equations are valid, the simplification of using the same biasing conditions for the 4 transistors of the structure was made. In this way all of the transistors have the same gm and gds values and the former equations in 4.9 simplify to

$$A_{ol} = \frac{gm^2 + gm.gds}{(Af - 1).(2.gm.gds + gm^2) + (a - 1).(2.gds^2 + gm.gds) - gds^2} \tag{4.10a}$$

$$R_{load} = \frac{r_o}{1 - a - gm.(Af - 1).r_o} \tag{4.10b}$$

$$a = \frac{gm.(Af1 - Af + 1) + gds}{gm + 2.gds} \tag{4.10c}$$

In simulation the analysis of the voltage gain and of the gain factor a were first performed using a BSIM3V3 model for a $0.35\mu m$ NMOS technology. Also, the implementation of the feedback networks for this simulation was realized using an ideal opamp in order to accurately control the feedback factors. At this point the objective is to demonstrate the validity of the equations as well as estimating the variation of the voltage gain with relation to the variation of the feedback factors Af and $Af1$.

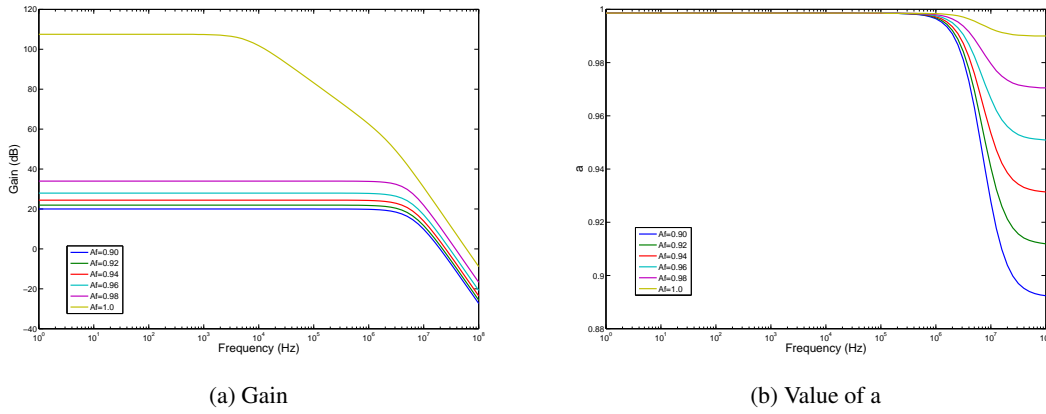


Figure 4.5: Sweep of both Af and $Af1$ in the novel topology, NMOS implementation

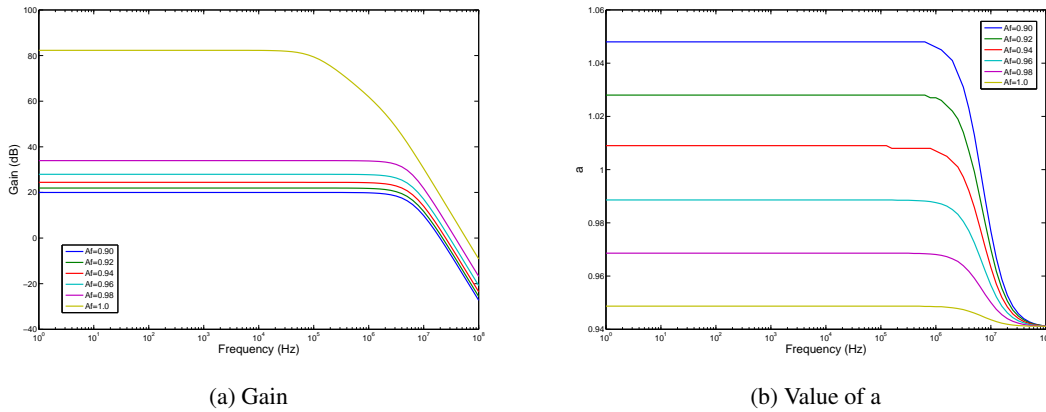


Figure 4.6: Sweep of Af in the novel topology keeping $Af1=0.95$, NMOS implementation

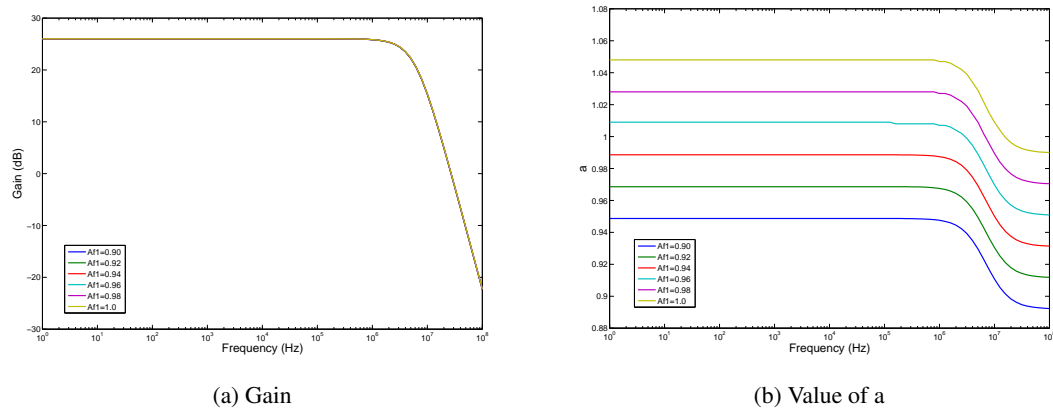


Figure 4.7: Sweep of $Af1$ in the novel topology keeping $Af=0.95$, NMOS implementation

From these results five major conclusions, regarding this topology can be taken:

- The value of a will go above one if $Af1 > Af$, $gm_3 = gm_4$ and $gds_3 = gds_4$. This is undesirable because a negative resistance will be introduced in the system, causing stability issues.
- The value of Af has more impact in the voltage gain of the topology than that of $Af1$, because having $Af1$ higher than Af does not increase gain, but $Af > Af1$ does. An effect justified by the fact that Af influences both the factor a and the voltage gain directly while $Af1$ only affects gain because of its effect in the value of the factor a .
- The closer Af and $Af1$ are to one with $Af \geq Af1$ the higher the voltage gain obtained.
- If $Af=Af1=1$ the load impedance will be equal to that of a complementary cascode load, demonstrated in section A.1.3 of appendix A, and the topology presents approximately a square of the intrinsic gain of the driver transistor.
- The expressions deduced for the topology are in agreement with the results obtained in simulation.

The same analysis was made with the a-GIZO TFT model and the same conclusions are observed. The simulation results of these simulations are depicted in figures 4.8, 4.9 and 4.10.

The biasing conditions and aspect ratios of the transistors used in these simulations can be consulted in section A.2.1 of appendix A.

Although they seem identical there is a difference between the behaviour of the topology in a-GIZO TFTs and NMOS. Comparing the gain results for the sweep of both the gain factors for NMOS and a-GIZO presented in figures 4.5a and 4.8a, respectively, there is major difference in the ratio between the gain obtained when $Af=Af1=1$ and $Af=Af1=0.9$ for both topologies. For NMOS this ratio is 87.51dB while for a-GIZO it is only 32.06dB. This result implies that the voltage gain

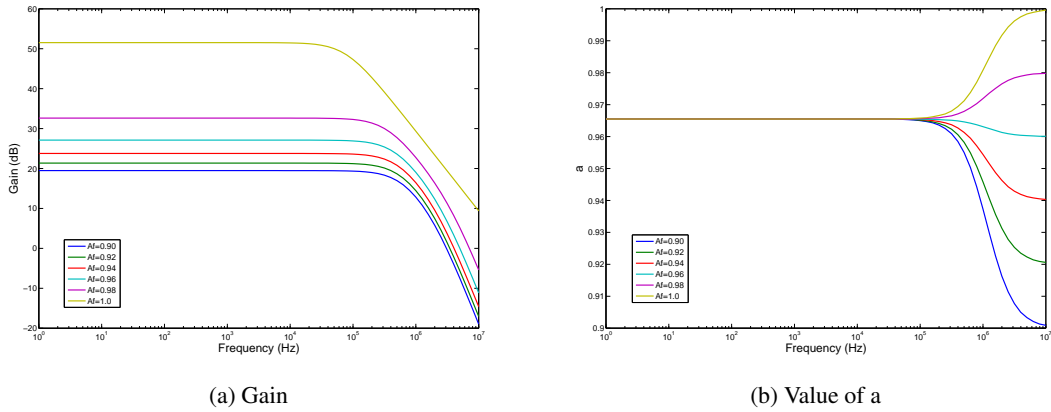


Figure 4.8: Sweep of both A_f and A_{f1} in the novel topology, a-GIZO TFT implementation

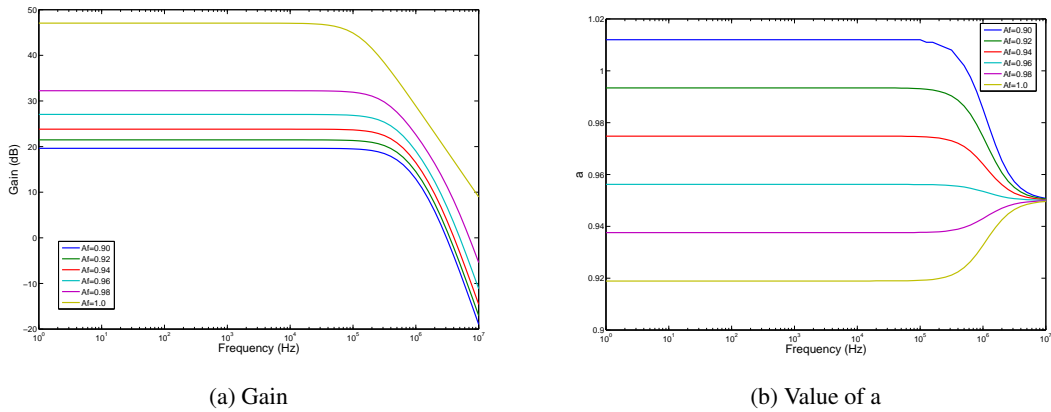


Figure 4.9: Sweep of A_f in the novel topology keeping $A_{f1}=0.95$, a-GIZO TFT implementation

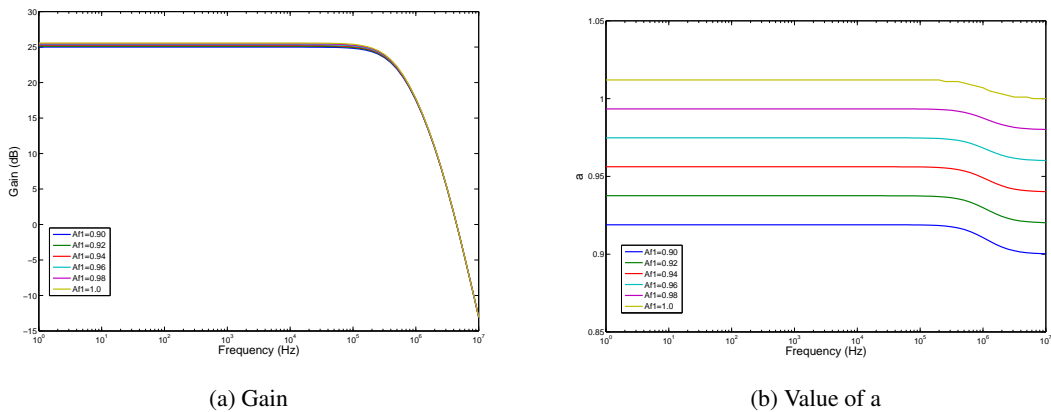


Figure 4.10: Sweep of A_{f1} in the novel topology keeping $A_f=0.95$, a-GIZO TFT implementation

of this topology drops more in NMOS than in a-GIZO with relation to how below 1 is the gain in the feedback networks. The major cause for such result resides on the difference in gm/gds ratio between the two technologies. Recalling that for a-GIZO TFTs the mobility of carries in the channel is several orders of magnitude lower than that of the one obtained in typical NMOS transistors, we already expected that the gm values for the former devices would be significantly lower than the ones of the latter, as would the ratio between gm and gds . Knowing that this ratio represents the difference in magnitude between the values of $r_o = 1/gds$ and $1/gm$ and that r_o is in parallel with $1/(gm(1 - Af))$ it becomes evident that even for a feedback factor slightly inferior to one, like for example 0.98, the bigger the value of gm in relation to gds the more dominant $1/(gm(1 - Af))$ will be in the value of the parallel resistance. Consequently, the impedance of the load will be lower as will be the voltage gain. For this reason the proposed topology presents a superior performance in TFT technologies because they possess lower carrier mobility than common silicon based technologies. This finding is very important because a-GIZO TFT is not yet a fully developed technology, therefore, the mismatches expected during fabrication will be superior to those obtained in circuits fabricated in commercial semiconductor technologies. This obliges the designer to give a security margin and therefore not implement the gain very close to unity in the feedback, because the value of this gain in the real circuits can be found to be above one causing stability issues. So, if there was a similar variation of the load impedance when Af is going below one as the one verified for NMOS, the use for this topology would be very limited because the voltage gain would be tremendously reduced when compared to the one that could be theoretically achieved if the gain of both the feedback networks was exactly unitary. In TFTs the reduction in gain will be also verified under the same conditions but it will not be as significant. Also, as the fabrication processes evolves and becomes more accurate there will be the possibility of aiming for values of Af that are very close to unity.

To verify that the formulas presented for the gain of the topology were valid, the results obtained for the factor a and for voltage gain when $Af=Af1=0.9$ and $Af=Af1=1$ were compared to results calculated with the formulas represented in 4.10. The values gm and gds , which were made the same for every transistor in these simulations, are presented in table 4.1.

Comparing the values obtained in simulation, table 4.2, with those calculated through the formulas it can be verified that the expressions can accurately estimate the values of a and of the voltage gain, A_{ol} . Furthermore the gain values measured with $Af=Af1=1$ are approximately given by $0.5 \cdot (gm \cdot (1/gds))^2$. This expression represents the equivalent gain obtained by a topology presenting a cascode in the drive with n-type transistors and a cascode with complementary devices as the load, assuming that between all transistors both gm and gds are equal. Therefore the topology can theoretically give the same gain as a cascode topology implemented with complementary type transistors.

Table 4.1: Transconductance values of the transistors used in the simulations

Technology	gm ($\mu A/V$)	gds (nA/V)
0.35 μm NMOS	520.90	756.6
a-GIZO TFT	14.41	534.1

Table 4.2: Values of the factor a and of A_{ol} measured in simulation

Technology	$a_{measured}$ (mV/V)	$A_{ol_{measured}}$ (Af=Af1=0.9) (V/V)	$A_{ol_{measured}}$ (Af=Af1=1) (V/V)
0.35 μm NMOS	998.55	-9.985	-237.417k
a-GIZO TFT	965.49	-9.414	-377.380

Table 4.3: Values of the factor a and of A_{ol} calculated with the formulas in 4.10

Technology	$a_{calculated}$ (mV/V)	$A_{ol_{calculated}}$ (Af=Af1=0.9) (V/V)	$A_{ol_{calculated}}$ (Af=Af1=1) (V/V)
0.35 μm NMOS	998.55	-9.985	-237.343k
a-GIZO TFT	965.49	-9.414	-377.449

Going back to the differential configuration of the positive feedback networks, it was found that this configuration not only allows the use of less transistors in the system but it also introduces an interesting characteristic regarding common-mode signals. In figure 4.11 a cascade cross-coupled load, also referred as gm cancellation load, implemented with p-type transistors is represented. This type of configuration is used as a complementary active load for differential amplifiers in CMOS, as for example in the switched opamp in [11], because it has a impedance for differential signals that is different from its impedance for common-mode signals, which are calculated by

$$R_{load_{diff}} = \frac{1}{2}(gm_3 \cdot r_{o3} \cdot r_{o4} + r_{o3} + r_{o4}) \quad (4.11a)$$

$$R_{load_{CM}} = \frac{1}{2 \cdot gm_4} \frac{1}{1 - \frac{r_{o3} - 1/gm_4}{gm_3 \cdot r_{o3} \cdot r_{o4} + r_{o3} + r_{o4}}} \quad (4.11b)$$

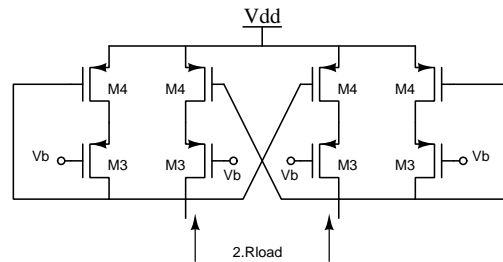


Figure 4.11: Cross-coupled load with p-type transistors

So, for the cross-coupled load the differential impedance is much higher than the one presented for common-mode, which if $gm_3 \cdot r_{o3} \cdot r_{o4} + r_{o3} + r_{o4} \gg r_{o3} - 1/gm_4$ can be approximated as $0.5/gm_4$.

Interestingly the novel topology presents a very similar effect to that of a cross-coupled load due to the differential feedback networks. To arrive at this conclusion consider again the representation of the topology in 4.2b. Since the feedback is implemented using the signal in the other half of the differential pair, positive feedback will be implemented in the case of differential signals. On the other hand for common-mode signals the feedback factors will be negative because the signals in each side of the differential pair are now in phase. Recalling the equivalent single stage model of the topology 4.4a, its equation for load impedance presented in 4.9 and considering the ideal case in which the module of the voltage gain in both feedback networks is exactly one, the load impedances for differential and common-mode signals are respectively given by

$$Rload_{diff} = gm_4 \cdot r_{o3} \cdot r_{o4} + r_{o3} + r_{o4} \quad (4.12a)$$

$$Rload_{CM} = \frac{r_{o3}}{2} \frac{1}{1 - \left(\frac{r_{o4} + r_{o3} / 2 - gm_3 \cdot r_{o3} (gm_4 \cdot r_{o3} \cdot r_{o4} + r_{o3})}{gm_4 \cdot r_{o3} \cdot r_{o4} + r_{o3} + r_{o4}} \right)} \quad (4.12b)$$

The differential impedance is considerably high and equal to the one obtained if a cascode configuration with complementary type transistors would be used. The common-mode impedance will be considerably lower than the differential one, although it may appear so at first glance. In fact considering that the term $gm_3 \cdot gm_4 \cdot r_{o3}^2 \cdot r_{o4} \gg (-r_{o4} + r_{o3}(1/2 - gm_3 \cdot r_{o3}))$ and that $gm_3 r_{o3} \gg 1$, the impedance for common-mode signals can be re-written as

$$Rload_{CM} = \frac{1}{2 \cdot gm_3} \quad (4.13)$$

The deduction of the 3 equations presented above is detailed in section A.1.3 of appendix A.

The above equations imply that the proposed load topology should operate in a way similar to that of a cascade cross-couple load in complementary devices. Since the value of the load resistance, for differential signals, could already be verified when both of the feedback factors were made equal to 1, figures 4.5a and 4.8a, the same analysis was performed executing a sweep from -1 to -0.9 in both the feedback factors. This simulation was performed for NMOS and in the same conditions of the previous analysis, and the obtained results are presented in figure 4.12. Analysing the results, the effect of having a common-mode resistance equal to $1/(2 \cdot gm_3)$ is verified because the gain for $Af=Af1=-1$ is -6dB, which corresponds to the expected result considering that all the transistors in the topology have the same gm and gds . From this result it is possible to demonstrate that this topology will offer high rejection for common-mode signals, especially when the $|Af|$ and $|Af1|$ are made close to one, because there is not much alteration of the common-mode gain when these values are below one but, on the other hand, there is a considerable drop in the differential gain of the configuration.

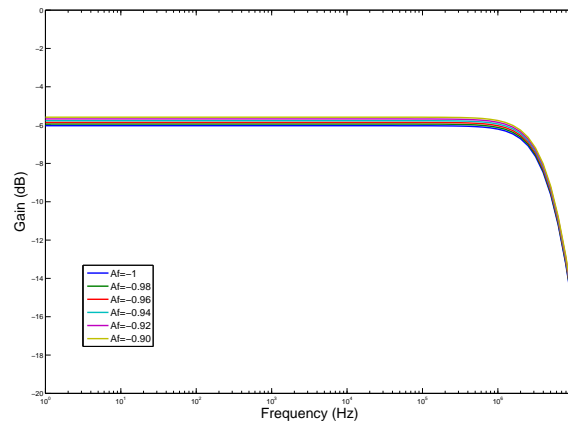


Figure 4.12: Voltage gain of the novel topology when A_f and A_{f1} are swept from -1 to -0.9, NMOS implementation

After performing the detailed analysis of the novel topology, the comparative analysis between it and the other topologies previously reported in literature was performed. The objective of this comparison being the selection of which topology would be more appropriate for the input stage.

To perform the analysis under the same conditions in all of the topologies this comparative study was performed using the same biasing conditions except for those transistors in the feedback loops. The results obtained from simulations of the various circuits implemented in $0.35\mu\text{m}$ NMOS process are displayed in figure 4.13, while the results obtained using the a-GIZO TFT model are presented in figure 4.14. The information on the aspect ratios and biasing conditions used for each circuit is presented in A.2.2 of appendix A. In all these simulations the gain of the feedback networks is made lower than one. The topologies here analysed are the ones presented in figures 4.1 and 4.2. In this graphic and in following results the topology in figure 4.2a is designated as *Amp1*, the one in figure 4.1a is *Amp2*, and the ones in figures 4.2b and 4.1b are, respectively, *Amp3* and *Amp4*.

The first notable finding in these results is that both technologies (NMOS and a-GIZO) are in agreement except for the response of the topologies with capacitive bootstrapping. This difference is due to the fact that there is slight voltage drop in the biasing transistors for the active loads of the ac bootstrap topologies in a-GIZO. This makes the load transistors in the cascode have considerably different r_o values, even for a difference of a few mV between the V_{DS} of both of them.

Analysing the results only in terms of voltage gain it is found that the topology using cascade capacitive bootstrap is the one that gives higher gain, which means that it is also the one where the load impedance is higher. Also, between both of the topologies using capacitive bootstrapping, the one with the cascade structure presents approximately 6dB more of gain in the NMOS implementation, a result that is expected considering that the cascade load presents an impedance that is much higher than that of the single load. This happens because for the single bootstrapped load

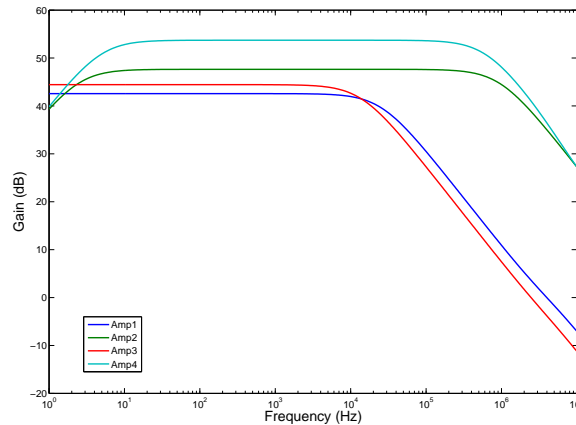


Figure 4.13: Simulation results of high-gain single-stage differential amplifiers with only n-type enhancement transistors, NMOS implementations

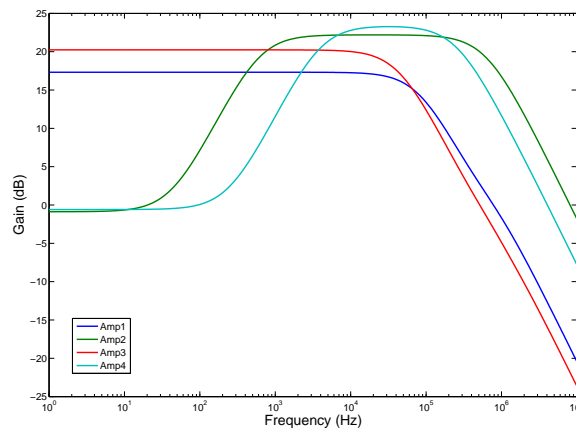


Figure 4.14: Simulation results of high-gain single-stage differential amplifiers with only n-type enhancement transistors, a-GIZO TFT implementations

the impedance will be approximately equal to r_o of the load transistor, while for the cascade structure it will be approximately $gm.r_o^2 + 2.r_o$. Therefore, in the case of the single bootstrapped load the gain will be approximately $0.5.gm.r_o$ while in cascade structure with bootstrapping it will be $gm.r_o$ as the output resistance of the driver transistor is much lower than the load impedance. The same 6dB difference in gain between the ac bootstrapping topologies is not verified in a-GIZO because the r_o for the transistor at the top of the cascode load was lower than that of transistor in the bottom of the cascode load. Nonetheless, the cascode load with capacitive bootstrapping still exhibits a higher gain than that of the same configuration with a single load transistor. The other two topologies give less voltage gain than the ones using capacitive bootstrapping because the feedback factors were kept below 1 with inferior values than those obtained with capacitive bootstrapping. Comparing both topologies it is possible to verify that the novel topology has an

increased gain when both configurations have the same value for the feedback factor A_f . Unlike the previous case there is no 6dB difference between the gain obtained with the cascade and single loads which is justified by the fact that for the cascade structure A_{f1} is also lower than 1.

If the comparison is realized only considering bandwidth clearly the capacitive bootstrapped topologies are superior, and the novel topology is the worse of the topologies because extra capacitive loading is added to the output node. Still, it is also necessary to take into account that the capacitive bootstrapped topologies cannot amplify dc while the others can. A relevant factor if the opamp is intended for generic purpose.

Finally, if power consumption is taken into account the capacitive bootstrapped topologies are also going to be superior because the feedback networks of the other topologies require extra current for biasing. Also, the novel topology will again be the inferior one in this category because it requires not one but two feedback networks and it also has the biggest number of transistors among the topologies analysed.

Table 4.4 shows the results obtained for each topology using NMOS. Table 4.5 presents the comparative analysis of the topologies in terms of the number of components that are necessary for their implementation.

Table 4.4: Comparative analysis of the performance high-gain differential stages with n-type enhancement transistors in NMOS

Topology	$A_{ol}(A_f = A_{f1} = 1)$	$A_{ol_{sim}}$ (dB)	Bandwidth (kHz)	A_f	A_{f1}
Amp1	$\simeq 0.5.gm.r_o$	42.57	25.64	0.9955	-
Amp2	$\simeq 0.5.gm.r_o$	47.64	959.50	0.9988	-
Amp3	$\simeq gm.r_o$	44.45	13.95	0.9955	0.9909
Amp4	$\simeq gm.r_o$	53.72	616.76	0.9994	0.9983

Table 4.5: Number of components necessary to implement each of the high-gain stages only with n-type enhancement transistors analysed

Topology	No. transistors	No. capacitors
Amp1	10	0
Amp2	7	2
Amp3	17	0
Amp4	11	4

After concluding this comparative analysis a decision on the input stage for the opamp had to be made and the decision fell on the novel topology developed. However, the drive of the circuit was altered to a cascode configuration, as represented in figure 4.15, to further increase the voltage gain and at the same time reduce the input capacitance of the opamp.

The factors behind this decision were the following:

- The possibility of amplifying dc makes the opamp also suited for generic applications.

- In terms of maximum voltage gain the novel topology is inferior to the ones using capacitive bootstrapping. However, unlike these topologies the one selected does not require the use of extra capacitors, which would increase the overall circuit area considerably.
- The behaviour of the novel topologies for common-mode signals makes it so that the rejection of common-mode disturbances in the input stage is significant even when the differential gain has a moderate magnitude. A characteristic not presented in capacitive bootstrapped topologies because the feedback of the output signal to the gate of the load transistors is not differential.

Still, there are also some drawbacks associated with the selection of this topology. For example, without using significantly wide transistors for the drive it would be very difficult to achieve a voltage gain close to 60dB with only this stage, especially because a margin has to be given in the feedback factors of the active load to ensure that after fabrication the opamp does not turn out to be unstable. So, avoiding very wide transistors and restricting the aspect ratios of the transistors to the ones that the model is able to simulate, W/L from $40/20\mu m$ to $320/20\mu m$, more stages were ultimately necessary in order to increase the overall gain. Other handicaps such as the number of transistors and increase power consumption were considered not significant, because of the limitations in the implementation of high-gain stages in this technology and of the lower currents of a-GIZO TFTs when compared to those of typical silicon based transistors.

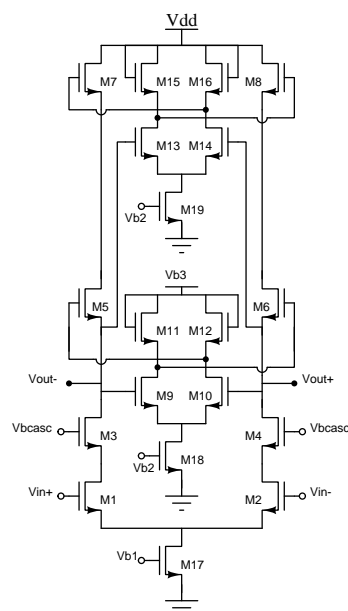


Figure 4.15: Input stage of the proposed opamp

4.4.2 Second Stage

Ideally the next stage added to the amplifier should be another stage that increased gain, but since the voltage at the output of the first stage is relatively high this is not possible. If complementary devices were available this problem would not exist but with only n-type transistors it is impossible to connect a common-source amplifier directly to the output of the first stage unless source-degeneration was to be used. If this option was employed, the common-mode voltage at the output of the opamp would be higher than $V_{dd}/2$ and the output swing would be considerably limited. Therefore, it is necessary to lower the voltage level before adding another stage to increase the overall voltage gain.

The level shift required was implemented through a source follower stage, depicted in figure 4.16. This stage reduces the overall voltage gain, although only slightly, but this effect is more than compensated by connecting another gain stage after this one. To ensure that the loss in gain is low, the active load of this stage is implemented by an n-type transistor that also determines the biasing current for the stage. If instead a diode connected transistor were used there would be a greater attenuation of gain because the load resistance would then be $2/gm$ instead of $1/gm + r_o$. The diode connected transistor between the input and load transistors is used to ensure that none of the a-GIZO TFTs in this stage will present a V_{GS} higher than 7V, which in real circuits can possibly damage the transistors.

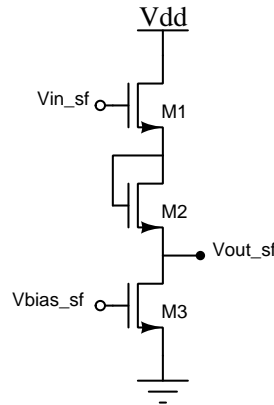


Figure 4.16: Schematic of the second stage of the opamp

The voltage gain of this stage is given by

$$A_{sf} = \frac{gm_1 \cdot (r_{o1} || (r_{o3} + (r_{o2} || \frac{1}{gm_2})))}{1 + gm_1 \cdot (r_{o1} || (r_{o3} + (r_{o2} || \frac{1}{gm_2})))} \quad (4.14)$$

The use of this stage, although necessary proved to introduce several drawbacks in terms of frequency response of the opamp and its respective compensation. This subject is detailed further in section 4.5.1 of the present chapter.

4.4.3 Remaining stages and V_{th} shift attenuation

A common-source stage is then connected to the output of the previous stage to further increase the overall voltage gain of the opamp. Ideally this stage would also constitute the output stage of the amplifier but not in this case. The reason for this is the need to add techniques for V_{th} shift reduction in the topology. One possible solution is to use a biasing transistor with twice the width of the diode connected transistor used to implement the load in the positive feedback networks. This technique proposed by Tarn et al. [6] which was previously presented in 3.2 reduces the effect of the threshold voltage shift in the output nodes of the differential positive feedback networks. Another possibility is to use common-mode feedback as proposed by Marien et al. [7], also previously addressed in 3.2. Both of these techniques were applied to opamp developed.

As referred in 2.6.4.1 the use of common-mode feedback is mandatory in fully-differential amplifiers implemented with complementary transistors or otherwise the CM level at the output will be undefined when negative feedback is applied to the opamp [27, p. 315]. However, this is not the case for fully-differential amplifiers implemented with a single type of transistor such as the one proposed in this work. The difference is associated to the fact that for an amplifier with a single type of transistor the voltages in each and every node of the circuit can be determined by the bias voltages applied, since no current source is implemented in the load transistors of the gain stages. The only justification for using common-mode feedback in the proposed topology is then to counteract the V_{th} shift. A common-source stage is then connected to the output of the previous stage to further increase the overall voltage gain of the opamp. Ideally this stage would also constitute the output stage of the amplifier but not in this case. The reason for this is the need to add techniques to reduce the V_{th} shift in the topology. One possible solution is to use a biasing transistor twice the width of the diode connected transistor used to implement the load in the positive feedback networks. This technique proposed by Tarn et al. [6] which was previously presented in 3.2 reduces the effect of the threshold voltage shift in the output nodes of the differential positive feedback networks. Another possibility is to use common-mode feedback as proposed by Marien et al. [7], also previously addressed in 3.2. Both of these techniques were applied to opamp developed.

As referred in 2.6.4.1 the use of common-mode feedback is mandatory in fully-differential amplifiers implemented with no complementary transistors or otherwise the CM level at the output will be undefined when negative feedback is applied to the opamp [27, p. 315]. However, this is not the case for fully-differential amplifiers implemented with complementary type transistors such as the one proposed. The difference is associated to the fact that for an amplifier with a single type of transistor the voltages in each and every node of the circuit can be determined by the bias voltages applied, since no current source is implemented in the load transistors of the gain stages. The only justification for using common-mode feedback in the proposed topology is then to counteract the shift in V_{th} overtime. This shift can be viewed as a common-mode disturbance if the topology is considered to be totally symmetric with the corresponding transistors in each branch of the opamp suffering exactly the same shift. In this case if V_{th} increases the common-mode feedback loop will tend to increase the V_{GS} of the biasing transistors to compensate this effect and keep the

common-mode level at the output in the desired level. However the performance of the opamp will still deteriorate over time because the increase of V_{GS} will only work until a certain margin is not exceeded, as at some point there will be transistors going into triode. Nonetheless the use of common-mode feedback is expected to increase the operational lifetime.

It is this necessity for common-mode feedback loop that constitutes the reason why one extra stage. Considering again that the CMFB loop is connected to the biasing transistor of the input stage (M17) and that a single common-source stage is added after the source follower level-shifter, it is found that the gain between the gate of M17 and the output node of the opamp would be positive in this case. This would imply an inversion of the CM level measured at the output within the CMFB circuit itself, therefore introducing extra poles in this circuit. Since the frequency response of the CM loop influences that of the differential loop, because of the time it takes to settle the common-mode level at the output, inverting the measured CM level signal within the CMFB circuit is undesirable. To avoid this, not one but two consecutive common-source stages were added after the source-follower stage. The schematics for these stages, which are the third and fourth stages of the opamp, from here on designated as *Common-Source1* and *Common-Source2*, are presented in figures 4.17a and 4.17b respectively.. This shift can be viewed as a common-mode disturbance if the topology is considered to be totally symmetric with the corresponding transistors in each branch of the opamp suffering exactly the same shift. In this case if V_{th} increases the common-mode feedback loop will tend to increase the V_{GS} of the biasing transistors to compensate this effect and keep the common-mode level at the output in the desired level. However the performance of the opamp will still deteriorate over time because the increase of V_{GS} will only work until a certain margin is not exceeded, as at some point there will be transistors going into triode. Nonetheless the use of common-mode feedback is expected to increase the operational lifetime of the circuit.

It is this necessity for common-mode feedback loop that constitutes the reason why one extra stage was used. Considering again that the CMFB loop is connected to the biasing transistor of the input stage (M17) and that a single common-source stage is added after the source follower level-shifter, it is found that the gain between the gate of M17 and the output node of the opamp would be positive. This would imply an inversion of the CM level measured at the output within the CMFB circuit itself, therefore introducing extra poles in this circuit. Since the frequency response of the CM loop influences that of the differential loop, because of the time it takes to settle the common-mode level at the output, inverting the measured CM level signal within the CMFB circuit is undesirable. To avoid this, not one but two consecutive common-source stages were added after the source-follower stage. The schematics for these stages, which are the third and fourth stages of the opamp, from here on designated as *Common-Source1* and *Common-Source2*, are presented in figures 4.17a and 4.17b respectively.

In the third stage voltage gain is achieved by using a wider transistor for the drive than the ones used as active loads. The use of three stacked-up diode connected loads is justified by the necessity of having V_{GS} values below 7V while at the same time providing an output voltage for the input of the last stage that imposes the common-mode level of $V_{dd}/2$. In the output stage

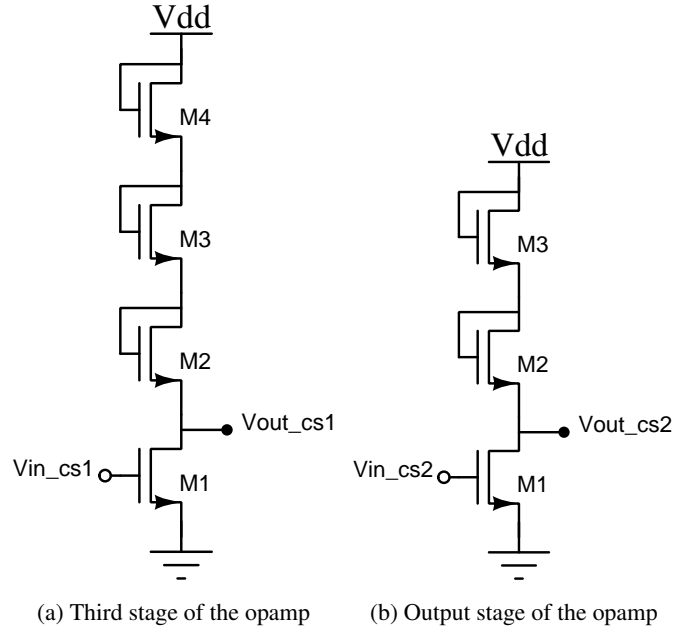


Figure 4.17: Final stages of the proposed opamp

the widest transistors possible are used in order to reduce the output resistance. Here all of the transistors have the same aspect ratio and two diode connected loads are used so as not to exceed the limit value for V_{GS} at the cost of a reduction on the output swing.

The expressions for voltage gain of the third and fourth stages are respectively

$$A_{CS1} = -gm_1 \cdot \left(\left(\frac{1}{gm_2} \parallel r_{o2} \right) + \left(\frac{1}{gm_3} \parallel r_{o3} \right) + \left(\frac{1}{gm_4} \parallel r_{o4} \right) \right) \quad (4.15a)$$

$$A_{CS2} = -gm_1 \cdot \left(\left(\frac{1}{gm_2} \parallel r_{o2} \right) + \left(\frac{1}{gm_3} \parallel r_{o3} \right) \right) \quad (4.15b)$$

4.4.4 Common-mode feedback Circuit

For the CMFB circuit a switched capacitor common-mode feedback (SC-CMFB) implementation, depicted in 4.18, was used. This choice was made because the CM loop can have great impact in the behaviour of the amplifier since the output signal can be distorted due to slow settling of the CM voltage at the output. To reduce this effect the CM loop should have a unity gain-frequency comparable to that of the differential loop which means that the number of poles in this loop should be minimized [34]. Since no inversion of the CM-level at the output was required and the opamp is designed for switched capacitor applications this topology was used because it adds no additional parasitic poles to the CM loop. Still as it is a switched capacitor circuit one must take into account that there will be clock feedthrough and charge injection effects induced in the opamp and also that the CMFB network will add extra capacitive loading to the outputs of the opamp.

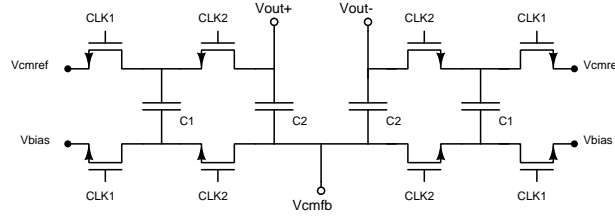


Figure 4.18: CMFB circuit of the proposed opamp

In terms of operation principle the topology used follows the generic operation of a switched common-mode feedback circuit which has been previously presented in 2.6.4.1. In clock phase 1 C_{lk1} is high, C_{lk2} is low, the C_1 capacitors are precharged to $V_{cmref} - V_{bias}$ and the capacitors C_2 are sensing the CM-level at the output. Here the voltage V_{cmref} is the desired CM level for the output of the opamp and V_{bias} is the voltage that guarantees this level at the output when applied to the bias network in open-loop. In clock phase 2 C_{lk1} is low, C_{lk2} is high and the capacitors C_1 and C_2 in each side are connected. In this last clock phase the rearrangement of charge between C_1 and C_2 determines the output voltage of the circuit V_{cmfb} which will be applied to the biasing network of the input stage of the amplifier. This voltage will be refresh in every clock 2 phase. Also, note that this circuit presents a low-pass filter effect because the switches on either side of C_1 implement a resistance approximately equal to C_1/f_{clock} .

Neglecting charge injection and clock feedthrough effects the charge equations for each of the above clock phases described above are

$$Q_1 = 2 \cdot C_1 \cdot (V_{cmref} - V_{bias}) + C_2 \cdot ((V_{out+}[n-1/2] - V_{cmfb}[n-1/2]) + (V_{out-}[n-1/2] - V_{cmfb}[n-1/2])) \quad (4.16a)$$

$$Q_2 = (C_1 + C_2) \cdot ((V_{out+}[n-1] - V_{cmfb}[n-1]) + (V_{out-}[n-1] - V_{cmfb}[n-1])) \quad (4.16b)$$

Considering also that C_{lk1} and C_{lk2} must not overlap and that there are no leakage currents, the charge at node V_{cmfb} will be conserved when C_{lk2} is low [34]. Therefore $V_{cmfb}[n-1/2] = V_{cmfb}[n-1]$, $V_{out+}[n-1/2] = V_{out+}[n-1]$ and $V_{out-}[n-1/2] = V_{out-}[n-1]$. If now the difference between Q_1 and Q_2 is calculated

$$Q_1 - Q_2 = C_1 \cdot (V_{cmref} - V_{bias}) - C_1 \cdot \frac{V_{out+} + V_{out-}}{2} + C_1 \cdot V_{cmfb}, \quad (4.17)$$

considering that $(V_{out+} + V_{out-})/2$ is the CM voltage at the output of the opamp, V_{cmout} , and that in steady state $Q_1 - Q_2 = 0$ due to the charge conservation principle we get

$$V_{cmout} = V_{cmfb} - V_{bias} + V_{cmref} \quad (4.18)$$

V_{cmout} will then be precisely defined and equal to V_{cmref} considering that when steady state is reached $V_{cmfb} = V_{bias}$.

In terms of designing the SC-CMFB feedback circuit, the non-ideal effect of charge injection that was neglected in the previous analysis must be taken into account as well as the gate capacitance of the transistor where V_{cmfb} will be applied. Starting by finding C_1 , we must take into account that there will be charge injected in both C_1 and C_2 when the switches are turned-off, therefore the charge equations for each clock phase presented in 4.16 must be changed to account for this effect. Representing the total charge injected in C_1 and C_2 as $\Delta q_{C_{1,2}}$, equation 4.18 will now be altered to

$$V_{cmout} = V_{cmfb} - V_{bias} - V_{cmref} + \frac{\Delta q_{C_{1,2}}}{C_1} \quad (4.19)$$

So ideally C_1 should be increased in order to reduce the steady state error induced by charge injection, however a big capacitance value for C_1 will reduce the bandwidth of CMFB network and its maximum allowed clock frequency. Therefore, considerably high capacitances values for C_1 must not be used. Another designing factor related with the maximum clock frequency is the size of the transistors used to implement the switches because $R_{on}.C_1 \ll T_{clk}/2$. This means that if C_1 is increased to reduce the effect of charge injection, R_{on} might have to be decreased in order to maintain the desirable clock frequency. On the other hand the use of wider switches will also increase the amount of charge stored in the transistors channel when the switch is closed, thus increasing the amount of charge injected in the capacitors when the switches open. So there will always be a trade-off between charge injection and the maximum clock frequency allowed for the circuit.

$$Q_{channel} = W.L.C_{ox}(V_{GS} - V_{th}) \quad (4.20)$$

Finally, in terms of the size selection for C_2 consider that this capacitor loads the opamp in both clock phases so it must be considerably lower than C_{load} in order to avoid excessive capacitive loading at the output. Still the value of this capacitor cannot be kept very low because it influences the gain in the CM loop. This effect is justified by the voltage divider effect between the equivalent capacitance of the CM loop, equal to C_2 in phase 1 and to $C_1 + C_2$ in phase 2, and the total gate capacitance of the biasing transistor for the differential pair. The overall gain of the CM loop is expressed as

$$A_{CM} = \frac{C_{CMFB}}{C_{CMFB} + C_{GS,bias}} \cdot \frac{g_{mbias}}{g_{minput}} \cdot A_d, \quad (4.21)$$

where A_d is the differential gain of the amplifier, C_{CMFB} is the equivalent capacitance of the CMFB network and $C_{GS,bias}$ is the gate-source capacitance of the biasing transistor for the first stage. For this reason C_2 must not be very small especially considering that the differential gain is not that big to start with. Besides, it has been shown in literature that the settling time of the CM level will be lower for higher C_1/C_2 ratios [40].

In the a-GIZO TFT implementation $C_1 = 25pF$ and $C_2 = 5pF$ were used considering that a $C_{GS,bias} \simeq 2.25pF$ was obtained and the R_{on} of the widest transistor available, $W=320\mu m$, was ap-

proximately 150kΩ. In fact, the capacitance value used for C_2 should have been bigger to increase the gain of the CM loop but since settling and bandwidth must also taken into consideration the trade-off between these characteristics and the gain for the CMFB loop was made.

4.5 Complete Operational Amplifier Topology

After the definition of the third and fourth stages and of the CMFB network, the presentation of the core opamp topology is finished. A schematic of the topology before the application of frequency compensation can be seen in figure 4.19 and the aspect ratios of the transistors used in simulation along with the bias voltages are presented in tables 4.6 and 4.7.

In terms of aspect ratios note that in the input stage transistors M1 and M2 are made wider in order to increase the voltage gain at this stage. Theses transistors will have a lower V_{GS} than that of the other transistors of this stage where V_{GS} is approximately 3V, which corresponds to about $2.V_{th}$, since V_{th} for these devices is estimated between 1.5 and 1.6V. This is the same approach used in the OTFT opamp proposed in [7] where the overdrive voltage ($V_{GS} - V_{th}$) of all transistors in the input stage are high to account for the shift in V_{th} overtime but the input transistors of the first stage are biased with lower V_{GS} to increase their gm/i_{DS} ratio and, therefore, increase the gain of the stage. As in this previous work a CMFB network is also used to partially compensate the V_{th} effect making possible the use of transistors with lower overdrive voltages at the input of the opamp. In terms of the choices for aspect ratios in the other gain stages an emphasis must be given to the first common-source gain stage load transistors. They were made bigger ($80\mu m$), thus decreasing the gain of this stage. This choice was made, again, so that none of the transistors would exceed a V_{GS} of 7V. The driver transistor has a width of $320\mu m$, which is the widest TFT supported by the simulation model, to maximize gain. At the output stage TFTs present a width of $320\mu m$ in order to decrease the output impedance of the opamp, as much as possible. Regarding the feedback amplifiers used to increase the load impedance in the first stage there must be great care during design so that the gain in any of these amplifiers does not exceed a magnitude of one, in order to avoid negative resistance values. Considering that each differential amplifier that constitutes the feedback network for the active loads is balanced, Af and Af1 can be determined as

$$Af = \frac{gm_9}{gm_{11} + gds_9 + gds_{11}} \quad (4.22a)$$

$$Af1 = \frac{gm_{13}}{gm_{15} + gds_{13} + gds_{15}} \quad (4.22b)$$

Therefore to avoid that neither Af and Af1 go above one, gm_9 must be lower than gm_{11} and gm_{13} as to be lower than gm_{15} . This was accomplished by making M11 and M15 wider than, respectively, M9 and M13 in such a way that the gm for the load transistors would be superior, as gm is proportional to the width of a transistor, equation 2.10. Also, to avoid that any of the transistors would be in the limier of saturation a Vdd of 20V was used in order to have some margin for the

V_{GS} of the input transistors to increase due to the effect of the common-mode feedback network, as a compensation method for the increase of V_{th} .

In the schematic presented the biasing networks that produce the various reference voltages for the opamp are not represented as all of the bias voltages were kept external. In this way adjustments can be to the biasing voltages during circuit testing, if so is required.

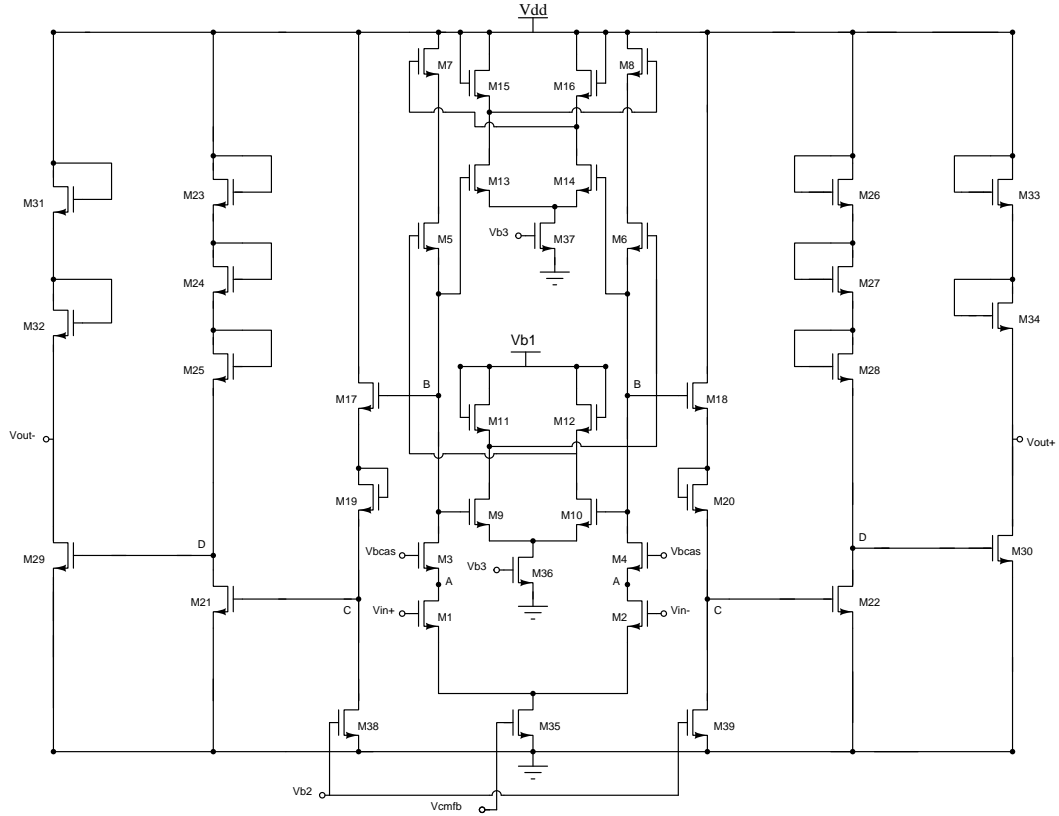


Figure 4.19: Schematic of the proposed opamp without frequency compensation

From figure 4.19 an approximation for the open loop gain of the topology, considering that $(1/gm)||r_o \simeq r_o$ can be determined by

$$A_d = -gm_1 \cdot ((gm_1 \cdot r_{o1} \cdot r_{o3} + r_{o1} + r_{o3}) || R_{load}) \cdot \frac{gm_{17} \cdot (r_{o38} + \frac{1}{gm_{19}})}{1 + gm_{17} \cdot (r_{o38} + \frac{1}{gm_{19}})} \cdot \frac{3 \cdot gm_{21}}{gm_{25}} \cdot \frac{2 \cdot gm_{29}}{gm_{31}} \quad (4.23)$$

R_{load} and the value of the factor a , which is necessary for its determination are calculated through the expressions in 4.24, while A_f and A_{f1} are calculated from 4.22.

$$R_{load} = \frac{r_{o5}}{1 - a - gm_5 \cdot (Af - 1) \cdot r_{o5}} \quad (4.24a)$$

$$a = \frac{gm_7 \cdot Af - gm_5 \cdot Af + gm_5 + gds_5}{gm_7 + gds_5 + gds_7} \quad (4.24b)$$

This topology is intended for $V_{dd}/2=10V$ as the common-mode level at the input and output. In terms of CM range, the input minimum and maximum voltage levels can be calculated as

$$V_{cmin,min} = V_{GS1,2} + V_{DS35,sat} \quad (4.25a)$$

$$V_{cmin,max} = V_{dd} - V_{DS7,8} - V_{DS5,6} - V_{DS3,4} + V_{th1,2}, \quad (4.25b)$$

where $V_{DS35,sat}$ is the minimum drain to source voltage for which transistor M35 is in still saturation.

Analysing the output swing, the maximum value is determined when the V_{GS} of both the diode connected transistors that compose the load of the output stage is equal to V_{th} . On the other hand, the minimum output level corresponds to the situation in which the drive transistor of the output stage is at the limit of saturation. To determine this voltage one must find the maximum V_{GS} for which the transistor is still in saturation, which considering that all the transistors in the output stage have the same aspect ratio and therefore the same V_{GS} , can be determine by the following set of equations

$$V_{dd} - 2 \cdot V_{GS29} \geq V_{GS29} - V_{th29} \quad (4.26a)$$

$$\Leftrightarrow V_{GS29} \leq \frac{V_{dd} + V_{th}}{3} \quad (4.26b)$$

$$V_{GS29,max} = \frac{V_{dd} + V_{th}}{3} \quad (4.26c)$$

Finally, $V_{out,min}$ is calculated as:

$$V_{out,min} = V_{dd} - 2 \cdot V_{GS29,max} \quad (4.26d)$$

$$V_{out,max} = V_{dd} - 2 \cdot V_{th} \quad (4.27)$$

These equations prove that, as expected, the necessity of using two diode connected loads to avoid V_{GS} values superior to 7V, leads to a reduction of the output swing of the topology as both the maximum and minimum voltage levels of the output are reduce when compared to the case of using only one diode connected load.

Table 4.6: Aspect ratios of the transistors

Transistor(s)	Aspect Ratio($\mu m/\mu m$)
M1,M2,M21,M22,M29,M30,M31,M32,M33,M34	320/20
M3,M4,M5,M6,M7,M8,M11,M12,M15,M16	160/20
M9,M10,M13,M14	90/20
M17,M18,M19,M20,M38,M39	40/20
M23,M24,M25,M26,M27,M28	80/20

Table 4.7: Bias Voltages of the opamp

Designation	Value(V)
Vdd	20.00
Vb1	17.50
Vb2	4.81
Vb3	2.50
Vbcas	13.00
Vbias	3.00
Vcmref	10.00

4.5.1 Frequency Compensation

As a multi-stage topology the opamp was at first unstable and therefore required the use of a frequency compensation scheme. However, the compensation of this topology proved to be a complicated task especially due to the source-follower in the second stage.

The first frequency compensation scheme applied was a cascode compensation [41] between the nodes highlighted as A and D in figure 4.19. This type of compensation is extensively used in amplifiers using a two-stage configuration that have a cascode in the input stage. The proposed opamp topology for this work is, however, different from those in which this scheme is usually employed, not so much because of the number of stages but because of the source-follower that is connected to the output of the first stage. In fact it is this source-follower that makes it impossible to use this frequency compensation scheme, as pole-zero analysis performed in simulation reported the presence of a right-half plane pole when it was used. After some theoretical analysis, the cause for this unexpected pole was found to be related to the input impedance of the source-follower stage. This impedance can be determined using the simplified schematic for the second stage of the opamp presented in figure 4.20. Using the small-signal equivalent for the transistor the input impedance of this stage is found to be

$$Z_{in} = \frac{1}{C_{GS} \cdot S} + \left(1 + \frac{gm}{C_{GS} \cdot S}\right) \cdot \left(\frac{R_L}{R_L \cdot C_L \cdot S + 1}\right) \quad (4.28)$$

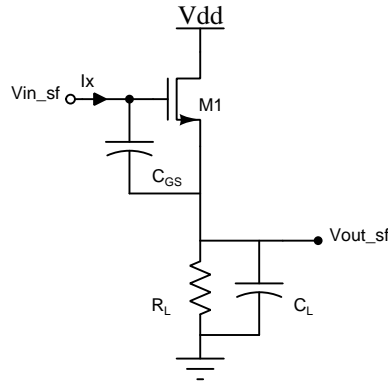


Figure 4.20: Schematic for the calculation of the input impedance of a source-follower stage

Focusing of the term representative of the equivalent load impedance, $R_L/(R_L.C_L.S + 1)$, it is clear that as the frequency increases at some point $|R_L.C_L.S + 1| \gg 1$ and the previous term will then simplify to $1/C_L.S$. Equation 4.28 is then rewritten as

$$Z_{in} = \frac{1}{C_{GS}.S} + \frac{1}{C_L.S} + \left(\frac{gm}{C_{GS}.C_L.S^2}\right) \quad (4.29)$$

Now if in this last equation $s = j\omega$, the impedance will present a negative real part equal to

$$Re(Z_{in}) = -\frac{gm}{C_{GS}.C_L.\omega^2} \quad (4.30)$$

It is this negative resistance that originates the right-half plane pole, because at certain frequencies the resistance presented above will be dominant in node B and the voltage gain across the compensation capacitor would then be positive instead of negative. This situation had not been previously reported for this compensation scheme because it usually applied to two stage opamps in complementary type transistors where the second stage is always a common-source stage.

After finding out that cascode compensation was not possible for the proposed topology the compensation of the topology was further analysed in order to come up with a new compensation scheme. The first step of this analysis was to determine in frequency what would be the relative position between all of the main poles of the topology from the analysis of the time constant associated to each node. From this analysis it was found that the dominant and the first non-dominant poles of the topology before compensation are the ones associated with nodes B and C, which are the nodes with the highest impedance. The third pole is associated with node D and the fourth with the output node of the topology. The expressions for the calculation of the time constants associated to the nodes of the opamp are presented in section A.3.1 of appendix A.

This finding led to the following conclusion, if Miller compensation is attempted by connecting a capacitance between nodes B and D only dominant pole compensation will be possible. This is so because such a compensation scheme would lower the frequency of the pole associated with node B due to the Miller multiplication of the compensation capacitor but the pole splitting effect would be carried out for a pole that is not the first non-dominant pole of the system. If this

topology was used, the opamp would have very low bandwidth because the dominant pole would have to be placed very close to the origin in order for the system to have a phase margin higher than 60° . Since the initial bandwidth before frequency compensation is already not that high due to large parasitic capacitances in a-GIZO TFTs, if the compensation is performed in this way a bandwidth of a couple tens of hertz would be achieved.

Ultimately two compensation schemes were used in an approach that was based in the opamp proposed by Young in [3] which from all of the topologies with only n-type enhancement transistors might be the one that is most similar to the one proposed, as it also utilizes a source-follower stage to perform level-shifting.

In the compensation scheme used, Miller multiplication was implemented by connecting a compensation capacitor between nodes C and D in order to set the dominant pole of the opamp at node C which has the second highest impedance of the topology, while moving the pole associated node D to higher frequencies. To deal with the right-half plane zero introduced by the feedforward path implemented by the compensation capacitor, a resistance is introduced in series with it in order to move this zero to the left-half plane so as to cancel one of the non-dominant poles of the system. In this case the frequency of the zero will be approximately given by

$$\omega_z = \frac{1}{C_c \left(\frac{1}{gm_{21}} - R_c \right)}, \quad (4.31)$$

where R_z is the resistance in series with the compensation capacitor. This resistance is implemented through a transistor in triode region considering that $R_{on} = 1/(\mu_n \cdot C_{ox} \cdot (W/L) \cdot (V_{GS} - V_{th}))$.

Because the pole at the output node of the input stage is placed in low frequencies and cannot be moved away from the origin, a bypass capacitor was introduced in the source follower. This capacitance will lower the frequency of the left-half plane zero associated with the source follower and will allow the compensation of the opamp with an appropriate phase margin if this zero is placed below the unity gain frequency in order to inject phase in the system. To verify the effect of the bypass capacitor on the source follower consider again figure 4.20. The capacitance C_{GS} provides a feedforward path for the signal at the gate of M1, and since the gain across this capacitance is positive a left half-plane zero at the frequency $\omega_z = gm_1/C_{GS}$ will be originated. By adding capacitance C_b in parallel with C_{gs} this zero will be shift towards a lower frequency, $\omega_z = gm_1/(C_{GS} + C_b)$. This zero could also be used to cancel the non-dominant pole of the system but in that case the bypass capacitor would have to be considerably big.

When compared to the results obtained if the compensation was realized by connecting the compensation capacitor between nodes B and C, the compensation scheme used allows for higher bandwidth and the use of lower values in the compensation capacitor. Still, the method used also has some disadvantages, the first being the necessity of using two extra compensation capacitors. However, the major drawback is related to the fact that the poles associated with the source-follower become complex conjugate instead of two different real poles. This means that even with the circuit presenting an appropriate phase margin there will be some overshoot in the opamp's step response [42, p. 190]. The poles of the source-follower become complex conjugate because

of the values of its input and output impedances, which are conditioned by the compensation capacitors and by the capacitive loading introduced in the input of the source-follower stage as a result of the two feedback networks used to increase the load impedance of the first stage.

The final schematic for the topology after the compensation scheme is added is presented in figure 4.21. The values of the components used for frequency compensation are

- $CC=120\text{pF}$
- $C_b=25\text{pF}$
- $R_c=200\text{k}\Omega$

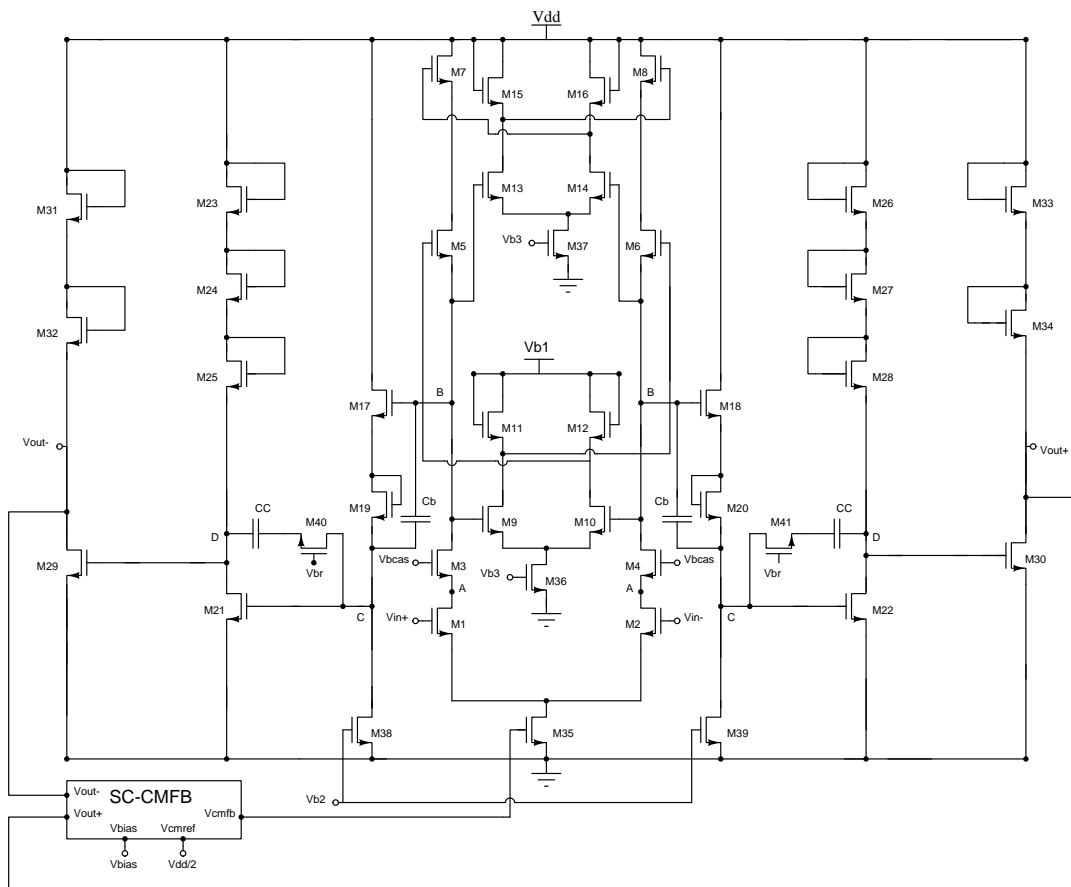


Figure 4.21: Complete schematic of the proposed opamp

These values were reached after an iterative process carried out during simulations and they are designed for a 100pF load capacitance. This value of load capacitance was selected because this capacitance is required to be much higher than the extra capacitive loading introduced by the CMFB network, which will have a minimum value equal to that of C_2 which was defined as 5pF .

The iterative process started with the definition of a value of $CC=100\text{pF}$ which is equal to that of the load capacitance. Then R_c was selected such that the zero introduced by CC would be

moved to a frequency close to that of the third pole of the system, which is the one associated with node D. After this the value of C_b was adjusted so that the opamp would present a phase margin of 45° , followed by a final tuning of the values of CC and R_c in order to ensure a phase margin above 60° .

Although the values presented above might seem to be considerably high, one should keep in mind that the values of transconductance for these transistors are in the order of tens of $\mu A/V$ and that due to their considerable dimensions they present parasitic capacitances in the order of some units of pF. Also, as there is no data regarding the accuracy of the values that were used for C_{GS} and C_{GD} in the simulations of the opamp, the values presented above are not guaranteed to work in the real circuit. They serve to validate the approach for the frequency compensation of the opamp, however, the components for frequency compensation of the fabricated circuit are expected to be of the same order of magnitude.

The results obtained for NMOS are in agreement with the ones presented above which in good extent also validates the approach for frequency compensation of the topology.

4.6 Simulation Results

The magnitude and phase of the open loop response of the opamp after frequency compensation are presented in figures 4.22a and 4.22b. In these results a left-half plane zero below the unity-gain frequency is clearly noticeable, as is its effect of increasing the phase of the system. This zero is the one associated with the source-follower, whose frequency was intentionally lowered through the use of a bypass capacitor. In table 4.8 the characteristics of the opamp that can be inferred from the simulated open-loop frequency response are presented.

Table 4.8: Characteristics of the opamp's open loop response

Gain	57.26 dB
Bandwidth	264.5 Hz
Unity-gain frequency	17.81 kHz
Phase Margin (100pF load)	68.83°

In table 4.9 the small-signal gain of each of the amplifiers stages is presented. As before, the gain of the differential stages used to implement feedback in the active load of the first stage are represented as A_f and A_{f1} and the third and fourth stages are designated as *Common-Source 1* and *Common-Source 2*, respectively.

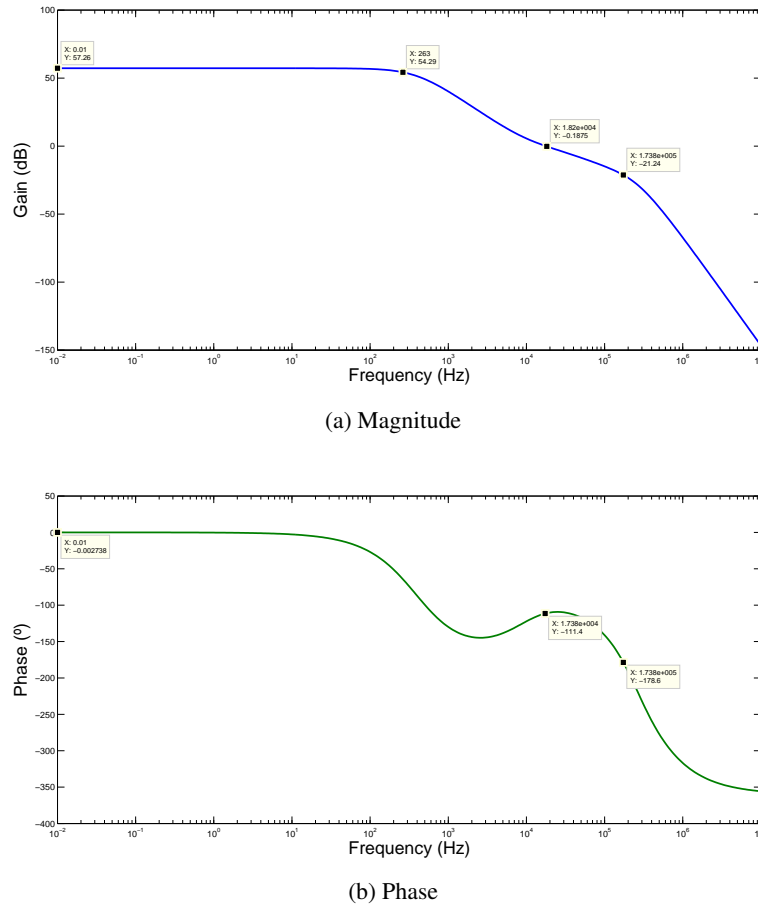


Figure 4.22: Frequency response of the a-GIZO TFT opamp

Table 4.9: Small signal gain of each stage of the opamp

Stage	Gain (dB)	Gain (V/V)
Input Stage	33.020	44.7300
Af	-0.240	0.9727
Af1	-0.149	0.9830
Source-follower	-2.597	0.7416
Common-Source 1	20.140	10.1625
Common-Source 2	6.701	2.1630

Here it is seen that the biggest part of the overall voltage gain is achieved in the input stage, also as expected the source follower introduces some attenuation but the two gain stages that come after it compensates this loss in gain.

Besides the analysis of the open-loop frequency response it is also important to analyse the performance of the opamp in terms of the rejection of common-mode signals, rejection of power supply noise and power consumption. The analysis of the common-mode rejection can be accomplished by applying the same signal to both of the opamp's inputs and measuring the voltage gain

for this case. Then the CMRR (Common-mode rejection ratio) can be determined by subtracting the obtained result to the differential gain of the opamp, with both gain values expressed in dB. The rejection of power supply noise can be determined by superimposing a signal to the power supply voltage while no signal is applied to the differential inputs of the opamp and then measuring the resulting voltage gain at the output. Then the PSRR (Power Supply Rejection ratio) is found as the difference between the differential gain, expressed in dB, and the gain of the signal applied in the power supply, also expressed in dB. The analysis of power consumption is fairly straight forward as it is directly obtained by the multiplication of V_{dd} with the total current in the opamp.

Currents per stage of the opamp are displayed in table 4.10. From these results it can be seen that the highest current consumption derives from the output stage. This high current is due to wide transistors and to V_{GS} values of 5V. To calculate the power consumption of the opamp all the currents must be added up, remembering that the source-follower and stages *Common-Source 1* and *Common-Source 2* must be accounted for twice since the opamp is fully-differential.

Table 4.10: Current per stage in the proposed opamp

Stage	Current (μA)
Input Stage	10.110
Af	5.465
Af1	5.473
Source-follower	5.558
Common-Source 1	15.010
Common-Source 2	49.490

Table 4.11 presents the results of all of the analysis mentioned above plus the analysis of input common-mode range, output swing and slew rate.

Table 4.11: Characteristics of the opamp that are not determined directly from the analysis of the open-loop frequency response

CMRR	90.35dB
PSRR	75.60dB
Supply Voltage	20V
Total Current	161.16 μA
Power Consumed	3.223mW
Input Common-mode range	3.6->10.5V (6.9V)
Output swing	5V->16.8V (11.8V)
Slew rate	0.03365V/ μs

The values for CMRR and PSRR are high especially taking into account that the differential gain is slightly inferior to 60dB. As for power consumption, it is low, as expected because of the low carrier mobility in the channel of a-GIZO TFTs. The total power consumption could be further reduced as there is margin to reduce supply voltage. Still, in technologies such as this one, biasing transistors with very low overdrive voltages should be avoided due to the increase in V_{th} as a result of constant bias stress. Also, even with a high supply voltage the proposed amplifier

could have potential application in the domain of photovoltaic panels where the voltage levels are usually superior to the supply voltage for which the opamp was designed.

The previous analysis were carried out for the complete amplifier topology. However since this topology has a CMFB network, the stability of this circuit must also be analysed, as the common-mode loop influences the response of the differential loop of the amplifier. This analysis was done in closed-loop using a fully-differential switched capacitor amplifier configuration, represented in figure 4.23, implemented with the proposed opamp. In this topology clk_1 and clk_2 are non-overlapping and the voltage gain is equal to C_1/C_2 . The results presented in figures 4.24a and 4.24b are relative to a 1kHz switching frequency in both the CMFB network and the switched capacitor amplifier. These results are resumed in table 4.12.

The information necessary to preform closed-loop stability analysis in Cadence Spectre is contained in appendix D.

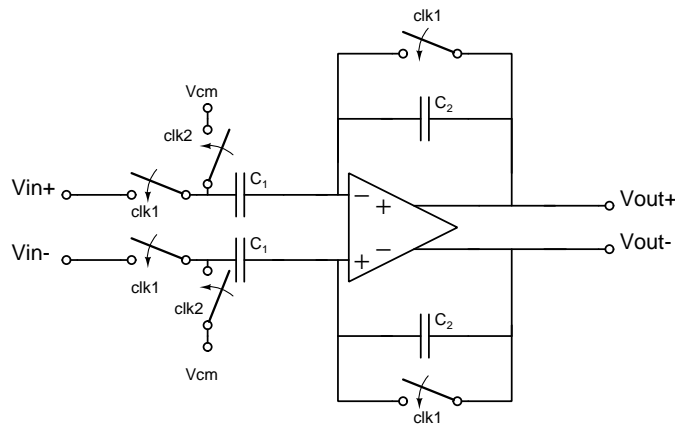


Figure 4.23: Fully-differential implementation of a non-inverting switched capacitor charge amplifier

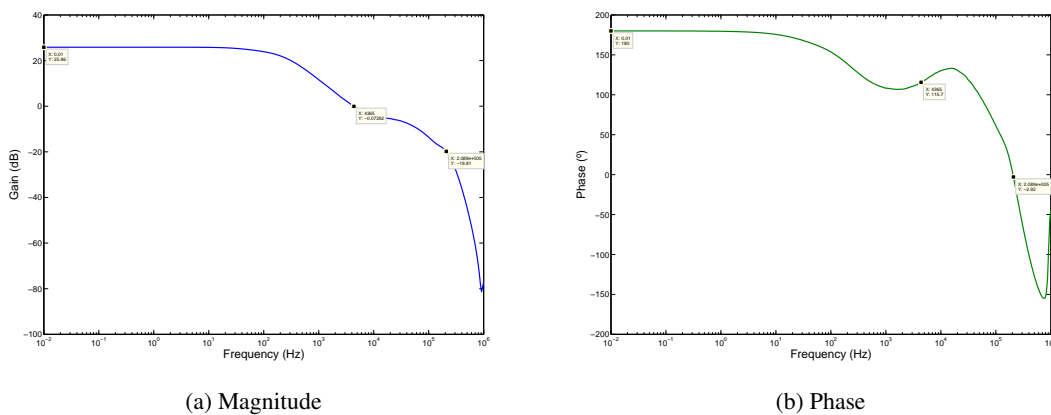


Figure 4.24: Frequency response of the CMFB network

Table 4.12: Characteristics of the frequency response of the Common-mode feedback loop

Gain	25.86 dB
Bandwidth	157.62 Hz
Unity-gain frequency	4.32 kHz
Phase Margin	115.5°

The stability analysis indicates that the CMFB loop is stable but that the gain of the loop is not very high. This low gain is caused by low common-mode gain of the input stage of the topology and it will be reflected in an offset of the common-mode level obtained at the output of the opamp, since the accuracy of the CMFB loop will be reduced. Also noted is the fact that the unity-gain frequency of this loop is lower than that of the differential loop. Because of this, some added distortion will be introduced in the differential response due to the low settling of common-mode components. Still, the lower unity-gain frequency for the CMFB loop was expected because all the stages of the opamp are included in it, and therefore the loop contains a significant number of poles. In fully-differential switched capacitor opamp design with CMOS this situation should be avoided, for example, by using two CMFB networks, one between the first stage and a stage in the middle of the topology and another from this last point to the outputs. However in the proposed opamp topology the use of two CMFB networks would require that the sensed CM level in at least one of these networks be inverted in order to have negative feedback across both CMFB loops. Also, one of these loops would have a very low-voltage gain and would originate a significant offset in the common-level at the output of the opamp. For this reason the trade-off was made between having more accuracy in the common-mode level at the output, at the cost of some extra distortion introduced by the fact that the common-mode component will have a slower settling time than that of the differential component.

Figure 4.25 represents the output of the common-mode feedback network and the respective common-mode level at the output of the opamp when no input is applied to the switched capacitor amplifier. The results obtained for settling time at 5% and steady state CM-level are presented in table 4.13. This results illustrate that the settling of the common-mode level takes some time but that the steady state common-mode voltage level for the output has an offset of only 0.1% in relation to the desired value which is $V_{dd}/2=10V$.

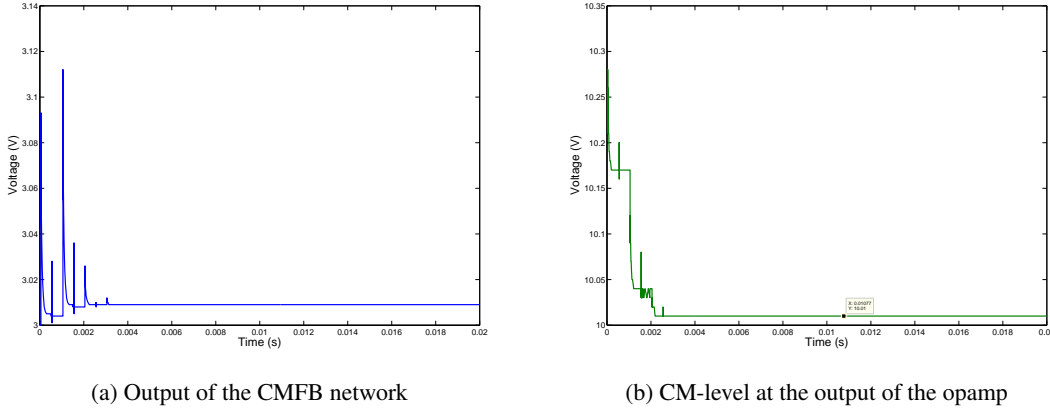


Figure 4.25: Transient response of the CMFB network and of the output of the opamp when no signal is applied

Table 4.13: Characteristics of the transient response of the CMFB circuit

Settling time (5%)	2.072ms
Output CM level (steady-state)	10.01V

All of these analysis of the SC-CMFB were performed using ideal switches instead of transistors to avoid convergence problems when the differential amplifier was set in closed-loop configuration. In open loop these problems did not exist. The ideal switches were defined as having an *on* resistance of similar magnitude to the *on* resistance of an $320/20\mu\text{m}$ a-GIZO TFT which is about $150\text{k}\Omega$. The reason for the convergence problem are the existence of leakage currents in the a-GIZO TFT characteristics represented in the model when $V_{GS} = 0$ and the fact that the model was not optimized for switching therefore during transients some of the constraints of the simulation software were violated. Many attempts were made to solve this issue such as using a model that approximated the characteristics of an a-GIZO TFT with the level 1 equation for a MOSFET device and using an altered version of the a-GIZO TFT neural network model. However only the use of ideal switches was able to solve the converge issue in simulations. Also, the level 1 model did not present a very good fit to the measured device characteristics. The I-V characteristics obtained for both the level one and neural network models are presented in appendix E.

After analysing the transient response of the common-mode loop, the closed response of the overall topology was then tested both for sinusoidal and step inputs. In the configuration C1 and C2 were set as equal in order to have unitary closed-loop voltage gain. In figures 4.26 and 4.27 the closed-loop response of the system for differential sinusoidal waves and differential voltage steps with an amplitude of 1V at a frequency of 100Hz are represented. From these results it is found that the topology behaves as expected in terms of gain and with the desired accuracy as it only has an offset of approximately 0.1%. There is, however, a visible overshoot which is due to the

existence of small-frequency complex poles in the open-loop response of the topology, but even with this pronounced overshoot there is no ringing effect noticeable in the output signal.

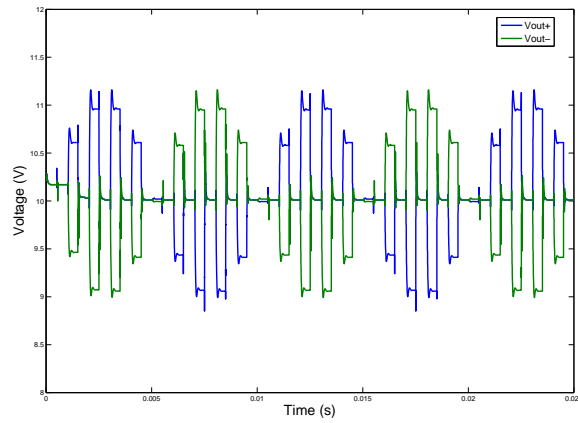


Figure 4.26: Transient response of the fully-differential switched capacitor amplifier when differential sine waves with 1V of amplitude at 100Hz are applied to the inputs

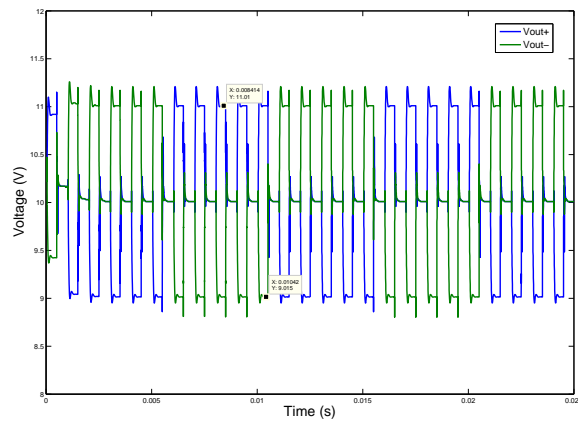


Figure 4.27: Transient response of the fully-differential switched capacitor amplifier when differential voltage steps with 1V of amplitude at 100Hz are applied to the inputs

Table 4.14: Step response results for the unity gain fully-differential switched capacitor amplifier

Steady-state error	0.098%
Overshoot	21.190%
Settling time (1%)	0.21ms

4.7 Layout

After designing the amplifier topology its respective layout was produced in order to fabricate the proposed opamp at CENIMAT.

4.7.1 Overview of layout design in the a-GIZO TFT technology used

The layout process in a-GIZO TFT is quite specific and requires an approach that is different from that used in common analog IC design. This difference stems from the fact that the technology library that is being used in this work does not present a complete behavioural model for a-GIZO TFT, as the devices intrinsic capacitances have not yet been characterized. For this reason additional precautions were taken to ensure that at least some important results could already be obtained from the first fabricated circuits. The expectation is that with a first fabrication run experimental data can be extracted about the characteristics of the individual stages that compose the amplifier in order to optimize it during a second try, as the behaviour of the proposed topology is highly dependent of the gain of the feedback networks for the input stage, which must be as close to one as possible to increase the gain of the opamp.

With these limitations in mind the approach was made of making a both complete and stage-by-stage layouts for the opamp. In this way there would be more flexibility in testing. Since the positive feedbacks are the most problematic stages 3 different version have been made in the final chip, each with different widths for the drive transistor, 90, 120, 140 μm . In all cases the diode connected load transistors have a width of 160 μm . The widths of the transistors for these stages have been kept intentionally high to guarantee that the gain does not exceed one. Also, as there is little information on the intrinsic capacitances of the transistors, the capacitances and resistances needed for the frequency compensation of the topology were not directly included in the layout. Instead, all of the nodes in which the compensation components must be connected are linked to external pads in the periphery of the circuits, making possible the compensation of the opamp using external components.

In terms of the layout design process with the a-GIZO TFT design kit used in this work there are significant differences when compared to analog layout design in CMOS, the most significant being the availability of only one level of metal for interconnections. In typical CMOS design there are several levels of metal that can be interconnected to implement complex routing schemes, in such a way that the total area of the circuits is reduced. Also, in our a-GIZO TFT technology design kit only two layers can be interconnect, therefore, the routing in complex topologies is more difficult and leads to an increase in circuit area.

The layers currently available in the design of circuits in a-GIZO TFT are presented in table 4.15 along with their respective colors. From now, on the layers will be referred to by the names attributed in this table and the colors indicated will correspond to the color of that layer in all of the layouts presented in this document.

Table 4.15: a-GIZO TFT Layer color scheme

Layer	Color
GATE	Red
SOURCE/DRAIN	Green
SEMICONDUCTOR	Blue
PASSIVATION	Magenta
METAL	Orange

In terms of functionality the layers can be characterized in the following way:

- GATE layer is used to implement the gate of the TFT. This layer is very similar in terms of functionality to the a poly-silicon layer in CMOS layout design. It is usually implemented in ITO, a material that is transparent but has a high resistivity, therefore all interconnections with this layer should be as wide and as short as possible. The only via to interconnect two different layers that exists, as of this time, for a-GIZO TFT layout design in the technology design kit used interconnects this layer and SOURCE/DRAIN.
- SOURCE/DRAIN is used to constitute the source/drain contacts of the TFTs and constitutes the equivalent of a metal layer in standard CMOS layout design. Since the material that constitutes this layer is typically a metal alloy like, for example, Ti/Au the longer interconnections should be implemented with it.
- SEMICONDUCTOR represents the semiconductor layer which corresponds to the active area in the transistors.
- PASSIVATION is only represented in pads although all of the chip is passivated during fabrication.
- METAL is used to represent the metal holes present in both vias and pads. It cannot be used as an interconnection layer in the design of layouts.

The information presented before constitutes only a slight overview on layout with a-GIZO TFTs. Additionally, there is a more detailed presentation on this subject in appendix C. Here the basic layout rules are displayed along with information on how to design basic components such as transistors, vias and pads.

The layout design kit for the a-GIZO TFT technology can be used with the layout editor of Cadence Virtuoso and it already possesses DRC (design rule check) and LVS (layout vs schematic). These tools are very important for the debugging process of the produced layouts and make the design process much swifter. On the other hand, the tool for parasitic component extraction is still under development so at the moment post-layout simulation is not possible. For this work the layouts were drawn entirely in Cadence Virtuoso.

After the layouts are completed they must be arranged in a chip of 2.5cm per 2.5cm as the one presented in figure 4.28 which corresponds to one of 3 chips sent for fabrication in this work.

This chip must have a border of 0.2cm all around and alignment marks must be placed along the border, hence the reason for the cross-like marks that can be seen in the figure.

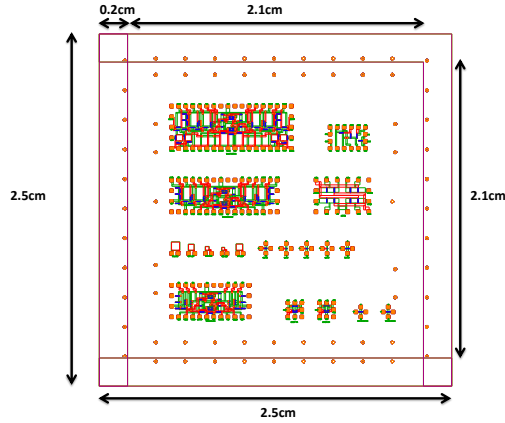


Figure 4.28: Example of a chip for fabrication

4.7.2 Layouts Designed

The layout of the the complete opamp is displayed in figure 4.29. In this layout there are no compensation components included and the CMFB network as also been left out. As there is no accurate idea on the capacitances values for C1 and C2, because they are dependent on the capacitances of the transistors in the biasing network, the CMFB loop has, therefore, been designed separately and also without any capacitors, instead there are pads that are connected to their respective nodes in order to allow their addition externally during testing. The layout of the CMFB network is presented in 4.30.

In the developed layouts the topologies are made completely symmetrical except for the positive feedback networks of the first stage due to inter-crossings. In terms of the area occupied these layouts are relatively big if compared to a layout in current CMOS technologies. Still, the need for a considerable area stems from the necessity of having external connections for the addition of frequency compensation components. All of these interconnections require pads and each one of these pads has an area of $62500\mu\text{m}^2$ ($250 \times 250\mu\text{m}^2$), and there should be sufficient spacing between them to allow wire bonding, therefore they are always spaced at least $250\mu\text{m}$. Also, all of the pads are placed in the periphery of the circuits so that no internal short circuits are caused during the execution of wire bonding.

Table 4.16: Layout areas

Layout	Area(mm^2)
OPAMP	14.375
SC-CMFB	10.000

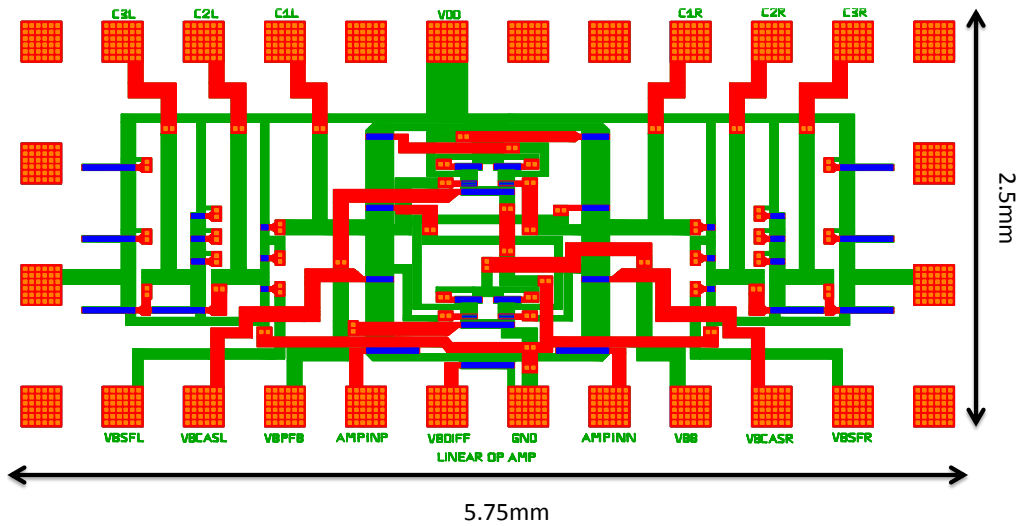


Figure 4.29: Layout of the proposed opamp

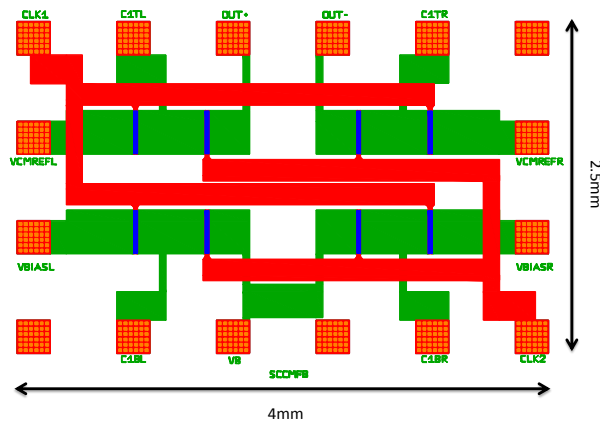


Figure 4.30: Layout of the Common-mode feedback network

In the layout here presented which corresponds to the final version of the circuits, the transistors are all drawn with direct layout. However, in the first layout produced all transistors presented a fingered structure and the input transistors of the differential stage were designed with an interdigitated configuration. The use of topologies with multiple fingers is commonly used in wide transistor to reduce the gate resistance as well as the total overlap capacitance between gate and

source/drain. On the other hand the use of interdigitated structures is commonly used in the layout of differential amplifiers to minimize mismatch, which hinders the performance of analog circuits [27, p. 635]. Figure 4.31 displays a multifinger version of a transistor with a channel width of $320\mu m$ and channel length of $20\mu m$. In figure 4.32 an interdigitated layout of two transistors, both with a width of $160\mu m$ and a length of $20\mu m$, is represented, a dummy gate is also added in each side of the structure so that both the transistors have the same surrounding environment in order to increase the matching between them. In both configurations the size of each finger is that of the minimum size transistor available in this technology, which has a width of $40\mu m$ and a length of $20\mu m$.

4.7.3 Problems when using multifinger structures for the fabricated a-GIZO TFTs

The reason for not using interdigitated or multifinger structures in the final layouts is that measures that were carried out during the work on transistors constructed with fingered structure showed that they were behaving as depletion type. Figure 4.33 displays the square root of I_{DS} in relation to V_{GS} of two transistors with $W/L=320/20\mu m$ both with and without fingered structure. To perform this analysis both transistors were biased with a V_{DS} of 14.5 V to ensure that when they are conducting they will always be in deep saturation, V_{GS} is swept between 0 and 10V. For the transistor with the multifinger structure it can be seen that the threshold voltage will be below 0V, which is not the case for the one with the direct layout. The threshold voltage is estimated as the intersection of the tangent (represented in green) of characteristic with the x-axis. The reason for this effect has not been completely determined by the team working in the a-GIZO TFT project at FEUP but it is thought that it may be caused by the non-interruption of the semiconductor layer below the source drain overlaps of adjacent fingers. Still, as the developed work is focused only in n-type enhancement transistors and as there is not enough data regarding the performance of the multifinger structures, in the final versions of the layouts all of the transistors have been drawn with the direct layout. However, the first chip was done before these results were known and it has also been sent for fabrication. In either case, individual copies of each transistor used in the circuits have been placed near each circuit in order to have an estimation of the behaviour of the transistors used by characterizing these replicas.

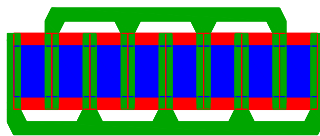
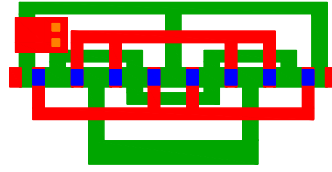
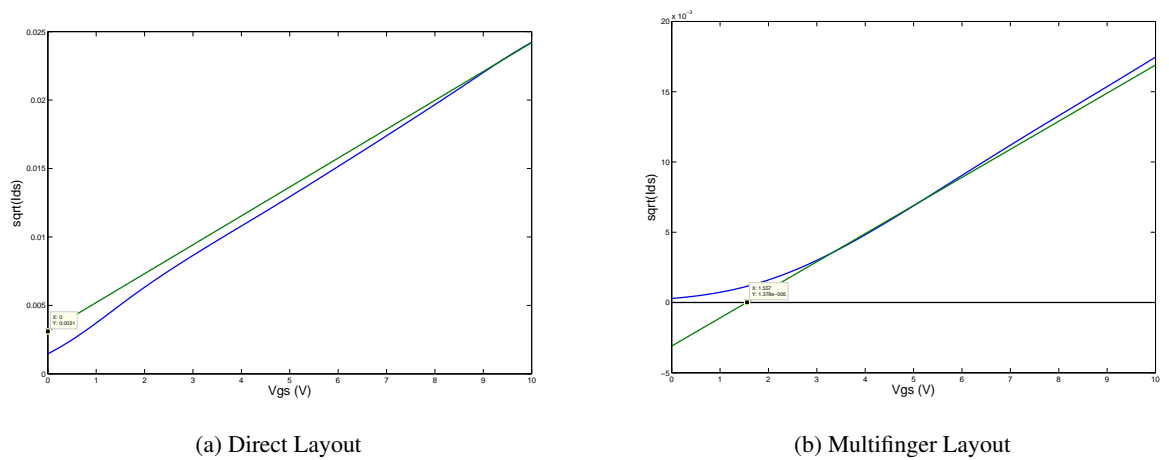


Figure 4.31: Multifinger layout for an a-GIZO TFT with $W/L=320/20\mu m$

Figure 4.32: Interdigitated layout of two 160/20 μm a-GIZO TFTsFigure 4.33: $\sqrt{I_{DS}}$ for various values of V_{GS} for 320/20 μm a-GIZO TFTs with different layout structures, results obtained from physical circuits

The layouts of individual stages of the the proposed opamp both with and without multifinger structures as well as the layouts for the other high-gain stages analysed in this chapter are presented in appendix C. The layouts of the other high-gain stages were drawn to preform the comparison of these topologies to the novel topology used in the input stage of the opamp.

4.8 Summary

In this chapter the proposed a-GIZO TFT opamp was presented along with the constraints and the methodology associated with its design process. The proposed topology was analysed both theoretically and through the results obtained in simulation. Finally the produced layouts are presented and discussed.

The proposed topology is a fully-differential 4-stage opamp implemented with only n-type enhancement transistors. This opamp is directed for application in switched capacitor circuits. As a unique characteristic it employs a novel topology in order to implement a cascode load in the input stage and increase the overall gain. In this way a considerable gain can be achieved without having to use very wide transistors or considerably big differences between the aspect ratios of the

transistors used, as the ratio of the W/L between the biggest and smallest transistors used is only 8.

This topology was presented, analysed and compared to other topologies that are used to increase the load impedance of gain stages in technologies possessing only a single type of transistor. Although the novel topology for high-gain has the highest power consumption and number of transistors between all of the topologies analysed, it is the one that assures the highest voltage gain while being able to amplify dc signals. However, the use of this topology requires a cascade structure at the input which lowers the input common-mode range and increases the required supply voltage. Another advantage of this novel topology, which is shared by all implementations that use differential feedback in the active load, is that it offers a high rejection of common-mode disturbances. This is characteristic stems from the topology presenting a lower impedance for common-mode than for differential signals.

Due to its structure and the use of multiple stages the frequency compensation of the opamp is complex, especially because of the source follower stage. After compensating the opamp with a phase margin above 60° , the existence of low-frequency complex poles associated with the source follower leads to the presence of some overshoot in the closed-loop response of the amplifier.

Since the a-GIZO TFT technology presents a shift in V_{th} overtime due to constant bias stress precautions have been taken to reduce this effect in the topology. Therefore, common-mode feedback was applied to the circuit and very low overdrive voltages were avoided.

In terms of the produced layouts care was taken to ensure symmetry in order to increase matching but multifinger and interdigitated structures are avoided in the final versions of the circuits sent for fabrication.

The results presented are all taken from measures performed in simulation. In simulations the parasitic capacitances of a-GIZO TFTs were approximated using the Meyer Capacitance Model in order to have a rough estimate on the frequency behaviour of the proposed topology. However, at this time there is no information regarding the accuracy of this model in the estimation of the intrinsic capacitances of a-GIZO TFTs, although it has been reported that for OTFTs the model provides a good approximation.

In terms of potential fields of application the opamp proposed can be best suited for use in the domain of photovoltaic panels as the voltage levels in such applications tend to be superior than the supply voltage for which it was designed, 20V.

Chapter 5

Switched Operational Amplifier with a-GIZO TFTs

Based on the opamp topology presented in the previous chapter there was the idea of changing the biasing scheme so that it would be *pulsed*. This idea stemmed from results presented for digital a-GIZO TFT circuits, reporting increased circuit lifetime when the transistors would not be constantly *on*, but switched *on* and *off* [17]. Such a concept exists also for operational amplifiers in CMOS technologies which are designated as switched opamps. This concept, previously introduced in chapter 2.6.5 is used in switched capacitor circuits in which low-power consumption and low supply voltages are required. However, in this work this concept is adopted for a-GIZO TFTs in order to guarantee that none of the transistors of the opamp will be constantly biased during the operation of a switched capacitor circuit. In this way the effect of gate bias stress on the transistors is expected to be less significant. This chapter reports the steps involved in the design of a novel switched capacitor with only n-type a-GIZO TFTs. In it the major advantages and limitations of the topology are presented. Also presented are the results obtained in simulation for both this novel topology and a sample-and-hold circuit that was implemented with it. This sample-and-hold circuit is based upon the topology proposed in [11].

As for the previous operational amplifier, for the switched opamp a preliminary set of performance goals was defined to serve as guideline during design. The methodology used was exactly the same as in the design of the previous topology, which is detailed in 4.1.

5.1 Performance Goals

The first consideration that must be taken into account is that unlike the switched opamps in CMOS the main objective of making the a-GIZO TFT opamp switched is not to reduce power consumption or the supply voltage. Nonetheless, power consumption will always be reduced as a consequence of switching-off the amplifiers stages. The main purpose is to reduce the effect of bias stress while keeping the same dc gain that was verified in the non-switched version of the opamp. Still, there must also be concern with the maximum allowed switching speed for the

opamp, because in switched capacitor circuits using this type of amplifier the circuit is switched at the same frequency as the opamp. Also, in terms of techniques that can be used to increase switching speed, only switching-off the output stage is not an option. This is so because all of the a-GIZO TFTs in the circuit will suffer from gate bias stress if constantly biased. For this reason in this design the biasing of all the stages of the opamp have to be disconnected when the amplifier is switched-off.

All things considered the set of goals that was defined maintained the goals of the opamp presented in the previous chapter 4.2 with a single extra addition:

- Every transistor in the topology has to be cut-off ($V_{GS} = 0$) in one of the two clock phases.

Although not set has a mandatory goal care was also taken to increase the switching speed.

5.2 Design of the Switched Operational Amplifier Topology

The core of the proposed switched opamp is the novel topology presented in the previous chapter excluding the common-mode feedback network. This choice was made because the aforementioned topology had already been studied and showed interesting results in simulation. Therefore the work develop aimed at the adaptation of the previously proposed topology rather than designing another opamp topology completely from zero.

The first step of this conversion process was the definition of a method to set the bias voltages for the stages of the amplifier to zero during the *off* phase. This was achieved by using pull-down transistors connected to the biasing networks of the stages. This approach is the same one taken in [8] and it is depicted in figure 5.1. The working principle of this topology is fairly straightforward. When *clk* is high, V_{bias} will have a value of some tens of mV due to the pull-down realized by transistor M_{pd} . This low voltage level when applied to the gate of a transistor will put it in cut-off. On the other hand, when *clk* is low V_{bias} will have the desired level to bias the transistor it is applied to because M_{pd} will act as a very high impedance.

In terms of the clock signal the maximum voltage allowed for switches in this configuration is 7V in order to avoid damaging the transistor used as a switch. As the clock signal as a voltage level considerably lower than V_{dd} all of the pull-down switches were implemented with the biggest transistor that can be simulated by the model, $W/L = 320/20\mu m$, to guarantee that the bias voltages will be pulled as closed to 0V as possible during the off-phase of the opamp.

Recalling the original topology, depicted in 4.21 it is easy to see that the approach explained above does not suffice to turn-off all of the transistors in the core of the amplifier. The common-source stages would still be biased with $V_{GS} > 0$ even when the secondary bias voltages are set to zero because V_{dd} must remain applied to the circuit. Therefore, an additional mechanism must be used to cut-off all of the transistors in the common-source gain stages. The solution developed to solve this problem is depicted in figure 5.2. When V_{bias} is at the level that adequately biases the second stage *clk1* will be high and *clk2* will be low. In this way V_{bias} is applied to the gate $M4$ through $S1$ which is in triode and the common-source stage is adequately biased because $S2$,

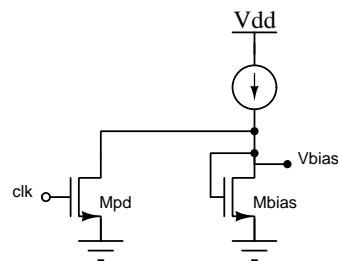


Figure 5.1: Generic topology to implement a pulsed biasing scheme

which is cut-off, acts as a high-impedance. On the other hand when V_{bias} is pulled to a level close to ground, the voltage at the source of M2 will be equal to the dc level of $V_{in_{sf}}$ minus a slight drop in M1 and M2 because these are n-type transistors. If this voltage level was applied to the gate of M4 at least this transistor would still be conducting, which is undesired. Therefore when V_{bias} comes close to 0V $clk1$ will be low and $clk2$ will be high. In these circumstances both the stages will have all transistors cut-off but at the cost of using two switches.

This switching scheme is also used between the third and fourth stages for the same reasons explained before. In this way all of the stages of the amplifier will be cut-off when the amplifier is switched *off*.

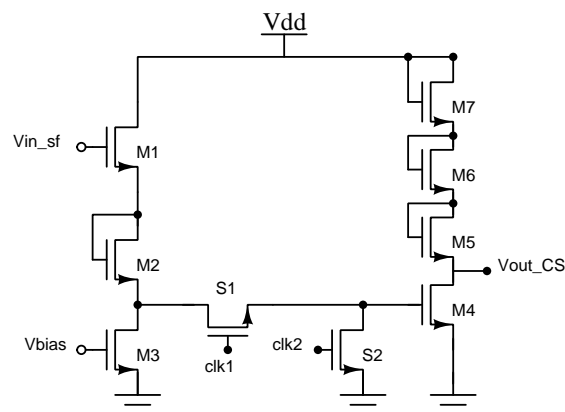


Figure 5.2: Switch-off mechanism for the first common-source stage

Already a considerable amount of switches are necessary to cut-off the transistors in the amplifier stages of the opamp, but extra switches are required to rail the output to V_{dd} when the amplifier is *off*. Setting the output to V_{dd} is not actually mandatory for a switched opamp, but it is common practice to either set V_{dd} or Gnd at the output when the amplifier is *off* in order to avoid constant offsets. In the case of the proposed topology, just switching-off the biasing for every stage does not impose V_{dd} at the output, but a level somewhat below this voltage. This happens because the active loads in the output stage are diode connected n-type transistors, therefore even when the drive transistor of this stage is cut-off there will still be a slight voltage drop across the active loads, although the output is still in a high impedance state. To solve this problem and set

V_{dd} at the output when the amplifier is *off*, additional switches were added in the output stage as depicted in 5.3. These switches short-circuit the gate and source terminals of each of the diode connected load transistors of this stage and thus the output will be set to V_{dd} . However, there is a drawback associated with this method, which is, $clk3$ will have to possess a high voltage level of at least $V_{dd} + V_{th}$ or otherwise the topology will not work. This means that to have the complete system-on-chip a charge pump will be required to generate this clock.

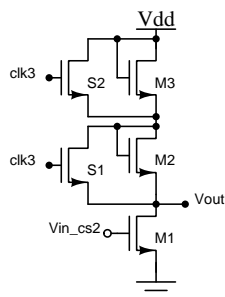


Figure 5.3: Schematic of the output stage of the switched opamp

As the switching speed is very important for the performance of circuits with switched opamps additional mechanisms were added in order to decrease the time necessary to complete recovery from the *off* phase. This time represents how long it takes for the output of the opamp to go from V_{dd} to $V_{dd}/2$ after the biasing is switched-on for all the stages. The aforementioned voltage levels represent, respectively, the voltage level at the output when the amplifier is turned *off* and the common-mode voltage level at the output during regular operation.

To improve the turn-on speed two techniques were used. The first one consisted in switching-off the transistors in triode which are in series with the compensation capacitors (CC). This is accomplished by pulling close to zero the biasing voltage for these transistors during the *off* phase of the opamp in the exact same manner as illustrated in figure 5.1. In this way these compensation capacitors remain charged during the off time, therefore reducing the turn-on time [9]. The second technique used for this purpose consisted in altering the number of stages that are included in the CMFB loop. In the previous topology all of the stages of the opamp were included in this loop because of the shift in V_{th} . However, in this topology the output of the CMFB circuit is applied to the biasing transistors of the source follower rather than those of the input stage. This in turn will increase the speed of the CMFB circuit. Although the CMFB circuit could in fact be excluded since the pulsed biasing of the amplifier is expected to reduce the shift in V_{th} , it was kept because it is expected to further increase the lifetime of the circuit. The circuit used for the CMFB network had to be specifically adapted for the context of switched opamps, therefore the topology used was that proposed in [10], as it does not require the introduction of extra poles in the CM loop and can be adapted to the a-GIZO opamp with only some minor modifications. A representation of the common-mode feedback circuit employed is presented in figure 5.4.

Regarding the original topology only three modifications were made. The first one is the

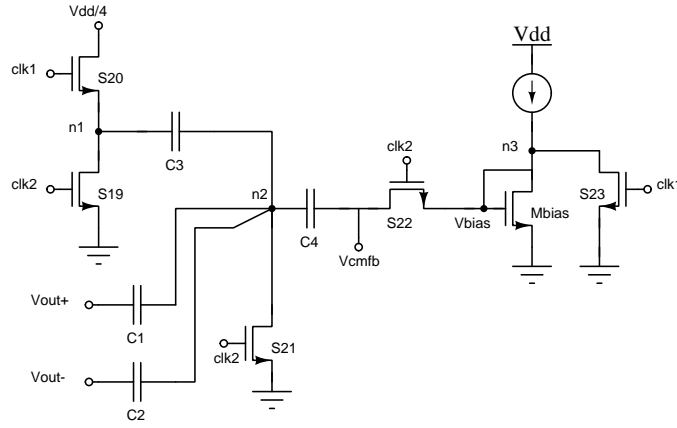


Figure 5.4: CMFB circuit of the proposed switched opamp

substitution of all the switches implemented with p-type transistors by n-type transistors, as complementary devices are not available in this technology. The second alteration is related with the relative sizes of capacitors. In the original circuit C_1 , C_2 and C_3 all had the same dimensions and therefore C_3 was connected to V_{dd} during the on phase of the opamp. This is not possible with the a-GIZO TFTs used because in the instant when clock would go high S_{20} would have a V_{GS} value that would damage the transistor as $clk1$ would necessarily have a high level above $V_{dd} + V_{th}$ and node $n1$ is set to ground in the instant there is a rising-edge of $clk1$. Since in all the designs a V_{GS} above 7 is avoided, instead of connecting C_3 to V_{dd} it is connected to $V_{dd}/4$ which for this topology is 5V. In this way not only can the high level for the clock at the gate of S_{20} be lower, but also there will be no damage in S_{20} as this switch can be operated by a clock with a high voltage level of 7V. However, changing the reference voltage from V_{dd} to $V_{dd}/4$ imposes that C_3 must have a capacitance four times bigger than those of C_1 and C_2 , otherwise the circuit will not function properly. A drawback of increasing the size of C_3 in relation to that of C_1 and C_2 is the reduction of the inherent gain of the topology which is $(C_1 + C_2)/(C_1 + C_2 + C_3)$. The final alteration performed is the addition of a pull-down switch to the circuit that is used to precharge C_4 during the *off* phase of the amplifier. In this way no transistor in the amplifier will be conducting in both clock phases.

In terms of the clocks represented in figure 5.4 $clk1$ and $clk2$ have the same high voltage level but have opposite phases. Designating the high phase of clock $clk1$ which corresponds to the *on* as ϕ_1 and the high phase of $clk2$ in which the amplifier is *off* as ϕ_2 , the charge equations for each clock phase are given by

$$Q_{\phi_1} = (V_{out+on} - V_{n2\phi_1}) \cdot C_1 + (V_{out-on} - V_{n2\phi_1}) \cdot C_2 + \left(\frac{V_{dd}}{4} - V_{n2\phi_1}\right) \cdot C_3 + (V_{n2\phi_1} - V_{cmfb}) \cdot C_4 \quad (5.1a)$$

$$Q_{\phi_2} = (V_{out+off} - 0) \cdot C_1 + (V_{out-off} - 0) \cdot C_2 + (0 - 0) \cdot C_3 + (0 - V_{bias}) \cdot C_4 \quad (5.1b)$$

Considering that $V_{out+on} = V_{out-on} = Vdd/2$, $V_{out+off} = V_{out-off} = Vdd$, and $C_3 = 4 \times (C_1)$ and $C_1 = C_2$ and assuming that there is no charge leakage so $Q_{\phi_1} = Q_{\phi_2}$ the equations are rewritten as

$$\begin{aligned} (Vdd/2 - V_{n2\phi_1}) \cdot C_1 + (Vdd/2 - V_{n2\phi_1}) \cdot C_2 + \left(\frac{Vdd}{4} - V_{n2\phi_1}\right) \cdot C_3 + (V_{n2\phi_1} - V_{cmfb}) \cdot C_4 = \\ = Vdd \cdot C_1 + Vdd \cdot C_2 - V_{bias} \cdot C_4 \end{aligned} \quad (5.2)$$

From this last equation it is found that for the circuit to work correctly $V_{n2\phi_1} = 0$ and $V_{bias} = V_{cmfb}$.

In terms of the dimensions of the capacitances of the circuit, C_1 and C_2 were made equal to 10pF and C_3 and C_4 equal to 40pF. The selection of the capacitance value for C_4 depends on the gate capacitances of the bias transistors in the source follower as the output of the CMFB circuit is connect to these transistors. Designating as A_0 the gain between the point where the output signal of the CMFB circuit is applied and the opamp outputs, the gain of the CMFB loop is determined as

$$A_{SOCMFB} = \frac{C_1 + C_2}{C_1 + C_2 + C_3} \cdot \frac{C_4}{C_4 + C_p} \cdot A_0 \quad (5.3)$$

Since the term $(C_1 + C_2)/(C_1 + C_2 + C_3)$ makes the inherent gain of the CMFB circuit equal to 2/6 and A_0 is approximately equal to 27dB then the term $(C_4)/(C_4 + C_p)$ should be as close to one as possible. Otherwise, the gain of the common-mode loop will be very reduced, causing a considerable offset in the common-mode level at the output of the switched opamp. Since C_p is estimated as approximately 545fF, by making $C_4 = 40pF$, $(C_4)/(C_4 + C_p)$ will be approximately 0.987. This way, the gain of the common-mode feedback loop will mostly depend on the gain of the two common-source stages and on the inherent gain of the level-shifter in the CMFB circuit.

The last step needed to finish the topology is guaranteeing that the during ϕ_2 the voltage at the output of the CMFB circuit (V_{cmfb}), which is set to V_{bias} , is not applied to the gates of the load transistors in the source-followers, M38 and M39. This can be accomplished by using a series switch and a pull-down switch, which is the same mechanism used to turn-off the common-source stages. In this way, when the amplifier is *on* the output voltage of the CMFB circuit is applied to the active load of each source follower, but when the amplifier is off the output of the CMFB circuit is in high impedance and all the transistors in the source follower are cut-off.

5.3 Complete topology for the novel a-GIZO TFT switched opamp

The complete schematic for the proposed switched opamp is presented in figure 5.5. In this schematic the biasing schemes are not represented and the block designated *CMFB* corresponds to the schematic presented in figure 5.4. The transistors in the core of the amplifier (represented as M) are exactly the same as in the opamp presented in the previous chapter and their aspect ratios can be found in table 4.6. The transistors used for switching (represented as S) are in total 23 and

all have the maximum size that can be simulated with the model which is $320/20\mu m$. The maximum size was selected because these TFTs have a high on resistance and therefore to minimize it as much as possible the biggest size of transistor is used. The significant number of switches is justified by the lack of complementary device, the limitations of not having V_{GS} above 7V which makes it necessary to use two diode connected loads in the output stages and the need to cut-off all the transistors of the amplifier stages during the *off* phase of the amplifier. Overall the topology has 64 transistors, without accounting for the transistors necessary to generate all of the biasing voltages from Vdd which would increase this number further. Another limitation of this topology is the number of clocks that must be used, as although there are only two different clock phases, clocks with different high level voltage are required. Also, since all of these voltages levels are different from Vdd there is the need to generate these voltages if complete system-on-chip is to be implemented. The high level voltage and phase for each clock are presented in table 5.1, with ϕ_1 representing the phase in which the opamp is *on* and ϕ_2 the phase in which it is *off*.

Table 5.1: High voltage level and phase of each clock in the novel switched opamp

Clock	High voltage level(V)	Phase
clk1	7	ϕ_1
clk2	7	ϕ_2
clk3	23	ϕ_2

The bias voltages for this opamp are very similar to those of the opamp presented in chapter 4. The biggest difference is that the reference bias voltage for the common-mode feedback circuit is now the bias voltage of the source-follower stage. All of the biasing voltages of the topology are presented in table 5.2.

Table 5.2: Bias Voltages of the switched opamp

Designation	Value(V)
Vdd	20.00
Vb1	17.50
Vb2	3.00
Vb3	2.50
Vbcas	13.00
Vbias	4.81
Vdd/4	5.00

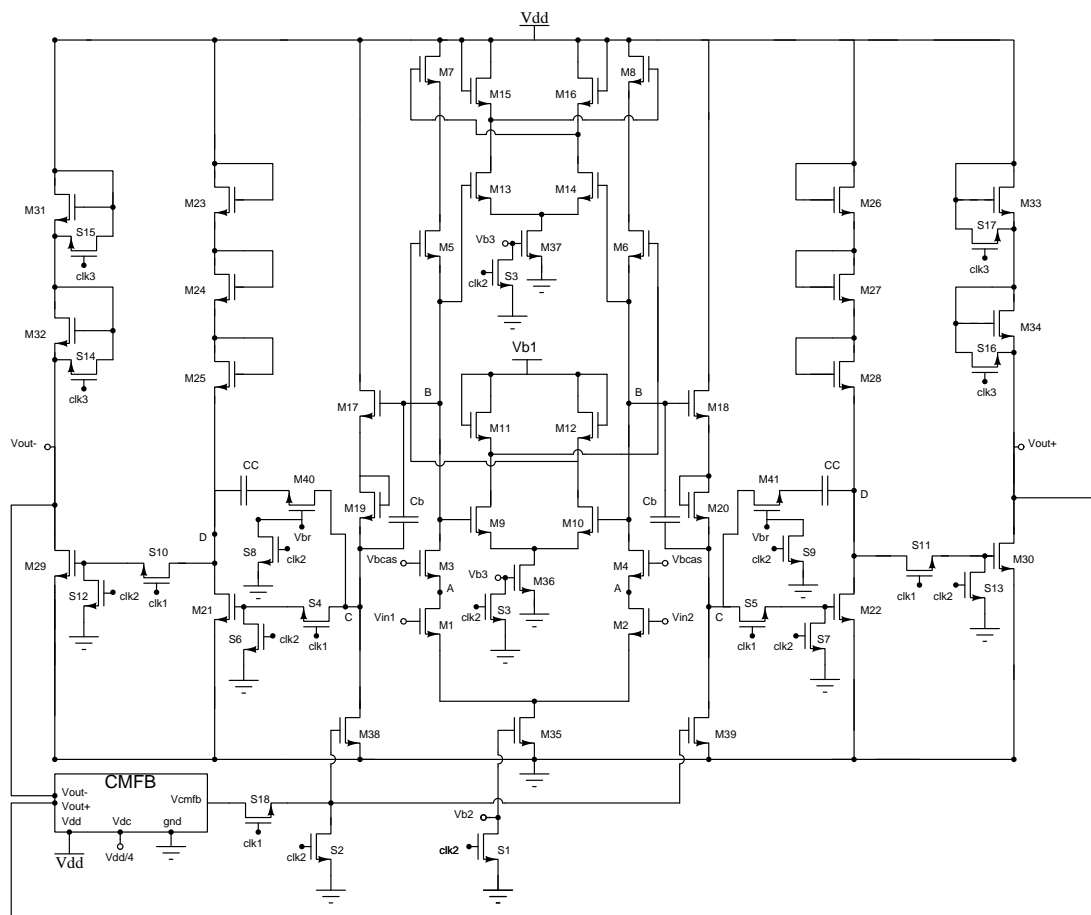


Figure 5.5: Complete schematic of the novel switched opamp with a-GIZO TFTs

Note that in the schematic although S3 is represented twice it is in fact a single transistor as all nodes connecting to Vb3 are interconnected. The drawing is done in this way to emphasize that there are pull-down switches for every bias voltage in the opamp.

5.3.1 Frequency Compensation

The principle of frequency compensation is exactly the same one used for the core opamp topology, explained in 4.5.1. However, if the exact same values presented for the previous opamp are used in this topology the phase margin will be inferior for the same value of load capacitance, 100pF. The cause for this are the series switches (S4, S5, S10, S11) that are connected to the gates of the drive transistor in each of the common-source stages. These switches constitute a resistance in series with the gate of the input transistor of each of the common-source stages and they will increase the poles associated with these nodes [27, p. 172]. As a consequence the pole at the output node of the third stage will occur in a lower frequency than in the case of the non-switched opamp.

The compensation of this topology is then done iteratively in simulation using the values of CC , C_b and R_c on the previous opamp as a starting point and then increasing CC and C_b . The increase of CC will bring the poles associated with the source follower closer to the origin while at the same time moving the pole at the output of the third stage to higher frequencies (pole splitting). On the other, hand increasing C_b will lower the zero of the source follower which is used to increase the phase of the system below the unity gain. The final values used for CC , C_b and R_c were the following:

- $CC=140\text{pF}$
- $C_b=30\text{pF}$
- $R_c=200\text{k}\Omega$

From these values it can be seen that for the switched opamp topology there is a slight increase in the values of CC and C_b when compared to the ones used for the non-switched version.

5.4 Implementation of a Sample-and-Hold with the proposed switched opamp

With the switched opamp designed its application in a circuit was necessary not only to verify the performance of the proposed topology but also to demonstrate that it can be used as a block in a signal processing chain. For this reason a S/H (Sample-and-Hold) circuit was built using the proposed opamp. This S/H is intended to constitute the first block of more complex applications such as ADCs.

This topology was previously proposed in [11], however, alterations were made to adapt it to the common-mode voltages levels of the developed switched opamp and the lack of complementary devices in the technology used. The S/H implemented is depicted in figure 5.6. As in the original topology a loading free architecture can be employed by taking the outputs from the opposite plate of capacitors C_h , providing that the opamp in the next stage of the signal processing chain has virtual ground voltage level of $V_{dd}/2$. Here however, the outputs of the circuit are defined as the output nodes of the switched opamp because the sample-and-hold is not included in a more complex signal processing circuit.

All the switches represented are implemented with n-type transistors. Consequently again for these transistors there will be the need for a clock with a high level voltage equal to at least $V_{dd}+V_{th}$. The phase and high voltage levels for each of the clocks represented are present in table 5.3. With ϕ_1 again representing the phase in which the opamp is *on* and ϕ_2 representing the *off* phase. Note that the value of the high level voltage for clocks $clk1a$, $clk2a$, $clk2c$ is defined as 17V in order not to exceed a V_{GS} of 7V in the switching transistors. This of course limits the maximum amplitude of the input signals of the S/H because switches $S1a$ and $S1b$ are in series with the input. Also, the clock $clk2c$ has a different clock phase which is represented by ϕ_2d ,

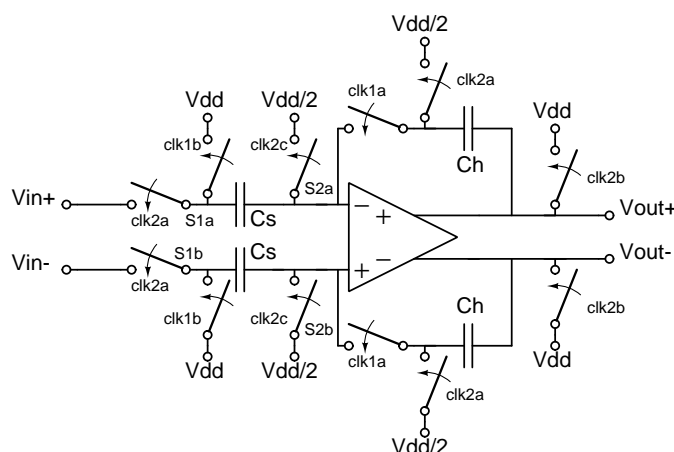


Figure 5.6: Schematic of the sample and hold circuit implemented with the proposed switched opamp

because it has exactly the same phase and period as clocks with phase ϕ_2 but its pulse width is slightly inferior. This clock is made different in order to implement bottom plate sampling [36, p. 841]. In this way, in the final stages of the sampling phase switches $S2a$ and $S2b$ will open first than $S1a$ and $S1b$ causing a constant injection of charge in C_s . Then when switches $S1a$ and $S1b$ open the capacitors C_s are in open circuit, therefore the charge injected by these switches will go to the path of least impedance which is back to the input terminals of the S/H circuit, V_{in+} and V_{in-} . In this way the effects of charge injection on C_s become constant and independent from the input signals. This constant offset is cancelled due to the differential operation of the topology.

The complete number of clocks required to operate this circuit also takes into account those needed to operate the switched opamp, represented in table 5.1. Therefore the circuit will require clocks with 3 different high level voltages and a total of 7 different clocks since $clk2b$ of the S/H is equal to $clk3$ of the switched opamp.

Table 5.3: High voltage level and phase of each clock exclusive to the S/H

Clock	High voltage level(V)	Phase
clk1a	17	ϕ_1
clk1b	23	ϕ_1
clk2a	17	ϕ_2
clk2b	23	ϕ_2
clk2c	17	ϕ_{2d}

In terms of operation of the circuit the opamp will be *off* during the sampling phase, in which capacitors C_s are connected between the input signal and $V_{dd}/2$, the output of the opamp is pulled to V_{dd} and C_h capacitors are reset. In the holding phase the opamp is turned on, the feedback loop across it is closed and the plate of C_s that is not connected to the opamp's input is connected to V_{dd} . The charge equations for the sampling and holding phases are defined as

$$Q_s = \left(V_{in} - \frac{V_{dd}}{2}\right).C_s + \left(V_{dd} - \frac{V_{dd}}{2}\right).C_h \quad (5.4a)$$

$$Q_h = (V_{dd} - V_{dd}/2).C_s + (V_{dd}/2 - V_{out}).C_h \quad (5.4b)$$

Since the common-mode levels for both the input and output of the opamp are defined as $V_{dd}/2$ and the input signals are made to have the same common-mode level, then $V_{in} = V_{dd}/2 + V_{signal}$ and $V_{out} = V_{dd}/2 + V_{signal}$, as the sampled signal charge in capacitors C_s is transferred to capacitors C_h during the holding phase. Also, $C_s = C_h$ making $Q_s = Q_h$ and therefore the circuit will function correctly, assuming that there is no charge leakage.

5.5 Simulation Results

Before displaying the results obtained it is important to note that as in the CMFB feedback circuit for the previous opamp, which was switched, there were also convergence problems in the simulation of the sample and hold circuit. Therefore for the simulation of the complete sample and hold circuit all of the transistors used as switches were substituted by ideal components with an on resistance similar to the on resistance of an $320/20\mu m$ a-GIZO TFT which is about $150k\Omega$. As in the previous case only the use of ideal switches proved able to solve the convergence problems in the simulations with a-GIZO TFTs. The use of ideal switches means that in the simulation results no clock feedthrough or charge injection effects are taken into account. These effects will exist in the fabricated circuits which for this reason are expected to have worse performance than the indicated by the simulation results.

5.5.1 Switched Opamp

The simulation results for the frequency response are presented in figure 5.7.

These results are very similar to those obtained in the non-switched opamp presented 4.6. This is clearly expected because the core of the switched opamp is the topology presented in the previous chapter, so the majority of the characteristics will remain unchanged. The only significant difference is that the switched version of the topology has lower bandwidth and unity-gain frequency. This is due to the need of lowering the dominant pole of the opamp in order to increase the phase margin, which decreased due to the addition of switches in series with the inputs of the common-source-stages, as explained in 5.3.1.

Since the opamp is switched there is a characteristic specific to this type of topology that must be analysed and that is the turn-on time. The turn-on time of a switched opamp is the time it takes the opamp to go from the voltage set at its output when it is *off*, to the common-mode voltage level at the output during regular operation. For the proposed topology it represents the time it takes to go from 20V to 10V. This time must be measured with no signal applied to the inputs of the opamp. Figure 5.8 represents the output voltage of the switched opamp at a switching frequency of 200Hz with a 10pF load capacitance at the output.

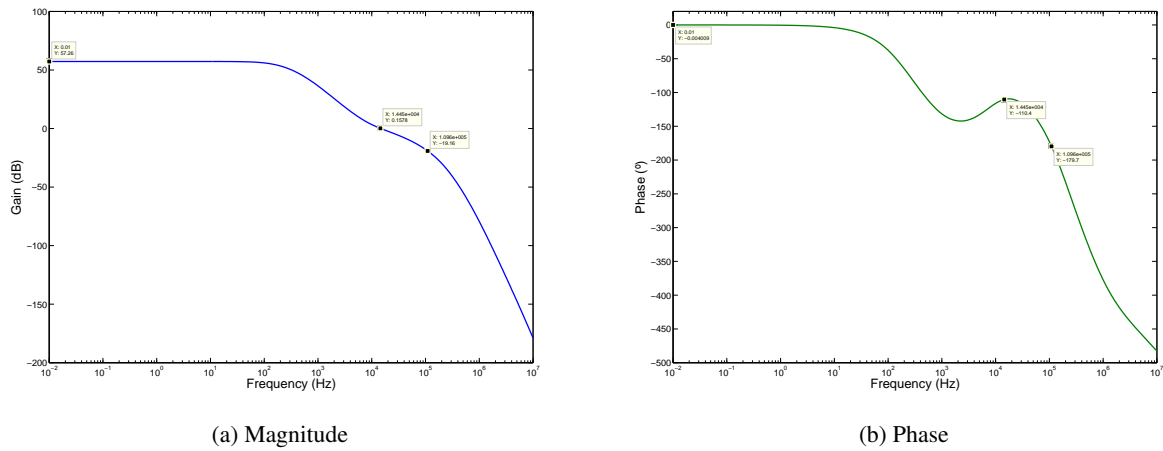


Figure 5.7: Frequency response of the switched opamp in a-GIZO TFT

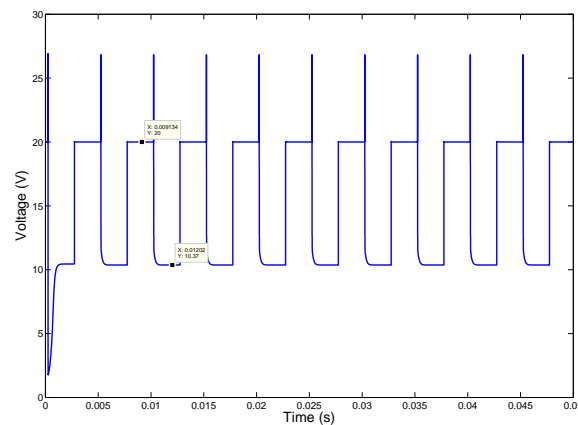


Figure 5.8: Output voltage of the proposed switched opamp with no signal applied to the input at a switching frequency of 200Hz

This graphic not only allows the measurement of the turn-on time but also to take an extra conclusion. The turn on time is measured between 20V and 10.368V because there is a constant offset in the common-mode voltage in the output when the amplifier is on, and this time is $912.65\mu s$. This means that the output of the opamp takes a considerable amount of time to recover from the off mode but this time length cannot be compared to that of switched opamps in CMOS as there are many differences between this topology and the state of the art topologies with complementary devices and besides the technologies themselves are different. There are two main causes for this high turn-on time, the first one is the fact that all of the stages of the opamp are turned-off. The second reason is that the parasitic capacitances for a-GIZO TFTs are in the order of a few pF due to the relatively big dimensions of these transistors. The extra conclusion that can be taken from the verified results is related to the offset present in the common-mode level when the amplifier is

on. This effect is caused by the small gain of the common-mode feedback loop. Still, since the amplifier is fully-differential the offset will be cancelled as it is constant and exactly the same for both outputs. The output of the CMFB circuit is represented in figure 5.9. In this signal it can be seen that there is an offset between the expected level, which is the level to which C_4 is precharged in the *off* period of the opamp, 4.81V, and the value at the output when the amplifier is turned-on, which is 4.697V. This difference is reflected in the constant offset verified in the common-mode level at the output of the opamp when it is turned-on.

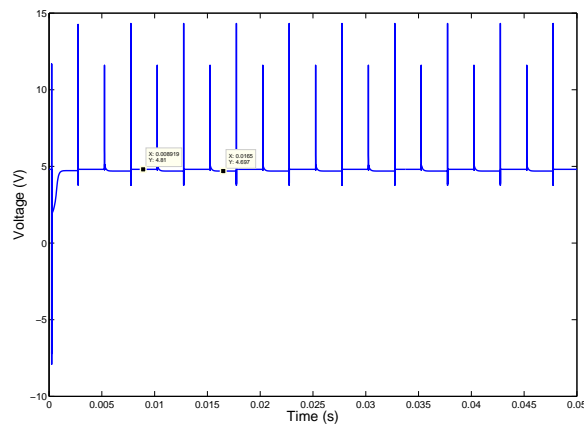


Figure 5.9: Output signal of the CMFB circuit of the switched opamp

Table 5.4 presents the main characteristics of the switched opamp.

Table 5.4: Characteristics of the switched opamp

Gain	57.26 dB
Bandwidth	169.8 Hz
Unity-gain frequency	14.749 kHz
Phase Margin (100pF load)	69.8°
CMRR	90.35dB
PSRR	75.60dB
Supply Voltage	20V
Total Current	161.16 μ A
Power Consumed	3.223mW
Input Common-mode range	3.6->10.5V (6.9V)
Output swing	5V->16.8V (11.8V)
Turn-on time	912.65 μ s

5.5.2 S/H implemented with the switched Opamp

The S/H circuit is to expected have a low maximum operating frequency as the operational amplifier takes 912.65 μ s to reach the expected common-mode voltage at the output. Therefore the

maximum frequency of operation for this circuit will be approximately:

$$\frac{1}{2 \times 912.65 \times 10^{-6}} \approx 547.85\text{Hz} \quad (5.5)$$

This switching frequency corresponds to a maximum operation of about 273 Samples/s. This means that the circuit will only be suited for low frequency applications as the switching frequency itself is low.

To analyse the operation of the sample and hold a differential sinusoidal signal with a frequency of 20Hz and an amplitude of 1V was applied to the inputs of the S/H circuit. To avoid aliasing and have a number of samples for period that would allow the shape of the sine wave to be clearly perceived at the output of the S/H, the circuit was simulated at a switching frequency of 200Hz. Presented in figure 5.10 are the input and output signals for one of the differential paths of the topology. Here the offset at the output is clearly visible as is the shape of the sine wave. Also verified, is that this topology does not function as a normal S/H circuit would, because the output voltage level is not held during the sampling phase, as the amplifier is disconnected and capacitors Ch are reset.

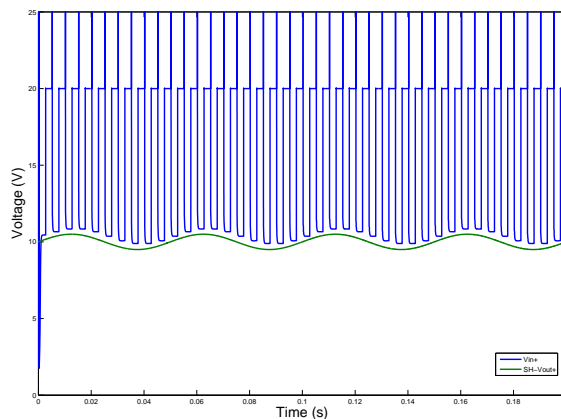


Figure 5.10: Positive phase differential input and output signals of the S/H for a 20Hz sinusoidal signal with an amplitude of 1V, S/H operated at $F_s=200\text{Hz}$

If the transient difference between the output signals is analysed and compared to the signal at the input it is verified that the constant offset is eliminated as illustrated in figure 5.11.

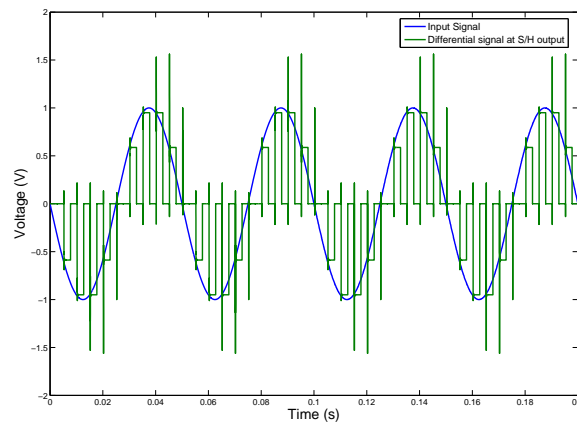


Figure 5.11: Differential signals at input and output of S/H circuit. S/H operated at $F_s=200\text{Hz}$

To analyse the performance of the circuit further the power spectral density of the output signal from 0 to $F_s/2$, presented in figure 5.12, was analysed

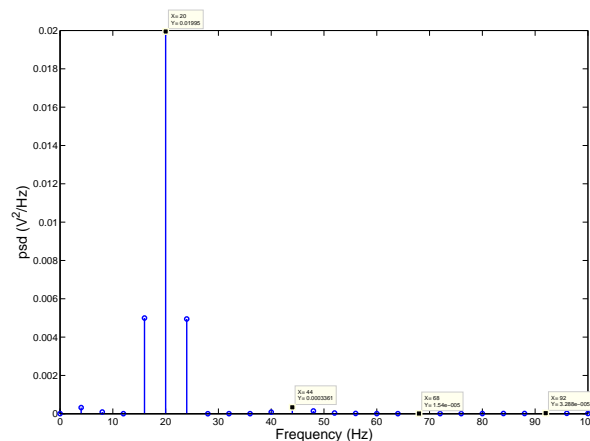


Figure 5.12: Power spectral density of the differential output signal of the S/H circuit. Fundamental frequency 20Hz.

Using the power spectral density spectrum the analysis of Spurious-Free Dynamic Range (SFDR) and the Total Harmonic Distortion (THD) can be made. Both of these analysis characterize the dynamic behaviour of the S/H. SFDR is defined as the ratio between the power of the fundamental frequency and that of the peak spurious spectral content. This measure is taken over the entire Nyquist zone (dc to $f_s/2$). THD on the other hand is a measurement of the harmonic distortion present in a signal and it is defined as the ratio between the power of the harmonics and that of the fundamental frequency. From the plot power spectral density plot presented in figure 5.12 these parameters were measured as:

- SFDR= 35.472dB

- THD= -34.299dB

These values do not include, however, the contributions from charge injection and clock feedthrough, for this reason the results obtained from real circuits are expected to be worse than the ones obtained in simulation.

5.6 Layout

As in the case of the non-switched version of the opamp for the switched opamp stage-by-stage layouts were designed along with the layout of the complete topologies for the switched opamp and for the complete S/H circuit. For these circuits no layouts were designed with interdigitated or multifinger configurations, as the depletion type behaviour of these structures was already known when the layouts for these topologies were designed.

The layout of the complete S/H circuit is presented in 5.13. As in the case of the previous layouts for the non-switched opamp, all the components used for compensation are not included because no accurate information regarding the characterization of the parasitic capacitances of a-GIZO TFT is yet available. Therefore, all nodes where compensation capacitors and resistors need to be connected are linked to external pads to allow the compensation of the topology externally. For this opamp the CMFB circuit has also been designed separately and also without any capacitors, still, these can be added during circuit testing. The layout for the CMFB circuit is presented in figure 5.14.

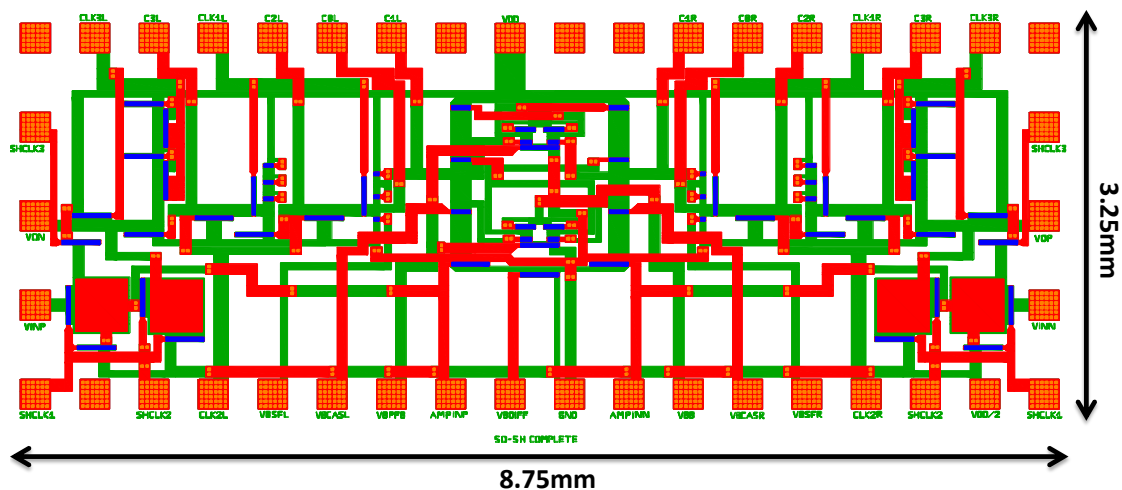


Figure 5.13: Layout of the complete S/H topology

As symmetry is necessary in the design and because only the gate and source-drain layers could be used for signal routing, the circuit requires a considerable number of pads because as clocks used in two different corners of the circuit cannot be routed from one side to the other unless the circuit area would be further increased. In cases such as these it was decided to have

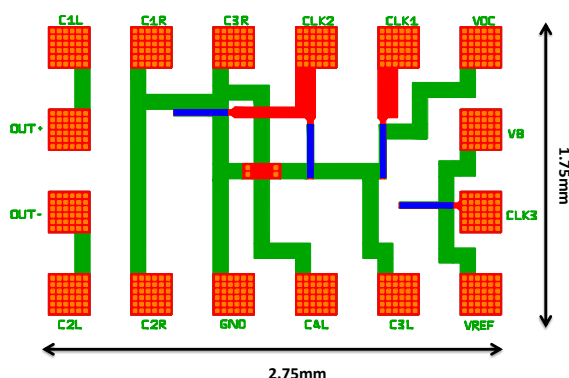


Figure 5.14: Layout of the Common-mode feedback network of the switched opamp (SOCMFB)

two pads for the same signal, one in each corner of the circuit, therefore avoiding long routing connections for the clock. In this way it is also ensured that the circuit is completely symmetric except for the stages that implement positive feedback in the active loads of the input stage. The area of each of the layouts displayed are presented in table 5.5.

Table 5.5: Layout areas

Layout	Area(mm^2)
S/H	28.4375
SOCMFB	4.8125

The layouts of the individual stages of the amplifier are presented in appendix C.

5.7 Summary

In this chapter a novel switched operational amplifier with only n-type enhancement transistors is presented. The proposed topology is adapted for the a-GIZO TFT technology that is fabricated at CENIMAT. This switched opamp uses the novel opamp presented in the previous chapter as its core and the transistors that constitute the switched opamp are conducting in only one of the two clock phases. The application of the switched opamp principle in the a-GIZO TFT technology is aimed at reducing the effects of the shift over time in the transistors threshold voltage due to constant biasing, as circuits with pulsed biasing in this technology have been reported to have reduced V_{th} shift [17].

The proposed switched opamp is used to implement a Sample-and-Hold Circuit based upon a topology proposed in [11]. The complete circuit has the drawback of possessing 7 different clocks and some of them requiring a voltage level above Vdd. The justifications for this high number of

clocks are the various limitations of the technology, namely the lack of complementary device and the impossibility of using a V_{GS} above 7V. This circuit was successfully implemented in simulation without any of the transistors being *on* in both clock phases. Still, simulation results indicate that the circuit has a long turn-on time. This long turn-on time is a cause of high parasitic capacitances of the a-GIZO TFTs and the turning-off of the bias for all the stages of the opamp, when it is switched-off.

The layouts for the proposed circuits are also presented and analysed.

Chapter 6

Conclusions and Future Work

This chapter presents an overview of all of the work developed in the Master Thesis, along with an analysis of the final state for each of the objectives that were set when the work started and the presentation of potential next steps for the work in the area of analog circuits in a-GIZO TFTs.

6.1 Summary of the work developed

The main objective of this work was the development of an operational amplifier topology for a-GIZO TFTs. The topology would have to take into account the various limitations of the technology such as the lack of complementary device, low mobility of carriers in the channel and the shift over time of the threshold voltage of these transistors.

In order to achieve this objective various phases were carried out. The work done and the conclusions arrived at in each phase are presented below.

- The first phase of the work was a study of all the limitations associated with the a-GIZO TFT technology along with its characteristics. Knowing all the limitations that the technology possesses was instrumental in the development of the proposed opamp topologies because these limitations conditioned the design process considerably.
- Secondly a study of previous work on the design of operational amplifiers with only n-type enhancement transistors was done to determine what circuit techniques had already been used in this specific context. This study served as the base for the elaboration of the core of the topologies proposed and from it a novel topology for a high-gain differential stage with only n-type enhancement transistors was developed.
- Then a comparative study was realized between the novel topology developed and other high-gain topologies for technologies with only a single type of transistor. In this study not only was the behaviour of the proposed topology extensively analysed but it was also concluded that this topology was going to be used as the input stage of the operational amplifier. This choice was made because the novel topology allows the highest voltage gain between all of the topologies with only a single type of transistor that can also amplify dc

signals. The ability to amplify dc signals is important because it makes the opamp suitable for a wider set of applications. Also, with this topology a significant gain can be achieved without using extremely high W/L for the transistors and without using transistors for the drive that are much wider than those used as loads in gain stages.

- After this the rest of the stages of the amplifier were designed in order to further increase the overall open-loop gain and be able to use common-mode feedback to reduce the effects of gate bias stress by adapting the biasing voltages for the circuit as the threshold voltage would increase. Simulations results indicate a gain of 57.26dB which is significant in a technology such as this, moreover without the use of bootstrapping implemented through a high-pass filter.
- After the main topology was finished the frequency compensation of the circuit was studied, as it initially presented a negative phase margin. Several compensation schemes were experimented but ultimately two compensations schemes were used in order to compensate the topology. Still, because of the atypical structure employed in the amplifier due to the limitations of having only one type of transistor, the dominant-pole of the system is a complex pole pair that is originated by a source-follower stage. This means that even with the circuit having a stable phase margin above 60° there is some overshoot in the response of the amplifier to a voltage step.
- Then the developed opamp topology was adapted to work as a switched operational amplifier which is expected to reduce the shift in the threshold voltage of the TFTs used. The main objective here was to create an operational amplifier that was going to be disconnect during one clock phase and in which no transistor would be biased constantly, but instead biased by pulses. This adaptation also required the alteration of the common-mode feedback circuit used in the opamp, and for this circuit an adaptation of a topology presented in [10] was used. The final topology for the switched opamp was successfully implemented in simulation with the objective of not having any transistor constantly biased completed successfully. The topology has however a significant level of complexity especially because of all the limitations that are involved with the design of circuits in a technology such as a-GIZO. Also, if complete system on-chip is to be implemented the use of a charge-pump will be necessary because a clock with a voltage level higher than V_{dd} is required for the circuit to operate correctly. This topology constitutes the first proposal of the use of the switched opamp to reduce gate bias stress in TFTs and it is also the first switched opamp implemented with only n-type enhancement TFTs.
- The proposed switched opamp was then used to implement a Sample-and-Hold circuit. The implemented circuit is adaptation of a circuit proposed in [11] as the characteristics of the a-GIZO TFT technology used had to be taken into account along with the fact that the common-mode voltage levels for the proposed the operational amplifier are different from those of the original circuit. Again the circuit was successfully implemented in simulation

but it was found to have a low maximum switching frequency which is determined by the switched operational amplifier. The causes of the low switching frequency are the need of switching *off* all of the stages in the amplifier when the opamp is not active during the sampling phase and the magnitude of the intrinsic parasitic capacitances of the a-GIZO TFTs.

- Finally both complete and stage-by-stage layouts were developed for both of the proposed amplifiers (switched version and regular version). Along with these layouts, additional layouts of high-gain differential stages with other techniques of increasing the load impedance were also designed. In this way, the novel topology for a single-stage high-gain differential amplifier with only n-type enhancement transistors presented in this work can be compared experimentally to other topologies that achieve high load impedance with a single type of transistor, such as topologies employing capacitive bootstrapping.

6.2 Concluded Objectives

The main objectives were completed, as not one but two novel operational amplifiers topologies were developed. This topologies present interesting results in simulation and are expected to have good performance in terms of gain in a technology where high-voltage gain is difficult to achieve especially without using depletion type transistors. A new approach to reduced the effects of the shift in the TFTs V_{th} is also proposed.

The layouts for all of the developed circuits were also developed and in a way that allows the testing of the developed circuits in a very flexible way.

However, until the time of this writing no measurements were done in fabricated circuits because these have not yet been fabricated due to factors that are beyond the control of the author.

6.3 Future work

In terms of the topology developed there is still the matter of realizing the measures in the circuits after fabrication. The data from the first fabricated chips should prove instrumental in the improvement and optimization of the developed topologies, especially if the transistors display a capacity to work with higher values for V_{GS} , as less transistors could be used in both opamps.

The frequency compensation scheme of the presented opamps should be restudied in order to try to find if there is a way of compensating the topology without complex poles associated with the source-follower stage, while still maintaining a bandwidth similar to the one obtained.

Also, if accurate ways to simulate the parasitic capacitances of the a-GIZO TFT are found, the layouts for the circuits could be redone without keeping pads to connect compensation capacitors externally. In this way the complete operational amplifier could be implemented on-chip.

The simulation model used must also be altered in order to solve the convergence issues that occur during the simulation of circuits where the a-GIZO TFT is used as a switch.

After these problems are solved and there is more data that can possibly allow a more detailed simulation of the behaviour of the a-GIZO TFTs used, the complete S/H circuit could be fully implemented on-chip along with all the auxiliary circuits required to generate the different voltage levels for its clocks. Finally, as an ultimate objective a complete ADC could be eventually designed and implemented with a-GIZO TFTs using the proposed topologies.

Appendix A

Expressions and simulation setups

A.1 Deduction of the small-signal expressions of the novel topology for high-gain with only n-type enhancement transistors

A.1.1 Deduction of the voltage gain equation

Recalling the equivalent small-signal circuit for the configuration in figure 4.4b. To start determining V_{out}/V_{in} the first step is to determine the factor a . This factor is determined by applying Kirchoff's Law in the node of aV_o , which will give:

$$gm_4.(Af1 - a).V_{out} - a.gds_4.V_{out} = gm_3.(Af - 1).V_{out} + (a - 1).gds_3.V_{out} \quad (A.1a)$$

$$\Leftrightarrow a.(gm_4 + gds_3 + gds_4) = gm_4.Af1 - gm_3.Af + gm_3 + gds_3 \quad (A.1b)$$

$$\Leftrightarrow a = \frac{gm_4.Af1 - gm_3.Af + gm_3 + gds_3}{gm_4 + gds_3 + gds_4} \quad (A.1c)$$

After determining a the next step is to determine $a1$ as a factor of V_{in} and V_{out} so again the nodal equation is done but for node $a1.V_{in}$.

$$gm_1.V_{in} + a1.gds_1.V_{in} = -gm_2.a1.V_{in} + (V_{out} - a1.V_{in}).gds_2 \quad (A.2a)$$

$$\Leftrightarrow a1.(gds_1.V_{in} + gm_2.V_{in} + gds_2.V_{in}) = -gm_1.V_{in} + gds_2.V_{out} \quad (A.2b)$$

$$\Leftrightarrow a1 = \frac{-gm_1.V_{in} + gds_2.V_{out}}{(gm_2 + gds_1 + gds_2).V_{in}} \quad (A.2c)$$

Using the previous expression for $a1$ and determining the nodal equation for the output node, V_{out}/V_{in} can be determined as shown below.

$$-gm_2.a1.V_{in} + gds_2.(V_{out} - a1.V_{in}) = gm_3.(Af - 1).V_{out} + gds_3.(a - 1).V_{out} \quad (A.3a)$$

Substituting a1 by its equivalent expression

$$\begin{aligned} &\Leftrightarrow -gm_2 \cdot \frac{-gm_1 \cdot V_{in} + gds_2 \cdot V_{out}}{(gm_2 + gds_1 + gds_2) \cdot V_{in}} \cdot V_{in} + gds_2 \cdot (V_{out} - \frac{-gm_1 \cdot V_{in} + gds_2 \cdot V_{out}}{(gm_2 + gds_1 + gds_2) \cdot V_{in}} \cdot V_{in}) = \\ &= gm_3 \cdot (Af - 1) \cdot V_{out} + gds_3 \cdot (a - 1) \cdot V_{out} \end{aligned} \quad (A.3b)$$

Then reducing everything to the same denominator we get

$$\begin{aligned} &\Leftrightarrow -gm_2 \cdot (-gm_1 \cdot V_{in} + gds_2 \cdot V_{out}) \cdot V_{in} + gds_2 \cdot ((gm_2 + gds_1 + gds_2) \cdot V_{in} \cdot V_{out} - (-gm_1 \cdot V_{in} + gds_2 \cdot V_{out}) \cdot V_{in}) = \\ &= ((gm_2 + gds_1 + gds_2) \cdot V_{in}) \cdot (gm_3 \cdot (Af - 1) \cdot V_{out} + gds_3 \cdot (a - 1) \cdot V_{out}) \end{aligned} \quad (A.3c)$$

$$\begin{aligned} &\Leftrightarrow V_{in} \cdot (gm_1 \cdot gm_2 + gm_1 \cdot gds_2) + V_{out} \cdot (-gm_2 \cdot gds_2 + gds_2 \cdot (gds_1 + gds_2) + gm_2 \cdot gds_2 - gds_2^2) = \\ &= V_{out} \cdot (gm_3 \cdot (Af - 1) \cdot ((gds_1 + gds_2) + gm_2) + (a - 1) \cdot gds_3 \cdot ((gds_1 + gds_2) + gm_2)) \end{aligned} \quad (A.3d)$$

Finally we arrive at the equation for V_{out}/V_{in}

$$\frac{V_{out}}{V_{in}} = \frac{gm_1 \cdot gm_2 + gm_1 \cdot gds_2}{(Af - 1) \cdot gm_3 \cdot (gds_1 + gds_2 + gm_2) + (a - 1) \cdot gds_3 \cdot (gds_1 + gds_2 + gm_2) - gds_1 \cdot gds_2} \quad (A.3e)$$

A.1.2 Deduction of the load impedance equation

To determine the equation for the load impedance the simplified scheme displayed in figure A.1 was used.

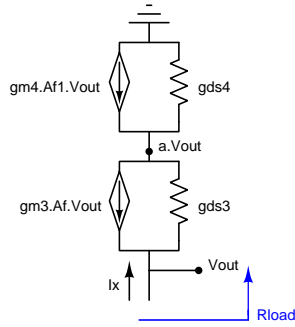


Figure A.1: Small-signal equivalent of the load for the novel high-gain topology with n-type enhancement transistors

Considering this figure, R_{load} can be determined as $-V_{out}/I_x$, therefore I_x must be determined. This is done by determining the nodal equation for the node of V_{out} .

$$I_x = -V_{out} \cdot ((a-1) \cdot g_{ds3} + g_{m3} \cdot (Af-1)) \quad (A.4)$$

The the load impedance is determined as

$$R_{load} = \frac{V_{out}}{-V_{out} \cdot ((a-1) \cdot g_{ds3} + g_{m3} \cdot (Af-1))} \quad (A.5a)$$

Then substituting g_{ds3} by $1/r_{o3}$ we get

$$\Leftrightarrow R_{load} = \frac{-1}{\frac{a-1}{r_{o3}} + g_{m3} \cdot (Af-1)} \quad (A.5b)$$

Finally we arrive at the equation of the load impedance

$$R_{load} = \frac{r_{o3}}{1-a-g_{m3} \cdot (Af-1) \cdot r_{o3}}, \quad (A.5c)$$

where the constant a is given by A.1

A.1.3 Load resistance with $|Af|=|Af1|=1$

An important consideration for the proposed topology is the equivalent small-signal impedance of the load in the ideal case that $|Af|=|Af1|=1$.

In this case if differential signals are considered the feedback implemented will be positive and $Af=Af1=1$. Then using the formulas for R_{load} and the factor a presented before in this chapter and replacing these values:

$$R_{load} = \frac{r_{o3}}{1-a-g_{m3} \cdot (1-1) \cdot r_{o3}} \quad (A.6a)$$

Now Substituting a

$$\Leftrightarrow R_{load} = \frac{r_{o3}}{1 - \frac{g_{m4} - g_{m3} + g_{m3} + g_{ds3}}{g_{m4} + g_{ds3} + g_{ds4}}} \quad (A.6b)$$

$$\Leftrightarrow R_{load} = \frac{r_{o3}(g_{m4} + g_{ds3} + g_{ds4})}{g_{m4} + g_{ds3} + g_{ds4} - g_{m4} - g_{ds3}} \quad (A.6c)$$

Representing g_{ds3} as $1/r_{o3}$ and g_{ds4} as $1/r_{o4}$

$$R_{load} = g_{m4} \cdot r_{o3} \cdot r_{o4} + r_{o3} + r_{o4} \quad (A.6d)$$

On the other hand for common-mode signals Af and Af1 will be equal to -1 and the load resistance can be found as:

$$R_{load} = \frac{r_{o3}}{1 - a - gm_3 \cdot ((-1) - 1) \cdot r_{o3}} \quad (A.7a)$$

Now Substituting a

$$\Leftrightarrow R_{load} = \frac{r_{o3}}{1 - \frac{-gm_4 + 2 \cdot gm_3 + gds_3}{gm_4 + gds_3 + gds_4} + 2 \cdot gm_3 \cdot r_{o3}} \quad (A.7b)$$

$$\Leftrightarrow R_{load} = \frac{r_{o3} \cdot (gm_4 + gds_3 + gds_4)}{gm_4 + gds_3 + gds_4 + gm_4 - 2 \cdot gm_3 - gds_3 + 2 \cdot gm_3 \cdot r_{o3} (gm_4 + gds_3 + gds_4)} \quad (A.7c)$$

Multiplying both the numerator and denominator by r_{o4} and applying some simplifications

$$\Leftrightarrow R_{load} = \frac{gm_4 \cdot r_{o3} \cdot r_{o4} + r_{o3} + r_{o4}}{2 \cdot gm_4 \cdot r_{o4} + 1 - 2 \cdot gm_3 \cdot r_{o4} + 2 \cdot gm_3 \cdot r_{o3} \cdot r_{o4} (gm_4 + gds_3 + gds_4)} \quad (A.7d)$$

Finally putting $r_{o3}/2$ in evidence we arrive at:

$$\Leftrightarrow R_{load} = \frac{r_{o3}}{2} \frac{gm_4 \cdot r_{o3} \cdot r_{o4} + r_{o3} + r_{o4}}{gm_4 \cdot r_{o3} \cdot r_{o4} + r_{o3}/2 - gm_3 \cdot r_{o3} \cdot r_{o4} + gm_3 \cdot r_{o3}^2 \cdot r_{o4} (gm_4 + gds_3 + gds_4)} \quad (A.7e)$$

Which simplifies to

$$R_{load} = \frac{r_{o3}}{2} \frac{1}{1 - \left(\frac{r_{o4} + r_{o3}/2 - gm_3 \cdot r_{o3} (gm_4 \cdot r_{o3} \cdot r_{o4} + r_{o3})}{gm_4 \cdot r_{o3} \cdot r_{o4} + r_{o3} + r_{o4}} \right)} \quad (A.7f)$$

This last equation can be simplified further considering that $gm_3 \cdot gm_4 \cdot r_{o3}^2 \cdot r_{o4} \gg (-r_{o4} + r_{o3}(-1/2 + gm_3 \cdot r_{o3}^2))$ and $gm_4 \cdot r_{o3} \cdot r_{o4} \gg (r_{o4} + r_{o3})$, in which case:

$$R_{load} \simeq \frac{r_{o3}}{2} \frac{1}{1 - \left(\frac{-gm_3 \cdot gm_4 \cdot r_{o3}^2 \cdot r_{o4}}{gm_4 \cdot r_{o3} \cdot r_{o4}} \right)} \quad (A.8a)$$

$$\Leftrightarrow R_{load} \simeq \frac{r_{o3}}{2} \frac{1}{1 + gm_3 \cdot r_{o3}} \quad (A.8b)$$

Finally, considering $gm_3 \cdot r_{o3} \gg 1$:

$$R_{load} \simeq \frac{1}{2 \cdot gm_3} \quad (A.8c)$$

A.2 Bias and aspect ratios for the simulations of the high-gain topologies with only n-type enhancement transistors

A.2.1 Aspect ratios and biasing conditions used in the simulations of the novel topology

Table A.1: Aspect ratios and biasing conditions used in the simulations of the novel topology

Technology	Width(μm)	Length(μm)	$V_{GS}(V)$	$V_{DS}(V)$
NMOS 0.35 μm	160	20	1.0	1.1
a-GIZO TFT	160	20	5.0	5.0

A.2.2 Aspect ratios and biasing conditions used in the simulations of high-gain single-stage amplifiers with only n-type enhancement transistors

The schematics of the topologies are presented in figures 4.1 and 4.2.

Regarding the topologies with differential feedback the bias voltages of the differential pair for the top load are made different from Vdd in order to guarantee that the transistors in the load of the main amplifier stage are biased with the same voltages as in the topologies using capacitive bootstrapping.

All of the capacitances designated C_b had the value of 50pF.

A.2.2.1 NMOS implementations

Table A.2: Aspect ratios for the differential amplifier with single ac bootstrapped load in NMOS (figure 4.1a)

Transistor(s)	Aspect ratio ($\mu m/\mu m$)
M1,M2,M3,M4	160/20
M5,M6	5/5
M7	320/20

Table A.3: Bias voltages for the differential amplifier with single ac bootstrapped load in NMOS (figure 4.1a)

Designation	Value(V)
Vdd	3.3
Vb1	1.0

Table A.4: Aspect ratios for the differential amplifier with cascade ac bootstrapped load in NMOS (figure 4.1b)

Transistor(s)	Aspect ratio ($\mu m/\mu m$)
M1,M2,M3,M4	160/20
M7,M8,M9,M10	5/5
M11	320/20

Table A.5: Bias voltages for the differential amplifier with cascade ac bootstrapped load in NMOS (figure 4.1b)

Designation	Value(V)
Vdd	4.4
Vbias	3.2
Vb1	1.0

Table A.6: Aspect ratios for the differential amplifier with single differential feedback in NMOS (figure 4.2a)

Transistor(s)	Aspect ratio ($\mu m/\mu m$)
M1,M2,M3,M4,M7,M8	160/20
M5,M6	159/20
M9,M10	320/20

Table A.7: Bias voltages for the differential amplifier with single differential feedback in NMOS (figure 4.2a)

Designation	Value(V)
Vdd	3.3
Vb1	1.0
Vb2	1.0
Vb3	4.2

Table A.8: Aspect ratios for the differential amplifier with cascade differential feedback in NMOS (figure 4.2b)

Transistor(s)	Aspect ratio ($\mu m/\mu m$)
M1,M2,M3,M4,M5,M6,M9,M10,M13,M14	160/20
M7,M8,M11,M12	159/20
M15,M16,M17	320/20

Table A.9: Bias voltages for the differential amplifier with cascade differential feedback in NMOS (figure 4.2b)

Designation	Value(V)
Vdd	4.4
Vb1	1.0
Vb2	1.0
Vb3	4.2
Vb4	5.3

A.2.2.2 a-GIZO TFT implementations

Table A.10: Aspect ratios for the differential amplifier with single ac bootstrapped load in a-GIZO TFT (figure 4.1a)

Transistor(s)	Aspect ratio ($\mu m/\mu m$)
M1,M2,M3,M4	160/20
M5,M6	40/20
M7	320/20

Table A.11: Bias voltages for the differential amplifier with single ac bootstrapped load in a-GIZO TFT (figure 4.1a)

Designation	Value(V)
Vdd	15
Vb1	5

Table A.12: Aspect ratios for the differential amplifier with cascade ac bootstrapped load in a-GIZO TFT (figure 4.1b)

Transistor(s)	Aspect ratio ($\mu m/\mu m$)
M1,M2,M3,M4	160/20
M7,M8,M9,M10	40/20
M11	320/20

Table A.13: Bias voltages for the differential amplifier with cascade ac bootstrapped load in a-GIZO TFT (figure 4.1b)

Designation	Value(V)
Vdd	20
Vbias	15
Vb1	5

Table A.14: Aspect ratios for the differential amplifier with single differential feedback in a-GIZO TFT (figure 4.2a)

Transistor(s)	Aspect ratio ($\mu m/\mu m$)
M1,M2,M3,M4,M7,M8	160/20
M5,M6	120/20
M9,M10	320/20

Table A.15: Bias voltages for the differential amplifier with single differential feedback in a-GIZO TFT (figure 4.2a)

Designation	Value(V)
Vdd	15
Vb1	5
Vb2	5
Vb3	20

Table A.16: Aspect ratios for the differential amplifier with cascade differential feedback in a-GIZO TFT (figure 4.2b)

Transistor(s)	Aspect ratio ($\mu m/\mu m$)
M1,M2,M3,M4,M5,M6,M9,M10,M13,M14	160/20
M7,M8,M11,M12	120/20
M15,M16,M17	320/20

Table A.17: Bias voltages for the differential amplifier with cascade differential feedback in a-GIZO TFT (figure 4.2b)

Designation	Value(V)
Vdd	20
Vb1	5
Vb2	5
Vb3	20
Vb4	25

A.3 Frequency Compensation analysis

The expressions shown in this chapter are relative to the schematic of the topology for the novel opamp in a-GIZO TFTs, presented in figure 4.21.

A.3.1 Estimation of the time constants associated with each node

The estimation of the time constants is obtained by determining the equivalent resistance for each node as well as the total capacitance connected between that node and ground. All of the time

constants presented below are determined before the use of compensation.

Node A:

$$R_A = 2/gm_3 \quad (\text{A.9a})$$

$$C_{eqA} = C_{GS3} + (1 - Av_1^{-1}).C_{GD1} \quad (\text{A.9b})$$

The value of R_A is represented as $2/gm_3$ instead of $1/gm_3$, because the input impedance value of a common-gate stage will also depend on the resistance at the drain and will be given by [27, p. 80]

$$R_{in} = \frac{R_D}{r_o} + \frac{1}{gm}, \quad (\text{A.10})$$

where R_D is the resistance at the drain of the common-gate stage. In this expressions the terms related to body effect have not been considered.

This equation reveals that if the drain resistance is high when compared to the intrinsic resistance of the transistor in the common-gate the input resistance will be higher than $1/gm$. In the particular case that $R_D = r_o$, $R_{in} = 2/gm$. In this case the load resistance, which is the equivalent resistance of the novel topology was found to be only slightly superior to r_o and therefore R_A which is the input resistance of $M_{3,4}$ was approximated to $2/gm_3$

Node B:

$$R_B = ((gm_1.r_{o1}.r_{o3} + r_{o1} + r_{o3}) || R_{load}) \quad (\text{A.11a})$$

$$C_{eqB} = C_{GD3} + C_{GD17} + C_{GS13} + C_{GS9} + (1 - Af).C_{GD9} + (1 - Af1).C_{GD13} \quad (\text{A.11b})$$

R_{load} is calculated from the expressions presented in 4.24.

Node C:

$$R_C = r_{o38} + \left(\frac{1}{gm_{19}} || r_{o19}\right) \quad (\text{A.12a})$$

$$C_{eqC} = C_{GD38} + (1 - Av_2).C_{GD21} + C_{GS21} \quad (\text{A.12b})$$

Node D:

$$R_D = r_{o21} \parallel \left(\left(\frac{1}{g_{m23}} \parallel r_{o23} \right) + \left(\frac{1}{g_{m24}} \parallel r_{o24} \right) + \left(\frac{1}{g_{m25}} \parallel r_{o25} \right) \right) \quad (\text{A.13a})$$

$$C_{eqD} = C_{GS29} + (1 - Av_2^{-1}) \cdot C_{GD21} + (1 - Av_3) \cdot C_{GD29} \quad (\text{A.13b})$$

Output node (Node E):

$$R_E = r_{o29} \parallel \left(\left(\frac{1}{g_{m31}} \parallel r_{o31} \right) + \left(\frac{1}{g_{m32}} \parallel r_{o32} \right) \right) \quad (\text{A.14a})$$

$$C_{eqE} = C_{load} + (1 - Av_2^{-1}) \cdot C_{GD29} \quad (\text{A.14b})$$

In the equations presented above $Av_1 = 3.451$, $Av_2 = 10.1625$, $Av_3 = 2.1627$, $Af = 0.9727$, $Af1 = 0.9784$ and $a = 0.962$. Av_1 is the voltage gain from the input to node A, Av_2 is the voltage gain of stage *Common-Source 1*, Av_3 the gain of the output stage and Af the voltage gain of the differential amplifier that implements positive feedback in the active loads of the input stage.

Appendix B

Overview of Single Stage Amplifiers

In the following subsections the common topologies of amplifying stages are presented and their main characteristics analysed. Only stages comprised of n-type enhancement transistors are considered because there are no complementary transistors available for use in the a-GIZO TFT technology, as previously referred in section 2.5.2.

B.1 Common-Source Stage

One of the common single stage amplifier topologies is the common source stage, presented in figure B.1.

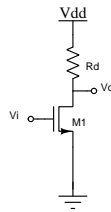


Figure B.1: Common-Source Stage

From the analysis of this configuration through the simplified small-signal model of the transistor it can be shown that the small-signal gain of the configuration for a generic load resistance R_D is given by

$$A_v = -g_m(R_D || r_o) \quad (\text{B.1})$$

When considering the analysis of the input and output impedances for this topology it can be quickly inferred from the small-signal model of the transistor that the output impedance of this configuration is

$$R_{out} = R_D || r_o \quad (\text{B.2})$$

And the impedance associated to the input is significantly high considering that the gate of the device is insulated.

Due to the characteristics presented above it is easily seen that this topology is ideally suited to achieve high input impedances and it can be used to achieve signal inversion due to the negative gain it presents. In terms of its application for high-gain stages, it is easily observed that in this configuration the overall gain that can be achieved is constrained by the value of the transistors output resistance, r_o which can assume values of some Mega Ohms in the a-GIZO TFT technology, by the load resistance present at the drain, R_D and by the transconductance of the drive transistor. Therefore, to achieve a high small-signal gain both resistances need to be high and of a similar magnitude (both resistors are in parallel), which means that if one of the resistors is significantly higher than the other, the value of the output impedance will be closer to the resistor with the lowest value between the two, conditioning the small-signal gain. This means that in order to have high-gain values with a-GIZO TFTs it is necessary to try to achieve load resistances of a similar, or even superior magnitude to that of the internal small-signal output resistance of the transistors used in the drive.

B.2 Common-Source Stage with Source Degeneration

A variation of the common-source stage is achieved introducing a resistance, R_S , at the source of the transistor, as shown in figure B.2.

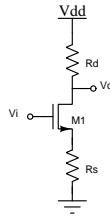


Figure B.2: Common-Source Stage with Source Degeneration

After analysing this topology using the small-signal model of the a-GIZO TFT the small-signal gain is determined after some mathematical manipulation as

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} \quad (\text{B.3})$$

If $g_m R_S \gg 1$ the gain can be approximated as

$$A_v \simeq -\frac{R_D}{R_S} \quad (\text{B.4})$$

This topology presents similar characteristics to the regular common-source stage for the input impedance.

The objective of using this configuration is to have a small-signal gain that is not as dependent of the intrinsic characteristics of the transistor as the gain of the regular common-source stage, avoiding non-linearities associated with the transconductance. As shown by equation B.4, if $g_m R_S$ is high enough, the magnitude of the small-signal gain is approximately determined by the ratio of drain and source resistors, therefore less sensitive to variations of g_m .

B.3 Source Follower

Another common amplifier stage is the source follower, also designated as common-drain stage, presented in B.3.

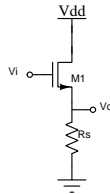


Figure B.3: Source Follower Stage

The small-signal gain of this topology is

$$A_v = \frac{g_m(R_S || r_o)}{1 + g_m(R_S || r_o)} \quad (\text{B.5})$$

If $g_m R_S \gg 1$ the small-signal gain is approximately equal to unity.

The input impedance of this stage is very high as with the common-source stages presented previously. The output impedance is given by

$$R_{out} = \frac{1}{g_m} || R_S || r_o \quad (\text{B.6})$$

Since the resistance $\frac{1}{g_m}$ is typically lower than R_S and r_o , this stage typically presents a low output impedance when compared with the output impedance of a regular common-source stage.

Due to its characteristics, this stage is normally used as a buffer to connect high voltage gain stages that depend on the value of the load impedance, such as the common-source stage, to low impedance loads. In this situations the almost unitary gain of the source follower allows for a very reduced loss of gain relatively to the previous stage and its very high-load impedance assures that the load impedance of the previous stage remains almost unaltered.

Nonetheless a factor that must be considered when designing an operational amplifier where one or more source follower stages are employed is that this stage can have a significant impact in the overall frequency response.

B.4 Common-Gate Stage

Another stage typically employed in signal amplification electronics is the Common-Gate stage, figure B.4. This topology has one main difference regarding the others previously presented, which is related to the terminal of transistor where the input signal is applied. Recall that in both the common-source and the source follower stages the input was applied to the gate of the transistor, however in this stage the input is applied to the source terminal.

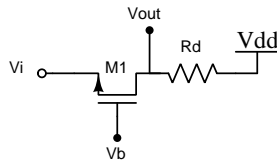


Figure B.4: Common-Gate Stage

The advantage of applying the input to the source terminal is related to the low-input impedance that the transistor presents seen into the source terminal and to the fact that in this configuration the input signal can be a current.

Analysing the small-signal model of the transistor, the input impedance is determined as

$$R_{in} = \frac{1}{g_m} \quad (\text{B.7})$$

This impedance is of course much smaller than the one presented by the gate terminal which is insulated and therefore presents a very high impedance. Also from the analysis of the small-signal model of the transistor, the gain of the stage is found to be

$$A_v = g_m(R_D || r_o) \quad (\text{B.8})$$

In terms of frequency behaviour it is important to note that unlike the common-source stage in this configuration there is no Miller multiplication of C_{GD} , which is an important advantage of this configuration and constitutes one of the main reasons behind the usage of the cascode topology.

B.5 Cascode stage

The Cascode Stage, figure B.5, uses a common-gate transistor as the load of the input transistor which is connected as a common-source. In this topology M1 converts the voltage signal at its gate into a current signal which is applied to the source of M2.

A set back of this topology is the voltage V_b that is necessary to bias M2 in saturation and a reduced output voltage swing when compared with the common-source stage. The minimum output level is given in this topology by the minimum level at which both M1 and M2 are in saturation. This level is equal to the sum of the overdrive voltages of both transistors. In comparison in a

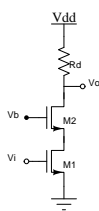


Figure B.5: Cascode Stage

common-source stage the minimum output level is only determined by the overdrive voltage of the single drive transistor.

From the analysis of the small-signal model of the transistor the gain of the stage is found to be

$$A_v = -\frac{g_{m1}}{g_{m2}}g_{m2}(R_D||r_o) \quad (\text{B.9})$$

The of gain of the cascode stage can be further simplified to

$$A_v \simeq -g_{m1}(R_D||r_o) \quad (\text{B.10})$$

Therefore, small-signal gain of the cascode stage is equal to that of a common-source-stage, presented in equation B.1.

Until now it seems that this topology presents no advantages relatively to the common-source topology; the gain is the same and it even has a lower output swing. But there are advantages related to the use of this topology, one of which is the very high output impedance of this stage, which is found to be

$$R_{out} = (1 + g_{m2}r_{o2})r_{o1} + r_{o2} \quad (\text{B.11})$$

Knowing that the intrinsic gain of an amplifying stage, which is the voltage gain an amplifying would present in the presence of an infinite load resistance, is given by

$$A_{int} = G_m R_{out} \quad (\text{B.12})$$

From B.11 and B.12 one can conclude that for this topology the maximum voltage gain is theoretically approximate to the square of the intrinsic gain of a single transistor, because R_{out} is proportional to $r_{o1}r_{o2}$. Nevertheless, the most important advantage is in terms of bandwidth since it reduces the Miller effect on the input transistor.

B.6 Differential Pair

In terms of the design of operational amplifiers there is one characteristic that must be present in every topology which is the use of a differential input. For this reason the differential becomes

possibly the most important configuration in an opamp because in some fashion it will always be used in the overall topology.

A basic version of the implementation of a differential pair is presented in figure B.6. In this figure the input transistors are M1 and M2 and the third transistor, M3, is used to provide bias for the configuration. In this topology it is important to analyse both the differential gain and the common mode gain in order to determine the common-mode rejection ratio, CMRR, which is an important parameter in the characterization of the immunity to noise of differential pairs.

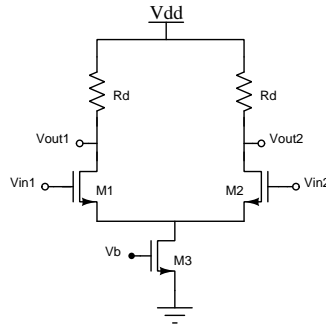


Figure B.6: Differential Pair with resistive load

The common mode rejection ratio is given by

$$CMRR = 20 \log_{10} \left(\frac{|A_d|}{|A_{CM}|} \right), \quad (\text{B.13})$$

where A_d is the differential gain and A_{CM} is the common-mode gain. To calculate both the differential gain and the common-mode gain it is necessary to define V_{in1} and V_{in2} .

$$V_{in1} = \frac{V_{in1} - V_{in2}}{2} + \frac{V_{in1} + V_{in2}}{2} \quad (\text{B.14})$$

$$V_{in2} = \frac{V_{in2} - V_{in1}}{2} + \frac{V_{in1} + V_{in2}}{2} \quad (\text{B.15})$$

In the above definitions, the first term refers to the differential component and the second term, which is common to both inputs, is the common-mode component.

To determine the differential gain consider that the input of M1 is $\frac{V_{in1} - V_{in2}}{2}$ and the input of M2 is $\frac{V_{in1} - V_{in2}}{2}$, leading to a virtual ground between the sources of both M1 and M2. In this case V_{out1} and V_{out2} are given by

$$V_{out1} = -g_m(R_D || r_{o1}) \frac{V_{in1} - V_{in2}}{2} \quad (\text{B.16})$$

$$V_{out2} = -g_m(R_D || r_{o2}) \frac{V_{in2} - V_{in1}}{2} \quad (\text{B.17})$$

Considering that both transistors are exactly matched, the differential gain can be determined as

$$A_d = V_{out1} - V_{out2} = -g_m(R_D || r_{o1})(V_{in1} - V_{in2}) \quad (\text{B.18})$$

To find the common-mode gain, we continue to assume that the circuit is symmetric and that M3 possesses a finite output resistance, r_{o3} . Because the common-mode component is symmetric in both inputs the configuration can be represented as in figure B.7.

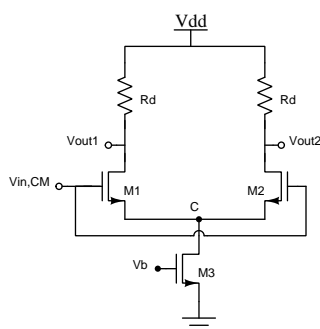


Figure B.7: Differential Pair with common-mode input

From this simplified configuration we determine that a change in the common-mode input, $V_{in,CM}$, induces a change in the voltage at node C, which in turn leads to an increase of the drain currents of M1 and M2, leading to lower voltage levels at the outputs V_{out1} and V_{out2} . Assuming that the circuit is completely symmetric, variations in both outputs will always be symmetric, as will the voltage level, so it's possible to short both outputs simplifying the analysis further, as represented in B.8.

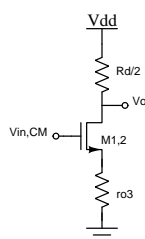


Figure B.8: Equivalent Circuit of a differential pair with common-mode input

In this circuit M1 and M2 are substituted by a virtual transistor with twice the width $W_{M1,2} = 2W_{M1} = 2W_{M2}$. The circuit is now reduced to a common-source stage with source degeneration, previously introduced in B.2, and the common mode gain is given by

$$V_{out2} = -\frac{\frac{R_d}{2}}{\frac{1}{2g_m} + r_{o3}} \quad (\text{B.19})$$

This analysis of the common-mode response justifies the importance of having a large CMRR, because variations of the common-mode level in the input are manifested at the output of the differential pair as variations of the outputs common-mode level and more importantly, these variations in the input are converted into differential components at the outputs. The later effect is even more severe in real circuits where there will always be a mismatches in the differential pair.

Appendix C

Layout in a-GIZO TFT

The layout in a-GIZO TFT using the technology design kit that is being developed at FEUP is different quite different when compared to the done for CMOS technologies. In this chapter an overview of how to produce common blocks such as transistors, pads and vias is shown along with the layouts for individual stages of the opamps designed.

Information regarding each layer used in the layout is presented in section 4.7.1 of chapter 4.

C.1 Basic design rules

The basic design rules for the a-GIZO TFT technology used are presented below:

- Different blocks of the same layer must be separated by at least $10\mu m$.
- The overlaps between GATE and SOURCE/DRAIN must have a length of at least $5\mu m$.
- Metal holes have a size of $20 \times 20 \mu m$ and must be separated by at least $20\mu m$.

C.2 Basic Components

Figure C.1 shows the layout of an a-GIZO TFT with $W/L=40/20\mu m$. The layers are displayed both with and without filling to illustrate that there must be a $5\mu m$ overlap between the source and drain contacts drawn with SOURCE/DRAIN layer and the SEMICONDUCTOR and GATE layers that compose, respectively, the active region and gate of the TFT.

In figure C.2 is a representation of the only via that currently exists in this technology and its respective dimensions. This via interconnects the SOURCE/DRAIN and GATE layers, as although it cannot be seen in this picture, the area represented as GATE is overlapping a SOURCE/DRAIN area of the same size.

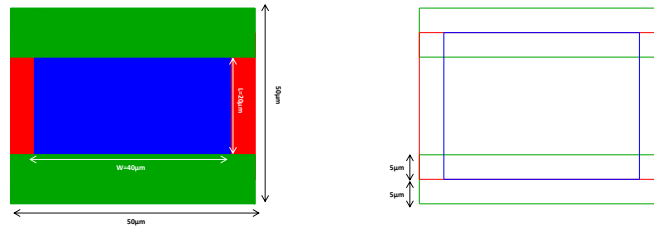


Figure C.1: Layout of an a-GIZO TFT with $W/L=40/20\mu\text{m}$

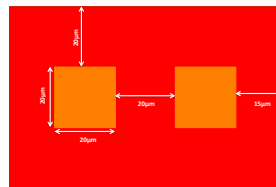


Figure C.2: Via that interconnects GATE and SOURCE/DRAIN layers

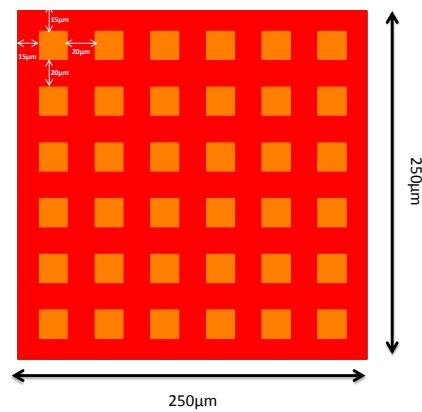


Figure C.3: External pad

Finally the layout of a capacitor is presented in C.4. One of the plates of the capacitance is done with GATE and the other with SOURCE/DRAIN, and the overlap between these two layers

is the corresponds to the area of the capacitance. During fabrication a dielectric layers is placed between these two layers in order to implement the capacitance but in the design of layouts the dielectric layer is not included. The capacitance value can be estimated considering that the dielectric constant, ϵ_r , is 10.5 and d , which is the distance between the plates of the capacitor is 300nm. Then the capacitance is calculated as

$$C = \frac{\epsilon_0 \cdot \epsilon_r \cdot A}{d}, \quad (\text{C.1})$$

where ϵ_0 is the permittivity of free space which is approximately equal to $8.85 \times 10^{-12} \text{ F/m}$.

Using the presented values the capacitance displayed in C.4 is estimated as having a value of 100pF.

$$C = \frac{8.85 \times 10^{-12} \times 10.5 \times (570 \times 10^{-6})^2}{300 \times 10^{-9}} \approx 100.64 \text{ pF} \quad (\text{C.2})$$

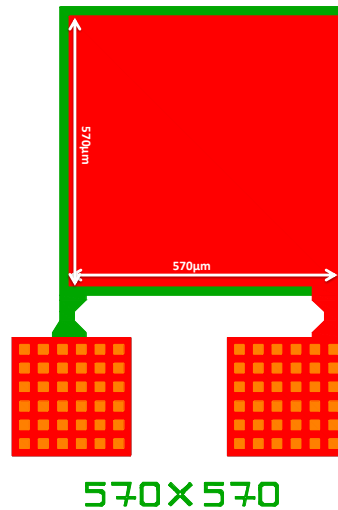


Figure C.4: Layout of a Capacitor

C.3 Additional layouts

In this section the remaining layouts designed are presented. The layouts sent for fabrication include the ones displayed here and those shown in sections 4.7 and 5.6.

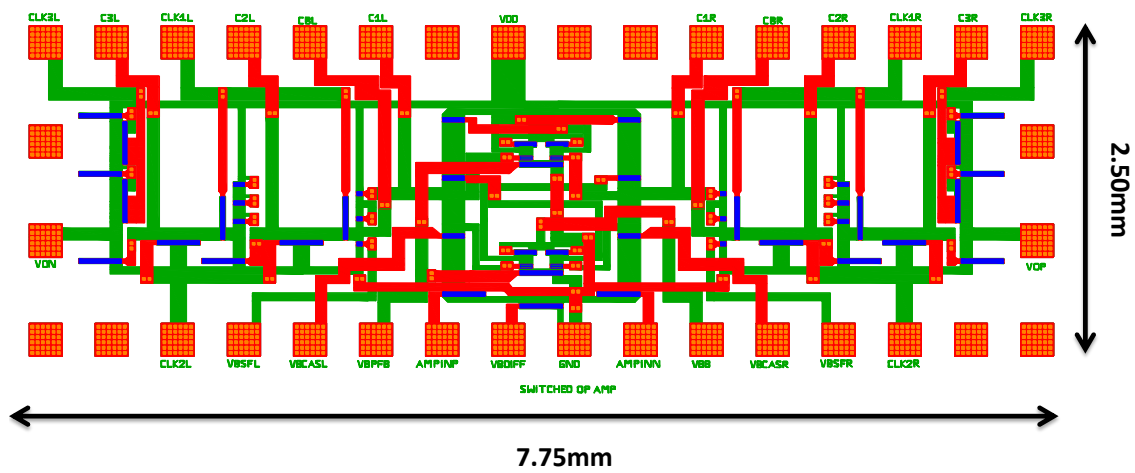


Figure C.5: Complete Layout of the Switched Opamp

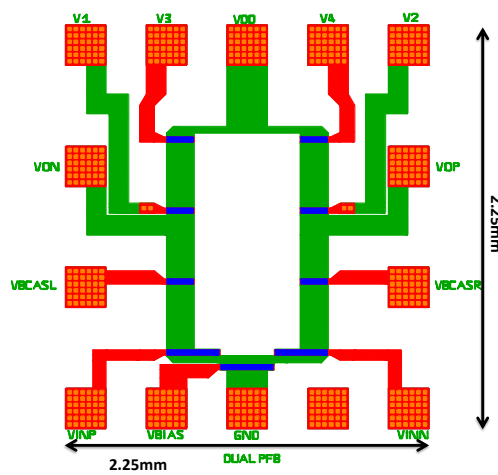


Figure C.6: Layout of the first stage without the positive feedback network

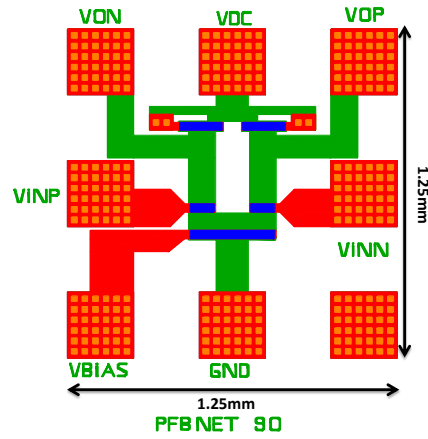


Figure C.7: Positive feedback network, drive transistors $W/L=90/20\mu m$, load transistors $W/L=160/20\mu m$

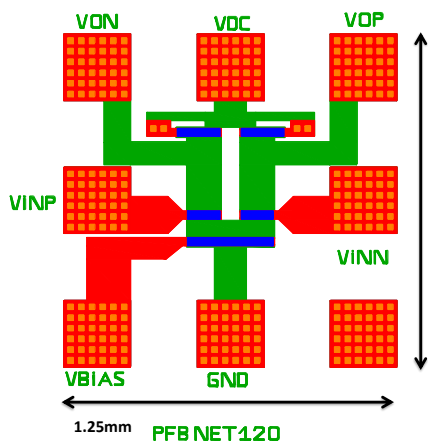


Figure C.8: Positive feedback network, drive transistors $W/L=120/20\mu m$, load transistors $W/L=160/20\mu m$

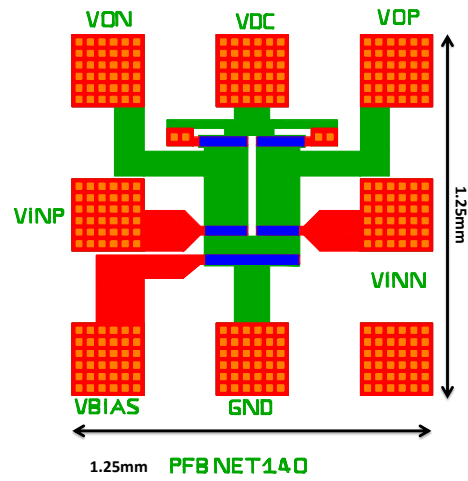


Figure C.9: Positive feedback network, drive transistors $W/L=140/20\mu m$, load transistors $W/L=160/20\mu m$

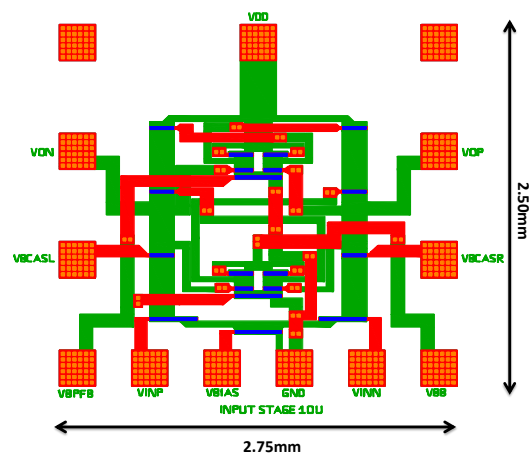


Figure C.10: Complete layout of the novel high-gain stage with only n-type enhancement transistors

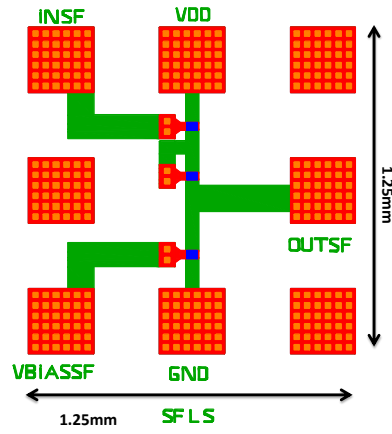


Figure C.11: Layout of the second Stage of the proposed opamps

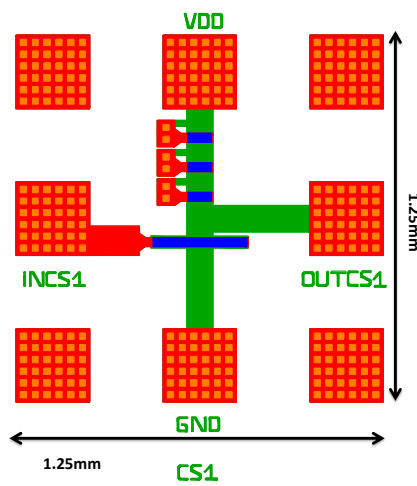


Figure C.12: Layout of the third stage of the regular opamp

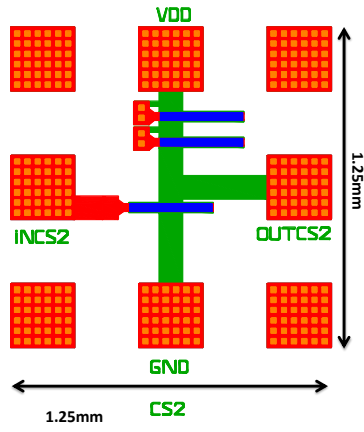


Figure C.13: Layout of the output stage of the regular opamp

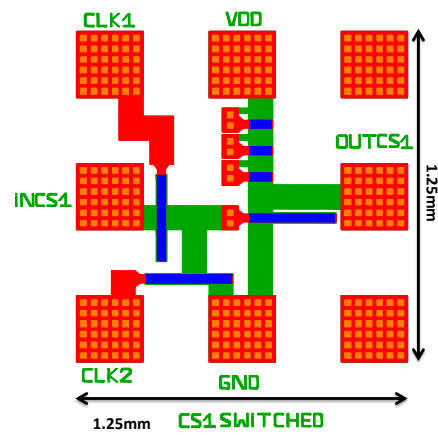


Figure C.14: Layout of the switched version the third stage of the switched opamp

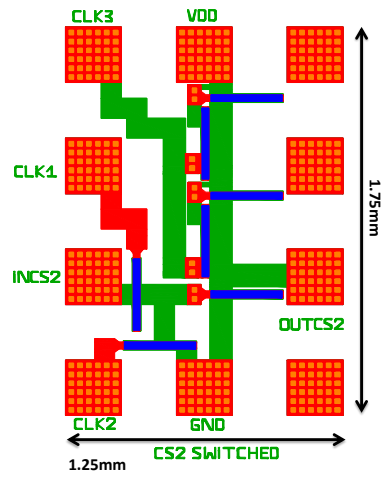


Figure C.15: Layout of the switched version of the output stage of the switched opamp

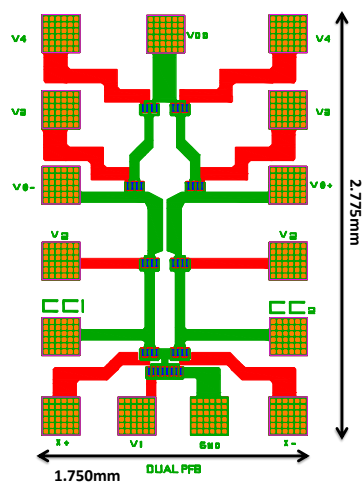


Figure C.16: Layout of the first stage without the positive feedback network, transistors with multifinger structure

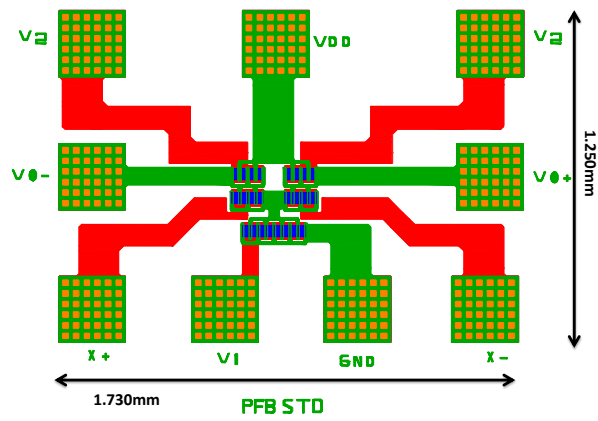


Figure C.17: Differential amplifier with positive feedback, positive feedback amplifier kept external

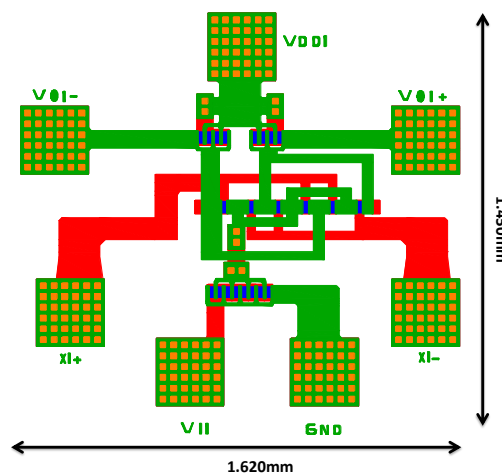


Figure C.18: Positive feedback network, drive transistors $W/L=120/20\mu m$, load transistors $W/L=160/20\mu m$, all transistors with multifinger structure

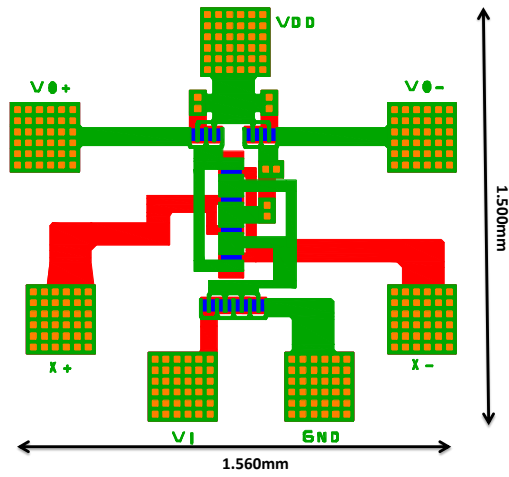


Figure C.19: Positive feedback network, drive transistors $W/L=140/20\mu m$, load transistors $W/L=160/20\mu m$, all transistors with multifinger structure

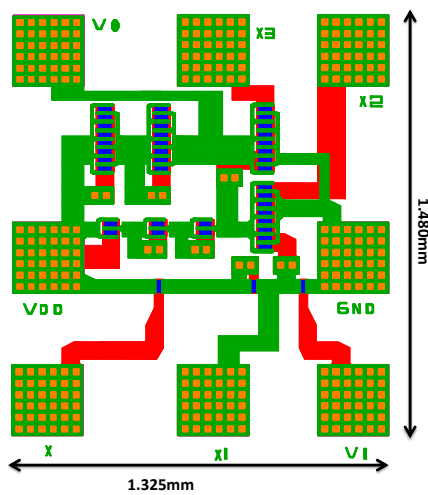


Figure C.20: Layout of all the stages that are connected to the output of the input stage

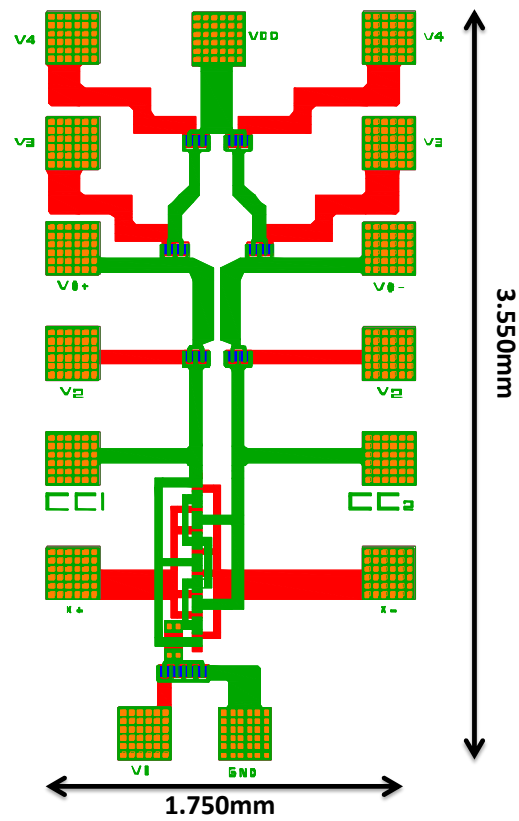


Figure C.21: Layout of the first stage without the positive feedback network, transistors with multifinger structure

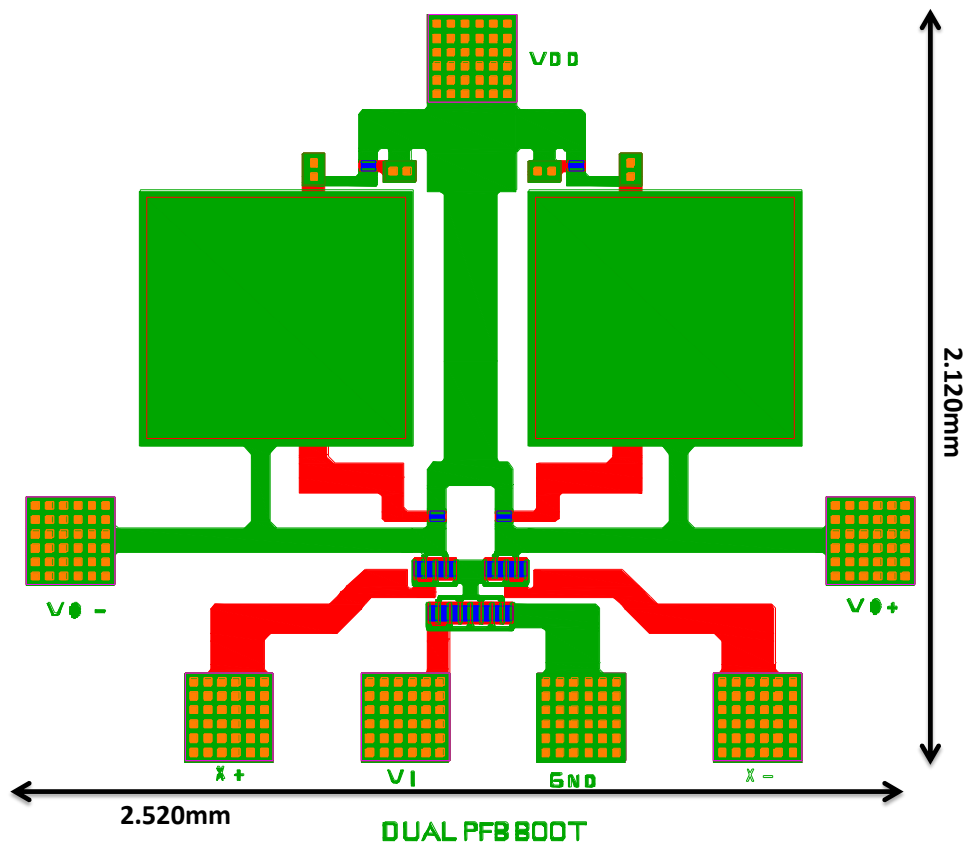


Figure C.22: Layout of the differential amplifier with single capacitive bootstrap load

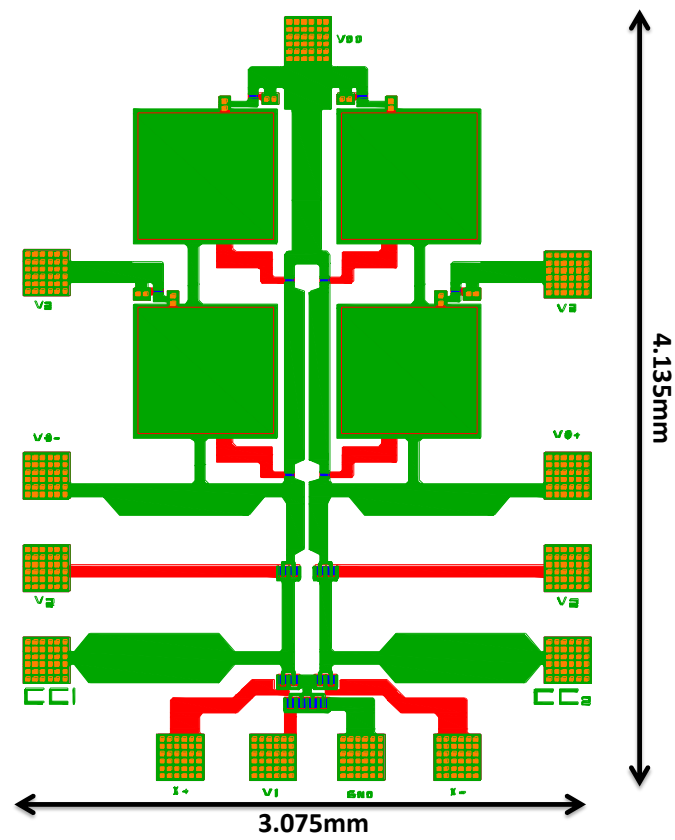


Figure C.23: Layout of the differential amplifier with cascade capacitive bootstrap load

Appendix D

Performing stability analysis of switched capacitor circuits in Cadence Spectre

The analog design environment in Cadence Virtuoso is a very powerful tool. It allows a user to run common circuit simulations such as transient, dc and ac analysis but it also gives the user the possibility of doing other types of advanced analysis such as closed loop stability analysis.

The focus of this work is switched capacitor circuits and for the analysis of these specific type of circuits all circuit simulations must be preceded by a *pss* (periodic steady-state) analysis. This analysis calculates the steady-state response of a circuit at a specified fundamental frequency and the circuit's periodic operating point. The periodic operating point is required to run small-signal analysis for periodic time-varying circuits.

To set up a *pss* analysis first launch the analog design environment in a schematic editor view in Virtuoso. To do so select Launch->ADE L. Then in the following window choose the analysis that is to be performed by selecting Analyses->Choose. A window such as the one depicted in figure D.1 will pop-up.

In this window select *pss* in the top part where all the different analysis are displayed, then select the *Auto Calculate* option next to the option *Beat Frequency*, in this way the software will determine the fundamental frequency of the circuit automatically as the lowest frequency used in it. With the a-GIZO model a great care must also be taken in the options selected for this analysis or the simulations might end up taking several hours, as the model is not optimized for this type of simulation. For this reason it is recommended to set the *Accuracy Defaults* to liberal and set a reasonable value for the maximum frequency of the *pss* analysis. To set the maximum frequency of the *pss* analysis press the *Options* button in the bottom part of the analysis window, then in the next pop-up window set the value in the *maxfreq* bracket under the *Accuracy* tab, as displayed in figure D.2. Keep in mind that this maximum frequency will limit all of the analysis that are carried out after this one, such as *pac* (periodic ac) analysis, for example, if the maximum frequency for *pss* is set as 1MHz it will not be possible to run *pac* with a frequency sweep that goes above this

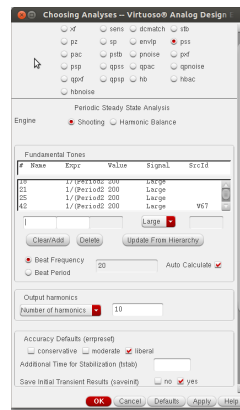


Figure D.1: Setting up a pss analysis in Cadence Virtuoso

frequency. Still, take also into account that the bigger the maximum frequency that is selected the more time it will take to run the circuit simulation. For this reason the *pss* analysis carried out had a maximum frequency of 1MHz as this value is considerably above the unity-gain frequency of the opamp topologies implemented in this work with a-GIZO TFTs.

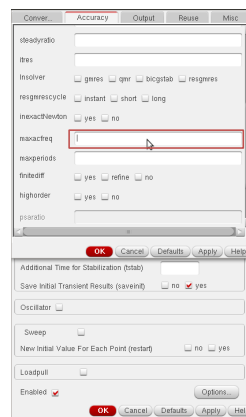


Figure D.2: Selecting the maximum frequency for the pss analysis

A very specific type of analysis that was executed in this work is dependent on a previous execution of *pss* and that analysis is designated as *psb* (periodic stability). The purpose of this analysis is verifying the stability of common-mode and differential loops. Therefore it serves to verify the stability of an opamp used in a closed loop switched capacitor configuration. For non-switched configurations there is the equivalent *stb* analysis that does not require a previous execution of *pss*. The stability analysis requires that the loop that is to be analysed be opened at some part, this is accomplished using a specific component that can be found in *AnalogLib*, the *cmdmprobe*. This component must be set within the loop to be analysed and it will serve the purpose of braking the loop automatically during simulation. This component has only a single option associated with it in a bracket designated as *CMDM*. This options must be set to 1 for

common-mode loops and to -1 for differential loops. After the probe is set within the loop to be analysed and with the correct option in the CMDM *parameter* according to the type of loop to be analysed the *pstb* analysis must be set up. To do this go again to Analyses->Choose, in the ADE L environment, and select *pstb* in the top of the pop-up window, figure D.3, then select the frequency range for the sweep and instantiate the *cmdmprobe* that was placed in the *Probe Instance* bracket by pressing the *Select* button and then clicking on top of the probe in the schematic. Note also that this analysis cannot be carried out without also running a *pss* analysis and no input signal must be applied to the circuit as the fundamental frequency for the *pss* analysis should be the switching frequency of the circuit.

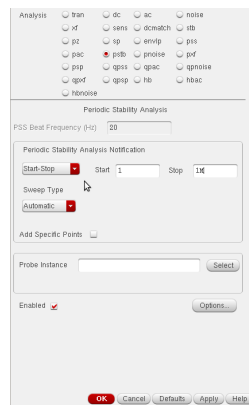


Figure D.3: Setting up a pstb analysis in Cadence Virtuoso

Then after both the *pss* and *pstb* analysis are complete the simulation results can be verified in the ADE L environment by selecting Results->Direct Plot->Main form. A pop-up window, figure D.4, will appear then select the *pstb* option on the top and you can now print the magnitude and phase of the open loop frequency response of the loop that was analysed or view a stability summary which immediately displays both the phase and gain margins of the loop.

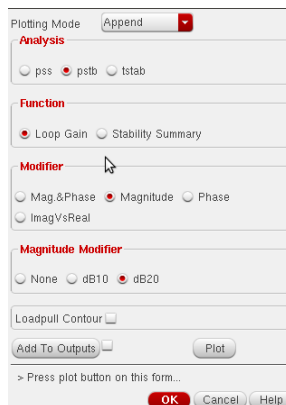


Figure D.4: Verifying the results of a pstb simulation

As a final note regarding these analyses it is important to stand out that when performing any analysis with the a-GIZO TFT verilog-A model that was used in this work an alteration must be made to the environment options of ADE L. To perform this alteration select Setup->Environment in ADE L and in the pop-up window that will appear add *veriloga* to the options presented in the first bracket, just as is depicted in figure D.5.

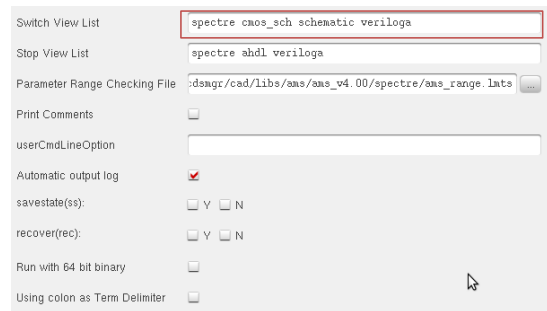


Figure D.5: Setting up the correct options to execute simulations in ADE L of circuits using the verilog-A model for a-GIZO TFT

Appendix E

I-V characteristics of the a-GIZO TFTs used

In figure E.1 the I-V characteristics of an a-GIZO TFT with $W/L=320/20\mu m$ are presented.

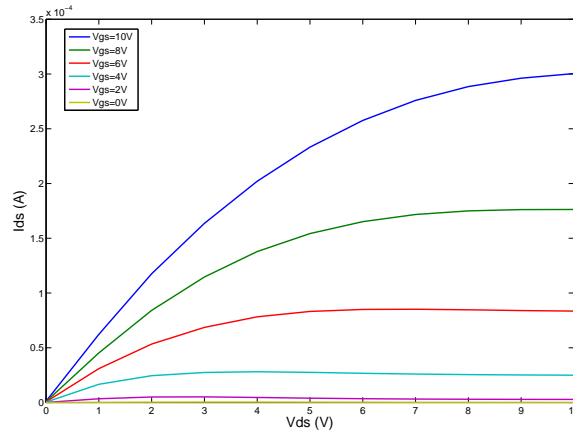


Figure E.1: I-V characteristics of a a-GIZO TFT with $W/L=320/20\mu m$. Results obtained from the neural network model

The negative values of g_{DS} obtained under some biasing conditions can be verified looking at figure E.2 which shows the current characteristics of the transistor for $V_{GS} = 4V$ and $V_{GS} = 6V$. In these two characteristics it can be seen that in the saturation region I_{DS} is decreasing with respect to V_{DS} .

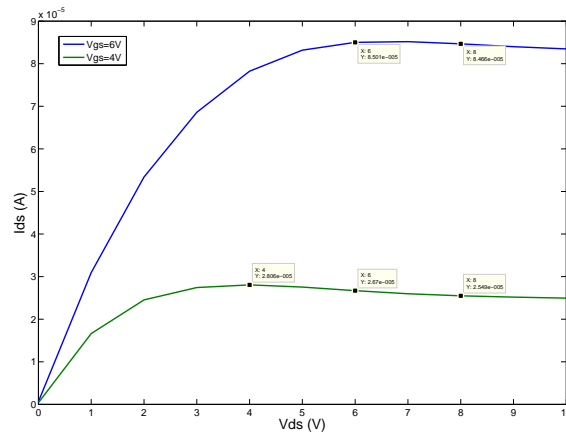


Figure E.2: Decrease of I_{DS} in relation to the increase of V_{DS} in saturation region

Figure E.3 illustrates the comparison between the level current characteristics for the $320/20\mu m$ a-GIZO TFT obtained with the neural network model developed from the measured I-V characteristics of the device and a level 1 MOSFET model fitted to the same measurements. There is a clear discrepancy between the measured results and those obtained through fitting. Therefore the level 1 model was not used in circuit simulations.

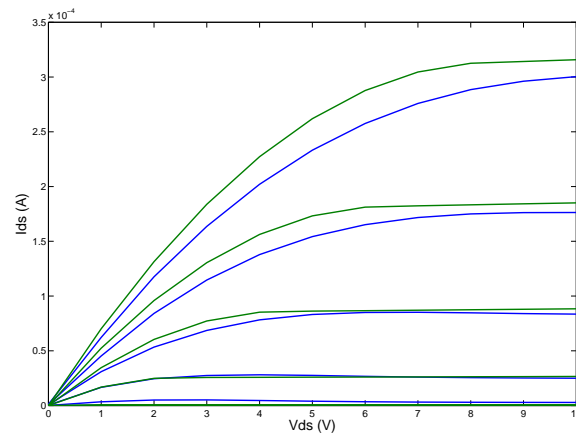


Figure E.3: Comparison between the measured I-V characteristics of a $320/20\mu m$ a-GIZO TFT (blue) and the characteristics obtained in simulation through fitting with the level 1 equations for MOSFET (green)

In terms of the estimation of the on resistance of this transistor in triode R_{on} it is done by placing the transistor in deep triode region and performing a sweep on V_{GS} . Then the derivative of the I_{DS} characteristic is taken and R_{on} is calculated as the inverse of the value of the derivative for a certain value of V_{GS} . From plot E.4 R_{on} is estimated as $1/(7.083 \times 10^{-6}) \simeq 141k\Omega$ for a $V_{GS} = 7V$. Therefore when approximating the switches implemented with a-GIZO TFTs, with ideal switches

to solve convergence problems, the R_{on} of these switches was made $150k\Omega$ in order to attain time constant similar to those obtained if transistors could be used in simulation to implement these switches.

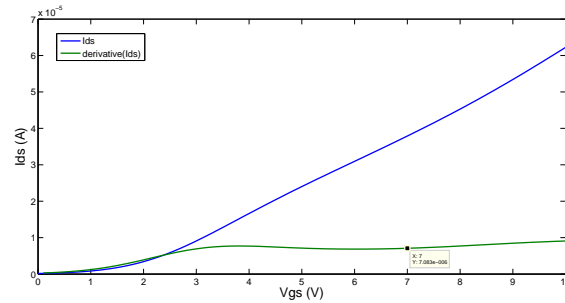


Figure E.4: Estimation of the R_{on} of an a-GIZO TFT with $W/L=320/20\mu m$

On the other hand the threshold voltage can be estimated by biasing the transistor in deep saturation, sweeping V_{GS} and plotting the tangent line for the linear part of the characteristic. This result of this simulation is shown in figure E.5. Here the threshold voltage is estimated as 1.557V.

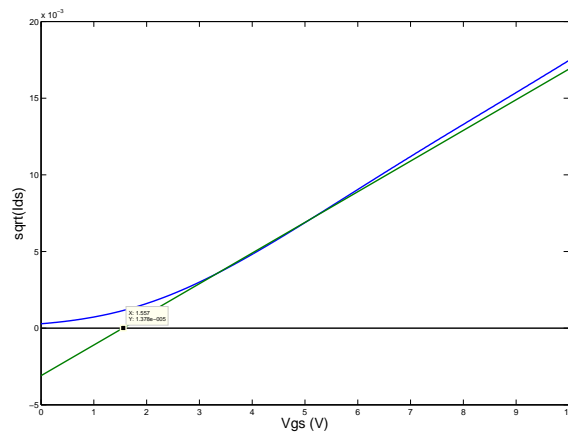


Figure E.5: Estimation of the V_{th} of an a-GIZO TFT with $W/L=320/20\mu m$

Appendix F

Previously Reported a-GIZO TFT Circuits

Until this date, several circuits with a-GIZO TFTs have been reported but most of them are digital. This tendency is explained with the lack of knowledge regarding some of the physical principles that influence the devices electrical characteristics, and by the inherent limitations that the technology presents. Most of the circuits reported are inverters and ring oscillators, however, a current-steering DAC, shift-registers and some analog circuits such as subtractors, adders and current mirrors, have also been reported.

In 2007 Ofuji et al. [43] reported the implementation of a five-stage ring oscillator using a-GIZO TFTs. This ring oscillator operated at a frequency of 410 kHz, corresponding to a delay of $0.24\mu\text{s}$ per stage, when supplied by a +18V power supply, presenting an output voltage swing of $7.5V_{p-p}$. All of the inverters that constituted the ring oscillators were implemented with n-type enhancement TFTs and presented a voltage gain of -1.7. The TFTs had channel lengths of $10\mu\text{m}$ and the channel widths for the drive and load transistors were $200\mu\text{m}$ and $40\mu\text{m}$ respectively. These a-GIZO TFTs employed a bottom-gate structure and were fabricated on a glass substrate. The semiconductor layer of the devices was deposited using RF sputtering and afterwards patterned by etching. The gate was composed of a trilayer of Ti/Au/Ti, and SiO_2 was used as the gate dielectric. The source/drain contacts were built with Ti/Au. The saturation carrier mobility in the channel for these TFTs presented a maximum value of $\mu_{sat} = 18.2\text{cm}^2\text{V}^{-1}\text{s}^{-1}$. This circuit was simulated in SPICE previously to implementation, approximating the model of a-GIZO TFT with a level 1 NMOS model, which correctly estimated the output voltage range of the circuit but led to a value of the oscillators frequency that was almost the double of the one measured in the physically implemented circuit. This difference is likely due to the imprecision that results of approximating the operation model of a-GIZO TFTs with that of an NMOS. This report was also the first practical implementation that demonstrated the superior performance of oxide

semiconductors, in terms of frequency operation, when compared to a-SI:H and organic TFTs.

In 2009 Lee et al. [44] reported the first full-swing a-GIZO TFT inverter using a depletion mode a-GIZO TFT as the loading device. The depletion type devices presented in this work were built by increasing the thickness of the active layer of the TFTs, which leads to a reduction of the saturation mobility of the TFTs as well as to a negative shift in their threshold voltage. The alteration of the carrier mobility is attributed to a possible increase of the device contact resistance, due to an increase of the distance between the source/drain contacts and the channel. When the thickness of the active layer is raised, it leads to an increase of the distance that the electrons have to travel within the semiconductor where no accumulation channel is formed, and consequently with a higher resistance than the channel region. The negative shift in V_{th} is possibly caused by an increased number of free carriers in the channel due again to the increased thickness of the active layer. This work also reported that the raise of the active layer thickness, in a-GIZO TFT, also degrades its off current and the subthreshold voltage swing, but this degradation did not present a serious influence in the switching characteristics of the inverter implemented. As a term of comparison, both the inverter with depletion-mode load and an inverter with enhancement load were implemented. The driver is an enhancement TFT, similar in both cases. The depletion load topology presents a superior output voltage swing, 19.6V versus 15.1V for the other, and as expected, with a significant increase in the magnitude of dc voltage gain, -37.4 versus -1.6. This increase in voltage gain is due to the higher load resistance of the diode connected depletion mode transistor, relatively to the same configuration but with enhancement mode transistor. The higher output swing shows that the usage of depletion mode loads increases the noise margins of inverters and that the switching characteristics of these circuits are also improved due to the increased voltage gain of the topology. The only trade-off being an additional mask necessary to fabricate depletion mode devices, in relation to the enhancement counterpart.

In the following year, Suresh et al. [45] reported ring-oscillators built with a-GIZO TFTs operating at higher frequencies, 2.1MHz for a 5 stage ring-oscillator, with 25V supply voltage. In this work the fabrication process was different than that used in the previous report of ring oscillators with a-GIZO TFTs, as the semiconductor layer was deposited by pulse laser deposition, the gate and source drain-electrodes were formed in ITO and Al_2O_3 was used for gate dielectric. The usage of ITO in the gate and source/drain electrodes made these a-GIZO TFTs fully transparent. The saturation mobility of the fabricated a-GIZO TFTs was reported as $\mu_{sat} = 15cm^2V^{-1}s^{-1}$. The improved results achieved in this work are possibly originated by the differences in the fabrication process, which may have resulted in smaller overlap capacitances. This work also reported a new simulation method. The measured dc characteristics of the a-GIZO TFTs were fitted in AIM-SPICE to construct the operation model of the device, which led to a better agreement between measured and simulated results than the reported by Ofuji et al. in their 2007 work.

Also in 2010, Jamshidi-Roudbari [46] designed and fabricated a ten-stage half-bit shift register

using a-GIZO TFTs. This circuit could operate at a maximum clock frequency of 40KHz, for a rail-to-rail supply voltage of 20 V, and was constructed with only bottom-gate staggered a-GIZO TFTs. This work was important to demonstrate the potential of the a-GIZO TFTs for the construction of system-on-panel (SoP) applications, especially in FPDs, with the possibility of incorporating in the same substrate the LEDs and the driving circuitry. Nonetheless, the TFTs used Al as the material for the source/drain electrodes therefore the circuit was not fully transparent

In 2011 Mativenga et al. [17] reported the fabrication of an 11-stage ring-oscillator and of a shift-register in a-GIZO TFTs deposited on flexible plastic substrates. The presented ring-oscillator had a lower operation frequency, 94.8kHz, than the reported ones in [43] and [45], which can be attributed to an increased number of stages and to the differences in the fabrication processes, namely the use of an increased width of the transistor channel, relatively to those used in previous reports of a-GIZO TFT ring oscillators. This work also applied an ac driving topology to the shift register previously proposed by the authors for a-Si:H TFTs [47]. The goal was to reduce the threshold voltage shift due to dc biasing, this in turn led to an estimated circuit lifetime of more than a decade, which is a very astonishing result in this technology.

In the same year, Zysset et al. [12] introduced the first bendable a-GIZO TFT transimpedance amplifier. The implemented amplifier topology is presented in figure F.1, it employs a load resistor R_l and a feedback resistor R_f that are made of a-GIZO TFTs with floating gate so as to use the resistance of the channel of these TFTs. Such option must be analysed carefully due to the devices parasitic capacities, especially the high-overlap capacitance that is usually present in bottom-gate staggered devices, which may lead to resistors that are not linear. The proposed amplifier exhibited a gain of 86.5 dB Ω and a cut-off frequency of 8.38kHz. The report also analysed the performance of this amplifier when stress tensions were applied verifying a 1 dB Ω decrease in the gain and a 1.45kHz increase of the cut-off frequency when a 5mm bending radius was applied to the circuit. The reduction in gain was attributed to a possible increase of electron mobility in the channel due to the applied strain. This work proved that the a-GIZO TFT technology presents promising characteristics for the implementation of signal amplification circuits that can be used in the future to build flexible system-on-panel applications.

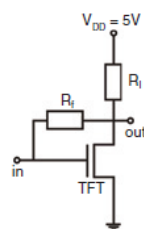


Figure F.1: Bendable a-GIZO TFT transimpedance amplifier proposed by Zysset et al. in 2011 [12]

Again in 2011, and in 2012 as well, Kim et al. [48, 49, 50, 51, 52] proposed several implementations of shift-registers using depletion mode a-GIZO TFTs. The objective of these functional blocks was to show the possibility of implementing driving circuits in a-GIZO TFTs in which the negative threshold voltage shift, due to illumination, was not as significant. Therefore, depletion mode TFTs were used instead of enhancement mode ones, because the former tend to present superior performance in terms of stability when compared to the latter. These circuits reinforced the possibility of implementing system-on-panel applications in the FPD industry, in the near future. But these shift register implementations present major drawbacks. Associated to the fact that more TFTs, power sources and input signals are required when compared to a shift register topology using an enhancement mode TFTs, which in turn leads to large circuit areas, higher power consumption and more complex circuit implementations result with depletion mode devices.

In 2011, Seok et al. [53] proposed a new way of accomplishing a full-swing inverter with a-GIZO TFTs using a depletion mode load. Unlike the inverter with a depletion load reported in [44], where the depletion mode transistor was attained by increasing the active layer thickness, at the cost of a reduction in the electrons mobility in the channel, and the degradation of the subthreshold voltage and off currents, the depletion mode load in this work was realized using a dual-gate a-GIZO TFT. This structure was able to vary the threshold voltage of the a-GIZO TFT by applying a constant positive bias to the top gate of the transistor, while a voltage sweep is applied to the bottom gate. If in turn the constant biasing of the top gate was negative, the threshold voltage would suffer a positive shift. This demonstrated that with the dual-gate structure it is possible to control the density of carriers in the accumulation channel and vary the characteristics of a a-GIZO TFT. The relation reported between the top gate bias voltage and the shift in the devices threshold voltage is approximately linear and given by $\Delta V_{th} \simeq -V_{TG}$. In this work the proposed inverter was also compared to an inverter using all n-type enhancement mode a-GIZO TFTs and the characteristics of the inverter, with depletion load, were again superior in terms of output swing. A setback of this implementation regarding the one in [44] is the fact that the magnitude of the voltage gain of the inverter, with the proposed depletion load, is much inferior to the one presented previously. This difference may be caused by the difference in the depletion mode load between both implementations, to differences in the fabrication process and to differences between the length and width of the TFTs. In fact transistors of the previous implementation presented much larger values of W and L, especially for the load transistor.

In 2011 as well, Kang et al. [54] reported the fabrication of ring oscillators with self-aligned co-planar top-gate a-GIZO TFTs. The objective of this work was to demonstrate the improvement in the performance of circuits when TFTs with lower parasitic capacitances are used. These capacitances occur in TFTs due to overlaps between the source/drain and gate electrodes, which is pronounced in a-GIZO TFTs employing bottom-gate structures, and are caused by misalignments

in the photolithographic processes during fabrication. As a result of this work, a 23-stage ring oscillator was reported, with a propagation delay of 17ns per stage, for a voltage supply of 22V, which is much inferior than the propagation delays reported in ring oscillators employing bottom-gate a-GIZO TFTs [43, 45, 17]. Even though, the number of stages used in this implementation is clearly superior. The improved performance of this circuit can be explained by a reduction of the intrinsic RC time constants of the a-GIZO TFT when a self-aligned co-planar top-gate structure is used, and by the possible superior mobility values in these TFTs, as the field effect mobility reported was $\mu_{fe} = 23.3\text{cm}^2\text{V}^{-1}\text{s}^{-1}$. Nevertheless, it is not possible to directly compare these mobility values with the ones of the previous reports because previous presentations only referred the saturation mobility of the a-GIZO TFTs used, which is not directly comparable to the field effect mobility.

Again in 2011, Münzenrieder [55] et al. reported a flexible 1-bit SRAM implemented with a-GIZO TFTs. In this work the performance of the circuit, when bending strains were applied, was again studied as in the transimpedance amplifier proposed in [17]. The bending of the circuit to tensile radii of 5 and 10mm originated only a small variation of the output signals in regard to the output of the flat circuit. On the other hand small bending radii of less than 5mm lead to the irreversible destruction of the circuit, attributed to the formation of micro cracks originated in some of the layers of the TFTs, namely the gate dielectric.

In 2012 Raiteri et al. [56] reported the first DAC manufactured with a-GIZO TFTs. The 6-bit DAC used a current steering approach and presented a spurious-free dynamic range (SFDR) greater than 30dB for frequencies up to 300kHz. This is the first mixed-signal application of a-GIZO TFTs and further reinforces the potentiality in system-on-panel applications requiring signal processing.

In the same year Luo et al. [57] reported the implementation of NAND, NOR and inverter logic circuits in a-GIZO TFTs. The TFTs used in these circuits were all n-type enhancement mode, employing a bottom-gate staggered structure and presented a threshold voltage of 0.2V, allowing the operation of the logic gates at small values of V_{DD} , down to 1.5V. In all of the logic gates implemented, the logic function was realized only by the pull-down network, the pull-up network was composed by a single diode-connected enhancement mode TFT. This work demonstrated that it is possible to implement logic gates in a-GIZO TFT technology, but as expected, due to the limitations of the technology, such as the high overlap capacitances, the maximum operation frequencies are very reduced when compared to logic gate implementations in other technologies such as CMOS. However, the performance of this devices can be further improved for example using other types of TFT structures, such as the self-aligned co-planar top-gate used in [54] which would lead to a decrease of the intrinsic RC time constant associated with each TFT,

thus improving the maximum frequency of operation of the logic gates.

Also in 2012, Geng et al. [58] reported the first shift register implemented with self-aligned co-planar a-GIZO TFTs. All of the TFTs presented high values of saturation mobility, reported as $\mu_{sat} = 24.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a low threshold voltage of 0.2V, which allows for low-voltage power supplies, as low as 1V. The values of rise and fall times achieved were faster than the ones previously reported, resulting in a maximum operation frequency of approximately 500kHz. This result can be attributed to a reduction of the parasitic capacitances of the TFTs when compared to the ones used in previous reports. This work reiterated that it is possible to achieve circuits with better performance by using other structures than the staggered bottom-gate. A setback that might occur in these topologies is the negative shift in V_{th} due to illumination stresses that was not accounted for in this work and that would hinder the lifetime of this circuit if it were to be used in commercial applications.

The first work solely focused on the implementation of analog circuits with a-GIZO TFTs was reported in late 2012 by Bahubalindrani et al. [37] and focused on a methodology for modelling and simulation of analog circuits with n-type enhancement a-GIZO TFTs. The main concept introduced in this work was the modelling of the static behaviour of an a-GIZO TFT through the use of an artificial neural network in order to avoid complex physical models whilst still achieving a high level of accuracy in the modelling of the device. The proposed model was implemented in Verilog-A in order to allow the simulation of a-GIZO TFT circuits with computer-aided design tools (CAD). The possibility of being able to possess an accurate model of small and large-signal operation for a-GIZO TFTs is of paramount importance because only with such tools, can a circuit designer run accurate simulations that can, at least, approximately predict what will be the behaviour of physically implemented circuits. This in turn accelerates the design process and reduces costs. It is not viable to fabricate a circuit each time a new topology is conceived just to find out in the end that the behaviour of the circuit implemented is much different than the one indicated in simulations. The validity of this model was tested through Cadence Spectre and used to simulate the behaviour of basic analogue circuits, such as adders, subtractors and a current mirror. It is reported that the proposed model can accurately predict the performance for static conditions and low-frequency-operation of n-type enhancement mode a-GIZO TFTs when the results from simulation are compared with measured data. A setback of this work, which must be further explored in the future, is the characterization of the devices parasitic capacitances which tend to be an important limitation in the bandwidth of analog circuits constructed with these TFTs.

In late 2012 Cho et al. [59] introduced a new method of achieving a depletion mode a-GIZO TFT that does not require an extra mask in the fabrication process as in [44]. The depletion mode TFT is attained exploring the negative shift in the threshold voltage of an a-GIZO TFT due to negative bias illumination temperature stress. In this work this effect usually seen as a limitation is purposely induced in the load TFT to shift its threshold voltage to negative values and force a

depletion mode operation on the transistor. This work demonstrated that it is possible to achieve n-type depletion mode a-GIZO TFTs from n-type enhancement mode ones without changing or adding any step in the fabrication process of the later. Nonetheless, the shift in the threshold voltage induced in this work is reversible over time which will degrade the performance of the inverter in the long run, limiting its application in systems with a long life-cycle.

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