A Built-In Mixed-signal Block Observer (BIMBO) to improve observability in 1149.4 environments

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Abstract

This document proposes an extension to the IEEE 1149.4 test infrastructure [1], whereby a bank of sigma-delta first order modulators enables the simultaneous observation of several analog pins in a single component. The modulator output bit streams are shifted out and made available to an external test controller that comprises the corresponding bank of decimation filters and other decision and control logic. The architecture proposed is fully non-intrusive and may be used to support debug and test operations in mixed-signal environments.

Introduction

The traditional wiring of the 1149.4 ATAP pins in a mixed-signal printed circuit assembly (PCA) supporting this IEEE test standard uses one line to interconnect all AT1 pins, and another line to interconnect all AT2 pins. Several analog output pins in one or more components may therefore be driven simultaneously by an analog stimulus applied at the PCA AT1 pin. However, only one analog pin may be observed at each time (since all AT2 pins are in parallel). This observability bottleneck restricts the usefulness of this test infrastructure in some parametric measurement setups and is of little help for debub and test scenarios, where the observability of several analog signals at once plays a key role for prototype validation. This paper proposes a built-in mixed-signal block observer (BIMBO) that overcomes this limitation. The overall architecture of BIMBO is first presented, followed by a short discussion concerning cost / benefit issues. A final section summarises the advantages of the proposed solution.

Architecture of the proposed solution

The first-order modulator stage in sigma-delta A/D converters oversamples an analog input signal to produce a 1-bit representation that shows its variation in time. Such blocks have low area overhead and produce a serial output which enables a high-resolution digital representation of the analog input [2]. However, this representation requires a decimation filter that is capable of converting the output bit stream of the modulator stage into an N-bit digital representation. The implementation of this block requires a much larger silicon area, and as such the inclusion of a complete sigma-delta architecture into a mixed-signal component, just to enable observability, is normally not acceptable.

The proposed solution takes advantage of the 1149.4 transport chain to deliver the output bit stream of the first-order modulator stages to an external test controller block, where the decimation filters, and other decision and control logic, support debug and test operations as defined by the user. The BIMBO architecture described in this document is restricted to the internal circuitry that extends the 1149.4 test infrastructure. The basic concept underlying BIMBO may be described as presented in figure 1, where a bank of four first-order modulators oversample the selected analog pins and produce serial bit streams which are then interleaved by the multiplexer that drives the TDO pin, when the corresponding 1149.4 instruction is active. All four sigma-delta modulators are driven by the same clock signal.

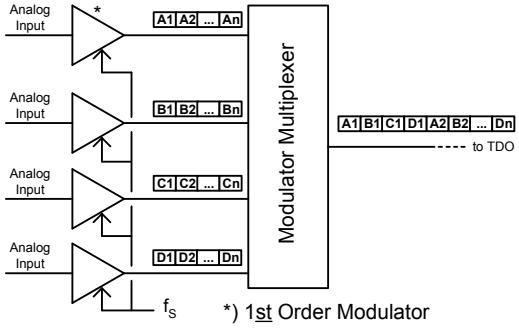

Fig. 1: Interleaving the oversampled representation of the selected analog signals.

The architecture of the proposed solution may then be represented as illustrated in figure 2, which shows how BIMBO interacts with the 1149.4 infrastructure. The acquisition of the input samples takes place once for each four TCK cycles.

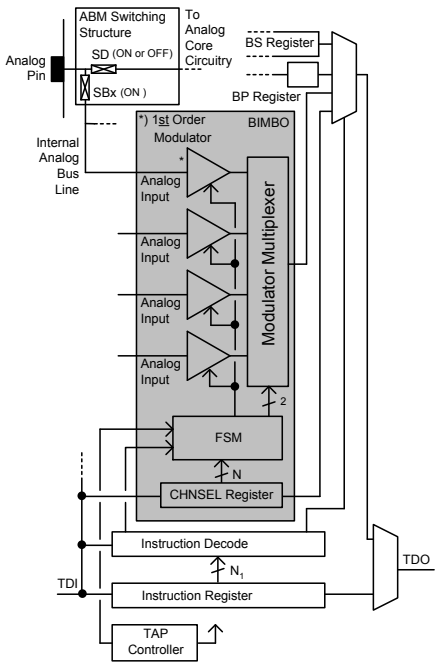

Fig. 2: Overall architecture of BIMBO.

The ABM switching structures (via SBx) define which signals are to be connected to the first-order modulators. Since the operation of BIMBO is non-intrusive, the SD switches in the ABM switching structures may be closed to enable the circuit mission mode. Notice that the modulator multiplexer is driven by a finite state machine (FSM), which is in turn controlled by an optional 1149.4 register called CHNSEL. The access protocol to this 1149.4 test extension is defined as follows:

1. Use SAMPLE / PRELOAD to load the control structure of the ABMs with the 4-bit words defining which analog pins are to be observed (i.e. which SBx switches are to be closed).
2. Using the optional 1149.4 instruction that selects CHNSEL, load into this register a 4-bit word that defines which modulator stages will be active (any combination of modulator stages may be chosen; the output of the remaining modulators is not used in the interleaving process).
3. Load the optional 1149.4 instruction that drives the modulator multiplexer output into TDO, and take the TAP controller into the Run Test / Idle (RT/I) state.
4. While in RT/I, the application of TCK cycles will carry the interleaved modulator output bit streams to the external test controller containing the corresponding bank of decimation filters.

The number of first-order modulators dictates how many internal analog bus lines are required. A bank of four modulators, as shown in figure 1, would require a partition of the internal analog bus, as described in the IEEE 1149.4 standard [1, sec. 6.5, *Partitioned internal test bus structure*]. In this case, the internal organisation of the extended 1149.4 architecture may be represented as illustrated in figure 3. However, if the required observability does not exceed two analog pins per component, the basic two-line internal analog test bus is sufficient.

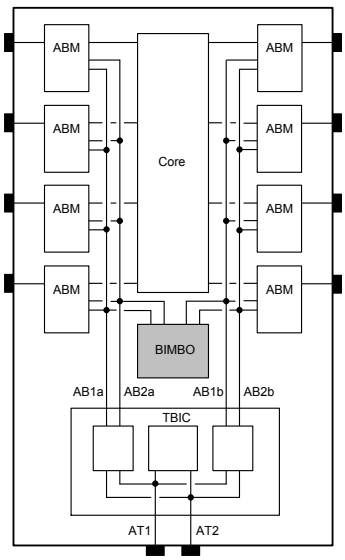

Fig. 3: Extended 1149.4 infrastructure to support the simultaneous observability of four analog pins per component.

All the remaining 1149.1 / 1149.4 components in the PCA must be in the BYPASS (BP) mode, and the transport chain made up by the PCA TDO-TDI interconnections and the BP register cells will be used to carry the modulator output bit streams to the external test controller.

Cost / benefit analysis (observability / silicon area / frequency)

Since the output bit stream shifted to TDO is driven by TCK, the frequency of the 1149.4 test clock signal dictates the maximum oversampling frequency when a single analog pin is under observation via BIMBO. When N analog pins are under observation simultaneously, interleaving the modulator outputs dictates that the maximum oversampling frequency is now given by (TCK / N). If we assume a 20 MHz TCK clock and an oversampling factor of 500, the maximum frequency of the analog signals is limited to 40 KHz when only one analog pin is under observation, or to 10 KHz when four analog pins are being observed simultaneously.

The additional circuitry imposed by BIMBO grows linearly with the number of observation channels. However, when more than two pins are to be observed simultaneously, a partition of the internal analog bus becomes necessary. Increasing the observability requirements naturally leads to higher silicon overhead and imposes a lower limit on the maximum frequency of the analog signals under observation. Notice that a basic BIMBO with two observation channels does not require the partition of the internal analog test bus.

Advantages of the inclusion of BIMBO

The main advantages of the proposed solution may be summarised as follows:

- Observation of the analog pins may be carried out in a transparent manner while the circuit operates in mission mode, since the extension proposed to the 1149.4 architecture is fully non-intrusive.
- The switching structure of the TBIC and the ATAP pins are not used by BIMBO, so it is possible to use the ATAP while BIMBO is in operation.

Since the same analog pin may be observed directly via AT2, and also in digital form via the output bit stream of a first-order modulator, it becomes possible to analyse the influence of the 1149.4 switching structures and eventually to carry out calibration operations with the objective of avoiding / correcting signal distortion.

While not necessarily an advantage, this feature may enhance the reliability of mission-critical circuits, where continuous online monitoring of the circuit performance is desirable.

References

[1] IEEE Std 1149.4-1999: IEEE Standard for a Mixed Signal Test Bus, ISBN 0-7381-1755-2.

[2] G. R. Alves, J. M. Martins Ferreira, “Using the BS Register for Capturing and Storing n-bit Sequences in Real-Time,” Proc. of the 1999 European Test Workshop (ETW'99), pp. 130-135.