FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

FPGA implementation of OFDM signals for application to radio-over-fiber systems

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Resumo

Os sistemas rádio-sobre-fibra consistem em transportar de forma (idealmente) transparente sinais rádio ao longo de uma rede baseada em fibra ótica devido à baixa atenuação e elevada largura de banda. Desta forma, estes sistemas permitem simplificar a arquitetura das estações-base remotas, transferindo funções complexas para a estação central.

No entanto, devido à não-linearidade dos vários componentes do sistema, os sinais RF (*radio-frequency*) analógicos sofrem distorção de intermodulação.

No caso dos sinais OFDM (*Orthogonal Frequency-Division Multiplexing*), as não-linearidades são bastante penalizadoras devido ao seu elevado *peak-to-average ratio*. Contudo, estes sinais têm sido adotados em praticamente todos os standards de comunicações wireless uma vez que a sua implementação em hardware é eficiente, possuem elevada eficiência espectral e um bom desempenho na presença de canais multi-percurso.

Com o objetivo de minorar estes problemas, as soluções de rádio digitalizado sobre fibra têm vindo a ser estudadas e apontadas como alternativa aos sistemas rádio-sobre-fibra analógicos. Esta técnica abre também a possibilidade de desenvolver redes *backbone* de distribuição de sinais RF digitalizados, de forma integrada com as atuais/futuras redes óticas digitais de alto débito.

Assim, como alternativa aos sistemas convencionais de rádio digitalizado sobre fibra, neste trabalho pretendeu-se implementar uma solução inovadora baseada num modulador sigma-delta utilizando para isso uma plataforma reconfigurável que permita gerar os sinais OFDM presentes nos vários standards permitindo avaliar o seu desempenho em sistemas rádio-sobre-fibra. Ao usar um modulador sigma-delta como conversor analógico-digital, a conversão digital-analógica no recetor é efetuada através de uma simples filtragem passa banda.

A criação do gerador de sinais OFDM, foi modelado com ajuda do software *Xilinx System Generator* e *Simulink*. De seguida, o sistema foi sintetizado e implementado através do software *Xilinx Vivado* para a placa *Xilinx Virtex-7 VC7203*.

O sistema foi testado e validado em laboratório usando equipamento de geração e receção/desmodulação de sinal, considerando como canal uma ligação ótica com lasers do tipo VCSEL (*Vertical-Cavity Surface-Emitting Laser*).

Abstract

The radio-over-fiber systems (RoF) consists of transporting radio signals over a network based on optical fiber in a (ideally) transparent way, due to its low attenuation and high bandwidth. Thus, these systems allows to simplify the architecture of the remote base stations, transferring complex functions to the central station.

However, due to the nonlinearity of the various system components, the analog RF (radio-frequency) signals suffers from intermodulation distortion.

In the case of the OFDM (Orthogonal Frequency-Division Multiplexing) signals, the non-linearities are very penalizing, due to their high peak-to-average ratio. However, these signals have been adopted in almost all wireless communication standards since its hardware implementation is efficient, have high spectral efficiency and good performance in the presence of multipath channels.

In order to reduce these problems, the digitized radio-over-fiber (D-RoF) solutions have been studied and identified as an alternative to analogue radio-over-fiber (A-RoF) systems. This technique also opens the possibility of developing distribution backbone networks of digitized RF signals, integrated with current/future high throughput digital optical networks.

Thus, as an alternative to conventional D-RoF systems, in this work is implemented an innovative solution based on a sigma-delta modulator (SDM) using for this a reconfigurable platform that generates the OFDM signals. Then, it is possible to evaluate their performance in RoF systems. Thus, using a SDM as analog-to-digital converter (ADC), the digital-to-analog conversion in the receiver is performed by a simple bandpass filtering.

The creation of the OFDM signals generator, was modulated with help of Xilinx System Generator (XSG) and Simulink software. Then, the system was synthesized and implemented through the Xilinx Vivado software.

The system was tested and validated in the laboratory using generation and reception/signal demodulation equipment, considering lasers of VCSEL (Vertical-Cavity Surface-Emitting Laser) type as an optical channel.

Acknowledgements

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Davide Cerqueira

"Há duas palavras que não se podem usar:
uma é sempre, outra é nunca."

José Saramago

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Abbreviations

ADC	Analog-to-Digital Converter
A-RoF	Analog Radio-over-Fiber
BPF	Band-pass Filter
BS	Base Station
CIC	Cascaded Integrator-Comb
CP	Cyclic Prefix
CS	Central Station
DAC	Digital-to-Analog Converter
DFT	Discrete Fourier Transform
DSP	Digital Signal Processing
DSO	Digital Storage Oscilloscope
DUC	Digital Up-Converter
D-RoF	Digital Radio-over-Fiber
EMI	ElectroMagnetic Interference
EVM	Error Vector Magnitude
FDM	Frequency Division Multiplexing
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
GSM	Global System Mobile
ICI	InterChannel Interference
IDFT	Inverse Discrete Fourier Transform
IFFT	Inverse Fast Fourier Transform
ILA	Integrated Logic Analyzer
IMD	Inter-Modulation Distortion
ISI	InterSymbol Interference
LTE	Long Term Evolution
LFSR	Linear-Feedback Shift Register
MER	Modulation Error Ratio
MIMO	Multiple-Input-Multiple-Output
MMCM	Mixed-Mode Clock Manager
NRZ	Non Return to Zero
NTF	Noise Transfer Function
OEC	Optical-Electrical Converter
OFDM	Orthogonal Frequency-Division Multiplexing
OSR	OverSampling Ratio
PA	Power Amplifier
PD	Photodiode
PISO	Parallel-Input-Parallel-Output
PON	Passive Optical Network
PPG	Pulse Pattern Generator
QAM	Quadrature Amplitude Modulation

QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RMS	Root Mean Square
RoF	Radio-over-Fiber
RTL	Register Transfer Level
SDM	Sigma-Delta Modulator
SMF	Single Mode Fiber
SNR	Signal-to-Noise Ratio
STF	Signal Transfers Function
VCSEL	Vertical-Cavity Surface-Emitting Laser
VSA	Vector Signal Analyser
VSG	Vector Signal Generator
WLAN	Wireless Local Area Network
XSG	Xilinx System Generator
ZOH	Zero Order Hold

Chapter 1

Introduction

1.1 Context

This document reflects the work performed in the final curricular unit of Integrated Master in Electrical and Computer Engineering course in the current year of 2015/2016.

The high transmission speed and bandwidth, the need to communicate without dependence on structures and access points on physical media as well as the reduction of implementation costs, are requirements of new technologies and emerging telecommunications services. Thus, to meet these requirements has emerged the concept of RoF systems, which is the subject of research by the group Optical and Electronic Technologies at INESC-TEC.

The RoF systems combine the advantages of optical communication with radio communication, and is used in transporting radio signal over optical fiber by means of an optical carrier between a remote site, were most of the signal processing is performed and a central node of a cellular network. These systems are considered to be the most economically viable and promising solutions for the implementation of wireless access networks, offering dynamic, multi-service and flexibility to users in specific environments. Those environments are mentioned in the next paragraph.

There are several application areas for RoF technology because it can be used to provide wireless service in hard-to-reach areas (where installation of big equipment is not feasible, such as tunnels and mountainous regions) and in telecommunications networks to make the connection between the central station and the base station. It allows the transfer of data with a desired bandwidth besides protecting the transmission from electromagnetic interference. RoF technology can also be used in satellite communications, because the satellite base stations can be connected through optical interlaces.

Thus, RoF is suitable for technologies that take advantage of optical fiber such as broadband technology and high frequencies, i.e., broadband mobile networks (3rd and 4th generation mobile), wireless network and ultra broadband networks. Apart from these applications, RoF is suitable for another high-bandwidth and high-bitrate telecommunication technology such as Passive Optical Network (PON). With RoF this technology can remove the need to convert the RF signals before

delivery to the end user and may also transmit signals of multiple services on the same fiber optic connection.

An other application scenario for a RoF system is one that allows for indoor environment, offer various services such as television service, mobile phone service and wireless Internet service over a single network of RoF.

1.2 Motivation

OFDM is an innovative modulation format for optical communications, where data is transmitted over many orthogonal subcarriers using the Fourier transform. With this new modulation format it is possible to transmit with a high-data-rate in a selective radio channel frequency. The digital signal processing can be performed at the transmitter side to take into account the transmission channel characteristics. At the receiver side, each sub-carrier is processed independently.

OFDM has advantages such as high spectral efficiency, a good performance in the presence of multipath channels and therefore has been adopted in almost all standards for wireless communications. Therefore, it is essential to develop a DSP (Digital Signal Processing) to generate OFDM signals present in the various standards, using for this a reconfigurable platform like Field Programmable Gate Array (FPGA). This platform provides a high interface data rate, parallel use of resources and allows greater flexibility to do various modifications and test different alternatives, such as different OFDM synchronization methods.

Thus, a platform which generates OFDM signals allows me to evaluate the performance/viability of the implemented design in RoF systems.

1.3 Objectives

The main objective of this dissertation project is the FPGA implementation of an OFDM modulator for application to RoF systems. The first objective for this dissertation is the extensive study of RoF, OFDM systems and the proper hardware architecture for implementation of the OFDM modulator. Then, the next objective is the implementation of the OFDM modulator, with it follows the functional validation of the hardware and FPGA verification of the implemented system. The last objective is the validation of the system in laboratory which will be performed using signal generation and reception/demodulation equipment and considering as channel an optical connection with a laser of the VCSEL type, performing a comparative study between simulation results and the results obtained experimentally.

1.4 Structure

This dissertation is organized as follow. Besides the introduction, this dissertation contains five more chapters. The fundamentals of OFDM are first introduced through theoretical derivations in chapter 2. The fundamentals of radio-over-fiber, the chosen method to evaluate the system and

related work are also described in this chapter. Chapter 3 presents a high-level perspective of the implemented design. Chapter 4 focuses on the system modeling of the OFDM functional blocks. For each function block, simulation results are presented for system verification. The results of the laboratory validation of the design, the implementation results and resource usage are summarized in chapter 5. The validation process of the design are also presented in this chapter. Finally, chapter 6 concludes the thesis and provides an outlook of future work.

Chapter 2

Fundamental concepts

This chapter covers the fundamental concepts of this dissertation. Section 2.1 describes the Radio-over-Fiber system. Section 2.2 characterizes the Orthogonal Frequency Division Multiplexing. Section 2.3 describes the Digital Radio-over-Fiber system. Section 2.4 describes the main parameters for evaluating the performance of transmission. Finally, section 2.5 describes the related work that was analyzed.

2.1 Radio over Fiber

2.1.1 Introduction

Since the beginning of the 80s that methods to carry RF signals in optical fibers have been developed, the first transport was performed in 1980 by Brenci and Checcacci [1]. In 1990, A. J. Cooper wrote an article with the first demonstration of an RoF system applied in mobile networks, where he proposed and demonstrated a short-range wireless telephone application called CT2, operating under an optical fiber link [2].

In the last years, with the implementation of the fourth-generation mobile network systems (4G) or also known as LTE (Long Term Evolution) and MIMO (Multiple-Input Multiple-Output) systems to be increasingly used, the RoF technology has come to be associated with these technologies.

The FUTON project started in 2008 and completed in 2010, was one of the most important projects that used RoF technology. A flexible architecture for wireless systems based on the joint processing of the radio signals from distinct remote antenna units and supported by a transparent fibre infrastructure was developed and validated in this project [3].

An RoF system consists of an RF signal modulated on an optical carrier, which is transmitted by an optical fiber [4]. The RF signals are thus transmitted over optical fiber between a central station (CS) and several base stations (BS) and are then sent to the transmitting antenna and radiated to multiple devices, as shown in figure 2.1. These systems are mainly intended to simplify the base stations, since all processing of the signals transmitted are on the central stations.

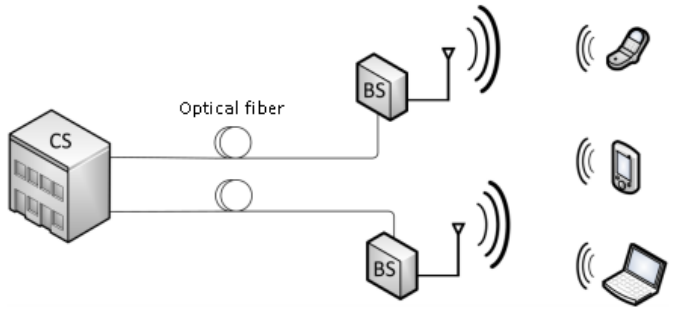


Figure 2.1: Radio over Fiber system concept (from [5]).

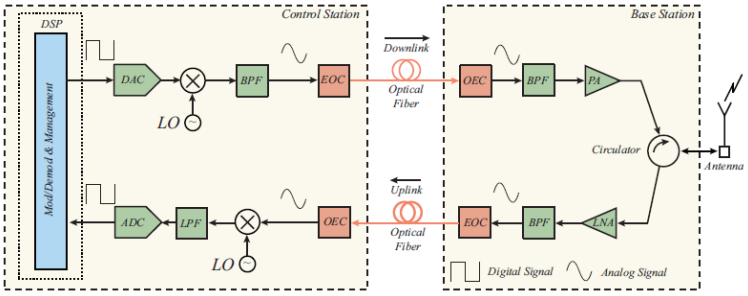


Figure 2.2: Diagram of a generic Radio-over-Fiber architecture (from [6]).

Figure 2.2 depicts a low-level typical radio-over-fiber scheme, this figure is a complementary figure of the previous one. This system is typically called as Analog Radio-over-Fiber and for this dissertation the most important transmission path is the downlink. So, DAC means digital-to-analog converter, LO means local oscillator, BPF means bandpass filter, EOC means electrical-optical converter, OEC means optical-electrical converter and finally PA means power amplifier.

2.1.2 Advantages

Some of the advantages of using the RoF technology are related to the use of fiber optics to transport RF signals and with the possibility of centralizing the processing in one single location (CS). Some of these advantages are described below [7].

2.1.2.1 Low attenuation loss

Since optical fibre offers very low loss, RoF technology can be used to achieve both low-loss distribution of millimeter waves, and simplification of the BSs at the same time. By transmitting microwaves in the optical form, transmission distances are increased several folds and the required transmission powers reduced greatly.

2.1.2.2 Large bandwidth

Another advantage of RoF is large bandwidth, this is achieved because optical fibres offer enormous bandwidth. This enormous bandwidth allows RoF technology a high capacity for transmit-

ting microwave signals. The high optical bandwidth also enables high speed signal processing. In other words, some of the demanding microwave functions such as filtering, mixing, up- and down-conversion, can be implemented in the optical domain.

2.1.2.3 Immunity to electromagnetic interference

Immunity to ElectroMagnetic Interference (EMI) is a very attractive property of optical fibre communications, especially for microwave transmission. This is so because signals are transmitted in the form of light through the fibre. Because of this immunity, fibre cables are preferred even for short connections at millimeter waves. Related to EMI immunity is the immunity to eavesdropping, which is an important characteristic of optical fibre communications, as it provides privacy and security.

2.1.2.4 Easy installation and maintenance

In RoF systems, complex and expensive equipment is kept at the CS, thereby making the BSs simpler. For instance, most RoF techniques eliminate the need for an local oscillator and related equipment at the BS. In such cases a photodetector, an RF amplifier, and an antenna make up the BS. Modulation and switching equipment is kept in the CS and is shared by several BSs. This arrangement leads to smaller and lighter BSs, effectively reducing system installation and maintenance costs. Easy installation and low maintenance costs of BSs are very important requirements for millimeter wave systems, because of the large numbers of the required BSs. In applications where BSs are not easily accessible, the reduction in maintenance requirements leads to major operational cost savings. Smaller BSs also lead to reduced environmental impact.

2.1.2.5 Reduced power consumption

Reduced power consumption is a consequence of having simple BSs with reduced equipment. Most of the complex equipment is kept at the centralised CS. In some applications, the BSs are operated in passive mode. Reduced power consumption at the BS is significant considering that BSs are sometimes placed in remote locations not fed by the power grid.

2.1.2.6 Multi-operator and multi-service operation

RoF offers system operational flexibility. Depending on the microwave generation technique, the RoF distribution system can be made signal-format transparent. For instance, the intensity modulation and direct detection technique can be made to operate as a linear system and therefore as a transparent system. This can be achieved by using low dispersion fibre (Single-Mode Fiber), in combination with pre-modulated RF subcarriers (Subcarrier Multiplexing). In that case, the same RoF network can be used to distribute multi-operator and multi-service traffic, resulting in huge economic savings.

2.1.2.7 Dynamic allocation of resources

Since the switching, modulation, and other RF functions are performed at a CS, it is possible to allocate capacity dynamically. For instance in an RoF distribution system for GSM (Global System for Mobile Communications) traffic, more capacity can be allocated to an area (e.g. shopping mall) during peak times and then re-allocated to other areas when offpeak (e.g. to populated residential areas in the evenings). This can be achieved by allocating optical wavelengths through Wavelength Division Multiplexing as need arises. Having the CS facilitates the consolidation of other signal processing functions such as mobility functions, and macro diversity transmission.

2.1.3 Disadvantages

Since RoF involves analogue modulation, and detection of light, it is fundamentally an analogue transmission system. Therefore, signal impairments such as noise and distortion, which are important in analogue communication systems, are important in RoF systems as well because these limitations reduce the capacity of optical transmissions.

In Single Mode Fibre (SMF) based RoF systems, chromatic dispersion may limit the fibre link lengths and may also cause phase de-correlation leading to increased RF carrier phase noise.

In Multi-Mode Fibre based RoF systems, modal dispersion severely limits the available link bandwidth and distance. It must be stated that although the RoF transmission system itself is analogue, the radio system being distributed need not be analogue as well, but it may be digital (e.g. WLAN (Wireless Local Area Network)), using comprehensive multi-level signal modulation formats such as OFDM [7].

The limitations of optical components are a problem as well. The optical fiber, introduces dispersion in optical signals, which leads to enlargement of the pulses. This enlargement can result in an overlap of neighboring pulses resulting in an inter-symbol interference. In optical fibers exists nonlinear effects which generate unwanted signals causing interference with the transmitted signals. There are other limitations due to noise introduced by the optical source [8].

2.2 Orthogonal Frequency Division Multiplex

2.2.1 Introduction

In 1966, R. W. Chang published in [9] the first approach to OFDM. He presents a principle for transmitting messages simultaneously through a linear bandlimited channel without InterChannel Interference (ICI) and InterSymbol Interference (ISI). After that, Saltzberg [10] performed an analysis based on Chang's work and he conclude that the focus to design a multichannel transmission must concentrate on reducing crosstalk between adjacent channels rather than on perfecting the individual signal. An important contribution to OFDM was presented in 1971 by Weinstein and Elbert [11], who used Discrete Fourier Transform (DFT) to perform baseband modulation/demodulation. To combat ISI and ICI they used both guard space between the symbols. But this system did not obtain perfect orthogonality between sub carriers over a dispersive channel. So, in

1980 another important contribution was due to Peled and Ruiz [12], who introduced the cyclic prefix, solving the orthogonality problem. Instead of using an empty guard space, they filled the guard space with a cyclic extension of the OFDM symbol.

The basic idea of OFDM is to divide the available spectrum in a number of narrowband and low-rate orthogonal subcarriers, making it a particular case of a multi-carrier modulation scheme like conventional frequency division multiplexing (FDM). This allows the information to be separated in lower rate sub-streams and to be transmitted in different subcarriers.

The main difference between OFDM and FDM is that while in FDM the transmitting data is modulated in a single carrier, in OFDM the data is transmitted in parallel in several subcarriers where the data rate for each one is inversely proportional to the number of subcarriers used for transmission. This subcarriers are overlapped because they are orthogonal to each other and thus there is no interference between the subcarriers reducing the needed spectrum up to 50%.

The orthogonal characteristic of the subcarriers is achieved by selecting a group of frequencies that are orthogonal, from a mathematical point of view. This property allows the spectrum of each subcarrier to overlap the others without interfering with them, providing a high spectral efficiency. So, orthogonality ensures a complete elimination of crosstalk between subcarriers.

The OFDM system technique is based in digital technology, using the DFT to move the signal to the frequency domain and the Inverse Discret Fourier Transfrom (IDFT) to move back the signal to the time domain without losing any original information. Since FFT (Fast Fourier Transform) algorithm are more cost effective to implement, it is usually used instead of DFT [13].

2.2.2 Transmitter system

As it was introduced above, the basic idea of the OFDM transmission technique is to split the total available bandwidth into many narrowband sub-channels at equidistant frequencies. This is done by the transmitter (see figure 2.3) which has the following functional blocks [14]:

- Demultiplexer, which converts the incoming serial data stream into parallel form.
- Constellation encoder, which maps the parallel data into N/2 multibit subchannels with each subchannel being represented by a QAM (Quadrature Amplitude Modulation) signal constellation.
- IDFT, which transforms the frequency-domain parallel data at the constellation encoder output into parallel time-domain data. For efficient implementation of the IDFT using the FFT algorithm, it is necessary to choose $N = 2^k$ where k is a positive integer.
- Parallel-to-serial converter, which converts the parallel time-domain data into serial form. Guard intervals stuffed with cyclic prefixes are inserted into the serial data on a periodic basis.
- Digital-to-analog converter (DAC), which converts the digital data into analog form ready for transmission over the channel.

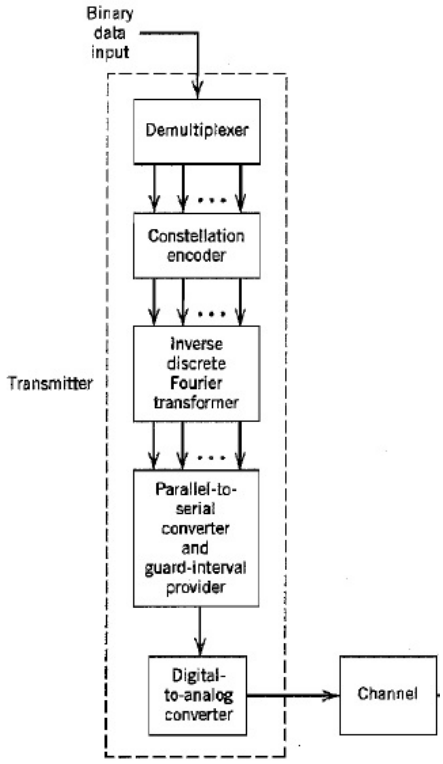


Figure 2.3: Block diagram of an OFDM data-transmission system (from [14]).

2.2.3 Mathematical description

An OFDM transmit signal consists of N adjacent and orthogonal subcarriers spaced by the frequency distance Δf. All subcarrier signals are mutually orthogonal within the symbol duration of length T, if the subcarrier distance and the symbol duration are chosen such that $T = 1/\Delta f$. On each subcarrier, the symbol duration T is N times as large as in the case of a single carrier transmission system covering the same bandwidth. For OFDM-based systems, the symbol duration T must be much larger than the maximum multipath delay $\tau_{(max)}$. In a mathematical approach, it is equivalent to express an OFDM signal as a sum of orthogonal time-limited subcarriers, $g_k(t)$ (see equation 2.2), that are shifted in time and frequency and then multiplied by data symbols. A continuous-time model for OFDM is given by

$$s(t) \quad = \quad \Re\{\tilde{s}(t)e^{j2\pi f_0 t}\} \tag{2.1}$$

where the $\tilde{s}(t)$ represent the baseband signal and f_0 is the frequency of the first subcarrier of the band-pass signal $s(t)$.

On the transmitter side, each subcarrier signal is modulated independently and individually by the complex valued modulation symbol $S_{n,k}$, where n refers to the time interval and k to the subcarrier signal number in the OFDM symbol. Thus, within the symbol duration time interval T the

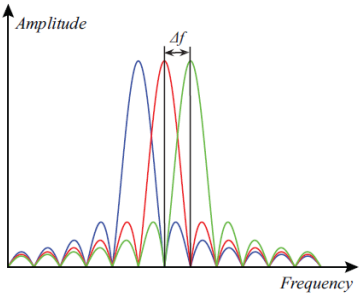


Figure 2.4: Frequency-domain representation (from [16]).

time-continuous signal of n-th OFDM symbol is formed by a superposition of all N simultaneously modulated subcarriers signals [15].

The equivalent baseband OFDM signal in time slot k, transmitted in consecutive symbol intervals can be written as

$$\tilde{s}_n(t) = \sum_{n=0}^{N-1} S_{n,k} g_k(t - nT) \tag{2.2}$$

Since the equation 2.2 can be used to represent any real-valued energy symbol vector and not just OFDM signals, the baseband subcarrier,$g_k(t)$ which satisfy the orthonormal requirement of OFDM signal, are described by a time-limited complex valued exponential function with carrier frequency equal to $k\Delta f$ and given by

$$g_k(t) = \begin{cases} \frac{1}{\sqrt{T}} e^{j\pi k \Delta f_t}, & \forall_t \in [0,T] \\ 0, & otherwise \end{cases} \tag{2.3}$$

As a result of application of the rectangular impulse $\frac{1}{\sqrt{T}}$ (see equation 2.3), each subcarrier spectrum has a cardinal sine shape with the peak of its main lobe at the center frequency and side lobes with nulls periodically spaced by the inverse of OFDM signal period. As shown in figure 2.4 the frequency-domain representation of the signal consists of N adjacent sinc-functions, which are shifted by Δf in the frequency direction for the k-th subcarrier signal. The spectrum is described by

$$G_k(f) = T \cdot sinc[\pi T(f - k\Delta f)] \tag{2.4}$$

In practical applications with high data rates and also a high number of subcarriers, the OFDM transmit signal $s_n(t)$ is generated as a time-discrete signal in the digital baseband, then is sampled with the sampling interval $\Delta t = 1/B = 1/N\Delta f$. So, the k-th sampled equivalent baseband OFDM signal can be given by

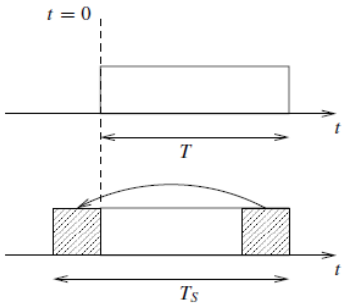


Figure 2.5: Introducing the cyclic prefix (from [17]).

$$s_n(kT + i\Delta t) \quad = \quad s_n(kT + iT/N) = \frac{1}{\sqrt{T}} \sum_{k=0}^{N-1} S_{n,k} e^{j2\pi k \frac{i}{N}} = \frac{1}{\sqrt{T}} s_{n,i}, \tag{2.5}$$

where

$$s_{n,i} \quad = \quad \frac{1}{N} \sum_{k=0}^{N-1} S_{n,k} e^{j2\pi k \frac{i}{N}} = IDFT\{S_{n,k}\} \tag{2.6}$$

Equation 2.6 exactly describes the IDFT applied to the complex valued modulation symbols $S_{n,k}$ of all subcarrier signals inside a single OFDM symbol. This means that, for each time interval of length T, OFDM is just a Fourier synthesis for that period. The perfectly synchronized receiver just performs a Fourier analysis to recover the data symbols from the signal.

2.2.3.1 Cyclic prefix

As can be seen in figure 2.3, after performing the IDFT a cyclic prefix (CP) is added. By doing this, the symbol will be cyclically extended from the original harmonic of the same frequency and phase, but of duration $T_S = T + T_{CP}$. As depicted in figure 2.5, this operation consists in copying the last part of the OFDM symbol and adding it to its beginning.

From a mathematical point of view, the baseband subcarrier, $g_k(t)$, is now given by

$$g_k(t) = \begin{cases} \frac{1}{\sqrt{T}} e^{j\pi k \Delta f_t}, & \forall_t \in [-T_{CP}, T] \\ 0, & otherwise \end{cases} \tag{2.7}$$

and the transmit signal is

$$\tilde{s}_n(t) \quad = \quad \sum_{n=0}^{N-1} S_{n,k} g_k(t - nT_S) \tag{2.8}$$

2.2.4 Channel estimation

The coherent or synchronized transmission is implemented in most wireless systems. For coherent detection of the transmitted signal, the channel must be known or estimated at the receiver. OFDM channel estimation techniques can be either blind or non-blind. While the former is not so much attractive since it mostly exploits the statistical properties of the channel and require a large amount of data, the later is the most commonly used. Blind techniques does not require the use of training sequences or pilot symbols, allowing a more efficient use of available bandwidth. The channel estimation is achieved using statistical properties of the received data that are acquired over specific time intervals. In the non-blind techniques, spaced pilot symbols are inserted to enhance the accuracy of blind estimation. This is known as semi-blind estimation of the channel that allows small variations in the channel. For this reason, the transmission with pilots is used in most wireless transmission systems. Due to the OFDM two-dimensional structure, the estimation procedures can be performed using a set of known training symbols that can be assigned to both time and/or frequency domain. These set of symbols are inserted at specific subcarrier indexes also known as pilot subcarriers and are used to enable channel estimation. Figure 2.6 depicts the two most common pilot schemes used. Pilot subcarriers can be inserted either in a block scheme where all (or at least the majority of the) subcarriers of a given OFDM symbol are used as pilots (right in the figure), or in a comb scheme where pilots are inserted in all OFDM symbols but only at specific indexes (left in the figure). The block-type domain scheme assumes that the channel is slow varying and thus the channel estimative is valid for a given number of consecutive OFDM symbols. This is done by inserting pilots on all subcarriers of the OFDM symbols with a specific period. On the other hand, the comb-type is mainly considered for transmissions where the channel varies significantly between two consecutive OFDM symbols. Since only some of the subcarriers are used as pilots, the channel estimate at others frequencies must be obtained using interpolation operations [18].

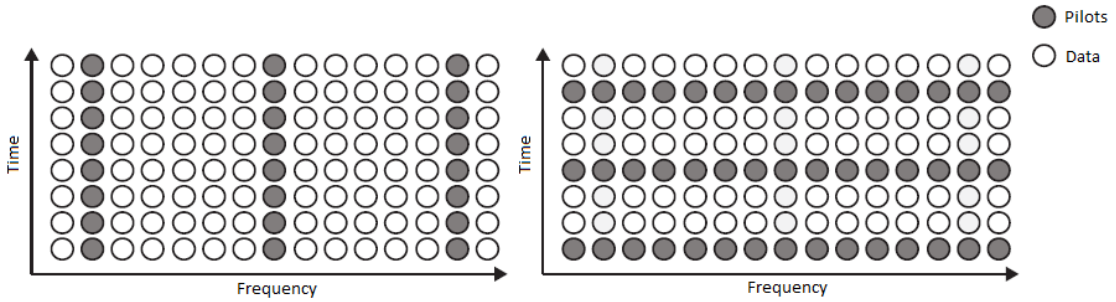


Figure 2.6: Representation of comb-type (left) and block-type (right) pilot subcarrier arrangements (from [18]).

2.3 Digital Radio over Fiber

RoF links where an optical carrier is modulated by (multiple) analog radio signals, known as analog radio-over-fiber, inherently suffer from inter-modulation distortion (IMD) arising from the nonlinearities incurred in both RF and optical components. Digitized radio-over-fiber transport schemes are being pointed as viable alternative solutions to their analog counterparts, in order to avoid distortion/dynamic range problems. In [6], the authors proposed a novel D-RoF architecture that takes advantage of a band-pass sigma-delta modulator at the transmitter which subsequently permits the usage of a simpler/cheaper base station that avoids the employment of a digital to analog converter. The proposed architecture exploits the properties of the digital signal to enable the extraction of an higher carrier frequency through the employment of a band-pass filter.

In figure 2.7 a typical D-RoF scheme is depicted.

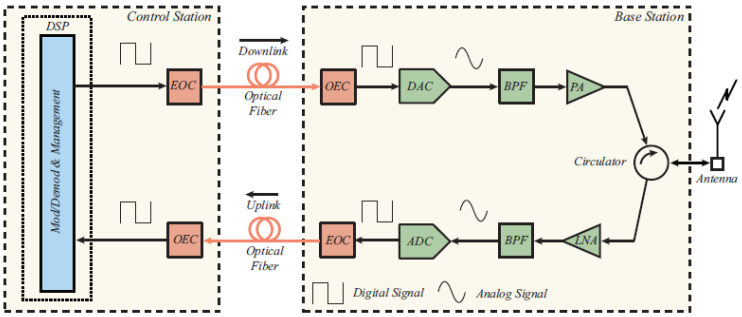


Figure 2.7: Diagram of a standard D-RoF architecture (from [6]).

D-RoF requires the usage of high bandwidth Analog-to-Digital converters at the transmit side and Digital-to-Analog converters at the receive side. Contrary to analog systems, by employing D-RoF the IMD is avoided and the dynamic range of the system remains constant and irrespective of the optical fiber length, provided that the received signal amplitude is above the sensitivity of the link [19]. Band-pass sampling is used in D-RoF schemes to lower the sampling rate requirements since most common wireless standards (e.g.,WiMAX, WiFi, 3G, 4G) have small fractional bandwidths relative to their carrier frequencies [20]. Optical links employing digitized transport of RF signals with both CS and BSs having digital interfaces open the possibility of designing backhaul networks seamlessly integrated with both existing and future broadband optical networks [21].

The solution proposed by the authors is based on the usage of a band-pass sigma-delta modulator at the transmitter side, working as a 1-bit ADC. The proposed digital transmission solution combines advantages of both digital and analog schemes. In the downlink the RF signal is digitized and transported over the optical fiber as a stream of bits, which, provides advantages in terms of IMD and dynamic range. However, contrarily to traditional D-RoF schemes, at the BS tha DAC is avoided, decreasing the BS's cost and complexity and power consumption. By using a SDM as ADC, the DAC at the BS can be suppressed since its equivalent operation is performed by means of a simple band-pass filter (BPF).

Figure 2.8 shows the scheme proposed by the authors. The downlink architecture is comprised of a completely digital transmitter at the CS that takes advantage of the digital signal processing implementation of a SDM to convert the digital representation of the analog wireless signal into a NRZ (Non Return to Zero) bit stream. At the CS, all of the analog blocks such as up/down frequency converters and mixers can be implemented in the digital domain jointly with the SDM block in a single platform. Then at the BS, a photodiode (PD) acts as an optical to electrical converter (OEC), followed by a band-pass filter tuned to the RF signal center frequency, then by an RF power amplifier (PA), and finally by an RF circulator and RF antenna.

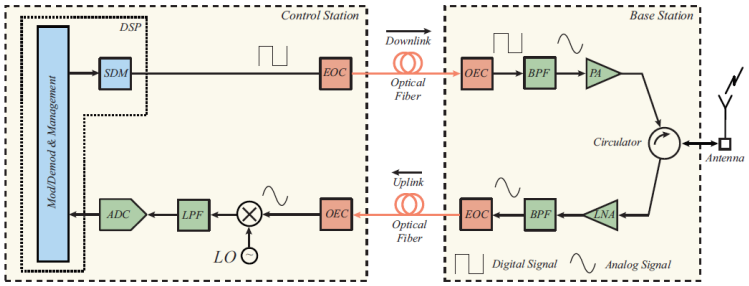


Figure 2.8: Diagram of the SDM based D-RoF architecture (from [6]).

Figure 2.9 depicts the normalized power spectrum obtained at the output of the band-pass SDM. Due the nature of the NRZ line code given by the Zero Order Hold (ZOH) and the sampling process, the spectrum of the digital signal repeats every f_s, where f_s stands for the sampling frequency of the 1-bit ADC of the band-pass SDM, generating high frequency replicas of the original RF signal. The bitrate of the SDM is then given by $R_b = f_s \times bit$, enabling the transmission of sub-Gbps digital streams from which RF signals centered at the Gigahertz frequency region can be obtained with no additional frequency up-conversion hardware at the BS. Figure 2.9 clearly shows the original RF signal (f_{c0}) at $f_s/4$, as well as two high frequency replicas f_{c1} and f_{c2} at $f_{c0}+f_{c0}$ and $2f_{c0}+f_{c0}$, respectively, as well as their image frequency components.

Another advantage of this SDM based D-RoF downlink architecture proposed by the authors is that it allows the transmission of both traditional analog as well as the sigma-delta modulated signals over the same network since the hardware at BSs is simultaneously compatible with both approaches. Therefore, currently installed A-RoF deployments could be migrated to the sigma-delta based D-RoF architecture without replacing BSs, while only the downlink path of the control station would need to be upgraded. On the contrary, the transition to a traditional D-RoF architecture would require the upgrading all of BSs. Furthermore, as for future deployments targeting all-digital networks, the proposed SDM based D-RoF architecture by the authors could be readily employed, with the advantage of avoiding the employment of the DAC in BSs [6].

2.3.1 Sigma-Delta Modulator

The sigma-delta modulator lays in the group of modulators that use oversampling and a feed-back loop to reduce the noise in the band of interest [22]. Additionally, the quantization noise spectrum

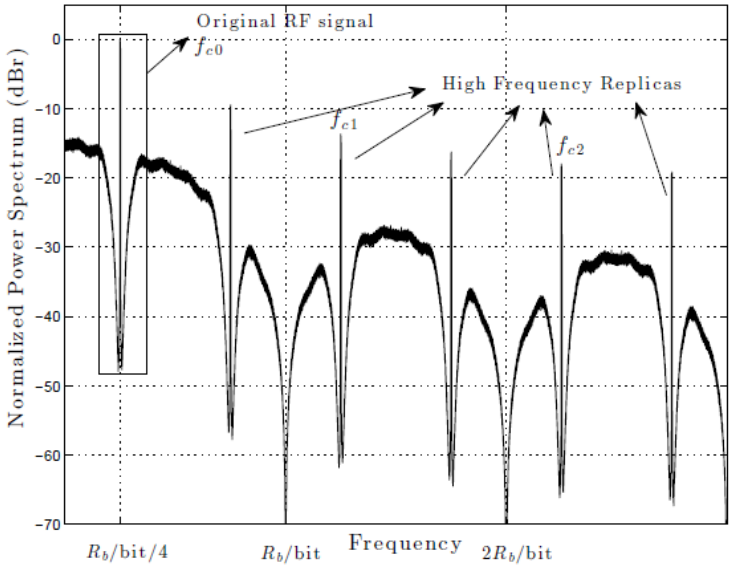


Figure 2.9: Normalized power spectrum obtained at the output of the band-pass SDM (from [6]).

is shaped and high signal-to-noise ratio (SNR) values in the band of interest may be achieved. Figure 2.10 represents a generic block diagram of the low-pass first order sigma-delta modulator. The modulator consist of a loop-filter composed by an integrator, a quantizer and a DAC in the feedback path. The signal and noise transfer functions (STF and NTF) are given by, respectively;

$$STF(z) = 1 \tag{2.9}$$

$$NTF(z) = 1 - z^{-1} \tag{2.10}$$

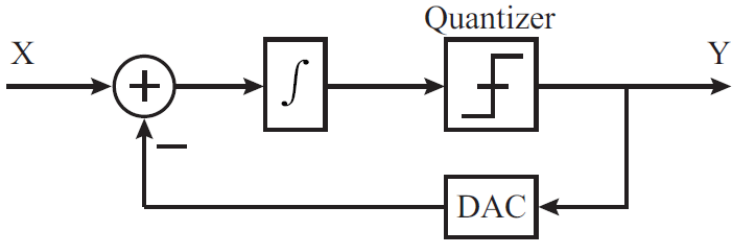


Figure 2.10: SDM block diagram (from [6]).

While $STF(z)$ is equal to the unity, the magnitude of $NTF(z)$ is actually shaped by a high-pass filter.

For low-pass structures like in figure 2.10, it is considered that $f_{max} \ll f_s$ and $OSR = f_s/(2f_{max})$, where OSR represents the oversampling rate, f_{max} the maximum frequency of the signal and f_s the

sampling frequency.

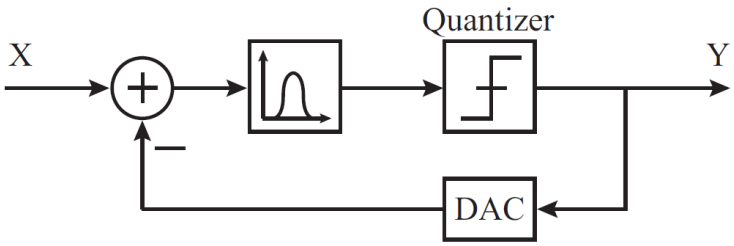


Figure 2.11: Equivalent band-pass SDM linear model (from [6]).

With minor changes, the SDM structure presented above can be applied to RF band-pass signals having $f_{max}/f_s \gg 1$ [23]. In fact, the high-pass characteristic of the noise shaping function can be transformed into a stop-band function with zeros located at the center frequency of the input signal. Moreover, the OSR only depends on the signal bandwidth, being given by $OSR = f_s/(2BW)$, BW being the two-side bandwidth of the RF signal, while for the low-pass structure the BW term is replaced by f_{max}. The NTF filter characteristic can be obtained by designing a band-pass filter with zeros away from DC instead of the integrator used in the low-pass version (see figure 2.11). This is done by substituting $z \rightarrow -z^2$. So, a band-pass NTF with zeros at $f_c = f_s/4$ is obtained (see figures 2.12 and 2.13). By placing the signal carrier frequency at $f_s/4$ the sampling frequency is automatically dictated.

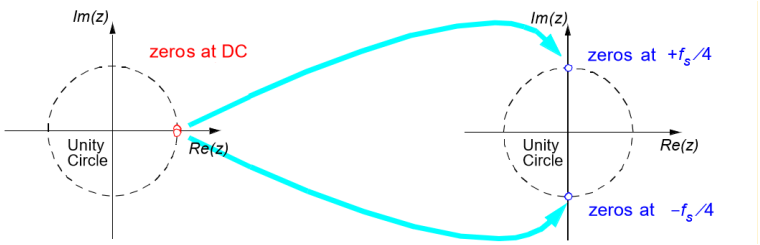


Figure 2.12: The low-pass-to-band-pass transformation (from [24]).

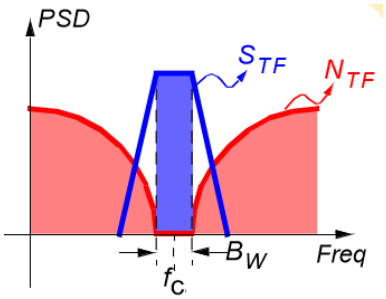


Figure 2.13: NTF and STF spectrum (from [24]).

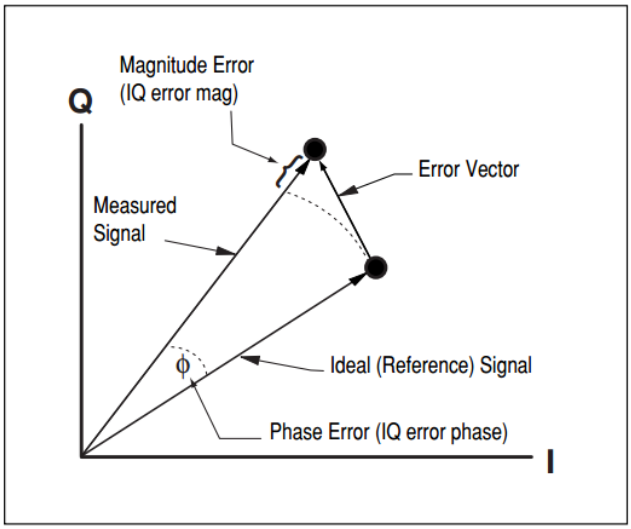


Figure 2.14: EVM and related qualities (from [26]).

2.4 System Performance

2.4.1 Error Vector Magnitude

The Error Vector Magnitude (EVM), is a measure used for quantifying the performance of a digital radio transmitter or receiver. A signal sent by an ideal transmitter or acquired by and ideal receiver would have all constellation points placed at their ideal locations. However, various imperfections in the implementation (such as carrier leakage, low image rejection ratio, phase noise and more) cause the actual constellation points to deviate from such ideal locations. An error vector is a vector in the I-Q plane between the ideal constellation point and the point received by the receiver, In other words, it is the difference between actual received symbols and ideal symbols (see figure 2.14). The EVM is equal to the ratio of the power of the error vector to the power of the reference. It is defined in decibels as:

$$EVM[dB] = 10\log_{10}\left(\frac{P_{error\ vector}}{P_{reference}}\right) \tag{2.11}$$

where $P_{error\ vector}$ is the root mean square (RMS) power of the error vector and $P_{reference}$ denotes the corresponding RMS power of the reference signal. For multi-carrier modulations like OFDM, $P_{reference}$ is, defined as the reference constellation average power [25].

2.5 Related work

The design and implementation of OFDM-based wireless communication system has been studied for many years. Most of the works have been focusing on specific areas of the implementation of

OFDM system using FPGA.

J.Garcia and R.Cumplido in [27] presented a FPGA design,validation and implementation of OFDM modulator for IEEE 802.11a. Xilinx System Generator which runs under Matlab Simulink was used in this project. This is a high-level design tool that provides a visual modeling and allows a high level abstraction of the system. Not only design was performed by System Generator but verification and finally targeting to a specific FPGA. This work divides the design into functional subsystems, such as, QAM mapping, pilot generator, inter-leaver which mix all sources (mapped data and pilots), IFFT and prefix adding. This design uses an 80 MHz for the main clock which is down-sampled to obtain a 16 MHz, used before IFFT block and 20 MHz after IFFT block. All bocks use a 16-bits signed fixed point representation. This work was synthesized for a Virtex XCV300 with the following results: 2367 flip flops, 2500 LUTs and 12 block RAMs. Finally, the authors concluded that this work employs less area resources than others OFDM implementations presented in others papers.

In [28], the authors implemented the OFDM transmitter in Matlab followed by Verilog HDL using both Simulink and Xilinx System Generator. In this work to generate the input source the authors used a Bernoulli binary generator which generates random binary numbers using a Bernoulli distribution. After that, a serial-to-parallel converter is used to convert groups of samples into single sample as bits, then a QPSK (Quadrature Phase Shift Keying) modulation is performed. In the end, the IFFT converts the signal from frequency domain to time domain. The Xilinx Intellectual Property Core FFT v7.1 was used to perform the IFFT. The authors conclude that the system hardware interface circuit is simple, convenient and efficient. The results from software simulation and hardware results of Xilinx blocks are compared and both are verified in Xilinx Spartan3E FPGA.

The design and performance evaluation of an OFDM transmitter, implemented on a FPGA platform for applications on a wireless wave radio system are presented in [29]. The transmitter is described in order by the blocks: LFSR (Linear feedback shift register), serial-to-parallel, 16-QAM mapping, IFFT. The LFSR block is used to generate the input data stream. The input bits stream are grouped into parallel by the serial-to-parallel block in order to be mapped into 16-QAM constellation. The Xilinx Intellectual Property Core FFT v7.0 was used to perform a 64-point (number of subcarriers employed) IFFT. The authors used System Generator and the implementation of the OFDM system was performed on Virtex-4 with a maximum frequency of 228 MHz. In this work a comparison between the floating point simulation of the OFDM by using Matlab Simulink and the 16-bits fixed point Xilinx block-set was performed. The results obtained by the authors from both simulations are very similar. The floating point performs slightly better than fixed point, this is the result of the limited 16-bits word length compared to 64-bits floating point.

In [6], a novel D-RoF architecture that takes advantage of a band-pass SDM at the transmitter was proposed. The details of the architecture was already presented in section 2.3. The experimental setup that the authors used to evaluate the system is in figure 2.15. The RF signal is generated at a digital signal processor emulated by a PC running Matlab, corresponding to the vector signal

generator (VSG) block. The authors used a pulse pattern generator (PPG) to directly modulate the VCSEL. After passing through the optical fiber, the bitstream is converted into the electrical domain by means of a photodiode. Then, the signal is sampled by an oscilloscope (DSO) running a vector signal analysis (VSA). For a 16-QAM signal centered at the fundamental frequency (250 MHz), a peak-to-peak input voltage equal to 200 mV, a bias current (I_b) equal to 7.5 mA the best result that the authors obtained was 47 dB using the Modulation Error Ratio (MER) performance metric. The authors concluded that, while performing similarly to conventional D-RoF schemes, the proposed architecture is economically competitive for either upgrading installed systems as well as for new deployments.

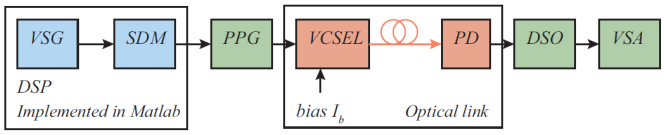


Figure 2.15: Experimental setup (from [6]).

Chapter 3

System Design

This chapter starts with the components used in this project. After that, a high-level perspective of the Verilog project created in Xilinx Vivado is presented. A general description of an OFDM system made with Xilinx System Generated to create an OFDM waveform with the fundamental frequency located at 250 MHz is also presented. At last, the modifications that where made in the model to change the fundamental frequency to 2.5 GHz are described.

3.1 System Components

The FPGA used in this project is the Xilinx Virtex-7 XC7VX485T-3FFG1761E. A brief characterization of the XC7VX485T FPGA is in figure 3.1. This FPGA provides a large number of DSP slices, Block RAM blocks and GTX transceivers which are necessary for the implementation of the design. GTX transceivers are important in this project, because with these is possible to achieve high data output rates, so the number of GTX transceivers is not so relevant in this case.

Device[1]	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[3]	Block RAM Blocks[4]			CMTs [5]	PCIe [6]	GTX	GTH	GTZ	XADC Blocks	Total I/O Banks[7]	Max User I/O[8]	SLRs[9]
		Slices[2]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)									
XC7VX485T	485,760	75,900	8,175	2,800	2,060	1,030	37,080	14	4	56	0	0	1	14	700	N/A

Notes:
1. EasyPath™-7 FPGAs are also available to provide a fast, simple, and risk-free solution for cost reducing Virtex-7 T and Virtex-7 XT FPGA designs
2. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
3. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
4. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
5. Each CMT contains one MMCM and one PLL.
6. Virtex-7 T FPGA Interface Blocks for PCI Express support up to x8 Gen 2. Virtex-7 XT and Virtex-7 HT Interface Blocks for PCI Express support up to x8 Gen 3, with the exception of the XC7VX485T device, which supports x8 Gen 2.
7. Does not include configuration Bank 0.
8. This number does not include GTX, GTH, or GTZ transceivers.
9. Super logic regions (SLRs) are the constituent parts of FPGAs that use SSI technology. Virtex-7 HT devices use SSI technology to connect SLRs with 28.05 Gb/s transceivers.

Figure 3.1: XC7VX485T FPGA (from [30]).

The VC7203 was the board used in this project and his block diagram is shown in figure 3.2. This board provides many features to the user, some of them are used in this project and presented in this chapter. For transmission of information was used one of the nine Samtec BullsEye connector pad, a cable with a BullsEye connector and 10 standard SMAs (see figure 3.3). For clocking was used the 200 MHz 2.5 V LVDS (Low-Voltage Differential Signaling) oscillator and the SuperClock-2 module that supports multiple frequencies.

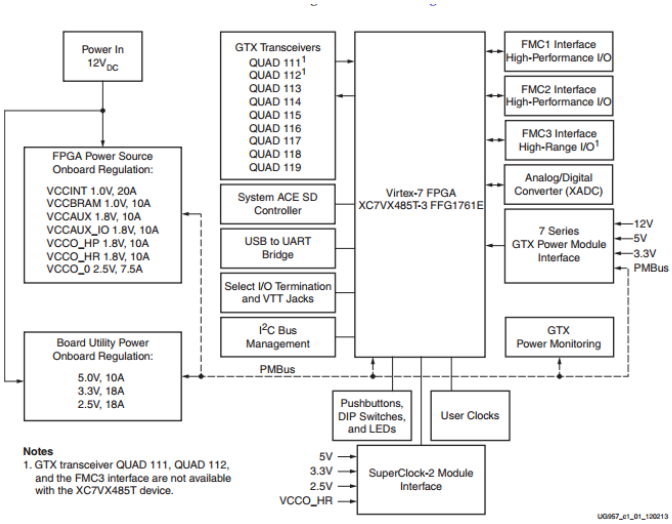
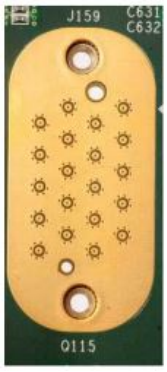


Figure 3.2: VC7203 board block diagram (from [31]).

The main feature used in this project was the GTX Transceivers of the FPGA, these are described in the next subsection.

(a)



(b)

(c)

Figure 3.3: VC7203 board (a), GTX connector pad (b) and cable with a BullsEye connector and 10 standard SMAs (c).

3.1.1 GTX transceivers

The 7 series FPGAs GTX transceivers are power-efficient transceivers, supporting line rates from 500 Mbps to 12.5 Gbps. The GTX transceiver is highly configurable and tightly integrated with the programmable logic resources of the FPGA. Some of the configurable parameters are the line rate, the reference clock, the peak-to-peak differential voltage and the encoding type of the transmitted bits.

The GTX transceivers provide different reference clock input options. For this project this reference clock is provided by the SuperClock-2 module interface, which provides a programmable, low-noise and low-jitter clock source for the board.

Like other SerDes (Serializer/Deserializer), the primary function of the GTX transceivers is to transmit parallel data as stream of serial bits, and convert the serial bits it receives to parallel data. In this project only the transmitter side is used, so the focus of this section is in the transmitter of the GTX transceivers. The most basic performance metric of an GTX transceiver is its serial bit rate, or line rate, which is the number of serial bits it can transmit or receive per second. Although there is no strict rule, GTX transceivers can typically run at line rates of 1 Gbps or more. GTX transceivers have become the "data highways" for data processing systems that demand high raw data input and output. They are becoming very common in FPGAs, such programmable logic devices being especially well fitted for parallel data processing algorithms. Beyond serialization and deserialization, GTX transceivers must incorporate a number of additional technologies to allow them to operate at high line rates [32]. Some of these technologies like differential signalling and Mixed-Mode Clock Manager (MMCM) are used in this project. Differential signalling allows faster switching, because the change in signal level required to switch from 1 to 0 or 0 to 1 is halved. To serialize data at high speeds, the serial clock rate must be an exact multiple of the clock for the parallel data. For this, the MMCM is used to multiply a reference clock running at the desired parallel rate to the required serial rate.

The basic structure of the relation between the design implemented and the GTX transceivers are demonstrated in figure 3.4. The figure demonstrates that the GTX transceiver provides the reference clock (TX_USR_CLK) for the design and the design sends to the GTX transceivers the data that wants to transmit (TX_DATA).

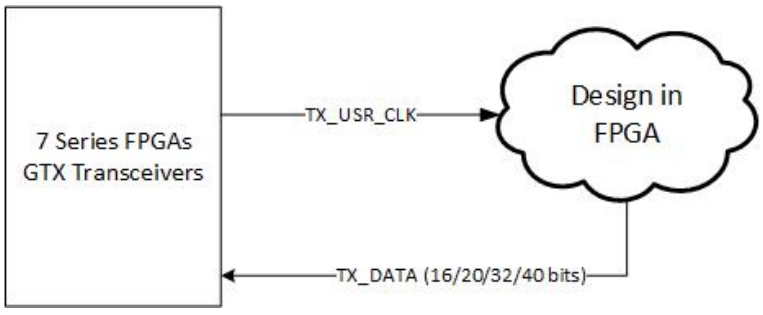


Figure 3.4: Relation between the design implemented and the GTX transceivers.

The "7Series FPGAs GTX Transceivers" block presented in the figure above is composed by

several GTX Quads. In this project only one Quad was used. Architecturally, the concept of a Quad, for this project, contains a grouping of four GTX_CHANNELs, one GTX_COMMON and one dedicated external reference clock pin (see figure 3.5). The GTX_CHANNEL is formed by three essential stages. Data flows from the FPGA logic into the FPGA TX interface to PISO (Parallel-Input-Serial-Output) and then out the TX driver as high-speed serial data.

The GTX_COMMON encapsulates the GTX QPLL (LC-based PLL (Phase-locked loops)). The QPLL output feed the TX clock divider blocks of each serial transceiver channel within the same Quad, which control the generation of serial clock used for transmit data and parallel clock used by design to supply data to the GTX transceivers.

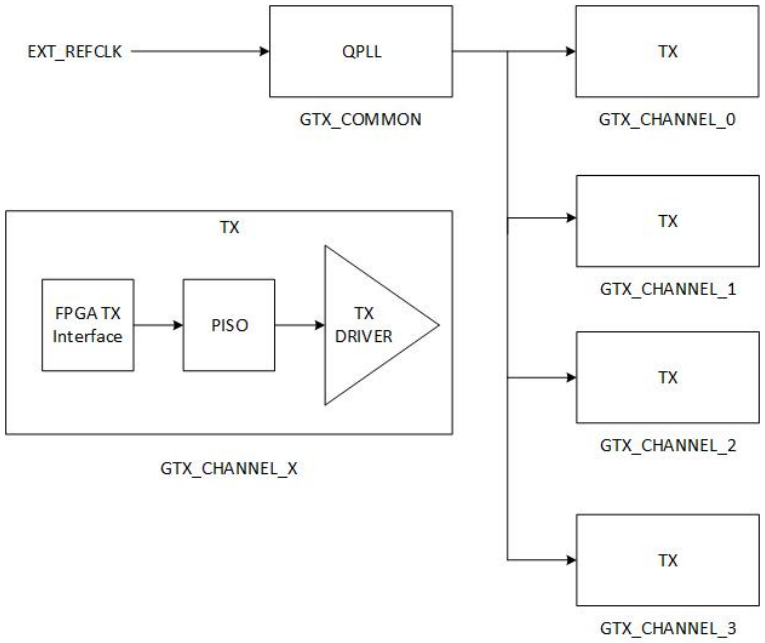


Figure 3.5: GTX Transceiver Quad Configuration.

Each GTX Quad and its associated reference clock are routed from the FPGA to a connector pad which is designed to interface with a Samtec BullsEye connector. A cable with a BullsEye connector and ten standard SMAs provides connection to a broad range of evaluation platforms, from backplanes and optical evaluation boards to high speed test equipment. Each BullsEye connector handles a full GTX Quad, four transmit/receive pairs as well as the two independent reference clocks, enabling the highest level of flexibility in testing custom applications.

3.2 Model synthesis

Figure 3.6 shows, in a simple way, the top-level of this project made in Verilog. This top-level instantiates four modules.

The "OFDM" module is the module created in XSG and imported to Xilinx Vivado. This module performs the creation of the OFDM signal and it is presented in the next section.

The "GTX" module is an IP core from Xilinx configured with help of the "7 Series FPGAs Transceivers Wizard v3.6". This wizard automates the task of configuring one or more high-speed serial transceivers of the Xilinx 7Series FPGAs GTX Transceivers. One of the most important thing that this wizard permits is to select the line rate (Gbps) of the FPGA output.

Two of the inputs of the "GTX" module are "ext_ref_clk_n_in" and "ext_ref_clk_p_in". These inputs are the external differential clock input pin pair for the reference clock of the 7 series FPGA transceiver Quad, more precisely for QPLL. The "tx_usr_clk_out" wire output from this module is the reference clock used for the implemented logic in the "OFDM" module to meet the desired requirements of the chosen line rate. As said before the serial clock rate must be an exact multiple of the clock for the parallel data. For this design the serial clock chosen is 1 GHz. To achieve this requirement, the clock for the parallel data must be 62.5 MHz, because the output of the "OFDM" module is 16-bit. Other input of this module is the "sysclk_in", it is a clock used to drive the FPGA logic in the design. "TX_N_OUT" and "TX_P_OUT" are the differential output pairs for each of the transmitters in the 7 series FPGA transceiver Quad.

Two of the instantiated modules are for clock generation and for them I used the "Clocking Wizard v5.1" from Xilinx's IP core library. This wizard simplifies the creation of the Verilog source code for clock circuits customized to specific clocking requirements. The "CLK" module creates a 125 MHz clock necessary for the correct operation of the "GTX" module. The input and reference clock of this module is the 200 MHz 2.5 V LVDS.

The other module of clock generation is the "CLK_OFDM" module that creates a clock necessary for the "OFDM" module that its value will be explained in section 3.3.3.

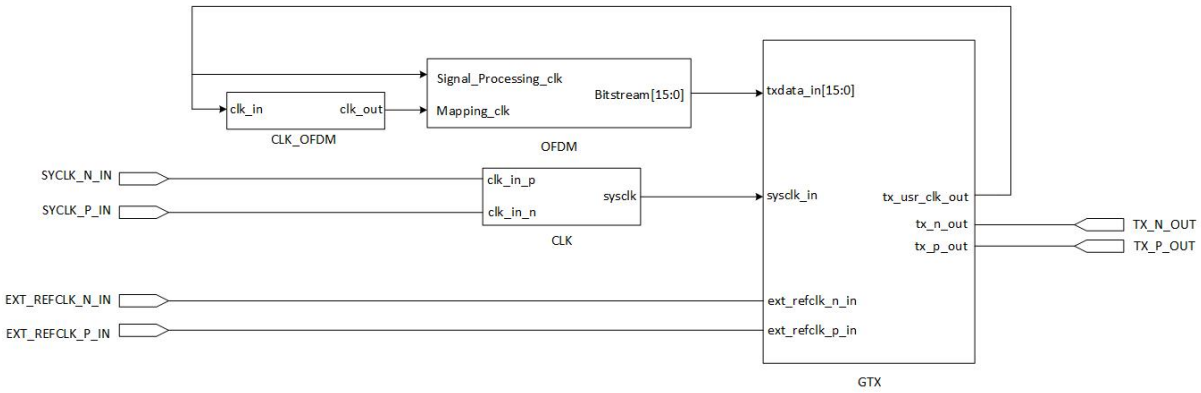


Figure 3.6: Top-level of the Verilog project in Xilinx Vivado.

3.3 Model of OFDM waveform generator

The implementation of the OFDM system starts with the establishment of the fixed point model in XSG. In this model, numbers are represented in signed two's complement form, denoted as "Fix_16_15" . In this representation 16 bits are used, in which the most significant one is the sign bit and the remaining 15 bits represent the fractional part. So, the highest number that can be

represented is 0.99 and the lowest number is -1. A few blocks show different forms due to precision requirements. This fixed-point representation is used in most of the computations including IFFT.

Figure 3.7 shows the two main blocks of the OFDM transmitter. The FIFOs inserted in the middle of the blocks are a restriction imposed by XSG to control data flow between two different clock domains. XSG configure these blocks to be either synchronous single clock blocks or multiple clock blocks based on their context in the design. In this design, the FIFO blocks are used to cross the clock domains. Sixteen is the depth of these FIFOs.

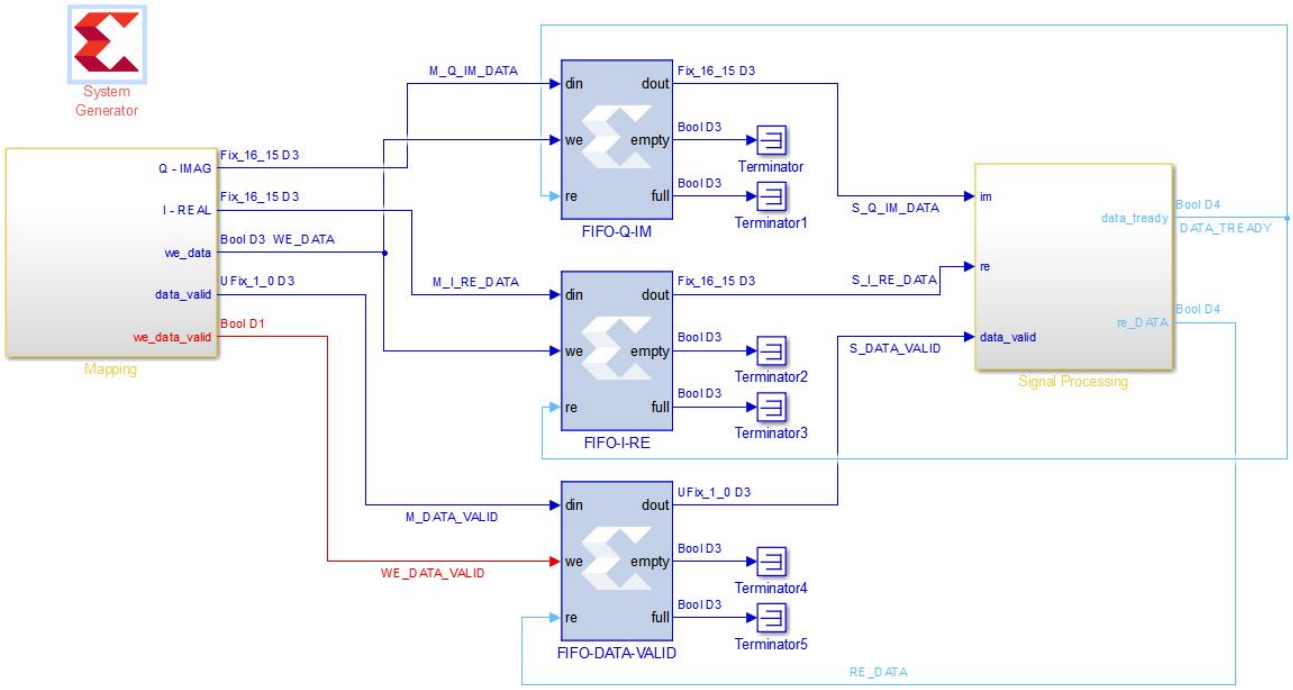


Figure 3.7: Top-level of the OFDM model implemented in XSG.

3.3.1 Mapping block

The first thing that this block does is to create the binary input of the system that simulates information to be transmitted and then modulated by a modulation scheme. As a frequency multiplexing scheme, the data on each subcarrier of OFDM can be modulated with phase difference or/and amplitude of the carrier. QPSK is selected in this design since it can be easily modified to implement more complex modulation schemes, like 16QAM and 64QAM. The QPSK modulation scheme has four phase states separated by $\pi/2$. Therefore, each QPSK symbol carriers two bits of data ($\log_2 4 = 2$). The I and Q values generated by this block are normalized to $1/\sqrt{2}$ in order to achieve the same average power for all mappings. The details of the implemented modulation scheme are shown in Table 3.1.

Table 3.1: QPSK symbol mapping with gray coding

Bit Set	I Value	Q Value	Phase(degree)
11	$1/\sqrt{2}$	$1/\sqrt{2}$	$\pi/4$
01	$-1/\sqrt{2}$	$1/\sqrt{2}$	$3\pi/4$
00	$-1/\sqrt{2}$	$-1/\sqrt{2}$	$-3\pi/4$
10	$1/\sqrt{2}$	$-1/\sqrt{2}$	$-\pi/4$

3.3.2 Signal Processing Block

After the Mapping block, the generated values (I and Q) are fed into the second main block called Signal Processing block.

In this block all the signal processing is done according to the approach demonstrated in chapter 2 to create a D-RoF.

This block can be subdivided in four stages. The first is the "Subcarrier Allocation" where, according to the explanation in subsection 2.2.4, the pilot insertion is done. In this same stage, the "null" insertion is done in the middle subcarrier. This middle subcarrier must always be set to zero (null), to avoid introducing any DC into the base band signal.

The transformation from frequency domain to time domain is the next stage. This is done by a block imported from Xilinx's IP core library, named "Fast Fourier Transform v9.0". It implements the Cooley-Turkey algorithm and for the chosen pipelined architecture, several Radix-2 butterflies and banks of memories are used for each engine, so that the data processing is pipelined and a high throughput is achieved. Thus, the core has the ability to simultaneously perform transform calculations on the current frame of data, load input data for the next frame of data, and unload the results of the previous frame of data. The configuration chosen for this block is the Pipelined Streaming I/O with Cyclic Prefix Insertion where the core computes a 64-point complex IFFT. With cyclic prefix insertion, more samples are taken out from the core than are received. Therefore, the core cannot continuously stream frames, but must insert a gap of cyclic prefix length clock cycles in between each frame of input data to accommodate the additional clock cycles required to send out the cyclic prefix. This block works based on a basic handshake (presented in subsection 4.2.2), thus, it is very simple to take control of the operation of the block.

The next stage is the Digital Up Converter (DUC), that translates the base band signal to a higher frequency band. This is done by first up-sampling the base band signal using the block from Xilinx's IP core library, named "FIR Compiler v7.2". This core provides a common interface to generate highly parameterizable, area-efficient and high-performance FIR filters. After that, the signal modulates a carrier and then pass through the Sigma-Delta modulator block like proposed in [6].

3.3.3 Frequency of the model

The clocks of the Mapping and Signal Processing are related by a ratio of two. This restriction is imposed by the choice of the constellation to map the input data. Since one QPSK symbol contains

two binary bit, the frequency of the Mapping block is twice that of the Signal Processing block. The "GTX" module is the one that determines the frequency of these two blocks. Due to the fact that the serial clock rate is 1 GHz, then the frequency of the Mapping block is 125 MHz, that is twice of the Signal Processing frequency (62.5 MHz).

3.3.4 Modification of the output data rate to 10 Gbps

1 Gbps was the initial requirement for output data rate of this design to have an OFDM signal centered at 250 MHz. A second requirement was to put the line rate to 10 Gbps to have an OFDM signal centered at 2.5 GHz. To achieve a transmission rate of 1 GHz it is necessary to perform a serial to parallel conversion (1 bit to 16 bit) after the Sigma-Delta block and then store these 16-bit words in a RAM (Read-Address-Memory). This procedure was integrated inside the Signal Processing block. So, to change the serial clock from 1 GHz to 10 GHz it is necessary to change the frequency of the two main blocks. To achieve 10 Gbps, the minimum of the parallel input must be 32 bits length and with this the clock of the Signal Processing block must be 312.5 MHz and the clock of the Mapping block must be 625 MHz. These frequencies are too high to meet the timing requirements and the project did not pass in the implementation phase. Then, the decision that was taken was to separate the process of saving the output of the Sigma-Delta block (bitstream) in other clock domain with a frequency that has not to do with the other blocks. Figure 3.8 shows the alterations sequence from the initial design to the 10 Gbps design. The Memory block was transfer (with some changes in the implementation) from Signal Processing block to the top-level of the project. Keeping the frequencies of the main blocks unchanged, this new block works at 250 GHz and the only thing it does is receive the bitstream from the Signal Processing block, perform a serial to parallel conversion from 1 bit to 40 bit and save this in a RAM.

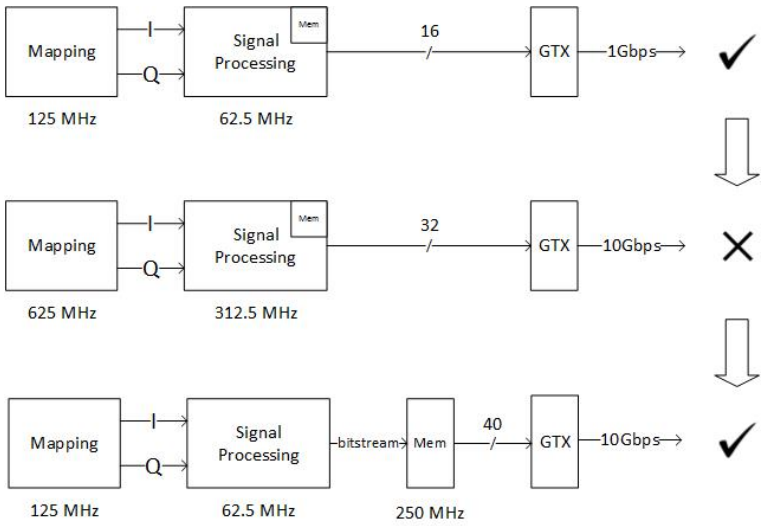


Figure 3.8: Visual description of the modifications in the design.

Chapter 4

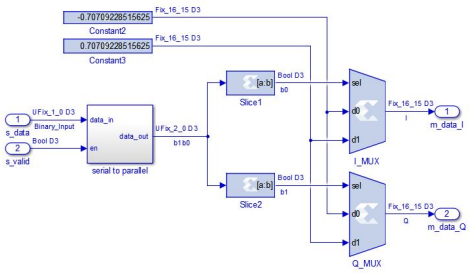
OFDM implementation

This chapter describes in detail the two main blocks presented in the previous chapter. Starting with the Mapping block and followed by the Signal Processing block. They were specified in Xilinx System Generator.

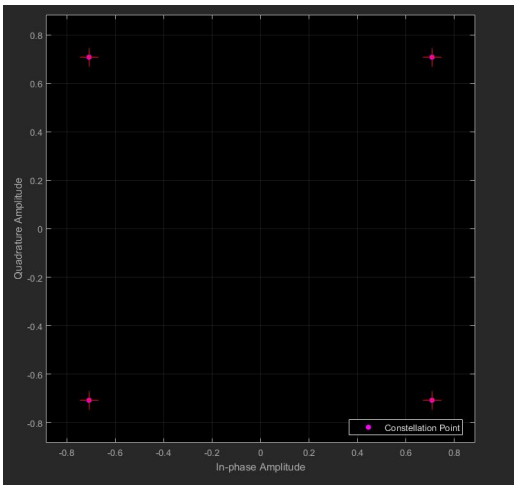
4.1 Mapping Block

4.1.1 QPSK Mapping

To map the binary input to QPSK symbol, the input sequence is first converted to two-bit symbols by serial to parallel conversion. This two-bit are then used as the select signal of two multiplexers. Finally, the output of the two multiplexers are the I and Q values of the desired complex symbol. The implementation module is illustrated in figure 4.1a. Figure 4.1b depicts the constellation diagram for the QPSK gray-coded mapping.



(a)



(b)

Figure 4.1: QPSK Mapping implementation module (a) and constellation diagram (b).

Figure 4.2 illustrates the waveforms of the QPSK mapping. The binary stream is mapped to the two-bit QPSK symbols. The most significant bit of the QPSK symbol controls the in-phase multiplexer while the least significant bit controls the quadrature multiplexer.

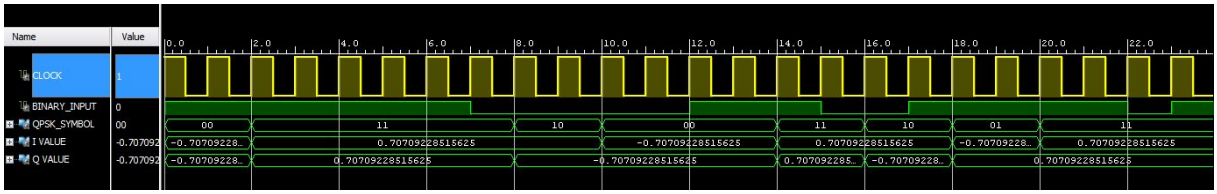


Figure 4.2: Waveforms of the QPSK mapping.

4.2 Signal Processing Block

Figure 4.3 shows the design of the implementation of this block. The "ready" represents the signal that the block uses to indicate that is ready to receive data. The "valid" represents the signal that the block uses to indicate that the output values of the block are valid.

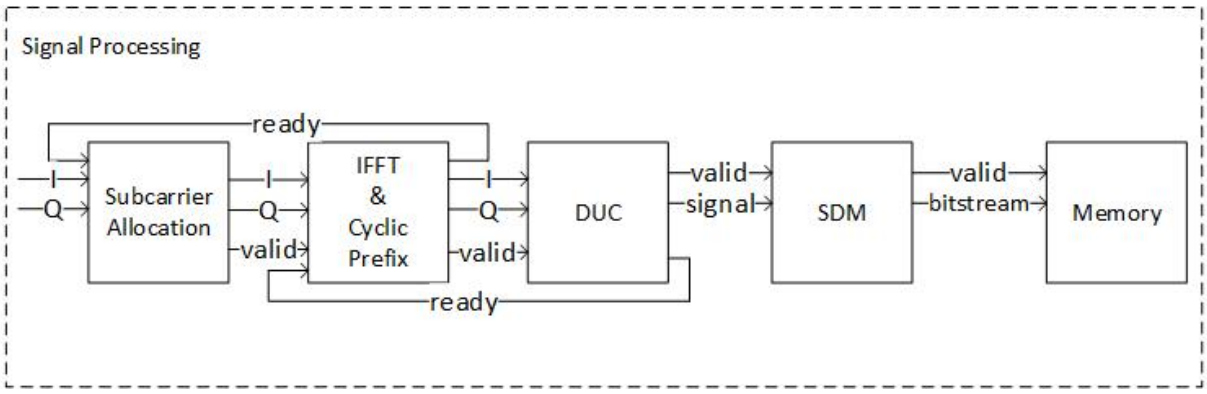


Figure 4.3: Inside of Signal Processing block.

4.2.1 Subcarrier Allocation

As was said in the previous chapter, there are two purposes for designing the Subcarrier Allocation block. The first is to insert the pilot subcarriers among the data, the second is to insert null subcarriers which carry "zero" information. In this project among the 64 subcarriers, 59 are used for carrying data information, 4 are used as pilots and 1 is null. The allocation of the data and pilot subcarriers is shown in figure 4.4, where the pilots are located at the subcarriers 15, 25, 39, 49 and the remaining 59 subcarriers are used for the modulated data symbols. Comb-scheme (presented in section 2.2.4) was the pilot scheme used in this project.

The implementation module is depicted in figure 4.5.

The allocation of the "null" subcarrier and the pilots are controlled by a counter, that counts from 0 to 63 and only starts when the first IQ pair arrives to the subcarrier allocation block. When

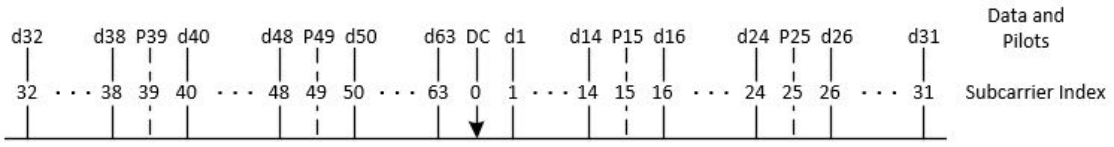


Figure 4.4: Data allocation onto subcarriers.

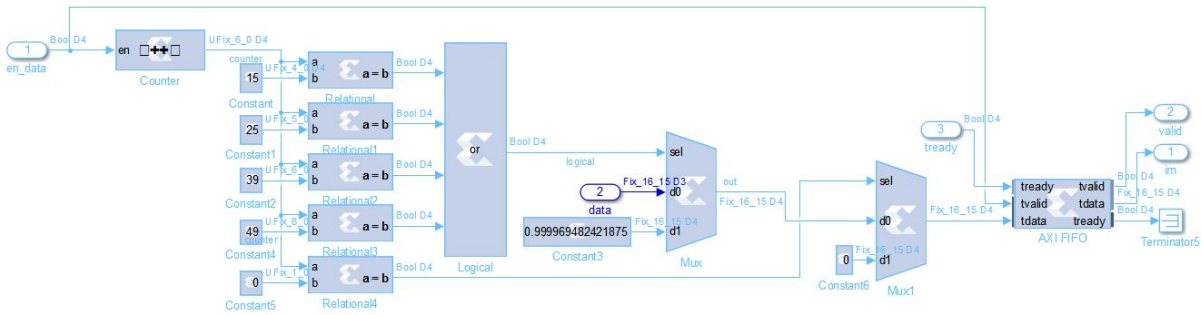


Figure 4.5: Implementation module of Subcarrier Allocation.

this counter is 0 the output of this block is 0. When the counter is 15, 25, 39 or 49 the output is 0.99 (pilot). 0.99 is the highest value that can be represented by the Fix_16_15 format. When the counter is another value, the output of the block is the data provided by the Mapping block.

The FIFO inserted in the end is for control of data that leaves this block and goes to the IFFT block. Figure 4.6 illustrates the waveforms of the Subcarrier Allocation. Five signals are represented in the figure. "Valid" represents when the data is valid. This signal is provided by the Mapping block. The "counter" represents the count of the valid input IQ pair from 0 to 63. "output_re" represents the output I value of the subcarrier allocation module. "output_im" represents the output Q value of the subcarrier allocation module. It is possible to observe in the waveforms that, when the "counter" is 0 the "output_re" and "output_im" are 0, and when the "counter" is 15 the "output_re" and "output_im" are 0.99.

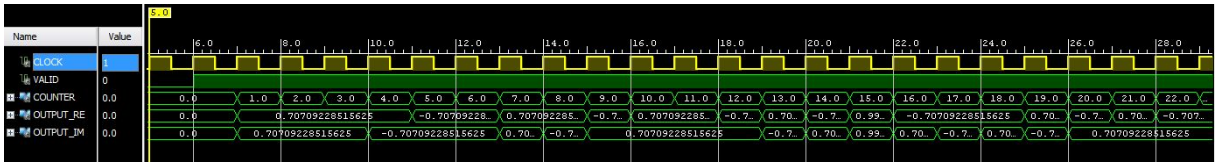


Figure 4.6: Waveforms of the Subcarrier Allocation module.

4.2.2 IFFT and Cyclic Prefix

Figure 4.7 shows the "Fast Fourier Transform v9.0" IP core. The real and imaginary components of the input are numbers represented in the Fix_16_15 format. The "s_axis_data_tvalid" signal indicates the data loading. By defining the "s_axis_config_tdata_cp_len" the Cyclic Prefix is automatically added during IFFT output process. The core implements IFFT when the

"s_axis_config_tdata_fw_inv" is set to low. "s_axis_config_tdata_scale_sch" shows the scaling schedule for each radix-2 pair (called as a group). In this design, it is set to "101010" (represents 3 groups). This configuration means that, for each radix-2 pair (group) the data is right shifted by 2 (10) and with this the output results are scaled by 1/8, which avoids overflow. The Pipelined Streaming I/O (architecture chosen for this project) solution pipelines several Radix-2 butterfly processing engines to offer continuous data processing. Each processing engine has its own memory banks to store the input and intermediate data (see figure 4.8). The core has the ability to simultaneously perform transform calculations on the current frame of data, receive input data for the next frame of data, and send out the results of the previous frame of data.

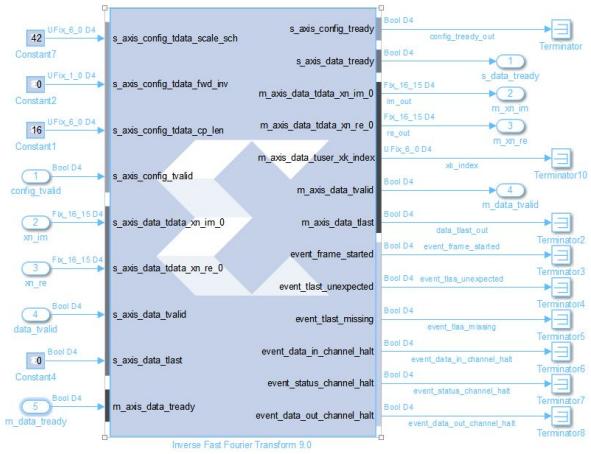


Figure 4.7: Implementation module of IFFT.

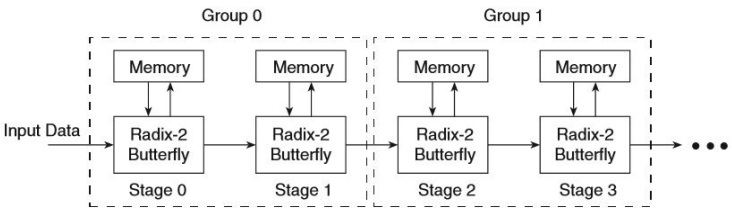


Figure 4.8: Pipelined Streaming I/O (from [33]).

This core uses a basic handshake and the signals that control the transfer of data are described in Table 4.1.

Figure 4.9 describes the data loading process of the IFFT block. The last signal (third) represented in the figure shows the real and imaginary values. In the loading process, the signals that control transfer of data are "s_axis_data_tvalid" (first signal in the figure) and "s_axis_data_tready" (second signal in the figure). When these two are high then a transfer occur. Notice that, when the "s_axis_data_tready" is low the input data stays unchanged, as noted in figure.

Figure 4.10 illustrates the IFFT output process. The last (fourth) signal represented in the figure shows the real and imaginary values. In the output process, the main signals are "m_axis_data_tready" (second signal in the figure) and "m_axis_data_tvalid" (third signal in the figure). If "m_axis_data_tready"

Table 4.1: Main port descriptions of the IFFT IP core.

Name	Direction	Description
s_axis_data_tvalid	Input	Asserted by the Subcarrier Allocation block to signal that it is able to provide data.
m_axis_data_tready	Input	Asserted by the SDM block to signal that it is ready to accept data.
s_axis_data_tready	Output	Used by the core to signal that it is ready to accept data. This signal controls the tready signal of the FIFO in Subcarrier Allocation.
m_axis_data_tvalid	Output	Used by the core to signal that it is ready to accept data.

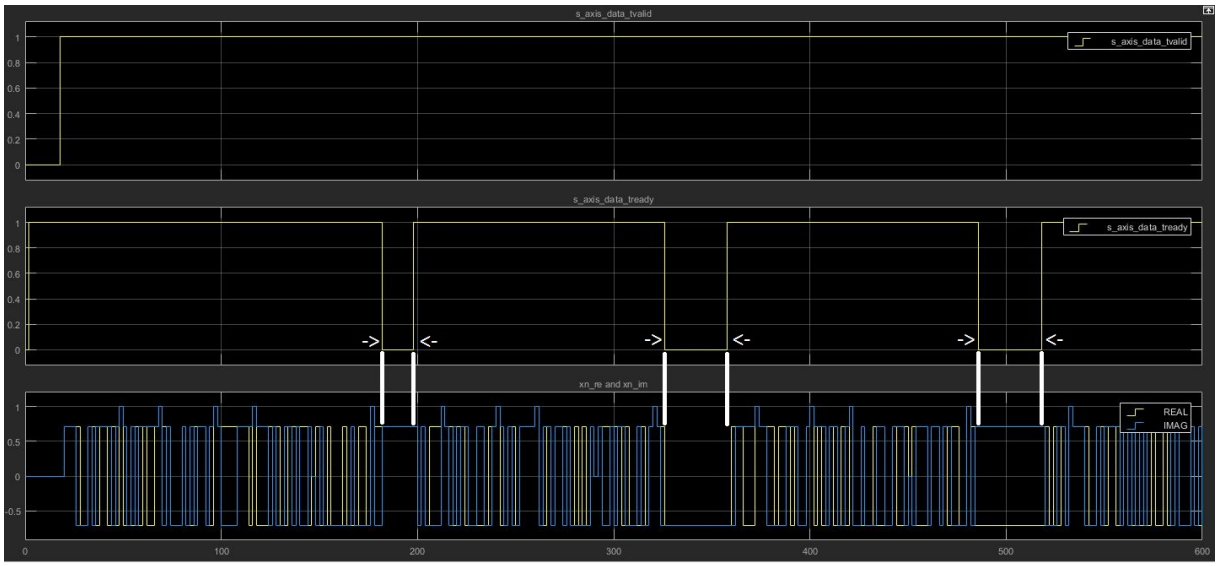


Figure 4.9: Waveforms of data loading for IFFT block.

goes low then the output of the IFFT stays unchanged. The output is produced in natural order represented by "xk_index" (first signal in the figure). Within one OFDM symbol period, it first counts from 48 to 63, when the 16-sample Cyclic Prefix is being sent. Then, "xk_index" counts from 0 to 63, showing the efficient OFDM symbol is sent. "m_axis_data_tvalid" is always high when the valid data is sent, irrespective of the Cyclic Prefix or the efficient symbol. Because of the scaling, the real and imaginary components of the output are also Fix_16_15 numbers. The real and imaginary values bellow of the white marker in the figure are the same. The output of this block was validated using Matlab. The input of the IFFT block was used to calculate the ifft in Matlab to validate this process.

4.2.3 Digital Up-Converter

In this block the up-sampling of the base band signal is done in the first place. For this a FIFO block and a FIR block were used like presented in figure 4.11.

The FIR Compiler was configured as an interpolating FIR filter with an interpolation rate value of $L = 100$. The filter architecture chosen was the "Systolic Multiply-Accumulate" (see figure 4.12).

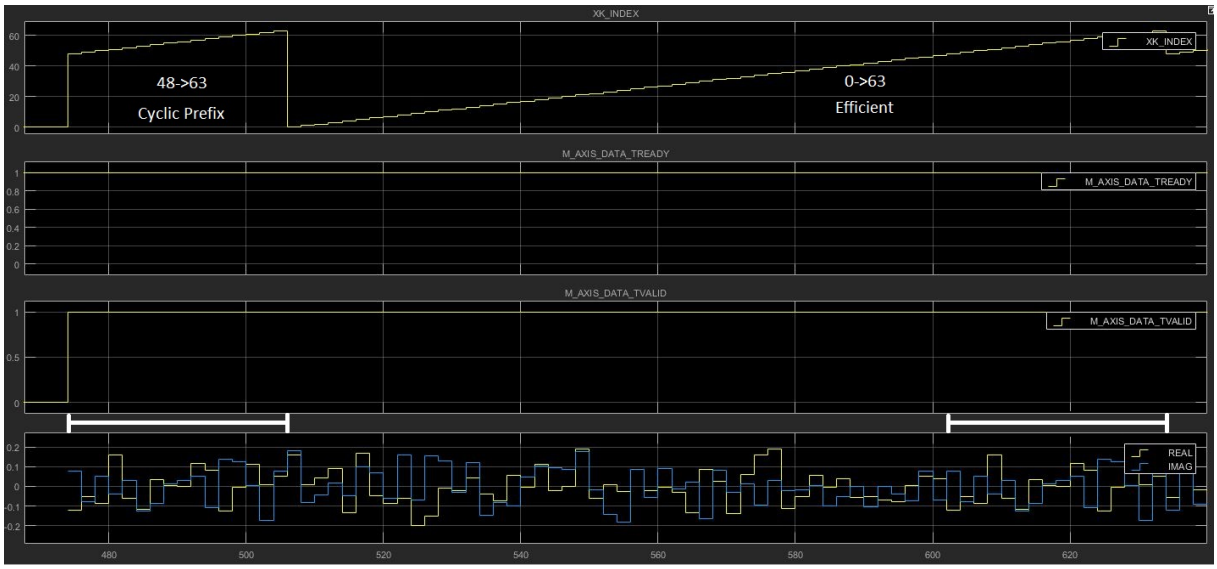


Figure 4.10: Waveforms of data output for IFFT block.

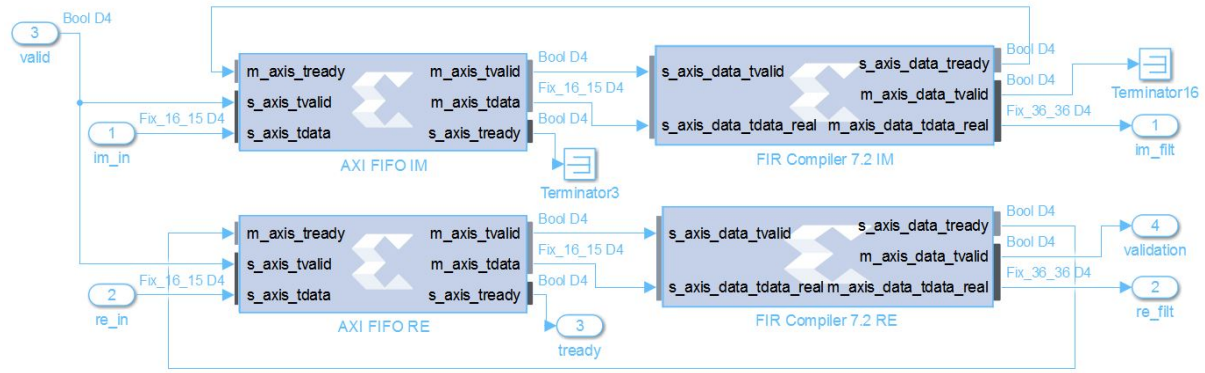


Figure 4.11: Implementation module of up-sampling.

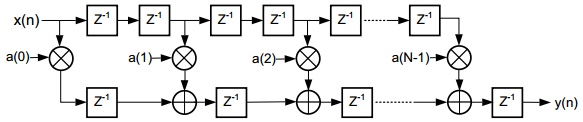


Figure 4.12: Systolic Multiply-Accumulate architecture implementing a pipelined Direct-Form filter (from [34]).

This architecture is directly supported by the DSP Slice and results in area-efficient and high performance filter implementation. The structure also extends to exploit coefficient symmetry, thus providing further resource savings. To enter the coefficients of the filter in FIR Compiler, I used the FDATool of Matlab. The filter has the passband frequency equal to 0.01 [normalized (0 to 1)]. The value of the passband frequency follows the theoretical explanation of this theme (up-sampling). When is performed an up-sampling by a factor of L, the normalized passband frequency is equal to 1/L $(\times \pi rad/sample)$ like presented in figure 4.13, to eliminate redundant

spectral images ($\pi/L < \omega < \pi$) on one period of the spectral representation of the discrete signal.

The stopband frequency is equal to 0.011 [normalized (0 to 1)], which provides a minimum transition band. The passband attenuation equal to 1 dB and the stopband attenuation equal to 80 dB provides a good performance of the filter. This configuration results in a direct-form FIR structure with an order equal to 5060. The frequency response and the corresponding angular frequency of the filter are represented in figure 4.14. Figure 4.15 demonstrates the frequency response with a zoom in the passband frequency. This is the expected frequency response of the filter.

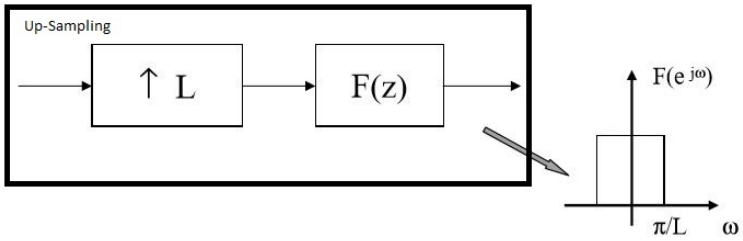


Figure 4.13: Theoretical explanation of up-sampling (from [35]).

The control of data entry is done by "s_axis_data_tready". This is high during one clock cycle in one hundred clock cycles. That means that the FIR filter reads one value from FIFO every one hundred clock cycles. The input and the output of the FIR Compiler can be seen in figure 4.16.

The DUC has two identical paths, one for the I-input and the other for the Q-input. For this reason, it is also referred to as a complex DUC. After this process of up-sampling, the I and Q values modulates a carrier. This implementation can be seen in figure 4.17.

For carrier modulation, two multiplexers were implemented, one for the cosine and other for the sine. They are controlled by a counter that counts from 0 to 3. After that, the samples are added to each others. The output can be seen in figure 4.18.

4.2.4 Sigma-Delta modulator

Figure 4.19 shows the implementation of the band-pass Sigma-Delta modulator following the theoretical presentation of the modulator in subsection 2.3.1. The spectrum at the output of the modulator can be seen in figure 4.20. These figures are from Matlab simulation process. Notice that, because of the action of the subcarrier allocation block, the power spectrum has peaks at the pilot subcarriers and has a dip at the null subcarrier (middle) as expected (see figure 4.20b).

Figure 4.20a is a good representation of the theoretical figure 2.13 presented in section 2.3. The action of the NTF and STF are well represented in this figure as expected.

An important thing to point out is the implementation of the "DAC" of the band-pass Sigma-Delta. For this, was used a multiplexer. If the sample at the input of the quantizer has the most significant bit equal to one that means that the sample is negative and the output of the multiplexer is the most negative (signed two's complement) number from the DUC output, on the other hand, if the most significant bit is equal to zero that means that the sample is positive (signed two's

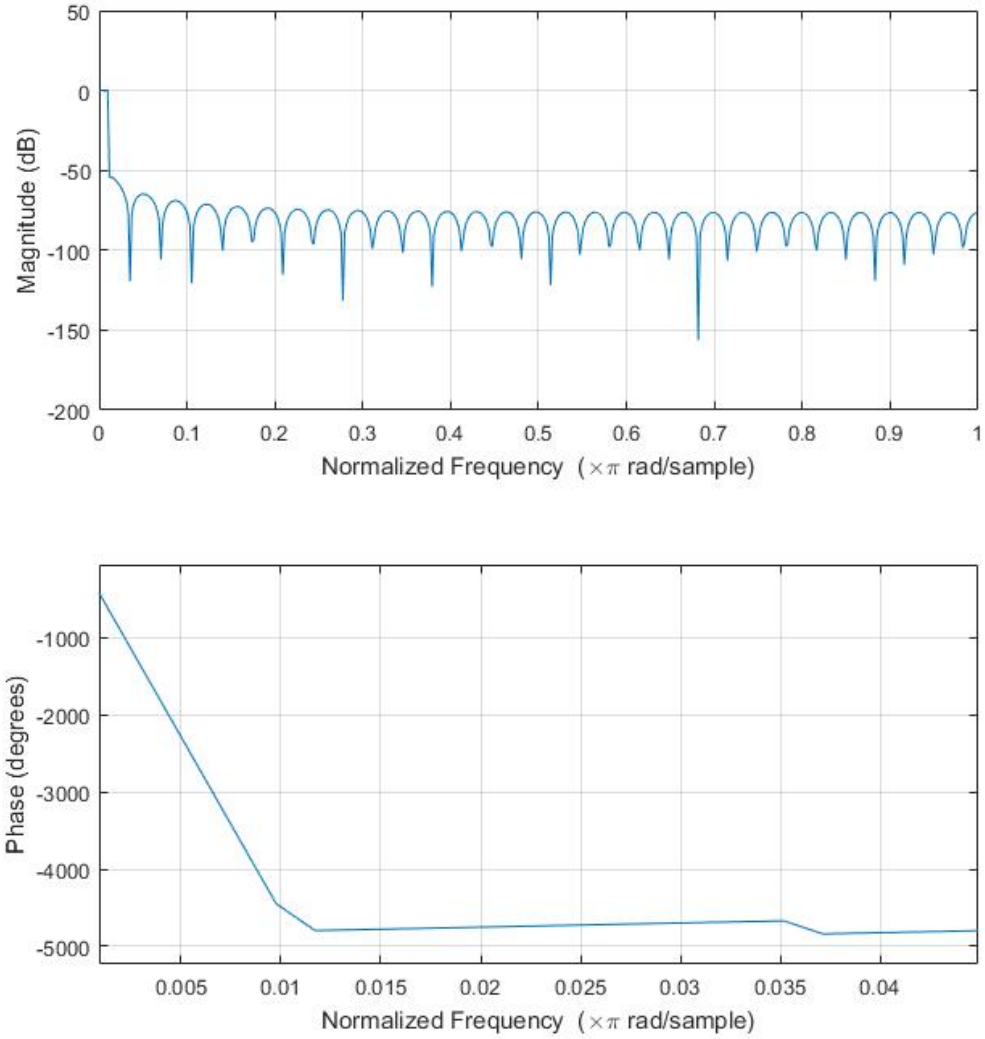


Figure 4.14: Frequency response and angular frequency of the filter.

complement) and the output of the multiplexer is the most positive number from the DUC output. All the operations like addition or subtraction are performed in signed two's complement form.

4.2.5 Memory

As was said in the previous chapter, it is necessary to have a block to store the bitstream from the Sigma-Delta. Figure 4.21 shows this implementation. I used a "Serial to Parallel" block to group 16-bit sequences. The "Single Port RAM" block is used to first store the 16-bit sequences, this is done by setting the "we" port to one while the "Counter2" is increased from 15 to 15 clock cycles. This counter controls in which address is written the 16-bit sequences from the "Serial to Parallel". After store the 16-bit sequences in RAM, the values are written in sequence to the outside of the

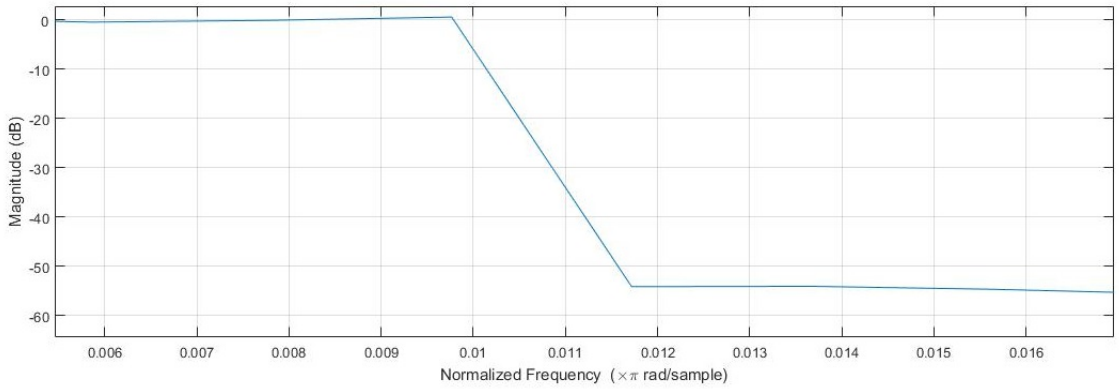
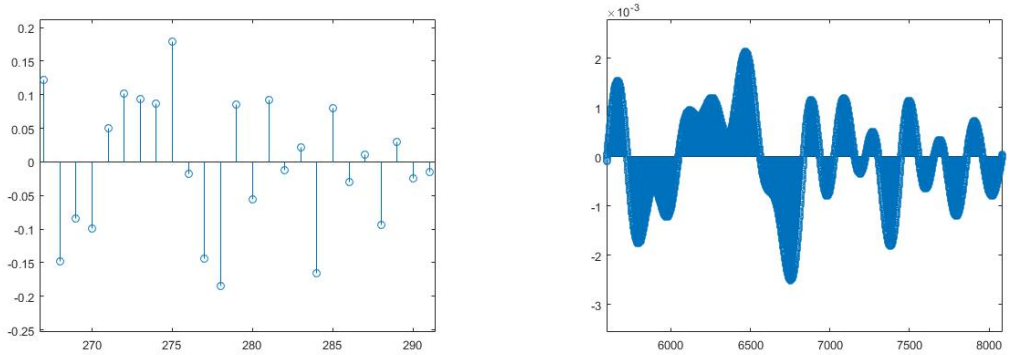


Figure 4.15: Frequency response in the passband frequency of the filter.



(a) (b)

Figure 4.16: Input of the FIR filter (a) and output of the FIR filter (b).

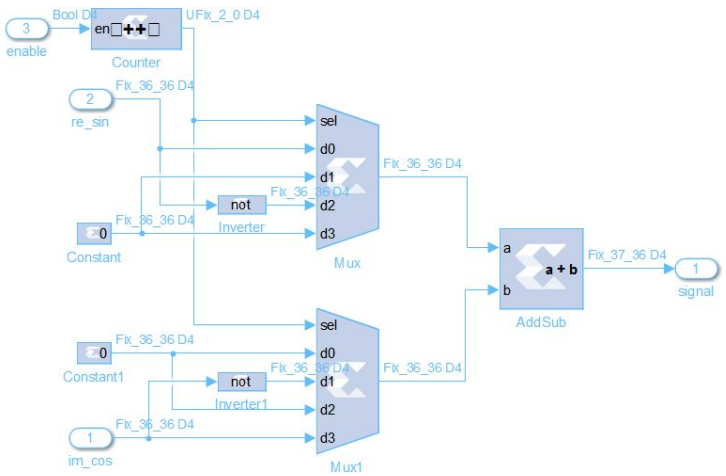


Figure 4.17: Implementation module of mixing with a carrier.

block, this is done by setting the "we" port to zero, disabling the "Counter2" and activating the "Counter3". The "global_enable" is the signal that enables the counters and the serial/parallel

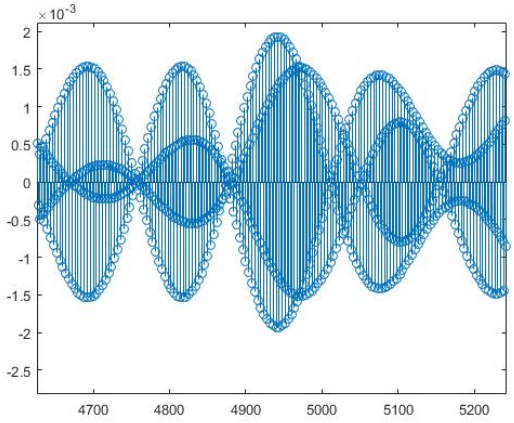


Figure 4.18: Waveform of data output of DUC block.

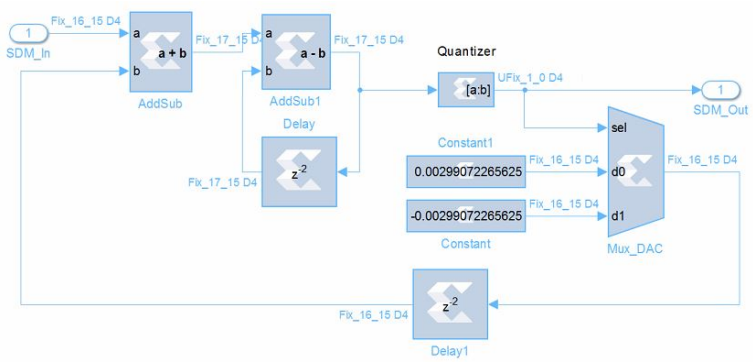
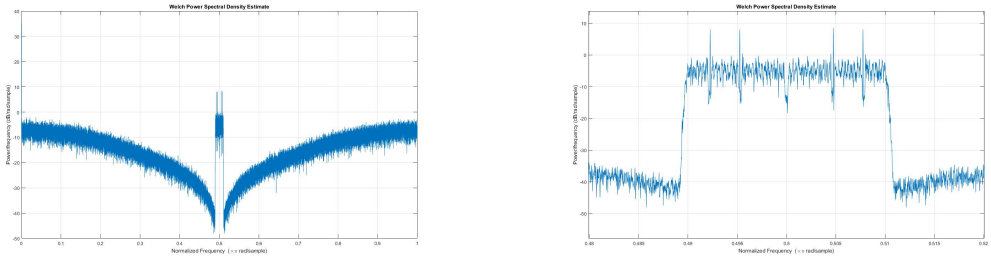


Figure 4.19: Implementation module of the band-pass Sigma-Delta.



(a) (b)

Figure 4.20: Spectrum at the output of the band-pass Sigma-Delta (a) and zoom in the band of interest (b).

blocks. This signal is provided by DUC block. The depth of the RAM was chosen to be 450000. The PPG was used to validate this process, to see if the bitstream generated by the sigma-delta block was correct or not. The minimum of bits required of PPG to represent a good quality of signal was 450000. So, this value was used as a reference to implement this memory block.

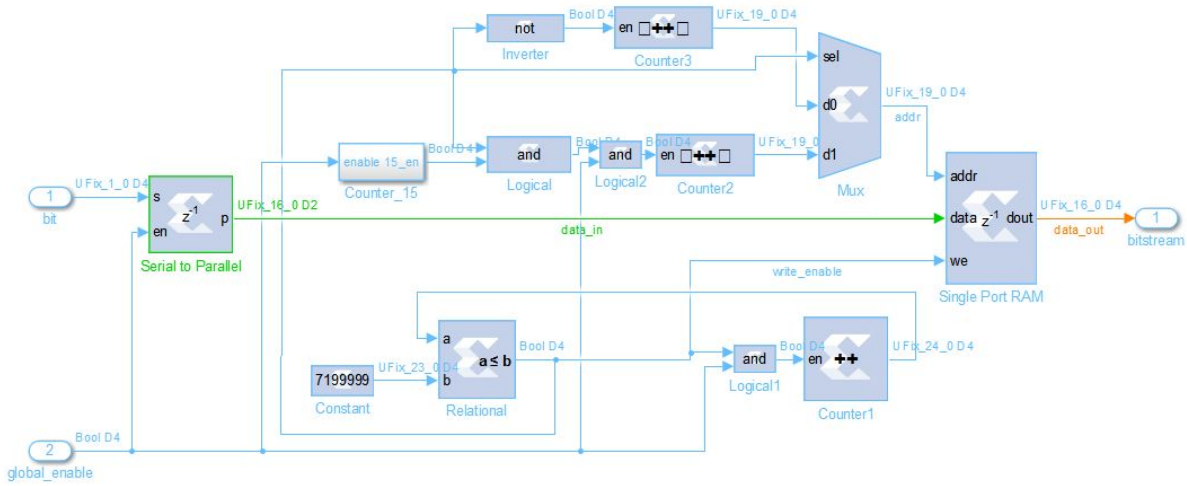


Figure 4.21: Implementation module of Memory block.

Chapter 5

System testing and experimental results

This chapter starts with the presentation of the validation process of the design. After that, the results of the hardware implementation are described. In the last part of the chapter the architecture and the results of the implementation in electrical and optical domains are presented.

5.1 System testing

The Matlab and the waveform viewer of the XSG were used to validate the implementation of the design in the initial phase. The next phase of the verification is the behavioral simulation using the Xilinx Vivado with a testbench created by the XSG. The last phase and the most important test of the implementation design was done while the FPGA is running (real-time testing). The ILA (Integrated Logic Analyzer) IP core from Xilinx was used for this evaluation.

The ILA IP core is a logic analyzer core that can be used to monitor the internal signals of a design. The many advanced features of modern logic analyzers that ILA provides, including boolean trigger equations and edge transition triggers were used for this evaluation.

The internal signals in the design are sampled at design speeds and stored using on-chip block RAM (BRAM). Communication with the ILA core is conducted using an auto-instantiated debug core hub that connects to the JTAG interface of the FPGA.

After the trigger occurs, the sample buffer is filled and uploaded into the Vivado logic analyzer. To view this stored data, the waveform window in Vivado logic analyzer was used.

Regular FPGA logic was used to implement the probe sample and trigger functionality. On-chip block RAM memory stores the data until it was uploaded by the software. No user input or output was required to trigger events, capture data or to communicate with the ILA core.

To validate the GTX transceivers of the FPGA, I created a little Verilog file that sends in sequence to the outside a bitstream of bits. This bitstream was 32'hAAAA0000. 0.5 Gbps was the line rate chosen. 500 MHz was the serial clock of the transceivers and 15.625 MHz was the parallel clock following the demonstrated in subsection 3.1.1 (32 bits $\times 15.625\,\mathrm{M} = 500\,\mathrm{M}$). To verified the bitstream at the output of the FPGA, a DSO was used. Figure 5.1 demonstrates the bitstream using a DSO. The white marker represents the measure of 1 bit (500 MHz). The light blue marker

represents the measure of 16 bits (31.25 MHz). The blue marker represents the measure of 32 bits (15.625 MHz).

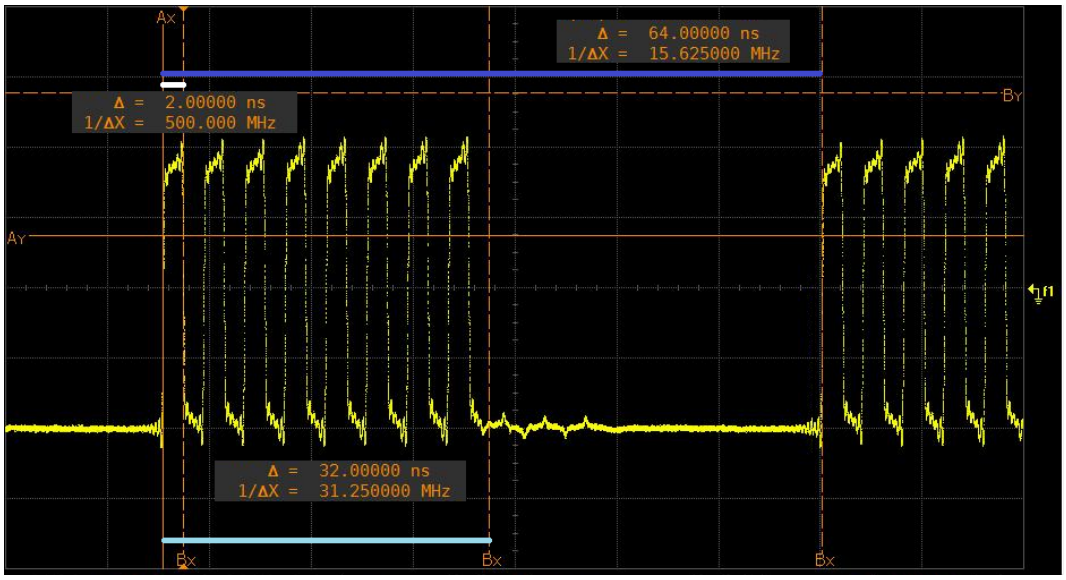


Figure 5.1: Bitstream in DSO.

After passing in all these tests, the design was finally validated.

5.2 Hardware implementation results

The design synthesis was performed with Xilinx Synthesis Technology and the gate-level netlist was obtained. After that, place and routing was performed. The routing delays was back annotated to the gate-level netlist for timing analysis and design optimization. Finally, a bitstream was generated to program the FPGA. Figure 5.2 and 5.3 shows the area results with regard to resource consumption, and the timing results of the implemented design, respectively. The timing report generated from Xilinx Timing Analyser tool indicates no timing conflict in the design. The project requires some BRAM blocks and DSP slices, as expected.

Resource	Utilization	Available	Utilization %
LUT	5789	303600	1.91
LUTRAM	1212	130800	0.93
FF	7696	607200	1.27
BRAM	257	1030	24.95
DSP	120	2800	4.29
IO	2	700	0.29
GT	4	28	14.29
BUFG	5	32	15.62
MMCM	2	14	14.29

Figure 5.2: Utilization report.

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4,011 ns	Worst Hold Slack (WHS):	0,045 ns	Worst Pulse Width Slack (WPWS):	1,100 ns
Total Negative Slack (TNS):	0,000 ns	Total Hold Slack (THS):	0,000 ns	Total Pulse Width Negative Slack (TPWS):	0,000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	35015	Total Number of Endpoints:	35015	Total Number of Endpoints:	10688

All user specified timing constraints are met.

Figure 5.3: Timing report.

5.3 Implementation in the electrical domain of the system

5.3.1 Architecture

Figure 5.4 presents the architecture of the electrical system implemented. The explanation of this setup is in next subsection.

Figure 5.4: Architecture of the electrical system implemented.

5.3.2 Experimental setup

The radio-frequency signal is generated in the FPGA like presented in the previous chapters. Then, the signal is directly sampled by the signal analyser in real time. Finally, using the VSA 8600 Agilent software, the demodulation and analysis of the OFDM signal was done.

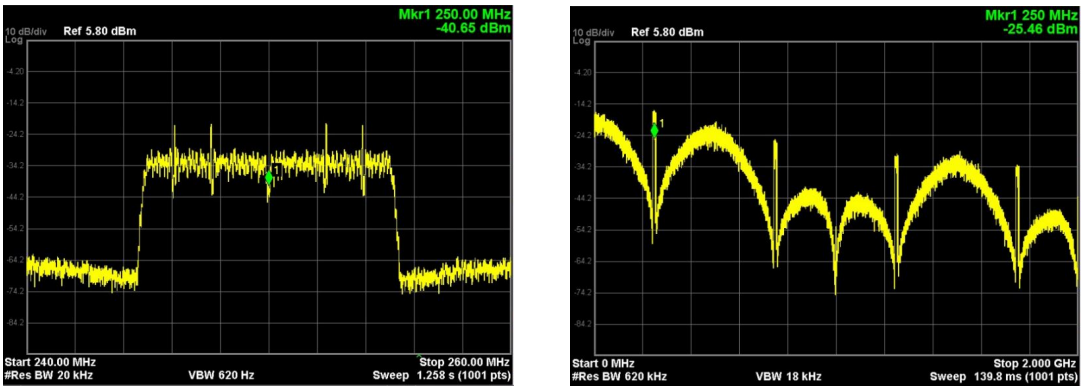
5.3.3 Spectrum of the signal

In this section, the power spectrum of the bandpass Sigma-Delta modulated signal obtained at the output of the FPGA for a QPSK signal with a fundamental frequency at 250 MHz is presented in figure 5.5a. This power spectrum has peaks at the pilot subcarriers and has a dip at the null subcarrier (middle) like demonstrated in simulation in the previous chapter. This signal has 10 MHz of bandwidth for an OSR of 50 according theoretical approach demonstrated in section 2.3.

Notice that, the peaks shown in figure 5.5b represents the high frequency replicas as presented in section 2.3. The first replica appears at 1.25 GHz and the second replica appears at 2.25 GHz

5.3.3.1 Signal centered at 2.5 GHz

As was presented in section 3.3.4, a modification on the initial design has allowed to put the fundamental frequency of the signal at 2.5 GHz, the first replica at 12.5 GHz and the second replica at 22.5 GHz. The power spectrum of this signal is shown in figure 5.6. This signal has 100 MHz of



(a) (b)

Figure 5.5: Power spectrum of the signal centered at 250 MHz (a) and with the high frequencies replicas (b).

bandwidth for an OSR of 50, as expected. This power spectrum has peaks at the pilot subcarriers and has a dip at the null subcarrier (middle).

The results presented in this subsection and subsection above are expected according the simulated results presented in subsection 4.2.4. So, the quality of these results are really good.

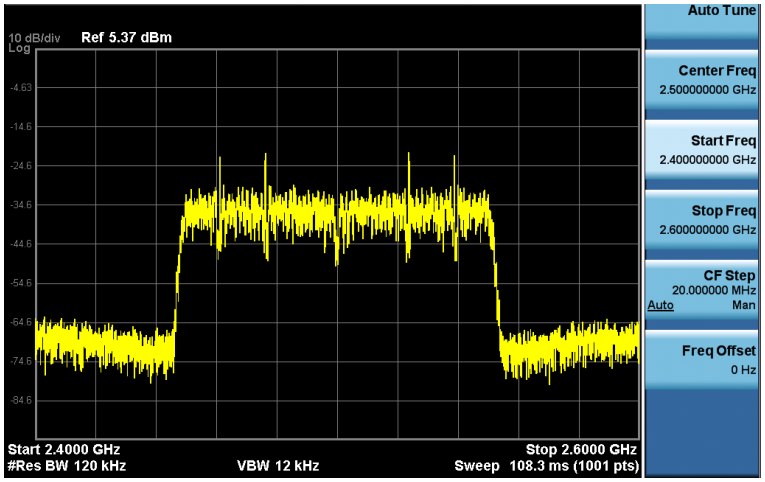


Figure 5.6: Power spectrum of the signal centered at 2.5 GHz.

5.3.4 Experimental results

In order to evaluate the performance of the system, I have considered the EVM performance metric obtained trough the VSA. First, the results of the received and bandpass filtered QPSK signal centered at the fundamental frequency ($f_{c0} = 250\,\text{MHz}$), as well as at the higher frequency given by the first replica ($f_{c1} = 1.25\,\text{GHz}$) as a function of the peak-to-peak ($_{pp}$) input voltage (V_{pp}) of the transmitted Sigma-Delta bit stream are presented. After, the same set of measurements for a 16-QAM modulation scheme are presented.

5.3.4.1 QPSK

Figure 5.7 shows the constellation diagram of the demodulated signal for V_{pp} = 1.119 V and f_{c0} = 250 MHz. The red points represents the points of the QPSK constellation, the white points represents the pilots and the grey points represents the "null" in the middle of the OFDM spectrum.

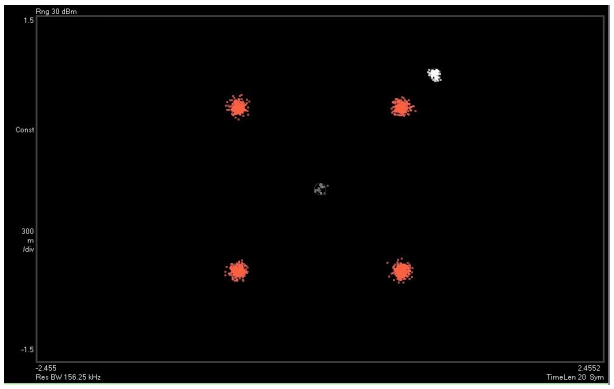


Figure 5.7: Constellation diagram of the QPSK demodulated signal.

Tables 5.1 and 5.2 shows the EVM results in decibel (dB) for f_{c0} = 250 MHz and f_{c1} = 1.25 GHz, respectively.

Table 5.1: EVM results for QPSK signal centered at 250 MHz.

V_{pp}	1.119 V	0.741 V	0.269 V
Pilot	-33.472	-31.148	-26.704
Data	-27.261	-25.804	-20.888
Null	-35.752	-28.389	-23.121

The best result for data was approximately -27dB for a V_{pp} = 1.119 V, which is a satisfactory result for the implementation. The constellation diagram, in figure 5.7, proves that is very easy to distinguish from each of the points of the constellation.

Table 5.2: EVM results for QPSK signal centered at 1.25 GHz.

V_{pp}	1.119 V	0.741 V	0.269 V
Pilot	-23.743	-14.433	-11.059
Data	-17.981	-13.001	-5.945
Null	-19.662	-14.121	-6.338

The performance decrease with the increase of the center frequency from 250 MHz to second replica at 1.25 MHz. The best result for data was approximately -18dB for a V_{pp} = 1.119 V.

5.3.4.2 16-QAM

Figure 5.8 shows the constellation diagram of the demodulated signal for V_{pp} = 1.119 and f_{c0} = 250 MHz. The blue points represents the points of the 16-QAM constellation, the white points

represents the pilots and the grey points represents the "null" in the middle of the OFDM spectrum.

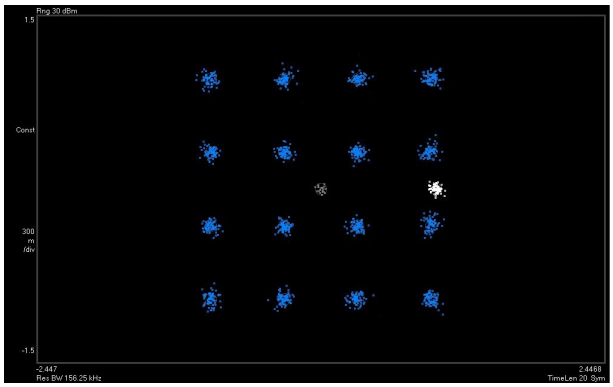


Figure 5.8: Constellation diagram of the 16-QAM demodulated signal.

Tables 5.3 and 5.4 shows the EVM results in decibel (dB) for $f_{c0} = 250\,\text{MHz}$ and $f_{c1} = 1.25\,\text{GHz}$, respectively.

Table 5.3: EVM results for 16-QAM signal centered at 250 MHz.

V_{pp}	1.119 V	0.741 V	0.269 V
Pilot	-25.503	-12.035	-11.709
Data	-22.178	-17.854	-16.157
Null	-29.362	-26.009	-23.538

The best result for data was approximately -22dB for a V_{pp} = 1.119 V, which is a satisfactory result for the implementation. The constellation diagram, in figure 5.8, proves that is very easy to distinguish from each of the points of the constellation. Another relevant result is the performance decrease with the increase of the points in the constellation. So, with the increase of the points in the constellation diagram (increase of M-QAM) the results will certainly become increasingly worse.

Table 5.4: EVM results for 16-QAM signal centered at 1.25 GHz.

V_{pp}	1.119 V	0.741 V	0.269 V
Pilot	-11.263	-10.693	X
Data	-15.533	-13.721	X
Null	-18.316	-15.913	X

The performance decrease with the increase of the center frequency from 250 MHz to second replica at 1.25 MHz and with the decrease of the V_{pp}. The best result for data was approximately -16dB for a V_{pp} = 1.119 V.

5.4 Implementation in the optical domain of the system

5.4.1 Architecture

Figure 5.9 presents the architecture of the electrical-optical system implemented. The explanation of this setup is in next subsection.

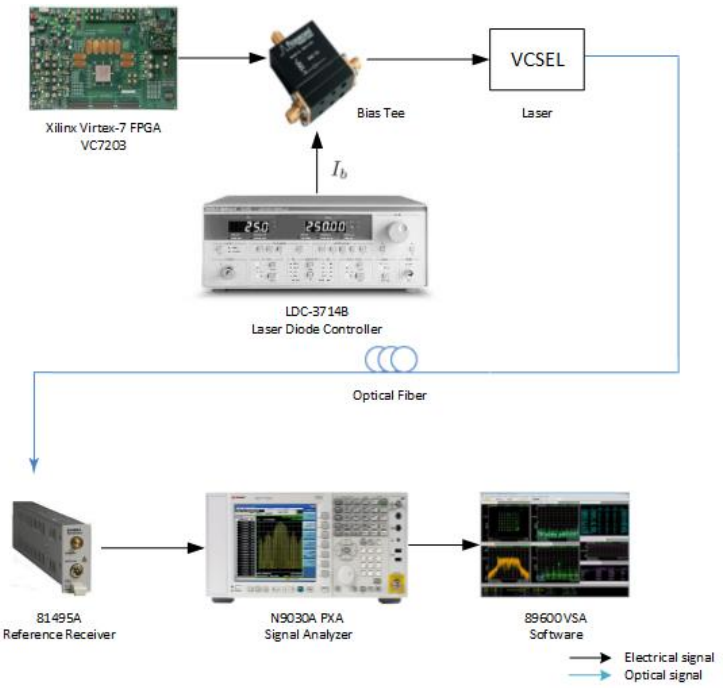


Figure 5.9: Architecture of the electrical-optical system implemented.

5.4.2 Experimental setup

The radio-frequency signal is generated in the FPGA like presented in the previous chapters. The output signal (electrical) from FPGA is used to modulate the VCSEL. The introduction of the Bias Tee is justified by the need of introducing a bias current on this laser. In VCSEL, an electrical-optical conversion occurs and is obtained an optical signal at the output of the VCSEL. In the optical domain, the signal with a 1550 nm wavelength, passes through the fiber. After passing through the optical fiber, the bit stream is converted into the electrical domain by means of a photodiode performed by an Agilent 81495A reference receiver. Then, the signal is converter to the electrical domain and is directly sampled by the signal analyser in real time. Finally, using the VSA 8600 Agilent software, the demodulation and analysis of the OFDM signal was done. Note that, the optical fiber channel does not reach one meter.

5.4.3 Experimental results

In order to evaluate the performance of the system, I have considered the EVM performance metric obtained trough the VSA. First, the results of the received and bandpass filtered QPSK with $f_{c0} =$

250 MHz and $f_{c1} = 1.25$ GHz as a function of (V_{pp}) and bias current (I_b) of the transmitted Sigma-Delta bit stream are presented. After, the same set of measurements for a 16-QAM modulation scheme are presented.

5.4.3.1 QPSK

Tables 5.5, 5.6 and 5.7 shows the EVM results in decibel (dB) for $f_{c0} = 250$ MHz as function of (I_b) for V_{pp} = 1.119 V, V_{pp} = 0.741 V and V_{pp} = 0.269 V, respectively. Tables 5.8 and 5.9 shows the EVM results in decibel (dB) for $f_{c1} = 1.25$ GHz as function of (I_b) for V_{pp} = 1.119 V and V_{pp} = 0.741 V, respectively.

Table 5.5: EVM results for QPSK signal centered at 250 MHz and V_{pp} = 1.119 V.

I_b	3 mA	5 mA	7.5 mA
Pilot	-22.556	-28.337	-31.301
Data	-16.661	-22.321	-25.397
Null	-17.253	-23.821	-30.081

Table 5.6: EVM results for QPSK signal centered at 250 MHz and V_{pp} = 0.741 V.

I_b	3 mA	5 mA	7.5 mA
Pilot	-15.231	-22.271	-30.741
Data	-13.501	-16.305	-24.681
Null	-15.604	-17.042	-26.388

Table 5.7: EVM results for QPSK signal centered at 250 MHz and V_{pp} = 0.269 V.

I_b	3 mA	5 mA	7.5 mA
Pilot	-13.616	-14.345	-24.425
Data	-12.862	-15.023	-17.219
Null	-13.710	-16.779	-19.695

The best result for data was approximately -25dB for a V_{pp} = 1.119 V and a I_b = 7.5 mA, which is a satisfactory result for the implementation. Another relevant result is the performance increase with the increase of the I_b and a performance decrease with the decrease of the V_{pp} as expected.

Table 5.8: EVM results for QPSK signal centered at 1.25 GHz and V_{pp} = 1.119 V.

I_b	3 mA	5 mA	7.5 mA
Pilot	X	-12.237	-21.197
Data	X	-10.539	-15.888
Null	X	-11.612	-17.375

The performance decrease with the increase of the center frequency from 250 MHz to second replica at 1.25 MHz. The best result for data was approximately -16dB for a V_{pp} = 1.119 V and a

Table 5.9: EVM results for QPSK signal centered at 1.25 GHz and V_{pp} = 0.741 V.

I_b	3 mA	5 mA	7.5 mA
Pilot	X	-12.235	-13.183
Data	X	-7.723	-10.018
Null	X	-8.090	-10.747

I_b = 7.5 mA. The performance increase with the increase of the I_b and the performance decrease with the decrease of the V_{pp} as expected.

5.4.3.2 16-QAM

Tables 5.10, 5.11 and 5.12 shows the EVM results in decibel (dB) for $f_{c0} = 250$ MHz as function of (I_b) for V_{pp} = 1.119 V, V_{pp} = 0.741 V and V_{pp} = 0.269 V, respectively. Tables 5.13 and 5.14 shows the EVM results in decibel (dB) for$f_{c1} = 1.25$ GHz as function of I_b for V_{pp} = 1.119 V and V_{pp} = 0.741 V, respectively.

Table 5.10: EVM results for 16-QAM signal centered at 250 MHz and V_{pp} = 1.119 V.

I_b	3 mA	5 mA	7.5 mA
Pilot	-18.742	-23.664	-24.669
Data	-16.141	-21.076	-21.081
Null	-16.632	-24.475	-27.462

Table 5.11: EVM results for 16-QAM signal centered at 250 MHz and V_{pp} = 0.741 V.

I_b	3 mA	5 mA	7.5 mA
Pilot	-11.027	-11.530	-12.003
Data	-15.333	-16.559	-17.574
Null	-18.312	-23.952	-25.771

Table 5.12: EVM results for 16-QAM signal centered at 250 MHz and V_{pp} = 0.269 V.

I_b	3 mA	5 mA	7.5 mA
Pilot	-10.011	-10.756	-11.098
Data	-12.092	-13.107	-14.638
Null	-14.714	-15.128	-17.214

The best result for data was approximately -21dB for a V_{pp} = 1.119 V and a I_b = 7.5 mA, which is a satisfactory result for the implementation. Another relevant result is the performance increase with the increase of the I_b and a performance decrease with the decrease of the V_{pp} as expected.

Table 5.13: EVM results for 16-QAM signal centered at 1.25 GHz and V_{pp} = 1.119 V.

I_b	3 mA	5 mA	7.5 mA
Pilot	X	X	-11.012
Data	X	X	-14.920
Null	X	X	-16.025

Table 5.14: EVM results for 16-QAM signal centered at 1.25 GHz and V_{pp} = 0.741 V.

I_b	3 mA	5 mA	7.5 mA
Pilot	X	X	-10.583
Data	X	X	-12.984
Null	X	X	-15.462

The performance decrease with the increase of the center frequency from 250 MHz to second replica at 1.25 MHz. The best result for data was approximately -15dB for a V_{pp} = 1.119 V and a I_b = 7.5 mA.

5.5 Final comments on the results

The maximum EVM achieved is in the back-to-back configuration, i.e., without the optical channel in the QPSK modulation scheme. This value is approximately -27 dB, which is very close to the EVM obtained with a bias current of 7.5 mA. In the 16-QAM modulation the maximum EVM achieved is in the same configuration setup. This value is approximately -22 dB, which is very close to the EVM obtained with a bias current of 7.5 mA. An important fact to refer is the performance increase in the optical domain with the increase of the I_b and the V_{pp}. Another relevant result is the performance decrease with the increase of the center frequency to the second replica. The "X" marked in the tables means that the value of the EVM is so low that the VSA could not measure. Notice that, in optical domain, values for $f_{c1} = 1.25$ GHz with V_{pp} = 0.269 V was not possible to measure, because these value are so low.

Chapter 6

Conclusion and future work

6.1 Conclusion

In this dissertation, the theoretical analysis and simulation as well as FPGA implementation of an OFDM system was presented. With QPSK or 16-QAM modulation scheme, this system generates an OFDM waveform with a fundamental frequency centered at 250 MHz with a 10 MHz bandwidth or centered at 2.5 GHz with a 100 MHz bandwidth and an OSR of 50. Different kinds of transmitting proprieties have been analyzed and compared. Starting from the study of OFDM principle, the system has been verified and realized with the help of both Matlab/Xilinx System Generator simulation and hardware implementation in Xilinx Vivado. The design of the entire project has been carried out in a top-down approach, from the system design to functional blocks design.

Developing an RTL (register-transfer level) project from scratch, working with a Virtex 7 VC7203 board, more precisely with the GTX Transceivers feature, was very challenging. The project included three main tasks, which are: system planning and conception, system implementation and finally, system testing.

The main problem was designing, modeling and testing an OFDM transmitter using a reconfigurable platform (FPGA) for application to radio-over-fiber systems. The OFDM system was prototyped based on the article in [6] and with the OFDM system which was developed in Matlab for this article.

The solution for the implementation of the OFDM system starts with the study of the floating-point system which was made in Matlab, with this, the principal parameters that implements the OFDM system was defined like the number of subcarriers, the length of the cyclic prefix, the bandwidth of the system, the best modulation type to use, the number of bits to use, the type of synchronization and the number of points of the IFFT module.

The implementation of the OFDM system starts with the establishment of the fixed point model designed block by block in XSG. Each functional block was verified by checking the waveforms in Simulink Scope block. Then, the complete OFDM system is integrated together. A comparison

between floating point simulation of the Matlab OFDM and the fixed point Xilinx block-set was performed.

After that, a project in Xilinx Vivado was created where the necessary modules are instantiated to create a project capable of being synthesizable. The main modules of this project are the design created in XSG and the one that configures one or more high-speed serial transceivers (GTX Transceivers). Then, the design synthesis, place and route and bitstream generation to target FPGA board in Xilinx Vivado was performed. With the bitstream created, the timing and resource reports was analysed.

For experimental validation, a link with and without fiber was tested. For both, comparison between simulation results and physical results was performed.

The validation and evaluation of the experimental link RoF was performed using the equipment in the lab, such as, VCSEL, optical receiver and the signal analyser running VSA. EVM was the metric performance used for this evaluation.

6.2 Future work

This dissertation offers a detailed design and implementation process of an FPGA-based system, and is an initial work on the implementation part for an prototype project. It can be used as a basis for the future projects towards applications in advanced RoF systems. The work could be extended further to the following aspects:

- Others modules can be added to this design to improve the system performance and implement a more practical system. Other modules may consist of preamble insertion module and insert signal module. The preamble is used for synchronization and channel equalization, which is subdivided in short training and long training. The signal module is used to transmit the length, modulation type, and data rate information of the signal before send the multiple OFDM symbols, which is the module implemented in this design. Since the system is designed with a top-down approach, the implementation of others modules will not affect the modules already implemented in the system or will only cause minor modifications to their interfaces.

- Algorithm and system optimization could be performed to reduce the hardware resource consumption. CIC (Cascaded Integrator-Comb) compiler core provides the ability to design and implement CIC filters. The implementations of CIC filters have structures that use only adders, subtracters and delay elements. This is a good idea to reduce the hardware resource consumption, instead of using the FIR Compiler core.

- The designed FPGA system can be realized for others environments according to different standards. The mapping block could be modified by using ROMs or MCODE blocks to realize up to 256-QAM. The usage of Xilinx IP core enables an easy upgrade from 64-point IFFT to 512-point IFFT.

- Increase the order of the bandpass Sigma-Delta and verify the performance for each one.
- Increase the binary representation would be a good idea to verify how much the performance of the system increases.

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