

FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO



FEUP

Polyphase Filter with Parametric Tuning

by

Luís Filipe da Costa Malheiro

A thesis submitted in partial fulfillment of requirements for the degree of
Integrated Master in Electrical and Computers Engineering

Telecommunications Major

Supervisor: **Vítor Grade Tavares** (*Ph.D.*)

Co-supervisor: **Cândido Duarte** (*Eng.*)

June 2010

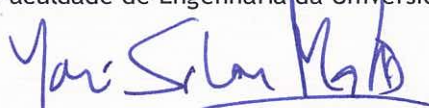
A Dissertação intitulada

“FILTRO POLIFÁSICO PARAMETRIZÁVEL”

foi aprovada em provas realizadas em 26/Julho/2010

o júri

Presidente Professor Doutor José Alfredo Ribeiro da Silva Matos
Professor Catedrático do Departamento de Engenharia Electrotécnica e de
Computadores da Faculdade de Engenharia da Universidade do Porto



Professor Doutor João Manuel Torres Caldeiras Simões Vaz
Professor Auxiliar do Departamento de Electrotécnica e de Computadores do
Instituto Superior Técnico da Universidade Técnica de Lisboa



Professor Doutor Vitor Manuel Grade Tavares
Professor Auxiliar do Departamento de Engenharia Electrotécnica e de
Computadores da Faculdade de Engenharia da Universidade do Porto (Orientador)



Mestre Manuel Cândido Duarte dos Santos
Assistente Convidado do Departamento de Engenharia Electrotécnica e de
Computadores da Faculdade de Engenharia da Universidade do Porto (Co-
Orientador)



O autor declara que a presente dissertação (ou relatório de projecto) é da sua exclusiva autoria e foi escrita sem qualquer apoio externo não explicitamente autorizado. Os resultados, ideias, parágrafos, ou outros extractos tomados de ou inspirados em trabalhos de outros autores, e demais referências bibliográficas usadas, são correctamente citados.



Autor - Luís Filipe da Costa Malheiro

Faculdade de Engenharia da Universidade do Porto

Abstract

The world of wireless communication systems has been growing very rapidly. The evolution of semiconductor technologies had significant impact on recent innovations seen in portable wireless systems. With the ever-increasing developments achieved with deep sub-micron CMOS processes, smaller devices with extended capabilities are continuously reinforcing the market of today's wireless technologies. The contemporary wireless scenario is driven by the need of better portability and lower cost production in a very competitive market of electronic systems. The overall performance of such devices cannot be significantly compromised by these demands. Hence, nowadays the wireless interfaces are taking the form of integrated circuits, where CMOS plays an important role contributing with higher levels of integration among other expensive technologies with better performances.

Recently, alternative receiver architectures have been preferably chosen instead of the classical topologies in which the integration levels were compromised by relatively high down-conversion intermediate-frequencies. Direct conversion and low-IF receiver schemes have been lately the focus of investigation in the area of radio-frequency microelectronics. In most of the radio-frequency receivers the image frequency is the most critical issue. This technical aspect often dictates the election of the receiver architecture for design of the radio-frequency hardware. One possible solution to mitigate this problem is the use of polyphase filters. A polyphase filter is an asymmetrical filter that performs filtering operations in the complex domain. By using this approach, the image signal can be further suppressed after down-conversion, thus avoiding lossy and expensive filters that are usually not capable of being integrated on-chip.

In this work, it is proposed the development of a polyphase filter in a 0.35- μm CMOS process using Cadence Virtuoso IC tools and SPECTRE/SPECTRE-RF simulator. The low-IF receiver has been chosen as preferable architecture for the present polyphase filter implementation. The proposed solution is based on the "Filter & Hold" (F&H) concept, which represents a new polyphase filter circuit approach with improved mixed-signal tuning capabilities when compared to several state-of-the-art implementations. Several circuit realizations have been proposed. Architectures based on g_m -C, active RC and MOSFET-C have been tested with the F&H technique. The g_m -C approach has been chosen due to significant performance advantages compared to other architectures, such as IRR, area and power consumption. A sixth-order Butterworth polyphase filter has been designed for operation at 2-MHz IF. Simulation results shown an IRR higher than 75-dB. Within the proposed polyphase-filter scheme the frequency response can be simply changed digitally due to the F&H approach adopted in the current design. This opens the possibility for simple digital baseband processing in calibration procedures for adaptive IRR optimization. The layout of a PPF implementation with the F&H technique showed an area reduction of about $\frac{1}{4}$ comparing with another implementation found in the literature.

Sumário

O mundo das comunicações sem-fios tem vindo a crescer contínua e rapidamente. As evoluções na tecnologia de semicondutores tiveram um impacto significativo em sistemas de comunicação sem-fios devido ao desenvolvimento da tecnologia CMOS. Equipamentos mais pequenos e com maior número de funcionalidades aparecem todos os dias no mercado das tecnologias sem-fios. Contudo, cada vez mais, é preciso melhorar a portabilidade destes sistemas e diminuir os custos de produção num mercado caracterizado pela elevada competitividade. Apesar de tudo, estas necessidades não devem comprometer a performance dos equipamentos. Por esse motivo, as interfaces sem-fios são desenvolvidas em circuitos integrados, onde a tecnologia CMOS tem um papel importante ao possibilitar níveis de integração mais elevados face a outras tecnologias mais dispendiosas, ainda que com melhor performance.

Recentemente, novas arquitecturas de recepção de rádio-frequência (RF) têm sido usadas em vez da arquitectura clássica, cujos níveis de integração eram reduzidos devido ao processo de conversão do sinal para uma frequência intermédia (FI) elevada. Receptores implementados em conversão directa e FI baixa têm sido foco de investigação na área de microelectrónica RF. Um dos maiores problemas na maioria dos receptores RF é a frequência imagem. A rejeição desta frequência influencia a escolha da arquitectura do receptor. Uma possibilidade de resolução deste problema é a utilização de filtros polifásicos. O filtro polifásico é um filtro assimétrico em que a filtragem é feita no domínio complexo. Desta forma, a rejeição da frequência da imagem é melhorada, evitando-se o uso de filtros dispendiosos, cuja integração não é possível.

Neste projecto é proposto o desenvolvimento de um filtro polifásico em tecnologia CMOS de $0.35\mu\text{m}$, usando o software Cadence Virtuoso IC e simuladores SPECTRE/SPECTRE-RF. Para tal, as arquitecturas de recepção típicas serão descritas, onde será justificada a utilização da arquitectura FI baixa para implementação do filtro polifásico. A solução proposta neste trabalho consiste em aplicar o conceito de “Filter & Hold” (F&H), apresentando assim uma nova arquitectura de filtro polifásico com novas possibilidades de calibração comparando com outras implementações do estado da arte. Neste trabalho são propostas várias possibilidades para implementação do circuito. Arquitecturas baseadas em g_m -C, active RC e MOSFET-C foram usadas para teste com o conceito de F&H. Optou-se pela implementação com g_m -C devido a uma performance superior, nomeadamente em termos de IRR, área e potência consumida. Um filtro polifásico Butterworth de sexta ordem com uma frequência central de 2-MHz foi assim implementado, apresentando uma rejeição de imagem superior a 75-dB. Nesta implementação, a área ocupada pelas capacidades foi reduzida devido ao uso da técnica F&H. Outra das vantagens desta implementação é a simplicidade de controlo digital da frequência central do filtro. Abre-se assim a possibilidade de uso de processamento digital simples na banda base para calibração adaptativa da rejeição de imagem do filtro polifásico. O layout do filtro foi realizado e demonstrou uma redução da área de cerca de $\frac{1}{4}$ comparativamente a outro trabalho na literatura com os mesmos objectivos.

Acknowledgments

Firstly, I would like to thank my parents and my brother for their love, constant encouragement, support through all the years and for giving me the opportunity to attend a Master's degree.

To my supervisor Vítor Grade Tavares I would like to express my gratitude for his advises and help with the implementation of the F&H technique.

To my co-supervisor Cândido Duarte I would like to express my deepest gratitude for his availability, continuous supervision and the constant help on trying to achieve the best out of this dissertation. Without his help this work would never had been possible.

To all the members from the Microelectronics Students' Group at the Faculty of Engineering of the University of Porto, of which I am a founder member, I would like to thank them for the support they gave and for providing me the infrastructures needed to develop this dissertation.

To Américo Dias and Amílcar Correia, who were also developing their dissertation at the same time as me, I would like to thank them for the good times we had together during this period.

To all my other friends, I would like to thank them for being a part of my life and making it better everyday.

Luís Malheiro

“In scientific work, those who refuse to go beyond fact rarely get as far as fact.”

Thomas Huxley

Contents

Abstract	iii
Sumário	v
Acknowledgments	vii
Abbreviations	xix
1 Introduction	1
1.1 Problem statement	1
1.2 Proposed solution	2
1.3 Dissertation outline	3
2 Background research	5
2.1 Fundamentals of RF Receivers	5
2.2 Image-Rejection techniques	10
2.2.1 Hartley IR	10
2.2.2 Weaver IR	12
2.2.3 Double Quadrature Mixing	14
2.2.4 Image-Rejection Ratio	16
2.3 Receiver Architectures	18
2.3.1 Superheterodyne	18
2.3.2 Homodyne	20
2.3.3 Wide-band IF	22
2.3.4 Low-IF	23
2.3.5 Comparison of architectures	25
2.4 Polyphase Filters	25
3 State of the Art	35
3.1 Polyphase filters	35
3.2 Tuning Schemes	39
3.3 G_m -C Filters	42
4 Architecture Development	49
4.1 Filter & Hold	49
4.1.1 F&H in the PPF	52
4.2 Implementation approach	54
4.2.1 G_m -C approach	57
4.2.1.1 First approach	65

4.2.1.2	Second approach	68
4.2.1.3	Third approach	70
4.2.2	Active RC approach	72
4.2.3	MOSFET-C approach	78
5	Conclusion	85
5.1	Results	85
5.2	Layout	90
5.3	Conclusion	91
5.4	Future work	92
	References	93

List of Figures

2.1	Heterodyne principle.	6
2.2	Signal spectrum of the heterodyne principle.	7
2.3	Down-conversion.	7
2.4	Image problem.	8
2.5	Half-IF problem.	8
2.6	Real and complex down-converters.	9
2.7	Block diagram of hartley image reject receiver.	10
2.8	Graphical representation of Hartley image-rejection exemplified.	12
2.9	Block diagram of the weaver image reject receiver.	12
2.10	Graphical representation of Weaver receiver.	13
2.11	Block diagram of the double quadrature mixing topology.	14
2.12	Graphical representation of the double quadrature mixing topology.	15
2.13	Generic quadrature down-converter.	16
2.14	Plots for constant ε in terms of IRR and θ , and constant IRR for different θ and ε	18
2.15	Block diagram of the heterodyne architecture.	19
2.16	Block diagram of homodyne architecture.	20
2.17	LO self-mixing causing DC offset.	21
2.18	Block diagram of a Wide-band IF receiver.	22
2.19	Block diagram of a low-IF receiver.	24
2.20	Examples of passive PPF stages.	26
2.21	RC-CR network analysis.	26
2.22	PPF AC analysis for one- and two-stage configurations.	27
2.23	Implementation for PPF quadrature generation.	27
2.24	Frequency translation of the LPF.	28
2.25	LP filter shift to complex BP.	29
2.26	Block diagram of the LPF shift to BPF with I and Q channels	29
2.27	Active-RC implementation of a PPF	30
2.28	Magnitude of the frequency response of an PPF designed in SIMULINK, SPECTRE-RF and the theoretical case	31
2.29	Magnitude representation of PPFs for several ω_{LP} , always with the same ω_{IF} and $\omega_0 = \omega_{LP}$	32
2.30	Constant IRR curves for a non-ideal PPF.	33
3.1	Sixth-order complex filter using G_m -C circuits.	36
3.2	Biquad circuit of Tajalli <i>et al.</i>	37
3.3	Schematic circuit of the amplifier of Song <i>et al.</i>	38
3.4	Schematic circuit of the amplifier in Abrishamifar <i>et al.</i>	38
3.5	PPF tuning scheme proposed by Sanchez-Sinencio <i>et al.</i>	40

3.6	Tuning circuit proposed in Dingkun Du <i>et al.</i>	41
3.7	Tuning scheme proposed in Fangxiong Chen <i>et al.</i>	41
3.8	PLL-based tuning proposed by Teo <i>et al.</i>	42
3.9	Transconductor with CMFF in Sinencio <i>et al.</i>	43
3.10	Transconductor with CMFB in Sinencio <i>et al.</i>	43
3.11	Nauta's transconductor.	43
3.12	OTA from Sanchez-Sinencio <i>et al.</i>	45
3.13	Transconductor from Chen <i>et al.</i>	45
3.14	CMFB/CMFF circuit from Chen <i>et al.</i>	46
3.15	Transconductor cell from Jader <i>et al.</i>	46
3.16	CMFB, active load and adaptive bias for the transconductor from Jader <i>et al.</i>	47
4.1	Single-pole RC filter with F&H concept applied.	50
4.2	Transient response of an F&H RC-filter	51
4.3	AC analysis of the F&H RC-filter and comparison with continuous-time implementation.	51
4.4	F&H for different sampling frequencies.	52
4.5	Active RC implementation with the F&H technique.	52
4.6	Bode magnitude plot and IRR of PPF with F&H depending on the value of k	53
4.7	G_m -C integrator.	54
4.8	Active RC integrator.	54
4.9	MOSFET-C integrator.	55
4.10	G_m -C op-amp integrator.	56
4.11	G_m -C LPF.	57
4.12	G_m -C LPF-biquad.	58
4.13	Ideal Butterworth LPF-biquad Bode magnitude plot.	60
4.14	G_m -C LPF-biquad with F&H.	60
4.15	Ideal LPF-biquad Bode magnitude plot with and without F&H for several duty-cycles.	61
4.16	G_m -C first-order PPF.	61
4.17	G_m -C second-order PPF.	62
4.18	Bode magnitude plot of the ideal g_m -C second-order PPF.	63
4.19	G_m -C PPF with F&H technique.	63
4.20	Sixth-order Butterworth PPF block diagram.	64
4.21	Bode magnitude plot of the ideal g_m -C sixth-order Butterworth PPF with and without F&H technique for several duty-cycles.	64
4.22	Bode plot of the left and right sides of the ideal sixth-order PPF centered at 2-MHz.	65
4.23	Amplifier used to fix the output voltage of some cells when the switches open.	67
4.24	Bode magnitude plot of the LPF-biquad for several duty-cycles.	67
4.25	Bode magnitude plot of LPF-biquad with F&H and without it for several duty-cycles.	69
4.26	Bode magnitude plot of the second-order PPF with F&H and without it.	69
4.27	Bode magnitude plot of LPF-biquad with F&H and without it for several duty-cycles.	71
4.28	Bode magnitude plots of the sixth-order Butterworth PPF with Nauta's OTA and side LPF for a duty-cycle of 0.5.	71
4.29	Bode magnitude plots of the sixth-order Butterworth PPF with Nauta's OTA for a duty-cycle of 0.25 and 0.75.	72
4.30	Active RC LPF-biquad.	73
4.31	Active RC LPF-biquad F&H.	73

4.32	Active RC LPF-biquad with F&H and without it ideal Bode magnitude plot for several duty-cycles.	74
4.33	Active RC PPF.	74
4.34	Active RC PPF F&H.	75
4.35	Active RC sixth-order Butterworth PPF with F&H and without it ideal Bode magnitude plot for several duty-cycles.	76
4.36	Bode magnitude plot of the left and right sides of the ideal sixth-order PPF. . . .	76
4.37	Active RC LPF-biquad with F&H and without it Bode magnitude plot for several duty-cycles.	77
4.38	Bode magnitude plots of the active RC implementation of the sixth-order Butterworth PPF and side LPF for a duty-cycle of 0.5.	77
4.39	Bode magnitude plots of the active RC implementation of the sixth-order Butterworth PPF for a duty-cycle of 0.25 and 0.75.	78
4.40	MOSFET-C LPF-biquad.	79
4.41	MOSFET-C LPF-biquad F&H.	79
4.42	MOSFET-C LPF-biquad with F&H and without it ideal Bode magnitude plot for several duty-cycles.	80
4.43	MOSFET-C PPF.	80
4.44	MOSFET-C PPF F&H.	81
4.45	MOSFET-C sixth-order Butterworth PPF with F&H and without it ideal Bode magnitude plot for several duty-cycles.	82
4.46	Bode magnitude plot of the left and right sides of the ideal sixth-order PPF centered at IF.	82
4.47	Folded cascode amplifier for MOSFET-C filter.	83
4.48	MOSFET-C LPF-biquad with F&H and without it Bode magnitude plot for several duty-cycles.	83
4.49	Bode magnitude plots of the MOSFET-C implementation of the sixth-order Butterworth PPF and side LPF for a duty-cycle of 0.5.	84
4.50	Bode magnitude plots of the MOSFET-C implementation of the sixth-order Butterworth PPF for duty-cycles of 0.25 and 0.75.	84
5.1	Comparison between g_m -C PPF implementation and the one from A. Emira <i>et. al.</i>	86
5.2	Changing the sampling frequency.	87
5.3	Changing the size of the first transconductor for the frequency translation.	88
5.4	Changing the size of the second transconductor for the frequency translation. . . .	88
5.5	Changing the size of the switches.	89
5.6	Changing the size of amplifier used as load.	89
5.7	Second-order PPF layout	90
5.8	Post-layout and center-frequency tuned Bode magnitude responses of the filter. . .	91

List of Tables

2.1	Comparison between receiver architectures.	25
2.2	IR in PPFs with different orders	33
3.1	Comparison between PPF implementations.	39
3.2	Experimental results for filter with transconductor from Nauta.	44
4.1	Integrator comparison.	56
4.2	Op-amp characteristics.	76
5.1	PPF implementations summary.	85
5.2	Comparison with the Bluetooth specifications.	86
5.3	Layout results.	91

Abbreviations

Abbreviations

AC	Alternating Current
ACS	Adjacent Channel Suppression
ADC	Analog-to-Digital Converter
BPF	Band-Pass Filter
CM	Common-mode
CMOS	Complementary Metal Oxide Semiconductor
CMFB	Common-mode Feedback
CMFF	Common-mode Feed Forward
CMRR	Common-mode Rejection Ratio
DAC	Digital to Analog Converter
DC	Direct Current
DSP	Digital Signal Processor
DT	Duty-cycle
F&H	Filter & Hold
GBW	Gain Bandwidth
GFSK	Gaussian Frequency Shift Keying
HPF	High-Pass Filter
I	In-phase
IC	Integrated Circuit
IF	Intermediate Frequency
IP_3	Third order intercept point
IR	Image-Rejection
IRR	Image-Rejection Ratio
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
OTA	Operational Transconductance Amplifier
OSR	Oversampling Ratio
PAC	Periodic AC
PLL	Phase-Locked Loop
PPF	Polyphase Filter
PSS	Periodic Steady-State
PXF	Periodic Transfer Function
PVT	Process, Voltage and Temperature
Q	Quadrature

Q_L	Loaded Quality
Q_u	Unloaded Quality
RF	Radio Frequency
SAW	Surface Acoustic Wave
S&H	Sample-and-Hold
SSB	Single-Side Band
TRF	Tuned Radio-Frequency
VGA	Variable Gain Amplifier

Chapter 1

Introduction

1.1 Problem statement

When down-converting the signal from radio frequency (RF) to an intermediate frequency (IF), there are always two signals with different frequencies translated to the same frequency value: one is the desired signal and the other is usually called image frequency. These two frequencies are equally distant to the local oscillator (LO) frequency, separated by the double of the IF value.

One of the main problems found in the implementation of wireless receivers is the rejection of the image frequency. In the most classical receiver architecture, the superheterodyne receiver, the image frequency is removed through band-pass or band-rejection filtering prior to the down-conversion. The main drawback of this procedure is the need for unloaded high-quality factors (Q_u) for the devices included in the filter. This represents a severe constrain in terms of integration since semiconductor technologies such as CMOS do not provide sufficiently high- Q_u devices. As so, these filters must be implemented off-chip, therefore increasing the overall cost.

Nowadays, alternative receiver architectures are being used. Direct-conversion receivers eliminate the image-frequency problem by translating the RF signal directly to baseband. However, from this solution other problems arise, such as the LO leakage and DC offsets that are also difficult to solve without recurring to complex compensation circuitry. On the other hand, the wide-band IF architecture tries to circumvent the typical problems of the superheterodyne and the direct-conversion receiver. However, since it uses an high-IF value, it leads to high power consumption, linearity problems and even-order distortion.

The low-IF architecture tries to surpass the problems of the wide-band IF using a lower IF value. This way, the power consumption can be reduced and good levels of integration can still be achieved.

In order to increase the integration level, the image rejection in the low-IF architecture is performed following the down-conversion stage. This avoids the use of high- Q_u devices and allows the use of active devices at much lower frequencies. However, to filter the image signal, other type of filtering operation must be provided. Since quadrature down-converters are often used, the image and the desired signal (at the same frequency value) can be distinguished by their relative phases. Nonetheless, complex filtering is required to perform a filtering in such conditions, such as band-pass filtering at solely one side of the frequency spectrum (asymmetrical filters).

Polyphase filters (PPFs) or complex filters provide for a way to do image rejection on RF receivers. These filters are multi-path asymmetrical filters that perform the filtering in the complex domain, thus making it possible to reject the image frequency at one side of the frequency spectrum in contrast with the typical bandpass circuits that filter equally both sides.

However, since the IF is quite low, in order of the channel bandwidth, the time constants needed for the filter to perform as intended are normally too large. Therefore, this constitutes a problem in terms of area leading to increased prices for the manufacturing of an integrated circuit (IC). As so, techniques for reducing the sizes of the components (normally capacitors) are required.

Moreover, due to typical process deviations, temperature, voltage and component aging, the frequency response of the filters can vary from specifications. Common solutions rely on capacitor or resistor banks, which increases significantly the area for the implementation of a reliable filter.

1.2 Proposed solution

To solve the typical problems of a PPF implementation, the “Filter & Hold” (F&H) technique [1, 2] is proposed to be included within a PPF structure. This technique can be used in filters to reduce the size of the components that define the time constants. This is achieved by adding switches to the filter that are controlled by a clock signal to halt the integration. The duty cycle of the clock defines the size reduction of the components. This also enables for the time constants of the filter to be corrected due to process, voltage and temperature (PVT) variations, by simply changing the duty cycle. One main advantage of the proposed solution is the possibility of simple digital circuitry to perform the required adjustments in an accurate way.

To implement the PPF several approaches can be used, namely based on g_m -C, active RC or MOSFET-C architectures. The g_m -C is one of the most used architectures for filter implementation, since it presents good levels of integration and low-power consumption. The active RC approach is also a good approach since it presents low-noise operation and high dynamic range although requiring significant area for the passive devices. The MOSFET-C approach can be used alternatively, by replacing the resistors of the active RC architecture by MOSFETs working in the triode region. In this work, the F&H technique is explored in all these architectures for the context of a PPF design. It is expected that the F&H presents itself as a potential improvement over other PPFs implementations found in literature.

1.3 Dissertation outline

This document is organized in five chapters as follows:

- Chapter 1: Introduction
- Chapter 2: Background research
- Chapter 3: State of the Art
- Chapter 4: Architecture development
- Chapter 5: Conclusion

On the next chapter the fundamentals of RF receivers are described along with the typical receiver architectures. In between, several ways to achieve image rejection in RF receivers are studied. To finalize this chapter, a study about the theory behind the PPF is presented.

Chapter 3 shows several state-of-the-art implementations of polyphase filters and typical tuning schemes. A brief survey on g_m cells used to design filters is also presented.

Chapter 4 provides information on the F&H technique and its application on PPFs along with the several architecture approaches, tested for the development of the filter for further comparison.

Chapter 5 presents a comparison of the tested architectures providing several simulation results. The conclusion of this dissertation and future work to improve the performance of the filter is presented at the end of this chapter.

Chapter 2

Background research

This chapter introduces the RF architectures commonly used in wireless receiver systems and also several technical issues relative to their performances. First, it is presented the fundamental aspects associated with the down-conversion of an RF signal to a lower frequency. Then, the most typical image-rejection techniques are presented in order to introduce the problem of image suppression in RF receivers. Special emphasis is given to the image problem, introducing the concepts which constitute the basis for the development of the present work. Then, the most common RF architectures are described along with their key issues, particularly in terms of RF circuit integration. In the end, the PPF concept is analyzed, which is the major technical concern of this work.

2.1 Fundamentals of RF Receivers

Basically, a radio receiver is a device able to convert information present in radio waves to a useful form. The first discovery towards radio receivers was made by the Scottish mathematician and physicist James Clerk Maxwell. In 1864, Maxwell formulated the electromagnetic theory of light and mathematically described the radio waves [3]. It was only in 1886 that Heinrich Rudolf Hertz started his experiment to prove the existence of the radio waves and two years later, in 1888, Hertz was able to transmit and receive electromagnetic waves of 5-m and 50-cm [4]. The receiver was a simple piece of wire bent into a circle with a ball in one end and a sharp edge on the other. Whenever the wire circumference was tuned at the same frequency as the spark-gap oscillator, there would be discharge between the two ends of the receiver circuit [5]. When asked about the importance of his discovery, Hertz replied: *“It’s of no use whatsoever... this is just an experiment that proves Maestro Maxwell was right – we just have these mysterious electromagnetic waves*

that we cannot see with the naked eye. But they are there.” [6]. Hertz seemed uninterested about his discovery because, as he said, “I do not think that the wireless waves I have discovered will have any practical application.”

Hertz’s form of a receiver was very primitive and thanks to the invention of Prof. Edward Branly, the “coherer” (a device that detects electromagnetic waves), Alexander Stepanovich Popov was able to build the first radio receiver in 1895 [4]. It was by this time also that Guglielmo Marconi is said to have read about the experiments of Hertz, and started to understand that radio waves could be used for wireless communication. In 1904, Marconi received the Radio patent from the United States Patent Office [7].

One remarkable contribution in the history of wireless receivers was the heterodyne principle introduced by Reginald Fessenden in 1901 [8]. Fessenden suggested that, in a radio receiver, mixing the incoming radio frequency wave with another one locally generated, could in fact result in a different and audible frequency. However, Fessenden was not able to put this principle into practice because of the local oscillator (LO) that still needed further developments. Only later it was possible to build functional heterodyne receivers with the versatility of the electron tubes to operate as oscillators. In this matter, Edwin H. Armstrong had relevant contribution [9, 10], using the electron tubes to build the regenerative receiver that used positive feedback [11]. The RF technology had further developments and was made available already during the World War I.

Another receiver, that replaced the regenerative was the tuned radio-frequency (TRF) receiver. It consisted of three tuned RF amplifiers in cascade followed by a detector and a power amplifier. It was very difficult to operate with this receiver because all the RF amplifiers had to operate at the same frequency. Thus, with the invention of the superheterodyne receiver by Armstrong [12], the TRF became obsolete. The superheterodyne was the first receiver based on the heterodyne principle. Figure 2.1 represents the mixing operation in which the heterodyne principle relies on. In fact, by using a simple multiplication of two signals, different tones can be generated.

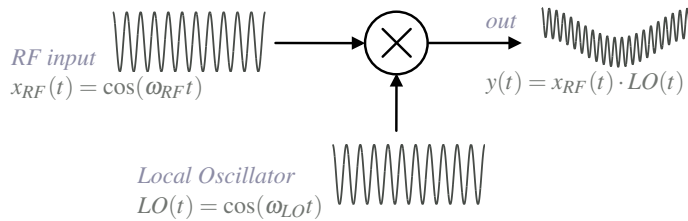


Figure 2.1: Heterodyne principle.

Bearing in mind that $\cos a \cdot \cos b = \frac{1}{2} \cos(a + b) + \frac{1}{2} \cos(a - b)$, one can get the resulting signal:

$$out(t) = \frac{1}{2} \cos [(\omega_{RF} + \omega_{LO})t] + \frac{1}{2} \cos [(\omega_{RF} - \omega_{LO})t] \quad (2.1)$$

The signal spectrum of this operation can be seen in figure 2.2. One can see from this figure that four frequencies result from the convolution of the RF signal and the LO signal. This is because the mixing operation does not preserve the polarity of the difference of the two input frequencies¹. The figure shows the case for low-side injection and high-side injection. Low-side injection is when the LO frequency is lower than the RF input frequency and high-side injection is when the LO frequency is higher than the RF input frequency. Only single tones were considered in this explanation but the same happens no matter what are the input signals.

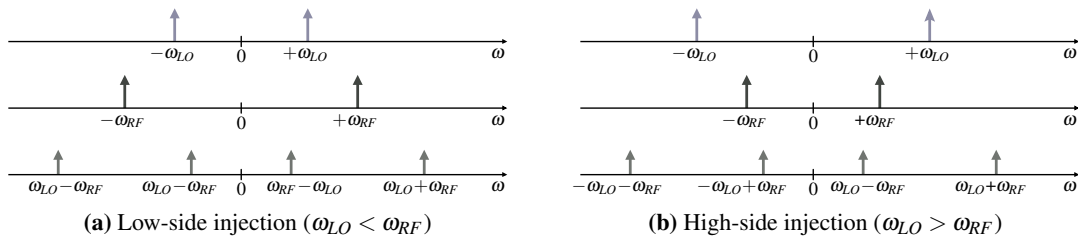


Figure 2.2: Signal spectrum of the heterodyne principle.

There are two very important notions in RF: down-conversion and intermediate frequency (IF). When two signals are mixed, the result of this operation is two signals: one at high-frequency and another one at low-frequency. The reason for mixing two signals at RF is to take advantage that the following required operations can be performed at a lower frequency. This procedure therefore gets the name of down-conversion. After a mixing stage, there is a filter used to suppress the high-frequency components of the mixing procedure in order to leave just the low-frequency part. The resulting low-frequency is named IF. The down-conversion procedure and the respective IF can be seen in figure 2.3.

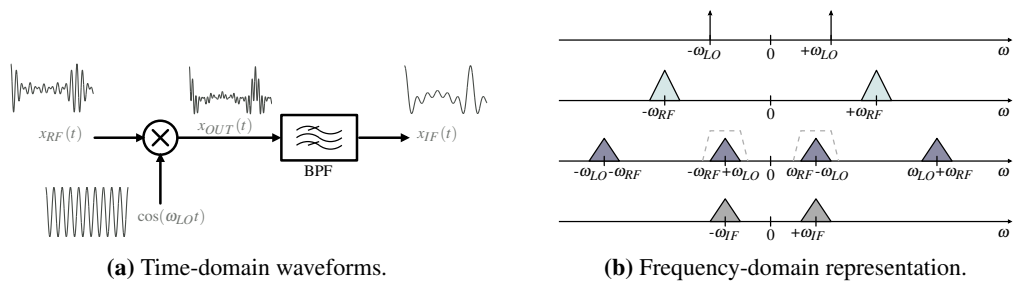


Figure 2.3: Down-conversion.

Although down-conversion is useful, it leads to one of the most critical issues in RF receivers: the image frequency problem. The image is the signal that is distanced from the desired signal by a frequency of $2\omega_{IF}$ that gets down-converted to the same frequency as the desired signal. Figure 2.4 depicts this problem.

¹Note that $\cos(a) = \cos(-a)$.

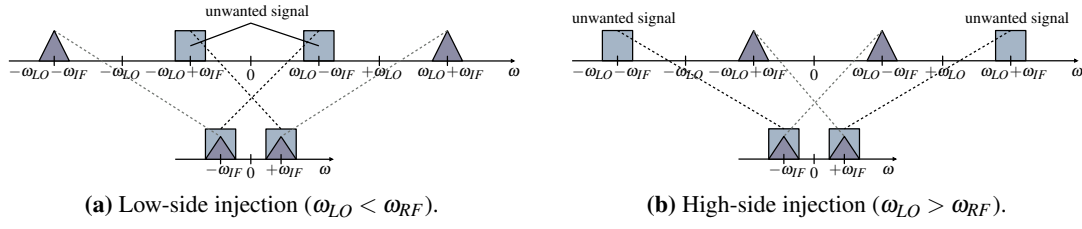


Figure 2.4: Image problem.

As seen in the figure 2.4, the image and the desired signal get overlapped, making it difficult to distinguish them. To solve this problem, each receiver has its own way to perform image rejection. To evaluate the performance of the receiver rejecting the image frequency, a specification in the receivers called image-rejection ratio (IRR), tells how good the image-rejection (IR) is.

Another common problem in RF receivers is the half-IF. Let us assume that in the RF signal, besides the desired band at ω_{RF} , we have an interferer at $\frac{\omega_{RF} + \omega_{LO}}{2}$. When down-converting, if the interferer experiences second order distortion and the LO contains a significant second harmonic as well, then it will result a non-null term at ω_{IF} . Also, the interferer can be translated to $\frac{\omega_{IF}}{2}$ and posteriorly undergoes second-order distortion in the baseband, making it being down-converted to the band of interest [13]. Figure 2.5 depicts this problem.

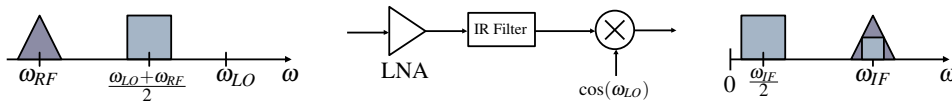


Figure 2.5: Half-IF problem.

The image problem is well-known in wireless communication systems. One way to deal with this problem is to avoid real mixers. That is, since the input is a real signal, let us call it $x_{RF}(t)$, then when multiplied by a single tone the output spectrum $X_{out}(\omega)$ will be symmetrical to DC [14]:

$$x_{OUT}(t) = x_{RF}(t) \cdot \cos(\omega_{LO}t) \Leftrightarrow X_{OUT}(\omega) = \frac{X_{RF}(\omega + \omega_{LO})}{2} + \frac{X_{RF}(\omega - \omega_{LO})}{2} \quad (2.2)$$

However, if the input signal is multiplied by two signals with equal magnitude but different in phase by $\pi/2$ rad, i.e. in quadrature, then the output signal can be considered as a complex signal comprised of an in-phase component $I(t)$ and a quadrature component $Q(t)$, which corresponds to the real and imaginary parts of the signal, respectively:

$$x_{OUT}(t) = I(t) + jQ(t) \quad (2.3)$$

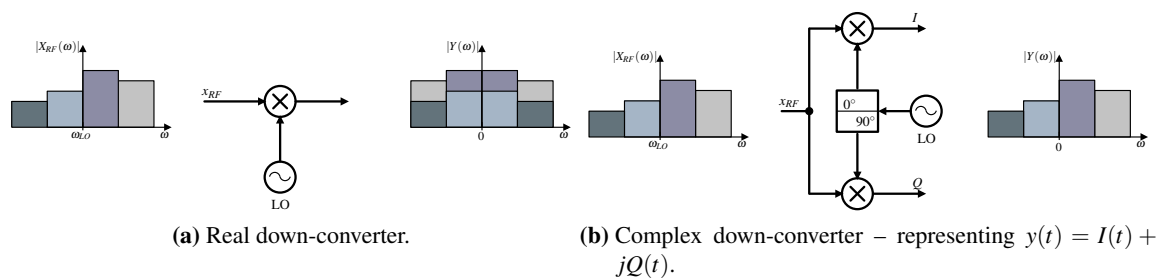


Figure 2.6: Real and complex down-converters.

Now, $x_{OUT}(t)$ can be considered asymmetrical to DC, since it is complex and its spectrum follows a different behavior:

$$x_{OUT}(t) = x_{RF}(t) \cdot e^{j\omega_{LO}t} \Leftrightarrow X_{OUT}(\omega) = X_{RF}(\omega - \omega_{LO}) \quad (2.4)$$

Therefore, the image problem can be overcome since X_{RF} suffers only one shifting in frequency instead of two in the case of multiplication by a real down-converter². This way, the image and the desired signal can be separated by means of down-conversion and complex filtering. Figure 2.6 presents the two types of mixers just mentioned. As can be seen, the output spectrum from the complex mixer is asymmetrical around DC. Along the present document, several techniques will be referred in order to deal with the image-rejection in complex down-conversion.

The RF receivers have typical figures of merit that evaluate its performance. Sensitivity, selectivity and linearity are such evaluation features. Sensitivity is defined as the minimum detectable desired signal strength to obtain a certain bit, frame or package error rate. Being one of the most important specifications, it is given by the overall noise figure of the receiver and processing gain/loss. Linearity is measured based on the third order distortion level of a receiver, which is represented by the third order intercept point (IP_3). The IP_3 is defined as the intersection point of the fundamental signal output magnitude versus the input power characteristic and the third order intermodulation. Selectivity is the characteristic of the receiver that allows the identification of the desired signal at one frequency apart from the rest [15]. For the PPF, being the main target of the present work, the IR is the figure of merit in which we will mainly focus our attention.

²The terms “down-converter” and “mixer” will be used interchangeably during this text.

2.2 Image-Rejection techniques

There are two fundamental methods used to suppress the image signal. One relies on filtering the image signal previously to down-conversion. This filter requires minimum loss in the RF passband and high-attenuation for the image frequencies. The other method relies on filtering the image after the down-conversion. Some classical IR schemes are based on Hartley and Weaver architectures that will be described next. The IRR will be also derived for a typical quadrature down-converter.

2.2.1 Hartley IR

This IR architecture has been idealized by Hartley in 1928 for single-side band (SSB) signals [16]. The block diagram of the Hartley architecture is shown in figure 2.7. The incoming signal is first down-converted through complex mixing with I and Q signals generated by an LO and a 90° phase-shifter. Then, the resulting signals are phase-shifted to attain a phase difference of 90° . When added at the output, the image frequency is completely eliminated.

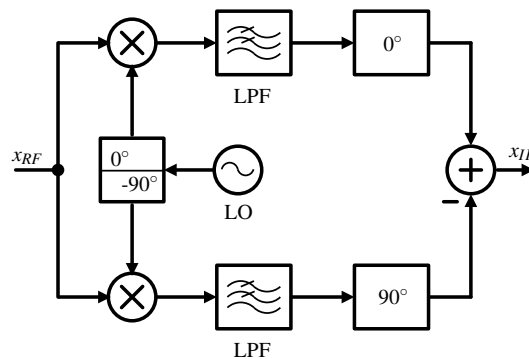


Figure 2.7: Block diagram of hartley image reject receiver.

In order to better explain the operation of Hartley IR scheme, let us present the following example. Suppose that the input RF signal is given by:

$$x_{RF}(t) = A_{sig} \cos[(\omega_{LO} + \omega_{IF})t] + A_{img} \cos[(\omega_{LO} - \omega_{IF})t] \quad (2.5)$$

where the first term is the intended signal and the second term is its image. The present case represents low-side injection, therefore the desired signal has frequency $\omega_{RF} = \omega_{LO} + \omega_{IF}$ and the image frequency is $2\omega_{IF}$ apart. Let us assume the quadrature signals locally generated at the mixer inputs written as³:

³We will adopt the LO quadrature signals as $\cos(\omega_{LO}t)$ and $-\sin(\omega_{LO}t)$ for clearance on other topics that will be described latter along this dissertation.

$$LO_I(t) = \cos(\omega_{LO}t) \quad (2.6)$$

$$LO_Q(t) = -\sin(\omega_{LO}t) \quad (2.7)$$

At the outputs of the mixers, taking into account the trigonometric identities one gets:

$$I_1(t) = \frac{A_{sig} + A_{img}}{2} \cdot \cos(\omega_{IF}t) + \frac{A_{img}}{2} \cdot \cos[(2\omega_{LO} - \omega_{IF})t] + \frac{A_{sig}}{2} \cdot \cos[(2\omega_{LO} + \omega_{IF})t] \quad (2.8)$$

$$Q_1(t) = \frac{A_{sig} - A_{img}}{2} \cdot \sin(\omega_{IF}t) - \frac{A_{img}}{2} \cdot \sin[(2\omega_{LO} - \omega_{IF})t] - \frac{A_{sig}}{2} \cdot \sin[(2\omega_{LO} + \omega_{IF})t] \quad (2.9)$$

Then, the low-pass filter (LPF) attenuates the high-frequency components around $2\omega_{LO} \pm \omega_{IF}$, leading to:

$$I_2(t) = \frac{A_{sig} + A_{img}}{2} \cdot \cos(\omega_{IF}t) \quad (2.10)$$

$$Q_2(t) = \frac{A_{sig} - A_{img}}{2} \cdot \sin(\omega_{IF}t) \quad (2.11)$$

After this step, the Q channel passes through a 90° shifter, meaning that the Q_2 signal will be delayed $\frac{\pi}{2}$ rad in its phase, while the in-phase counterpart remains the same since there is no phase-shifting required:

$$I_3(t) = \frac{A_{sig} + A_{img}}{2} \cdot \cos(\omega_{IF}t) \quad (2.12)$$

$$Q_3(t) = \frac{A_{sig} - A_{img}}{2} \cdot \sin(\omega_{IF}t - \pi/2) = -\frac{A_{sig} - A_{img}}{2} \cdot \cos(\omega_{IF}t) \quad (2.13)$$

In the end, when the two channels are subtracted, from (2.12)–(2.13), the image signal is eliminated. A graphical representation of this example can be seen in figure 2.8.

$$x_{IF}(t) = A_{sig} \cos(\omega_{IF}t) \quad (2.14)$$

The main problem of this architecture is its sensitivity to mismatches in the gain and phase of the two channels, which makes the image suppression incomplete. Also, broadband phase-shifters are difficult to achieve at high-frequencies.

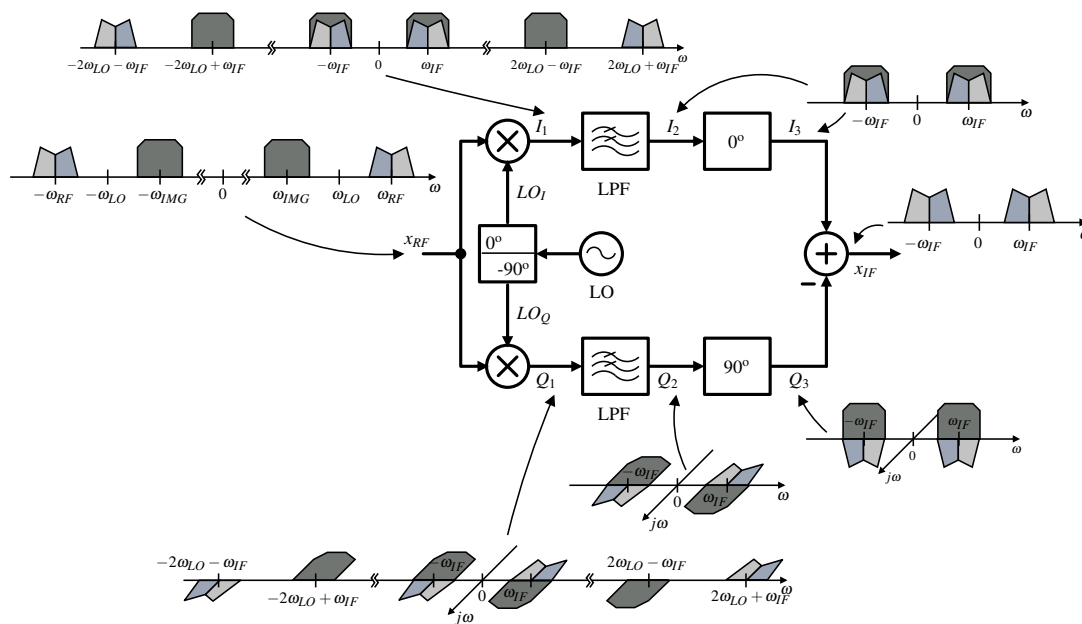


Figure 2.8: Graphical representation of Hartley image-rejection exemplified.

2.2.2 Weaver IR

Another possibility, and perhaps the most common for image suppression is the Weaver architecture, first used for SSB signal generation [17]. The block diagram for this architecture is represented in figure 2.9.

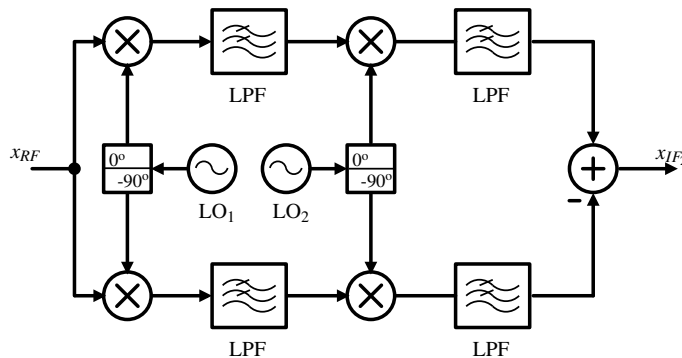


Figure 2.9: Block diagram of the weaver image reject receiver.

The difference between this architecture and the previous one is that instead of having the phase-shifter in the Q channel, there is another LO in both channels, which will equivalently perform the phase-shifting required to eliminate the image signal.

Let us assume the same input signal as considered in equation (2.5) and the LO quadrature signals as in equations (2.6)–(2.7). Considering low-side injection, the output of the first complex down-conversion and the respective low-pass filtering is identical to the Hartley architecture given

by equations (2.10)–(2.11). Now, for the second down-conversion stage, let us admit low-side injection such as $\omega_{IF_2} = \omega_{IF_1} - \omega_{LO_2}$. At the output of the second down-conversion with its low-pass filtering, one gets:

$$I_4(t) = \frac{A_{sig} + A_{img}}{4} \cdot \cos(\omega_{IF_2}t) \tag{2.15}$$

$$Q_4(t) = \frac{A_{img} - A_{sig}}{4} \cdot \cos(\omega_{IF_2}t) \tag{2.16}$$

Subtracting both outputs will lead to image cancellation:

$$x_{IF_2}(t) = \frac{A_{sig}}{2} \cdot \cos(\omega_{IF_2}t) \tag{2.17}$$

The graphical representation of this architecture can be seen in figure 2.10. One problem common to the Hartley receiver is I/Q mismatching that can lead to degradation of the image rejection.

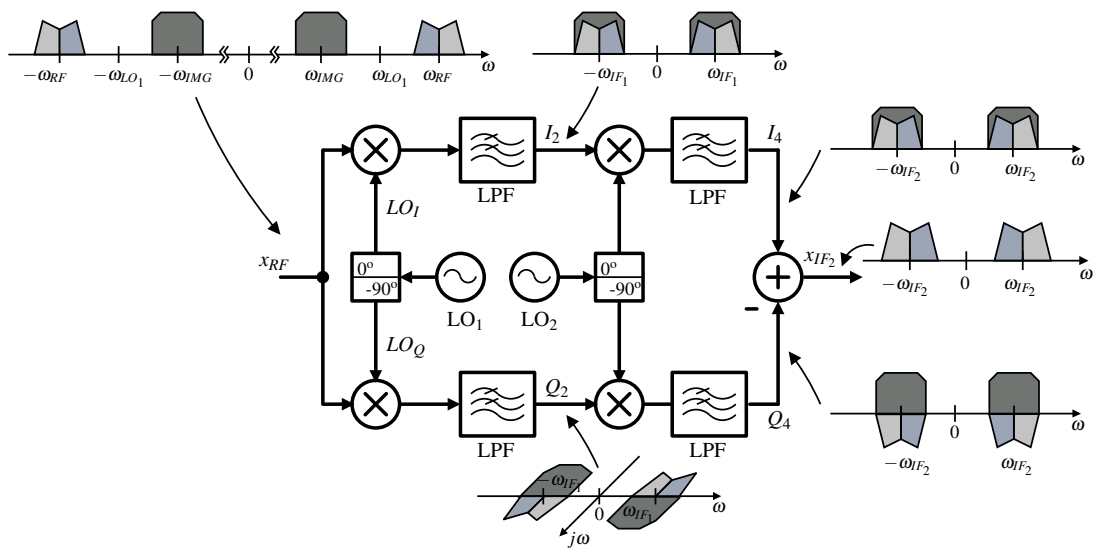


Figure 2.10: Graphical representation of Weaver receiver.

2.2.3 Double Quadrature Mixing

Double quadrature mixing is another way of performing down-conversion taking into account the IR. Comparing to the conventional quadrature mixing, this topology requires even more mixers, i.e. four down-conversion mixers are needed. The output signals are then combined two-by-two. The block diagram of a double quadrature mixer topology can be seen in figure 2.11.

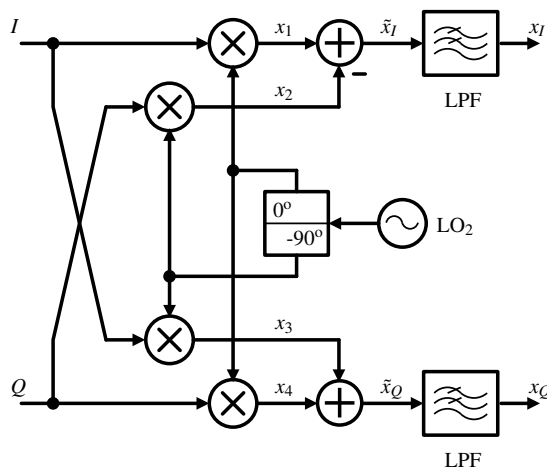


Figure 2.11: Block diagram of the double quadrature mixing topology.

It can be seen in the figure 2.11 that the double quadrature mixing requires a previous quadrature down-conversion in order to be used correctly. To better understand its functionality we will describe it mathematically as follows. Let us assume an input signal given by a signal and its image in a low-side injection scheme, e.g. the signal given previously by equation (2.5). The output of the first down-conversion is therefore similar to the previously determined signals after low-pass filtering as given by (2.10)–(2.11) in the Hartley technique. For the second down-conversion, i.e. the down-conversion shown in figure 2.11, it will be assumed here that $\omega_{LO_2} = \omega_{IF_1}$ in order to perform direct conversion this way avoiding secondary image problems. The quadrature signals for the second local oscillator are given by:

$$LO_{I_2}(t) = \cos(\omega_{IF_1}t) \quad (2.18)$$

$$LO_{Q_2}(t) = -\sin(\omega_{IF_1}t) \quad (2.19)$$

The signals x_1 and x_2 represented in figure 2.11 are identical to the resulting signals in the Weaver architecture, although are repeated here for convenience. The other signals, i.e. x_3 and x_4 are easily determined as follows.

$$x_1(t) = \frac{A_{sig} + A_{img}}{4} \cdot \left[1 + \cos(2\omega_{IF_1}t) \right] \quad (2.20)$$

$$x_2(t) = \frac{A_{sig} - A_{img}}{4} \cdot \left[1 - \cos(2\omega_{IF_1}t) \right] \quad (2.21)$$

$$x_3(t) = \frac{A_{sig} + A_{img}}{4} \cdot \sin(2\omega_{IF_1}t) \quad (2.22)$$

$$x_4(t) = \frac{A_{sig} - A_{img}}{4} \cdot \sin(2\omega_{IF_1}t) \quad (2.23)$$

It results then:

$$\tilde{x}_I(t) = x_1(t) - x_2(t) = \frac{A_{sig}}{2} + \frac{A_{img}}{2} \cdot \cos(2\omega_{IF_1}t) \quad (2.24)$$

$$\tilde{x}_Q(t) = x_3(t) + x_4(t) = -\frac{A_{img}}{2} \cdot \sin(2\omega_{IF_1}t) \quad (2.25)$$

Following the low-pass filtering, results then:

$$x_I(t) = \frac{A_{sig}}{2} \quad (2.26)$$

$$x_Q(t) = 0 \quad (2.27)$$

In fact, the I and Q components are separated in each respective branch. Figure 2.12 shows a graphical representation of an example of the spectrum along the receiver blocks.

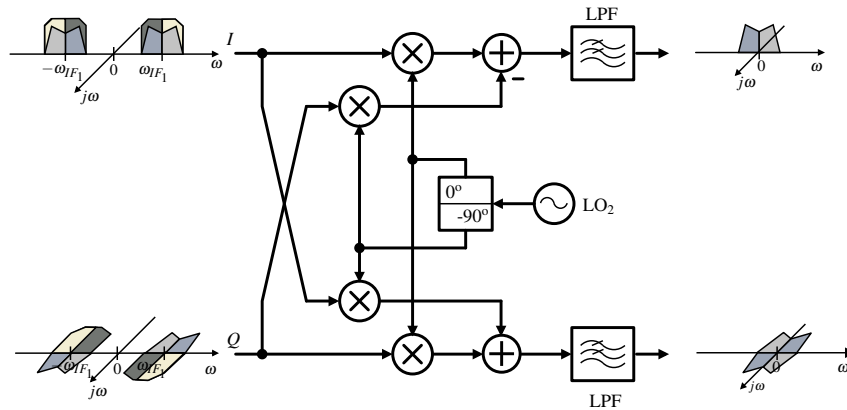


Figure 2.12: Graphical representation of the double quadrature mixing topology.

One can notice that this scheme differs from the Weaver approach in which the I and Q components are present in both branches. In this receiver the image signal is removed from both paths previously to sum of I - Q outputs. In the end, this double quadrature mixing can be seen as two Weaver architectures.

One particular aspect about this architecture is that it is not influenced by the first down-conversion mismatch if there is no mismatch in the LO_2 from it and vice-versa, although mismatches in both results in lower suppression of the image signal [18]. Comparing to other techniques, this architecture has some drawbacks concerning higher power consumption and larger area.

2.2.4 Image-Rejection Ratio

In this section it will be presented a study relative to the performance measurement in terms of IR. The IRR is most of the times used as specification for certain communication standards [19]. The mismatches, both in amplitude and phase, lead to degradation in image suppression for receivers using complex mixers. Considering the quadrature down-converter in figure 2.13, let us write the quadrature signals locally generated as:

$$LO_I(t) = A_{LO} \cdot \cos(\omega_{LO}t) \quad (2.28)$$

$$LO_Q(t) = -(A_{LO} + \Delta A_{LO}) \cdot \sin(\omega_{LO}t + \Delta\theta) \quad (2.29)$$

where ΔA_{LO} denotes the absolute error in the LO amplitude, and $\Delta\theta$ represents its error in terms of phase that affects one side of the I/Q down-converter.

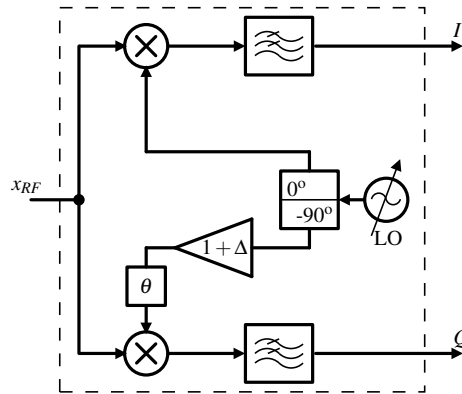


Figure 2.13: Generic quadrature down-converter.

Considering a given signal $x_{RF}(t)$ at the both mixers inputs, the output can be written as:

$$x_{OUT}(t) = x_{RF}(t) \cdot \left[A_{LO} \cdot \cos(\omega_{LO}t) - j(A_{LO} + \Delta A_{LO}) \cdot \sin(\omega_{LO}t + \theta) \right] \quad (2.30)$$

$$= x_{RF}(t) \cdot A_{LO} \cdot \left[\cos(\omega_{LO}t) - j \varepsilon \cdot \sin(\omega_{LO}t + \theta) \right] \quad (2.31)$$

where the imbalance between both Q and I branches is defined by:

$$\varepsilon = \frac{A_{LO} + \Delta A_{LO}}{A_{LO}} \quad (2.32)$$

Equation (2.31) can also be written in the following exponential complex form:

$$x_{OUT}(t) = x_{RF}(t) \cdot A_{LO} \cdot \left[\frac{e^{j\omega_{LO}t} + e^{-j\omega_{LO}t}}{2} - j \varepsilon \cdot \frac{e^{j(\omega_{LO}t + \theta)} - e^{-j(\omega_{LO}t + \theta)}}{2j} \right] \quad (2.33)$$

$$= \frac{x_{RF}(t) \cdot A_{LO}}{2} \cdot \left[(1 - \varepsilon \cdot e^{j\theta}) e^{j\omega_{LO}t} + (1 + \varepsilon \cdot e^{-j\theta}) e^{-j\omega_{LO}t} \right] \quad (2.34)$$

The power rejection obtained from the frequency translations defined in (2.34) defines the IRR as follows:

$$IRR_{dB} = 10 \log_{10} \left(\frac{|1 + \varepsilon \cdot e^{-j\theta}|}{|1 - \varepsilon \cdot e^{j\theta}|} \right) = 10 \log_{10} \left(\frac{(1 + \varepsilon \cdot e^{-j\theta})(1 + \varepsilon \cdot e^{j\theta})}{(1 - \varepsilon \cdot e^{j\theta})(1 - \varepsilon \cdot e^{-j\theta})} \right) \quad (2.35)$$

$$= 10 \log_{10} \left(\frac{\varepsilon^2 + 1 - 2\varepsilon \cos(\theta)}{\varepsilon^2 + 1 + 2\varepsilon \cos(\theta)} \right) \quad (2.36)$$

Figure 2.14a shows a plot of equation (2.36) for several values of θ and ε . From equation (2.36) one can also define θ as:

$$\theta = \cos^{-1} \left(\frac{\varepsilon^2 + 1}{2\varepsilon} \cdot \frac{10^{-\frac{IRR_{dB}}{10}} - 1}{10^{-\frac{IRR_{dB}}{10}} + 1} \right) \quad (2.37)$$

Figure 2.14b represents a plot of equation (2.37) for constant values of IRR. Several regions for the same IRR can be identified in terms of phase differences and different magnitude imbalances between I and Q branches.

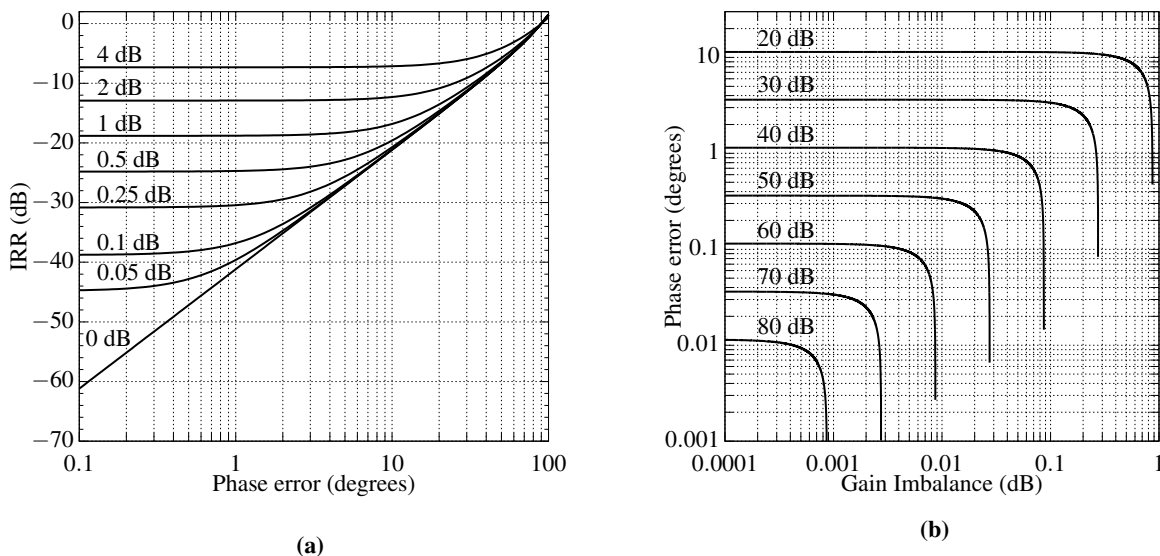


Figure 2.14: Plots for constant ϵ in terms of IRR and θ , and constant IRR for different θ and ϵ .

Normally, the IR receivers have an IRR between 30 and 40-dB, meaning that there is a possible combination of 0.2 to 0.6-dB gain mismatch and 5° to 15° of phase imbalance. However, most of the RF applications nowadays need a IRR around 80-dB, thus making it impossible to achieve image rejection without additional filtering [13].

2.3 Receiver Architectures

Next the most common RF receiver architectures are presented. These architectures are categorized in terms of relative value of IF. First, the most classical architecture is described, that is, the superheterodyne receiver. Then, the homodyne, the wide-band IF and the low-IF are presented together with their main performance features, which are further compared in a final section.

2.3.1 Superheterodyne

The superheterodyne was conceived in 1918 by Edwin Armstrong [12] and it has been one of the most used architecture over the last decades. The typical block diagram of this architecture can be seen in figure 2.15. It shows a dual-IF conversion, meaning that it has two frequency down-conversions stages in the process. It can have multiple down-conversions until it reaches baseband, but this configuration is the most typical one. The value of the first IF is quite high in this architecture, with its value being at least 30-MHz and sometimes over 100-MHz [19]. Theoretically, its value should be higher than twice the bandwidth of all channels of the communication system.

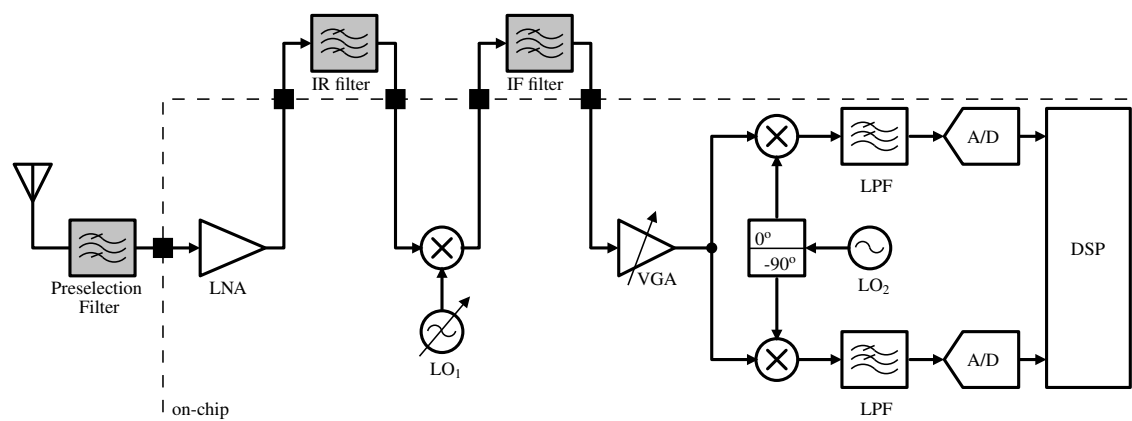


Figure 2.15: Block diagram of the heterodyne architecture.

The shadowed blocks shown in figure 2.15 are normally implemented as high- Q external components⁴, which means that this receiver cannot feature good levels of integration in the context of integrated circuit implementations. This is because of the unavailability of high- Q inductors in common IC technologies. However, not really everything is bad from having external blocks. The results are good sensitivity and good selectivity in terms of typical performances for implementations of this architecture [20].

Based on the figure 2.15, the signal flow in the heterodyne receiver can be described as follows. The RF signal received at the antenna is firstly filtered using a preselection filter. The preselection filter is a band-pass filter (BPF) used to remove the signal energy that is out of band as well as some part of the received noise. Next, the signal is amplified by the low-noise amplifier (LNA) to achieve a good sensitivity in the receiver. It follows the IR filter usually implemented as a surface acoustic wave (SAW) filter, which typically are lossy filters. The IR filter removes the image signal and further suppresses other interference signals. Since this block is normally implemented as an external component, it requires the LNA to drive the $50\text{-}\Omega$ input impedance of the filter, leading to several trade-offs between the gain, noise figure, stability and power dissipation in the LNA [13]. As referred previously, the need for this kind of filter is due to the narrow-bandwidth filtering requirement in this architecture, i.e. high- Q filters, which is not attainable using typical on-chip components.

The mixer performs the down-conversion to IF. The frequency synthesizer produces a variable LO at RF to select the desired channel. This relatively high-frequency channel selection demands good performance synthesis of the LO, therefore requiring also discrete components to obtain the needed high- Q tuning [21]. The IF filter removes out-of-channel signals. Hence, it is also required to be implemented as a filter with high-selectivity, in order to provide good suppression of the bands apart from the desired one. The variable gain amplifier (VGA) that follows the IF filter

⁴Note that since $Q = f_{IF}/B$, for the same bandwidth B results in high- Q requirements when using a high IF values, which is the case of the superheterodyne receiver.

reduces the distortion and dynamic range requirements for the next blocks. The second down-conversion is performed in I and Q channels, translating the signal to baseband. An LPF is used to suppress the unwanted mixed products as well as other interferer signals. In the end, the signal is digitized by the analog-to-digital converter (ADC) to provide the digital data input to a digital signal processing (DSP) block. Because the signal is down-converted in I and Q channels, there will be inherently I/Q mismatches that can be responsible for degrading the bit error rate.

To avoid the IR filter, an IR front-end can be used. That is, instead of a real mixer, a complex mixer can be used, which comprises two mixers. However, it results in higher I/Q matching requirements [19], which are already difficult to attain in low-frequency regimes.

2.3.2 Homodyne

The homodyne architecture was first considered in the 1920s, but its first practical applications took place only in 1947 for a measuring instrument [22]. A possible block diagram of this architecture can be seen in figure 2.16.

The homodyne receiver is different from the heterodyne because of the translation to the baseband that is done in a single down-conversion step, making its design simpler and integration more attractive. The only block that is normally external is the preselection filter. The LO frequency is the same as the RF input, therefore the image problem is virtually solved. That is why this architecture is also known in literature as direct-conversion or zero-IF. With the signal at zero frequency and no image problem, the channel selection can be performed by low-pass filtering, allowing good selectivity, good gain and phase responses. On the other hand, its sensitivity is degraded by several system dependent issues that will be discussed next.

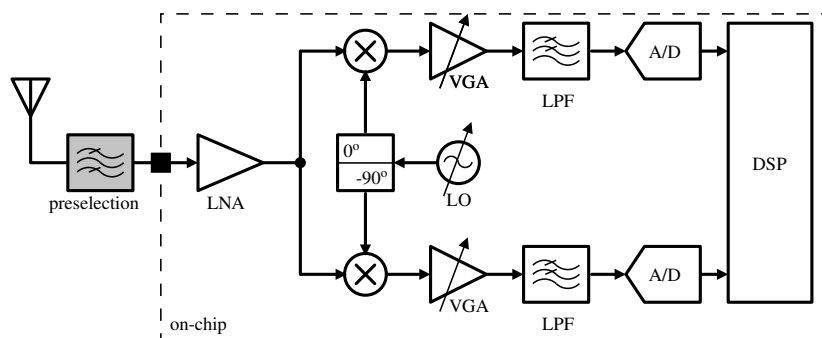


Figure 2.16: Block diagram of homodyne architecture.

- **LO self-mixing and DC Offsets**

This is probably the most serious problem usually found in homodyne receivers [23]. Figure 2.17 represents this problem, which is derived from the LO frequency being the same as the

RF. This is called LO self-mixing because some of the signal from the LO might go back due to capacitive and substrate coupling, being then amplified by the LNA and down-converted to DC when mixing with LO, appearing in the desired signal after. This problem gets worse if self-mixing varies with time, which is when the LO leaks to the antenna and is reflected from moving objects back to the receiver or radiates to other receivers and becomes an interferer [23]. Another possibility for the exhibition of this effect comes from the finite isolation from the LNA and the LO, where a strong interferer can phase-modulate the LO and self-mix, getting down-converted to baseband [24]. Actually, this is not a problem just for the homodyne architecture, it is also found in the superheterodyne receiver. However in homodyne architectures such effect is much more severe [25].

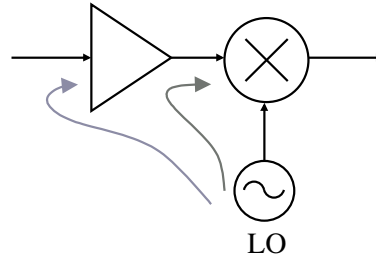


Figure 2.17: LO self-mixing causing DC offset.

- **I/Q Mismatch**

The signal in the homodyne receiver is down-converted into I and Q channels. These channels have their own amplifiers and filters, which makes difficult to maintain perfect balance in magnitude and phase between both paths, corrupting the signal constellation and increasing the bit error rate [20]. This problem also exists in other architectures.

- **Even-Order Distortion**

This can be a big threat if the distortion is not low enough. Let us consider the case where we have device with weak linearity represented by:

$$y(t) = y_1(t) + y_2(t) = a_1x(t) + a_2x^2(t) \quad (2.38)$$

and a two strong narrow-band interferer given by $x(t) = A \cos \omega_a t$ and $B \cos \omega_b t$. When the interferer passes through the device, we get second-order distortion plus high-frequency components:

$$y_2(t) = a_2 \cdot (A \cos \omega_a t + B \cos \omega_b t)^2 = a_2 \cdot \frac{A^2 + B^2}{2} + a_2 \cdot AB \cos(\omega_a - \omega_b) \quad (2.39)$$

It can be seen from equation (2.39) that this causes a DC offset proportional to the coefficient a_2 [15].

- **Flicker Noise**

Flicker noise is also known as $1/f$. Since the down-converted spectrum extends to zero-valued frequency, the flicker noise can highly degrade the signal in the homodyne architecture [26].

2.3.3 Wide-band IF

The wide-band IF architecture was firstly proposed to reduce the problems of the image signal or direct conversions to baseband. In the beginning, this architecture was called quasi-IF [27]. The typical block diagram of this architecture can be seen in figure 2.18. It consists on a dual conversion architecture with the same criteria for the first IF as the superheterodyne.

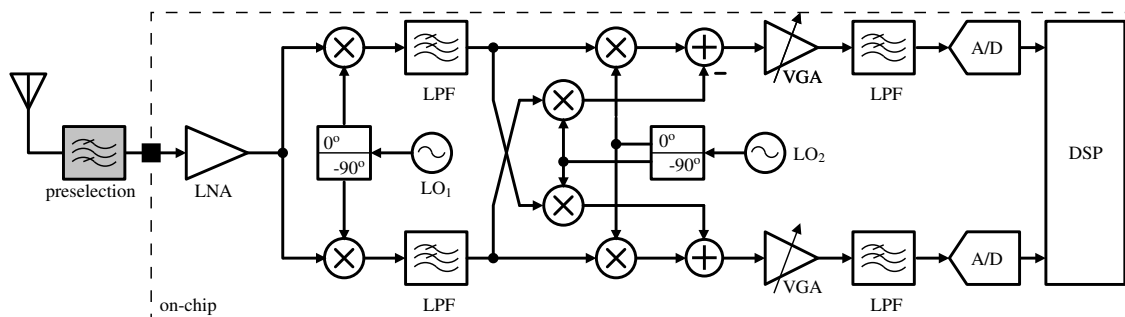


Figure 2.18: Block diagram of a Wide-band IF receiver.

In fact, the first IF stage is identical for both architectures when the superheterodyne receiver is designed with an IR front-end. The first down-conversion takes place after the preselection and amplification of the RF signal. The typical value for the IF in this architecture is normally higher than 100-MHz [19]. As shown in figure 2.18, only the preselection filter is implemented normally with an external component. Therefore, this architecture is well-suited for integration with IC technologies. In comparison to the superheterodyne architecture, the integration is better, although the wide-band IF has a lower sensitivity and selectivity [21]. Also, due to the shared similarities with the superheterodyne receiver, the wide-band IF architecture also suffers also from the half-IF problem.

Like in other architectures, the down-conversion is performed in I and Q channels. After the first down-conversion, an LPF is used to suppress the up-converted product due to the down-conversion operation. The second down-conversion is performed by complex mixing from IF to baseband, using a tunable channel-select frequency-synthesizer. In this down-conversion step, adding the outputs of the real multipliers in pairs, cancels the image frequencies leaving just the desired channels [20]. This technique, called double quadrature down-conversion, as been

described previously in this document as an IR scheme. However, if the signal is not down-converted directly to baseband in the second down-converter stage, it suffers also from secondary image problem [13]. This architecture is not restricted to be used with double quadrature down-conversion. Other techniques can be used instead of this scheme to perform IR and direct down-conversion in the second down-converter stage.

The wide-band topologies transfer the problems of the direct conversion just mentioned into the second down-conversion. When compared with the homodyne receiver, the big difference is that the frequency conversion (or operation frequency) is scaled down by a factor of 2 to 20 [19]. Also, channel selection takes place in the same way as in the homodyne architecture. Nonetheless, the wide-band architecture solves some typical problems found in the homodyne architecture, as further described.

In the first down-conversion, as shown in figure 2.18, the LO_1 and the RF frequency are different thus minimizing the time varying DC offsets and the LO leakage. In the second down-conversion stage, since the LO_2 frequency is lower, it is also easier to design the frequency synthesizer responsible for generating the signal LO_2 that is responsible for selecting the channel to be received. Therefore, the performance of this oscillator can be significantly better. Still in the second down-conversion, although the LO_2 is the same as the IF, the DC offsets are almost constant and can be canceled using adaptive signal processing methods [20].

Channel selection is performed after the second down-conversion. Therefore, this mixers stage constitutes the most critical part since it has to handle all the channels, meaning that linearity constitutes a major concern. At last, the wide-band architecture also suffers from even order distortion and flicker noise almost in the same way the homodyne architecture.

2.3.4 Low-IF

The idea behind the low-IF architecture is to combine the advantages of the heterodyne and homodyne architectures, like in the wide-band, preserving the performance in selectivity and sensibility. The block diagram of this architecture can be seen in figure 2.19. It shows a dual conversion topology for this architecture [28]. However, it is not the only possibility of implementation, since there is also the chance of having only a single conversion if demodulation circuits are implemented at IF operation – which is reasonably low when compared to other architectures.

As in the wide-band architecture, the only normally external block is the preselection filter, allowing a good integration level for this architecture. The value of the IF in this architecture is typically chosen from one to about two times the channel bandwidth [29]. Choosing a lower IF will relax the image rejection requirements and avoids the half-IF problem, whereas a high-IF will lower the flicker noise and the self-mixing will be reduced [19].

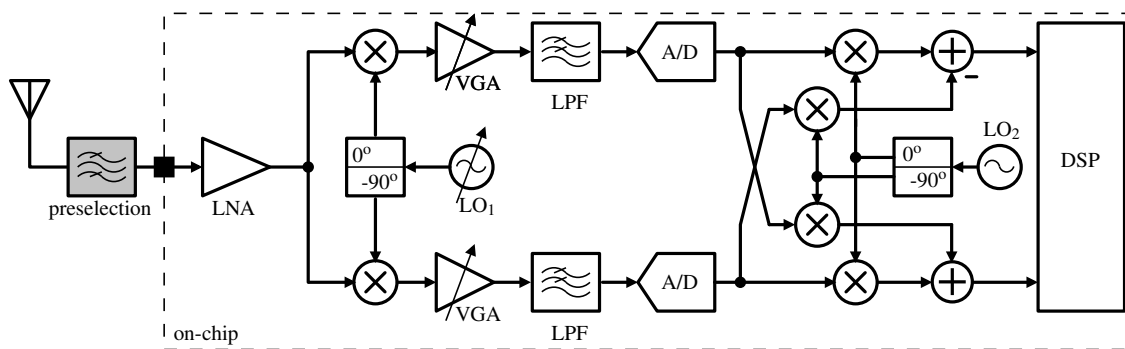


Figure 2.19: Block diagram of a low-IF receiver.

The channel selection is performed following the first down-conversion. It can be implemented using a variable LO, i.e. the signal LO_1 as shown in figure 2.19. For the present case it is followed by an LPF and an ADC, which converts the signal into the digital domain for post down-conversion to baseband and demodulation in the DSP. The LPF must be designed according to the fixed bandwidth of the desired channel⁵. The signal path to the ADC can be AC-coupled, therefore not requiring a complicated DC-offset cancellation circuit.

The ADC demands a resolution higher than the one found in the wide-band architecture [20]. This requirement is due to both the desired signal and the image still being present at this stage, whereas the analog-to-digital conversion in the wide-band IF is performed only after image rejection of the second down-conversion stage, i.e. at baseband. In the low-IF architecture, despite the same frequency value, the different phases of the desired signal and its image lead to time-varying envelopes that demand high-resolution in order to correctly sample the signals for further image-rejection in the digital domain.

The IR mixer is implemented in digital domain and in the case of figure 2.19 it uses a double quadrature down-conversion like in wide-band architecture previously presented [30]. This is not an unique solution to achieve image-rejection. This can also be implemented by using polyphase BPF at low-IF prior to the analog-to-digital conversion [31]. A good thing of having the IR mixer implemented in the digital domain is that it will not have any I/Q mismatches, although at the inputs of the ADC the imbalances of I and Q can be around 0.5 to 0.75-dB in amplitude and 3° to 5° in phase [15]. These imbalances can be corrected using adaptive techniques [32].

The main problem of this architecture is that the IF value is so low that the image-band and the desired signal are very close, making it difficult to do the image suppression by using any passive BPF without degrading the receiver sensitivity. Finally, the low-IF architecture is not immune from the half-IF problem due to the even order distortion.

⁵Although it might be preferable to use a BPF to remove static DC offsets.

2.3.5 Comparison of architectures

Along the previous sections, different receiver architectures have been described in terms of basic operation and performance features. The superheterodyne requires external components with high- Q values. This architecture, once famous, has been depreciated in last generation of receivers due to the disadvantage of low-level of integration.

Meanwhile, other architectures received increased attention during last decades. The wide-band IF relies in a topology similar to the superheterodyne. The great difference is that in the former case the IR and channel selection are performed in the second down-conversion stage, leading to significant advantages in terms of integration.

Homodyne and low-IF architectures are also well-suitable for integration. The homodyne receiver, although simple in topology, demands additional circuitry for compensation of second-order effects, such as DC-offsets. The low-IF tries to circumvent such issues by using an IF value slightly different from zero and performing image-rejection with particular schemes. Table 2.1 shows a summary of the main benefits and drawbacks of each architecture.

Architecture	Integration	I/Q mismatch	Image-Rejection
Superheterodyne	×	×	×
Homodyne	✓	×	✓
Wide-band IF	✓	×	×
Low-IF	✓	✓	×

Table 2.1: Comparison between receiver architectures.

2.4 Polyphase Filters

PPFs, also known as complex filters, are filters that are typically used for IR. Since these filters artificially work in the complex domain, its resulting frequency response is not symmetric to DC. Asymmetric polyphase networks were first used in audio applications for generating quadrature signals by Gingell [33]. Latter, these circuits have reborn when introduced in RF circuits by Michiel Steyaert [34].

The PPF can be distinguished in two basic categories: passive and active. Sequence symmetric polyphase networks constitute the passive implementation of complex filters. Although PPF networks are a good way to achieve high IRR [18], unfortunately they present limited selectivity. That is, the suppression of adjacent channels is not high enough, specially in the case of strong folded-back interferences. This way, extra filtering is required in order to eliminate the adjacent

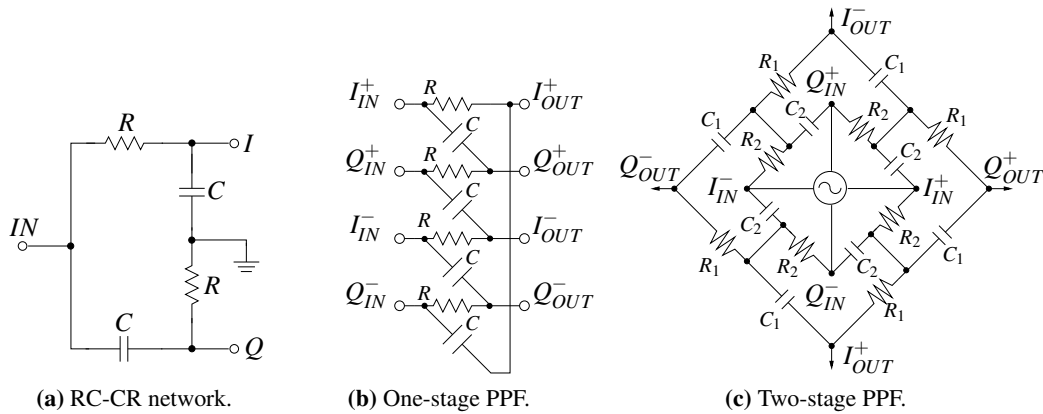


Figure 2.20: Examples of passive PPF stages.

channel signals. Also, the input impedance of the passive PPFs is low, which represents significant load values to the mixers outputs, thus deteriorating the linearity and efficiency.

Figure 2.20 shows several passive PPF networks, differing in order. Using RC-CR networks one can get two different filters, one high-pass filter (HPF) and the other LPF. At the cut-off frequency the outputs are phase-shifted by 90° , since at cut-off frequency the phase of the outputs are $\pm 45^\circ$. However, this phase-shifting is only attainable near at one frequency, i.e. the 3-dB cut-off frequency f_c . Figure 2.21 presents the transient and AC responses of an RC-CR network.

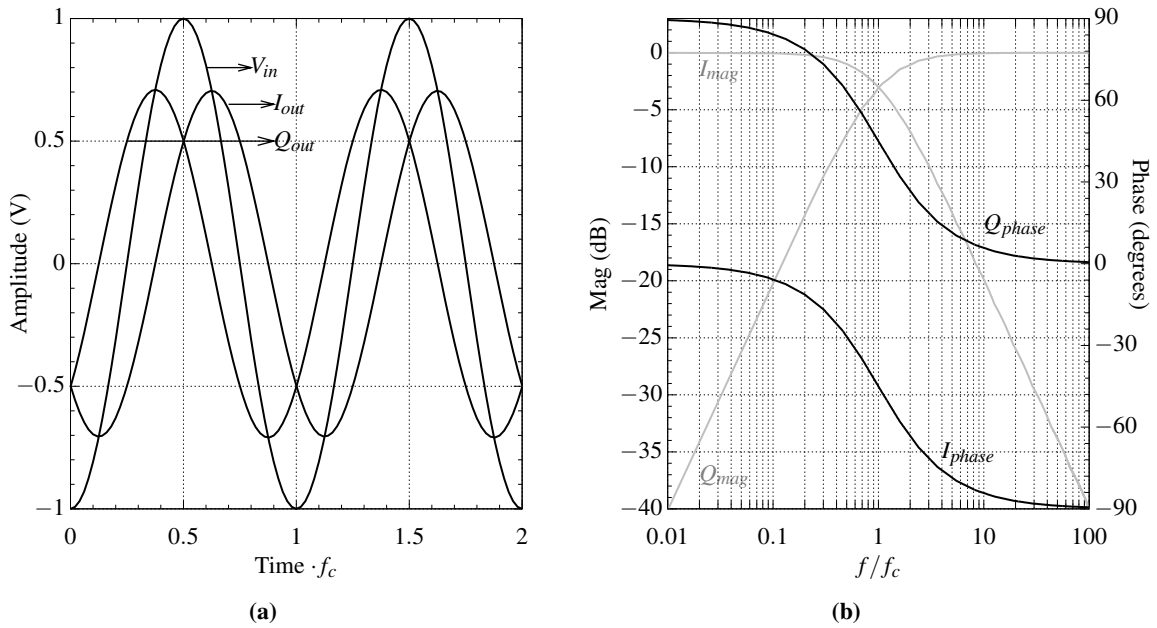


Figure 2.21: RC-CR network analysis.

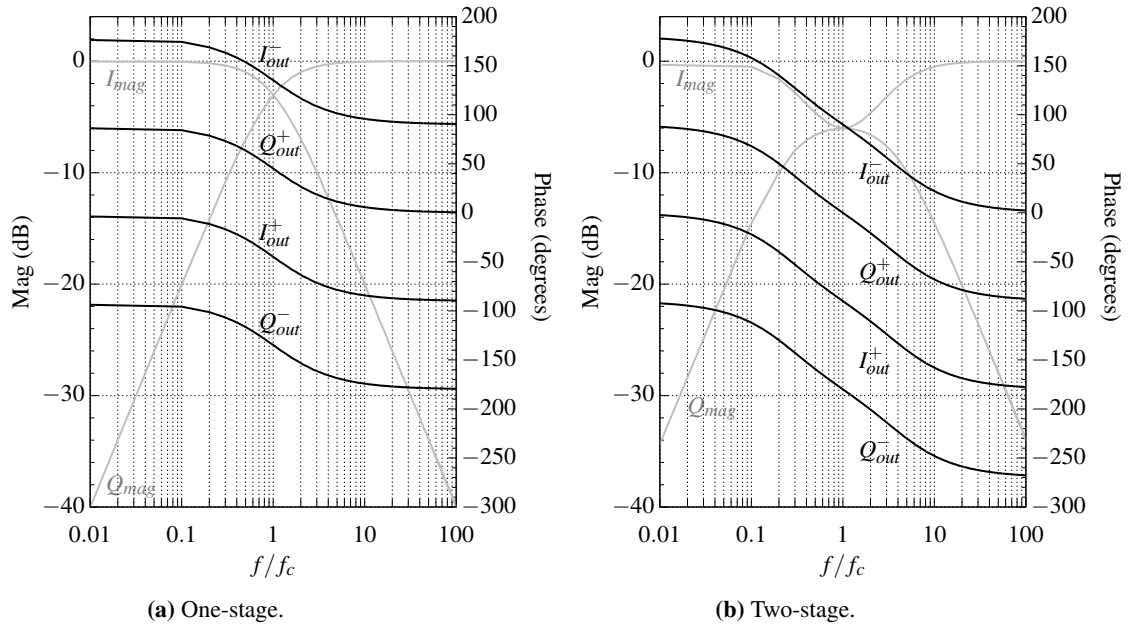


Figure 2.22: PPF AC analysis for one- and two-stage configurations.

The one-stage shown in figure 2.20b finds its application in generation of quadrature signals with differential outputs. Nonetheless, in order to extend $\pi/2$ phase-shifting in frequency, the order of the passive PPF must be increased. A two-stage PPF is also represented in figure 2.20. The broadband behavior in phase-shifting is effectively achieved, as seen in the AC analysis of figure 2.22 in which one- and two-stages can be compared.

It should be noted that each stage introduces a 3-dB loss [35]. Also, due to the high number of resistors used, matching can be a critical issue. In order to obtain quadrature signals from one single-phase source, the circuit of figure 2.23 can be used.

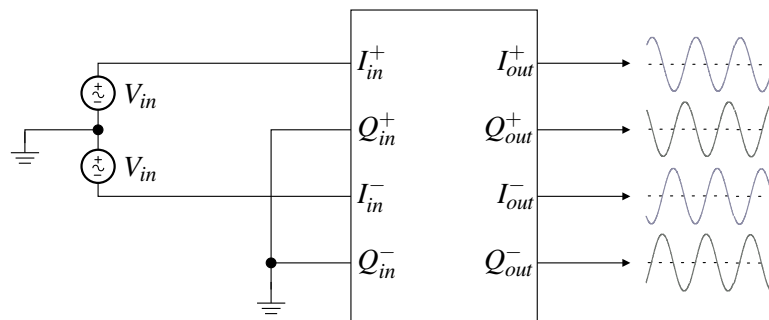


Figure 2.23: Implementation for PPF quadrature generation.

Active filters, on the other hand, can achieve a good image rejection and simultaneous adjacent channel interference rejection [36, 37]. However, comparing to the passive counterparts, the active

PPF implementations consume more power and occupy larger area. In order to better explain how an active PPF can be realized let us present the following brief theoretical explanation. Consider an RF signal given by the superposition of image and desired signal:

$$x_{RF}(t) = A_{sig} \cos[(\omega_{LO} + \omega_{IF})t] + A_{img} \cos[(\omega_{LO} - \omega_{IF})t] \quad (2.40)$$

After eliminating the high-frequency components from the down-conversion I/Q mixer output that respectively uses $LO_I(t) = \cos(\omega_{LO}t)$ and $LO_Q(t) = -\sin(\omega_{LO}t)$ as LO signals, it results then the I/Q inputs of the polyphase filter given by:

$$I(t) = \frac{A_{sig} + A_{img}}{2} \cdot \cos(\omega_{IF}t) \quad (2.41)$$

$$Q(t) = \frac{A_{sig} - A_{img}}{2} \cdot \sin(\omega_{IF}t) \quad (2.42)$$

From equations (2.41)–(2.42), the output written as follows:

$$x_{OUT}(t) = I(t) + jQ(t) \quad (2.43)$$

$$= \frac{A_{sig}}{2} \cdot e^{j\omega_{IF}t} + \frac{A_{img}}{2} \cdot e^{-j\omega_{IF}t} \quad (2.44)$$

Given the complex representation just referred, a possible graphical representation of the signal and its image can be seen in figure 2.24. The signal and its image are located at different sides of the frequency axis, that is, the signal is at a positive IF value⁶ while its image is located at a negative IF value. Thus, in order to reject the image component, one has to use a complex BPF centered at ω_{IF} .

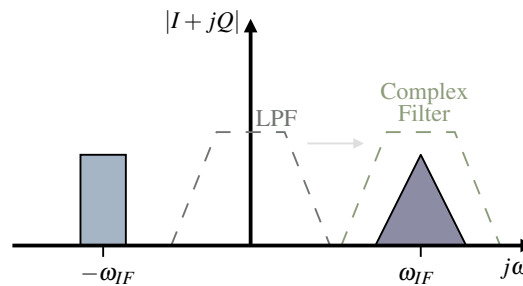


Figure 2.24: Frequency translation of the LPF.

To convert an LPF to a complex BPF centered at $\omega = \omega_{IF}$, every frequency dependent element in the LPF should be changed to be a function of $s - j\omega_{IF}$ instead of s solely. This operation is

⁶This was the reason why, for simplicity, $-\sin(\omega_{LO})$ was chosen as quadrature signal in the LO since the beginning of this text.

shown in figure 2.25 for the case of a first order complex filter. Higher orders can be achieved by cascading this filter topology.

By using feedback on a low-pass system one can obtain the intended complex BPF. However, the term $j\frac{\omega_{IF}}{\omega_0}$ must be used in the feedback loop. Since this is not a real signal operation, an equivalent approach must be used in the real domain in order to obtain this complex domain behavior.

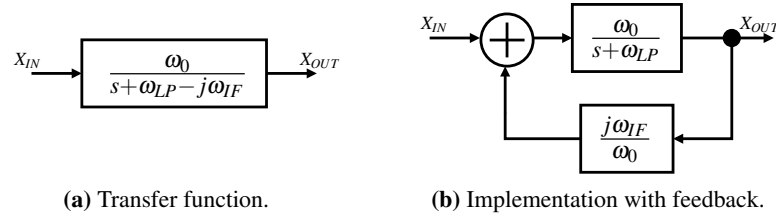


Figure 2.25: LP filter shift to complex BP.

Figure 2.26 shows a possible implementation of a complex filter in the real domain based on a LPF [34, 36] by using both I and Q channels in the filter topology. The terms ω_{IF} , ω_{LP} and ω_0 are respectively the intermediate frequency, the cut-off frequency of the translated LPF, and the gain at the central frequency of the complex filter relative to ω_{LP} .

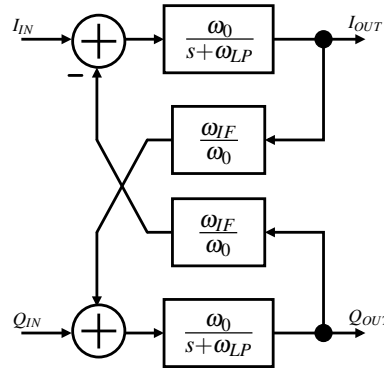


Figure 2.26: Block diagram of the LPF shift to BPF with I and Q channels [34, 36].

The filter topology given in figure 2.26 can be represented by the following two transfer functions [36]:

$$I_{OUT}(s) = \frac{\omega_0}{s + \omega_{LP}} \cdot \left(I_{IN}(s) - \frac{\omega_{IF}}{\omega_0} \cdot Q_{OUT}(s) \right) \quad (2.45)$$

$$Q_{OUT}(s) = \frac{\omega_0}{s + \omega_{LP}} \cdot \left(Q_{IN}(s) + \frac{\omega_{IF}}{\omega_0} \cdot I_{OUT}(s) \right) \quad (2.46)$$

When combining the outputs as $X_{OUT} = I_{OUT} + jQ_{OUT}$, equations (2.45)–(2.46) lead to [36]:

$$\frac{X_{OUT}(s)}{X_{IN}(s)} = \frac{\omega_0}{s + \omega_{LP} - j\omega_{IF}} \quad (2.47)$$

where $X_{IN} = I_{IN} + jQ_{IN}$ and in which the transfer function is the same as the one in the complex filter representation of figure 2.25a.

A possible circuit implementation of this type of PPF is shown in figure 2.27 [36].

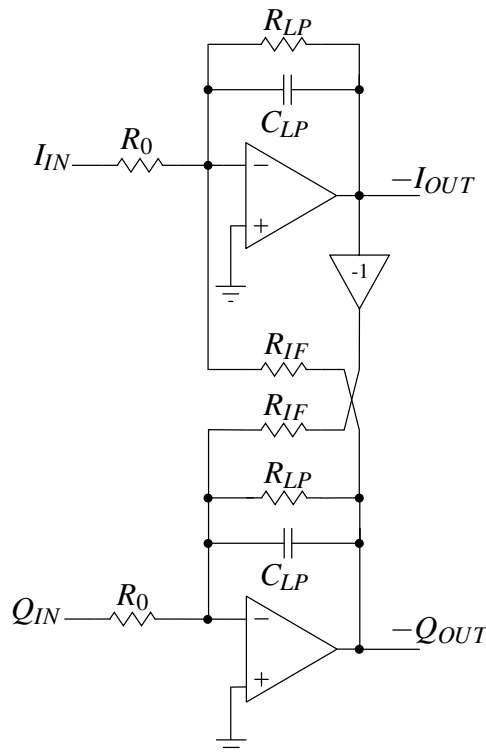


Figure 2.27: Active-RC implementation of a PPF [36].

The equivalence of this circuit with the system implementation shown in figure 2.26 can be easily determined by circuit analysis as follows:

$$\frac{I_{IN}(s)}{R_0} = \frac{1}{R_{IF}} \cdot Q_{OUT}(s) + \left(s C_{LP} + \frac{1}{R_{LP}} \right) \cdot I_{OUT}(s) \quad (2.48)$$

$$I_{OUT}(s) = \frac{\frac{1}{R_0 C_{LP}}}{s + \frac{R_{LP}}{C_{LP}}} \cdot \left(I_{IN}(s) - \frac{R_{IF} C_{LP}}{R_0 C_{LP}} \cdot Q_{OUT}(s) \right) \quad (2.49)$$

where (2.48) has been manipulated for (2.49) to be compared with (2.45) to conclude that:

$$\omega_0 = \frac{1}{R_0 \cdot C_{LP}} \quad (2.50)$$

$$\omega_{LP} = \frac{1}{R_{LP} \cdot C_{LP}} \quad (2.51)$$

$$\omega_{IF} = \frac{1}{R_{IF} \cdot C_{LP}} \quad (2.52)$$

Figure 2.28 shows the results of an implementation of several active-RC PPF of several orders (cascaded systems) in Cadence[®] SPECTRE-RF, also the results of a SIMULINK implementation of the system shown in 2.26 and, at last, the magnitude of the transfer function denoted in equation (2.47). The magnitude represents the absolute value in dB of $(I_{OUT} + jQ_{OUT})/(I_{IN} + jQ_{IN})$.

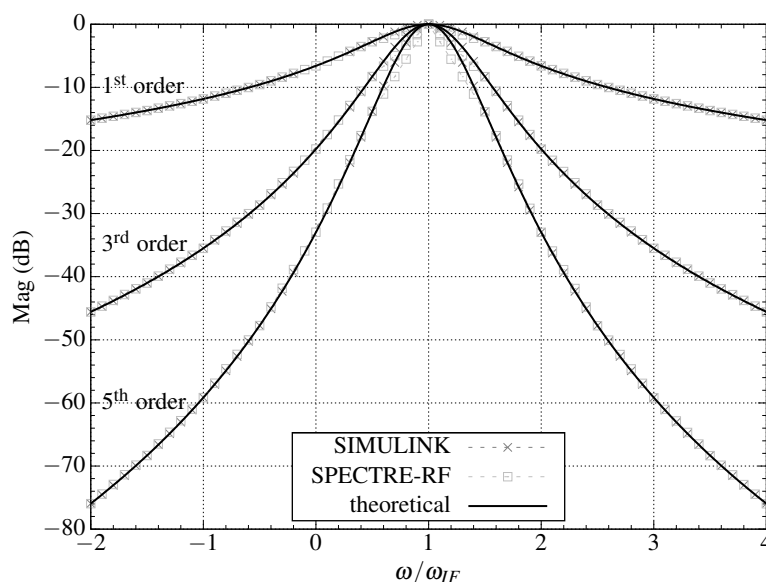


Figure 2.28: Magnitude of the frequency response of a PPF in SIMULINK, SPECTRE-RF and the theoretical case ($\omega_{LP} = \omega_0 = 0.53 \cdot \omega_{IF}$).

The frequency response shown in figure 2.28 makes use of a linear frequency scale. In fact, due to negative values of some frequencies a logarithmic scale is not possible. It should be noted however that even for positive values of frequency, directly applying $\log_{10}(\omega)$ to convert into a logarithmic scale would not lead to the expected values in which we are used to have a first-order BPF symmetrical to its central frequency.

Indeed, the required transformation to obtain the typical filter behavior is $\pm \log_{10}(\pm \omega \mp \omega_{IF})$. This will lead to a graphical form that we are used to for filter interpretation in which the attenuation is measured in terms of decades in which the order of the filter turns out to be clear.

Figure 2.29 shows this kind of representation⁷ for a first-order PPF with several values of ω_{LP} , in which ω_0 has been kept equal to ω_{LP} in order to maintain the same gain at IF. As seen in figure, the attenuation follows an attenuation of 20/decade, i.e. each tic in the xx axis represents a decade. The filter response is centered at the signal frequency, i.e. ω_{IF} . The value of ω_{LP} has been chosen as very low comparing to ω_{IF} for a clear and simpler representation.

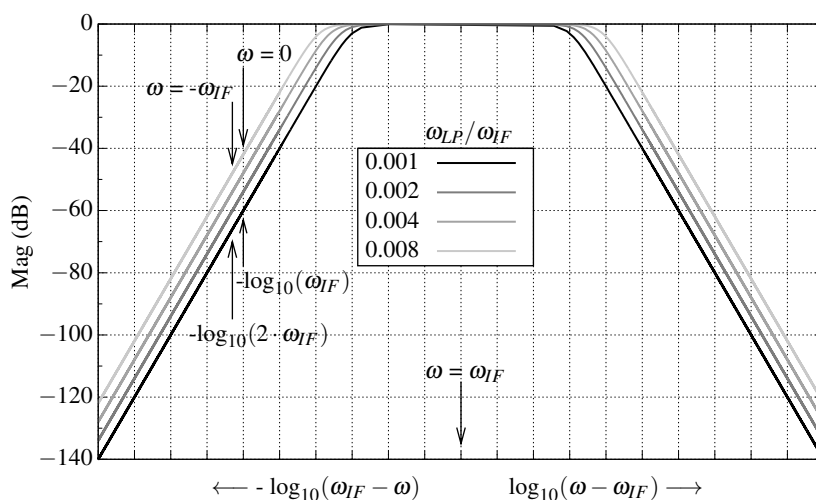


Figure 2.29: Magnitude representation of PPFs for several ω_{LP} , always with the same ω_{IF} and $\omega_0 = \omega_{LP}$.

For a PPF the IRR can be determined based on the order of the filter N (or equivalently a N -stage first-order filter), its central frequency ω_{IF} and half-bandwidth ω_{LP} as follows [38]:

$$IRR_{dB}(\omega) = 10 \cdot N \cdot \log_{10} \left(\frac{1 + \left(\frac{\omega - \omega_{IF}}{\omega_{LP}} \right)^2}{1 + \left(\frac{\omega + \omega_{IF}}{\omega_{LP}} \right)^2} \right) \quad (2.53)$$

whereas for $\omega = \omega_{IF}$:

$$IRR_{dB}(\omega_{IF}) = -10 \cdot N \cdot \log_{10} \left(1 + \left(\frac{2\omega_{IF}}{\omega_{LP}} \right)^2 \right) \quad (2.54)$$

From equation (2.54), for instance for a low-IF Bluetooth system with $\frac{\omega_{IF}}{2\pi} = 2$ -MHz, and $\frac{\omega_{LP}}{2\pi} = 530$ -kHz [36], it can be seen in table 2.2 the typical values for the IRR that can be obtained with an ideal PPF.

⁷Nonetheless, this graphical representation in PPF Bode diagrams is not common in any paper in the literature known although it is seen here as quite useful for describing PPFs functionality.

Order	IRR (dB)
1 st	-17.63
3 rd	-52.89
5 th	-88.16
7 th	-123.42

Table 2.2: IR in PPFs with different orders with $\frac{\omega_{IF}}{2\pi} = 2$ -MHz and $\frac{\omega_{LP}}{2\pi} = 530$ -kHz.

It should be noted that, due to non-idealities, when there are mismatches in the PPF the IRR is degraded. In a study presented in [39], mismatches of amplitude and frequency have been derived as:

$$IRR_{PPF}(\omega) \cong \left\{ \frac{\left[64A^2(\omega^4 - \omega_{LP}^4) \frac{\Delta A}{A} + 64A^2 \omega \cdot \omega_{LP} (\omega - \omega_{LP})^2 \frac{\Delta \omega_{LP}}{\omega_{LP}} + 64A^2(\omega^2 + \omega_{LP}^2)(\omega - \omega_{LP})^2 + 16A^2(\omega^2 + \omega_{LP}^2)(\omega + \omega_{LP})^2 \frac{\Delta A^2}{A} + 32A^2 \omega_{LP}^2(\omega^2 + \omega_{LP}^2)(\omega^2 - \omega_{LP}^2 + \omega \cdot \omega_{LP}) \left(\frac{\Delta \omega_{LP}}{\omega_{LP}} \right)^2 \right]}{64A^2(\omega^4 - \omega_{LP}^4) \frac{\Delta A}{A} - 64A^2 \omega \cdot \omega_{LP} (\omega + \omega_{LP})^2 \frac{\Delta \omega_{LP}}{6} 4A^2(\omega^2 + \omega_{LP}^2)(\omega + \omega_{LP})^2} \right\}^{1/2} \quad (2.55)$$

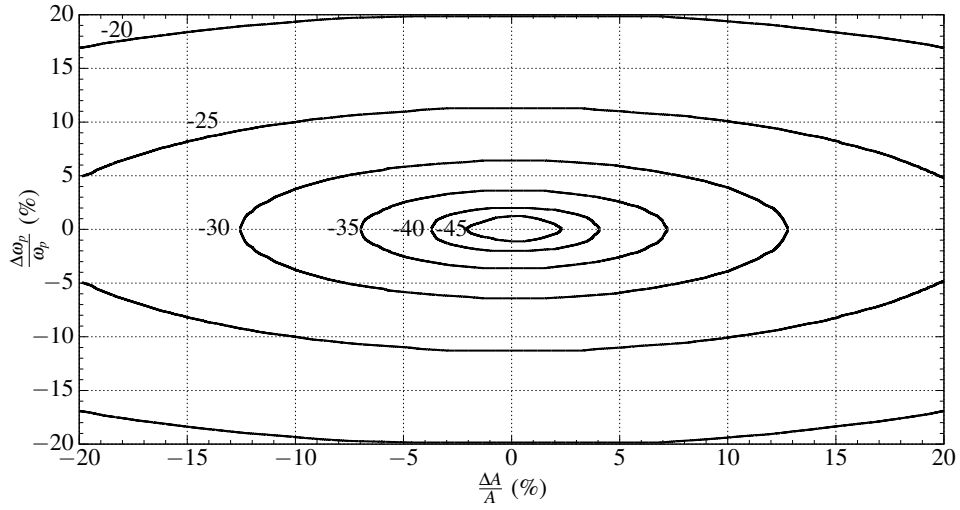


Figure 2.30: Constant IRR curves for a non-ideal PPF [39].

As seen in [39] and in figure 2.30, for $|\Delta A/A| > 12\%$ or $\Delta \omega/\omega_{IF} > 5\%$ the IRR of the PPF is degraded about 30-dB [39]. This has to be taken into account when designing a PPF, since the overall IRR is affected. Therefore, tuning schemes for PPF implementations are required for compensation, to achieve the best performance from the PPF.

Chapter 3

State of the Art

Along this chapter some of the most interesting reported implementations of polyphase filters are described. Due to PVT variations tuning systems are usually required for compensation. Some interesting tuning systems found in literature are presented in a latter section. At the end, implementations of g_m -C cells for filter design are also shown.

3.1 Polyphase filters

A. Emira *et al.* present in [36] a PPF based on a Butterworth approximation. The possible solutions analyzed in this paper for the filter prototype were a fourth-order Chebyshev LPF and a sixth-order Butterworth. To achieve the necessary selectivity, the Butterworth topology was preferred due to several reasons: small group delay variation ($0.6\mu\text{s}$) within the passband and all the poles with the same frequency, thus leading to better matching in the cross-coupled operational transconductance amplifiers (OTAs) implemented using g_m -C circuits.

Still in this work, the highest quality factor in the LPF prototype is two, which can tolerate for mismatches without affecting the filter performance significantly. Using only grounded capacitors to implement the transformation to the BPF reduces area and power consumption of the complex filter. To reduce the input referred noise, the least number of transistors is used in the OTA and long-channel transistors (about $6\mu\text{m}$) to enhance the output resistance, thus improving matching and reducing flicker noise. The PPF uses a pseudo-differential topology in order to reduce the required supply-voltage.

As seen in [36], the gain distribution among the filter stages is also another important design issue. Assigning all the gain at the input stage will optimize the noise performance but will degrade the linearity whereas designing the PPF with most of the gain in the last stage will lead the

opposite effect. For example, in Bluetooth, in-band linearity is not a big issue since it uses Gaussian Frequency Shift Keying (GFSK), which is a constant envelope modulation so no information is present in the signal amplitude. Therefore, the design should focus on the out-of-band linearity. The out-of-band blockers will be attenuated by the filter, so the generated harmonics by these out-of-band blockers are dominated by the first gain stage of the filter. Hence, to improve the overall filter linearity, the gain stage is designed to have better linearity by using large overdrive voltage $V_{GS} - V_T$ of the input NMOS transistors.

Common-mode rejection ratio (CMRR) is another key aspect in the design of g_m -C filters. To enhance the CMRR of the OTAs common-mode feedback (CMFB) or common-mode feed forward (CMFF) is used in [36] depending on the common-mode (CM) impedance at the output node. If the output CM impedance is high, then CMFB is needed to lower this impedance. By using the minimum number of CM control circuits, this efficient scheme saves considerable power and silicon area and contributes to less noise than using a CM control circuit for each OTA. The complete complex filter circuit implemented in [36] is shown in figure 3.1. It uses three biquads with different quality factors (Q_L) preceded by a highly linear gain stage due to the reasons previously mentioned.

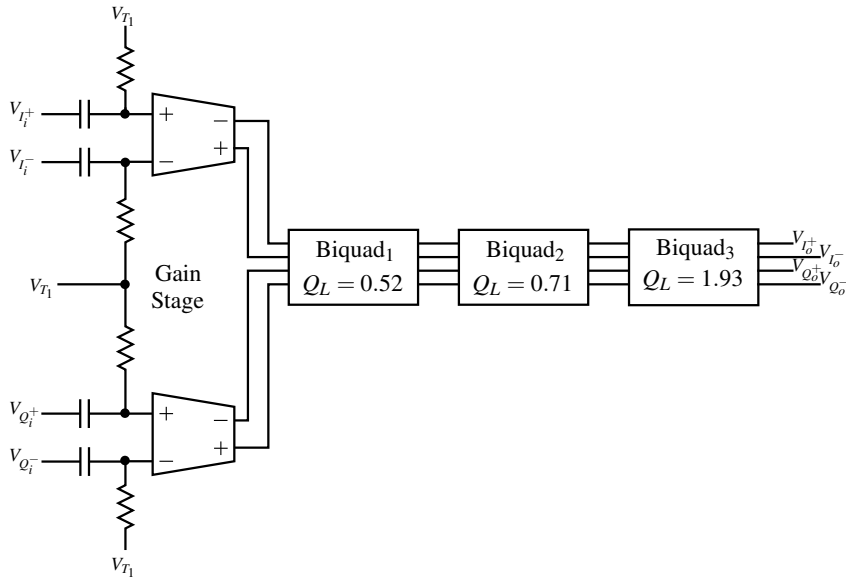


Figure 3.1: Sixth-order complex filter using G_m -C circuits [36].

In [40] it is proposed the implementation of a PPF using four cascaded stages with each having high input impedance to prevent gain degradation of the preceding stage. The largest gain is assigned to the first stage for better noise performance. A constant- g_m bias circuit is incorporated into the PPF to reduce variations in gain and attenuation of out-of-band frequencies.

J. Crols *et al.* propose in [34] a PPF based on an active RC topology with operational amplifiers (op-amps). There are two main reasons why the active-RC technique is used for the realization

of the PPF. A small wanted signal can be surrounded by large neighbor signals and this requires a very high dynamic range at the input. This can only be achieved with active-RC technique. Another reason for using this approach is the mismatch. The signal crosstalk from negative to positive frequencies should be as small as possible and it is mainly determined by the matching between equivalent resistors in the I and Q paths. With MOSFET-C or OTA-C the performance would depend on the matching of transistors, which is claimed in [34] that these are options to be avoided when comparing to better matching attainable with large resistors.

In [41], another active-RC PPF topology is proposed due to its excellent noise and linearity performance. It uses a Cauer prototype since it claims to be the best compromise in terms of the equi-ripple in the pass- and stop-band and acceptable group delay variations. It is stated in [41] that when designing a filter with an OTA it is desirable that the external components determine the filter characteristics and so that the OTA influence can be minimized.

A sixth-order biquad elliptic filter is proposed in [42] – figure 3.2. One of the benefits of this circuit is that almost all the parasitic capacitors of the transistors can be absorbed in the main capacitors of the filter except only one. Another advantage is the good matching between two PMOS transistors whose bulks are tied to their sources. Additionally, it can realize both zeros and poles. The parasitic capacitors in such a simple and compact structure have insignificant negative effects, but finite output resistance can degrade the quality factor of the filter.

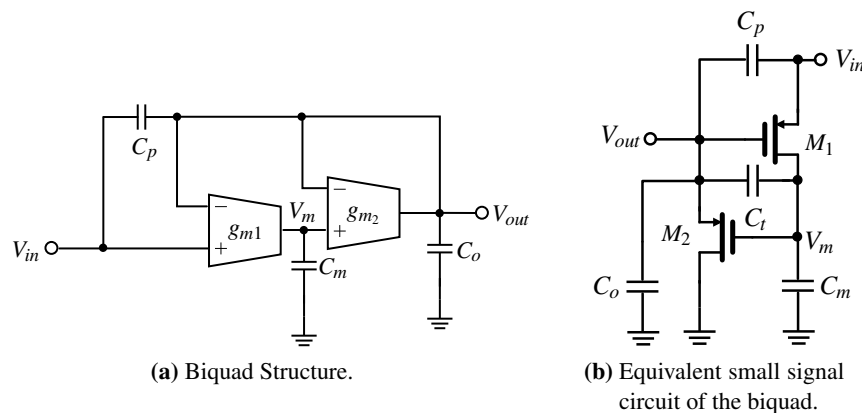


Figure 3.2: Biquad circuit of [42].

In Teo *et al.* [43] it is implemented a fifth-order transitional Bessel-Chebyshev filter. The same topology is used in [44]. It has no internal nodes, so it does not introduce extra phase-shifting in its integrator, thus increasing power efficiency more than simple common source transconductors. It is employed a high-speed CMFB circuit to provide sufficient CMRR. In the layout of the transistors, a common-centroid technique is used to further improve matching.

A two-stage low-voltage/low-power opamp PPF is presented in [38] – figure 3.3. The opamp must have enough phase margin to avoid oscillation with the PVT variations. Thus, a Miller capacitor compensates the frequency response by pole-splitting: moving the first pole near to

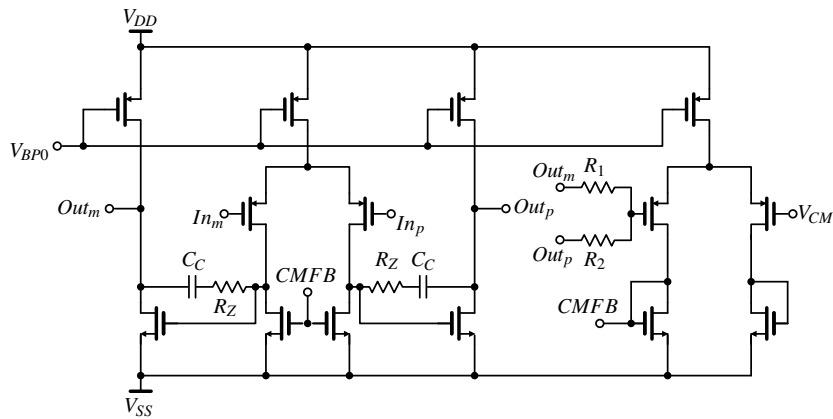


Figure 3.3: Schematic circuit of the amplifier of [38].

origin and shifting the second pole beyond the unity gain frequency so the unity-gain frequency of the opamp is high enough to satisfy the specifications. However, a zero is produced using Miller capacitor compensation, reducing the phase margin and deteriorating the stability. Using a string resistor together with the Miller capacitor moves the zero to the left complex half-plane. The amplifier uses PMOS transistors as input transistors to reduce input noise. The dominant pole of the frequency response is determined by the transconductance of the input transistors and load capacitance of the amplifier, and non-dominant pole is related to the transconductance of the cascade transistors. By selecting PMOS as input transistors, the dominant pole will move to lower frequencies (due to lower g_m) and the non-dominant pole will move to higher frequencies (due to higher g_m of NMOS transistors). Hence, an intrinsic pole splitting will occur. The major drawback is that the amplifier provides little gain.

Abrishamifar *et al.* [45] present a PPF with a new Class-AB amplifier that can drive heavy capacitive and low resistive loads. It uses a cascode configuration to increase bandwidth – figure 3.4.

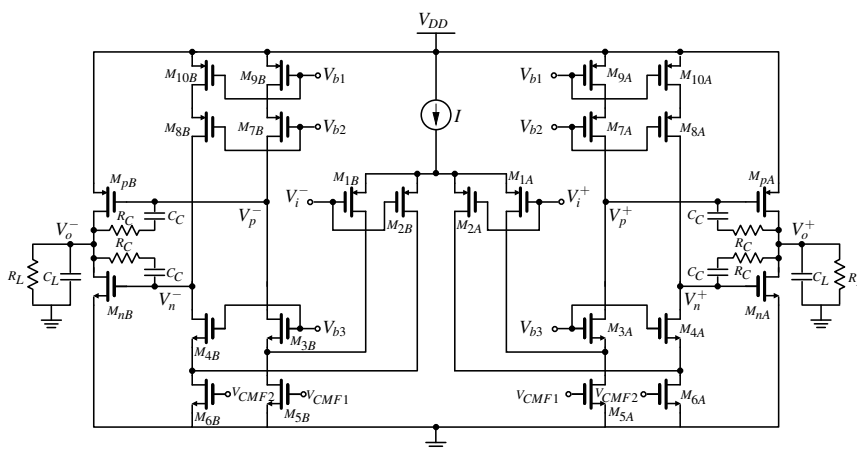


Figure 3.4: Schematic circuit of the amplifier of [45].

Table 3.1 shows a comparison between several implementations of polyphase filters. The most important specifications for a polyphase filter were the base to elaborate this comparison. These include IRR, adjacent channel suppression (ACS), power consumption, technology and consumed area.

Ref.	IRR (dB)	ACS (dB)	Power (mW)	Technology	Year	Area (mm ²)
[34]	> 64	–	450	1.2 μ m CMOS	1995	7.5
[36]	> 45	27 (1 st), 58 (2 nd)	12.69	0.35 μ m CMOS	2003	1.28
[40]	> 60	–	6.85	0.18 μ m CMOS	2002	0.94
[41]	50	> 60	1.575	0.25 μ m BiCMOS	2006	0.68
[42]	45	–	2.16	0.18 μ m CMOS	2003	0.374
[43]	30–40	18	13.5	0.18 μ m CMOS	2004	0.752
[38]	38	–	4.2	0.18 μ m CMOS	2008	0.26
[45]	40	19	4.3	0.18 μ m CMOS	2007	–
[46]	28	–	6.1	0.18 μ m CMOS	2006	3.0 (*)
[47]	48.85	\geq 40.7	–	0.18 μ m CMOS	2008	0.607
[48]	> 53	> 40	7.36	0.35 μ m CMOS	2000	0.374
[49]	24.2	33.1	4.68	0.18 μ m CMOS	2008	0.542
[50]	60–72	–	20.68	0.18 μ m CMOS	2002	–
[51]	55	27	0.72	0.18 μ m CMOS	2006	1.28

Table 3.1: Comparison between PPF implementations
(*) tuning circuit included.

3.2 Tuning Schemes

Since any wireless receiver using quadrature mixers is essentially a multi-path system, inherent mismatches in the analog paths lead to degradation of the IRR. Although, an ideal PPF thwarts the IRR reduction, in fact, realistic mismatches in the implementation of the PPF structure disfavor the expected IRR improvement in the overall performance, thus requiring proper tuning schemes to be implemented within the PPF structure.

The frequency tuning scheme for the PPF presented in [36] consists of a relaxation oscillator, two counters to measure the oscillator and reference frequencies, a comparator, an up/down counter and a digital-to-analog converter (DAC) as shown in figure 3.5.

The operation of the circuit shown in figure 3.5 is as follows. When a reset signal occurs, the oscillator and the reference counters start counting until the reference counter reaches 64. Then, the value in the oscillator counter is compared with the reference value 64, which will increase or decrease a voltage by means of an up/down counter depending on the result of the comparison. This scheme implies the use of a 7-bit DAC to obtain an analog control voltage. This voltage controls the frequency of the relaxation oscillator and also the g_m of the polyphase filter. When the reference counter overflows, the system is reseted so that this new frequency is compared to the reference frequency of 1-MHz, which is obtained by a frequency division by 16 of a 16-MHz crystal. The basis of this scheme is that the relaxation oscillator has a g_m cell identical to the one

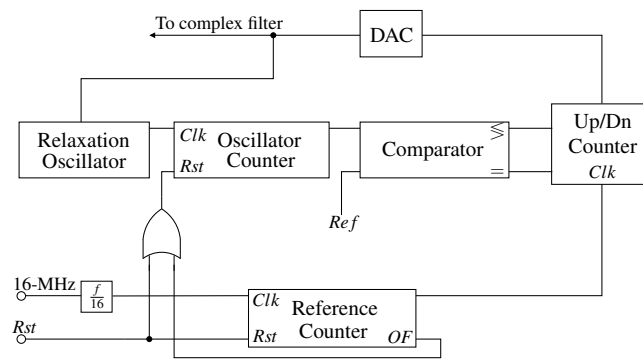


Figure 3.5: PPF tuning scheme proposed in [36].

used in PPF, so by means of the oscillating frequency the supposed value of the g_m cell is tuned. This operation can be performed online, that is, while the PPF works under typical operation. Therefore, it is not required for the PPF to be stopped for tuning process.

The oscillator frequency reaches 1-MHz reference frequency within an error depending on the DAC resolution. The comparator has a dead-zone to avoid oscillation in the loop around the desired frequency. For a $\pm 30\%$ process variation and a 7-bit DAC, the maximum frequency error is about $\pm 0.23\%$, which is quite tolerable for Bluetooth applications. The 7-bit DAC is implemented using resistive string to ensure monotonicity and, hence, stability of the tuning loop.

Mismatches between the transconductance and capacitance in the passive RC LPF and the oscillator should be considered, and they can add a frequency mismatch of about 1%, that is, still within the range for Bluetooth specifications. The advantage of such circuit over the other existent schemes such as the traditional PLL-based frequency tuning is that it does not need a low-frequency low-pass-loop filter, which would consume a lot of power and area. Instead, it uses a square wave relaxation oscillator, which is easier to build and still guarantees the need functionality.

In [46] it is proposed a tuning system that is mainly composed by an integrator, comparator a capacitor bank and digital circuitry – see figure 3.6. Its operation is as follows. The output of the integrator (V_o) is compared with the reference voltage (V_{ref}) of the comparator. At the output of the comparator, if V_o is lower than V_{ref} , the digital circuit increases the 5-bit digital word of the capacitor bank until $V_{ref} \leq V_o$. The opposite occurs when $V_o > V_{ref}$.

The digital part operates as follows. The output of the comparator is sent to an encoder, which codes the 1-bit signal into 5 bits. In the following clock cycle, the output of the counter is changed and applied to the capacitor bank. The capacitance of the capacitor bank will be changed to generate a new voltage to be compared to the reference one. This will continue to happen until the tuning process is complete.

The tuning system can be turned off after the tuning is complete. The tuning circuit takes at most 32 cycles to tune the filter. The accuracy of the tuning circuit is determined by the number of bits n of the capacitor bank and its value is determined by $\frac{1}{2^n}$.

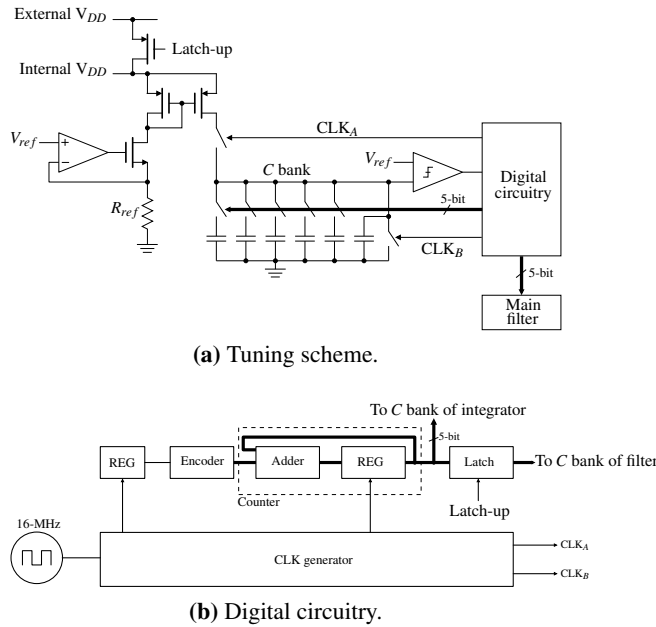


Figure 3.6: Tuning circuit proposed in [46].

In Fangxiong Chen *et al.* [49] the proposed tuning circuit consists of a digital circuit, a latch comparator and an integrator, which comprises of a capacitor bank, transistors, an amplifier and a variable resistor as shown in figure 3.7.

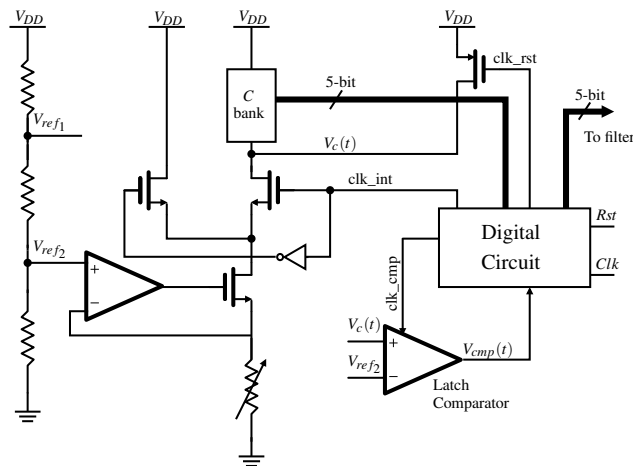


Figure 3.7: Tuning scheme proposed in [49].

It uses master-slave technique and is based on the binary search algorithm. The master refers to the integrator of the tuning system, which models the RC constants in the slave circuit. The slave is the complex filter.

The digital circuit consists of a counter and a wave generator, that generates periodic waveforms. The output voltage of the integrator (V_c) depends on the value of the capacitor bank. This value is compared with a reference voltage (V_{ref}) and the capacitor bank is adjusted accordingly. Through the digital part a 5-bit word is set in order to change the value of the capacitor bank. It takes less than 10-ns for the tuning to be completed.

The PPF with tuning circuit described in [43] uses PLL-based automatic frequency control loop, but instead of a harmonic oscillator it uses a relaxation oscillator in the loop – figure 3.8. The measurements on the circuit showed that with the relaxation oscillator the tuning circuit is insensitive to process, temperature (-40° to $+85^\circ$) and supply voltage variations (1.3V to 2.1V), keeping the frequency tuning error less than 7%.

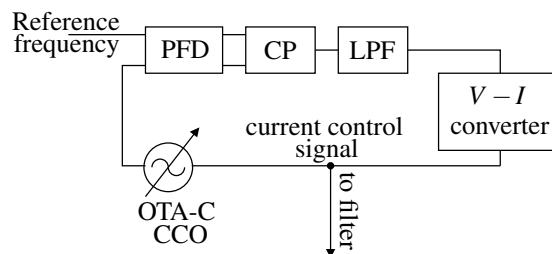


Figure 3.8: PLL-based tuning proposed in [43].

3.3 G_m -C Filters

A pseudo-differential OTA is presented in [52] by Mohieldin *et al.*. Unlike other typical implementations, it has an inherent CMFF and CMFB, thus avoiding an implementation that adds more load to the driving stage. CMFF is achieved by using the same transconductance and making copies of the differential current and subtracting the CM current at the output. CMFB can be employed by connecting two of the presented OTAs. In this case, the DC level of the output is compared to the reference, which is then fixed to the correct value. This arrangement has the advantage that differential-mode signals and CM signals share the same loop if grounded capacitors are used, and the low-frequency transconductance of the CMFB loop is the same as differential transconductance, making it easier to obtain similar bandwidth for common-mode and differential-mode loops. Figures 3.9 and 3.10 show the circuit for the OTA with CMFF and CMFB respectively. The transconductor proposed in [52] can be tuned by changing the CM input voltage. In the case of the typical differential pair with a tail current source, this changes the linearity performance. However, in a pseudo-differential architecture as this one, this effect is less severe. A 100-MHz fourth-order linear phase Bessel-Thomas was designed with this OTA in a $0.5\text{-}\mu\text{m}$ CMOS technology. It consumes 26-mA from a 3.3-V supply voltage and occupies an area of $450 \times 350\text{-}\mu\text{m}^2$.

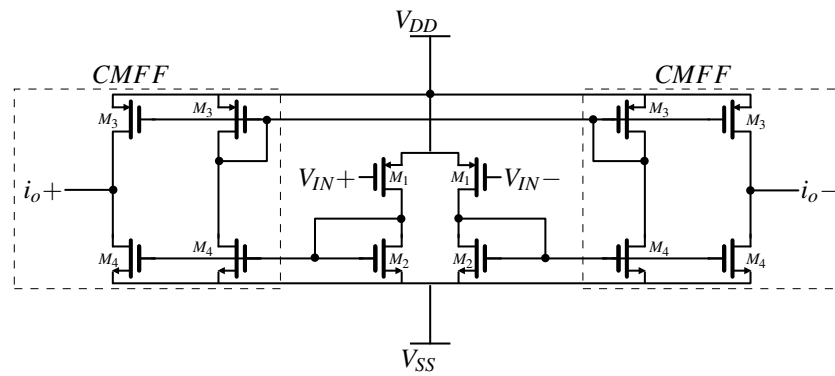


Figure 3.9: Transconductor with CMFF in [52].

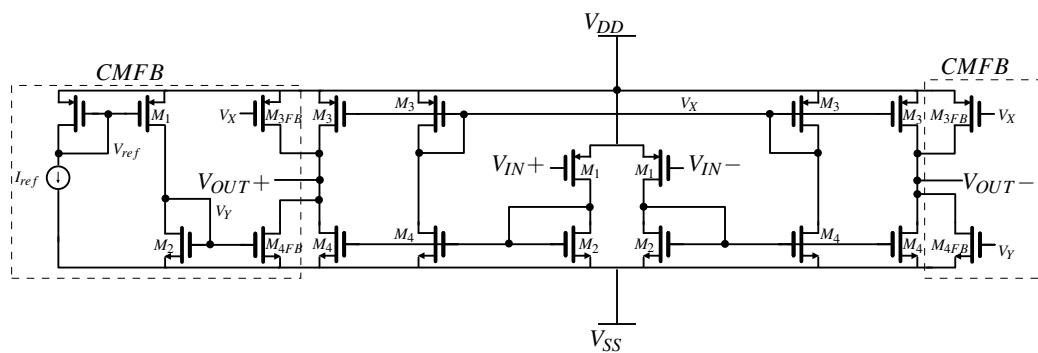


Figure 3.10: Transconductor with CMFB in [52].

Bram Nauta presents a transconductor based on CMOS inverters in [53]. The CMOS inverters have no internal nodes and have a good linearity if the β factors of the NMOS and PMOS are perfectly matched. The circuit of the transconductor can be seen in figure 3.11.

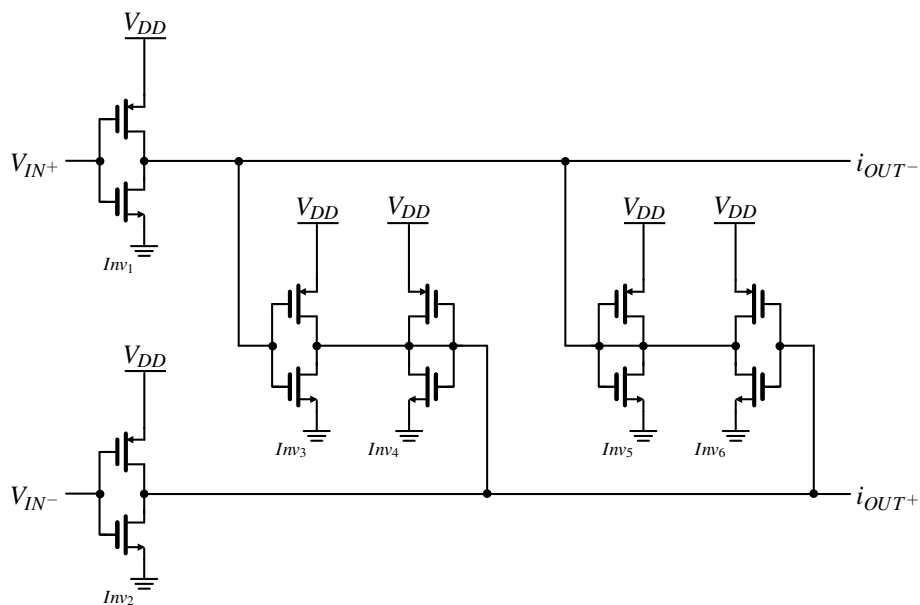


Figure 3.11: Nauta's transconductor [53].

This architecture is fully-differential and in order to work properly the transistors need to operate in the strong inversion and in saturation. As can be seen in figure 3.11, the transconductor has no internal nodes (except ground and V_{DD}) meaning that the capacitors at the outputs will be connected to the parasitic capacitances [54]. This will allow for the capacitors of the filter to be smaller than the theoretical value. The inverters Inv_3 - Inv_6 are responsible for the CM stability, while Inv_1 and Inv_2 are responsible for the voltage-to-current conversion.

The bandwidth of the transconductor is large due to not having internal nodes. The only parasitic poles are due to the finite time of the carriers in the channel that are in the GHz range. In the distortion aspect, the mobility reduction of both the NMOS and PMOS causes mostly third-order distortion. Channel-length modulation, which is common in circuits with “square-law linearization” such as this one, is no source of distortion due to the compensation of the output resistances in the transconductor. This circuit can be tuned by means of the supply voltage, and the output resistance by adding a different supply voltage to inverters Inv_4 and Inv_5 . A third-order elliptic filter has been implemented with this transconductor in a 3- μm CMOS process with the results present in table 3.2.

Parameter	$V_{DD} = 2.5 \text{ V}$	$V_{DD} = 5 \text{ V}$	$V_{DD} = 10 \text{ V}$
Cut-off frequency	22 MHz	63 MHz	98 MHz
Total passband input noise	-	$81 \mu V_{rms}$	$96 \mu V_{rms}$
Dynamic range	-	68 dB	72 dB
CMRR passband	40 dB	40 dB	40 dB
Transconductance	0.35 mA/V	1.06 mA/V	1.38 mA/V
Power dissipation	4 mW	77 mW	670 mW

Table 3.2: Experimental results for filter with transconductor from [53].

Another pseudo-differential OTA is presented by A. Emira *et al.* in [36] based on the circuits shown in figure 3.12. The implementation in this paper was preferred over Nauta’s transconductor [53], presented above, for two reasons: *i*) it has the possibility to choose which type of CM stability is used, thus avoiding additional circuitry that occupies space and consumes power; and, *ii*) since Nauta’s transconductor is tuned through the supply power, a buffer with high-current driving capability is needed to drive the OTA supply node. The circuit for the OTA is the typical pseudo-differential architecture that can be seen in figure 3.12a.

To bias the circuit in figure 3.12a, one of the circuits shown in figures (3.12b)-(3.12d) needs to be used. The circuit in figure 3.12b is used when the OTA does not need any CM control, that is when the CM impedance at the output node is low. To improve the CMRR of the OTA, CMFB or CMFF needs to be used. When the output CM impedance is small, CMFF is used to isolate the input and output CM signal of the OTA by canceling the CM signal. This is represented in figure 3.12c. If the output CM impedance is high, CMFB is needed to lower this impedance and to fix the dc operating point. This OTA was used to implement the PFF proposed by A. Emira *et al.* in [36] that was described in the first section of this chapter.

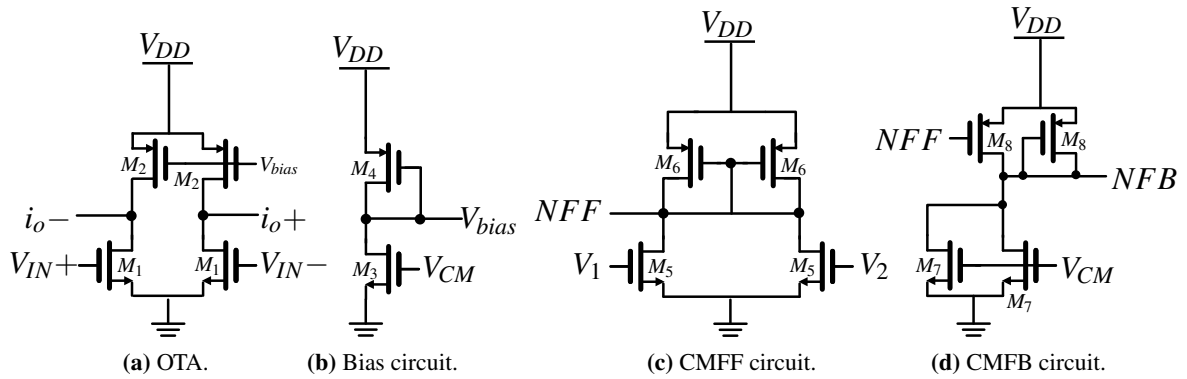


Figure 3.12: Transconductor from [36].

A new g_m -C filter is presented in [55]. It is a pseudo-differential architecture but with the input transistors working in the triode region. It is stated that this enhances the input range of the transconductor and is suitable for low-power operations. The transistors M_2 together with the amplifier form a regulated-gain-control loop are used to fix the drain voltage of the input transistors. This way the V_{DS} is constant and the value of the transconductance is βV_{DS} . To adjust the transconductance the tuning voltage V_{tune} is used. The circuit for the OTA can be seen in 3.13.

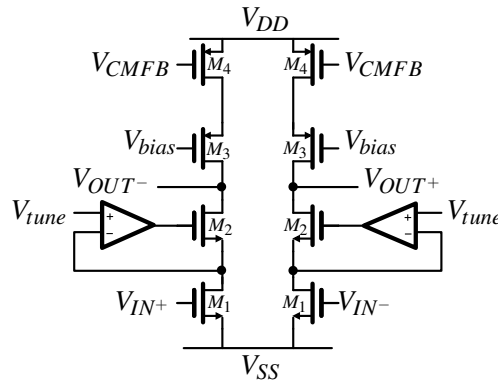


Figure 3.13: Transconductor from [55].

The circuit for the CM control can be seen in figure 3.14. This circuit integrates CMFB and CMFF in the same structure, to make the design simpler and more efficient. The CMFF part is one branch of the OTA with the input transistors having half the size comparing to the ones in the OTA. This structure cancels the CM signal. For the CMFB part, the transistors M_{6B} and M_{6A} are connected to the outputs of the OTA and the analog ground respectively, and they compare the output CM voltage with the reference and convert the difference into a correcting current. This current is going to be mirrored to transistors M_3 and M_4 through transistors M_{7A} , M_{7B} , M_{8A} and M_{8B} . The transistors M_{5A} and M_{5B} are working in triode region to act like resistors in a source degeneration scheme to improve the linearity of the CMFB. In a filter configuration, only one CM control circuit is needed per node. A fourth-order equiripple linear phase filter was built with

this implementation. This was fabricated in a 0.35- μm CMOS process achieving a bandwidth of 80-200-MHz, consuming 90-mW from a 2.3-V supply and allowing input signals up to $2 V_{pp}$.

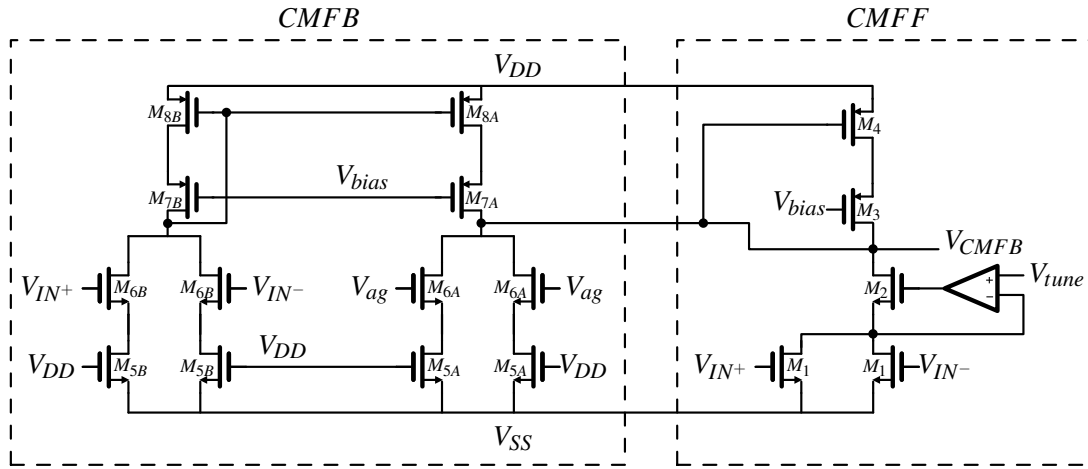


Figure 3.14: CMFB/CMFF circuit from [55].

A low-voltage transconductor is presented in [56]. It is a transconductor with a new adaptive-bias that is stated to improve the stability of the CM. This transconductor is a pseudo-differential and it can be seen in figure 3.15.

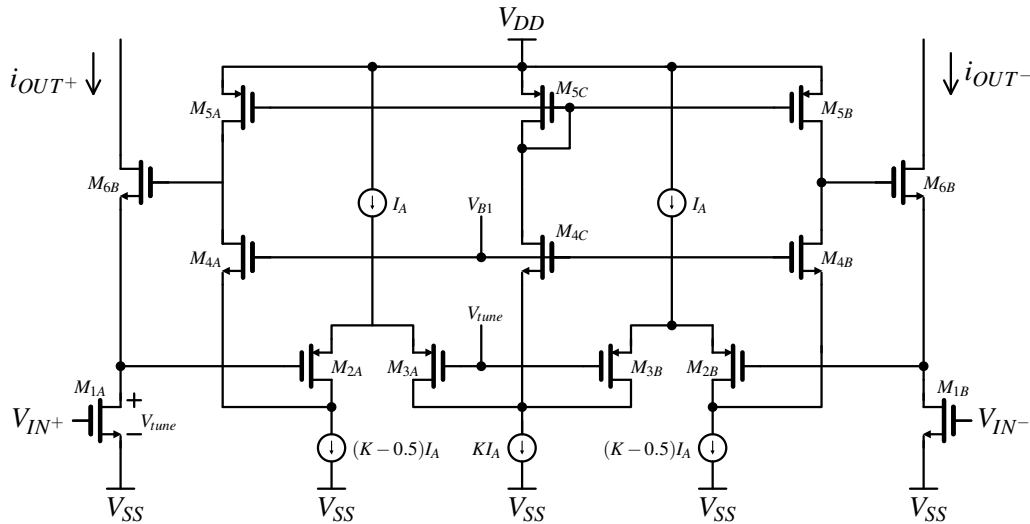


Figure 3.15: Transconductor cell from [56].

In the cell, the input transistors M_{1A} and M_{1B} work in the triode region while the rest of the transistors work in saturation. The transistors are maintained in triode through a regulated-cascode-loop whose feedback amplifier is composed by transistors M_2 - M_5 that is biased by the currents shown in the figure 3.15. This currents make sure that the voltage V_{tune} is replicated to the drain of the input transistors. Also, the loop amplification (K) boosts the output resistance of the transconductor and isolates the output from the low input low-impedance drains. The low-voltage

operations is achieved since the V_{GS} drops are not stacked between power lines. The transistors M_6 are used to increase the output resistance. The CMFB circuit used for this transconductor can be seen in figure 3.16.

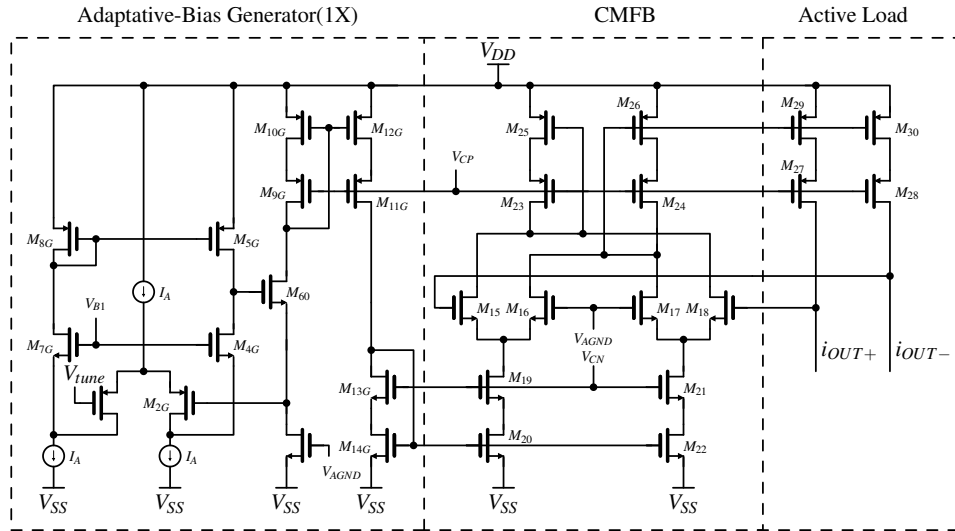


Figure 3.16: CMFB, active load and adaptive bias for the transconductor from [56].

This CMFB is a new technique where it is claimed that remarkably suppresses CM voltage deviations. It is comprised of an active load, a CMFB and the transconductor cell. The active load assures high impedance at the output to approach an ideal voltage-controlled current-source. The CMFB part is composed by an error amplifier with a bias tail current that is supplied by transistors M_{19} - M_{22} . M_{23} - M_{26} are cascode diode-connected transistors that load the error amplifier and copy their currents to the active load. The control voltages V_{CN} and V_{CP} are chosen to minimize the voltage compliance to $2 \cdot V_{DSAT}$.

Current downscaling reduces the saturation voltage of the current mirror while reducing the power consumption. Considering a constant bias current the response from the error amplifier is to unbalance the V_{GS} drops at the differential pairs, causing an offset V_{CM} comparing to the analog ground reference V_{AGND} . On an adaptive scheme, the output current will be upscaled depending on the size difference between the transistors from the CMFB and the active load. It ideally matches the variations in the output currents with the voltage V_{tune} . As so, the differential pairs are balanced and only deviations due to mismatches are expected. A third-order elliptic LPF was built with this transconductor with a -3-dB cut-off frequency of 1-MHz, having a tuning range from 50-Khz to 2.1-MHz and consuming 1.73-mW. The V_{CM} variation is said to be around 13-mV.

Chapter 4

Architecture Development

This chapter reports the work development of the PPF proposed for the present dissertation. To try surpass some of the problems of a PPF implementation, the concept of F&H is employed. This technique is firstly described in the following section. It is shown in this chapter that when the F&H technique is applied to an active RC PPF, it provides a way to control the central frequency of the PPF and reduces the size of the capacitor needed. Several ways to implement filters are described. Following, PPFs implementations are tested in those architectures with the F&H technique to decide which one should be the best for the final implementation.

4.1 Filter & Hold

The F&H concept was first introduced by V. G. Tavares *et. al.* [1, 2]. It is a technique well-suitable for the design of filters with large time constants avoiding the practical realization of huge capacitances. Its operation relies on halting the state of a continuous-time filter every T_s seconds, where T_s is the sampling period, resulting in a filter in which the time constants can be electrically controlled. This approach allows for the filter to be implemented with a very low-power consumption. To better understand how the F&H technique works let us consider the first-order LPF circuit on figure 4.1.

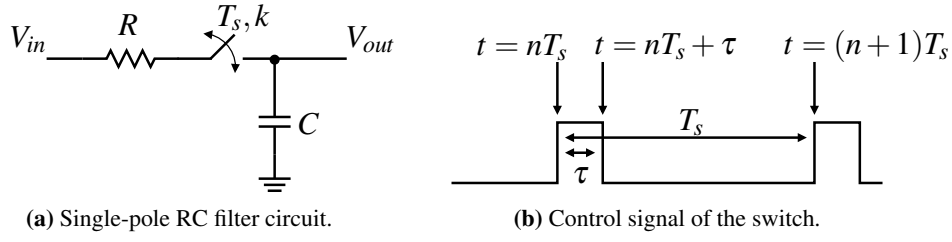


Figure 4.1: Single-pole RC filter with F&H concept applied.

The figure 4.1 shows an RC filter with a switch controlled by the clock on figure 4.1b with period T_s and closure duration τ , thus having a duty-cycle of $k = \frac{\tau}{T_s}$. Let us assume we have a signal from the output of a sample-and-hold (S&H) circuit $V_{in}(nT_s)$, which can be considered constant in the interval $nT_s \leq t \leq nT_s + \tau$. Bearing this in mind we have for $V_{out}(nT_s + \tau)$:

$$V_{out}(nT_s + \tau) = V_{out}[(n+1)T_s] \quad (4.1)$$

$$= V_{in}(nT_s) + [V_{out}(nT_s) - V_{in}(nT_s)] \cdot e^{-\alpha k T_s} \quad (4.2)$$

with $\alpha = \frac{1}{RC}$ and $\tau = k \cdot T_s$. The value of V_{out} is equal in $t = nT_s + \tau$ and $t = (n+1)T_s$ because when the switch opens the voltage is kept along the capacitor until the switch closes again. The transfer function of equation (4.2) is then defined by [1]:

$$H(z) = \frac{(1 - e^{-\alpha k T_s}) \cdot z^{-1}}{1 - e^{-\alpha k T_s} \cdot z^{-1}} \quad (4.3)$$

Since $k \leq 1$ the time constant can be made bigger by the factor k or, equivalently, the capacitance can be reduced by the same amount. Figure 4.2 shows the transient response of a first-order LPF as in figure 4.1 with signal firstly applied to an S&H at the input of the F&H. The circuit has been simulated using Cadence[®] SPECTRE. The input sine waveform has $f = f_c$ where f_c is the cut-off frequency of the RC-filter taking into account the τ scaling. As seen in figure, the amplitude is decreased to about $\sqrt{2}$, i.e. an attenuation of 3-dB.

Figure 4.3 shows the AC analysis of the F&H and its continuous-time counterpart where time constants are compensated for comparison. The frequency spectrum is taken from DC to half the sampling frequency $f_s = 1/T_s$. The simulations used Periodic Steady-State (PSS) analysis and Periodic AC analysis (PAC) from Cadence[®] SPECTRE-RF.

An oversampling ratio (OSR) of 10 has been used, i.e. f_s compared with f_c at $k = 1.0$, with 10 values of k equally spaced from 0.1 up to 1.0. The comparison with the continuous-time filter realization is also plotted, in which the capacitance is compensated with the k factor in order to perform the respective comparison. As seen, the F&H technique performs the pole scaling as desired.

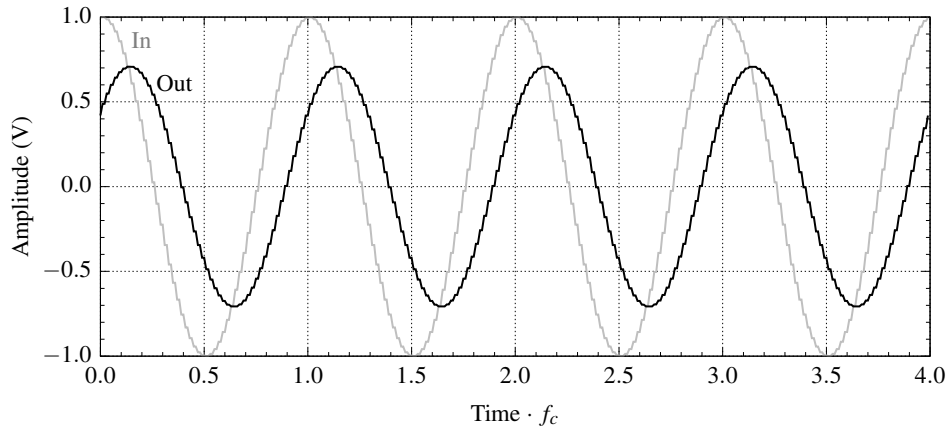


Figure 4.2: Transient response of an F&H RC-filter.

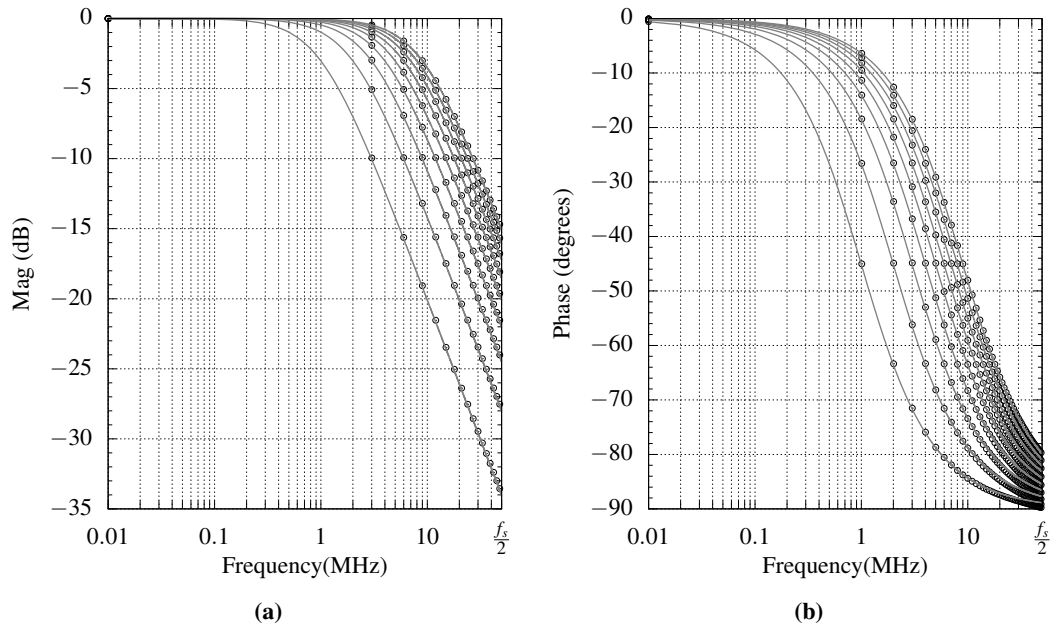


Figure 4.3: AC analysis of the F&H RC-filter (data points) and comparison with continuous-time implementation (solid-lines).

In order to demonstrate the validity of the F&H for different OSR values and several duty-factors, the sampling frequency has been swept to obtain the results shown in figure 4.4. For comparison, the continuous-time implementation is also plotted with the respective capacitance calculated for equivalent AC behavior. As seen in figure, the results only depend on the duty-cycle k , not on the sampling frequency although the latter defines the maximum frequency of operation of the filter and the signal time resolution.

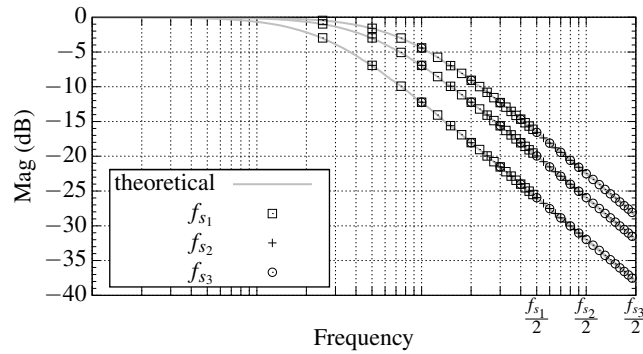


Figure 4.4: F&H for different sampling frequencies.

4.1.1 F&H in the PPF

In this section we will present the application of the F&H technique in the PPF. It will be shown that this technique is suitable for use with the PPF.

In order to apply the F&H technique in an active PPF, the circuit previously shown in figure 2.27 is changed by inserting switches in way that charge in the capacitor is maintained during the OFF state. The resulting circuit is shown in figure 4.5.

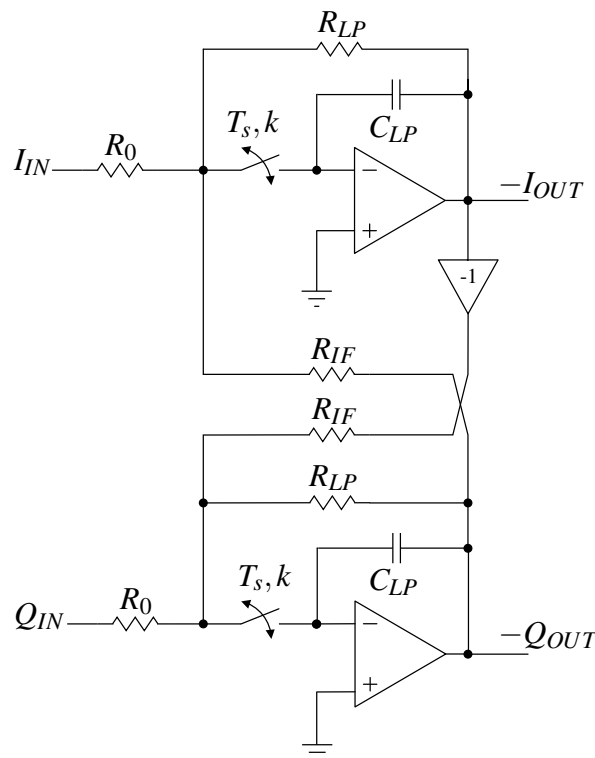


Figure 4.5: Active RC implementation with the F&H technique.

To test for the validity of the F&H technique applied to the PPF, simulations in Cadence[®] SPECTRE-RF have been performed for this first-order filter. Since changing the value of the duty-cycle affects the value of C_{LP} by the same amount, it can be seen from (4.4)–(4.6) for the F&H-PPF results the following parameter values.

$$\omega_0 = \frac{k}{R_0 \cdot C_{LP}} \quad (4.4)$$

$$\omega_{LP} = \frac{k}{R_{LP} \cdot C_{LP}} \quad (4.5)$$

$$\omega_{IF} = \frac{k}{R_{IF} \cdot C_{LP}} \quad (4.6)$$

As can be seen in figure 4.6a, as the k value increases the circuit behavior is equivalent to move the AC response from lower to higher frequencies, increasing its bandwidth and maintaining the gain at its new central frequency. Now, depending on how we assume to be the value of k_{opt} related to a chosen ω_{IF} the IRR may vary in different ways for each side, i.e. $k \leq k_{opt}$. Figure 4.6b shows the IRR possible for three given values of k_{opt} , that is, if we consider the ω_{IF} at $k_{opt} = \{0.1, 0.5, 1.0\}$. For better tuning margins, k_{opt} should be chosen as a middle value, e.g. 0.5.

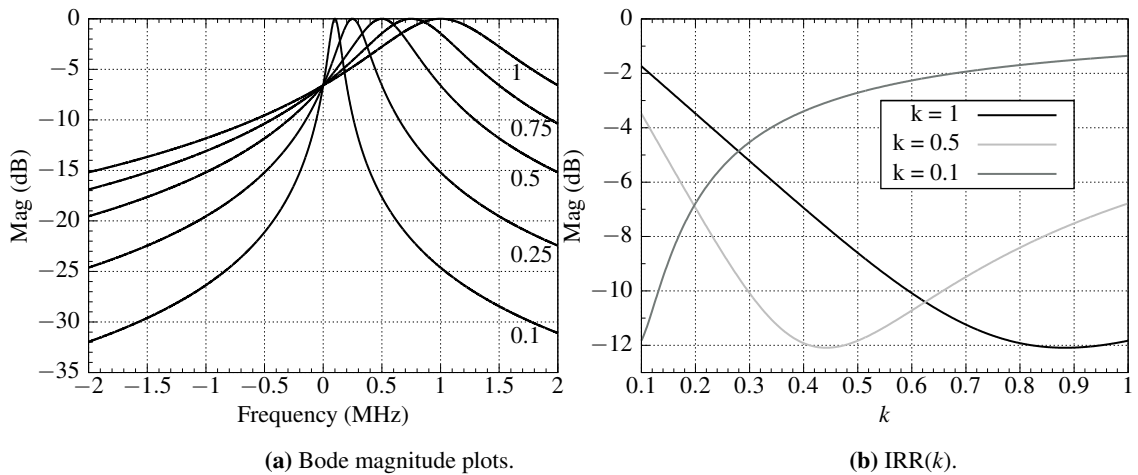


Figure 4.6: Bode magnitude plot and IRR of PPF with F&H depending on the value of k .

The simulations carried out for the PPF with the F&H showed that at least a clock of 50 MHz was needed so that the PPF transfer function did not have any attenuation in the passband.

4.2 Implementation approach

To implement the LPF prototype for the active PPF there are several possible solutions. The most common techniques used are g_m -C, active RC, MOSFET-C and g_m -C op-amp [57]. In a g_m -C integrator, we have a transconductor in which we apply an input voltage, converting it into a current that is then integrated by a capacitor, like seen in figure 4.7.

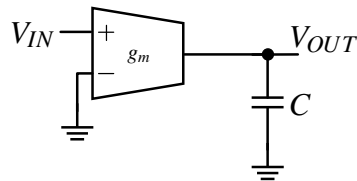


Figure 4.7: G_m -C integrator.

The unity gain frequency of this integrator is given by $\frac{g_m}{C}$. An advantage of such an integrator is the programmability achieved by simply changing the value of g_m , using for example an array of transconductors, or by changing the value of the integrating capacitor with the use of a capacitor array. A disadvantage of this integrator is its poor linearity not allowing it to perform well in wide swing applications [58].

Using this type of architecture for high frequency applications can be achieved by increasing the transconductance or using smaller capacitances. Increasing the transconductance means increasing the transistors size and the parasitic capacitances, while in the case of decreasing the integrating capacitor, the noise performance is deteriorated along with the matching between the transconductors. On both solutions the distortion increases along with the degradation of the dynamic range of the filter [59]. The g_m -C filters were used quite early in commercial applications like video in 1980 [60].

Active RC is another commonly used possibility. In this case a resistor is used to perform the voltage-to-current conversion and after that a capacitor in a feedback loop of an op-amp integrates the current. This can be seen in figure 4.8.

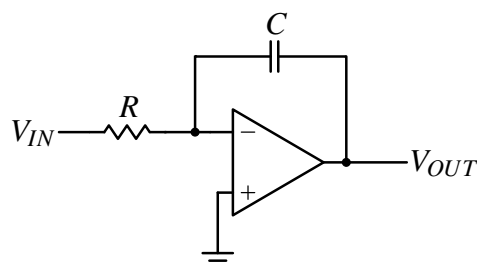


Figure 4.8: Active RC integrator.

For this integrator, the unity gain frequency is given by $\frac{1}{RC}$. Comparing to the g_m -C technique, if $\frac{1}{R}$ is made to be equal to g_m , we have an integrator with the advantage of lower noise by a factor of 2 or 3. Also this integrator can offer a high dynamic range if highly linear resistors are used in the circuit [57]. On the other hand, this technique has a limited bandwidth and a high power consumption. Also, integration in this type of architecture is not easy to achieve due to the size of the resistors and the capacitors. Another drawback is its poor tunability, since the tuning of such circuit as to be done with arrays of resistors or/and capacitors.

Another type of integrator is the MOSFET-C. In this architecture, comparing to the active RC, the resistors are replaced by MOSFETs operating in the triode region where they can be treated as resistors. This type of integrator does not suffer from even-order effects and has a noise performance equivalent to the active RC architecture [57]. The typical circuit of a MOSFET-C can be seen in figure 4.9.

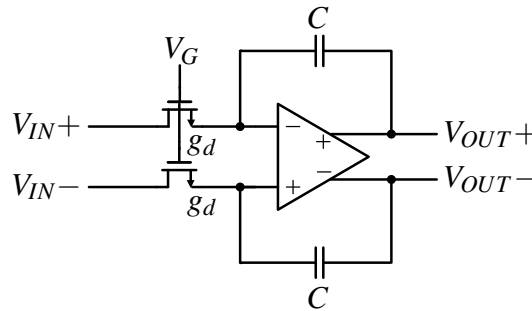


Figure 4.9: MOSFET-C integrator [57].

The value g_d represents the conductance of the MOSFET and it is dependable on the value V_G , so this architecture is tunable by changing the voltage applied to the gate of the MOSFETs, as long as this voltage maintains the MOSFETs in the triode region. This makes the tunability very limited [59] and also limits the voltage input swing [61].

The unity gain frequency for this integrator is given by $\frac{g_d}{C}$. The linearity comparing to the active RC architecture is not so good, but it has the advantage of not needing resistors [57]. Also, the active RC integrator can be transformed into a MOSFET-C where integration is easier [62], with the possibility of tuning [61] and that is insensitive to all typical nonidealities, except for the effect of the parasitic capacitances [63]. Unlike the other techniques, that can be single ended or balanced, the MOSFET-C architecture is always restricted to be balanced [57].

Another integrator that trades the resistor for another component is the g_m -C op-amp, where it is changed for a transconductor cell. This integrator, together with the two previous ones is less sensible to parasitic capacitances than the g_m -C one [57, 59], due to the fact that capacitors are in the feedback loop of an amplifier. The architecture for the g_m -C op-amp can be seen in figure 4.10.

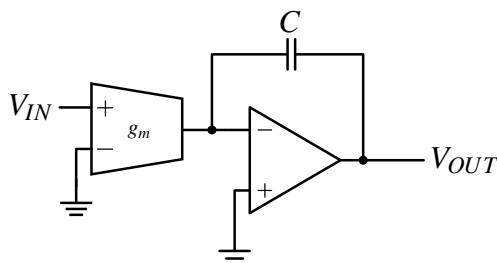


Figure 4.10: G_m -C op-amp integrator [57].

Like in the g_m -C technique, the unity frequency response is $\frac{g_m}{C}$. This architecture presents some important advantages: the leakage current in the parasitic capacitances present at the input of the op-amp is low because there is little voltage change across them; the g_m cell is easier to design due to its output being connected to a virtual ground; and, since the DC gain of the circuit is the product of the g_m cell and the op-amp DC gains, it is easier to make it high.

Power consumption is a drawback of this circuit, since it has the transconductor and the op-amp consuming power [59]. A solution to the power consumption would be the use class AB or B transconductors, since they consume less power however, they introduce crossover distortion [61]. A summary with the main drawbacks and advantages can be seen in table 4.1.

	G_m -C	Active RC	MOSFET-C	G_m -C op-amp
Influence of active elements bandwidth	Low	High	High	High
Influence of parasitic capacitances	High	Low	Low	Low
Influence of output resistance	High	Low	Low	Low
High-frequency capability	High	Moderate	Moderate	Moderate
Tunability	Medium	Very poor	Medium	Medium

Table 4.1: Integrator comparison [59].

Following, it is described the theory behind the design of a PPF for some of the architectures mentioned previously. In each architecture, one implementation for comparison purposes with the other architectures is shown with the results for a sixth-order Butterworth filter. A low-IF Bluetooth receiver is supposed to serve as application, therefore defining the frequency/bandwidth specifications.

4.2.1 G_m -C approach

To realize a first-order g_m -C LPF, two transconductors and a capacitor are needed. Figure 4.11 shows how to implement such filter.

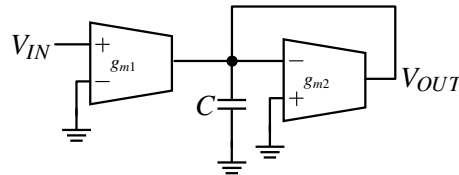


Figure 4.11: G_m -C LPF.

To prove that the above circuit works as an LPF, let us assume at the input of the circuit a signal V_{IN} . For the output current of the first transconductor, one gets:

$$i_{o1} = g_{m1} \cdot V_{IN} \quad (4.7)$$

and at the output of the second transconductor:

$$i_{o2} = -g_{m2} \cdot V_{OUT} \quad (4.8)$$

From equations (4.7)-(4.8) one can define:

$$V_{OUT} = \frac{g_{m1} \cdot V_{IN} - g_{m2} \cdot V_{OUT}}{sC} \quad (4.9)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{g_{m1}}{C}}{s + \frac{g_{m2}}{C}} \quad (4.10)$$

Comparing the above equation with the equation of a first-order LPF:

$$H_{LPF}(s) = \frac{\omega_0}{s + \omega_{LP}} \quad (4.11)$$

one can see that it represents a LPF with:

$$\omega_0 = \frac{g_{m1}}{C} \quad (4.12)$$

$$\omega_{LP} = \frac{g_{m2}}{C} \quad (4.13)$$

So, for example, to have an LPF with a cut-off frequency of $2\pi \cdot 530$ -Krad/s, it is needed a transconductor with the g_m value of 3.33 - μ A/V for a capacitor of 1 -pF.

We decided that the polyphase filter should be a frequency translation of a sixth-order Butterworth LPF. This opens the possibility to be used within the Bluetooth specifications [36]. To design a filter of such order, three cascaded LPF-biquads are used [64, 65]. The biquad is a second-order filter that possesses several features. One of the useful features is that low-pass, high-pass, band-pass and notch are often present at the nodes of the biquad, making it useful for adaptation [65]. The structure of the g_m -C LPF-biquad [66] can be seen in figure 4.12.

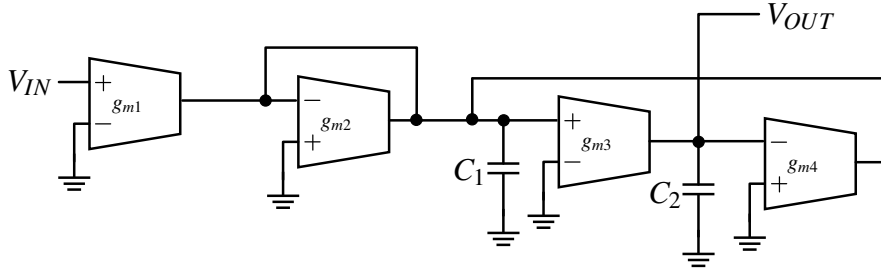


Figure 4.12: G_m -C LPF-biquad.

Doing the same exercise as we did for the first-order one gets:

$$V_{OUT} = \frac{i_{o3}}{sC_2} \quad (4.14)$$

$$i_{o3} = V_1 \cdot g_{m3} \quad (4.15)$$

$$V_1 = \frac{-i_{o4} - i_{o2} + i_{o1}}{sC_1} \quad (4.16)$$

$$i_{o4} = V_{OUT} \cdot g_{m4} \quad (4.17)$$

$$i_{o2} = V_1 \cdot g_{m2} \quad (4.18)$$

$$i_{o1} = V_{IN} \cdot g_{m1} \quad (4.19)$$

with i_{o1} , i_{o2} , i_{o3} , i_{o4} being the output current of the first, second, third and fourth transconductors respectively, and V_1 the voltage at the capacitor C_1 . Solving the equations in order of V_{OUT} one gets:

$$V_1 = \frac{-V_{OUT} \cdot g_{m4} - V_1 \cdot g_{m2} + V_{IN} \cdot g_{m1}}{sC_1} \quad (4.20)$$

$$= \frac{-V_{OUT} \cdot g_{m4} + V_{IN} \cdot g_{m1}}{sC_1 \left(1 + \frac{g_{m2}}{sC_1}\right)} \quad (4.21)$$

$$V_{OUT} = \frac{(-V_{OUT} \cdot g_{m4} + V_{IN} \cdot g_{m1}) g_{m3}}{sC_2 \cdot sC_1 \left(1 + \frac{g_{m2}}{sC_1}\right)} \quad (4.22)$$

Therefore,

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_{m1} \cdot g_{m3}}{sC_2 \cdot sC_1 \left(1 + \frac{g_{m2}}{sC_1}\right) \left(1 + \frac{g_{m4} \cdot g_{m3}}{sC_2 \cdot sC_1 \left(1 + \frac{g_{m2}}{sC_1}\right)}\right)} \quad (4.23)$$

$$= \frac{g_{m1} \cdot g_{m3}}{sC_2 \cdot sC_1 \left(1 + \frac{g_{m2}}{sC_1}\right) + g_{m4} \cdot g_{m3}} \quad (4.24)$$

$$= \frac{g_{m1} \cdot g_{m3}}{s^2 C_1 C_2 + s \cdot g_{m2} \cdot C_2 + g_{m4} \cdot g_{m3}} \quad (4.25)$$

$$= \frac{\frac{g_{m1} \cdot g_{m3} \cdot g_{m4}}{g_{m4} \cdot C_1 C_2}}{s^2 + s \frac{g_{m2}}{C_1} + \frac{g_{m3} \cdot g_{m4}}{C_1 C_2}} \quad (4.26)$$

The equation for a second-order filter is the following [66]:

$$\frac{V_{OUT}}{V_{IN}} = A_0 \frac{\omega_0^2}{s^2 + s \frac{\omega_0}{Q} + \omega_0^2} \quad (4.27)$$

Comparing equation (4.26) with equation (4.27), one can see that the DC gain (A_0), 3-dB frequency bandwidth (ω_0) and quality factor are defined by:

$$A_0 = \frac{g_{m1}}{g_{m4}} \quad (4.28)$$

$$\omega_0^2 = \frac{g_{m3} g_{m4}}{C_1 C_2} \quad (4.29)$$

$$Q = \frac{C_1}{g_{m2}} \omega_0 \quad (4.30)$$

It can be seen that equation (4.30) defines the quality factor of the filter. In the case implementing a second-order Butterworth filter, this value is equal to $\frac{1}{\sqrt{2}}$, being this value the one that presents the maximum flat response in the passband. With a value higher than this, the LPF shows a peak (overshoot) in the passband, which may lead to instability [67]. The Bode magnitude plot for an ideal Butterworth LPF-biquad can be seen in figure 4.13. It has a -3-dB cut-off frequency of 1-MHz and it can be seen that the attenuation is 40-dB per decade as expected from a second-order filter.

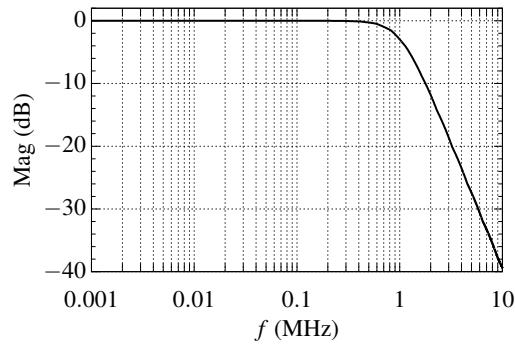


Figure 4.13: Ideal Butterworth LPF-biquad Bode magnitude plot.

Now that we know all we need about the g_m -C LPF-biquad, we can apply the F&H technique to it. When applying this technique to the g_m -C LPF-biquad, some of the transconductors will have no load at the output when the switches open. To solve this problem, the best solution found was to place an amplifier with unitary gain to force the voltage at the output of those transconductors to be the same as the voltage of the corresponding capacitors when the switches are closed, sinking the current from the g_m amplifiers.. This leads to the circuit shown in figure 4.14. This way it is guaranteed that when the main switches open (ϕ_1) the transconductors output is loaded. Notice that ϕ_1 and ϕ_2 cannot be coincident.

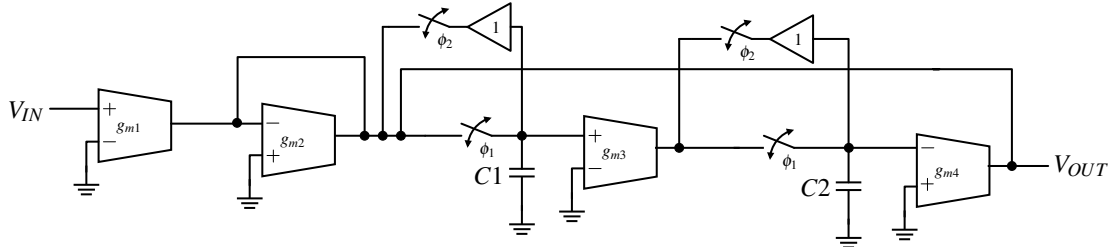


Figure 4.14: G_m -C LPF-biquad with F&H.

Figure 4.15 shows the frequency response of the Butterworth LPF-biquad with and without the F&H technique. Duty-cycles from 0.1 to 0.9 demonstrate that the cut-off frequency changes accordingly. The ideal Bode magnitude plot with the capacitor compensated for the F&H technique is also shown for comparison purposes.

It is proved that, in fact, changing the duty-cycle the cut-off frequency changes as in figure 4.3a. The data points show the frequency response with the F&H technique and the solid lines the one of the ideal circuit with the capacitor compensated for the F&H technique.

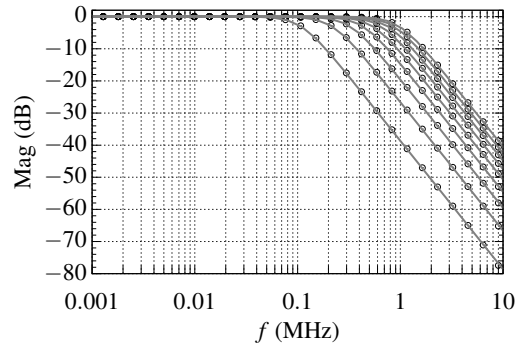


Figure 4.15: Ideal LPF-biquad Bode magnitude plot with (circles) and without F&H (solid lines) for several duty-cycles.

To implement a PPF with a g_m - C LPF, some extra circuitry needs to be added to perform the frequency translation. This is achieved by the implementation shown in figure 4.16.

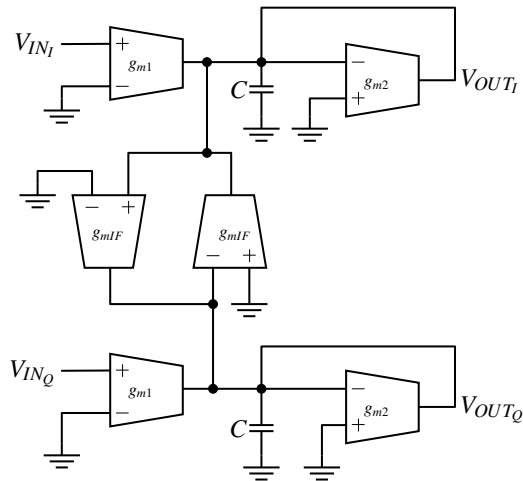


Figure 4.16: G_m - C first-order PPF.

To prove that this performs the polyphase filter implementation let us analyze the circuit by writing the voltages at the nodes in terms of the circuit component values:

$$V_{OUT_I} = \frac{i_{OUT_I}}{sC} \quad (4.31)$$

$$i_{OUT_I} = -V_{OUT_I} \cdot g_{m2} + V_{IN_I} \cdot g_{m1} - V_{OUT_Q} \cdot g_{mIF} \quad (4.32)$$

$$V_{OUT_I} = \frac{-V_{OUT_I} \cdot g_{m2} + V_{IN_I} \cdot g_{m1} - V_{OUT_Q} \cdot g_{mIF}}{sC} \quad (4.33)$$

$$= \frac{V_{IN_I} \cdot g_{m1} - V_{OUT_Q} \cdot g_{mIF}}{sC \left(1 + \frac{g_{m2}}{sC}\right)} \quad (4.34)$$

$$= \frac{V_{IN_I} \cdot \frac{g_{m1}}{C} - V_{OUT_Q} \cdot \frac{g_{mIF}}{C}}{s + \frac{g_{m2}}{C}} \quad (4.35)$$

$$= \frac{\frac{g_{m1}}{C}}{s + \frac{g_{m2}}{C}} \left(V_{IN_I} - \frac{g_{mIF}}{g_{m1}} \cdot V_{OUT_Q} \right) \quad (4.36)$$

Comparing (4.36) with (2.45) one proves that the circuit implements the PPF:

$$\omega_0 = \frac{g_{m1}}{C} \quad (4.37)$$

$$\omega_{LP} = \frac{g_{m2}}{C} \quad (4.38)$$

$$\omega_{IF} = \frac{g_{mIF}}{C} \quad (4.39)$$

The PPF can be applied to the g_m -C LPF-biquad leaving us with the circuit from figure 4.17.

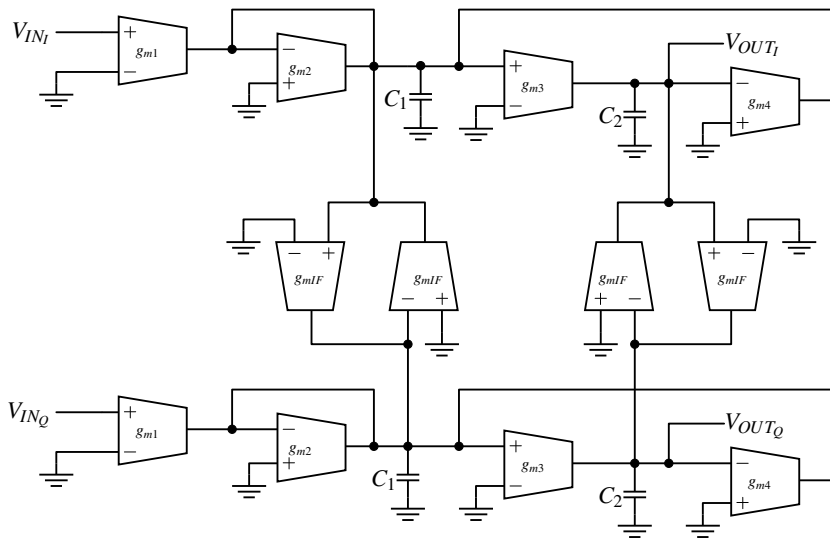


Figure 4.17: G_m -C second-order PPF.

Figure 4.18 shows the ideal Bode magnitude plot of the PPF. To plot the Bode magnitude plot of the PPF it was used PSS analysis and Periodic Transfer Function (PXF) from Cadence[®] SPECTRE-RF. The filter is centered at 2-MHz and has a -3-dB passband of 1-MHz (500-KHz for each side). The image frequency is located at -2-MHz.

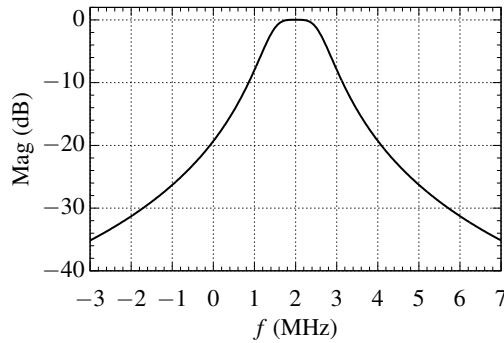


Figure 4.18: Bode magnitude plot of the ideal g_m -C second-order PPF.

Now that the PPF implementation with the g_m -C architecture has been introduced, using the g_m -C LPF-biquad with the F&H from figure 4.14, one can build the PPF with the F&H. The circuit becomes the one shown in figure 4.19.

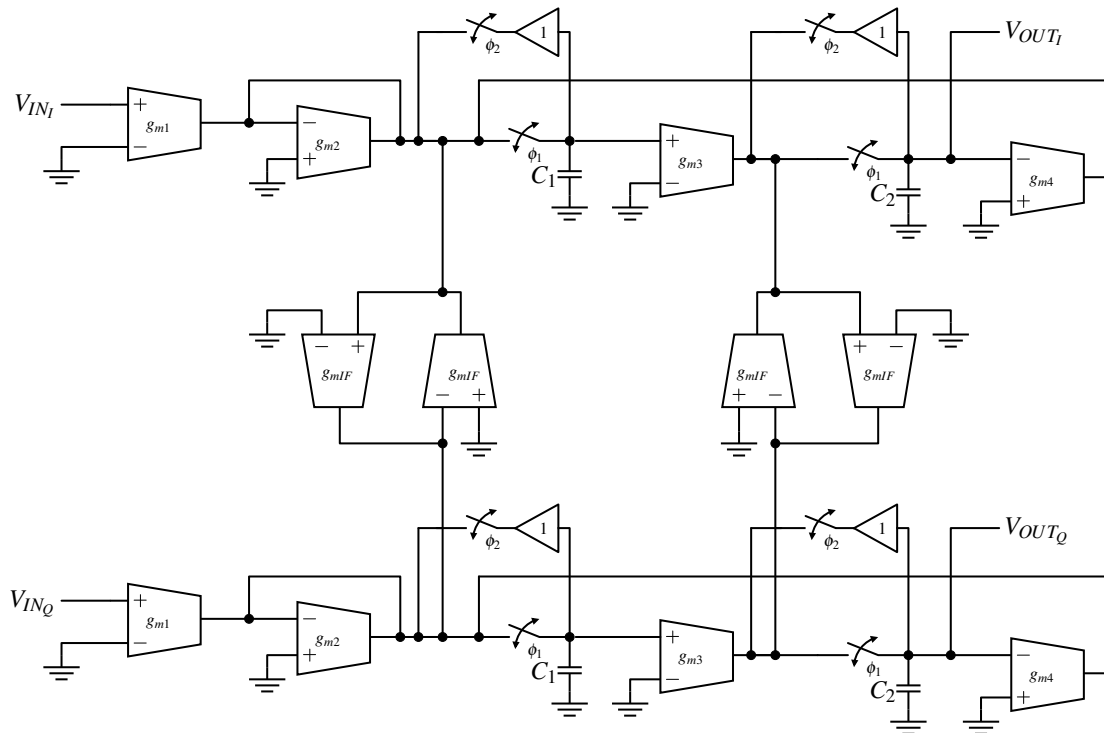


Figure 4.19: G_m -C PPF with F&H technique.

To implement the sixth-order Butterworth PPF, it is needed to cascade three circuits like the one seen in figure 4.17 or 4.19 for the circuit with the F&H technique, with the correct quality factors. This leads to the block diagram seen in figure 4.20.

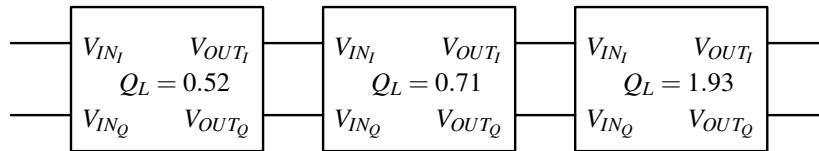


Figure 4.20: Sixth-order Butterworth PPF block diagram.

Figure 4.21 shows the transfer for the sixth-order Butterworth PPF. In the figure it is represented the continuous circuit (solid lines) and the one with the F&H technique implemented (circles) for comparison purposes. Several duty-cycles (DTs) are plotted to verify that in fact the DT changes the center frequency and the bandwidth.

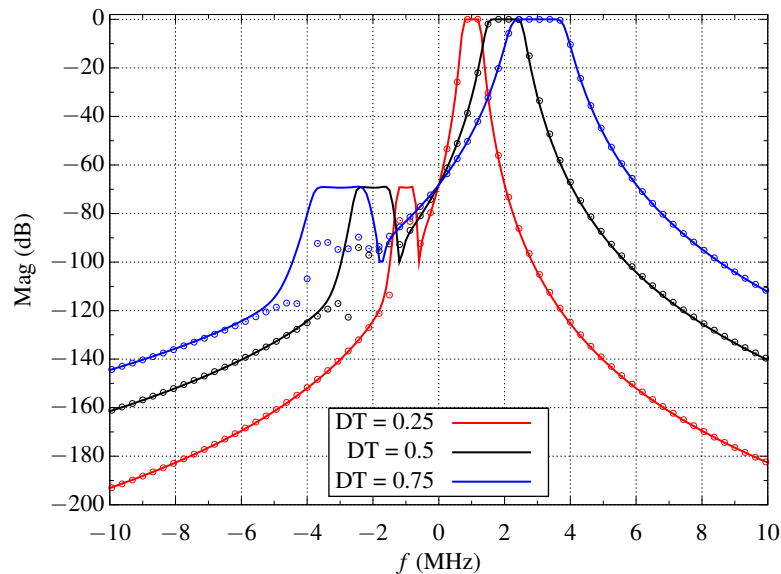


Figure 4.21: Bode magnitude plot of the ideal g_m -C sixth-order Butterworth PPF with (circles) and without F&H (solid lines) technique for several duty-cycles.

It can be seen that near the image frequency (-2-MHz) there is a bump degrading the image rejection of the filter. This is due to the finite tolerances for the simulation in SPECTRE-RF. This effect is only visible for high-order filters since the simulation error is higher than the expected signal amplitude at the image frequency. Decreasing the tolerances for the simulation (`vabstol`, `iabstol` and `reltol`) reduces this degradation, but the values needed to mitigate such effect leads to convergence issues. Throughout this document this effect is visible in the results of simulations for the different tested architectures, where a reasonable value for the simulation tolerances

has been used concerning convergence. In fact, this frequency behavior would be the same as having a mismatch and LO phase error [68], image aliasing [32] or cross-coupling between quadrature branches. Nonetheless, the image-rejection degradation seen in results of our analysis is only due to simulation issues, which are difficult to circumvent.

The duty-cycle with the value 0.5 (black circles) was chosen as the optimal value in this case, having the center frequency at 2-MHz and the -3-dB passband bandwidth being 1-MHz. The solid lines represent the frequency response of the filter without the F&H. As seen in figure, when the DT becomes 0.25 (red circles), half the optimal value, the center frequency becomes 1-MHz and the -3-dB passband bandwidth becomes 500-KHz. For DT of 0.75 (blue circles) the value of the center frequency and the -3-dB passband bandwidth become 1.5 times higher, being 3-MHz and 1.5-MHz respectively. Figure 4.22 shows the two LPFs (left side and right side) Bode plots simulated using an ideal PPF. It is seen in the figure that the left ($f < 2$ -MHz) and right ($f > 2$ -MHz) side of the function responses are coincident with themselves and with the LPF continuous frequency response (represented by the gray line).

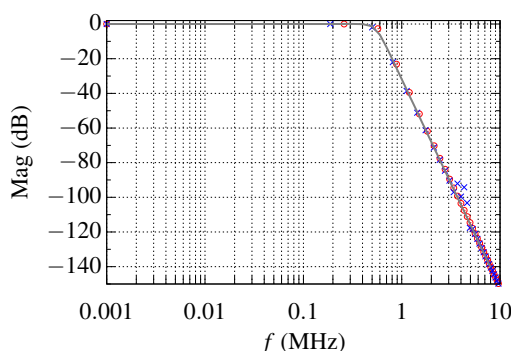


Figure 4.22: Bode plot of the left (blue crosses) and right (red circles) sides of the ideal sixth-order PPF centered at 2-MHz.

Several g_m cells were tested before implementing the PPF. Each cell add its advantages and drawbacks which will be described and analyzed in the following section.

4.2.1.1 First approach

The first OTA tested to implement the PPF was the one described in [52]. This OTA is pseudo-differential, allowing it to have wider input range and making it suitable for low power applications, but having a poor common mode gain as drawback. As it is a pseudo-differential architecture, it requires a CMFF technique to reject the common mode signal at the input and a CMFB to fix the DC common mode at the output of the OTA. The good thing about the transconductor described in this paper is that it does not need another cell to do the CMFF, thus avoiding the problem of having a cell with a possible different value of g_m due to process variations, that reduces

the CMFF rejection. Also, applying CMFB in the circuit can easily be done by connecting two of the described transconductors, not having the need to add a CM detection circuit. The circuits can be seen in figure 3.9 for the transconductor with CMFF only, and figure 3.10 with both CMFF and CMFB. To calculate the g_m of the above transconductor we need to know the current flowing out of transistors M_1 :

$$i_{1+} + i_{1-} = K_p \cdot \left(\frac{W_1}{L_1} \right) \left\{ (V_{DD} - V_{ICM} - |V_{TP}|)^2 + 0.25 \cdot V_d^2 \right\} \quad (4.40)$$

$$= \beta \cdot (V_{OV}^2 + 0.25 \cdot V_d^2) \quad (4.41)$$

with $V_{IN+} = V_{ICM} + \frac{V_d}{2}$, $V_{OUT+} = V_{ICM} - \frac{V_d}{2}$ and $V_{OV} = V_{DD} - V_{ICM} - |V_{TP}|$. It should be noticed that the CMFF mirrors to the output $\frac{i_{1+} + i_{1-}}{2}$ that contains the desired CM information. From this value, i_{1+} (for i_{OUT+}) or i_{1-} (for i_{OUT-}) is going to be subtracted and from there we get the value for the output current, which is (considering $M_4 = B \cdot M_2$):

$$i_{OUT+} = \frac{i_{1-} - i_{1+}}{2} \quad (4.42)$$

$$= \frac{B \cdot K_p \cdot \left(\frac{W_1}{L_1} \right) (V_{DD} - V_{ICM} - |V_{TP}|)}{2} V_d \quad (4.43)$$

$$i_{OUT-} = -i_{OUT+} \quad (4.44)$$

$$I_{od} = i_{OUT+} - i_{OUT-} = i_{1-} - i_{1+} \quad (4.45)$$

$$= B \cdot \beta \cdot V_{OV} \cdot V_d = g_m \cdot V_d \quad (4.46)$$

Hence, we get for g_m the value $B \cdot \beta \cdot V_{OV}$ [52]. For the circuit of the OTA with CMFB (figure 3.10), the DC level fix is obtained with transistors M_{3FB} and M_{4FB} . The voltages V_X (that depends on the voltage V_{ICM}) and the voltage V_Y (that depends on the voltage V_{ref}) are going to apply to the drain of transistors M_{3FB} and M_{4FB} the correct CM voltage.

The circuit used to implement the amplifier with unitary gain seen in figure 4.14 is the represented in figure 4.23. Figure 4.24 shows the results of the simulation to validated the LPF-biquad with the F&H implemented with this OTA.

In the figure, it is represented the frequency response of the LPF-biquad with the F&H (circles) for duty-cycles from 0.1 to 0.9. The transfer function for the circuit without F&H (solid lines) with

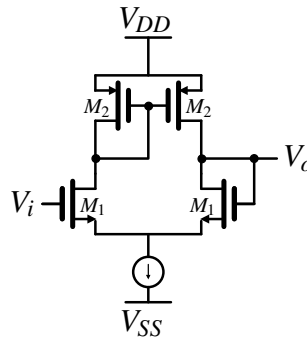


Figure 4.23: Amplifier used to fix the output voltage of some cells when the switches open.

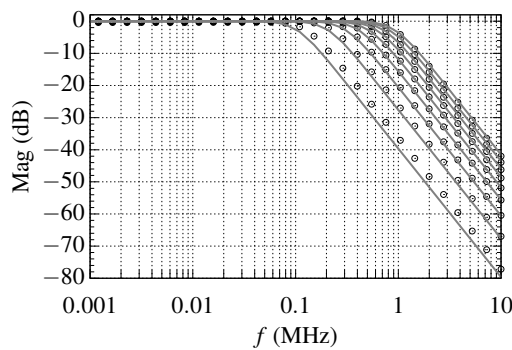


Figure 4.24: Bode magnitude plot of the LPF-biquad for several duty-cycles.

the capacitors compensated is also present for comparison purposes¹. It can be seen that the cut-off frequency changes with the duty-cycle accordingly.

While trying to implement the PPF, it was discovered that for the range of frequencies we were working with, the g_m value of the OTA was not constant. The IF could be chosen up to 1-MHz, but for higher values, an increase of $0.1\text{-}\mu\text{m}$ of size in the transistors responsible for the g_m would center the bandpass behavior at 4-MHz. As a conclusion, this was not a very stable region for the g_m . Another cause for this problem could be variations on the V_{ICM} value, but simulations showed that this value was equal at the input and output of the OTAs used in the PPF. This proved that this OTA could not be used for the proposed PPF implementation.

¹This representation of the transfer function for the circuit – with F&H plotted as circles, and the circuit without F&H with the compensated capacitor value plotted as the solid lines – is going to be used throughout this dissertation.

4.2.1.2 Second approach

The OTA described in [36] was chosen to be tested within the proposed PPF. It is also a pseudo-differential architecture like the previous. The great difference between these two OTAs is that the CMFB and CMFF in [36] are external to the main circuit, although it can lead to increased mismatches. The circuits needed to implement a PPF with this architecture can be seen in figure 3.12.

Let us analyze the circuit starting with 3.12a. This is the typical structure of a pseudo-differential OTA [69]. The value of g_m is only dependent on the NMOS sizes and voltages (M_1 on figure 3.12a) as given by [36]:

$$g_m = K_{pn} \frac{W}{L} (V_{CM} - V_{tn}) \quad (4.47)$$

The PMOS transistors (M_2 on figure 3.12a) can be biased using the circuits in figures 3.12b, 3.12c and 3.12d, depending if the circuit does not need CM control (the case of the circuit in figure 3.12b), if it only needs CMFF (the case of the circuit in figure 3.12c) or if it needs CMFF and CMFB – in this case, we need the circuit in figure 3.12c with the output connected to the NFF input of the circuit in figure 3.12d.

As mentioned above, the circuit of figure 3.12b is used when no CM control is needed. Note that this circuit transfers the input CM signal to the output, and is used in the OTAs in which the impedance at the output is low, otherwise it leads to instability [36]. The size of the transistors for this circuit is the double size of the transistors in the circuit of figure 3.12a.

To improve the CMRR of the circuit, CMFB or CMFF needs to be used. To decide which one to use we need to know if the output CM impedance is high or not. CMFF is used when the output CM impedance is low. As can be seen in figure 3.12c, what the circuit for CMFF does is to cancel the common-mode signal by subtracting it from the output of the transconductor. The inputs of this circuit are the inputs of the circuit of the transconductor. Notice that the transistors in this circuit should have the same size as the transistors of the circuit from the transconductor (M_5 equal to M_1 and M_6 equal to M_2). In the case of the CM impedance being high and to fix the output DC value, CMFB is used. To apply a CMFB to the circuit, the circuit in figure 3.12c is used in the same conditions as above, but now the output is connected to the respective input in the circuit of figure 3.12d and at the other input the CM signal. In these circumstances, at the output of the circuit we will have the value to bias the transconductor correctly in order to define the DC value at the output of the transconductor. The sizes of transistors in this circuit are the double size of the transistors in the transconductor (M_8 twice the size of M_1 and M_6 twice the size of M_2). Following, the results of the simulation for the LPF-biquad are shown in figure 4.25.

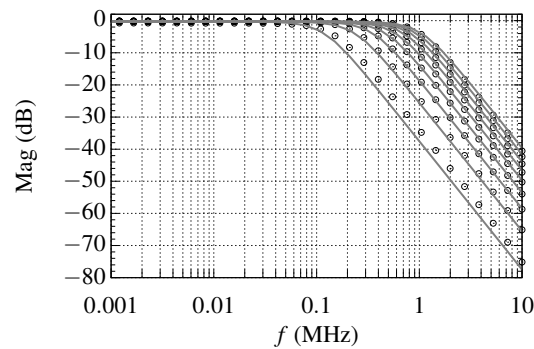


Figure 4.25: Bode magnitude plot of LPF-biquad with F&H (circles) and without it (solid lines) for several duty-cycles.

In the figure it is depicted the Bode magnitude plot of the circuit with F&H, for duty-cycles of 0.1 to 0.9, and without F&H with the compensated capacitor values. It can be seen that the plots are coincident except for small deviations at higher frequencies, demonstrating that the circuit acts as intended when changing the duty-cycles.

Figure 4.26 shows the Bode plot magnitude of the PPF with F&H for several duty-cycles. The frequency response of the continuous-time version is also included for comparison. The greatest difference between the circuit with F&H and the one without it is the gain in the passband, which is more or less 2-dB lower. When trying to implement the sixth-order Butterworth PPF for this approach, some problems arise. The CM voltage changes at the input of every transconductor, resulting in a frequency behavior that is quite different from the desired. Hence, the alternative was to try other circuits where the g_m was not dependent on the CM voltage.

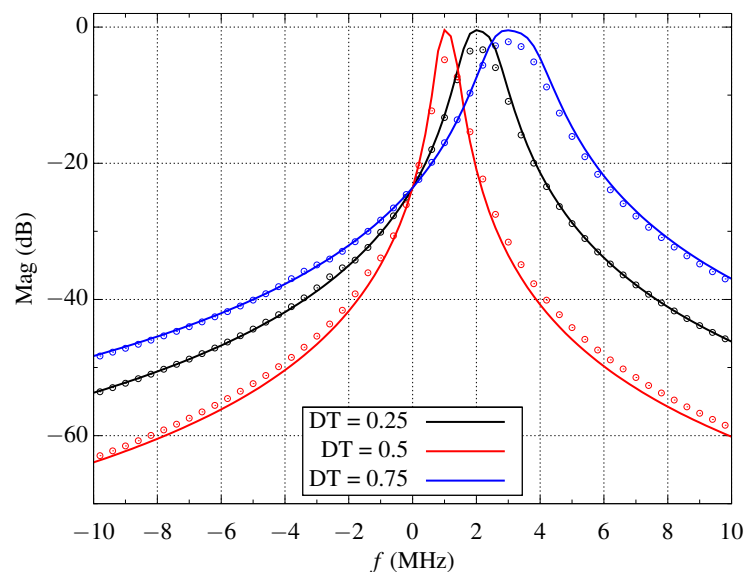


Figure 4.26: Bode magnitude plot of the second-order PPF with F&H (circles) and without it (solid lines).

4.2.1.3 Third approach

In this third approach the OTA described in [53, 70] was chosen to implement the PPF, hereafter called as Nauta's OTA. This OTA is based on the CMOS inverter with the transistors working in the saturation region. Since it is based on inverters, its very suitable for low-voltage applications [54]. This is a fully-differential OTA, thus having a smaller dynamic range compared to the pseudo-differential versions [36]. This may not be a problem since the voltages it will have to handle are not high. The circuit for this OTA can be seen in figure 3.11.

The g_m of this transconductor cell is given by [53, 70]:

$$g_m = (V_{DD} - V_{tn} + V_{tp}) \sqrt{\beta_n \cdot \beta_p} \quad (4.48)$$

The transistors that are taken into account for the g_m value are those from inverters 1 and 2 (Inv_1 and Inv_2 in figure 3.11). The other four inverters are responsible for ensuring CM stability [71, 53, 70]. When designing such transconductor, the inverters, Inv_1 and Inv_2 , transistors sizes should meet the requirement of $\beta_n = \beta_p$, although for the CM stability this is not absolutely necessary.

Let us assume $\beta_n = \beta_p$. The inverters Inv_4 and Inv_5 are connected as resistors between the output node and the CM voltage. The equivalent value of the resistors is $\frac{1}{g_{m4}}$ and $\frac{1}{g_{m5}}$ respectively. The inverters Inv_3 and Inv_6 are injecting current in these two resistors (Inv_3 in Inv_4 , and Inv_6 and Inv_5) with values $g_{m3}(V_c - V_{OUT-})$ and $g_{m6}(V_c - V_{OUT+})$, respectively. Here V_{OUT-} corresponds to the i_{OUT-} output and V_{OUT+} corresponds to the i_{OUT+} output.

In the presence of CM signals, the output i_{OUT-} is loaded with a resistor $\frac{1}{g_{m5} + g_{m6}}$ and the output i_{OUT+} is loaded with a resistor $\frac{1}{g_{m3} + g_{m4}}$. In the case of differential signals, the output i_{OUT-} is loaded with a resistor $\frac{1}{g_{m5} - g_{m6}}$ and the output i_{OUT+} is loaded with a resistor $\frac{1}{g_{m3} - g_{m4}}$. Since we have assumed $\beta_n = \beta_p$ and if V_{DD} is the same for all of the inverters, we have a low resistance load for CM signals and a high resistance load for differential signals, which results in a controlled CM voltage at the outputs. If $\beta_n \neq \beta_p$ or if V_{DD} is different in inverters Inv_3 to Inv_6 , the load resistance is nonlinear for CM signals only [70].

Figure 4.27 shows the Bode magnitude plot of the LPF-biquad based on the Nauta's transconductor. In this figure the results for several duty-cycles are plotted, from 0.1 to 0.9 for the circuit with F&H, and the also the frequency response for the circuit without F&H with the capacitor compensated for each duty-cycle.

It can be seen that increasing and decreasing the duty-cycle in fact changes the cut-off frequency but the more we decrease or increase the duty-cycle the more the LPF behavior deviates from the LPF without the F&H. This is due to the amplifier used as load.

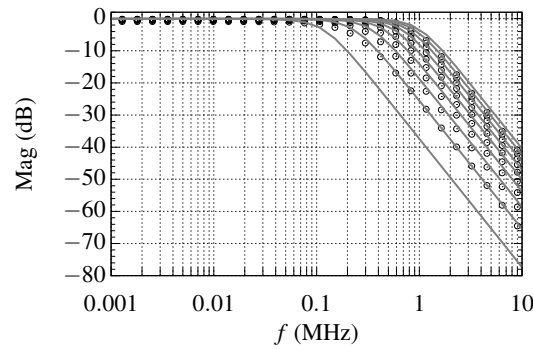
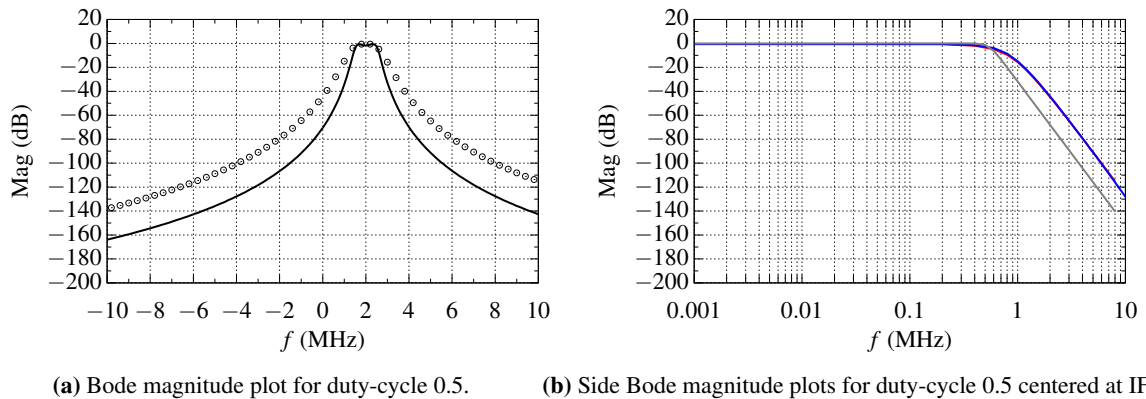


Figure 4.27: Bode magnitude plot of LPF-biquad with F&H (circles) and without it (solid lines) for several duty-cycles.

Figures 4.28 and 4.29 show the Bode magnitude plot of the PPF implementation with Nauta's transconductor. It is included the frequency behavior for duty-cycles of 0.25, 0.5 and 0.75 for the circuit with F&H and the correspondent without the F&H (with the capacitor value compensated).



(a) Bode magnitude plot for duty-cycle 0.5.

(b) Side Bode magnitude plots for duty-cycle 0.5 centered at IF.

Figure 4.28: Bode magnitude plots of the sixth-order Butterworth PPF with Nauta's OTA and side LPF for a duty-cycle of 0.5.

The first results shown an attenuation of -15.2-dB in the passband for the duty-cycle of 0.5 (optimal value). So, the present results were obtained following some compensation, introduced with the increase of the transconductance value g_{m1} . Also, the quality factor of the filter was degraded when compared to the ideal solution, and it could not be equal to the LPF response (gray line) as seen in figure 4.28b. The left side (blue line) and the right side (red line), are coincident, which means that the filter is completely symmetrical at the center frequency (IF). The size reduction of the capacitor ($C_{no\ FH}/C_{FH}$) was of 1.95 and the IRR of this circuit is about 78.5-dB.

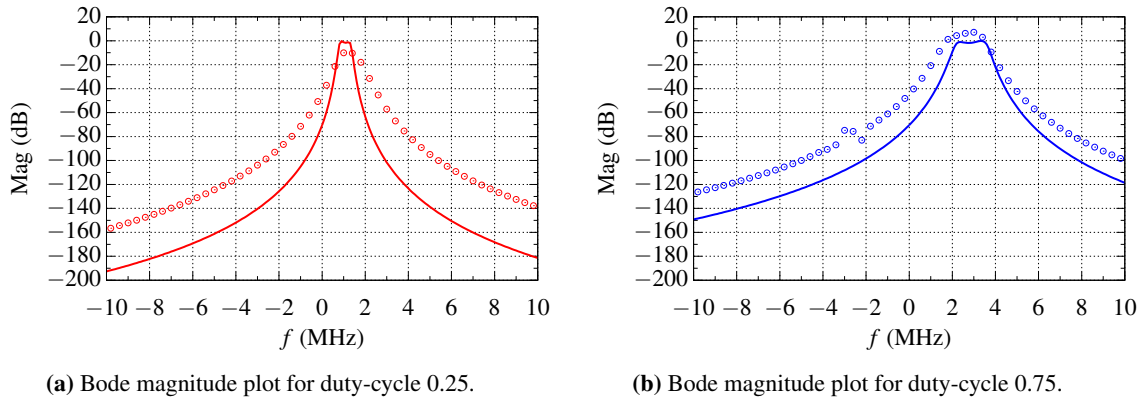


Figure 4.29: Bode magnitude plots of the sixth-order Butterworth PPF with Nauta's OTA for a duty-cycle of 0.25 and 0.75.

Figure 4.29 shows that changing the duty-cycle in fact changes the center frequency and the passband of the frequency response, although it is not coincident with the circuit without the F&H as expected from the results seen in figure 4.27. It can also be noted that changing the duty-cycle, the passband gain changes. This proves that the switching operation is deteriorating the passband gain of the filter. The reasons why this happens are the clock feedthrough and the series resistance of the switches. These effects could not be eliminated, although they were minimized by changing device sizes.

4.2.2 Active RC approach

In this section the PPF design is presented for the active RC architecture. The theoretical explanation will be minimal since it was already presented in chapter 2 and it is similar to the g_m -C architecture. The circuit that implements the active RC LPF-biquad for the single-ended version² is shown in figure 4.30 [67, 72]. The last op-amp in the circuit together with the resistors R is used to invert the output signal for the feedback. In fully-differential architecture there is no need for this amplifier since inverted signals can be achieved at any op-amp output.

The transfer function for this circuit is given by [72]:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{R_3}{R_1} \cdot \frac{1}{R_3 R_4 C_1 C_2}}{s^2 + s \cdot \frac{1}{R_2 C_1} + \frac{1}{R_3 R_4 C_1 C_2}} \quad (4.49)$$

²Also known as the Tow-Thomas biquad.

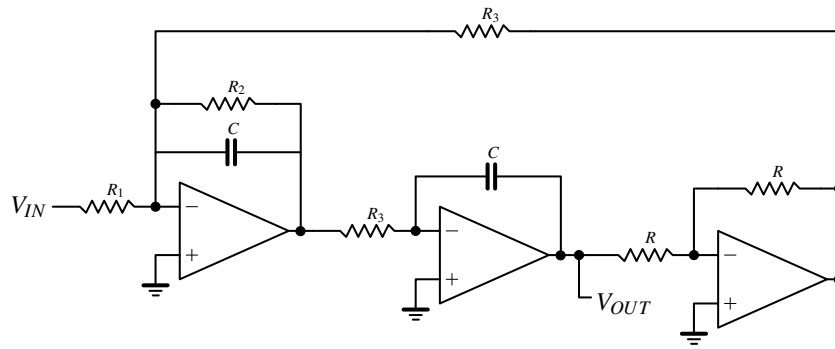


Figure 4.30: Active RC LPF-biquad.

Comparing equation (4.49) with equation (4.27) one can see that they are the same, having:

$$A_0 = \frac{R_3}{R_1} \tag{4.50}$$

$$\omega_0^2 = \frac{1}{R_3 R_4 C_1 C_2} \tag{4.51}$$

$$Q = \frac{1}{R_2 C_1} \omega_0 \tag{4.52}$$

proving that the circuit in fact represents the LPF-biquad.

To apply the F&H technique in the circuit, the switches must be placed as seen in figure 4.31.

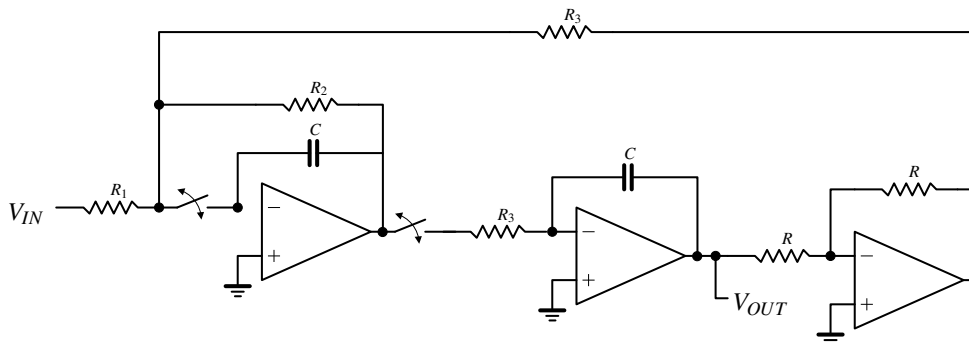


Figure 4.31: Active RC LPF-biquad F&H.

Figure 4.32 shows that the above circuit implements the active RC LPF-biquad with the F&H technique.

In the figure it is depicted the Bode magnitude plot of the active RC LPF-biquad circuit with the F&H technique for duty-cycles from 0.1 to 0.9. The results from the version without the F&H technique is also shown for comparison purposes, with compensated capacitors for each duty-cycle. It can be seen that when changing the duty-cycle, the cut-off frequency changes accordingly and is coincident with the version without the F&H technique.

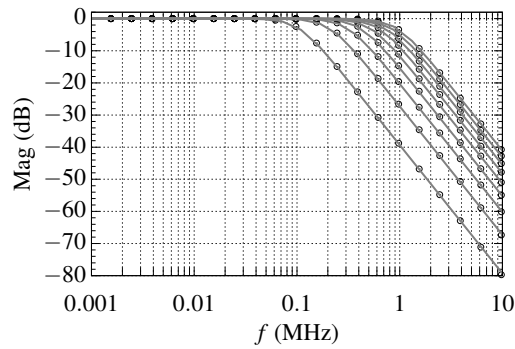


Figure 4.32: Active RC LPF-biquad with F&H (circles) and without it (solid lines) ideal Bode magnitude plot for several duty-cycles.

The PPF implemented with the active RC technique can be seen in figure 4.33. In this circuit, the frequency translation of the LPF-biquad is achieved by the resistors R_4 . Once again, an op-amp with gain -1 is needed in the frequency translation due to the fact of not having differential outputs.

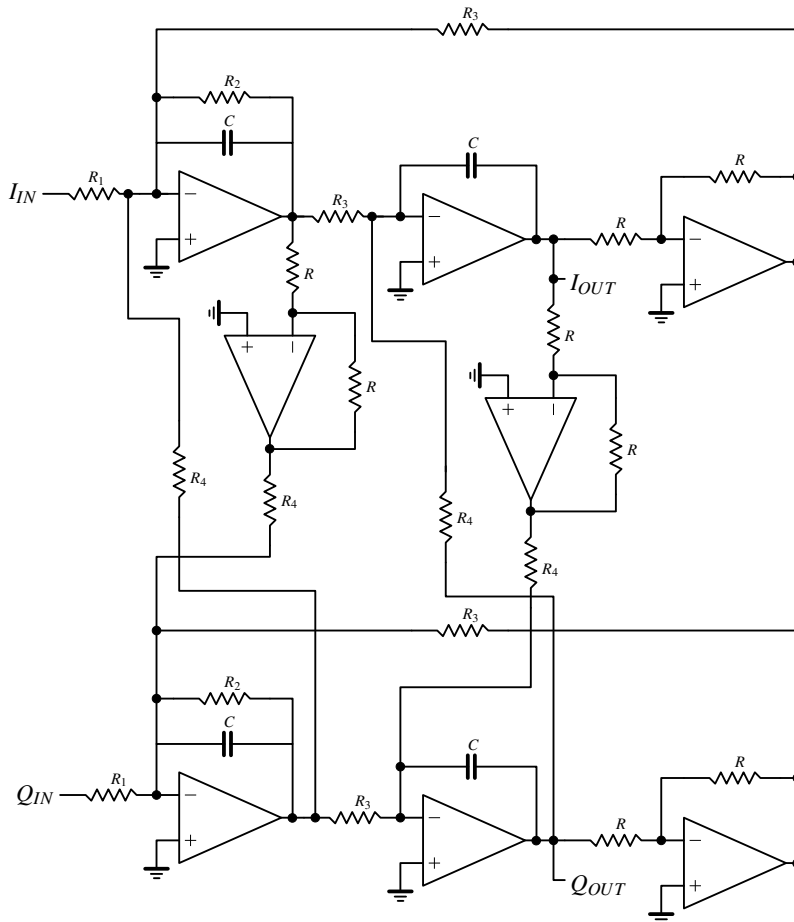


Figure 4.33: Active RC PPF.

The active RC PPF with the F&H technique can be achieved with the circuit present in figure 4.34. To demonstrate that the circuit implements the PPF, the Bode magnitude plot of the sixth-order PPF Butterworth is plotted in figure 4.35. Several duty-cycles are tested, 0.25, 0.5 and 0.75, along with the version without the F&H technique with the capacitors compensated for comparison purposes.

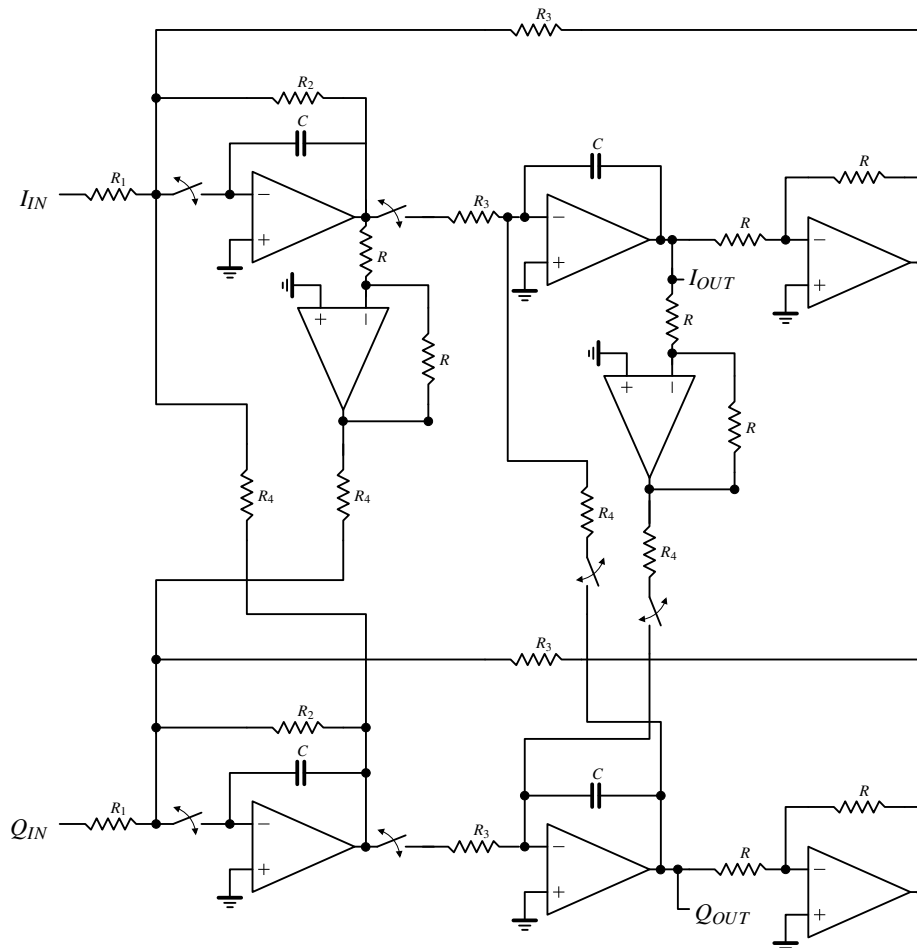


Figure 4.34: Active RC PPF F&H.

It can be seen that the circuit works as intended and that changing the duty-cycle in fact changes the center frequency and the passband bandwidth. Moreover, this behavior is coincident with the PPF version without F&H. The passband gain is 6.02-dB. Since this is a single balanced version, at the output we have the same result as if we added the frequency responses of the circuit with differential outputs. Figure 4.36 shows the two LPFs (left side and right side) Bode magnitude plot in a log-scale at IF. It is seen in the figure that the left and right side of the frequency responses are coincident with themselves and with the LPF continuous frequency response, represented by the gray line.

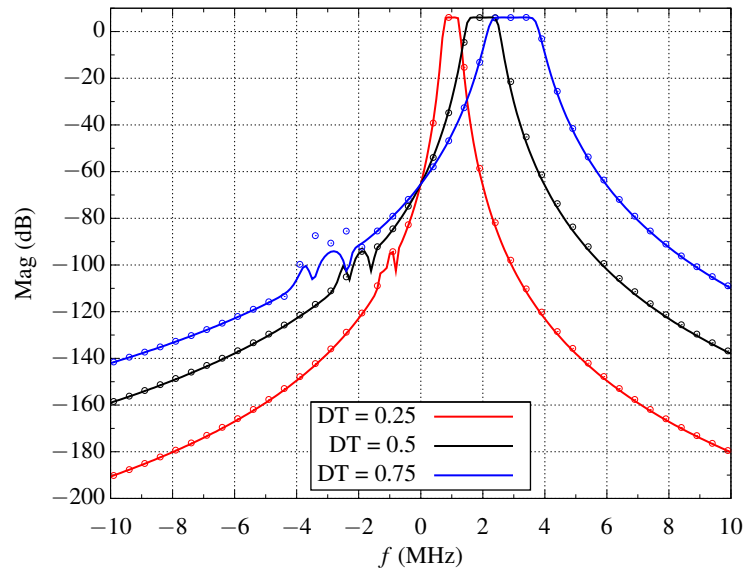


Figure 4.35: Active RC sixth-order Butterworth PPF with F&H (circles) and without it (solid lines) ideal Bode magnitude plot for several duty-cycles.

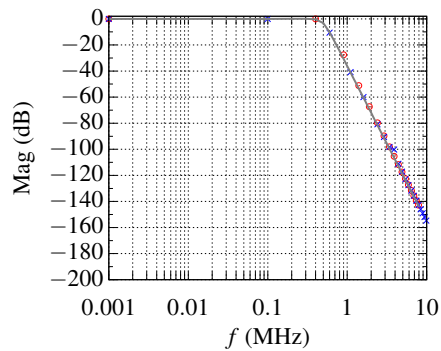


Figure 4.36: Bode magnitude plot of the left (blue crosses) and right (red circles) sides of the ideal sixth-order PPF centered at IF.

To implement the op-amp for the active RC architecture, one op-amp provided by ams foundry (CMOS $0.35\text{-}\mu\text{m}$) was used. The main characteristics of this op-amp can be seen in table 4.2 [73].

	Min	Typ	Max	Unit
Output resistance @ 1 KHz	0.22	0.34	0.56	Ω
Open loop gain	77	86	92	dB
Gain Bandwidth (GBW)	34.58	49.78	75.37	MHz
CMRR @ 1 KHz	85	92	95	dB
Total Harmonic Distortion @ 1 KHz	-130	-120	-79	dB
Power Consumption	3.41	6.06	11.87	mW

Table 4.2: Op-amp characteristics [73].

Figure 4.37 shows the Bode magnitude plot for the active RC LPF-biquad with the F&H technique for duty-cycles from 0.1 to 0.9. The results for the circuit without the F&H technique with the capacitor compensated are also presented for comparison purposes.

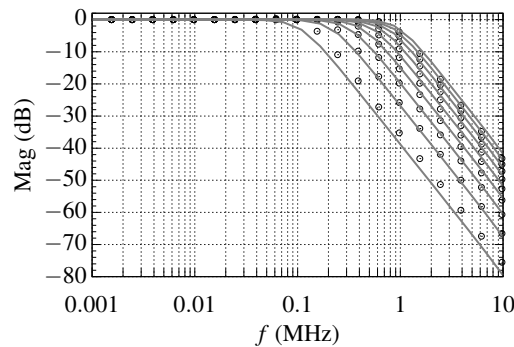
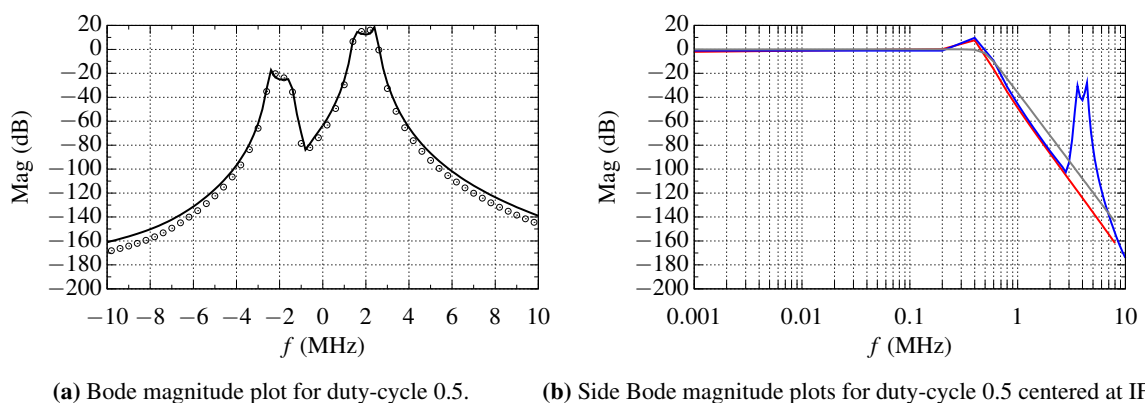


Figure 4.37: Active RC LPF-biquad with F&H (circles) and without it (solid lines) Bode magnitude plot for several duty-cycles.

It can be seen that changing the duty-cycle changes the cut-off frequency, and it is almost coincident with the frequency behavior of the circuit without F&H, except for the duty-cycle of 0.1. The size reduction achieved was 1.74 for the same cut-off frequency at the 0.5 duty-cycle.

Figures (4.38)-(4.39) show the Bode magnitude plot of the sixth-order Butterworth PPF with the F&H technique for several duty-cycles. It can be seen that changing the duty-cycle changes the center frequency as well as the passband bandwidth. The frequency behavior for the circuit without the F&H technique with the capacitors compensated is also plotted for comparison purposes.



(a) Bode magnitude plot for duty-cycle 0.5.

(b) Side Bode magnitude plots for duty-cycle 0.5 centered at IF.

Figure 4.38: Bode magnitude plots of the active RC implementation of the sixth-order Butterworth PPF and side LPF for a duty-cycle of 0.5.

From the figure 4.38, it can be seen that the plotted results are very similar. The passband gain is more than the expected 6.02dB. This was achieved without changing the gain parameters of the filter. The IRR of the filter is about 41.5-dB. For the side frequency responses, it can be noticed

that the quality factor of the filter is being affected, showing a peak in the passband and thus making the response of the filter a little different from the Butterworth filter proposed. This is the consequence of the finite GBW of the amplifier [74]. Despite this, the -3-dB passband bandwidth of 1.06-MHz is achieved. For a clear representation, the gain was reduced to 0-dB in the figure 4.38b.

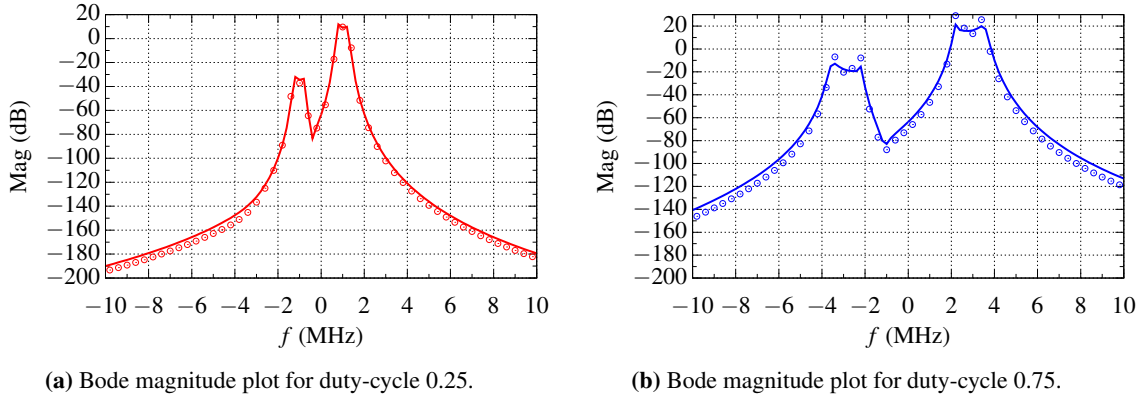


Figure 4.39: Bode magnitude plots of the active RC implementation of the sixth-order Butterworth PPF for a duty-cycle of 0.25 and 0.75.

Figures 4.39a and 4.39b show the Bode magnitude plot for the duty-cycles of 0.25 and 0.75. It can be seen that the changes in the center frequency and the passband bandwidth are in accordance with the frequency behavior of the circuit without the F&H.

4.2.3 MOSFET-C approach

In this section the polyphase filter design is presented for the MOSFET-C architecture. The theoretical basis is similar to the active RC architecture. The LPF-biquad version of the MOSFET-C architecture can be seen in figure 4.40 [62]. As the circuit is the same as the active RC architecture, the transfer function for this circuit is the same as 4.49 except for the resistors that are replaced by the equivalent transconductance of the MOSFETs, represented by g_d in equation (4.53).

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{g_{d1}}{g_{d3}} \cdot \frac{g_{d3}g_{d4}}{C_1C_2}}{s^2 + s\frac{g_{d2}}{C_1} + \frac{g_{d3}g_{d4}}{C_1C_2}} \quad (4.53)$$

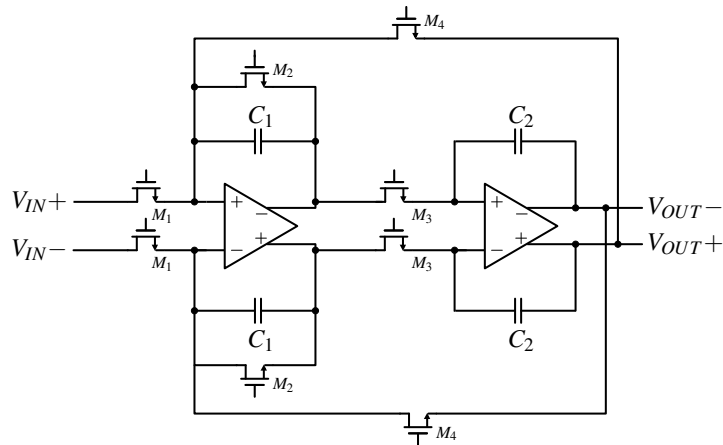


Figure 4.40: MOSFET-C LPF-biquad.

The DC gain, the -3-dB cut-off frequency and the quality factor are given by the following values:

$$A_0 = \frac{gd1}{gd3} \tag{4.54}$$

$$\omega_0^2 = \frac{gd3gd4}{C_1C_2} \tag{4.55}$$

$$Q = \frac{gd2}{C_1} \omega_0 \tag{4.56}$$

To implement the F&H technique in the MOSFET-C LPF-biquad, the switches should be placed as seen in figure 4.41.

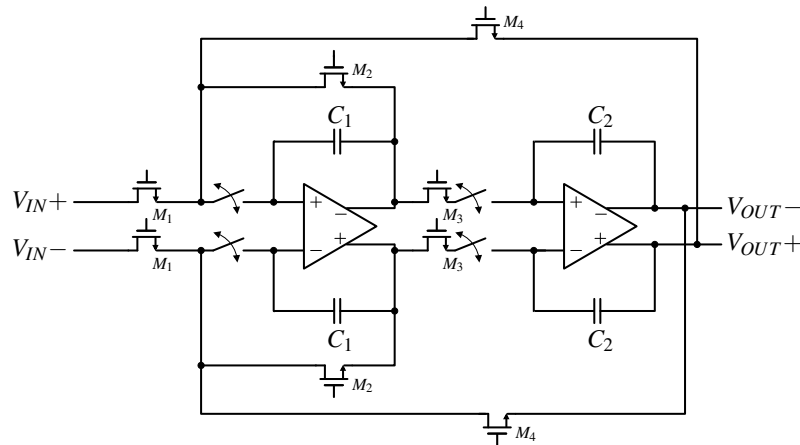


Figure 4.41: MOSFET-C LPF-biquad F&H.

To prove that the circuit in fact implements the MOSFET-C LPF-biquad with the F&H technique, figure 4.42 shows its Bode magnitude plot. The results with the circuit without the F&H technique with the capacitor compensated are also depicted for comparison purposes.

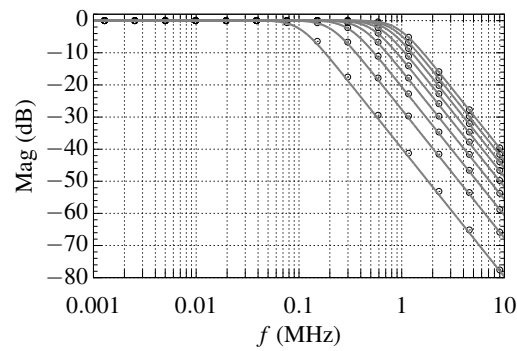


Figure 4.42: MOSFET-C LPF-biquad with F&H (circles) and without it (solid lines) ideal Bode magnitude plot for several duty-cycles.

It can be seen that the frequency responses are coincident and that changing the duty-cycle, changes the cut-off frequency accordingly. The MOSFET-C LPF-biquad circuit can implement the PPF, using the circuit in figure 4.43.

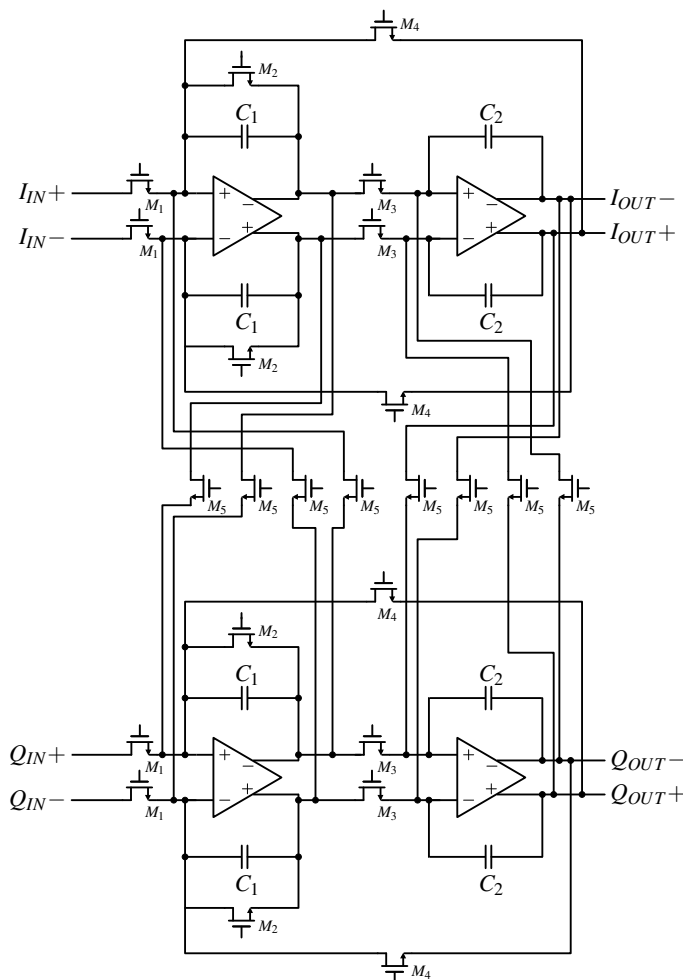


Figure 4.43: MOSFET-C PPF.

Notice that eight MOSFETs (all denoted M_5) were added to the circuit to perform the frequency translation. To implement the F&H technique in the circuit from figure 4.43, the switches should be placed as seen in 4.44.

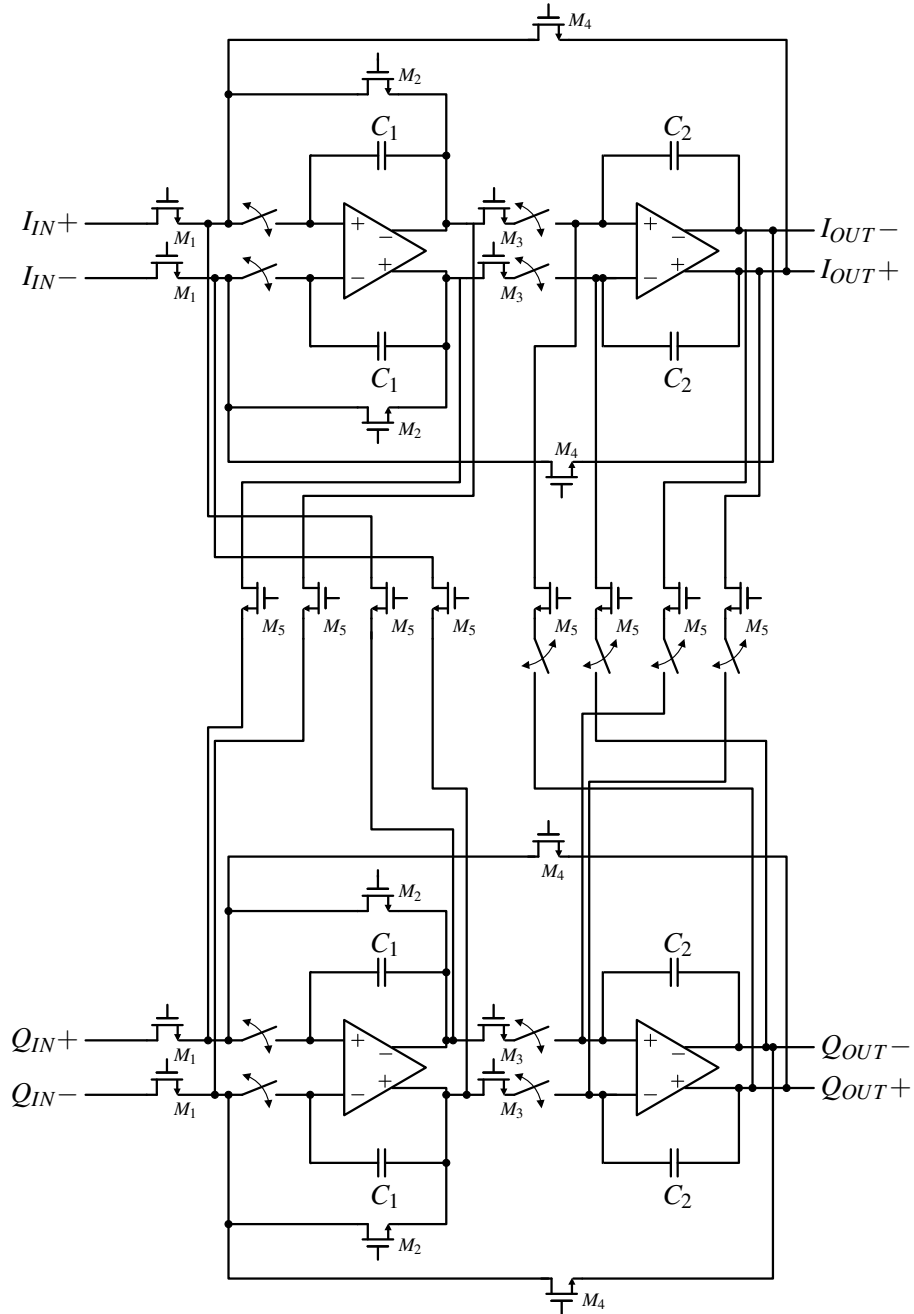


Figure 4.44: MOSFET-C PPF F&H.

Results in figure 4.45 demonstrate that the circuit implements the PPF as intended. It is depicted the sixth-order Butterworth PPF by the Bode magnitude plot with the F&H for duty-cycles of 0.25, 0.5 and 0.75. The results from the circuit without the F&H is also shown for comparison purposes. It can be seen that changing the duty-cycle changes the center frequency and the passband bandwidth accordingly.

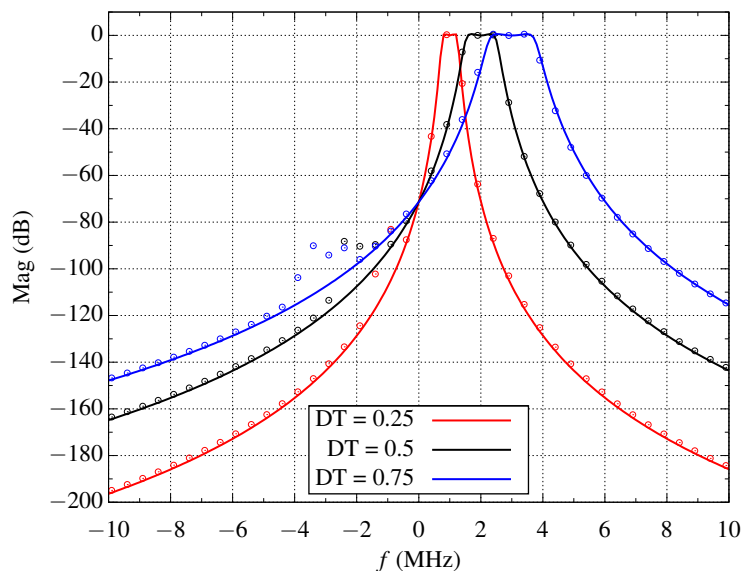


Figure 4.45: MOSFET-C sixth-order Butterworth PPF with F&H (circles) and without it (solid lines) ideal Bode magnitude plot for several duty-cycles.

In figure 4.46 the Bode magnitude plot is shown for both sides of the PPF centered at IF, as well as the sixth-order LPF for comparison. It is seen in the figure that the left and right side of the frequency behavior are coincident with themselves and with the LPF continuous frequency response, represented with a gray line.

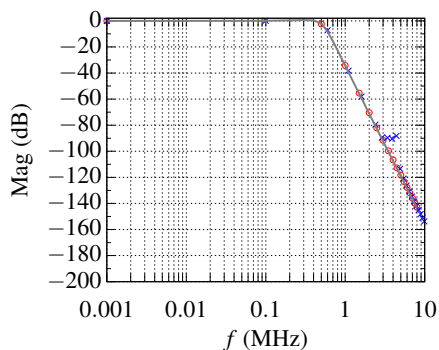


Figure 4.46: Bode magnitude plot of the left (blue crosses) and right (red circles) sides of the ideal sixth-order PPF centered at IF.

To implement the MOSFET-C version of the PPF filter the amplifier seen in figure 4.47 was used. This is a modified version of the amplifier found in [75].

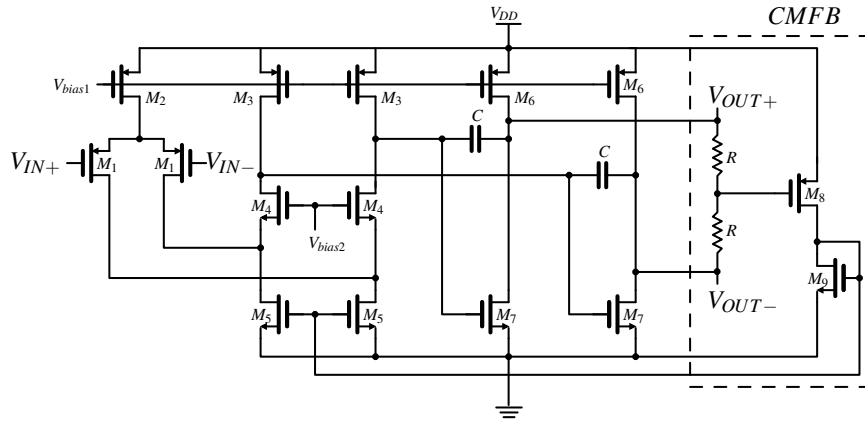


Figure 4.47: Folded cascode amplifier for MOSFET-C filter.

This amplifier is a two-stage differential folded cascode. It has a DC gain of 45.81-dB and GBW of 350-MHz, which is enough for the PPF implementation. The Bode magnitude plot of the MOSFET-C LPF-biquad implementation can be seen in figure 4.48. The results for F&H for duty-cycles from 0.1 to 0.9 are plotted in figure. For comparison purposes, the results from the circuit without F&H are also included.

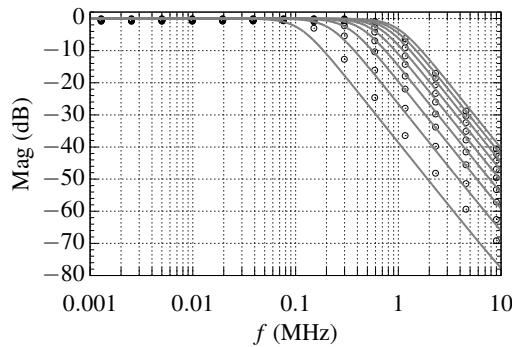


Figure 4.48: MOSFET-C LPF-biquad with F&H (circles) and without it (solid lines) Bode magnitude plot for several duty-cycles.

It can be seen that changing the duty-cycle changes the cut-off frequency. Also, it is coincident with the Bode magnitude plot of the circuit without the F&H except for a small deviation at the duty-cycle of 0.1. The size reduction achieved in the MOSFET-C is about 1.653. Following, in figures 4.49 and 4.50 the Bode magnitude plots are depicted for the PPF with duty-cycles of 0.25, 0.5 and 0.75. In figure 4.49b it is shown the side LPF frequency response of the PPF with duty-cycle 0.5 for comparison with the ideal sixth-order filter. The circuit presents an attenuation in the passband of 13-dB and this was compensated by increasing the conductance of transistor M_1 in the filter.

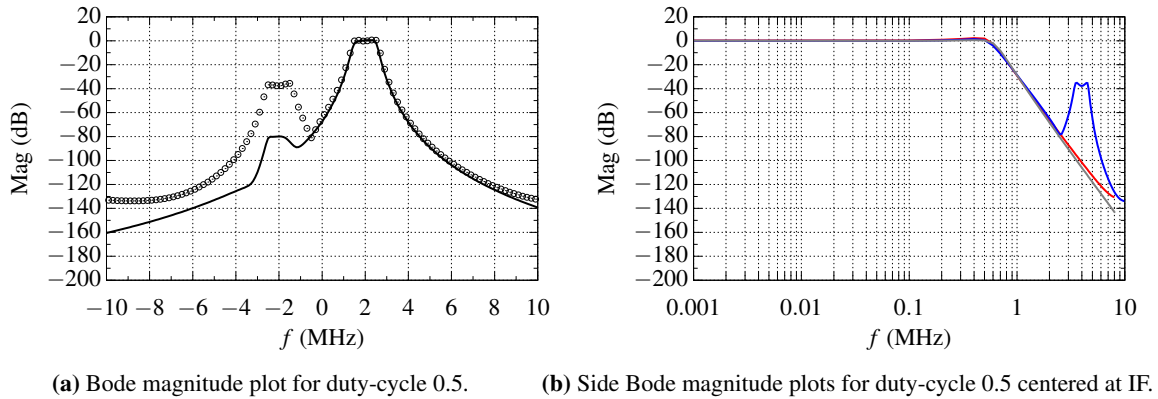


Figure 4.49: Bode magnitude plots of the MOSFET-C implementation of the sixth-order Butterworth PPF and side LPF for a duty-cycle of 0.5.

It can be seen that the frequency response of the F&H implementation is coincident with the circuit without it up to 6-MHz. This effect is due to the finite GBW of the amplifier, which degraded when including the switch operation. This is also the cause for the peaks present in the passband, as seen in the active RC architecture. The same can be seen in figures 4.50a and 4.50b, where decreasing the duty-cycle affects even more the filter response. Also in these figures it can be seen that changing the duty-cycle changes the center frequency and the passband bandwidth.

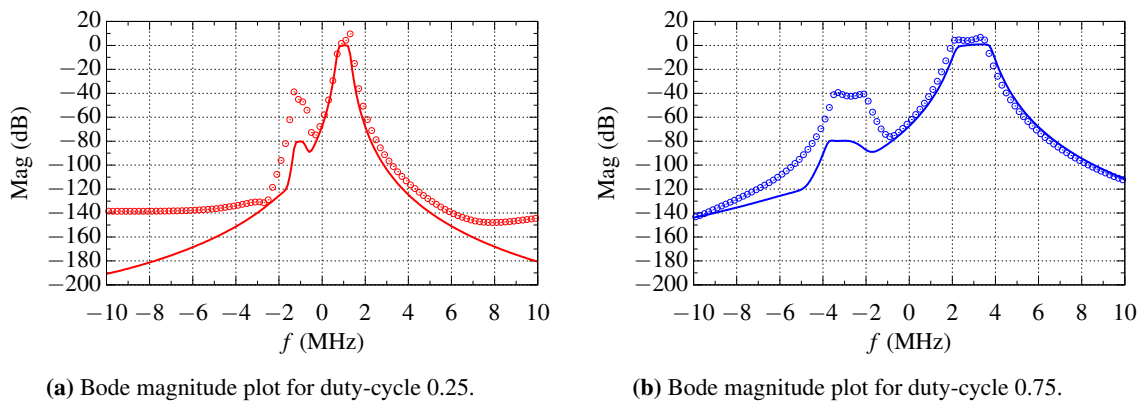


Figure 4.50: Bode magnitude plots of the MOSFET-C implementation of the sixth-order Butterworth PPF for duty-cycles of 0.25 and 0.75.

Chapter 5

Conclusion

In this chapter the approaches for the three PPF architectures presented in last sections are firstly compared. The g_m -C is chosen as the most indicated and further results are included. Following, the conclusions of this work will be presented and the future work described.

5.1 Results

Table 5.1 presents a summary with the most important results of the implementations from chapter 4. Analyzing the results, we can conclude that the best implementation is the one with the g_m -C since it is the one that presents the best performance for all the figures of merit.

	G_m -C	Active RC	MOSFET-C	Unit
Power consumption	15.55	378.8	57.67	mW
Reduction achieved ($C_{no FH}/C_{FH}$)	1.95	1.74	1.653	-
IRR	78.5	41.5	37	dB

Table 5.1: PPF implementations summary.

Comparing the PPF having the F&H implementation using g_m -C cells with the one without the F&H, we obtain a PPF with an IRR 28.2-dB lower, with a power consumption increase of 27.5% but with a decrease in the size of the capacitor of 1.95. The loss in the IRR is a minor loss when considering, for example, the IRR requirement for a Bluetooth receiver. Simulations of the present solution demonstrated an IRR (of 78.5-dB) quite higher than other implementation results found in literature (around 45-dB at the same IF [36]) in similar CMOS process, 0.35- μ m.

The increase in the power consumption is the most critical issue that appears from the use of the amplifier required in the g_m -C cell to keep the OTA output loaded with a constant voltage, i.e. the same voltage as in the capacitor. Nonetheless, in terms of area, the capacitor sizes are significantly reduced as mentioned.

Table 5.2 presents the results of the PPF implementations in contrast with version 3.0 Bluetooth specifications [76]. It can be seen that all the architectures tested to implement the PPF comply with the Bluetooth requirements.

	Bluetooth requirement	G_m -C PPF	Active RC PPF	MOSFET-C PPF
Adjacent (1 MHz) Interference (dB)	0	-14.9	-40.6	-28
Adjacent (2 MHz) Interference (dB)	-30	-44.87	-80	-64.8
Adjacent (≥ 3 MHz) Interference (dB)	-40	≥ -64.79	≥ -89.5	≥ -60
Image frequency Interference (dB)	-9	-78.5	-41.5	-37

Table 5.2: Comparison with the Bluetooth specifications.

To compare our PPF implementation with real results from a published work for Bluetooth, the PPF results presented in [36] are plotted in figure 5.1. Actually, there are few works in literature that can be used for comparison within the same target specifications.

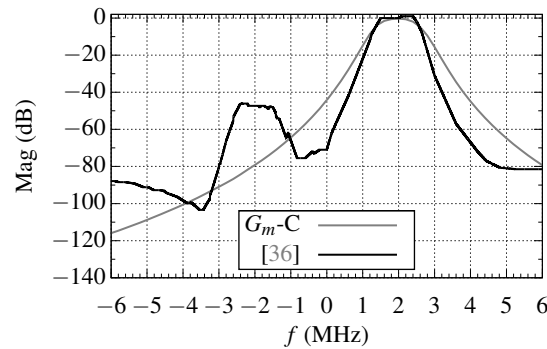


Figure 5.1: Comparison between g_m -C PPF implementation and the one from [36].

The filter from [36] presents a gain of 15-dB in the passband. Here we have normalized it to provide a better comparison. Needless to say that in the solution proposed in this thesis, the gain is given solely by the size of the first transconductor in the biquad, so the required 15-dB gain can be easily achieved.

As seen in figure, both filters behave similarly in the passband. Following the cut-off frequency, our solution starts to deviate from the frequency response seen in [36]. In fact, this behavior has already been demonstrated when comparing a continuous-time solution with our proposed F&H scheme – see figure 4.28a. Nonetheless, although the attenuation is somehow lower in our implementation, it should be noted that our proposed solution presents better performance nearby the image frequency, thus better IRR is achieved. Obviously, in terms of actual implementation this still needs to be validated through real IC measurements. In such case, cross-coupling between

channels, path mismatches, and other effects can lead to similar behaviors around the image frequency as observed in [36].

A comparison between the IRR can also be made with the PPF presented in [68], which is about 40-dB. This filter is also centered at 2-MHz but with a passband bandwidth of 1.1-MHz. The passband is about 40-kHz higher than the filter developed in this work but this difference is very small and the comparison can still be acceptable.

Following, some interesting results for the PPF implementation are illustrated. These results show the resulting magnitude response due to changes in some of the parameters of the PPF. Figure 5.2 shows the Bode magnitude plots for a sampling frequency of 25- and 100-MHz.

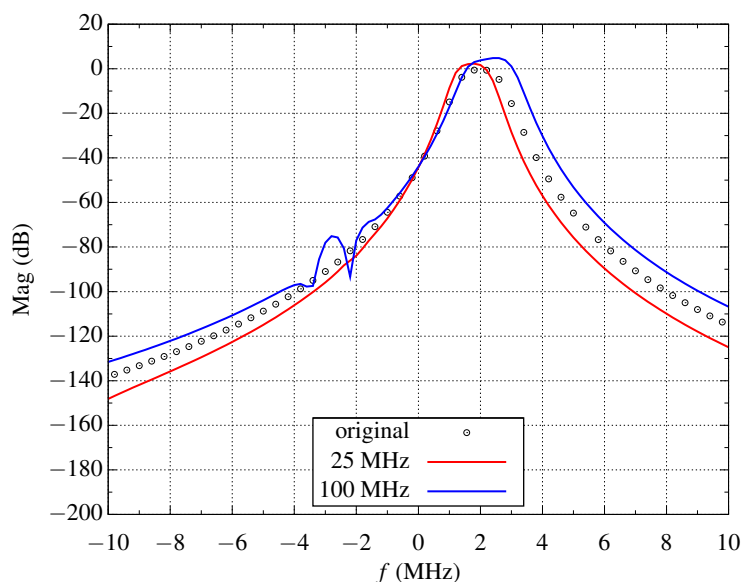


Figure 5.2: Changing the sampling frequency.

It can be seen that changing the sampling frequency slightly changes the center frequency of the filter. Also, the increase of the sampling frequency degraded the response in the passband but still maintaining the desired bandwidth. The simulations on the ideal PPF showed that at least a sampling frequency of 50-MHz was needed for the PPF with F&H to work correctly. Actually, as seen, in the schematic implementation the sampling frequency can be lower than this value.

Next, in figures 5.3 and 5.4 the Bode magnitude plots are shown for changes in the size of the first and second transconductors belonging to the frequency translation stages. It can be seen that increasing the size in one of the transconductors has the same effect of decreasing the size in the other transconductor. This is because at the input of the first transconductor there is a first-order BPF and a second-order LPF at the second transconductor [66]. This means that both transconductors need to translate the respective transfer function to the same center frequency.

Otherwise, different frequency shifts lead to a degraded magnitude response like the ones seen in figures 5.3 and 5.4.

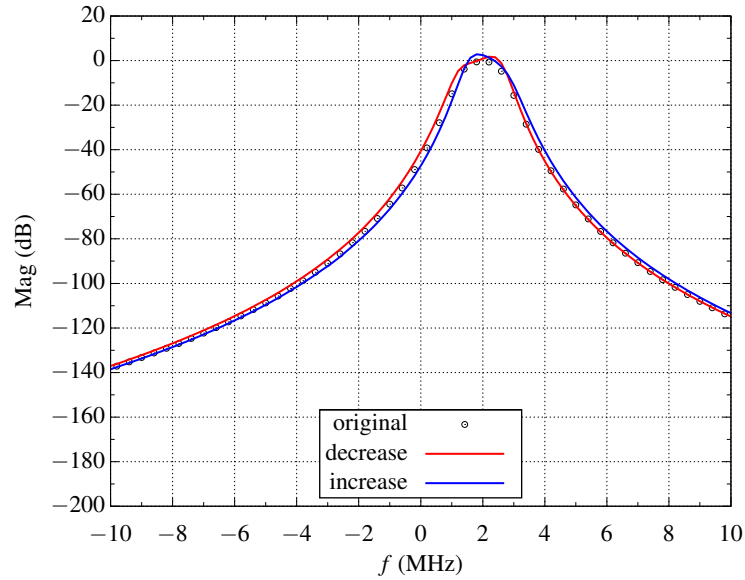


Figure 5.3: Changing the size of the first transconductor for the frequency translation.

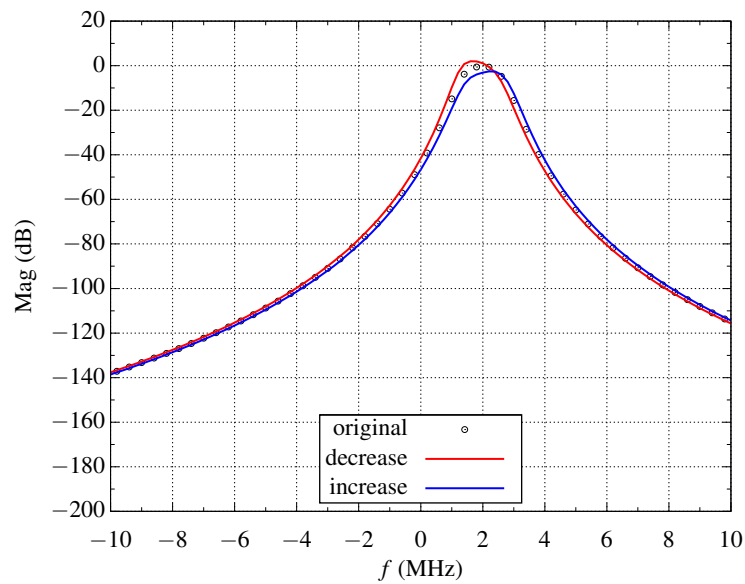


Figure 5.4: Changing the size of the second transconductor for the frequency translation.

Another interesting result comes with changing the sizes of the switches as seen in figure 5.5. From the results, we can notice that using small switches reduces drastically the magnitude response. However, increasing them, increases the passband gain but not significantly. Also, simulations showed that increasing the size of the switches too much limited the desired functionality provided by changing the duty-cycle. This influence is due to the series resistance of the switches.

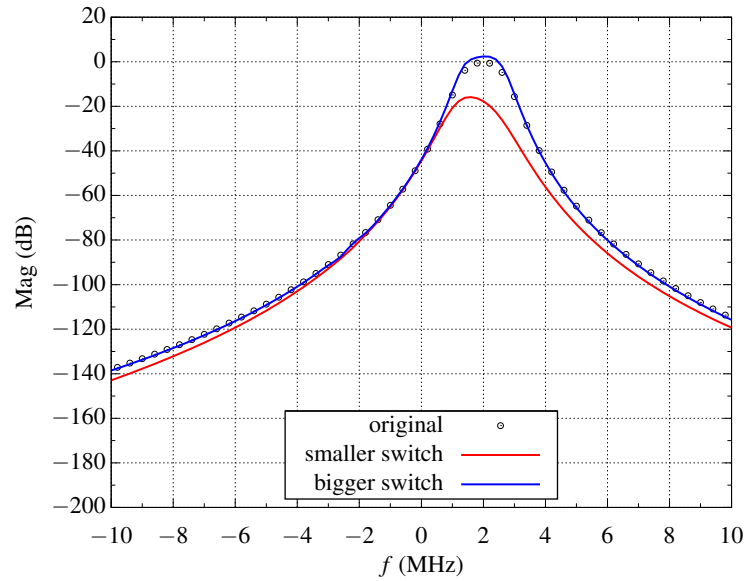


Figure 5.5: Changing the size of the switches.

The final result displayed in figure 5.6 exhibits the changes in magnitude due to changing the size of the amplifier used as load. Analyzing the figure we can see that the amplifier is the key component that is responsible for the biggest differences in the frequency response. Increasing its size would provide for a better response of the filter but would have a higher power consumption as drawback, while reducing would have the opposite result.

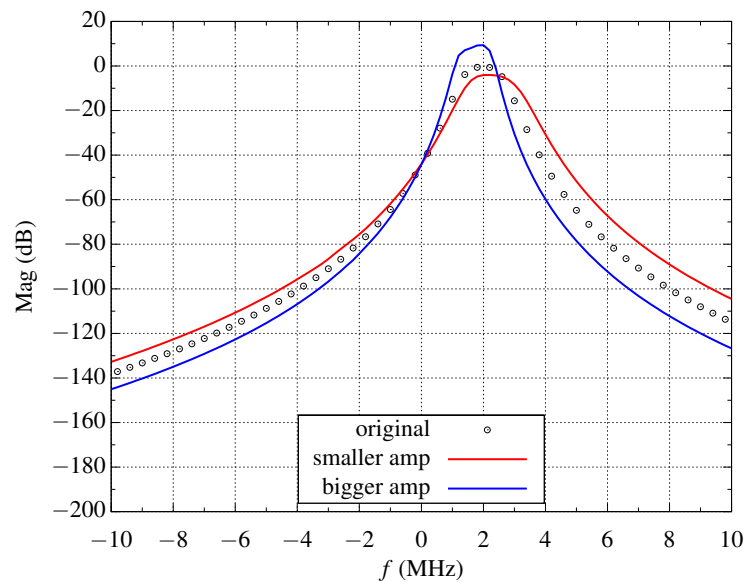


Figure 5.6: Changing the size of amplifier used as load.

5.2 Layout

After the study of the several possible architectures to implement the PPF with the F&H technique, the layout of a PPF for a low-IF Bluetooth was performed. The value chosen for the IF was 2-MHz. The chosen architecture was the g_m -C due to its superior overall performance. The layout of the second-order PPF can be seen in figure 5.7. The filter was implemented as a sixth-order Butterworth PPF in order to comply with the Bluetooth requirements.

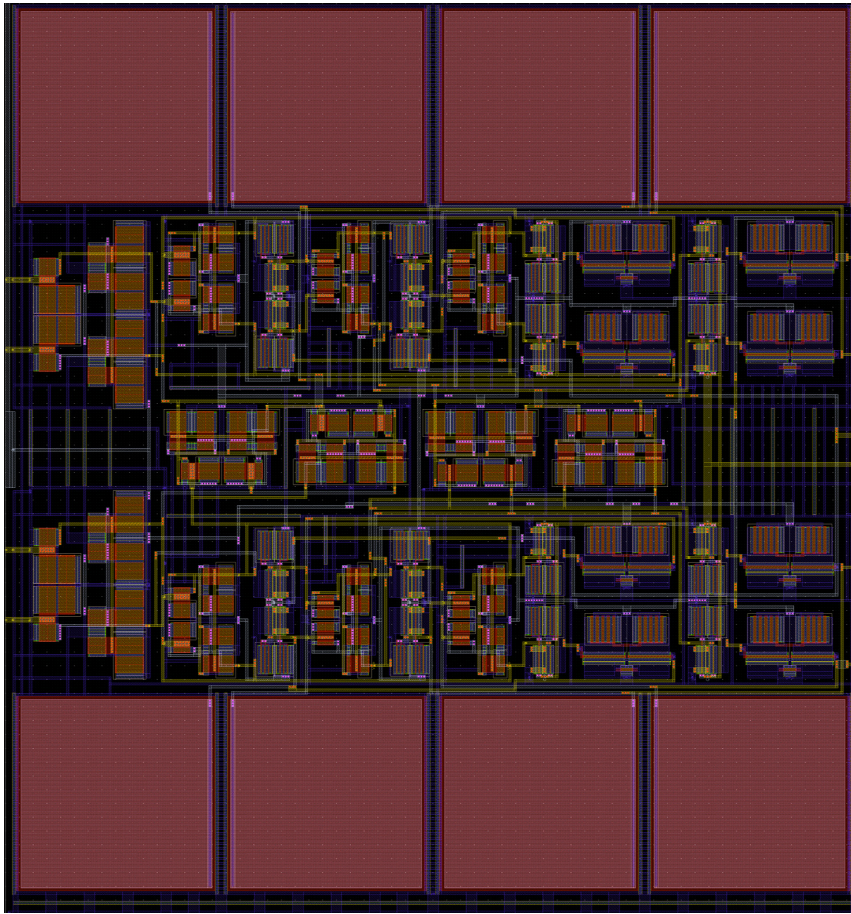


Figure 5.7: Second-order PPF layout

The post-layout simulations showed a frequency response of the filter centered at 1.9-MHz. To center the frequency response at IF, the duty-cycle of the filter was changed from 0.5 to 0.55. The post-layout and the central-frequency tuned frequency response of the filter can be seen in figure 5.8.

The main results for the layout circuit can be seen in table 5.3. A comparison with another PPF found in the literature is also present.

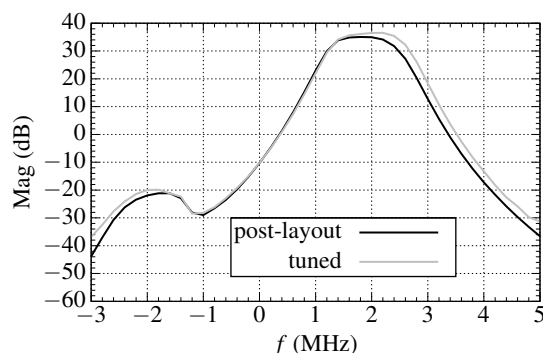


Figure 5.8: Post-layout and center-frequency tuned Bode magnitude responses of the filter.

	This work	[36]
Passband gain	36.5 dB	15 dB
Center frequency	2-MHz	2-MHz
IRR	56.5 dB	45 dB
Adjacent 1-MHz interference	14.5 dB	29 dB
Adjacent 2-MHz interference	46.5 dB	58 dB
Adjacent ≥ 3 -MHz interference	≥ 56.5 dB	-
Power consumption	19.67 mW	12.69 mW
Area	0.31mm^2	1.28mm^2

Table 5.3: Layout results.

Notice that the comparison of the results, resulting from this project, with the literature is not fair, we still need to have the actual testing results from a real chip. Nevertheless, it indicates that the overall performance should be reasonably good. Despite this fact, the area is actually reduced (by $\frac{1}{4}$), which shows the effectiveness of the F&H technique in the present design.

5.3 Conclusion

A new polyphase filter implementation with parametric tuning has been proposed in this thesis. First, studies were carried out to choose the low-IF as the most suitable receiver architecture for the present PPF implementation, regarding its main advantages in terms of circuit integration and image rejection. The specifications of a Bluetooth receiver were adopted for a target application.

The fundamental concepts related to the PPF have been presented. The required area and the need to have a tuning circuit were identified as the main problems to be solved. With that in mind, the F&H technique has been proposed to be included within the PPF circuit. This technique allowed reduced size of the capacitors in the PPF, while providing simple digital tuning. The theory supporting this technique applied to the PPF has also been presented. Several architectures on how to perform the PPF were presented, namely the g_m -C, active RC, and MOSFET-C. Simulations shown that the g_m -C approach is the most indicated due to superior performance, in terms of IRR, capacitance reduction and power consumption.

A PPF schematic based on g_m -C amplifiers has been designed in Austria-microsystems CMOS 0.35- μm and simulated using Cadence SPECTRE/SPECTRE-RF simulators. The PPF is a sixth-order Butterworth filter with center frequency at 2-MHz, and 3-dB bandwidth of 1.06-MHz. The proposed PPF can be digitally tuned by employing different duty-cycles to the switches operating at 50-MHz or less. Results shown an IRR of 78.5-dB and ACS levels better than 14-dB compared to the Bluetooth minimum requirements. These results are in compliance with the Bluetooth specification standard with great safety margin. The circuit was designed for optimum duty-cycle control of 50 percent, has 15.55-mW of power consumption and provides a size reduction of about 1.95 when compared to the PPF version without implementation of the F&H.

The layout of a PPF based on the g_m -C architecture was completed. The post-layout simulation has shown a deviation from the center frequency, which was easily tuned back to 2-MHz with the duty-cycle. This shows the tuning capabilities of the F&H technique. The final simulation results of the PPF present a passband gain of 36.5-dB, an IRR of 56.5-dB, compliance with the Bluetooth minimum requirements, and a power consumption of 19.67-mW. In terms of area, it occupies 0.31- mm^2 , which is about $\frac{1}{4}$ smaller when compared to an actual implementation found in the literature (with the same goals).

5.4 Future work

Due to PVT variations, the tuning circuit is a necessity in a PPF. The proposed PPF can be tuned in two ways: through the supply voltage of the g_m cells or by changing the duty-cycle. Changing the supply voltage provides a small tuning range. Changing the duty-cycle can provide for a large tuning range but changes both the center frequency and the passband bandwidth.

Therefore, these two methods can be used in a combined way to provide an accurate tuning procedure. Simple algorithms can then be applied to ensure an optimum value for the IRR. Also, due to the flexible calibration introduced, it should be possible to have online and offline calibration procedures.

References

- [1] V. G. Tavares, J. C. Príncipe, and J. G. Harris, “F&H filter: a novel ultra-low power discrete time filter,” *Electronics Letters*, vol. 35, no. 15, pp. 1226–1227, Jul 1999.
- [2] V. G. Tavares, J. C. Príncipe, J. G. Harris, and P. G. Oliveira, “Filter and hold circuit utilizing a charge/discharge current,” Patent US 6,420,927, July 16, 2002.
- [3] S. Haykin, *Communication Systems*, 4th ed. Wiley, May 2000.
- [4] T. K. Sarkar, R. Mailloux, A. A. Oliner, M. Salazar-Palma, and D. L. Sengupta, *History of Wireless*. Wiley-IEEE Press, 2006.
- [5] C. Buff, “Radio receivers-past and present,” *Proceedings of the IRE*, vol. 50, no. 5, pp. 884–891, May 1962.
- [6] J. Conti, “The 10 greatest communications inventions,” *Communications Engineer*, vol. 5, no. 1, pp. 14–21, Feb-Mar 2007.
- [7] G. Marconi, “Wireless signaling,” Patent US 763,772, June 28, 1904.
- [8] R. A. Fessenden, “Wireless signaling,” Patent US 706,740, August 12, 1902.
- [9] E. Armstrong, “Operating features of the audion,” *Electrical World* 64, pp. 1149–1151, 1914.
- [10] —, “Some recent developments in the audion receiver,” *Proceedings of the IEEE*, vol. 51, no. 8, pp. 1083–1097, Aug. 1963.
- [11] J. Smith, *Modern Communication Circuits*. New York, NY, USA: McGraw-Hill, Inc., 1988.
- [12] E. Armstrong, “A new system of short wave amplification,” *Proceedings of the IRE*, vol. 9, no. 1, pp. 3–11, Feb. 1921.
- [13] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ, USA: Prentice-Hall, Inc., 1998.
- [14] S. Galal, M. Tawfik, and H. Ragaie, “On the design and sensitivity of RC sequence asymmetric polyphase networks in RF integrated transceivers,” in *IEEE International Symposium on Circuits and Systems*, vol. 2, Jul 1999, pp. 593–597.
- [15] Q. Gu, *RF System Design of Transceivers for Wireless Communications*. Secaucus, NJ, USA: Springer-Verlag New York, Inc., 2006.
- [16] R. V. L. Hartley, “Modulation system,” Patent US 1,666,206, Apr 17, 1928.
- [17] D. Weaver, “A third method of generation and detection of single-sideband signals,” *Proceedings of the IRE*, vol. 44, no. 12, pp. 1703–1705, Dec. 1956.

- [18] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 873–887, Jun 2001.
- [19] A. Parssinen, *Direct Conversion Receivers in Wide-Band Systems*. Hingham, MA, USA: Kluwer Academic Publishers, 2001.
- [20] S. Mirabbasi and K. Martin, "Classical and modern receiver architectures," *IEEE Communications Magazine*, vol. 38, no. 11, pp. 132–139, Nov 2000.
- [21] J. Rudell, J.-J. Ou, T. Cho, G. Chien, F. Brianti, J. Weldon, and P. Gray, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 2071–2088, Dec 1997.
- [22] D. G. Tucker, "The history of the homodyne and synchrodyne," vol. 14, pp. 143–154, April 1954.
- [23] A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 12, pp. 1399–1410, Dec 1995.
- [24] R. Harjani, *Design of High-Speed Communication Circuits*. River Edge, NJ, USA: World Scientific Publishing Co., Inc., 2006.
- [25] B. Yang and N. R. Sollenberger, "DC offset correction for very low intermediate frequency receiver," Patent US 7,277,688, January 13, 2005.
- [26] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 6, pp. 428–435, Jun 1997.
- [27] P. Gray and R. Meyer, "Future directions in silicon ICs for RF personal communications," in *Proceedings of the IEEE Custom Integrated Circuits Conference.*, May 1995, pp. 83–90.
- [28] J. Crols and M. Steyaert, "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 12, pp. 1483–1492, Dec 1995.
- [29] J. Rudell, J.-J. Ou, R. Narayanaswami, G. Chien, J. Weldon, L. Lin, K.-C. Tsai, L. Tee, K. Khoo, D. Au, T. Robinson, D. Gerna, M. Otsuka, and P. Gray, "Recent developments in high integration multi-standard CMOS transceivers for personal communication systems," in *Proceedings of the International Symposium on Low Power Electronics and Design*, Aug 1998, pp. 149–154.
- [30] J. Crols and M. Steyaert, "Low-IF topologies for high-performance analog front ends of fully integrated receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 3, pp. 269–282, Mar 1998.
- [31] M. J. Gingell, "Single sideband modulation using sequence asymmetric polyphase networks," *Electrical Communication*, vol. 48, pp. 21–25, 1973.
- [32] L. Yu and W. Snelgrove, "A novel adaptive mismatch cancellation system for quadrature IF radio receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 6, pp. 789–801, Jun 1999.

- [33] M. J. Gingell, "Polyphase symmetrical network," Patent US 3,559,042, Jan 26, 1971.
- [34] J. Crols and M. Steyaert, "An analog integrated polyphase filter for a high performance low-IF receiver," in *Digest of Technical Papers of the Symposium on VLSI Circuits*, Jun 1995, pp. 87–88.
- [35] Z. Zhang, "Analysis, design, and optimization of RF CMOS polyphase filters," Ph.D. dissertation, Universität Duisburg-Essen, Sep 2005.
- [36] A. Emira and E. Sanchez-Sinencio, "A pseudo differential complex filter for Bluetooth with frequency tuning," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 50, no. 10, pp. 742–754, Oct. 2003.
- [37] K.-P. Pun, J. Franca, and C. Azeredo-Leme, "A switched-capacitor image rejection filter, for complex IF receivers," in *IEEE Asia-Pacific Conference on Circuits and Systems*, Tianjin, China, 2000, pp. 140–143.
- [38] J. you Song, X. ye Liu, and Z.-G. Wang, "Design of an active polyphase filter in GSM receiver with low-IF topologies," in *9th International Conference on Solid-State and Integrated-Circuit Technology*, Oct. 2008, pp. 1673–1676.
- [39] C.-Y. Chou and C.-Y. Wu, "The design of wideband and low-power CMOS active polyphase filter and its application in RF double-quadrature receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 5, pp. 825–833, May 2005.
- [40] ———, "The design of a new wideband and low-power CMOS active polyphase filter for low-IF receiver applications," in *Asia-Pacific Conference on Circuits and Systems*, vol. 1, 2002, pp. 241–244.
- [41] M. Notten, H. Brekelmans, and V. Rambeau, "A 5th order 14 mWatt active polyphase filter for analog and digital TV on mobile applications," in *Proceedings of the 32nd European Solid-State Circuits Conference*, Sept. 2006, pp. 211–214.
- [42] A. Tajalli and S. Atarodi, "A compact biquadratic gm-C filter structure for low-voltage and high frequency applications," in *Proceedings of the International Symposium on Circuits and Systems*, vol. 1, May 2003, pp. 501–504.
- [43] T. Teo, E.-S. Khoo, D. Uday, and C.-B. Tear, "Design, analysis, and implementation of analog complex filter for low-IF wireless LAN application," in *Proceedings of the 17th International Conference on VLSI Design*, 2004, pp. 416–421.
- [44] T. Teo, E.-S. Khoo, and D. Uday, "Gm-C complex transitional filter for low-IF wireless LAN application," in *Proceedings of the 15th International Conference on Microelectronics*, Dec. 2003, pp. 110–113.
- [45] A. Abrishamifar, R. Zanbaghi, S. Mehrmanesh, and G. Lahiji, "A low-power complex active-RC filter for low-IF receivers using a new class-AB operational amplifier," in *International Symposium on Integrated Circuits*, Sept. 2007, pp. 309–312.
- [46] D. Du, Y. Li, Z. Wang, and S. Tan, "An active-RC complex filter with mixed signal tuning system for low-IF receiver," in *IEEE Asia Pacific Conference on Circuits and Systems*, Dec. 2006, pp. 1031–1034.

- [47] Y. Jiao, Z. Huang, and L. Li, "CMOS analog polyphase filters for use in Bluetooth systems," in *9th International Conference on Solid-State and Integrated-Circuit Technology*, Oct. 2008, pp. 1677–1680.
- [48] P. Andreani, S. Mattisson, and B. Essink, "A CMOS gm-C polyphase filter with high image band rejection," in *Proceedings of the 26th European Solid-State Circuits Conference*, Sept. 2000, pp. 272–275.
- [49] F. Chen, H. Ma, B. Chen, Y. Shi, M. Lin, and H. Jia, "A complex BPF with on chip auto-tuning architecture for wireless receivers," in *11th IEEE Singapore International Conference on Communication Systems*, Nov. 2008, pp. 1451–1455.
- [50] K. Linggajaya, D. M. Anh, M. J. Guo, and Y. K. Seng, "A new active polyphase filter for wideband image reject downconverter," in *Proceedings of the IEEE International Conference on Semiconductor Electronics*, Dec. 2002, pp. 213–217.
- [51] R. Zanbaghi, M. Atarodi, and A. Tajalli, "An ultra low power Gm-C complex filter for low-IF wireless PAN applications," in *IEEE Region 10 Conference*, Nov. 2006, pp. 1–4.
- [52] A. Mohieldin, E. Sanchez-Sinencio, and J. Silva-Martinez, "A fully balanced pseudo-differential OTA with common-mode feedforward and inherent common-mode feedback detector," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 4, pp. 663 – 668, Apr 2003.
- [53] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp. 142 –153, Feb 1992.
- [54] P. Andreani and S. Mattisson, "On the use of Nauta's transconductor in low-frequency CMOS gm-C bandpass filters," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 2, pp. 114 –124, Feb 2002.
- [55] M. Chen, J. Silva-Martinez, S. Rokhsaz, and M. Robinson, "A $2-V_{pp}$ 80-200-MHz fourth-order continuous-time linear phase filter with automatic frequency tuning," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1745 – 1749, Oct. 2003.
- [56] J. De Lima and C. Dualibe, "A linearly tunable low-voltage CMOS transconductor with improved common-mode stability and its application to gm-C filters," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 7, pp. 649 –660, Jul 2001.
- [57] Y. Tsvividis, "Continuous-time filters in telecommunications chips," *IEEE Communications Magazine*, vol. 39, no. 4, pp. 132 –137, Apr 2001.
- [58] H. Alzaher and N. Tasadduq, "A CMOS low power current-mode polyphase filter," in *Proceedings of the 14th ACM/IEEE international symposium on Low power electronics and design*. New York, NY, USA: ACM, 2009, pp. 75–80.
- [59] T. Georgantas, Y. Papananos, and Y. Tsvividis, "A comparative study of five integrator structures for monolithic continuous-time filters: a tutorial," in *IEEE International Symposium on Circuits and Systems*, vol. 2, 3-6 1993, pp. 1259 –1262.
- [60] K. Moulding, J. Quartly, P. Rankin, R. Thompson, and G. Wilson, "Gyrator video filter IC with automatic tuning," *IEEE Journal of Solid-State Circuits*, vol. 15, no. 6, pp. 963 – 968, Dec 1980.

- [61] Y. Tsvividis, "Integrated continuous-time filter design - an overview," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 3, pp. 166–176, Mar 1994.
- [62] Y. Tsvividis, M. Banu, and J. Khoury, "Continuous-time MOSFET-C filters in VLSI," *IEEE Journal of Solid-State Circuits*, vol. 21, no. 1, pp. 15–30, Feb 1986.
- [63] M. Banu and Y. Tsvividis, "Detailed analysis of nonidealities in MOS fully integrated active RC filters based on balanced networks," *IEE Proceedings on Electronic Circuits and Systems*, vol. 131, no. 5, pp. 190–196, Oct 1984.
- [64] R. Mancini, *Op Amps for everyone*. Texas Instruments, Aug 2002.
- [65] A. Carusone and D. Johns, "Analogue adaptive filters: past and present," *IEE Proceedings on Circuits, Devices and Systems*, vol. 147, no. 1, pp. 82–90, Feb 2000.
- [66] P. Crombez, J. Craninckx, and M. Steyaert, "A linearity and power efficient design strategy for architecture optimization of g_m -C biquadratic filters," in *Ph.D. Research in Microelectronics and Electronics Conference*, 2-5 2007, pp. 229–232.
- [67] A. S. Sedra and K. C. Smith, *Microelectronic Circuits 5th Edition*. New York, NY, USA: Oxford University Press, Inc., 2004.
- [68] S.-B. Hyun, G.-Y. Tak, S.-H. Kim, B.-J. Kim, J. Ko, and S.-S. Park, "A dual-mode 2.4-GHz CMOS transceiver for high-rate Bluetooth systems," in *ETRI journal*, vol. 26, 2004.
- [69] F. Bahmani and E. Sanchez-Sinencio, "A highly linear pseudo-differential transconductance [CMOS OTA]," in *Proceeding of the 30th European Solid-State Circuits Conference*, 21-23 2004, pp. 111–114.
- [70] B. Nauta and E. Seevinck, "Linear CMOS transconductance element for VHF filters," *Electronics Letters*, vol. 25, no. 7, pp. 448–450, 30 1989.
- [71] P. Crombez, J. Craninckx, and M. Steyaert, "A 100kHz - 20MHz reconfigurable nauta g_m -C biquad low-pass filter in 0.13 μm CMOS," in *IEEE Asian Solid-State Circuits Conference*, 12-14 2007, pp. 444–447.
- [72] J. Tow, "A step-by-step active-filter design," *IEEE Spectrum*, vol. 6, no. 12, pp. 64–68, Dec. 1969.
- [73] (Last accessed on June 27, 2010) Op_wb. [Online]. Available: asic.austriamicrosystems.com/databooks/c35_a/op_wb_c35_rev.pdf
- [74] S.-B. Kim, "A contribution to continuous-time quadrature bandpass sigma-delta modulators for low-IF receivers," Ph.D. dissertation, Rheinisch-Westfälischen Technischen Hochschule Aachen, 2009.
- [75] G. C. Ahn, "Design techniques for low-voltage and low-power analog-to-digital converters," Ph.D. dissertation, Oregon State University, 2005.
- [76] (April 2009, Last accessed in June 19, 2010) Bluetooth Specification Version 3.0 + HS. [Online]. Available: http://www.bluetooth.com/Specification%20Documents/Core_V30__HS.zip