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CMOS-RF Power Amplifier for Wireless Communications

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Abstract

The present work addresses the study and implementation of a radio-frequency (RF) power amplifier (PA). Several classes of amplification are analyzed, from both the linear and the non-linear classes of amplification. From the non-linear class amplifiers, the current-mode class-D (CMCD) amplifier was chosen, because it is a zero-voltage-switching (ZVS) amplifier but with a lower peak drain voltage than other ZVS amplifiers, like the class-E amplifier. Since CMOS devices have a low breakdown voltage, having a lower peak drain voltage is an important feature. The ZVS characteristic enables the CMCD to work at higher frequencies ideally without energy losses at each RF cycle, in opposition to its dual counterpart, the voltage-mode class-D (VMCD).

Following the basic operation of the CMCD amplifier, a non-linear analysis is made starting with the impact of the load network quality factor, Q_L , on the amplifier performance. The second part of the non-linear analysis comprises a study to understand the impact of the inductor unloaded quality factor, along with Q_L , on the PA efficiency. It is concluded that lowering Q_L by increasing the RLC network inductor size, and decreasing the filter capacitance by the same factor, greatly improves the PA overall performance.

A vast set of simulations is presented in this work. First the low Q_L approach that improves the PA performance is corroborated, achieving nearly 76% of drain efficiency with 16-dBm of output power. A small comparative study between a 90-nm and a 350-nm CMOS technology is also performed, showing that the selected 90-nm technology is better suited to implement the CMCD PA. The NMOS-RF I - V characteristic curves of both technologies are also shown in order to discuss the breakdown voltage of the transistors.

The CMCD cascode topology is presented as a solution to increase the output power, sacrificing only a small percentage of the drain efficiency. Since with the cascode architecture there are two transistors at each branch, it is possible to raise the supply voltage to higher values than with the basic topology.

A layout with the selected 90-nm CMOS technology, of the current-mode class-D PA cascode topology is presented. A group of post-layout simulations is performed with *Assura* and *Calibre* parasitic extractions, which leads to the need of a post-layout RLC filter re-tuning. After a correction in the RLC filter capacitance value, new *Assura* and *Calibre* parasitic extractions are performed producing good results. A 64.06% drain efficiency with *Assura* extraction and 62.81% with *Calibre* are achieved against the 66.18% drain efficiency of the ideal case. The output power is approximately 21-dBm with both parasitic extractions and in the ideal case.

Resumo

O presente trabalho tem como objectivo o estudo e implementação de um amplificador de potência (PA) para rádio-frequência (RF). Várias classes de amplificadores são analisadas e destas, o amplificador de funcionamento classe-D em modo corrente (CMCD) é o seleccionado para implementação. Devido ao amplificador CMCD possuir a característica *zero-voltage-switching* (ZVS) e de ter uma tensão de pico no dreno dos transístores menor que o amplificador classe-E, também ele um amplificador ZVS, fazem dele a melhor opção para um estudo aprofundado e implementação. O facto de não existirem implementações desta classe em CMOS, reportadas até à data também teve influência na decisão.

Após o estudo do funcionamento básico do amplificador classe-D em modo corrente, é efectuada uma análise ao impacto do factor de qualidade da rede de carga, Q_L , no desempenho do PA. A segunda parte desta análise não linear do comportamento do CMCD, é feita tendo em conta o impacto do factor de qualidade da bobine da rede RLC juntamente com Q_L . Daqui pode-se concluir que baixar o Q_L , aumentando o valor da bobine e diminuindo o valor do condensador de carga pelo mesmo factor, traduz-se num aumento de desempenho por parte do amplificador.

Um vasto conjunto de simulações é apresentado neste trabalho. Nestas simulações o método de baixar o factor de qualidade da rede de carga é comprovado com recurso a uma tecnologia CMOS de 90-nm, obtendo-se aproximadamente 76% de eficiência de dreno com 16-dBm de potência de saída. Um estudo comparativo entre a tecnologia CMOS de 90-nm e outra de 350-nm é efectuado, onde se demonstra que a tecnologia de 90-nm é mais adequada à implementação do amplificador de potência. As curvas características I - V dos transístores de rádio-frequência NMOS, de ambas as tecnologias, são apresentadas para definir as tensões de quebra dos transístores.

A topologia cascode do amplificador classe-D em modo corrente é apresentada como solução para aumentar a potência de saída do amplificador, sacrificando apenas uma pequena percentagem da eficiência de dreno. Este aumento de potência de saída do amplificador é possível pois, com a topologia cascode temos dois transístores em cada ramo, o que nos permite aumentar a tensão de alimentação do circuito.

Um *layout* do amplificador de potência CMCD desenhado na tecnologia CMOS 90-nm é apresentado. Foi necessário efectuar uma re-sintonização do filtro RLC após terem sido efectuadas simulações *post-layout* e os resultados não serem os esperados. Após a correcção na capacidade do filtro RLC, novas extracções parasitas do layout são efectuadas com as ferramentas *Assura* e *Calibre* produzindo bons resultados. Eficiências de dreno de 64.06% com o *Assura* e 62.18% com o *Calibre* foram atingidas contra os 66.18% do caso ideal. A potência de saída atingida é aproximadamente 21-dBm nas extracções parasitas e no caso ideal.

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At last, I would like to show my gratitude to all my other friends that make part of my life and always bring me something positive into it. I hope I also bring something positive into your life.

Daniel José Azevedo Oliveira

“An expert is a man who has made all the mistakes which can be made in a very narrow field.”

Niels Bohr

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Abbreviations and Symbols

List of abbreviations

ACP	Adjacent Channel Leakage Power
BFC	Big Fat Capacitor
CMCD	Current-Mode Class-D
CMOS	Complementary Metal-Oxide Semiconductor
DPSK	Differential Phase-Shift Keying
DQPSK	Differential Quadrature Phase-Shift Keying
DRC	Design Rule Check
FOM	Figure Of Merit
GFSK	Gaussian Frequency-Shift Keying
HS	High Speed
IC	Integrated Circuit
ISM	Industrial, Scientific and Medical
LVS	Layout Versus Schematic
MMSIM	Multi-Mode Simulation
PA	Power Amplifier
PAE	Power Added Efficiency
RF	Radio-Frequency
RFC	Radio-Frequency Choke
SMPA	Switch-Mode Power Amplifier
VMCD	Voltage-Mode Class-D
ZCS	Zero-Current-Switching
ZVS	Zero-Voltage-Switching

List of symbols

η_D	Drain efficiency
f_c	Central frequency
Q_L	Loaded quality factor
Q_u	Unloaded quality factor
ω	Angular frequency
ω_c	Central angular frequency
r_{on}	Transistor on-resistance
V_{break}	Transistors breakdown voltage

Chapter 1

Introduction

Power amplifiers (PA) account for a good part of the power consumption in an RF transceiver. The need for higher efficiencies is putting pressure on the research for new PA architectures, and consequently from it new problems are deriving. Concurrently, low-cost and high integration capabilities are also important factors when considering the hardware support to build the transceiver. These are factors that match with CMOS technologies, and this is one of the reasons for the amount of new work being reported on CMOS transceivers, and also on PA design. However, thin gate transistors operate at very low power voltages, putting a limit on power transmission, especially with the most efficient PAs such as class E. The main goal of this project is to study a class-D based power amplifier (PA) not yet reported in CMOS technology. This is a non-linear amplifier similar to class E¹, but with the benefit of theoretically more output power capability.

In this chapter a brief introduction to several classes of amplifiers is described, as well as a short survey on the selected communication standard. A state of the art showing published works with results achieved by several classes of amplifiers working on 2.45GHz is then presented. Some implementations of current-mode class-D (CMCD) power amplifiers are also discussed.

1.1 Motivation

Communication is essential to society as we know it, thus any evolution that leads to improvement in this field is always important. The continuous growth of interests in mobile communications creates new problems in the integrated circuit (IC) design field, namely in CMOS implementations because of the typical high-frequencies involved in these systems. Power amplifiers are the main block of any wireless transmitter. However, low efficiency can be a strong detriment to its application, because the battery life-time of portable devices gets compromised by power needs. Besides the high-efficiency concern, mobile communication systems also demand for cheap and reliable technologies.

¹In the sense that is also a zero-voltage-switching power amplifier.

The need for higher efficiencies in power amplifiers leads to the research of new classes that are not usually associated with radio-frequency (RF) and CMOS implementations. One example are the class-D architectures, which are normally related with audio applications. Although in theory, class-D power amplifiers can achieve 100% efficiency like other non-linear PAs, RF applications are nearly inexistent. This lack of RF applications using this class of amplifiers is the basis of the present study, which will use the class-D architecture as a starting point for a CMOS IC implementation.

As referred ahead, class-D amplifiers are in fact unsuitable for high-frequency applications, mainly due to the intrinsic parasitic capacitance of the transistors. To overcome this problem a class-D⁻¹ PA can be used, owing to its zero-voltage-switching (ZVS) property. Although class-E amplifiers can also overcome the parasitic capacitance problem, the CMCD power amplifier is a good solution because in theory generates lower peak voltages, being more suitable for the low breakdown voltage of CMOS devices. This dual version of the voltage-mode class-D (VMCD) amplifier with a lower drain peak voltage, still manages to get a theoretical efficiency as good as class-E architectures.

1.2 Bluetooth features

In order to choose a communication standard for this project, it is necessary to select one that has proper technical requirements attainable by the proposed amplifier. The main aspects to look into are the output power and the operation frequency of the PA. After the analysis of some mobile communications standards, *Bluetooth* was chosen because it is a low power system. Table 1.1 shows the different levels required in the *Bluetooth* standard [1–3]. It is generally used for short-distance wireless communication between several devices, up to 100 meters distance.

Table 1.1: *Bluetooth* power classes.

Class	Power (dBm)	Power (mW)	Distance (m)
1	20	100	100
2	4	2.5	10
3	0	1	1

The *Bluetooth* operation frequency was also a favorable factor taken into consideration for our targeted technology. Operates in the industrial, scientific and medical (ISM) 2.4-GHz frequency band. This is important since it is not possible to integrate on-chip inductors and still get good results in sub-GHz CMOS implementations [4]. As referred ahead, an on-chip inductor has great impact on the overall performance of the amplifier. This make inductors critical components for PA design.

Bluetooth technology operates in the frequency range of 2400-2483.5-MHz. It is made up of 79 channels², each with a 1-MHz of bandwidth. The first 2-MHz and the last 3.5-MHz are guard bands. This is to comply with out-of-band regulations in each country [3].

²The 79 channels of the *Bluetooth* standard are numbered from 0 to 78.

An important measure in this standard is the adjacent channel leakage power (ACP). The leakage power interferes with adjacent channels, and a high-leakage value can ruin the system transmission capability. The transmitted power is measured in a 100-KHz bandwidth, at maximum power. Table 1.2 shows the ACP requirements for the *Bluetooth* standard [5].

Table 1.2: *Bluetooth* ACP requisites.

Frequency offset	Transmitted power
± 500	-20dBc
2MHz	-20dBm
≥ 3 MHz	-40dBm

The ACP test is performed in the middle channel and 3-MHz inside the upper and lower guard band limits, *i. e.* in the 3rd, 39th and 75th channels. If the ACP measurement is performed in the 3rd channel the -20-dBm condition (table 1.2) must be checked for channels 1 and 5, and the -40-dBm condition (table 1.2) must be checked for the remaining channels [6].

Since its creation, *Bluetooth* technology has evolved and it is now on version 3.0+HS. Throughout this evolution, *Bluetooth* has improved its modulation scheme and the recent versions make use of non-constant envelope signals. Therefore, linear power amplification is now required, whose efficiency is usually low. There are alternative solutions which uses non-linear amplifiers, such as class-D, with non-constant envelope signals [7]. However, this is not the objective of the present study. We will be using the constant envelope modulation scheme employed in the first versions of *Bluetooth* that is still compatible with the newer versions.

In its first version, *Bluetooth* used the GFSK modulation in which the positive and negative frequency deviations represent the binary 1 and 0, respectively. Although some recent versions use $\frac{\pi}{4}$ -DQPSK and 8-DPSK (figure 1.1) to achieve 2-Mb/s and 3-Mb/s against the 1-Mb/s from the first version, the symbol rate remains exactly the same, *i.e.* 1-Ms/s [3].

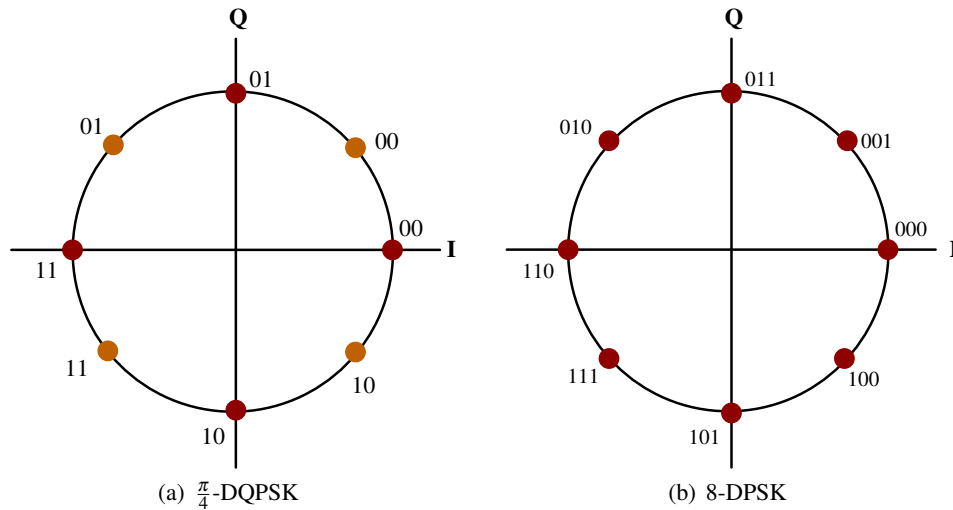


Figure 1.1: Bluetooth modulation schemes.

Figure 1.1(a) shows the $\frac{\pi}{4}$ -DQPSK modulation. It is composed by two equal constellations, 45 degrees ($\frac{\pi}{4}$) out-of-phase from each other. A jump between two symbols is always made with $\frac{3\pi}{4}$, $\frac{\pi}{4}$, $-\frac{\pi}{4}$ or $-\frac{3\pi}{4}$. Therefore the symbols are always jumping between the two existing constellations.

The 8-DPSK modulation is depicted in figure 1.1(b). With this scheme it is possible to achieve data rates up to 3-Mb/s. This is due to the utilization of 3 bits, instead of the 2 bits used in the $\frac{\pi}{4}$ -DQPSK modulation scheme, which allows a 2-Mb/s data rate.

1.3 Power amplifiers overview

The class of a PA is defined by its operation mode, and classes can be separated onto two major groups, those that work in linear and the non-linear mode³. In figure 1.2 some classes are shown separated into the two groups.

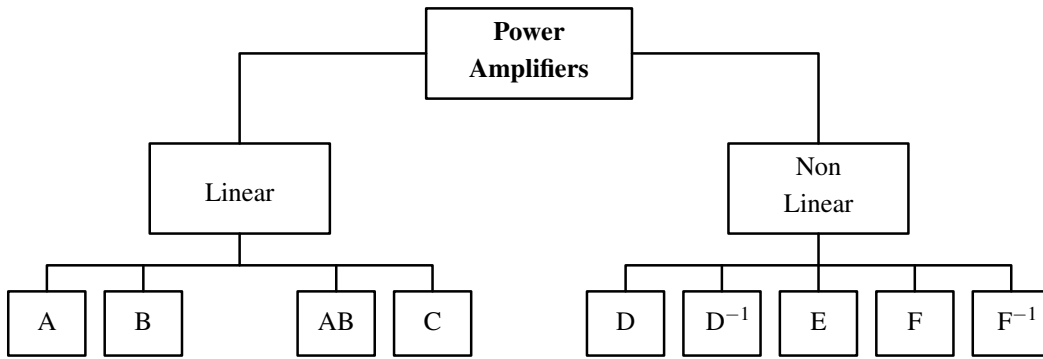


Figure 1.2: Power amplifier classes and groups.

1.3.1 Linear amplifiers

On the linear power amplifiers group, we have the classic topologies A, B, AB and C (figure 1.2). As already referred, this group of amplifiers is able to amplify signals with non-constant envelope, *i.e.* modulated amplitude signals. All these classes share a common topology, that is all of them can be implemented using the same circuit, which is depicted in figure 1.3. The amplifier class of operation is distinguished solely by the bias conditions. All these classes are driven with a sinusoidal waveform, or approximately sinusoidal, and the transistor behaves as a controlled current source, at least for a certain portion of the RF cycle [8].

The tuned parallel LC filter, shown in figure 1.3, is not part of the basic schematic circuit for this kind of amplifiers, but its recommended to filter the signal outside the fundamental frequency. This tuned filter improves the efficiency of the amplifier because the device only "sees" the load at the fundamental frequency; at all the other frequencies the filter acts as a short-circuit.

The class of operation, of linear amplifiers, can easily be identified observing the drain current waveform. The percentage of the RF cycle in which the transistor is conducting defines the

³We consider linear power amplification in the sense that the output magnitude is somehow linearly correlated with the input voltage.

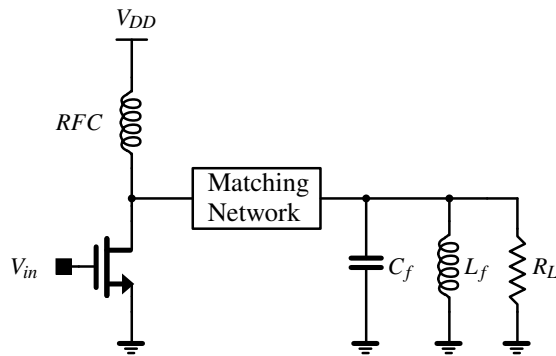


Figure 1.3: Linear power amplifier schematic.

power amplifier operation class. Table 1.3 shows the differences between the linear classes of amplification [9].

Table 1.3: Transistor conduction percentage of the RF cycle.

Class	RF cycle conduction (%)
A	100
B	50
AB	> 50 and < 100
C	< 50

1.3.1.1 Class-A amplifier

To work as a class-A amplifier, the bias levels must be chosen so that the transistor is kept in the active region for all the time. Therefore the drain current waveform has a conduction angle of 360 degrees that is, 100% as shown in figure 1.4.

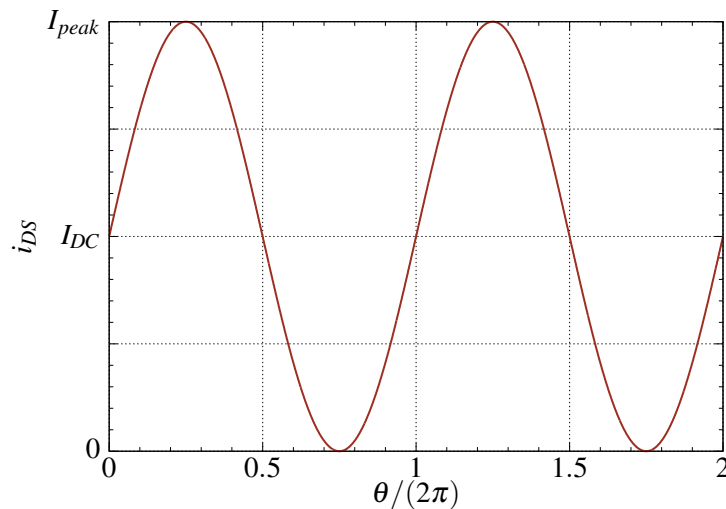


Figure 1.4: Class-A amplifier drain current waveform (two RF cycles shown).

Although the class-A has the highest conduction angle of all linear amplifiers, its efficiency is the lowest off all, achieving only a theoretical maximum of 50%. The class-A amplifier efficiency can be obtained through:

$$\eta_D = \frac{P_{out}}{P_{DC}} \quad (1.1)$$

$$= \frac{1}{2} \cdot \left(\frac{V_{out}}{V_{DD}} \right)^2 \quad (1.2)$$

where, V_{out} is the output voltage amplitude. Hence, it can be concluded that the amplifier only achieves its 50% of maximum efficiency, when the maximal output swing occurs. If this amplifier is used with an amplitude modulated signal, the output voltage, V_{out} , will change according to the envelope signal $A(t)$. If we consider the probability density function of $A(t)$, the efficiency of the amplifier will fluctuate with it, leading to an average efficiency much lower than 50% [2].

1.3.1.2 Class-B amplifier

The class-B amplifiers have their bias levels chosen in a way that the drain current waveform has a conduction angle of 180 degrees. The operation point of the transistor is located exactly at the boundary between the cut-off and the active region [10]. The lower conduction angle, when compared with class-A, increases the efficiency but makes the amplifier less linear. The drain current waveform is depicted in figure 1.5.

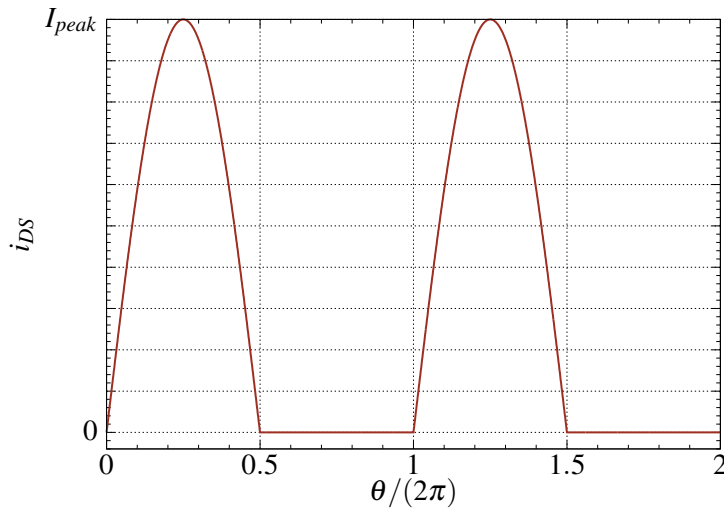


Figure 1.5: Class-B amplifier drain current waveform (two RF cycles shown).

The drain efficiency for a class-B amplifier can be calculated as follows:

$$\eta_D = \frac{\pi}{4} \cdot \frac{V_{out}}{V_{DD}} \quad (1.3)$$

Like in the class-A, amplifier the maximum efficiency only occurs when $V_{out} = V_{DD}$, which leads to an approximated efficiency of 78.5% [10]. If an amplitude modulated signal is amplified, the average efficiency will also drop according to the envelope signal probability density function $A(t)$.

1.3.1.3 Class-AB and C amplifiers

The class-AB configuration works between the class-A and class-B operation, *i.e.* between 180 and 360 degrees. Therefore, depending on its bias levels this kind of amplifier conducts somewhere between 50% and 100% of an RF cycle. It can also be concluded that its drain efficiency lays somewhere between the 50% maximum of the class-A amplifier or the 78.5% of the class-B [9].

As shown in table 1.3, the class-C amplifier has the lowest conduction angle of all the linear amplifiers. Although the efficiency rises when the conduction angle is lowered, the amplifier becomes less linear because turning off the transistor increases the number of higher harmonics generated [2]. This non-ideal behavior is not considered in the present analysis. The LC resonant tank is considered to have a high-quality factor, which becomes a short circuit to other frequencies besides the central one. The drain current waveform is presented in figure 1.6.

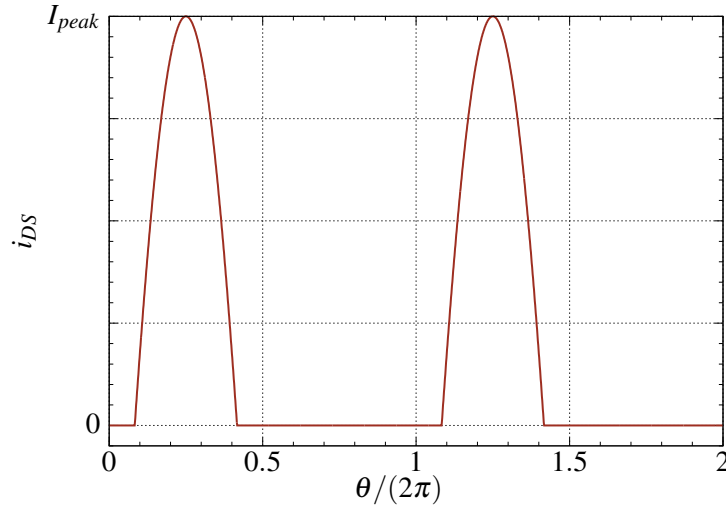


Figure 1.6: Class-C amplifier drain current waveform (two RF cycles shown).

Some authors do not consider the class-C as part of the linear amplifiers group. This is due to its low conduction angle, which greatly reduces the drain current linearity. In fact the amplifier drain efficiency can be arbitrary increased toward 100% by decreasing the conduction angle until zero. This has the drawback of also reducing the utilization factor of the amplifier, toward zero, and increasing the drive power to the infinity [11]. The drain efficiency of a class-C amplifier can be obtained through:

$$\eta_D = \frac{\theta - \sin(\theta)}{4 \left[\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2} \cos\left(\frac{\theta}{2}\right) \right]} \quad (1.4)$$

where θ represents the conduction angle [9], which for a class-C can be $(0; \pi)$. Equation 1.4 is also valid for classes A, B and AB with their respective conduction angles.

In figure 1.7 it is depicted the drain efficiency of the several linear amplifiers presented. Notice that the class-AB and C amplifiers have a range of possible values that depend on the conduction angle, as previously referred.

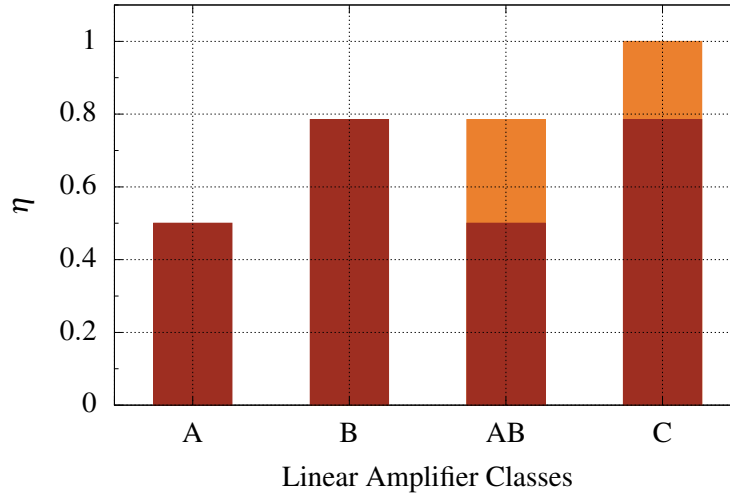


Figure 1.7: Efficiency of linear amplifiers.

1.3.2 Non-linear amplifiers

The non-linear amplifiers group are also known as switch-mode power amplifiers (SMPA). In the non-linear PAs the transistors act like switches by turning on and off during operation. In this group we have the classes D, D^{-1} , E, F and F^{-1} (figure 1.3). An ideal switch dissipates no power, for there is either zero voltage across it or zero current through it. Thus, the resultant product voltage-current is always zero. So, the transistor dissipates no power and the efficiency must be ideally 100% [9], if there are no other losses in the amplifier circuit. This makes this group of amplifiers a good solution to amplify constant envelope signals.

The class- D^{-1} as the main subject of this thesis and will be discussed in detail on chapter 2. A brief analysis on the voltage-mode class-D amplifier is also described on the same chapter.

1.3.2.1 Class-E

The basic configuration of a class-E power amplifier is depicted in figure 1.8. The output network is made up of a series tuned circuit RLC and a shunt capacitor C_s . This capacitor includes the inherent parasitic capacitance of NMOS transistors.

The C_s capacitance value should be carefully designed, because it is the responsible for the soft-switching capability of the class-E amplifier. Hard-switching devices suffer from switching losses. This occurs when the voltage across the transistor drops abruptly from a high value to

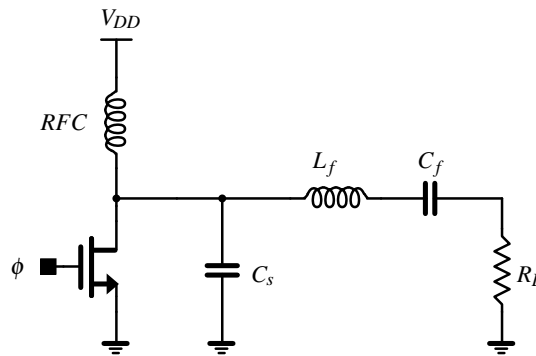


Figure 1.8: Class-E power amplifier schematic.

zero. The shunt capacitance C_s charges and discharges between the ON and OFF state of the transistor. Therefore, C_s does not allow instant variation in the drain voltage. This guarantees a smooth transition between the ON-OFF states of the transistor [10].

Since the class-E architecture absorbs the parasitic capacitance of the transistor with C_s , the so-called ZVS state is achieved. This prevents energy loss at each RF cycle, which is critical at high-frequencies, thus increasing the amplifier performance [2]. As further referred, this energy loss is the major drawback in the use of class-D amplifiers at high-frequencies.

Another switch characteristic responsible for efficiency drop in power amplifiers is the on-resistance, r_{on} , associated with MOS transistors. This parasitic component can be diminished by increasing the transistor size, but this also increases the parasitic C_{DS} capacitor and C_{GS} , increasing driving requirements.

The voltage and current drain waveforms of the device are represented in figure 1.9.

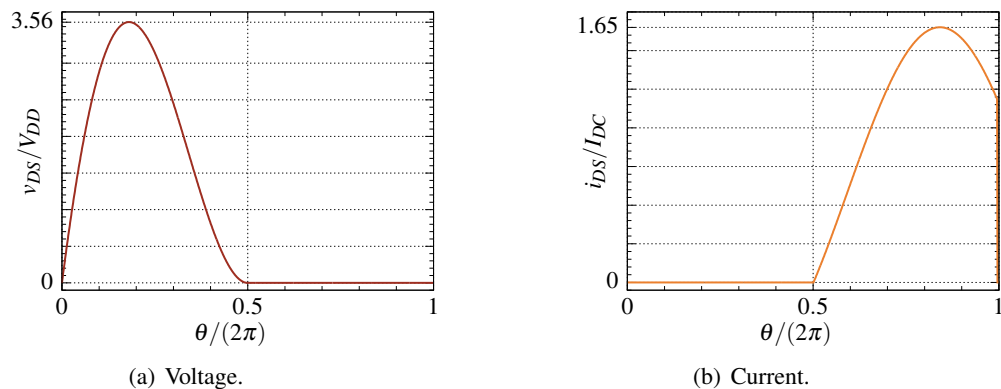


Figure 1.9: Class-E drain current and voltage waveforms.

1.3.2.2 Class-F

Class-F amplifiers present an elegant solution in order to achieve high-efficiency. This class of amplifiers is characterized by a load network with resonance frequencies at one or more harmonic

frequencies as well as at the carrier frequency (figure 1.10).

The tank resonators depicted in figure 1.10 are tuned to odd-harmonics, which maintain a square voltage waveform at the transistor drain and simultaneously provides a half-sinusoidal current waveform [12]. An infinite number of tanks must be used to set the ideal waveform shaping, figure 1.11.

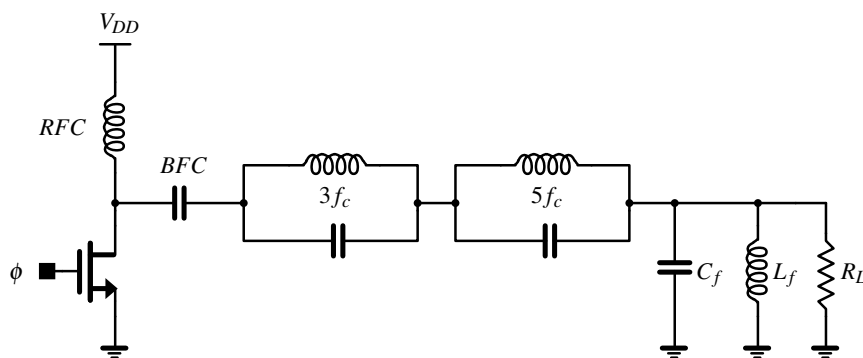


Figure 1.10: Class-F power amplifier schematic with 5th harmonic peaking.

Ideally, all parallel resonant circuits have infinite impedance at the corresponding harmonic resonant frequency and zero impedance at other harmonics [12]. Consequently, the load impedance of the transistor is R_L at fundamental frequency, infinite at the tank resonators frequencies and zero otherwise [8].

From figure 1.11, we can see that ideally there is no overlap between voltage and current due to the harmonic filtering of the tank resonators. Thus, no power dissipation is produced, leading to 100% of theoretical efficiency. In practice, the infinite harmonic tuning is not achievable. Most of the times the load network is setup by harmonic filtering tuned up to the 3rd or 5th harmonic only (commonly called harmonic peaking). This lowers the attainable efficiency well below 100%.

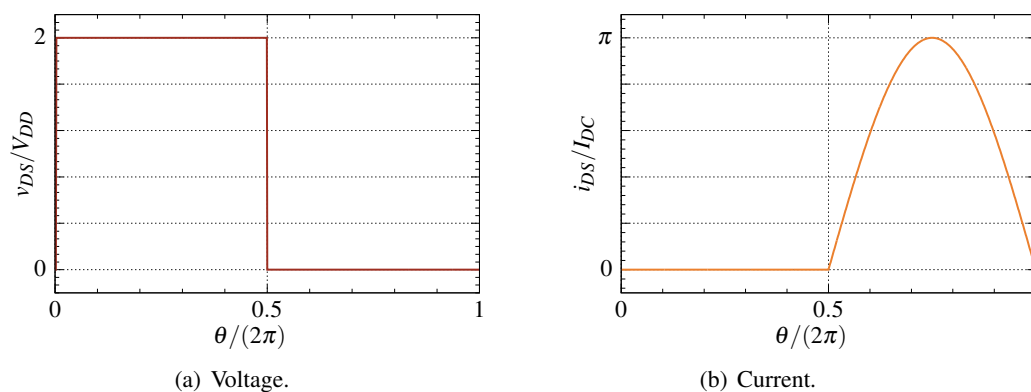


Figure 1.11: Class-F drain current and voltage waveforms.

1.3.2.3 Class-F⁻¹

The inverse class-F power amplifier can be implemented using the circuit presented in figure 1.12. The circuit shown in figure 1.10 can also be used, but now the tank resonators need to be tuned to even-harmonic resonant frequencies. This duality in the configuration can be applied also to the inverse class-F amplifier represented in figure 1.12. Thereby, it is necessary, in this case, to perform the tuning only with even-harmonics [12].

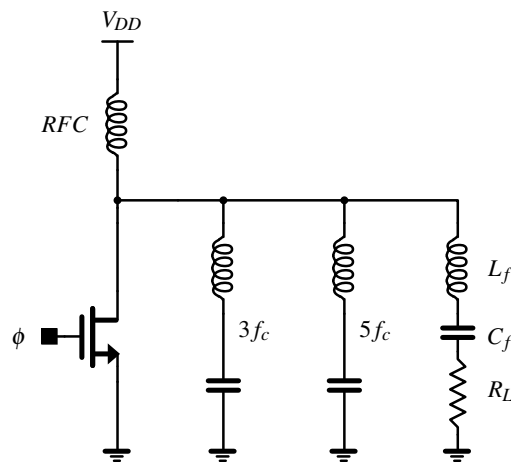


Figure 1.12: Class-F⁻¹ power amplifier schematic with 5th harmonic peaking.

Analyzing the schematic represented in figure 1.12 one realizes that at the fundamental frequency and odd-harmonics, each resonant circuit has zero impedance but infinite impedance at even-harmonics. This produces the idealized square current and the half-sinusoidal voltage waveforms at the drain terminal, as shown in figure 1.13. As a result, the active device "sees" the load resistance R_L at the fundamental frequency, while the odd-harmonics are shorted by the series resonant circuits [12].

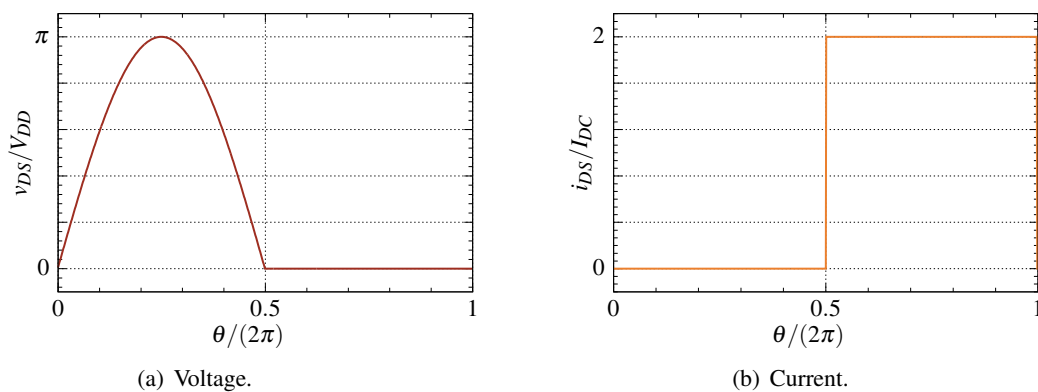


Figure 1.13: Class-F⁻¹ drain current and voltage waveforms.

1.4 State of the art

This section presents a state of the art of reported implementations showing results achieved by several classes of amplifiers working at 2.45GHz. A comparison between some published implementations of CMCD power amplifiers is also covered.

1.4.1 Amplifiers for Bluetooth

Bluetooth technology, in an early version, was operated with a modulation scheme that produces constant envelope signals. More recent versions uses modulation methodologies that combines two types of modulations to send data packages. The constant envelope signal of the early version is lost with the more recent modulations. In [7] is reported an implementation of a simple polar-loop transmitter with a class-E PA that is capable of working with the early version of *Bluetooth*, as well as the medium-rate non-constant envelope signal version.

A very important power amplifier figure of merit (FOM) is the power added efficiency (PAE), which can be calculated by:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \quad (1.5)$$

The PAE can be improved by applying a sliding bias technique like the one described in [13]. This technique is applied to a two stage self-biased cascode PA. PAE is in fact increased, but at the cost of a decrease in power gain.

The peak drain voltage, a problem in class-E due to the low breakdown voltage of transistors, was reduced in [14], thus lowering the chances of damaging the device due to the high drain voltages characteristic of the PAs. The power amplifier is referred as a class BE.

Interesting enough, when all losses are taken into account and for certain component values, a better performance is achievable by diverging from class-E to C [14, 15]. Combinations of distinct classes of amplifiers try to take advantage of the positive aspects of each one to produce better results than the originals. Classes BE and CE are examples of PAs that are able to reduce the peak voltage problem. Class CE has been reported in [16], but presents very low performance (PAE of 25.8%) when compared with class-AB in [1], both fabricated with 0.25 μ m CMOS technologies.

The switching nonlinear amplifiers families share a common practical difficulty, the input square wave needed to achieve high amplifier efficiency. Typically, when the switching amplifiers are driven with non-square waveforms the efficiency diminishes. This is due to the fact that the amplifier momentarily operates as a current source (linear amplifier). A way to deal with this problem is to apply a solution like the one presented in paper [17], where it is described a latch-structured pre-amplifier followed by a class-E PA. The pre-amplifier enables a more ideal switching waveform for the PA, reducing the rise and fall times of the driving signals. The procedure effectively reduces the voltage-current overlap on the switch, optimizing the efficiency of the system. Excellent results are obtained with PAE in the order of 66% [17].

Another work that shows a solution to solve the square wave driving issue is presented in [18]. Here a classical class-E PA is driven by a class-F amplifier to provide a better switching behavior, hence improving the efficiency of the amplifier.

Although the early version of *Bluetooth* was based on constant envelope modulation schemes, linear PA classes have been extensively used. A single-ended two-stage common-source topology biased in class-AB operation is presented in [1]. It uses MOS transistor models developed specifically by *Philips* for high-frequencies with low supply voltage. A maximum PAE of 48% is attained for 24dBm of output power. The referred study also addresses the hot carrier effect as a reliability measurement of the amplifier. This effect happens when high-electric fields, near the drain, damage the crystalline structure of the transistor, increasing threshold voltage and also degrading the overall performance of the device. The hot carrier effect is also responsible for inducing noise into the circuit [19].

A class-AB amplifier is also implemented in [20]. The proposed configuration uses two parallel output stages that can provide different levels of output power. With only one active output stage, the impedance seen by the device is different from the case when the two stages are on, by then controlling delivered output power. A PAE of 22% is achieved with 22.7dBm for output power.

Another configuration that allows different levels of output power is presented in [14]. A set of four amplifiers are implemented on-chip within a differential topology, thus producing two differential power amplifiers. The amplifiers are combined with an on-chip LC balun structure, which also performs impedance transformation that increases the amplifiers output power capability. However the PAE is still very low, 29%. The power control feature is done by turning on or off the circuit amplifiers. When a set of amplifiers is off, the LC balun section becomes a high-impedance parallel tank, connected in parallel with the load.

Table 1.4 shows a short compilation of results obtained in the previously discussed works and others. This gives us a perspective on how the research is currently being performed in this field. All the class-E implementations have more than 30% in PAE. Most of the works have an output power of about 20dBm. One can also note that drain efficiency values are quite higher for switching PAs. On the other hand, due to the need for square wave drive, P_{in} can be higher when compared to linear PAs. The dissipated power value turns out to be lower in switching PAs, thus justifying the higher PAE achieved in switching PA classes.

Note that not a single class-D amplifier is reported in table 1.4 since it cannot be found in literature for 2.45GHz. This somehow indicates its inability to produce good results at RF frequencies.

1.4.2 Class-D⁻¹ amplifiers

A straightforward comparison between the VMCD and CMCD architectures is performed in [26]. The inability of VMCD to work at high-frequencies is presented. The main responsible is, as already referred, the inexistent ZVS condition. The CMCD is presented as a solution. A

Table 1.4: State of the art of *Bluetooth* amplifiers

Class	Technology (μm)	Max. power (dBm)	PAE (%)	η_D (%)	Ref.	Year
AB	CMOS 0.25	24	48	-	[1]	2001
AB	CMOS 0.35	19	33.7	-	[21]	2006
AB	CMOS 0.18	3.5	-	16	[22]	2003
AB	CMOS 0.25	22.7	22	-	[20]	2003
B	CMOS 0.24	23	39	45	[23]	2000
BE	CMOS 0.13	23	29	35	[14]	2007
CE	CMOS 0.25	21.4	25.8	38	[16]	2002
E	CMOS 0.25	20	65.8	66.4	[17]	2005
E	CMOS 0.35	13	30.7	-	[7]	2005
E	CMOS 0.35	20	59	64	[18]	2003
E	CMOS 0.35	20	35	-	[24]	2003
F	BiCMOS 0.24	20	34.2	-	[25]	2006
-	CMOS 0.18	23	42	-	[13]	2003

theoretical analysis of a class-D⁻¹ is also described in [26] as well the circuit implementation and its results.

In [27] the characteristics of both VMCD and CMCD power amplifiers are also described. Several design considerations are discussed, like the high-order odd harmonic effects, as well as the parasitic resistance of the LC resonator. This parasitic resistance might be of great importance, because it is pointed out as a critical part of the overall system. Two different amplifiers were fabricated, one with a bond-wire and the other with an on-chip spiral inductor. Better results were achieved with the bond-wire implementation due to the high-quality factor that this solution provides. Also in work [27], input and output baluns are used in order to get unbalanced input and output, while the PA works in differential mode.

Works [28–31] present CMCD power amplifiers manufactured in various technologies. Different implementation methodologies applied in the design process of these PAs are exposed in each work. A direct explanation about the advantage of ZVS amplifiers over the non-ZVS is made in [28]. Work [29] reports the highest output power of all CMCD power amplifiers presented, and the second best drain efficiency. Another comparison between the the voltage-mode and current-mode class-D power amplifiers is made in [30]. The class-D⁻¹ basic principles of operation are also discussed in [31].

Table 1.5 shows the results obtained for the discussed CMCD amplifiers. However, none of these works operate at our frequency of interest, 2.45GHz, neither are implemented in Si-CMOS.

Table 1.5: State of the art of class-D⁻¹ amplifiers

Technology	Frequency (GHz)	Max. power (dBm)	η_D (%)	Ref.	Year
GaAs FET	0.9	24.6	76.3	[26]	2001
GaAs HBT	0.7	29.5	78.5	[27]	2005
GaN HEMT	1	36	64.4	[28]	2007
GaN MESFET	0.9	43.2/47.1	75/78	[29]	2007
LDMOS	1	41.1	60	[30]	2002
LDMOS	1	43.1	71	[31]	2006

Chapter 2

Class-D⁻¹ Power Amplifier

This chapter presents a group of analysis on the class-D⁻¹ power amplifier behavior. First the basic operation of the amplifier is demonstrated. Next, an ideal analysis comprising the key features of the CMCD power amplifier, like the ZVS state and its low peak drain voltage, is presented. The main FOM are also analyzed.

The last study focuses on the non-ideal behavior of the CMCD power amplifier. A study on the impact of the load network quality factor in the circuit performance is first presented. Afterward, a study is made to understand the influence of the inductor unloaded quality factor, along with QL, has on amplifier efficiency.

2.1 Current-Mode Class-D power amplifier

The current-mode class-D power amplifier is the dual version of the voltage-mode class-D power amplifier. Its architecture is shown in figure 2.1. As presented, the CMCD is constituted by two branches, each with a radio-frequency choke (RFC) and an NMOS transistor. A RLC differential network, tuned to the central frequency, connects the two branches of the circuit.

Like any other SMPA, the class-D⁻¹ power amplifier can achieve 100% of theoretical efficiency since the transistors act like switches, maximizing this way the amplifier performance. This high theoretical efficiency is achieved because ideal switches only have voltage across them or current flowing through¹, never both at the same time. This non-overlapping of voltage and current means that no power dissipation is produced, thus the PA manages to achieve 100% of theoretical efficiency. However, available transistors are not ideal switches, because they have parasitic capacities and inductors as well as finite on resistance r_{on} , which degrades the overall performance of the amplifier [26].

¹An open ideal switch has only a voltage drop across him, while a closed one only has current flowing through.

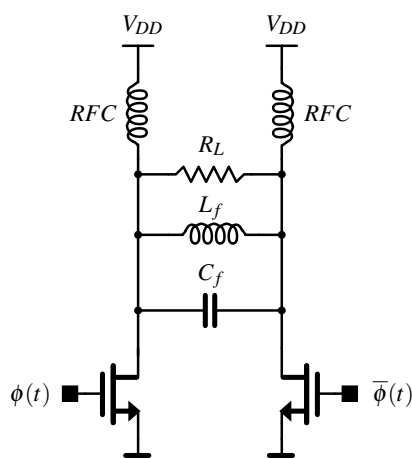
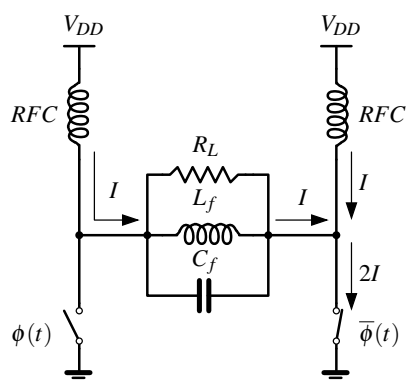


Figure 2.1: Circuit of the CMCD power amplifier.

2.2 Basic operation

In this current-mode class-D amplifier configuration, the transistors are driven by two square waves, in opposite phase. Then only one transistor will be switched on at a time. Since the RFCs act like DC current sources, the current is always switching from one branch of the circuit to the other, passing through the RLC network. From here, we can say that the current is a square waveform with 50% of duty-cycle in each side of the circuit, and with 180 degrees out-of-phase. This operation is depicted in figure 2.2.

Figure 2.2: Current flow in the class- D^{-1} power amplifier.

One can then say that a zero centred square current waveform is applied to the RLC network. This waveform can be derived through the Fourier series,

$$i_{RLC}(\theta) = \sum_{-\infty}^0 i_{-k} e^{jk\theta} + \sum_0^{\infty} i_k e^{-jk\theta} \quad (2.1)$$

$$= i_0 + \sum_{k=1}^{\infty} i_k (e^{jk\theta} + e^{-jk\theta}) \quad (2.2)$$

where $\theta = \omega_0 t$ and $i_k = i_{-k}$ because $i_{RLC}(\theta)$ its an even function.

The first member of equation 2.2 can be obtained through,

$$i_0 = \frac{1}{\pi} \int_{-\pi}^{-\frac{\pi}{2}} \frac{-I_{peak}}{\omega_0} e^0 d\theta + \frac{1}{2\pi} \int_{\frac{\pi}{2}}^{\pi} \frac{I_{peak}}{\omega_0} e^0 d\theta \quad (2.3)$$

which leads to $i_0 = 0$. We can also calculate i_k as follows:

$$i_k = \frac{1}{\pi} \int_{-\pi}^{-\frac{\pi}{2}} \frac{-I_{peak}}{\omega_0} e^{-jk\theta} d\theta + \frac{1}{2\pi} \int_{\frac{\pi}{2}}^{\pi} \frac{I_{peak}}{\omega_0} e^{-jk\theta} d\theta \quad (2.4)$$

$$= \frac{8I_{peak}}{k\pi} \sin\left(\frac{k\pi}{4}\right)^3 \cos\left(\frac{k\pi}{4}\right) \quad (2.5)$$

Combining equations 2.2 and 2.5, gives us the square waveform formula,

$$i_{RLC}(\theta) = \sum_{k=1}^{\infty} \frac{16I_{peak}}{k\pi} \sin\left(\frac{k\pi}{4}\right)^3 \cos\left(\frac{k\pi}{4}\right) \cos(k\theta) \quad (2.6)$$

which can be simplified to look like,

$$i_{RLC}(\theta) = \sum_{k_{odd}}^{\infty} \frac{4I_{peak}}{k\pi} \sin\left(\frac{k\pi}{2}\right) \cos(k\theta) \quad (2.7)$$

$$= \frac{4I_{peak}}{\pi} \sum_{k_{odd}}^{\infty} \frac{1}{k} \cos(k\theta + \varphi_k) \quad (2.8)$$

where φ_k assumes the following values:

$$\begin{cases} 0 & k = 1, 5, 9, \dots \\ \pi rad & k = 3, 7, 11, \dots \end{cases} \quad (2.9)$$

Since the RLC parallel network is tuned at the fundamental frequency f_c , at all the other frequencies it acts like a short-circuit. This way, there is only current flowing through R_L at the frequency of interest, *i.e.* a sinusoidal current waveform². Therefore, a sinusoidal voltage waveform is also present at the R_L load, which means a semi-sinusoidal waveform at each branch of the circuit. Thus, the voltage at the load network can be expressed as follows:

²Assuming that we have an infinite quality factor Q_L .

$$v_{RLC}(\theta) = |I_1| R_L \cos(\theta + \varphi_1) \quad (2.10)$$

$$= \frac{4}{\pi} I_p R_L \cos(\theta) \quad (2.11)$$

Because there is no voltage drop across the RFCs, and having a semi-sinusoidal waveform with a mean value V_{DD} at each branch the peak drain voltage is πV_{DD} [26]. This can be obtained through:

$$V_{DD} = \frac{1}{2\pi} \int_0^\pi \frac{v_{DS}(\theta)}{\omega} d\theta \quad (2.12)$$

$$= \frac{1}{2\pi} \int_0^\pi \frac{V_{peak} \sin(\theta)}{\omega} d\theta \quad (2.13)$$

$$= \frac{V_{peak}}{\pi} \quad (2.14)$$

In figure 2.3 a comparison between the drain peak values of several SMPA is made. It can be noticed that there are classes with a lower peak drain voltage than the CMCD, namely the class-D, the class-F and its inverse architecture. As further referred ahead, the VMCD power amplifier, with a peak drain voltage value equal to V_{DD} [10], is unable to work at high frequencies due to the intrinsic parasitic capacitance of the active devices. The class-F amplifier and its dual version, with a peak voltage of $2V_{DD}$ and $\frac{\pi V_{DD}}{2}$ respectively [12], depend on the number of attainable harmonic tuning, which in practice lowers the overall efficiency.

We can now represent the ideal waveforms for the class- D^{-1} PA. To perform this, we also need to calculate the value of the peak drain current. Having V_{peak} , the peak current value can be obtained through:

$$I_{peak} = \frac{\pi^2}{4} \cdot \frac{V_{DD}}{R_L} \quad (2.15)$$

With the peak values of the drain voltage and current and considering a infinite quality factor Q_L for the load network, we have a half-sinusoidal wave and a 50% duty-cycle square waveform for the drain voltage and current respectively, at each branch of the circuit depicted in figure 2.1. The ideal waveforms for the CMCD power amplifier can be represented as in figure 2.4.

2.3 Ideal analysis

As already said before, transistors are not ideal switches with their inherent parasitic components such as the intrinsic capacity C_{DS} , the finite on-resistance r_{on} and an associated parasitic

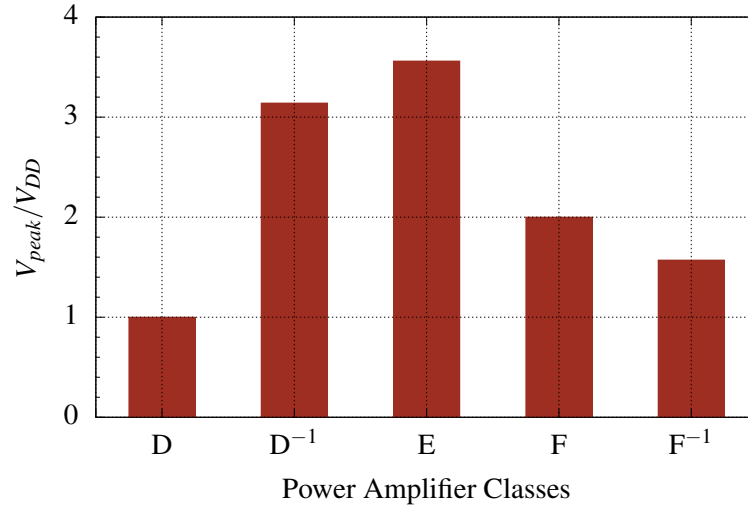


Figure 2.3: Drain peak voltage of several SMPA.

inductor. In fact, the key issue related to the inability of applying the VMCD power amplifier at RF frequencies is the C_{DS} parasitic capacitance, that exists in all transistors. In figure 2.5 the basic schematic for a class-D power amplifier is presented.

The C_{DS} parasitic capacitance of the transistors will charge during turn on to V_{DD} , so the instant non-null overlapping of voltage and current cannot be avoided. This causes an energy accumulation:

$$E_C = \frac{1}{2}C_{DS}V^2 \quad (2.16)$$

in C_{DS} that is dissipated in r_{on} and reduces the overall efficiency of the amplifier [27]. The power dissipation can be described by:

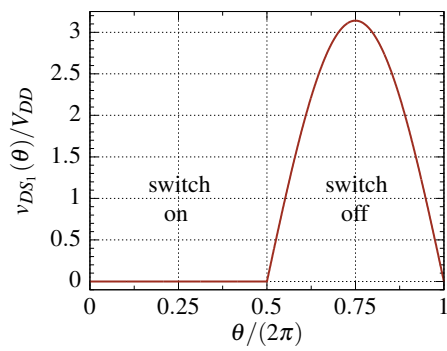
$$P_{diss} = \frac{1}{2}fC_{DS}V^2 \quad (2.17)$$

The power dissipation increases with the frequency of operation of the devices, making the class-D architecture not good solution for RF applications [2].

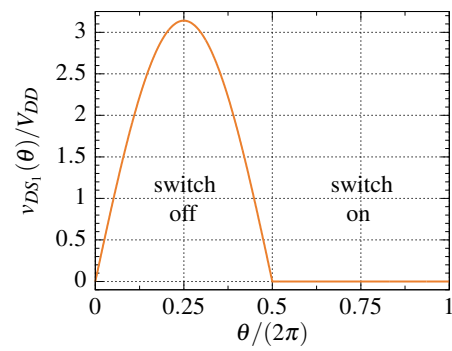
A possible solution to solve the voltage and current overlap problem is to apply a ZVS amplifier architecture. This can be accomplished using the class- D^{-1} PA (figure 2.1). If the RLC load network has an infinite quality factor Q_L , which can be expressed by:

$$Q_L = \frac{R_L}{\omega_c L} \quad (2.18)$$

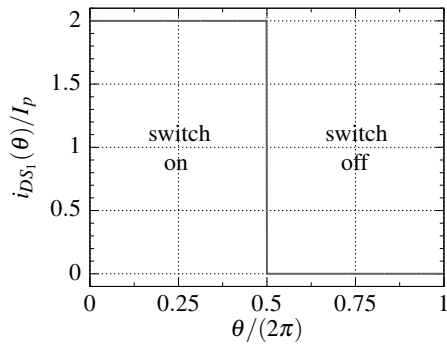
the load acts like a short circuit at all frequencies except at the fundamental. This guarantees that there is no voltage across the transistors at the switching time, and the so-called ZVS is achieved. Therefore, the VMCD problem is apparently solved. Other PA architectures can also achieve ZVS, like the class-E and the class-F. While the class-E PA has a higher peak drain voltage than



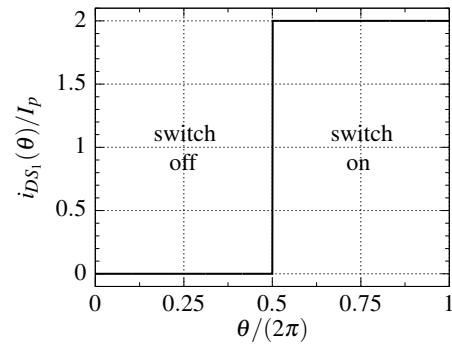
(a) Voltage waveform in switch 1.



(b) Voltage waveform in switch 2.



(c) Current waveform in switch 1.



(d) Current waveform in switch 2.

Figure 2.4: CMCD power amplifier waveforms.

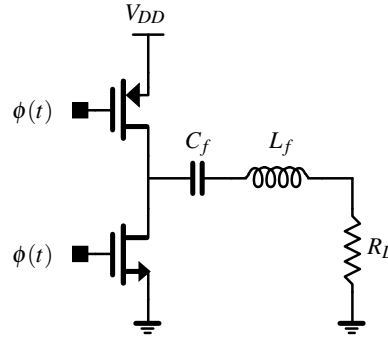
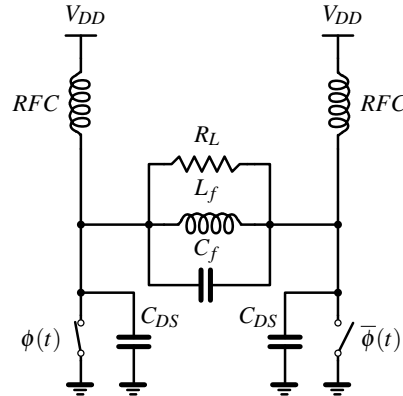


Figure 2.5: Circuit of the VMCD power amplifier.

the CMCD³ [2, 10, 12], which is important due to the low breakdown voltage of CMOS devices, the class-F is limited to the finite harmonic tuning that lowers his overall performance.

In the class-D⁻¹ architecture, even the C_{DS} parasitic capacitances are absorbed and become part of the parallel filter. In figure 2.6, $\phi(t)$ is on with its parasitic capacity shorted to GND while the C_{DS} capacitance of the other switch is in parallel with C_f . The same occurs when $\bar{\phi}(t)$ is on due to the circuit symmetry. The ZVS state along with a lower drain peak voltage are the key features of the CMCD power amplifier.

Figure 2.6: Class-D⁻¹ power amplifier with parasitic capacities.

Another important feature to take into account in a power amplifier is the zero-current-switching (ZCS), which avoids inductance losses by making the current zero at the switching instant. This energy loss can be obtained through:

$$E_I = \frac{1}{2}LI^2 \quad (2.19)$$

Although this feature is not present in the the class-D⁻¹ power amplifier, it is less important than the ZVS, because the way transistors are modeled [26]. However it is important to diminish its value in order to improve the amplifier efficiency.

³The class-E power amplifier has a peak drain voltage of approximately $3.56V_{DD}$, while the CMCD peak voltage value is πV_{DD} .

Another relevant FOM of a power amplifier is the output power it can deliver, *i. e.* the power dissipated in R_L at f_c . This can be easily obtained through:

$$P_{out} = \frac{1}{2} \text{Re}\{V_{RLC}I_{RLC}^*\} \quad (2.20)$$

$$= \frac{8}{\pi^2} R_L I_{peak}^2 \quad (2.21)$$

$$= \frac{\pi^2}{2} \cdot \frac{V_{DD}^2}{R_L} \quad (2.22)$$

Calculating the supplied power to the circuit leads to:

$$P_{DC} = V_{RLC}I_{RLC} \quad (2.23)$$

$$= \frac{\pi^2}{2} \cdot \frac{V_{DD}^2}{R_L} \quad (2.24)$$

With P_{out} and P_{DC} its possible to evaluate another important FOM in the power amplifiers domain, the drain efficiency η_D . This quality measure of a PA can be obtained with,

$$\eta_D = \frac{P_{out}}{P_{DC}} \quad (2.25)$$

which in a class- D^{-1} , like in other SMPA architectures considering all the components lossless, achieves a theoretical efficiency of 100%.

The different classes of power amplifiers do not differ solely in the method of operation and in the efficiency capability. The transistor utilization factor is also an important FOM of a power amplifier [11]. This relevant measure is expressed by:

$$U_f = \frac{1}{n} \cdot \frac{P_{out}}{V_{peak}I_{peak}} \quad (2.26)$$

Applying the equation to the CMCD power amplifier we obtain a $\frac{1}{2\pi}$ utilization factor. A comparison between the U_f of several classes of power amplifiers is made in figure 2.7. Here we can see that the CMCD power amplifier and its voltage mode dual architecture, the class-D PA, have the highest utilization factor of all [11]. This indicates a good exploitation of the circuit resources.

The U_f for the class-F, and its inverse version, assumes different values according to the number of harmonic tuning that is applied. The lowest value, with just one harmonic tuning, is the same as the one obtained in power amplifier classes A and B, *i. e.* $\frac{1}{8}$, while the highest equals the classes D and D^{-1} [11]. Opposing to this attainable high utilization factor is the class-E PA, which has the lowest U_f from all the compared classes in the chart [11, 12].

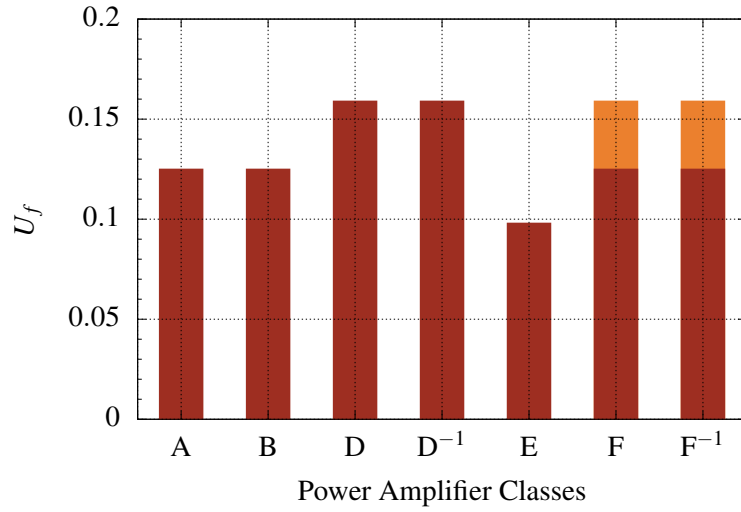


Figure 2.7: Utilization factor comparison between several power amplifiers.

2.4 Non-ideal analysis

In this section of the class- D^{-1} power amplifier analysis, the parasitic components that cause a non-ideal behavior will be taken into account. The first study is the impact of the RLC network quality factor in the performance of the amplifier. Next the inductor unloaded quality factor Q_u influence is also studied, along with the Q_L quality factor.

2.4.1 Impact of Q_L in the circuit performance

To study the effect of the RLC network quality factor, we consider the transistors as ideal switches that is, with zero r_{on} and free of any other parasitic components. The RFCs are also considered to be ideal current sources, providing in both sides of the circuit an equal current. Having this in mind, to better perform an analysis on the RLC network we can transform the CMCD basic architecture into an equivalent electric circuit, depicted in figure 2.8.

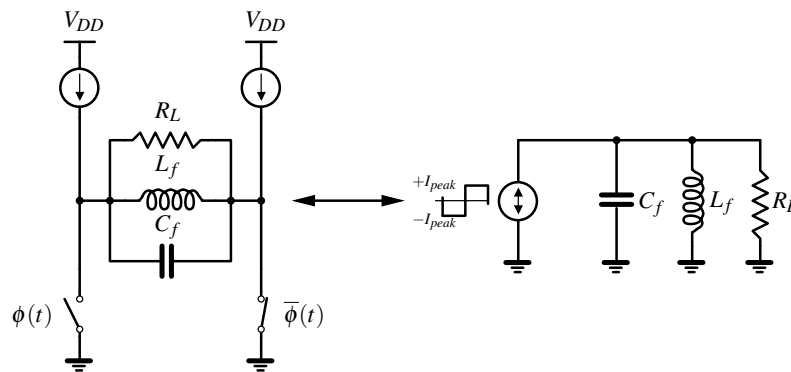


Figure 2.8: CMCD ideal architecture and equivalent circuit.

The equation of the load network is given by:

$$Z_{eq} = \frac{j\omega R_L L_f}{R_L - R_L L_f C_f \omega^2 + j\omega L_f} \quad (2.27)$$

$$= R_L \cdot \frac{k^2 + jkQ_L(1-k^2)}{k^2 + Q_L^2(1-k^2)^2} \quad (2.28)$$

where for every harmonic,

$$\omega = k\omega_c \quad (2.29)$$

At the fundamental frequency, the value of Z_{eq} is always R_L . If Q_L is assumed to be an infinite value, the load network acts like a short circuit for all the other harmonics, *i.e.* $\text{Re}\{Z_{eq} = 0\}$ for all harmonics except for the fundamental one. When Q_L is not infinite, Z_{eq} assumes non-null values for every harmonic. This behavior is shown in figure 2.9.

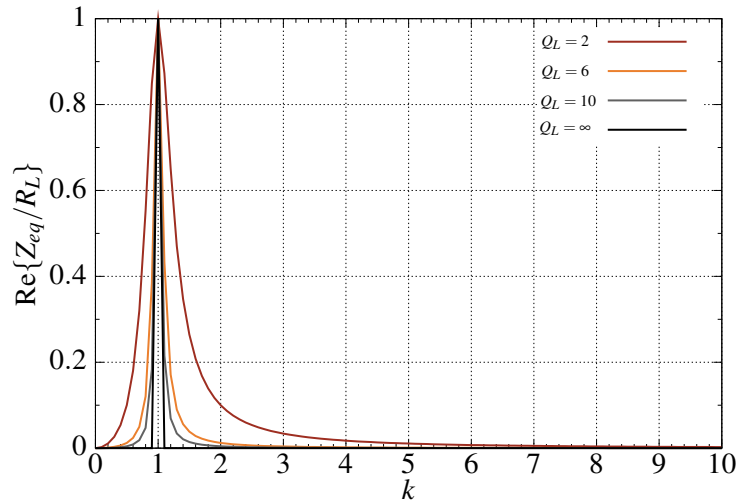


Figure 2.9: Value of the RLC network for various harmonics and Q_L .

The non-ideal response of the RLC network has an impact on the overall performance of the PA. Power is dissipated at other harmonics besides the central frequency, which causes the efficiency of the power amplifier to drop. The power at each harmonic can be obtained with equation 2.8 and 2.28 through:

$$P_k = \frac{1}{2} \text{Re}\{Z_{eq} |I_k|^2\} \quad (2.30)$$

$$= \frac{8I_{peak}^2 R_L}{\pi^2} \cdot \frac{1}{k^2 + Q_L^2(1-k^2)^2} \quad (2.31)$$

Moreover the total power dissipated in the load network can be calculated by,

$$P_{DC} = \sum_{k_{odd}}^{\infty} P_k \quad (2.32)$$

and the power dissipated at the frequency of interest is given by,

$$P_{out} = P_{k=1} \quad (2.33)$$

$$= \frac{8I_{peak}^2 R_L}{\pi^2} \quad (2.34)$$

Thus the drain efficiency η_D of the PA can now be calculated with equation 2.25, which leads to:

$$\eta_D = \frac{1}{\sum_{k_{odd}}^{\infty} \frac{1}{k^2 + Q_L^2(1-k^2)^2}} \quad (2.35)$$

In picture 2.10 is depicted the influence of the load network quality factor in the power amplifier drain efficiency. A low Q_L has a great impact on the PA performance and can in fact diminish it. If the RLC quality factor is under 2, a considerable drop in the amplifier efficiency can be noticed.

As further referred in this work, if other non-ideal components of the CMCD are taken into account, a low Q_L does not mean a poorer performance.

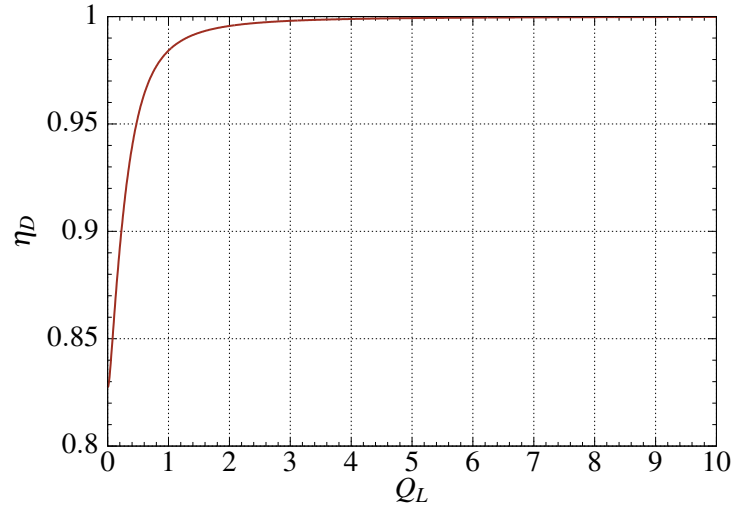


Figure 2.10: Efficiency of the CMCD for various values of Q_L .

2.4.2 Influence of Q_u in the circuit performance

In RF-CMOS technologies on-chip inductors have a poor performance, *i.e.* a low quality factor typically between 5 to 20. Integrated inductors bring with them many parasitic components that degrade their quality factor. This has great impact on the overall performance of the circuit, thus making inductors critical components for a PA [32]. It is then necessary to have inductors with

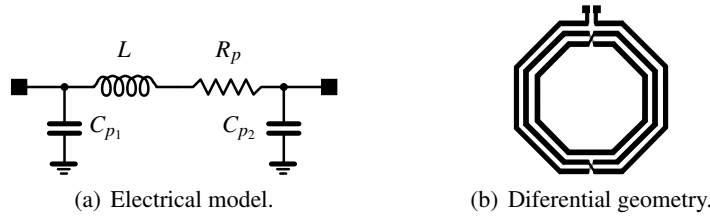


Figure 2.11: On-chip inductor.

the highest quality factor possible, reducing this way the impact of the parasitic components. The unloaded quality factor of an inductor can be calculated through:

$$Q_u = \frac{\omega_c L}{R_p} \quad (2.36)$$

In figure 2.11(a) a simplified electrical π -model of an on-chip inductor is presented [2, 33]. It is composed by the inductance L , its parasitic resistance R_p and the associated parasitic capacitances C_{p1} and C_{p2} . This simplified model does not take into consideration the substrate parasitic components.

The CMCD power amplifier has a differential inductor, which is part of its RLC differential network. Differential inductors, such as the one represented in figure 2.11(b), have approximately equal parasitic capacitances on both sides that is, $C_{p1} \approx C_{p2}$. The value of the inductance is also the same in both of its ports. Although the parasitic capacitances of the inductor are absorbed as part of the PA load network capacitance C_f , the parasitic resistance R_p plays an important role in the power amplifier efficiency.

In order to study the impact of an on-chip inductor, once again the transistors will be considered as ideal switches, free of any parasitic components. The chokes act like ideal current sources, providing in both sides of the CMCD power amplifier circuit an equal current. A parasitic resistance R_p in series with the inductor L_f of the RLC network is used to simulate the on-chip inductor. Figure 2.12 depicts this architecture and its equivalent circuit to better perform future analysis.

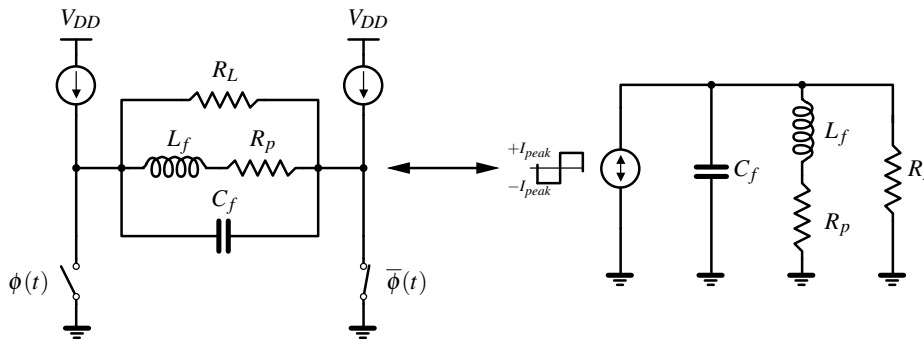


Figure 2.12: CMCD architecture with parasitic resistance of the on-chip inductor and equivalent circuit.

The load network equation is given by,

$$Z_{eq} = \frac{R_L(R_p + j\omega L_f)}{R_p + j\omega L_f + R_L(1 + j\omega C_f(R_p + j\omega L_f))} \quad (2.37)$$

$$= R_L \cdot \frac{kQ_u - j}{k(Q_L + Q_u) + j[Q_L Q_u(k^2 - 1) - 1]} \quad (2.38)$$

$$= R_L \cdot \frac{1 + Q_u(Q_L + k^2 Q_u) - j[kQ_L(1 + Q_u^2(k^2 - 1))]}{k^4 Q_L^2 Q_u^2 + (Q_u Q_L + 1)^2 + k^2(Q_u^2 + Q_L^2(1 - 2Q_u^2))} \quad (2.39)$$

$$= R_L \cdot \frac{1 + Q_u(Q_L + k^2 Q_u) - j[kQ_L(1 + Q_u^2(k^2 - 1))]}{k^2(Q_L + Q_u)^2 + (Q_L Q_u(k^2 - 1) - 1)^2} \quad (2.40)$$

where with equations 2.18 and 2.36 R_p can be written as:

$$R_p = \frac{R_L}{Q_L Q_u} \quad (2.41)$$

From equation 2.40 we can calculate the value of the load network at the fundamental frequency as follows:

$$\text{Re}\{Z_{eq_{k=1}}\} = R_L \cdot \frac{Q_u(Q_L + Q_u) + 1}{(Q_L + Q_u)^2 + 1} \quad (2.42)$$

One can see that when R_p is taken under consideration, the quality factors Q_L and Q_u strongly affect the real part of the RLC network. When the R_p is not contemplated in the circuit design, *e.g.* using a ideal inductor, the real part of the load network is always R_L as depicted in figure 2.9. On the other hand, if the on-chip parasitic resistance is considered as part of the PA design, a combination of quality factors Q_L and Q_u modify the real part of the RLC network at the central frequency. This has a deep impact on the power amplifier efficiency. This behavior is shown in figure 2.13.

Considering equation 2.42 and figure 2.13, we can see that the real part value of the load network drops when $Q_L \rightarrow \infty$ and rises when $Q_u \rightarrow \infty$. From here we can say that a high quality factor of the load network by itself does not mean high efficiency by the power amplifier. In fact with a low Q_L and a high Q_u it is possible to obtain better results.

The impact of Q_u and Q_L on the power amplifier efficiency can now be analyzed. First it is necessary to have the power at each harmonic in the RLC network. This can be obtained with equations 2.8 and 2.40 as follows:

$$P_k = \frac{1}{2} \text{Re}\{Z_{eq} |I_k|^2\} \quad (2.43)$$

$$= \frac{8I_{peak}^2 R_L}{\pi^2} \cdot \frac{1}{k^2} \cdot \frac{Q_u(Q_L + k^2 Q_u) + 1}{k^2(Q_L + Q_u)^2 + (Q_L Q_u(k^2 - 1) - 1)^2} \quad (2.44)$$

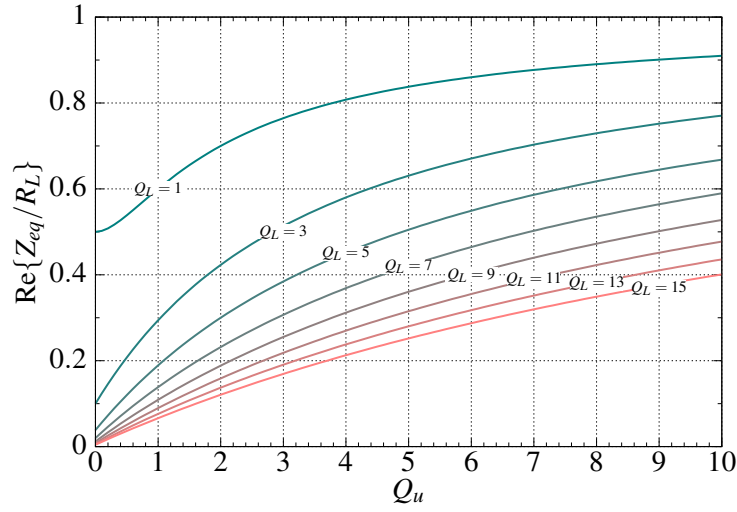


Figure 2.13: Value of the RLC network at f_c for several Q_L and Q_u .

Secondly, the total power dissipated at all harmonics in the load network can be calculated, as already referred in equation 2.32, through:

$$P_{DC} = \sum_{k_{odd}}^{\infty} P_k \quad (2.45)$$

where the power at the central frequency in the load network can be calculated with,

$$P_{k=1} = \frac{8I_{peak}^2 R_L}{\pi^2} \cdot \frac{Q_u(Q_L + Q_u)}{(Q_L + Q_u)^2 + 1} \quad (2.46)$$

$$= \frac{8I_{peak}^2}{\pi^2} \cdot \text{Re}\{Z_{eqk=1}\} \quad (2.47)$$

At the fundamental frequency the power is dissipated not only through the load resistance R_L but also through the parasitic resistance R_p . Only the power dissipated through R_L can be considered to calculate the PA efficiency. The power consumed in R_p is wasted energy. Thus, it is necessary to calculate the current that flows through R_L at f_c . This current can be obtained as follows:

$$I_{RLk=1} = \frac{Z_{eqk=1}}{R_L} \cdot I_{RLC} \quad (2.48)$$

$$= \frac{4I_{peak}}{\pi} \cdot \frac{Q_u(Q_u + Q_L) + 1 - jQ_L}{(Q_u + Q_L)^2 + 1} \quad (2.49)$$

Moreover the power amplifier output in R_L at the frequency of interest can now be expressed by:

$$P_{out} = \frac{1}{2} R_L |I_{RLk=1}|^2 \quad (2.50)$$

$$= \frac{8I_{peak}^2}{\pi^2} \cdot \frac{[Q_u(Q_u + Q_L) + 1]^2 + Q_L^2}{[(Q_u + Q_L)^2 + 1]^2} \quad (2.51)$$

$$= \frac{8I_{peak}^2}{\pi^2} \cdot \frac{Q_u^2 + 1}{(Q_L + Q_u)^2 + 1} \quad (2.52)$$

We now have all the data needed to calculate the class-D⁻¹ PA efficiency. Therefore, using equations 2.45 and 2.52 the expression for the power amplifier efficiency can be written by:

$$\eta_D = \frac{\frac{Q_u^2 + 1}{(Q_L + Q_u)^2 + 1}}{\sum_{k_{odd}}^{\infty} \frac{1}{k^2} \cdot \frac{Q_u(Q_L + k^2 Q_u) + 1}{k^2(Q_L + Q_u)^2 + (Q_L Q_u(k^2 - 1) - 1)^2}} \quad (2.53)$$

$$= \frac{F(Q_L, Q_u)}{\sum_{k_{odd}}^{\infty} \frac{1}{k^2} \cdot \frac{Q_u(Q_L + k^2 Q_u) + 1}{k^2(Q_L + Q_u)^2 + (Q_L Q_u(k^2 - 1) - 1)^2}} \quad (2.54)$$

where,

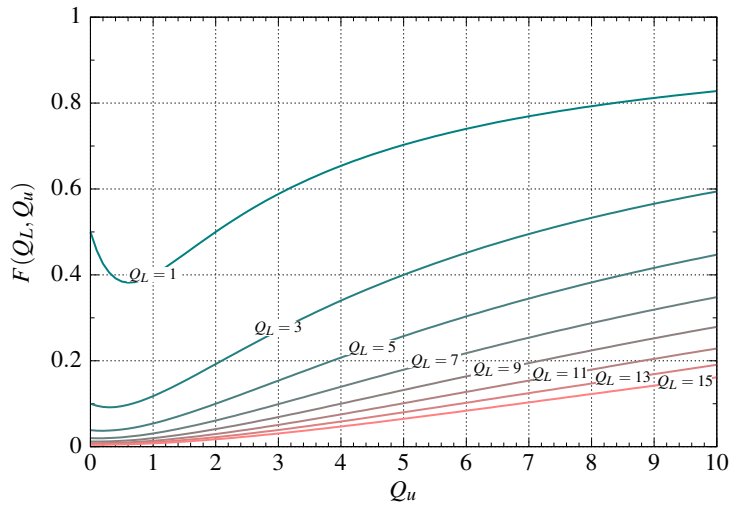
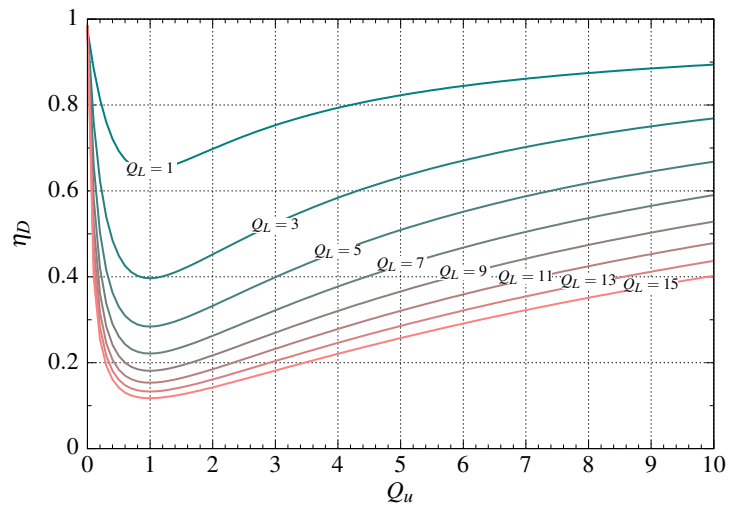
$$F(Q_L, Q_u) = \frac{Q_u^2 + 1}{(Q_L + Q_u)^2 + 1} \quad (2.55)$$

which is the normalized output power of the PA. The impact of Q_L and Q_u on the CMCD efficiency and output power is depicted in figure 2.14. When $Q_L \rightarrow \infty$ the power output and the efficiency drop but, the two FOM rise when $Q_u \rightarrow \infty$.

Analyzing picture 2.14 it can be verified that low values of Q_L are beneficial. Since in RF-CMOS, as already referred, integrated inductors have poor quality factors, *i.e.* a maximum value between 5 to 20 depending on the technology employed, the use of a low Q_L is almost mandatory in order to get an high performance from the PA. Therefore, a logical first step in the power amplifier design is to select a low value for Q_L , and through equation 2.18 calculate the value of the inductor for the RLC network. Then, in the selected technology choose the inductor with the highest Q_u with the value previously obtained. This enables numerous combinations between Q_L and Q_u in order to achieve the best results.

Lowering the quality factor of the load network increases the number of harmonics present at the load (antenna). In the ideal case, the RLC network acts like an short circuit at all frequencies except at the carrier frequency, dissipating the entire power in R_L and achieving 100% of efficiency. So, a low Q_L increases the number of power dissipated at other harmonics. In fact, if we calculate the ratio between the total power and the power the power dissipated at f_c through,

$$\frac{P_{k=1}}{P_{DC}} = \frac{\text{Re}\{Z_{eqk=1}\}}{R_L} \cdot \frac{1}{\sum_{k_{odd}}^{\infty} \frac{1}{k^2} \cdot \frac{Q_u(Q_L + k^2 Q_u) + 1}{k^2(Q_L + Q_u)^2 + (Q_L Q_u(k^2 - 1) - 1)^2}} \quad (2.56)$$

(a) Power dissipated in R_L at f_c 

(b) PA drain efficiency

Figure 2.14: Effect of Q_L and Q_u in the PA performance.

it can be stated that even for low values of Q_L and Q_u , at least 97% of the power is still dissipated at the fundamental frequency. This shows that even with more harmonic content in the load network, the vast majority of the power is still dissipated at f_c , which enhances the PA overall performance. This behavior can be observed in figure 2.15.

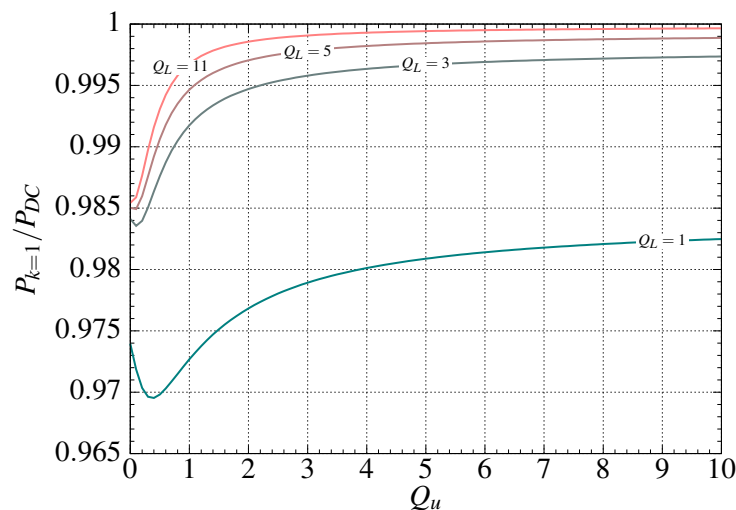


Figure 2.15: Ratio between the power at f_c and the total power delivered to the load.

2.5 Summary

This chapter explored the CMCD power amplifier architecture. In the first sections, some features of other SMPA architectures were present in a comparative approach with the class-D⁻¹ PA characteristics.

Like any other SMPA, the CMCD power amplifier ideally achieves 100% of efficiency, as long as the inherent losses in the RLC differential network are not considered, and also no overlapping of current and voltage is verified with ideal switches. However, real devices have parasitic components that degrade the PA performance. In fact, the on-chip inductor can be pointed out as the main responsible for the drop of efficiency. This is caused by its associated parasitic resistance (R_p). R_p also dissipates power and modifies the value of the load network at f_c from the desired R_L . The negative impact of R_p in the power amplifier performance, and a method to diminish its impact were presented.

Chapter 3

Simulations

In this chapter the results achieved by several simulations are presented. In the pre-layout section, the low Q_L factor approach is demonstrated. A comparison between a 90-nm and a 350-nm standard CMOS technology is made. A brief discussion about the way transistors are modeled in both technologies, and their breakdown region, is presented. Solutions to increase the output power of the CMCD PA are also discussed. Two methods for controlling the output power of the PA are demonstrated. Finally, from all the solutions previously presented, one is chosen to proceed to the layout stage for implementation.

The post-layout section shows the designed layout and the results obtained. A comparison between the results achieved with *Assura* parasitic extraction and with *Calibre* parasitic extraction is made. A post-layout re-tuning is performed in order to diminish the impact of the parasitic components generated with the layout extraction. The final results for the designed CMCD power amplifier are presented.

All simulations presented in this chapter were performed with *Cadence Design Systems Virtuoso/MMSIM* [34].

3.1 Pre-layout simulations

3.1.1 Lowering the Q_L factor

To validate the approach discussed in chapter 2, several simulations were performed. A 90-nm standard CMOS technology was chosen to implement the CMCD power amplifier circuit, which the basic architecture is shown again in figure 3.1.

Several technology on-chip inductors were selected to implement L_f , having different values of Q_u . These inductors were also chosen in order to have different loaded quality factors between them. Two different sets of simulations were then performed. In one of them, only the RLC network inductor was replaced with an on-chip technology inductor. In the other set of simulations, both RFCs were also replaced with a selected technology inductor. This way the impact of the

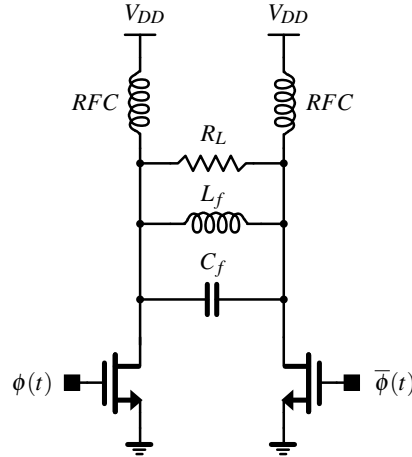


Figure 3.1: Circuit of the CMCD power amplifier.

RFCs in the PA performance can also be analyzed. The simulation results can be observed in figure 3.2.

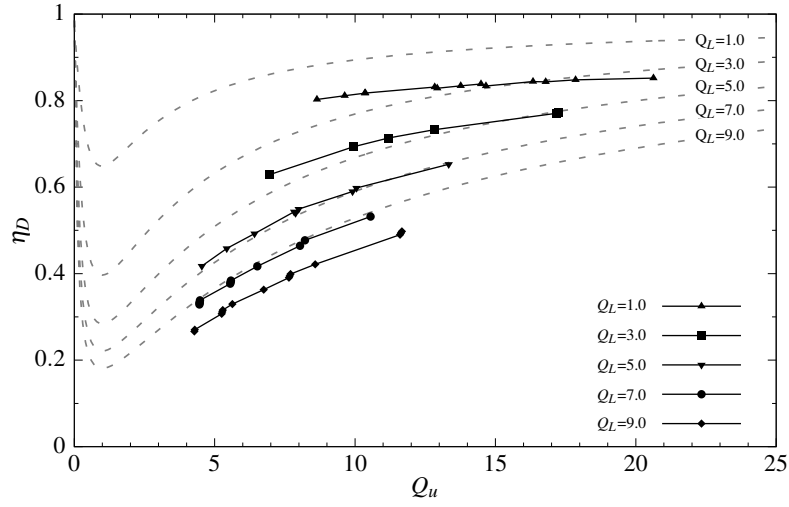
The dashed lines are the estimated efficiency of the PA, which were obtained with equation 2.54. The solid lines represent the values obtained for the several technology inductors, each one with a different Q_u , and for various values of Q_L . As can be seen, lowering Q_L is in fact beneficial and increases the power amplifier efficiency.

One can see that there is a 5-10% decrease in efficiency between the solid lines of figures 3.2(a) and 3.2(b). This shows the impact of having on-chip chokes on the amplifier performance. The lower drain efficiency is caused by the energy dissipation on the parasitic resistance of the on-chip RFCs. Also the transistors peak drain voltage decreases, which lowers the PA output power at the fundamental frequency. Since the theoretical analysis (dashed lines) does not take into account power losses other than the non-ideal on-chip inductor, there is a noticeable offset in the value of the simulated results. Apart from this offset, which is due to the intrinsic on-resistance, r_{on} , of the transistors, one can observe similar curves behavior in both plots.

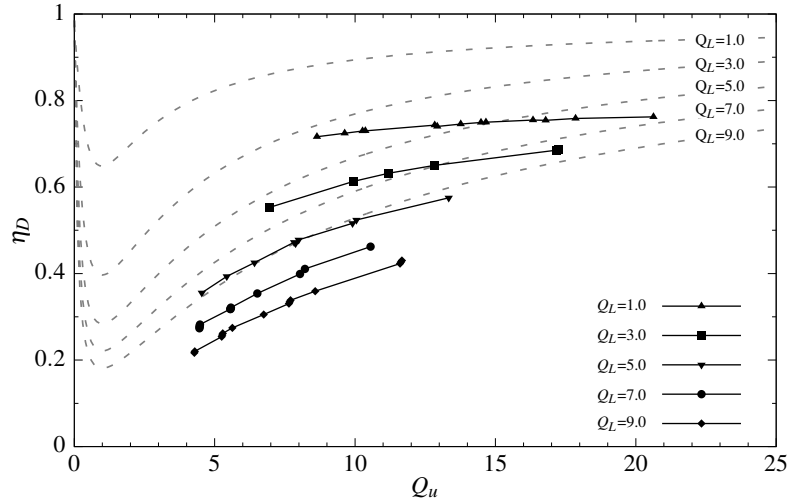
A maximum efficiency of approximately 76%, with a transmit power of 16-dBm, was achieved with all on-chip inductors. This high performance was achieved by increasing the RLC network inductor size and lowering C_f by the same factor, thus maintaining the RLC parallel filter tuned at f_c . Therefore, it results in a smaller quality factor Q_L , which increases the PA drain efficiency.

3.1.2 Impact of the transistors size

The offset between the theoretical analysis and the simulation results perceived in figure 3.2(b), shows the influence that the energy dissipated at the transistors have on the PA overall performance. To reduce r_{on} , diminishing this way the energy dissipation, it is necessary to increase the transistors size. On the other hand, increasing a transistor size also increases its driving requirements.



(a) Simulation with ideal chokes and load on-chip inductor.



(b) Simulation with technology models of all on-chip inductors.

Figure 3.2: Simulation waveforms for drain-efficiency with the technology models of on-chip inductors (solid lines) and the estimated efficiency from the theoretical analysis (dashed lines).

To further analyze the impact of the transistors dimension in our CMCD power amplifier, another set of simulations were performed. The transistors width was increased from 15 to 960- μm . All the other components were maintained on-chip. Their parameters were the same used to achieve the 76% of η_D and 16-dBm of output power previously reported. The simulation results are shown in figure 3.3.

As can be seen, reducing r_{on} by increasing the transistors width can effectively increase the power output and the PA drain efficiency. One can also notice that above 720- μm , the efficiency remains almost the same. This means that r_{on} is already too small, and other parasitic components present in the circuit take over the efficiency losses.

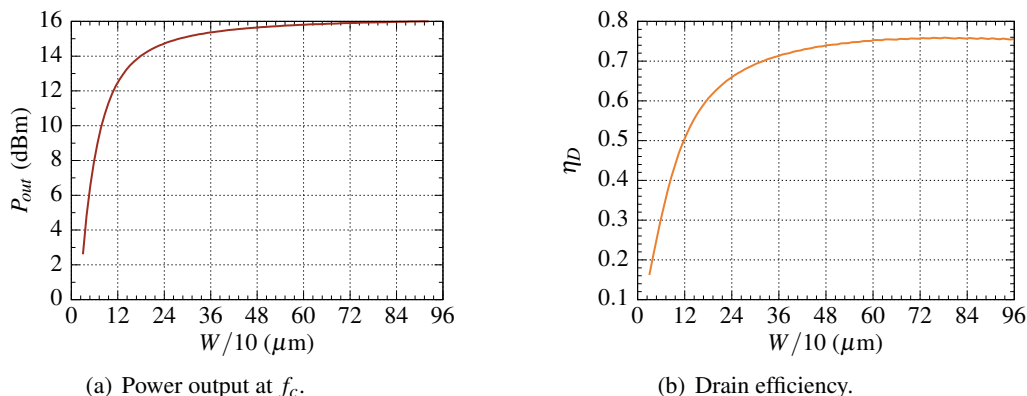


Figure 3.3: Impact of the transistors size on the drain efficiency and power output of the PA.

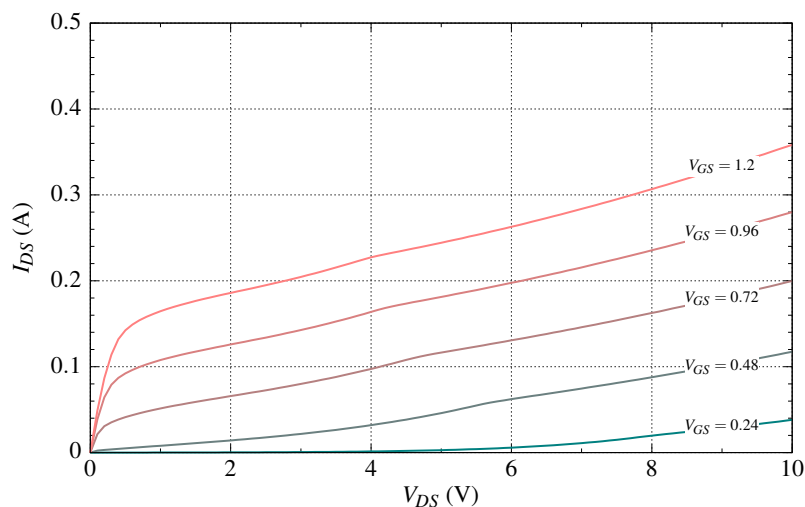
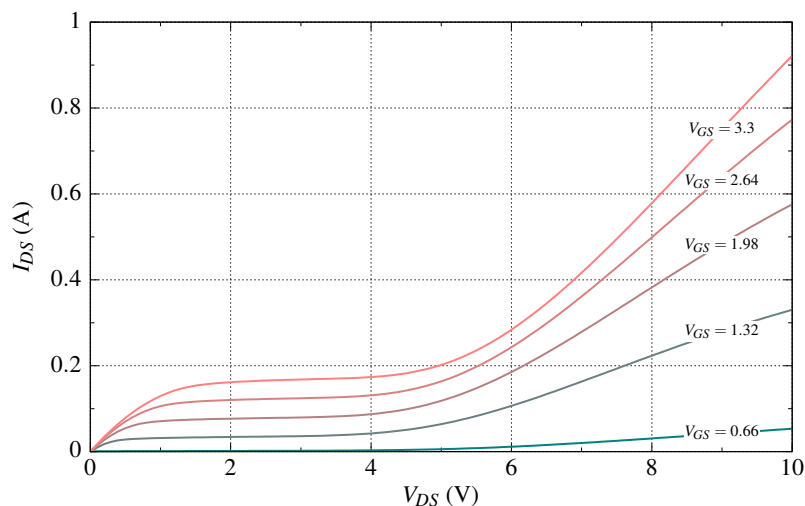
3.1.3 90-nm versus 350-nm

A 350-nm CMOS standard technology was also taken under consideration to implement our CMCD power amplifier. The low unloaded quality factor of the technology inductors was a major drawback to implement the PA. For 16-dBm of output power, the 350-nm process has 33.5% of drain efficiency against the 76% of the 90-nm process. This somehow demonstrates the impact that the on-chip inductors have on the PA performance.

3.1.3.1 Impact of varying V_{DD}

With both CMOS technologies the power amplifier did not achieve the 20-dBm to work as a class 1 *Bluetooth* compliant device. One method to boost the output power of the PA is to increase the V_{DD} value. Raising the supply voltage in order to achieve higher output power must be done carefully. This is due to the low breakdown voltage of the CMOS devices, namely the transistors. We already know that in each branch of the class- D^{-1} PA circuit (figure 3.1) the peak drain voltage of the transistors is πV_{DD} . Therefore, it is necessary to ensure that the peak drain voltage does not exceed the transistors breakdown voltage, V_{break} . To find out what is the value of V_{break} , it is necessary to analyze the transistor $I-V$ characteristic. The $I-V$ characteristic curves, for the 90-nm and 350-nm CMOS technologies, are depicted in figure 3.4.

Analyzing figure 3.4(a), we can see that the transistor model of the 90-nm process is not correctly characterized above the typical MOS saturation region. On the other hand, in figure 3.4(b) we can see that the 350-nm process model resembles the typical breakdown behavior when high-voltage values are applied both for the drain and gate terminals. Indeed, a little *bump* is noticeable in the $I-V$ characteristic curves of the 90-nm process, between 4 and 6-V for the V_{DS} . For voltages above this *bump*, the $I-V$ behavior seems to be modeled as the saturation region, thus erroneously extrapolating the breakdown of the transistor. One can also note that due to the mentioned *bump*, the derivative of the current related to the drain voltage is negative. This is somehow strange for the typical characteristics found in MOS devices, although it can really occur but due to thermal

(a) 90-nm I - V characteristic.(b) 350-nm I - V characteristic.Figure 3.4: NMOS-RF transistor I - V characteristics.

issues. We can then say that to ensure a reliable operation from the transistor models in both technologies, values above 4.5-V of V_{DS} are not trustworthy. Therefore, the maximum supply voltage for the 90-nm and 350-nm CMOS technologies is set to 1.4-1.5 Volt.

Since the CMCD is a SMPA with ZVS, the main reliability issue for the transistors is the oxide breakdown due to the large difference between the V_{DS} and V_{GS} . The hot carrier effect¹ only happens when a large drain current coexists with a large drain voltage [2]. The ZVS characteristic guarantees that there is no overlapping between current and voltage. Even if there is an overlap, due to non-ideal behavior, the values of the current and drain voltages are not large enough to cause hot carrier phenomena.

¹The hot carriers, electrons in MOS technologies, crash into the gate oxide. In a long term, this behavior causes the oxide between the gate and the drain to be destroyed. When this happens the transistor is ruined.

Figure 3.5 shows the output power and η_D for the 90-nm and 350-nm CMOS technologies, for several supply voltage values. As expected, the drain efficiency is not sensible to V_{DD} variations. On the other hand, the output power increases significantly when the supply voltage is raised. However the peak drain voltage in the transistors also increases, which can lower their long-term lifetime operation. Thus, this increase of V_{DD} must be done carefully.

When comparing with the 350-nm process, the 90-nm technology can achieve a higher output power and still maintain good drain efficiency (figure 3.5). This proves that the 90-nm process is better suited for the implementation of our CMCD PA.

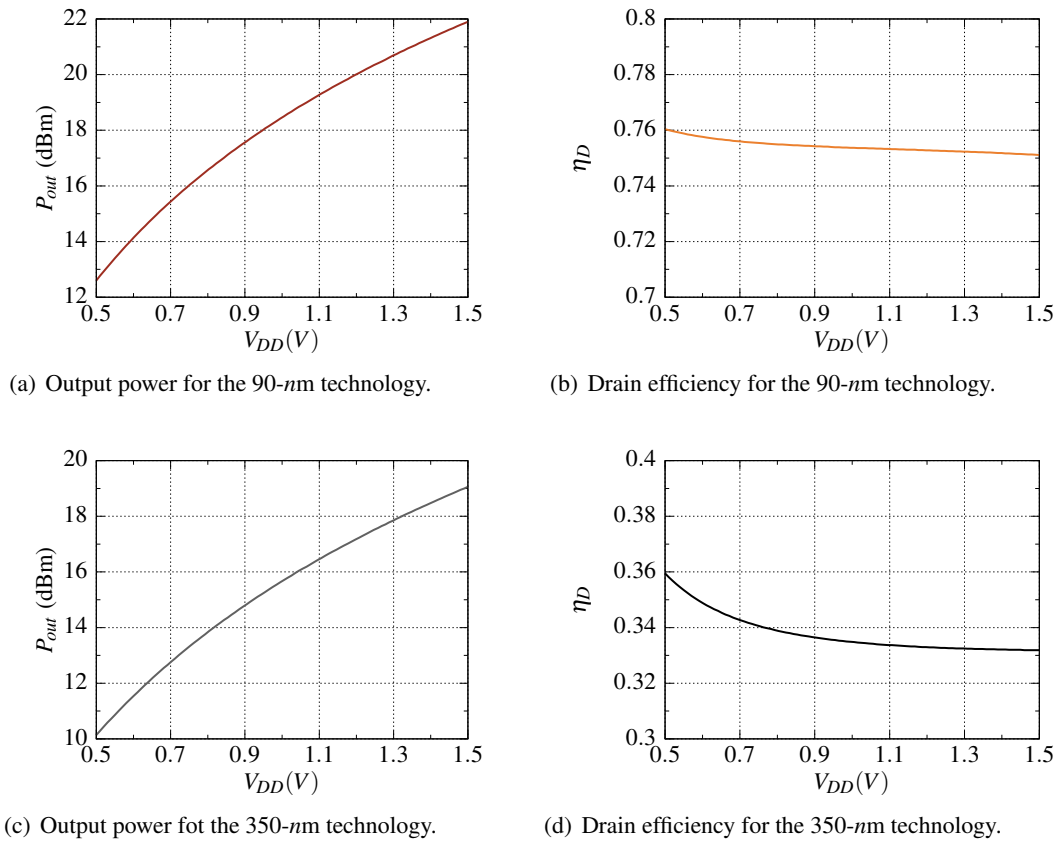


Figure 3.5: Output power and drain efficiency for the 90-nm and 350-nm processes, varying the supply voltage.

3.1.4 CMCD PA cascode configuration

Another way to increase the output power of our PA is to utilize a cascode configuration like the one depicted on figure 3.6. With this configuration it is possible to further increase the supply voltage beyond the 1.4-1.5 Volt previously referred, achieving this way a higher output power. The 4.5-V limit of V_{DS} drop across a transistor is now split between the two devices of the cascode pair in each branch. This enables us to raise V_{DD} up to a theoretical value of 2.8-3 Volt, in order to have the same V_{DS} drop across the two transistors.

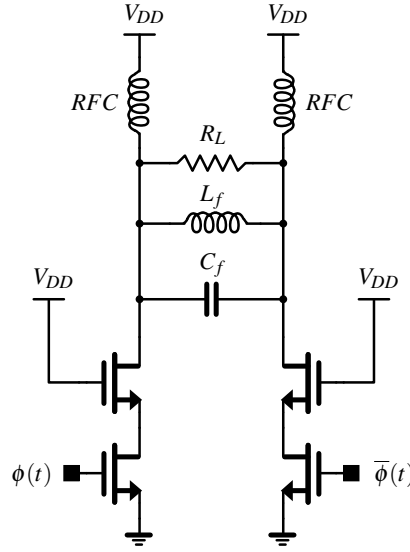
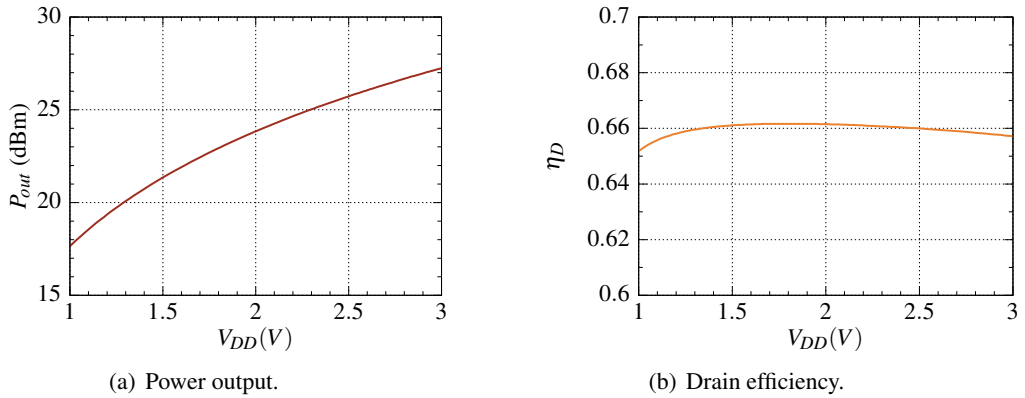


Figure 3.6: Cascode configuration of the CMCD power amplifier.

Figure 3.7 shows the simulation results for several values of V_{DD} . With 3-V of supply voltage, the power amplifier achieved an output power above 27-dBm. Analyzing figures 3.5(b) and 3.7(b), one can notice that the drain efficiency is lower with the cascode configuration. Since there are two transistors at each branch, there are also two on-resistances r_{on} . This means that more energy is dissipated at each RF-cycle, hence the η_D lowers. This is a good trade-off between the two FOM, because the output power increases more significantly than the existing drop in efficiency.

Figure 3.7: CMCD PA cascode configuration P_{out} and η_D for several values of V_{DD} .

3.1.5 Power control

A simple way to control the power output of the CMCD power amplifier is presented in figure 3.8. As can be seen, in both branches of the power amplifier circuit all the transistors are in parallel with each other, and each one is controlled by a different input. To correctly control the

output power, each input must be activated with its dual 180 degrees out-of-phase version, *e.g.* $\phi(t)_1$ with $\bar{\phi}(t)_1$. The output power increase happen when multiple inputs are activated.

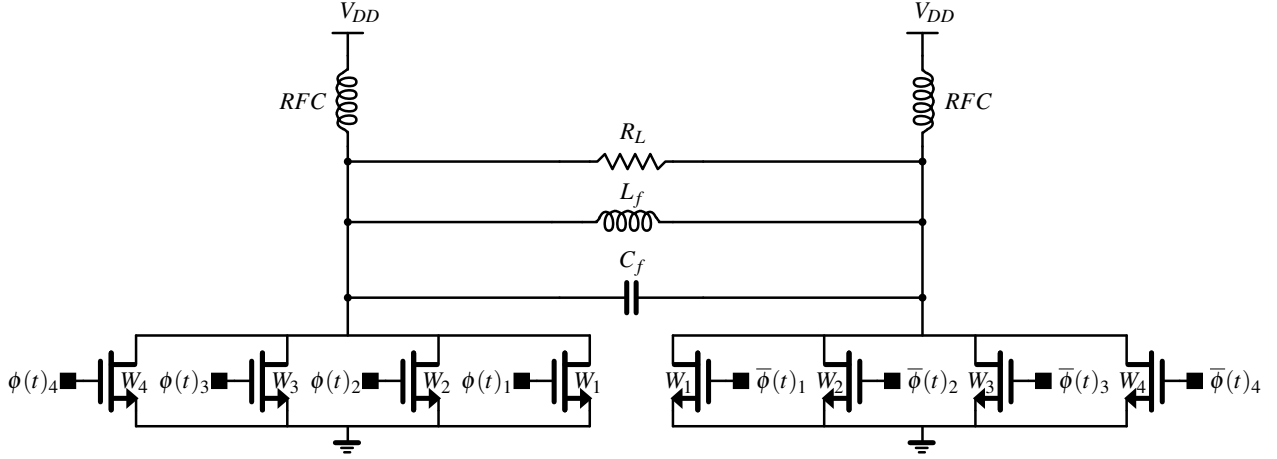


Figure 3.8: Power control configuration of the CMCD power amplifier.

One can notice that the transistors represented in figure 3.8 have different sizes². This increases the difference between the different power levels produced by the amplifier, but lowers the average drain efficiency. Table 3.1 shows the results obtained with the circuit configuration depicted in figure 3.8.

Table 3.1: Power output and drain efficiency with power control.

ϕ - $\bar{\phi}$ activated	P_{out} (dBm)	η_D %
1	5.1	22.1
1,2	12.4	50.8
1,2,3	14.9	67.7
1,2,3,4	15.8	75

The power output ranges from 5.1-dBm up to 15.8-dBm, while the η_D lowest value is 22.1% and its maximum is 75%. An average output power and drain efficiency could be estimated according to the probability density function of the several inputs. Other input combinations different than the ones already reported in table 3.1 are also possible, *e.g.* $\phi(t)_1$ - $\bar{\phi}(t)_1$ with $\phi(t)_4$ - $\bar{\phi}(t)_4$, resulting in extra power output levels and drain efficiencies.

3.1.5.1 Power control with cascode configuration

Figure 3.9 depicts another possible configuration to control the output power of a CMCD PA. As already referred, with a cascode configuration it is possible to increase the maximum output power of the PA at the cost of a lower drain efficiency. In table 3.2(a) are presented the results

² $W_1 = 40\mu m$, $W_2 = 80\mu m$, $W_3 = 160\mu m$, $W_4 = 320\mu m$

obtained when the transistors width W_1 , W_2 and W_3 are different³. On the other hand, table 3.2(b) shows the achieved results when the value of W_1 , W_2 and W_3 are the same.

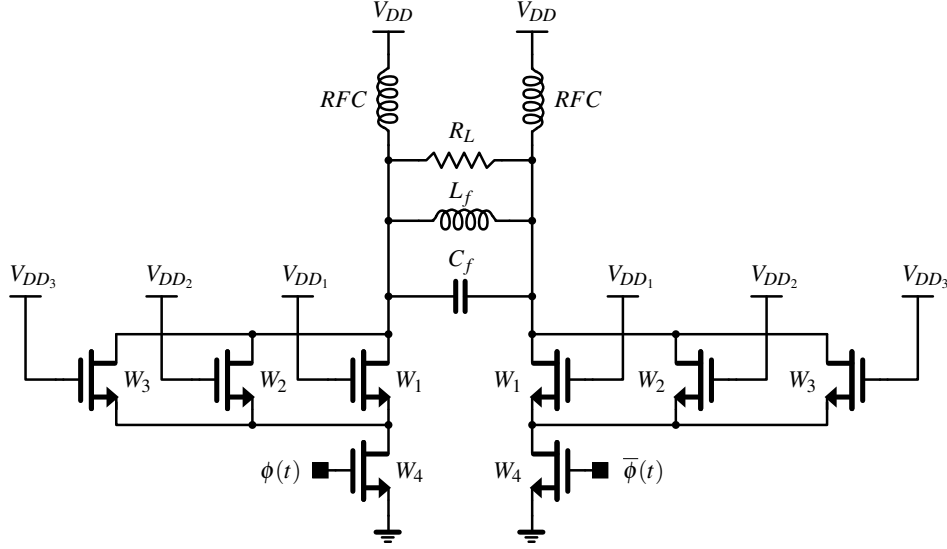


Figure 3.9: Cascode power control configuration of the CMCD power amplifier.

Analyzing tables 3.2(a) and 3.2(b) we can see that in fact having different widths for W_1 , W_2 and W_3 increases the range of the output power for our PA. However, when all the widths are the same a higher average drain efficiency is obtained, mainly due to the reduction of r_{on} . Like the previously presented power output control solution (figure 3.8), other input combinations different than the ones already reported are also possible, e. g. V_{DD1} with V_{DD3} or V_{DD2} with V_{DD3} ⁴. Hence, these different combinations result in extra output power levels and drain efficiencies.

Table 3.2: Power output and drain efficiency with cascode power control.

(a) Transistors with different sizes.			(b) All transistors with the same size.		
V_{DD} activated	P_{out} (dBm)	η_D %	V_{DD} activated	P_{out} (dBm)	η_D %
1	14.31	28.2	1	20.25	59.3
1,2	20.1	59.5	1,2	21.09	64.7
1,2,3	21.2	67.4	1,2,3	21.35	66.1

3.1.6 PA re-tuning

The next step in our project is to select a solution from all the previously presented, to then perform the layout. It is desired that the selected configuration achieves the desired *Bluetooth* protocol output power with good drain efficiency. The necessary silicon area to implement the selected design must be taken under consideration too, since it is what defines the cost of our PA

³ $W_1 = 80\mu m$, $W_2 = 160\mu m$, $W_3 = 320\mu m$

⁴ Note that V_{DD1} , V_{DD2} and V_{DD3} are equal to V_{DD} when activated and zero otherwise.

CMOS implementation. After the circuit is chosen, it is necessary to perform a re-tuning of the RLC parallel filter. Since the transistors C_{DS} parasitic capacitances are part of the RLC network, the filter capacitor size should be adjusted increasing this way the overall performance of our PA.

The cascode topology seems like the right choice because with it a higher output power can be achieved. This way it is possible to easily attain the 20-dBm of output power that defines a *Bluetooth* class-1 device. The higher output power compensates the drain efficiency drop due to the r_{on} of each transistor, so the trade-off between this two important FOM favours the cascode implementation.

Figure 3.10 shows the results of the performed simulation, helping with the PA RLC parallel filter tuning. As can be seen, the peak drain efficiency occurs when the C_f value is between 950-fF and 1-pF. On the other hand, P_{out} value decreases for the successive intervals of C_f values. Choosing 995-fF for C_f , results in 66.18% of η_D and 21.38-dBm of output power. The simulation was performed using 1.5-V supply voltage.

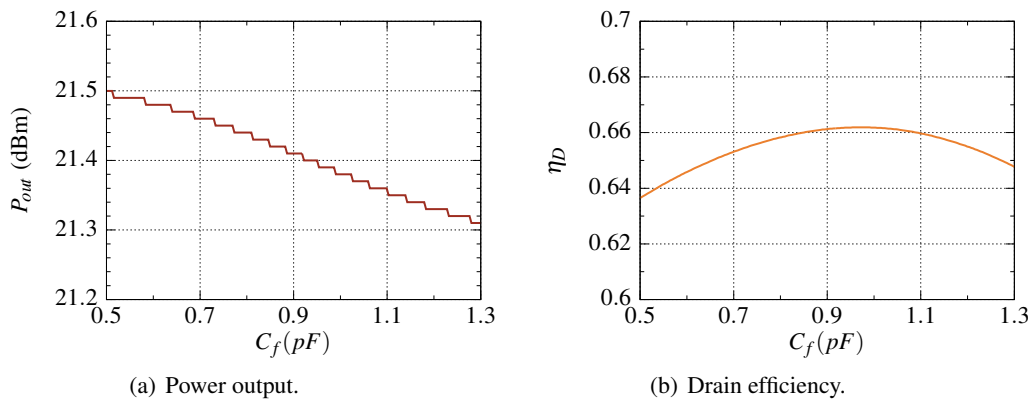


Figure 3.10: P_{out} and η_D obtained for several values of C_f .

3.2 Power amplifier layout

A design contest for our selected 90-nm CMOS technology is being held this year. Among the submitted designs, two will be chosen and submitted free of charge on the next run. The rule is simple, the design must have a maximum die area of $1875 \times 1875 \text{-}\mu\text{m}^2$. In order to participate in this contest, our PA was designed with this area as our boundary. In figure 3.11 it is depicted the designed layout of our PA. A bigger representation of the PA layout is shown in appendix A.

As can be seen, the $1875 \times 1875 \text{-}\mu\text{m}^2$ area is more than enough. In fact the area occupied by the PA is only $1330 \times 975 \text{-}\mu\text{m}^2$, *i.e.* 37% of the total area. This number goes up to 40%-45% including the input/output pads. The rest of the die is filled with metal-1, which provides shielding to isolate empty die area from external noise and between the designed devices.

The design rules for this 90-nm technology only allow metal tracks with $12\text{-}\mu\text{m}$ of maximum width. To obey the electro-migration recommendations, one can see that several metal tracks are

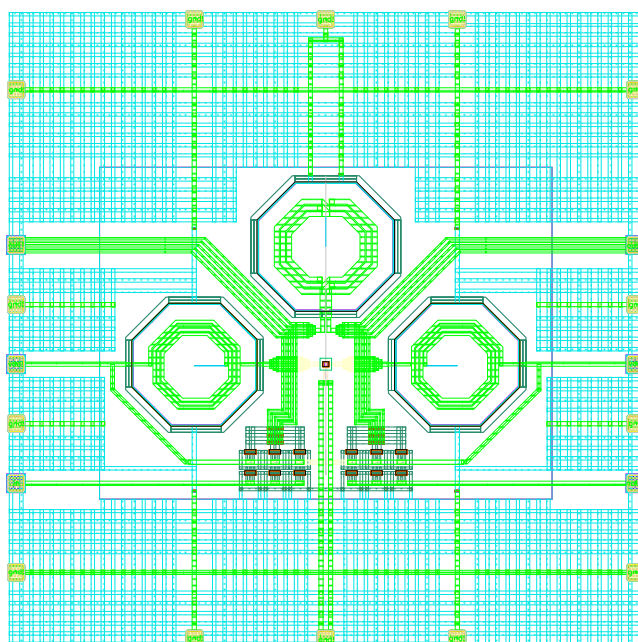


Figure 3.11: CMCD power amplifier layout ($1875 \times 1875\text{-}\mu\text{m}^2$).

designed in parallel and connect together. This increases the maximum current that can safely flow through the metal tracks, and at the same time is compliant with the technology design rules. All the inputs and outputs are designed with metal-9, which has lower impedance and is more thick than all the other metal levels. The metal track only descends to a lower level metal when necessary. One can also notice that there is also a guard-ring surrounding the PA devices, which further increases the protection against noise sources helping this way to enhance the amplifier performance.

The layout is composed by twelve transistors, each one with $320\text{-}\mu\text{m}$ of width. Since the transistors of the same level are connected in parallel with the others, this results in an equivalent width of $960\text{-}\mu\text{m}$ for each level of each branch of the cascode configuration. The RFCs have an inductance of 5-nH with an unloaded quality factor of 14.35. The parallel filter differential inductor has a Q_u of 20.6 with an inductance of 3.23-nH . Metal-9 is the top layer metal of all three inductors. As already referred, C_f has a capacitance value of 995-fF .

3.2.1 Post-layout Simulations

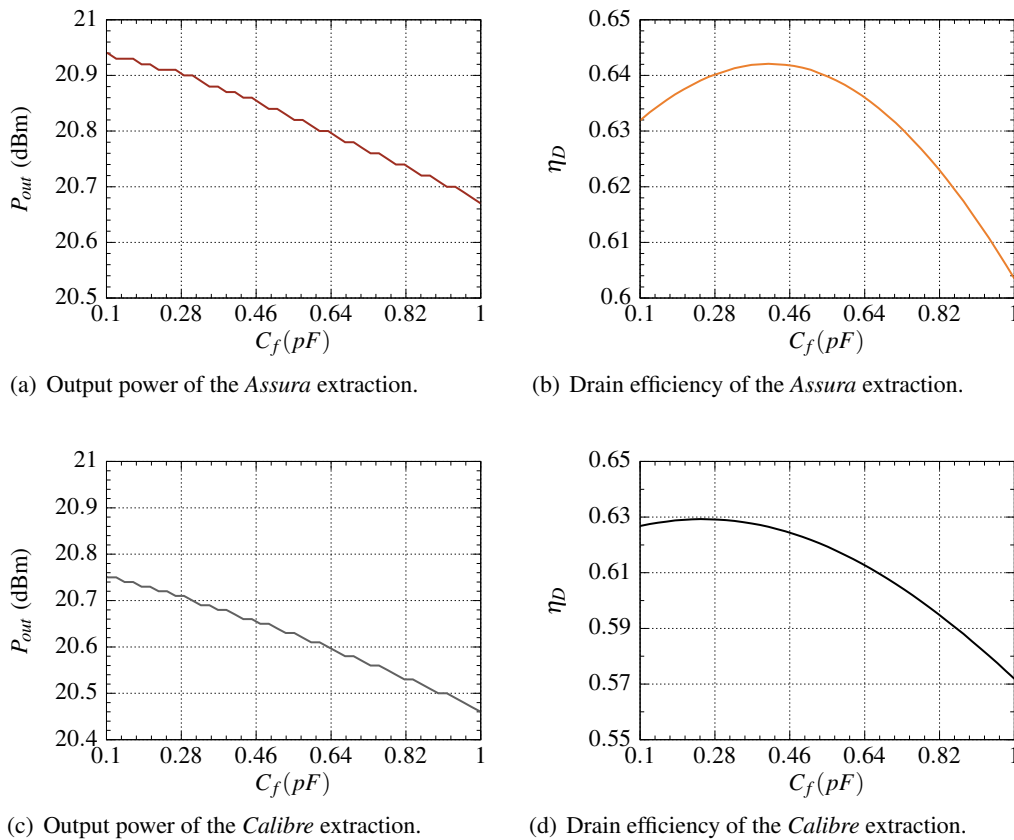
Throughout the whole layout design process, the design rule check (DRC) was performed with the *Mentor Graphics Calibre* [35] software tool. For the layout versus schematic (LVS) verification, *Cadence Design Systems Assura* [36] software tool and also *Calibre* were used. The parasitic extraction was also performed with both tools from the two different vendors, which produced two different layout parasitic extractions. Table 3.3 shows the results obtained with the two different extractions, and compare them with the ideal case.

Table 3.3: Post-layout simulation results.

	<i>Assura</i>	<i>Calibre</i>	Ideal
η_D (%)	59.51	55.55	66.18
P_{out} (dBm)	20.64	20.37	21.38

The results obtained with both *Assura* and *Calibre* extractions are significantly different from the ideal case. The parasitic capacitances and resistances formed during the layout design process are responsible for the decrease in the PA performance. Although the parasitic capacitances normally have small values, when in great number they can seriously untune the RLC parallel filter from the desired frequency. This causes efficiency and power loss in the power amplifier.

To minimize the impact of the parasitic components, a post-layout re-tuning was performed to find a value of C_f that compensates the generated parasitic capacitances. Despite the fact that the layout was already designed, and since the C_f re-tuned value should be smaller than the initially calculated, fitting a new C_f into the design was not an issue. A modified version of the layout, *i.e.* without C_f , was extracted with both *Assura* and *Calibre* software. A set of simulations were performed with the two different extractions, with an ideal capacitor C_f for several capacitance values. The results obtained can be examined in figure 3.12.

Figure 3.12: P_{out} and η_D of *Assura* and *Calibre* extractions, for several values of C_f .

As can be seen, the maximum drain efficiency occurs in very different values of C_f for the two different extractions (figures 3.12(b) and 3.12(d)). With the *Assura* extraction, the ideal RLC filter capacitance value is 410-fF. On the other hand, with the *Calibre* extraction the ideal C_f capacitance value is 250-fF. Both values are significantly different from the initial 995-fF RLC network capacitance value. This shows the impact that the parasitic capacities, generated during the layout stage, have on the overall performance of the PA. Two layouts were then designed with different C_f capacitance values. One with 410-fF and the parasitic extraction was made with *Assura* and the other one with 250-fF and extracted with *Calibre*. The results obtained with the two different parasitic extractions are shown in table 3.4.

Table 3.4: Post-layout simulation results with re-tuning.

	<i>Assura</i>	<i>Calibre</i>	Ideal
η_D (%)	64.06	62.81	66.18
P_{out} (dBm)	20.85	20.7	21.38

With the post-layout re-tuning the results achieved are more similar to the values calculated in the ideal case (table 3.4). The remaining difference between the ideal and the extracted simulations is due to the inherent parasitic resistances formed during the layout design stage. These resistances dissipate energy, which lowers the PA efficiency and output power at central frequency. Since the *Calibre* software tool is more commonly used in industry than *Assura*, the results provided with its parasitic extraction are in principle more trustworthy. Nevertheless, the results obtained with *Assura* give us some insurance that the real value of the η_D and P_{out} are somewhere in between the results of the two parasitic extractions. The CMCD PA layout depicted in figures 3.11 and in the appendix A are already the final *Calibre* layout version, that is with the 90-nm technology 250-fF capacitance value for C_f .

In figure 3.13, simulation results for several values of V_{DD} using the *Calibre* parasitic extraction circuit are shown. As expected, the drain efficiency is almost unaffected, changing from nearly 61% up to approximately 63%. However, the power amplifier output power at f_c varies from 16-dBm up to a stunning value near 27-dBm.

3.3 Summary

This chapter started by presenting simulation results that corroborate the low Q_L approach discussed in chapter 2. The impact of the transistors width in lowering r_{on} and increasing the η_D was also shown. The difference between the 90-nm and 350-nm selected technologies was presented, and the 90-nm proved to be better suited for silicon implementation.

The CMCD cascode configuration proved to be a good choice to increase the output power of the PA, compromising only a little the amplifier drain efficiency. With the cascode configuration it is possible to raise the supply voltage beyond the values possible with the normal CMCD configuration.

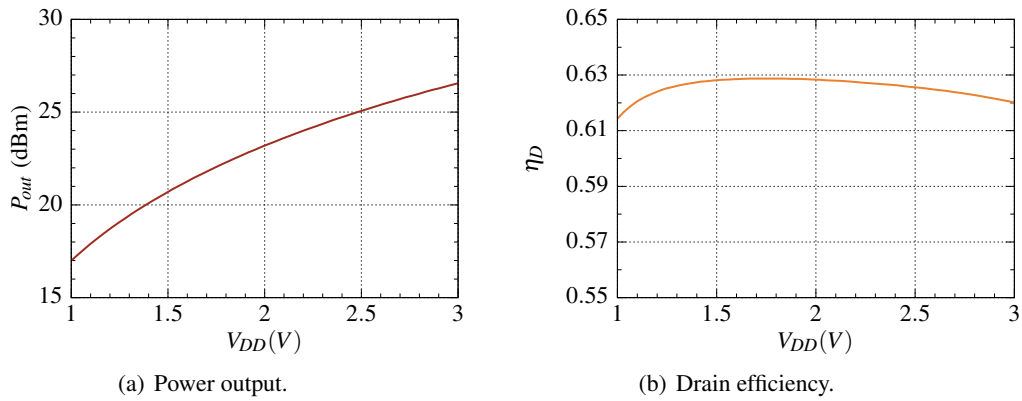


Figure 3.13: P_{out} and η_D obtained with *Calibre* parasitic extraction for several values of V_{DD} .

A post-layout re-tuning of the RLC network capacitance is made, proving to be a good method to achieve better results when the die area of the chip is not an issue. *Assura* and *Calibre* parasitic extraction simulation results were also compared.

The designed CMCD power amplifier layout achieves 62.83% of η_D with 20.85-dBm of output power with 1.5-V of supply voltage, and a maximum P_{out} of 26.6-dBm with 62% of drain efficiency when V_{DD} is 3-V.

Chapter 4

Conclusion

4.1 Achievements

The objective of this dissertation was to implement a CMOS-RF PA. The goal was accomplished with an amplifier class which did not have any known reported CMOS implementations, the current-mode class-D amplifier. Before selecting the CMCD amplifier, several classes of amplifiers were analyzed, from both linear and non-linear classes of amplification. The linear class amplifiers can amplify non constant envelope signals however, they typically have a low drain efficiency¹. The non-linear class amplifiers, also known as SMPA, are a good solution to amplify constant envelope signals (like with *Bluetooth* early versions) since they have 100% of theoretical drain efficiency. From the non-linear class amplifiers group, the CMCD amplifier was the chosen, because it is a ZVS amplifier but with a lower peak drain voltage than other ZVS amplifiers, as the class-E. Since CMOS devices have a low breakdown voltage, having a lower peak drain voltage is an important feature. The ZVS characteristic enables the CMCD to work at higher frequencies ideally without energy losses at each RF cycle, in opposition to its dual counterpart, the VMCD. The CMCD amplifier also exhibits the highest utilization factor of all the analyzed amplifiers. All these characteristics makes the current-mode class-D power amplifier a good choice for implementation in a CMOS technology.

Besides the ideal behavior analysis of the amplifier, a non-ideal study was also performed where the impact of the RLC network Q_L is taken under consideration. The influence of the unloaded quality factor of the differential inductor was also performed. In this analysis it is demonstrated that lowering Q_L by increasing the RLC filter inductance value, and diminishing its capacitance by the same factor, while having a high Q_u , greatly improves the power amplifier performance.

¹Class-C amplifiers can achieve 100% of theoretical drain efficiency, but to do so they need infinite drive power and the U_f of the transistor drops toward zero.

A set of simulations, to corroborate the low Q_L approach, were performed. A maximum drain efficiency of nearly 76% with 16-dBm of output power was achieved. The impact of the transistors size and of the supply voltage was also studied. When the width of the transistors is increased their r_{on} diminishes, which increases the drain efficiency. If an higher output power is needed, raising the supply voltage is a good solution but at the cost of an higher stress drain voltage. Since the peak drain voltage of an CMCD PA is πV_{DD} , it was necessary to verify the maximum V_{DD} allowable by the technology. Several NMOS-RF I - V characteristic curves were traced in a 90-nm and in a 350-nm CMOS technology. With these analyzes it was possible to find out the maximum V_{DS} value before the breakdown occurs. This V_{DS} value provided us the maximum supply voltage that can be applied to the PA circuit. The low performances achieved by the 350-nm process dictated our choice, selecting the 90-nm process to implement the PA. Furthermore, with the 350-nm process a maximum η_D of 33.5% was obtained against the 76% of the 90-nm process.

To further increase the output power of the CMCD power amplifier, in order to easily achieve the 20-dBm that class-1 *Bluetooth* standard demands, a cascode configuration was introduced. Since an higher supply voltage can be applied, also an higher output power can be achieved. This happens at the cost of a smaller drain efficiency. With a cascode configuration there are more transistors in the circuit, thus more on-resistances. Since the on-resistances dissipate energy, they lead to a lower η_D . Methods to control the output power were also presented.

The CMCD cascode PA layout was implemented using the selected 90-nm CMOS technology. The layout was drawn in a die area of $1875 \times 1875 \mu m^2$. A post-layout re-tuning of the RLC network was necessary to compensate the generated parasitic components during the layout stage. The post-layout simulations, with *Assura* and *Calibre* parasitic extractions, achieved a η_D of 64.06% and 62.81% respectively. As for the output power, the *Assura* extraction managed to achieved 20.85-dBm against the 20.7-dBm of the *Calibre* parasitic extraction. Using *Calibre* parasitic extraction, and varying the V_{DD} supply voltage, a maximum P_{out} of near the 27-dBm, with 59.37% of η_D , was achieved.

4.2 Future work

Like any other work, some improvements and other tests should be made in the future. This power amplifier is at the point were it can be sent to fabrication. This is an important future work that needs to be done, in order to corroborate with real measurements the simulations and analysis performed throughout this work.

The *Bluetooth* ACP test is a measurement that could not be performed within the time frame of this dissertation. Knowing that this is an important power amplifier evaluation testing procedure, it should be implemented in a near future. This test should be made both at simulation level and with the fabricated chip.

A polar transmitter modulates a signal by modulating the supply voltage of the power amplifier. This way non-constant envelope signals can be transmitted using non-linear power amplifiers.

Transforming the CMCD power amplifier into a polar transmitter seems a challenging task, and an excellent opportunity for future research.

Appendix A

Power Amplifier Layout

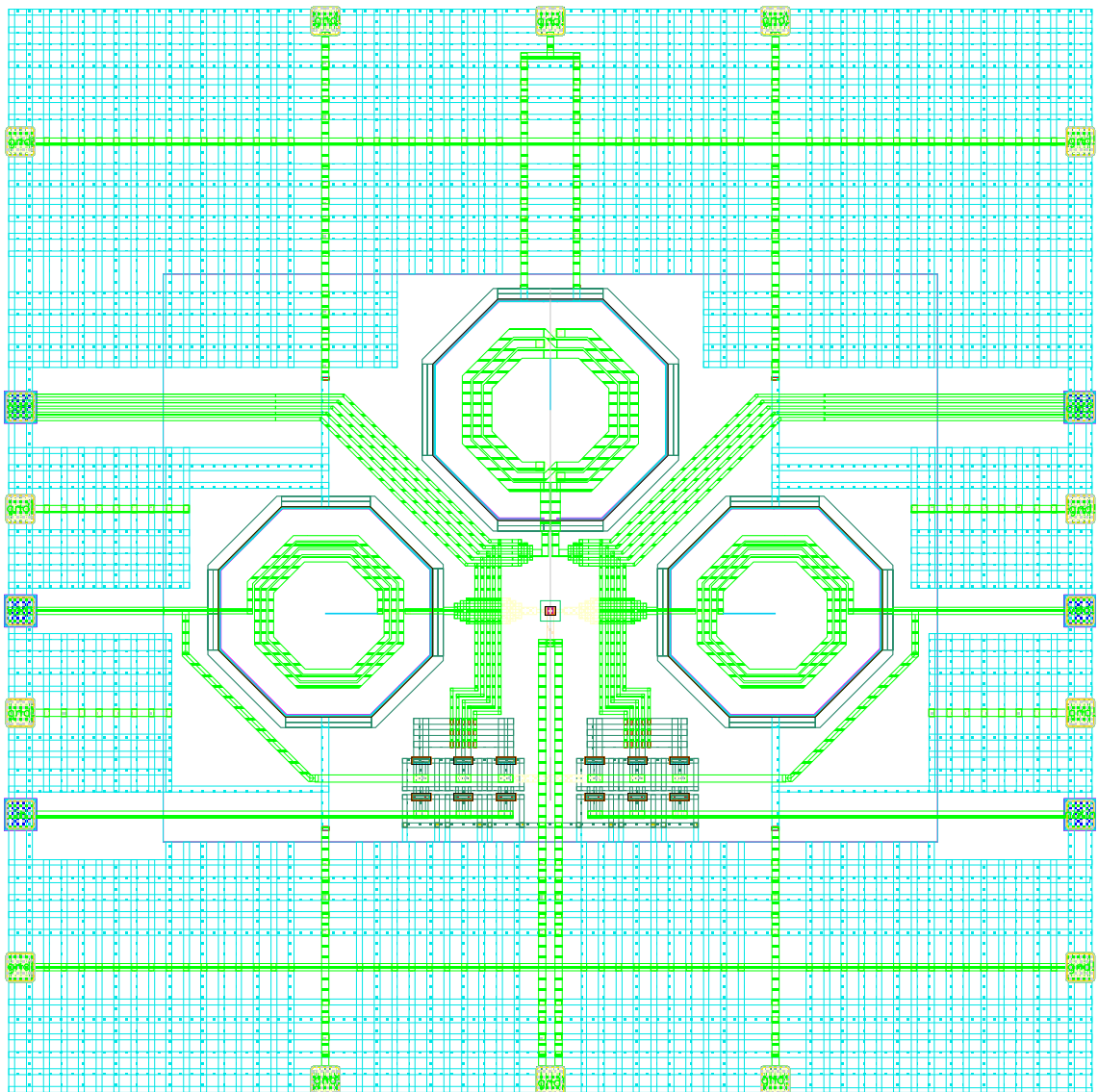


Figure A.1: CMCD power amplifier layout ($1875 \times 1875 \mu\text{m}^2$).

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