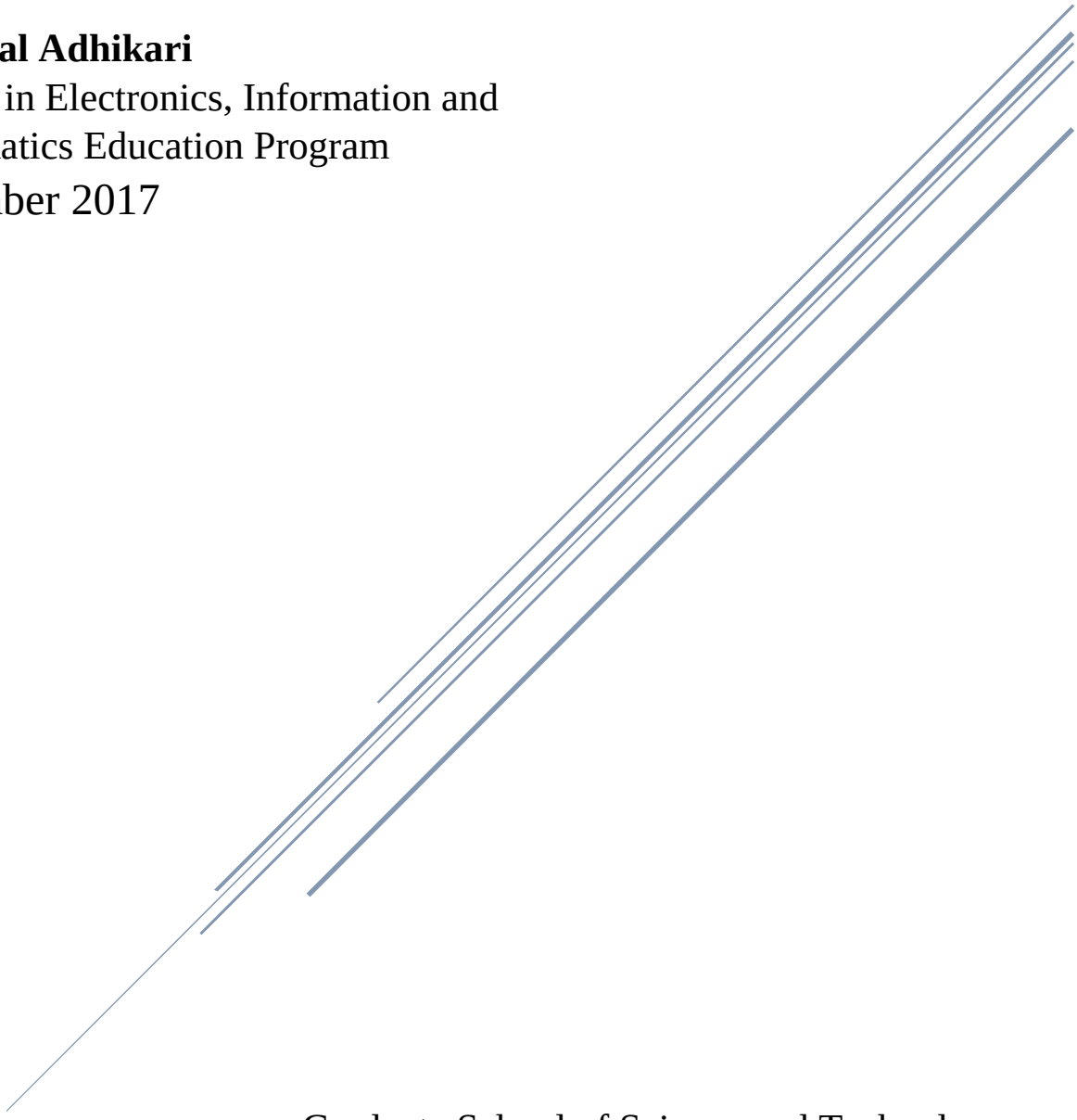
DESIGN OF GRAY CODE INPUT DAC FOR GLITCH REDUCTION IN COMPARISON WITH R-2R LADDER DAC

By Gopal Adhikari
Masters in Electronics, Information and Mathematics Education Program
September 2017



Graduate School of Science and Technology
Gunma University

Design of Gray Code Input DAC for Glitch Reduction in Comparison with R-2R Ladder DAC

A Dissertation Submitted to the
Graduate School of Science and Technology
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As a Fulfillment of Thesis Requirement
for the Master′s in Electronics, Information and Mathematics
Education Program

By

Gopal Adhikari
Gunma University
Department of Science and Technology
2017

Declaration

I hereby declare that the thesis entitled "**Design of Gray Code Input DAC for Glitch Reduction in Comparison with R-2R Ladder DAC**" has been carried out in Gunma University, Faculty of Science and Technology, Division of Electronics and Informatics, Kobayashi Laboratory. The work is original and has not been submitted in part or full by me for any degree or diploma at any other University. I further declare that the material obtained from other sources has been duly acknowledged in the thesis.

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Certificate

It is certified that the work reported in this thesis entitled "**Design of Gray Code Input DAC for Glitch Reduction in Comparison with R-2R Ladder DAC**" by Gopal Adhikari, has been carried out under my supervision and is not submitted elsewhere for a degree.

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Approval

This is to certify that the thesis entitled "**Design of Gray Code Input DAC for Glitch Reduction in Comparison with R-2R Ladder DAC**" written by Gopal Adhikari has been approved by the thesis advisor, and further approved by the Board of Examiners as one of the requirements for the completion of Master′s in Electronics, Information and Mathematics Education Program, Gunma University. This dissertation complies with the regulation of the University and meets the accepted requirements with respect to originality.

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"Occasionally in life there are those moments of unutterable fulfilment which cannot be completely explained by those symbols called words. Their meanings can only be articulated by the inaudible language of the heart. "

-Martin Luther King, Jr.

When this thesis has been completed, many individuals have contributed to this work towards its success. Although the space allocated to acknowledge the help and suggestions from supervisors and colleagues is only about a small part of the entire thesis, the impact of their work has been much larger.

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Gunma University, 2017 Gopal Adhikari

Abstract

This dissertation deals with a technique to reduce glitches in digital-to-analog converters. It is well known that frequently used R-2R ladder DACs are prone to glitches. R-2R DACs use binary code as their input. Binary code DACs trigger multiple switches at one time for 1-LSB change. This is the reason for occurrence of glitch. Although, a reconstruction analog filter usually follows DAC, it comes with a disadvantage of taking larger chip area in an IC, and/or it requires more components and hence increases the cost. In addition, complete elimination of glitches is very difficult. So, techniques to reduce glitches should be implemented especially for the high-speed DAC. Here, we purpose a DAC which does not require extra space in IC, the number of components as well as the cost of implementation is reduced along with eliminating the glitches (within a simple circuit) that are thought to occur

One candidate as glitch reduction technique is using Gray code [1], which uses only one switch transition at one time for 1-LSB change. However, it has been considered that Gray code input DAC is difficult to realize efficiently and systematically. In fact only one patent [1] has been registered and it has already been expired. Here we take the challenge to develop some topologies for the Gray code input DAC, using the characteristics that binary and Gray codes can be converted to each other using exclusive OR operation.

This thesis also attempts to compare the R-2R DAC and Gray code DAC in terms of their glitch performance. Two topologies (Current Steering Mode and Voltage Mode) of R-2R DACs are compared to corresponding two topologies of Gray code DACs. All the DACs are designed using MOSFETs, and their operation with glitch behaviour was confirmed with SPICE simulation. It was found that the glitches occur due to the multiple switch transition. This happens only in case of the binary code input DAC and not in case of the Gray code input DAC.

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1

Introduction

Electronic products have become a vital resource for day-to-day life in today′s perspective. We can barely think to manage our daily life without the help of electronic equipment like computers, television, or means of modern telecommunication. Most of these products are digital but the need of analog system is and will still be an important aspect in modern electronic world as the world stays analog in nature. Hence, the data conversion should be performed at various points in electronic systems.

There are two forms of data; digital and analog. Data conversion is the process of changing or converting one form of data in to another form. In today's digitized world, processing and transmission of digital data has become easy and secure with computers. Most complicated applications or logic can easily be done by the use of digital systems than analog circuits. This encouraged the conversion of analog data to digital form. The processing of data is done in digital form. However, the output has to be in analog form because of the fact that human beings can perceive analog signals comfortably than digital. This encouraged the conversion of digital data to analog form. These conversions require devices that can convert digital signals to analog signals and vice versa. The device that converts digital data in to analog data is called Analog to Digital Converter (ADC) and device that converts digital to analog is called Digital to Analog Converter (DAC).

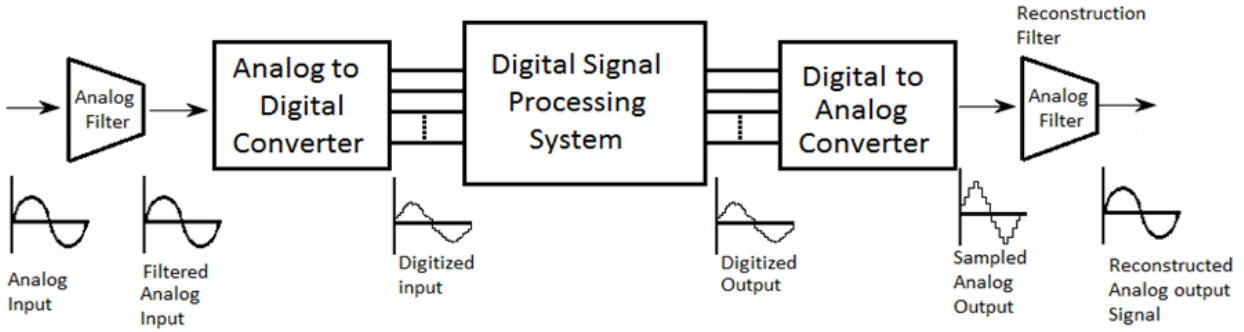


Figure 1-1 Basic Overview of Signal Processing System

The basic overview of signal processing system is depicted in figure 1-1. Generally, the electronic systems take analog signals as input. Because processing must be done using digital methods, an ADC is required to convert the analog signals into digital equivalents, and a DAC is needed to convert the processed signals back to analog for compatibility with analog devices. The filters eliminate undesired higher frequency components and correct other errors during the signal conversion process.

1.1 Thesis Organization

The thesis is organized as follows:

Chapter 1. Introduction. This chapter describes the basic introduction to DAC.

Chapter 2. Digital to Analog Converter Overview: Overview of different types of DACs, specifications and Errors associated with DACs

Chapter 3: Describes the design of different building blocks of DAC like OPAMP, current mirror, switch matrix, code converters, Bandgap Voltage reference and Flipped Voltage follower.

Chapter 4. R-2R Ladder DAC: This chapter describes the two architectures of R-2R Ladder DACs. Current Mode and Voltage Mode architectures. These architectures are designed and simulated using resistors as well as MOS transistors. This chapter is the base to compare the purposed Gray code DAC architectures.

Chapter 5. Purposed Gray code input DAC. This chapter describes the two purposed architectures of Gray code input DAC. These architectures are designed and simulated by using passive elements like resistors and current sources as well as MOS Transistors.

Chapter 6: Glitch Analysis of VMGCI DAC in case of sinusoidal signals: Contains simulation of purposed DAC with different inputs and different configurations.

Chapter 7: Conclusion and future works

Appendix: Contains the netlist of the simulated circuits of this thesis

2

Digital to Analog Converter Overview

The Digital to Analog Converter (DAC) is an interface between the digital signal processing system and the analog world. It is a device that converts digital signals to analog signals (voltage levels, current levels or electric charge). Since human senses are analog in nature and can only perceive analog signals, the digital signals from the DSP systems should first be converted to the analog form before presentation. For example, if the presentation is in the form of strings of 1s and 0s, only people with high technical knowledge can generate the meaning out of it and is a tedious time consuming task. This is where a DAC comes to play a significant role. A DAC helps the user to interpret the data easily. Therefore, the need of DAC is inevitable.

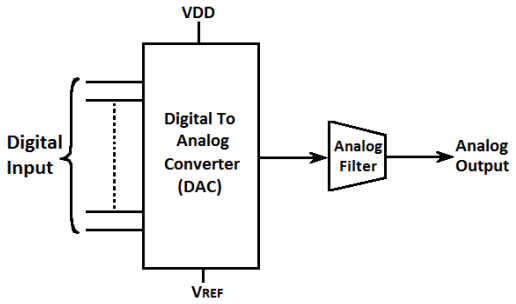


Figure 2-1 Block Diagram of Digital to Analog Converter

The N-bit DAC takes digital data in the form of Binary code as input and converts it to its corresponding analog output in the form of voltage or current. Basic block diagram of a DAC is shown in Figure 2-1. Here, an input N-bit digital word (b1, b2...bN) has a value **Digital Input** given by Equation 2.1

$$Digital\ Input = B_{N-1}2^{N-1} + \cdots + B_1 2^1 + B_0 2^0 \qquad (2.1)$$

Where, B_{N-1} is MSB, B_0 is LSB and they take values of either 1 or 0.

DACs are commonly used in various electronic applications such as music players to convert digital data streams into analog audio signals. They are also used in televisions and mobile phones to convert digital video data into analog video signals, which connect to the screen drivers

to display monochrome or colour images. They find applications in various other signal processing equipment.

2.1 Types of Digital to Analog Converters

The most common types are DACs are;

2.1.1 The Pulse Width Modulator

The pulse width modulator is the simplest of DACs. A stable current (electricity) or voltage is switched into a low pass analog filter with a duration determined by the digital input code. This technique is used for motor speed control and is now commonly used in hi-fi audio systems.

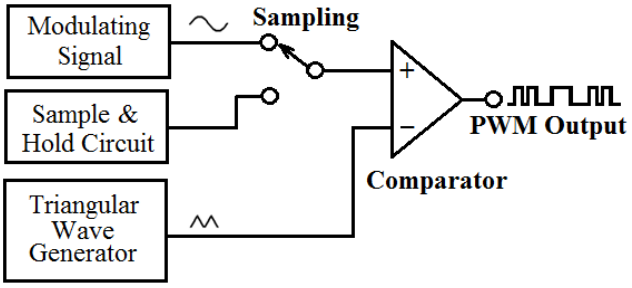


Figure 2-2 Pulse Width Modulator

2.1.2 Oversampling DAC

It is a pulse density conversion technique. A simple 1-bit DAC is often chosen, as it is inherently linear. The DAC is driven with a pulse density modulated signal, created through negative feedback. Most very high resolution DACs (greater than 16 bits) are of this type due to its high linearity and low cost. Speeds of greater than 100 thousand samples per second and resolutions of 24 bits are attainable with Delta-Sigma DACs.

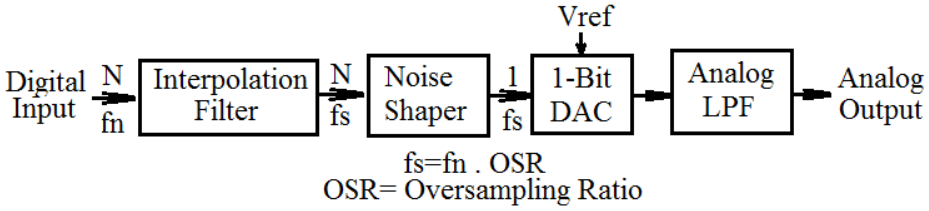


Figure 2-3 Oversampling DAC

2.1.3 The Binary Weighted DAC

It contains resistor or current source for each bit of the DAC connected to a summing point. These precise voltages or currents sum to the correct output value. This is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual

voltage or current. Such high-precision resistors and current sources are expensive, so this type of converter is usually limited to 8-bit resolution or less.

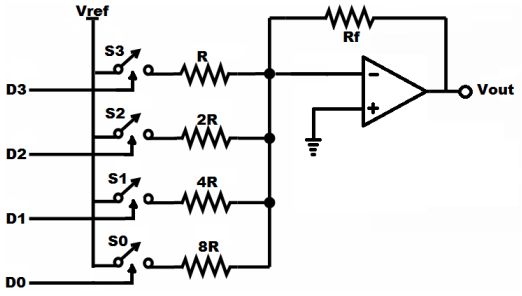


Figure 2-4 Binary Weighted DAC

2.1.4 The R-2R Ladder DAC

Most commonly used type of DAC. It contains only two values of resistors per bit and a switch. This improves DAC precision due to the ease of producing many equal matched values of resistors or current sources, but lowers conversion speed due to parasitic capacitance.

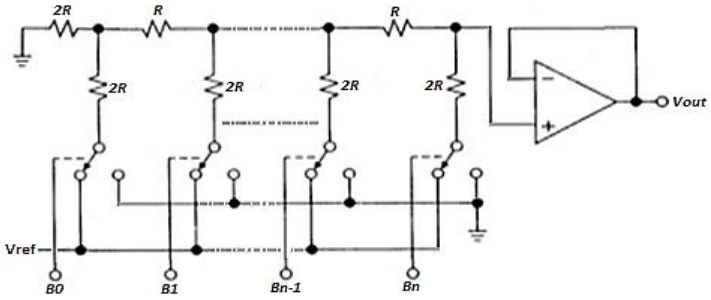


Figure 2-5 R-2R ladder DAC

2.1.5 The Segmented DAC

The Segmented DAC contains an equal resistor or current source segment for each possible value of DAC output. An 8-bit binary-segmented DAC would have 255 segments, and a 16-bit binary-segmented DAC would have 65,535 segments. This is perhaps the fastest and highest precision DAC architecture but at the expense of high cost.

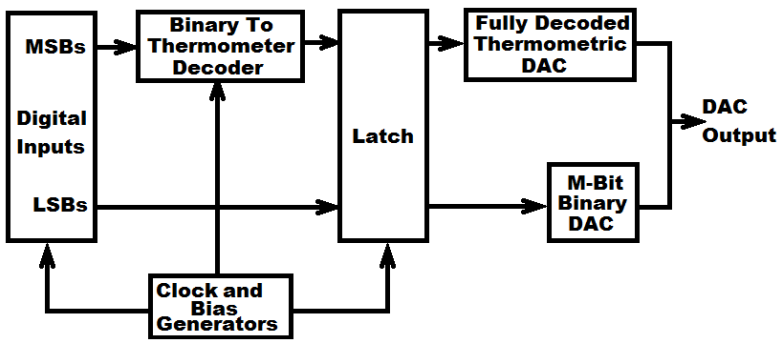


Figure 2-6 Segmented DAC

2.1.6 Hybrid DACs

Hybrid DACs are those using a combination of the above techniques in a single converter. Most DAC integrated circuits are of this type due to the difficulty of getting low cost, high speed and high precision in one device.

2.2 Specifications of DAC

D/A converters are available with wide range of specifications specified by manufacturer. Some of the most important specifications are as follows:

2.2.1 Resolution:

Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or, alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, the resolution is the value of 1 LSB.

$$Resolution(Volts) = \frac{V_{REF}}{2^N} \qquad (2.2)$$

Where $\boldsymbol{V_{REF}}$ is the reference voltage, N is the number of input bits.

2.2.2 Accuracy:

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. The relative accuracy is the maximum deviation after the gain and offset errors have been removed. Accuracy is also given in terms of LSB increments or percentage of full-scale voltage.

2.2.3 Stability:

The ability of a DAC to produce a stable output all the time is called stability. The performance of a converter changes with drift in temperature, aging and power supply variations. So all the parameters such as offset, gain, linearity error & monotonicity may change from the values specified in the datasheet. Temperature sensitivity also defines the stability of DAC.

2.2.4 Linearity:

The difference between the desired analog output and the actual output over the full range of expected values. The linearity of a DAC is also defined as the precision or exactness with which

the digital input is converted into analog output. An ideal DAC produces equal increments or step sizes at output for every change in equal increments of binary input.

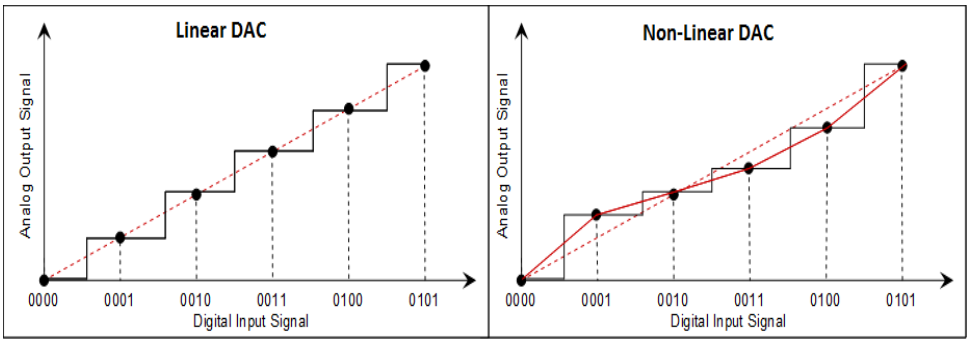


Figure 2-7 Linearity

2.2.5 Monotonicity:

A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. If a DAC has to be monotonic, DNL error should be less than or equal to 1 LSB at each output level [2].

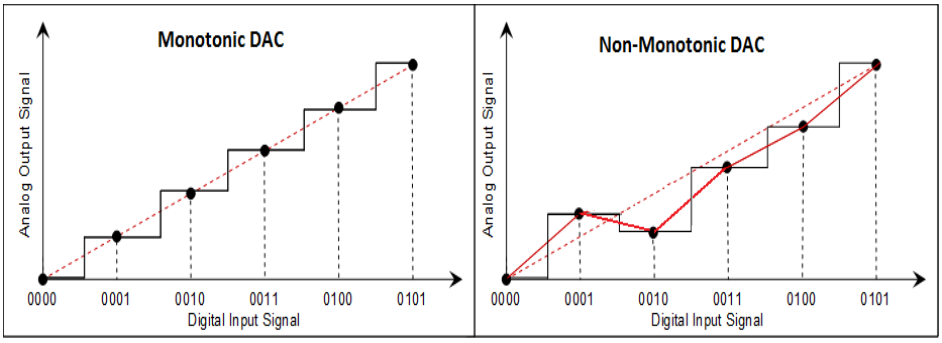


Figure 2-8 Monotonicity

2.2.6 Settling time:

Time required for the output signal to settle within +/- (1/2) LSB of its final value after a given change in input scale. The settling time is limited by slew rate of output amplifier. Ideally, an instantaneous change in analog voltage would occur when a new binary word enters into the DAC.

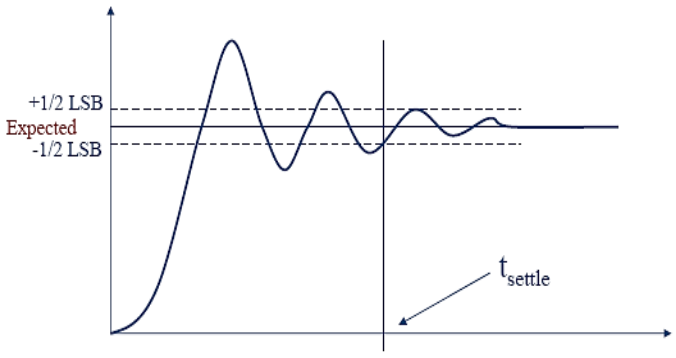


Figure 2-9 Settling Time

2.2.7 Speed

Rate of conversion of a single digital input to its analog equivalent. Conversion rate depends on clock speed of input signal and settling time of converter. When the input changes rapidly, the DAC conversion speed must be high.

2.3 Errors in DAC

The different types of errors that occur in DACs are briefly discussed below. The different types of errors include offset error, Gain Error, INL error, DNL error, and glitches.

2.3.1 Offset Error

It is the difference between an ideal and actual DAC output when zero digital code is applied to the input. Offset errors are normally bipolar and often expressed in a DAC data sheet in terms of millivolts.

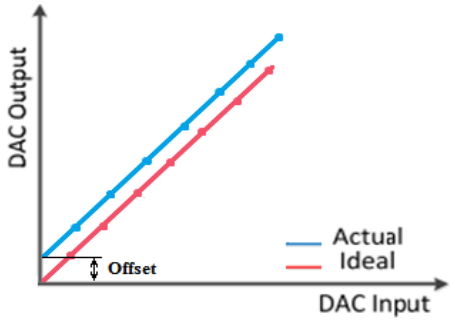


Figure 2-10 Offset Error

2.3.2 Gain Error

It is the difference between an ideal and actual output when full-scale digital code applied to the input. The gain error strongly depends on VREF stability. Gain error of DAC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or as a percent of full-scale range (%FSR), and it can be calibrated out with hardware or in software. Gain error is the full-scale error minus the offset error.

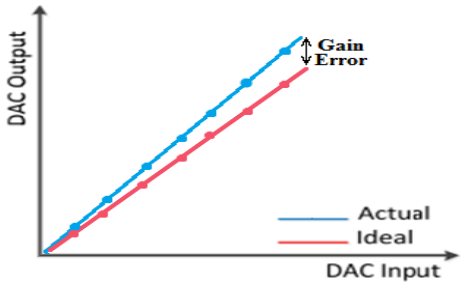


Figure 2-11 Gain Error

2.3.3 Differential Non-Linearity

DNL (Differential Non-Linearity) shows how much two adjacent code analog values deviate from the ideal 1 LSB step. The end fit method corrects the gain and offset error [3]. So, this method is simple and effective. The DNL is calculated using the equation 2.3. Here actual refers to the simulated values and ideal means the end fit reference line.

$$DNL(n) = \big(Vout(n) - Vout(n-1)\big)_{actual} - \big(Vout(n) - Vout(n-1)\big)_{Ideal} \qquad (2.3)$$

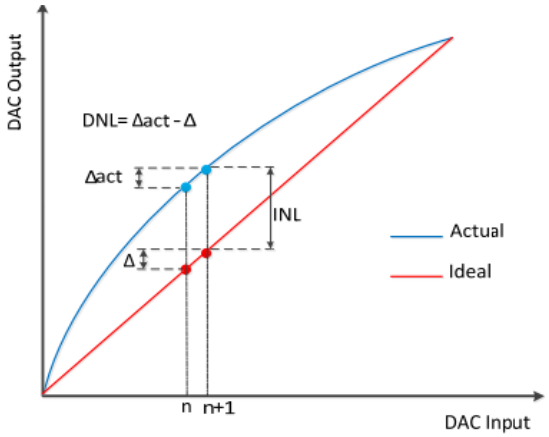


Figure 2-12 Differential Non-Linearity

2.3.4 Integral Non-Linearity

INL (Integrated Non-Linearity) shows how much the DAC transfer characteristic deviates from an ideal one. The ideal characteristic is usually a straight line; INL shows how much the actual voltage at a given code value differs from that line, in LSBs (1 LSB steps). Figure 2.13 shows an example of INL for a 3-bit DAC. INL is calculated using the equation 2.4.

$$INL(n) = Vout_{actual}(n) - Vout_{ideal}(n) \qquad (2.4)$$

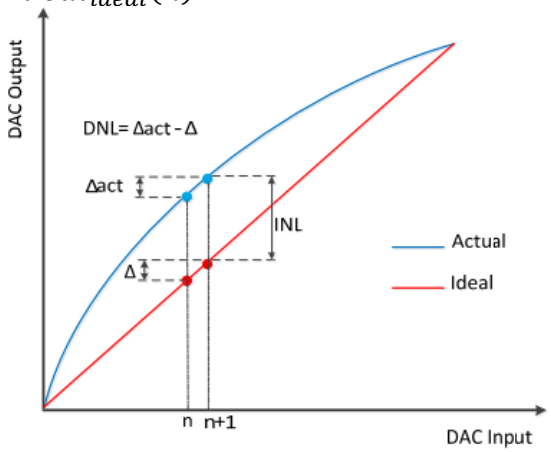


Figure 2-13 Integral Non-Linearity

2.3.5 Glitches

Glitches are a limitation at high-speed data transfers. They occur during a transition between two output values, as an undesired output value due to difference in signal propagation delay. For a short period of time a false code could be represented at the output [4]. For example if the code transition is from 0111 to 1000 and if the MSB is switching faster than the LSBs, the code 1111 may be present for a short time. This code represents the maximum value and hence the glitch would be large.

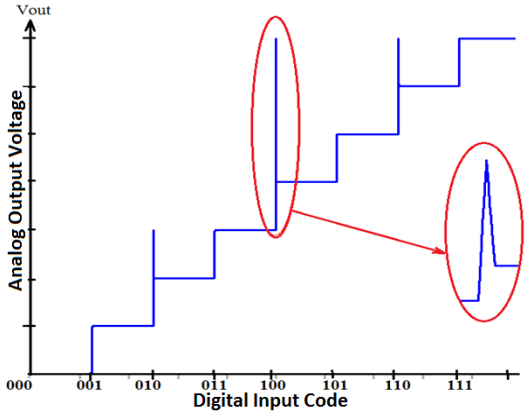


Figure 2-14 Glitches

3

DAC Building Blocks

Various analog circuit blocks are required to design a fully functional electronic circuit. For example, current mirror circuits, an OPAMP, switches, a reference voltage generator, etc. The Gray code input DAC also requires some functional blocks like current mirrors, switch matrices, and an OPAMP. This chapter attempts to explain and design some of the circuit blocks required for DACs.

3.1 Two Stage OPAMP

Operational amplifier, abbreviated as OPAMP, is an integral part in most of the analog circuits and systems. The basic OPAMP is a 3-terminal device with two inputs; one of which inverts the phase of the signal, the other preserves the phase, and one output (excluding power supply pins). OPAMP is characterized by very high input impedance, very high bandwidth, very high gain, very low output impedance, low power consumption, very high common mode rejection, etc. The popular and most commonly used architecture of OPAMP is a two stage OPAMP. The basic block diagram of two stage OPAMP is depicted in Figure 3-1.

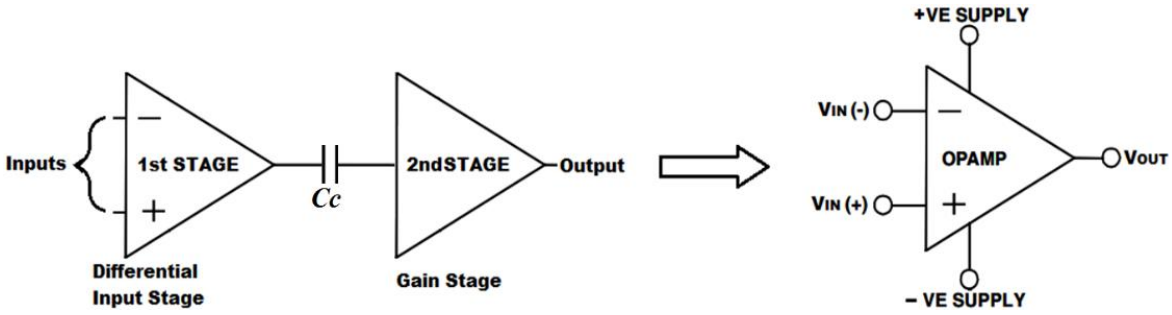


Figure 3-1 Block Diagram of two stage OPAMP

A two-stage operational amplifier consists of a differential amplifier in the 1st stage followed by a common source amplifier (CSA) in the 2nd stage [5]. Differential amplifier stage is to ensure high gain and CSA stage is to further increase the gain and also provide high voltage swing at the output. It can give a differential voltage or single ended voltage, depending on the configuration at the output which depends on differential input voltage. Single-ended output degrades the output

swing of the amplifier. Also the common mode rejection ratio (CMRR) degrades as the symmetry of the circuit is lost.

Figure 3-2 shows the small signal model of two-stage operational amplifier. The first stage differential amplifier is connected to the second stage source follower amplifier by a compensation capacitor Cc.

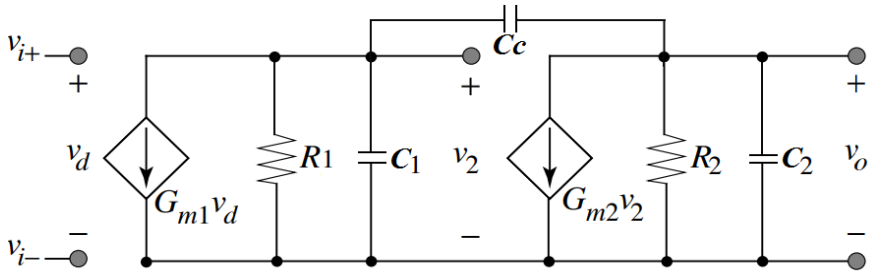


Figure 3-2 Small Signal Model of two stage OPAMP

The transfer function of the OPAMP is derived using the small signal model.

Determination of Transfer Function

$$\frac{Vout}{Vin} = \frac{V2}{Vd} \times \frac{Vo}{V2} \qquad (3.1)$$

Applying KCL at the input node,

$$\frac{V2}{1/sc1} + \frac{1}{R1} + Gm1Vd + \frac{V2-Vout}{1/sCc} \qquad (3.2)$$

$$V2 = \frac{Vo.\,sCc.R1 - Gm1Vd.R1}{1+sR1(C1+Cc)} \qquad (3.3)$$

Applying KCL at the output node,

$$Vout\left[s(C2+Cc) + \frac{1}{R2}\right] = V2(sCc - g_{m2}) \qquad (3.4)$$

From (3.3) and (3.4)

$$\frac{\boldsymbol{Vout}}{\boldsymbol{Vin}} = \frac{g_{m1}R1g_{m2}R2(1-\frac{sCc}{g_{m2}})}{s^2[R1R2(C1C2+C1Cc+C2Cc)]+s[R2(C2+Cc)+R1(C1+Cc)+Cg_{m1}R1R2]+1} \qquad (3.5)$$

Determination of poles, Zeroes, and other parameters from the transfer function

At DC, s=0, so the poles and zero are given by

$$\boldsymbol{P1} \approx \frac{1}{g_{m2}.R2.R1.Cc}, \qquad \boldsymbol{P2} \approx \frac{g_{m2}}{C2}, \qquad \boldsymbol{Z} \approx \frac{g_{m2}}{Cc} \geq 10 \cdot GBW$$

For given specifications of DC Gain A_{DC}, Gain Bandwidth GBW, Slew Rate SR, Phase Margin PM, can be related to the circuit parameters as follows:

$$DC\ Gain:\ A_{DC} = g_{m1}R1g_{m2}\mathrm{R2} \quad (3.6)$$

$$Gain\ Bandwidth:\ GBW = A_{DC} \times P1 \approx \frac{g_{m1}}{\mathrm{Cc}} \quad (3.7)$$

$$Slew\ Rate:\ SR = \frac{Iout}{Cc} \quad (3.8)$$

$$Phase\ Margin:\ PM = -\tan^{-1}\frac{GBW}{Z} - \tan^{-1}\frac{GBW}{P1} - tan^{-1}\frac{GBW}{P2} \quad (3.9)$$

$$Compensation\ Capacitor:\ Cc \geq 0.22C_L \quad (3.10)$$

3.1.1 Design specifications and design procedure

The two-stage OPAMP is designed using the TSMC 0.18 micrometer process. The design parameters and specifications are shown in Table 3.1. The design procedure [6] involves the determination of transistor sizes, gain and other specifications.

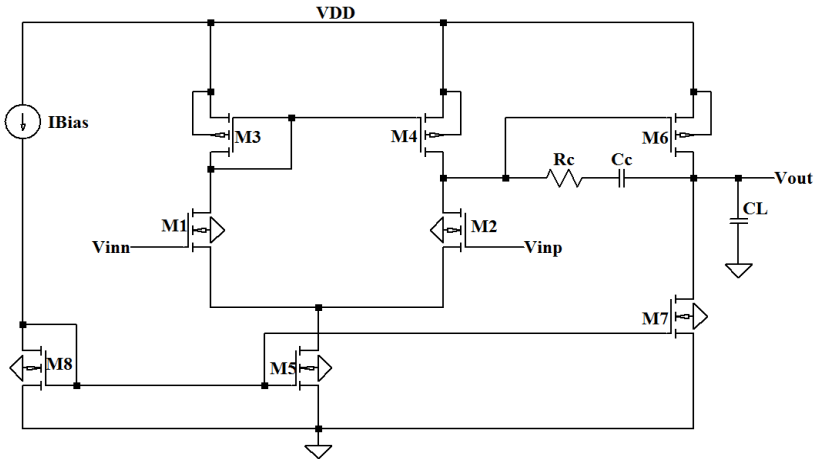


Figure 3-3 Two stage OPAMP Schematics

Table 3-1 Design specifications of a two stage OPAMP

Design Specifications	
Technology	TSMC 018um Process
DC Gain	≥60dB
Gain Bandwidth (GBW)	30MHZ
Phase Margin	$\geq 60°$
Slew Rate	$\approx 10V/\mu S$
Input Common Mode Range(ICMR)	1.6 (max)~ 0.8(min)
Load Capacitance	2pf
Power Dissipation	$\leq 300\mu W$
Vdd	1.8V-3.3V
Trans Conductance PMOS Kp	$92.75uA/V^2$
Trans Conductance NMOS Kn	246.79 uA/V^2

1. $Cc \geq 0.22 \cdot CL = 0.44pf \approx 0.6pF$ *(3.11)*
2. $Slew\ Rate = \frac{I5}{Cc} \rightarrow I5 = SR \cdot Cc = 20\mu\ (Adjusted)$ *(3.12)*

3. $gm1 = GBW \cdot Cc \cdot 2\pi = 113.09\mu \approx 170u$ *(3.13)*

$(W/L)_{1,\ 2} = \frac{gm1^2}{\mu nCox \cdot 2I_5} = 5.186 \approx 7$ *(3.14)*

4. For design of M3 and M4

$(W/L)_{3,4} = \frac{2I_{D3}}{\mu pCox \cdot [VDD - ICMRmax - V_{t3max} + V_{t1min}]} \approx 14$ *(3.15)*

5. For design of M5

$Vin \geq Vgs1 + V_{dsat\ 5} => V_{dsat\ 5} = 0.1004$ *(3.16)*

$(W/L)_5 = \frac{2I_5}{\mu nCox \cdot V_{dsat\ 5}^2} \approx 16$ *(3.17)*

6. Design of M6, for 60° Phase Margin, *gm6=10gm1*

$\left(\frac{W}{L}\right)_6 = \frac{gm_6}{gm_4} \cdot \left(\frac{W}{L}\right)_4 \approx 150$ *(3.18)*

7. Design of M7

$I_6 = \left(\frac{W}{L}\right)_6 / \left(\frac{W}{L}\right)_4 \times I_4 = 110\mu A$ *(3.19)*

$I_7 = \left(\frac{W}{L}\right)_7 / \left(\frac{W}{L}\right)_5 I_5 => \left(\frac{W}{L}\right)_7 = 88$ *(3.20)*

Gain of first stage,

$Gain1 = gm1(ro1||ro4) = \frac{gm1}{gds1+gds4} = 71.8894$ *(3.21)*

Gain of second stage,

$Gain2 = gm6\ (ro6||ro7) = \frac{gm6}{(gds6+gds7)} = 48.0059$ *(3.22)*

Total gain

Gain (A_{DC}) =20log71.8894+20log 48.0059=70.759

3.1.2 Simulation Results

The simulation results of the OPAMP is shown in Figure 3-4.

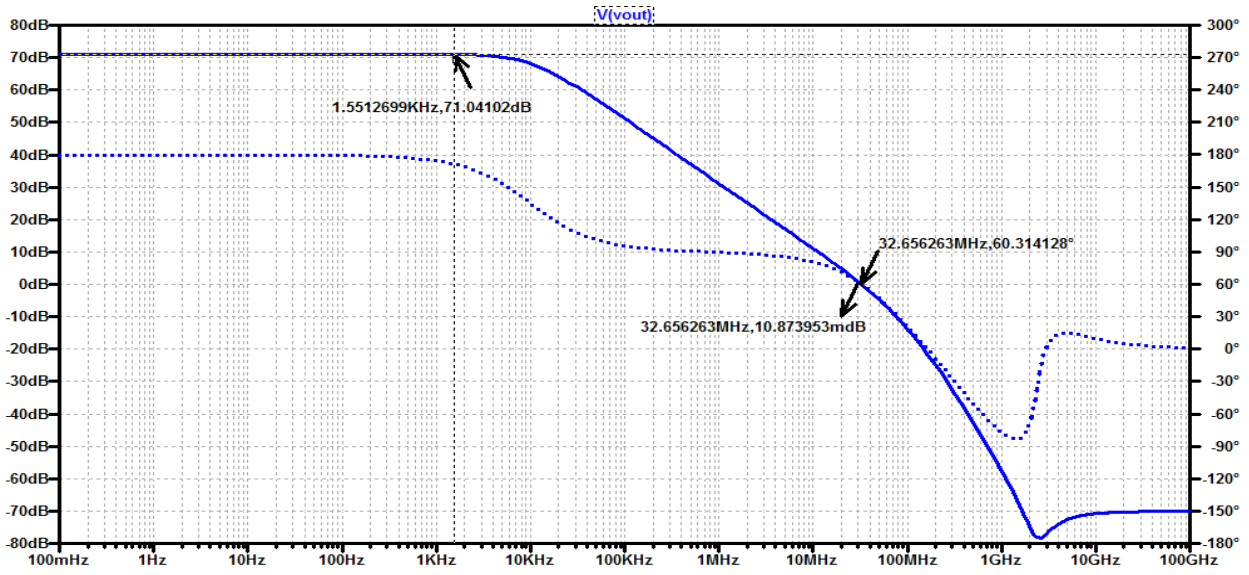


Figure 3-4 AC response of the designed two stage OPAMP

Table 3-2 Transistor sizes and Simulated results of two stage OPAMP

Transistors	W/L	Specifications	Simulated
M1	2.7u/0.5u	**Gain**	71.978dB
M2	2.7u/0.5u	**GBW**	31.23MHz
M3	7u/0.5u	**Phase**	58.25◦
M4	7u/0.5u	**ICMR**	0.8-1.6V
M5	6u/0.5u	**VDD**	1.8V
M6	88u/0.5u	**CL**	2PF
M7	38u/0.5u	**Cc**	600fF
M8	6u/0.5u	**Rc**	1k

From the simulated results we can see that the designed OPAMP has met almost all the specifications. Although the phase and GBW trade-off is present in the design as every design does.

3.2 Switch Matrix

The current/voltage switch matrix is a double pole double throw (DPDT) switch, which contains two inputs (IN1 and IN2), two outputs (OUT1, OUT2), and a switch control pin (CTL). The switch connects IN1 to OUT1 and IN2 to OUT2 when CTL is logic LOW. Similarly, it connects IN1 to OUT2, and IN2 to OUT1 when CTL signal is logic HIGH. The CTL pins are provided with Gray code input as generated by circuit in Figure 5-2. The definition, realization and timing diagram of current/voltage switch matrix are shown in figure 3-5 (a), (b) and (c) respectively.

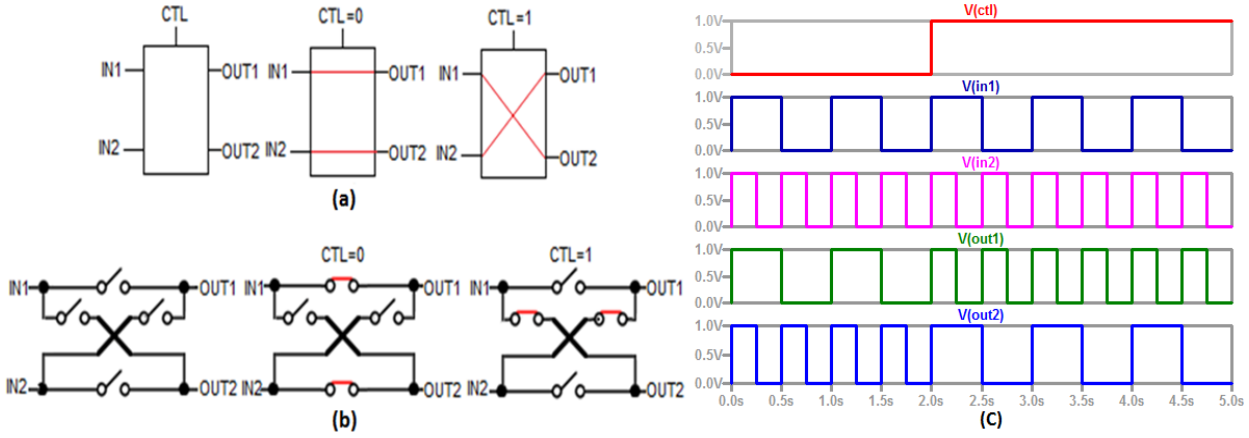
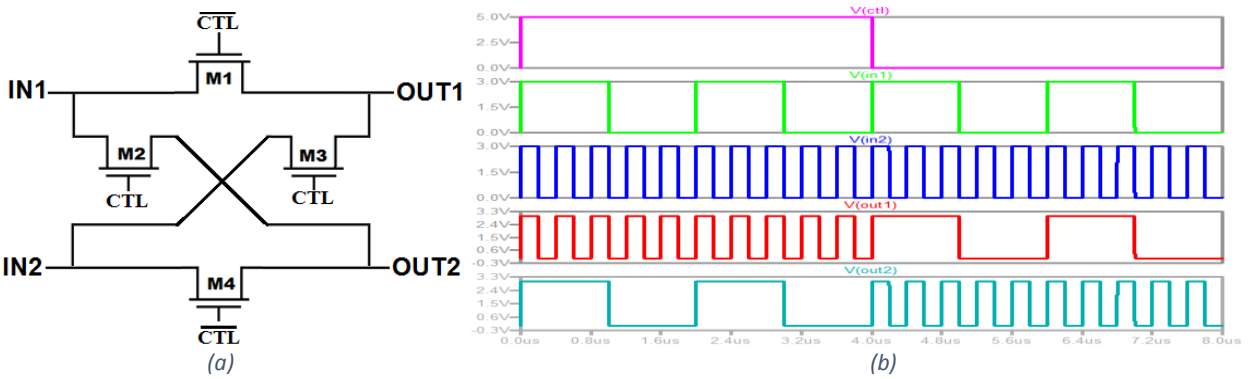


Figure 3-5 Current Voltage Switch Matrix (a) Definition (b) Realization (c) Timing Diagram

These DPDT switches are modelled using NMOS transistors. The transistors' aspect ratio was used as W/L=2um/0.18um. Figure 3-6 shows the implementation and timing waveforms of MOSFET only DPDT switch for IC implementation.



(a) (b)

Figure 3-6 MOSFET Implementation of DPDT Switch (a) Construction (b) Timing Waveforms

3.3 Binary to Gray Code Converter

Conversion of Binary to Gray code can be realized by using the XOR operation of the binary bits [7]. Binary code: B3, B2, B1, B0, are converted to Gray code: G3, G2, G1, G0 as follows:

$$G3 = B3, \quad G2 = B3 \oplus B2, \quad G1 = B2 \oplus B1, \quad G0 = B1 \oplus B0 \qquad (3.23)$$

The conversion process and the circuit diagram used for binary to Gray code conversion are shown in Figure 3-7. Also timing diagrams for both binary and Gray codes are depicted in Figure 3-8 (a) and (b).

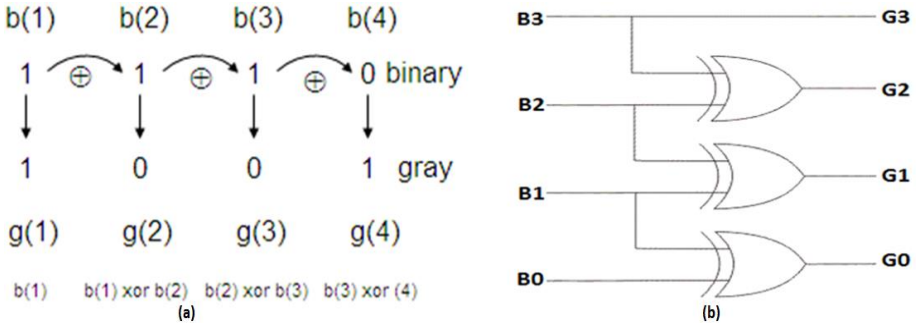


Figure 3-7 (a) The conversion process from Binary to Gray (b) circuit diagram for Binary to Gray code conversion

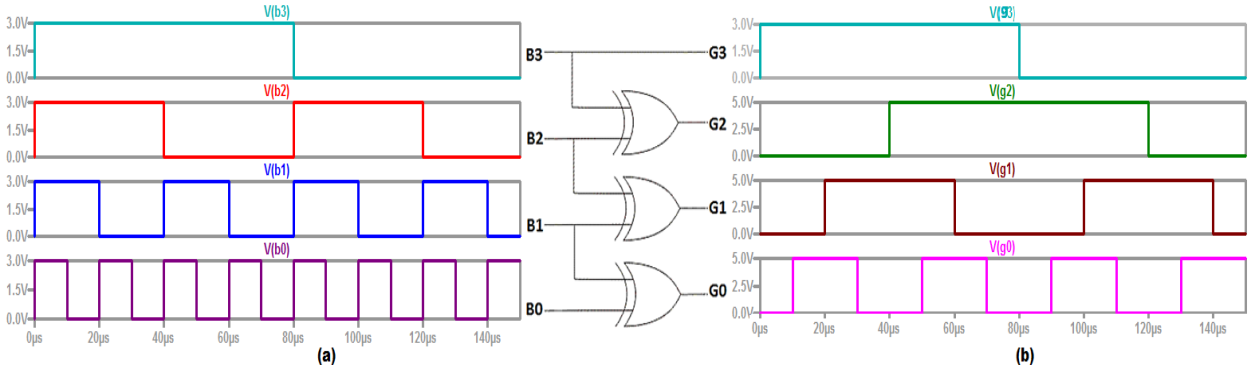


Figure 3-8 Timing Diagram of (a) Binary code (b) Gray code

3.4 Current Sources and Sinks

A current mirror is a circuit which copies the input current to a current sink or current source as an output current. The principle of the current mirror is that if the gate-source potential of two identical MOSFETs are equal, then the current through these two transistors should be equal [6]. The output current can be identical to the input current or it can be scaled by some factor. It is a basic building block for analog circuits and is used to provide bias currents and voltages to different stages of analog circuits. The current mirror is characterized as:

- Output current is linearly related to the input current as $I_{out} = k \times I_{in}$
- Input resistance is very low
- Output impedance is very high

A simple current mirror can be constructed using MOSFETs. It requires two identical MOSFETs M1 and M2 where M1 or the input MOSFET is diode connected. And the output is taken from the MOSFET M2. Figure 3-9 shows the circuit diagram of a simple current mirror.

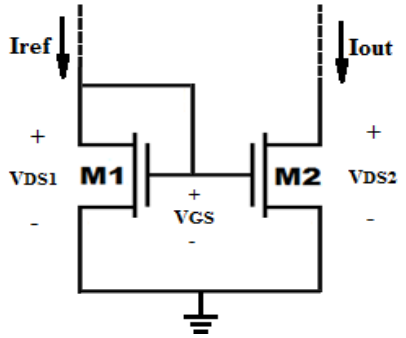


Figure 3-9 Simple MOSFET Current Mirror Circuit

Since M1 is diode-connected, the MOSFET works in the saturation region. The current equation for a diode-connected MOSFET is given in equation 3.24.

$$I_{in} = \frac{1}{2}\mu_n C_{ox}\frac{W1}{L1}(V_{GS1} - V_{TH})^2 \qquad (3.24)$$

Assuming the MOSFET M2 is in saturation,

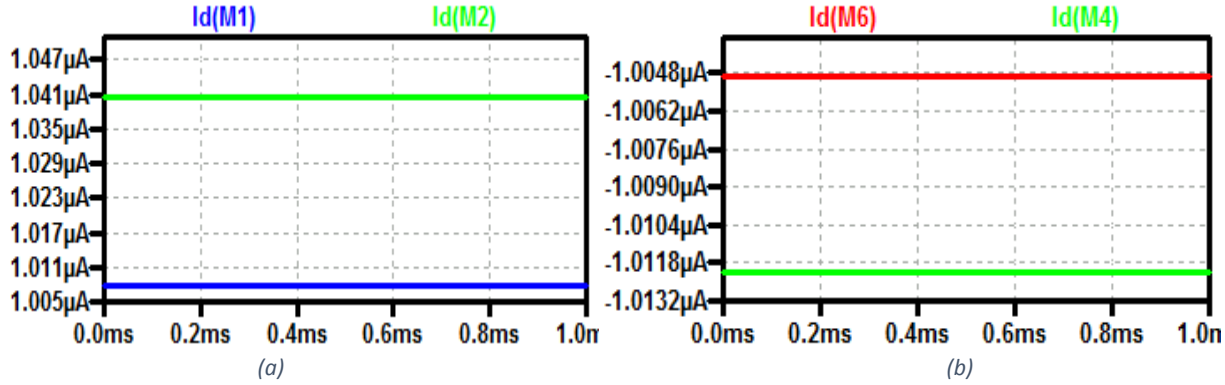
$$\mathrm{I_{out}} = \frac{1}{2}\mu_n \mathrm{C_{ox}}\frac{\mathrm{W2}}{\mathrm{L2}}(V_{GS2} - V_{TH})^2 \qquad (3.25)$$

Dividing equation 3.25 by 3.24, we get

$$\frac{\mathrm{I_{out}}}{\mathrm{I_{in}}} = \frac{\frac{1}{2}\mu_n \mathrm{C_{ox}}\frac{\mathrm{W2}}{\mathrm{L2}}(\mathrm{V_{GS1}} - \mathrm{V_{TH1}})^2}{\frac{1}{2}\mu_n \mathrm{C_{ox}}\frac{\mathrm{W1}}{\mathrm{L1}}(V_{GS2} - V_{TH2})^2}$$

If the MOSFETs are matched, i.e. $V_{GS1} = V_{GS2}$ and $V_{TH1} = V_{TH2}$, then we have

$$\frac{I_{out}}{I_{in}} = {W_2 L_1}/{W_1 L_2} \qquad (3.26)$$

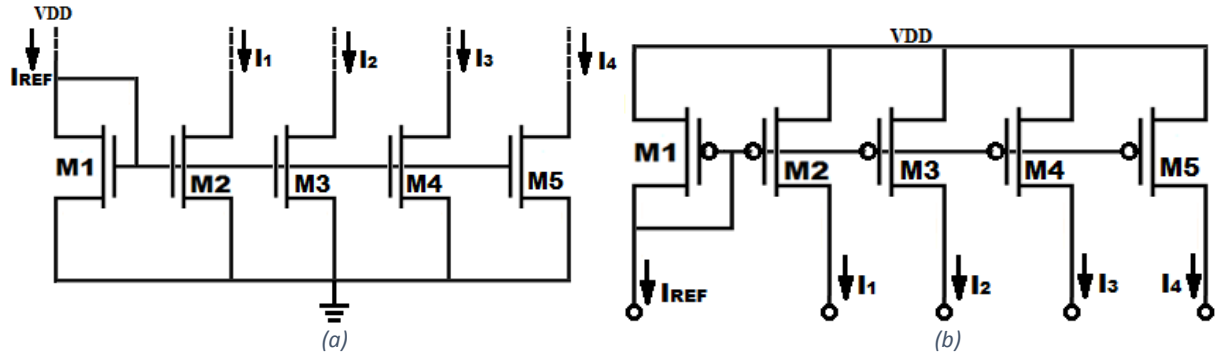


(a) *(b)*

Figure 3-10 Simulation Results of Current Mirror

We know from equation 3.26 that it is possible to replicate the current in input MOSFET to the output if the aspect ratios of the transistors are the same. Also different values of currents can be produced by changing the aspect ratio of the MOSFETs. NMOS current source sinks current to ground, also known as a current sink. PMOS current source sources current from positive supply, hence termed as a current source.

In an integrated circuit, there is often need of multiple current sources and sinks. It is possible to tie up multiple current mirrors to single current source or sink. Multiple current sources or sinks generating from the same reference current is referred as current steering circuit.



(a) *(b)*

Figure 3-11 Current Steering Circuit (a) NMOS (b)PMOS

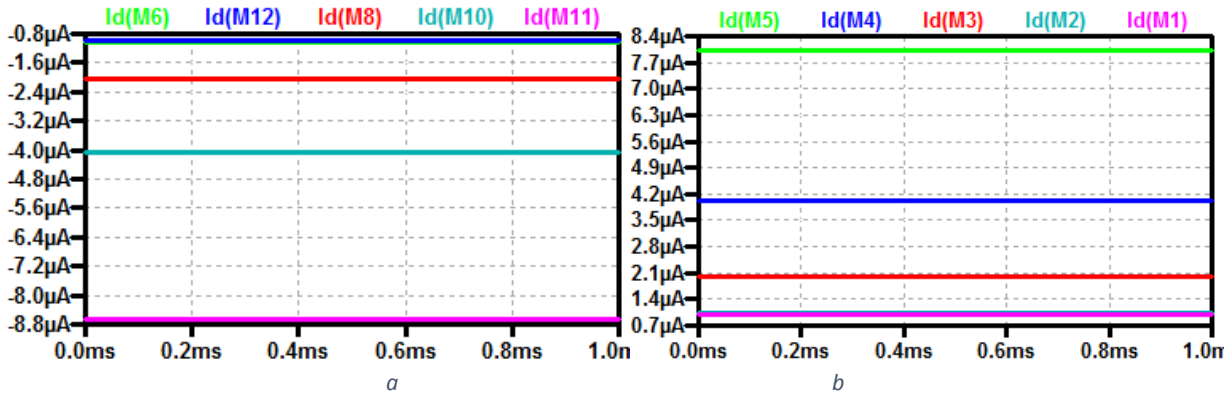
For example, the reference current is 1µA, and aspect ratio of M1 is 2. We need to generate currents of I1=1µA, I2=2µA, I3=4µA and I4=8µA, then, the aspect ratios of M2, M3, M4 and M5 is calculated as:

$$(W/L)_2 = I_1 \times \frac{(W/L)_1}{I_{REF}} = 1 \times \frac{2}{1} = 2$$

$$(W/L)_3 = I_2 \times \frac{(W/L)_1}{I_{REF}} = 2 \times \frac{2}{1} = 4$$

$$(W/L)_4 = I_3 \times \frac{(W/L)_1}{I_{REF}} = 4 \times \frac{2}{1} = 8$$

$$(W/L)_5 = I_4 \times \frac{(W/L)_1}{I_{REF}} = 8 \times \frac{2}{1} = 16$$



a *b*

Figure 3-12 Simulation Result of (a) PMOS and (b) NMOS Current Steering Circuit

3.5 Bandgap Voltage Reference

Bandgap voltage generators are widely used in many applications of Analog and Digital Circuits such as LDO (Low Drop Out), Buck/Boost Converters, A/D, D/A, DRAM and flash memories. The low-power and low voltage operations are increasingly in demand for battery operated portable devices. The output generators are designed to stabilize over supply voltage, process and temperature variations. Bandgap voltage reference is a self-biased reference voltage generator that can successfully achieve these requirements. The constant voltage can be generated by combining the PTAT (Proportional to Absolute Temperature) and CTAT (Complementary to Absolute Temperature) [8]. This is the basic idea behind the BGR.

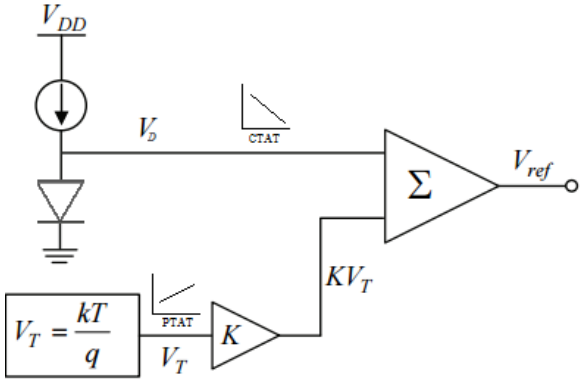


Figure 3-13 Block Diagram of BGR

The working principle of BGR Circuits can be illustrated in Figure 3-13. The voltage across the diode has a negative temperature coefficient of about -1.6mV / °C also known as the CTAT. The VT has a positive temperature coefficient of about 0.086mV/°C also known as PTAT. Since the PTAT is very low in comparison to CTAT so that the PTAT has to be multiplied by some factor to cancel the effect of CTAT to get the constant reference voltage at the output. The reference output voltage can be expressed as

$$Vref = V_D + KV_T \ldots\ldots \quad (3.27)$$

3.5.1 CTAT Circuit Design

If we pass a constant current Io through a diode, the voltage across the diode is found to be a CTAT.

$$I_o = I_S\, exp^{V_D/V_T}$$

$$V_D = V_T \ln\frac{I_o}{I_S} \ldots\ldots \quad (3.28)$$

Here V_D is composed of two terms $V_T = KT/q$ which is a PTAT as it is directly proportional to temperature.

$$\frac{dV_T}{dT} = \frac{K}{q} \quad (3.29)$$

The second term $\ln\frac{I_o}{I_S}$ is a CTAT as I_S is a CTAT term. This can be verified as follows:

$$I_S \propto \mu.K.T.{n_i}^2 \quad (3.30)$$

$\mu \propto \mu_o T^m$ Where m≈-3/2

$$n_i \propto T^3 exp^{-Eg/KT} \quad (3.31)$$

Combining these terms, we have the followings:

$$I_S \propto T^{4+m}\exp\frac{-Eg}{KT} \quad (3.32)$$

$$\frac{dI_S}{dT} \propto I_S\left(\frac{4+m}{T} + \frac{Eg}{KT^2}\right) \quad (3.33)$$

$$\frac{dV_D}{dT} \propto \frac{(V_D - (4+m)V_T - \frac{Eg}{q})}{T} \quad (3.34)$$

$$\frac{dV_D}{dT} \approx -1.88mV \quad (3.35)$$

3.5.2 PTAT Circuit Design

Let us consider a circuit as shown in Figure 3-14 to generate a PTAT Voltage. From this figure

$$V_{D1} = V_T \ln\frac{I_o}{I_S} \quad (3.36)$$

$$V_{D2} = V_T \ln \frac{I_o}{nI_S} \quad (3.37)$$

$$V_{D1} - V_{D2} = V_T \ln(n) \quad (3.38)$$

$where\ n = no\ of\ diodes.$

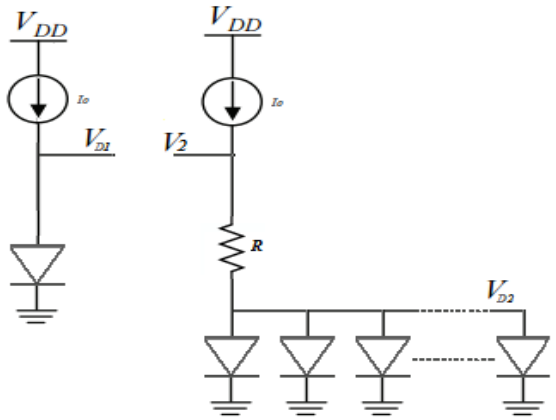


Figure 3-14 PTAT Circuit

So in order to generate a PTAT circuit, we somehow need to equalize the voltages V_{D1} and V_2. So when,

$$V_{D1} = V_2 \quad (3.39)$$

We have the followings:

$$I_o R = V_{D1} - V_{D2} = V_T \ln(n) \quad (3.40)$$

This is a PTAT voltage and it is across the resistor R1. So to get a PTAT node, we use the properties of the current mirror as shown in Figure 3-15.

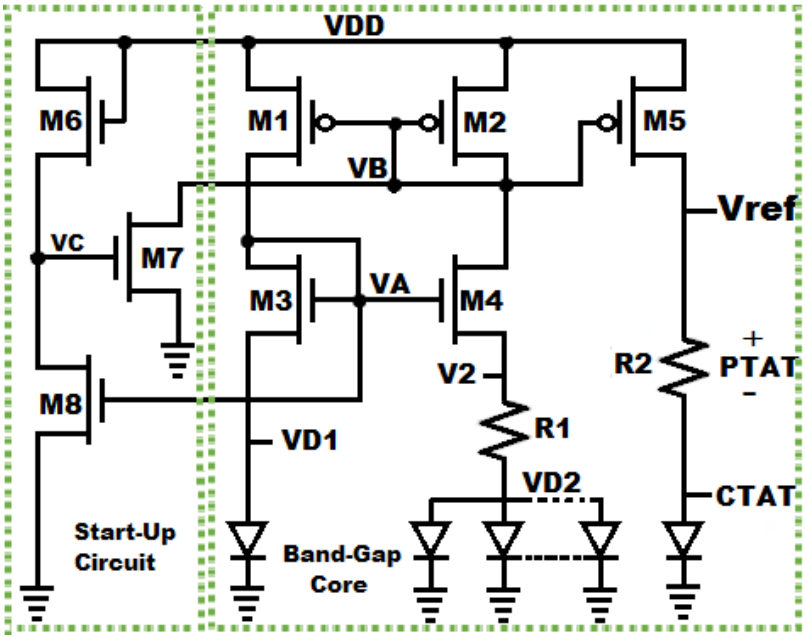


Figure 3-15 BGR Circuit implementation.

3.5.3 BGR Design

The implementation of PTAT and CTAT is done. Now the BGR is the combination of PTAT and CTAT. Figure 3-15 shows the complete BGR implementation where the PTAT voltage and the CTAT voltage adds together to generate a constant voltage Vref.

$$V_{ref} = \alpha_1 \cdot PTAT + \alpha_2 \cdot CTAT \quad (3.41)$$

$$V_{R2} = I_o R_2 \quad (3.42)$$

$$V_{R2} = \frac{R_2}{R_1} V_T \ln(n) \quad (3.43)$$

For Vref to be constant with respect to temperature,

$$\frac{\partial V_{ref}}{\partial T} = 0$$

$$V_{R2} = \frac{R_2}{R_1} V_T \ln(n) + V_D \quad (3.44)$$

$$\alpha_2 = 1$$

$$\alpha_1 = \frac{R_2}{R_1} \ln(n) \quad (3.45)$$

For n=2, $V_T = 26mV, Io = 5u$, R1=3.6k

$$R_2 = \frac{\alpha_1 \cdot R_1}{\ln(n)} = 97.94k \quad (3.46)$$

3.5.4 Simulation Results of BGR

Figure 3-16 (a) shows that Vref is almost constant with respect to temperature, but Figure 3-16 (b) shows that Vref is slightly varying with change in VDD. This can be corrected using the cascode current mirror and the output is shown in Figure 3-16 (c).

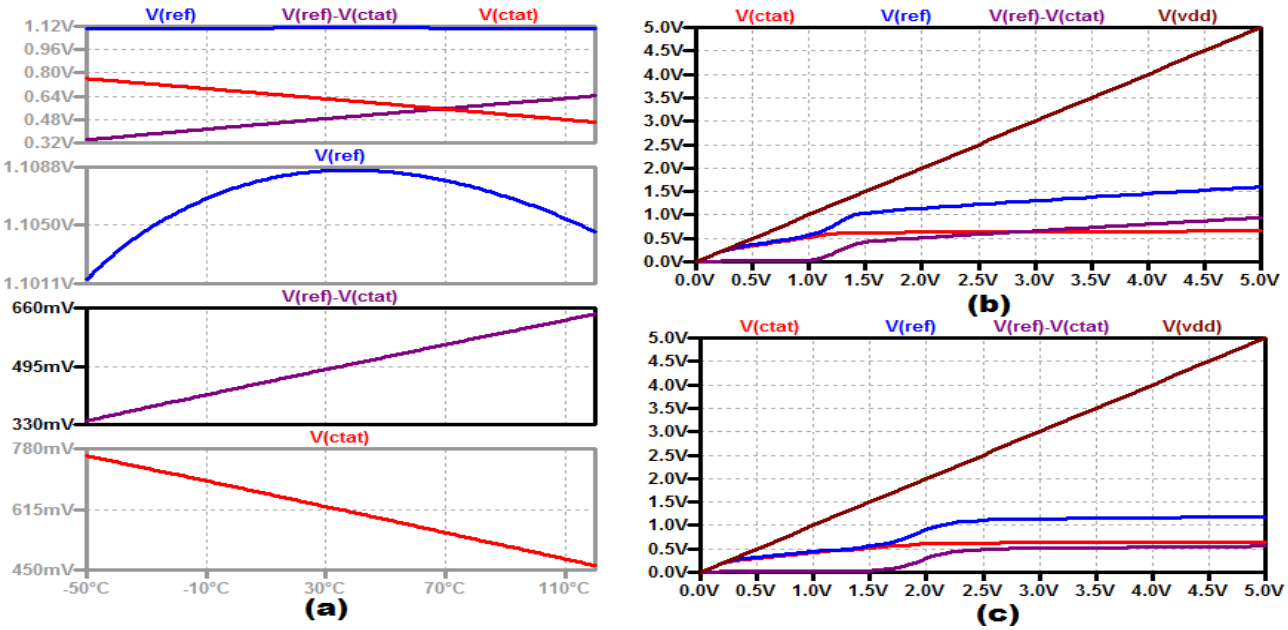


Figure 3-16 Simulation results of a BGR Circuit (a) Variation of Different Voltage with change in Temperature (b) Variation of Reference Voltage with change in VDD (c) Stabilization of Reference Voltage employing Cascode Current Mirror

3.5.5 Start-up Circuits for Current Mirror Based BGR

There are conditions in self-biased circuits where the circuit reaches in zero current state. In current mirror based circuit, this state is reached when VA= 0 and VB= VDD (refer Figure 3-15). An NMOS (M7) is connected to VB so when VB reaches to VDD, current starts to flow through M7 pulling VB below VDD. Hence current starts to flow through the mirror. As soon as the current mirror turns on, a big MOSFET M8 starts to conduct pulling VC below VDD. As the VC goes near to zero, M7 turns off, turning off the start-up circuit. The start-up issue is shown in Figure 3-17 (a). Where, the voltage at node VA is 0 and VB is VDD. The waveforms of Figure 3-17 (b) verifies the start-up issue being eliminated by using a start-up circuit. Table 3.3 shows the sizes of transistors and resistors during the time of simulation.

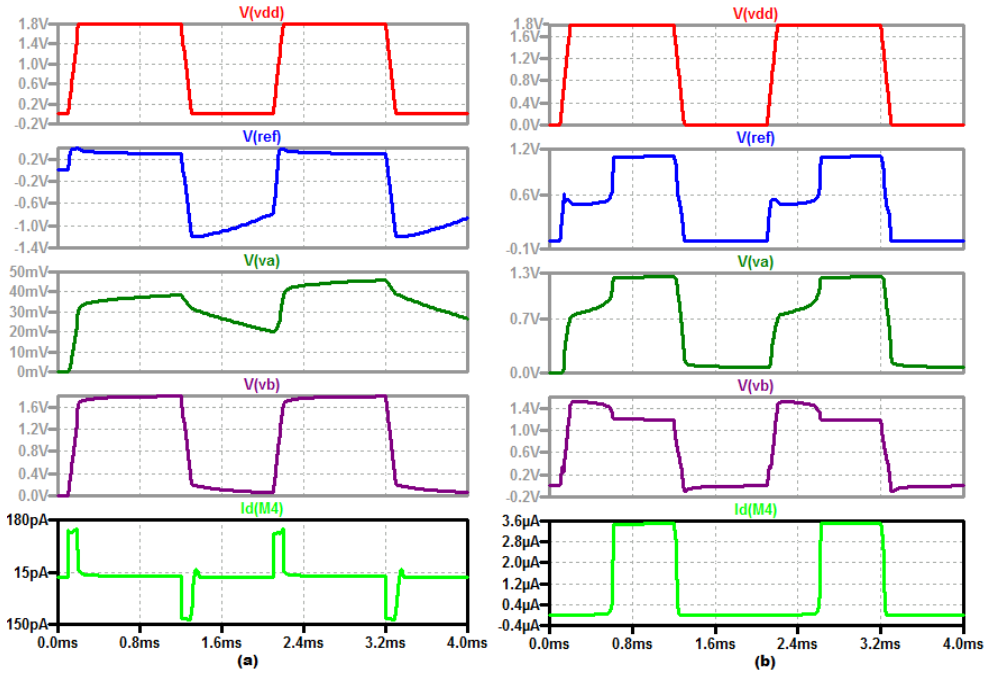


Figure 3-17 Transient simulation of different node voltages (a) Before employing Start-up Circuit (b) After employing Start-up Circuit.

Table 3-3 Sizes of transistors and resistors for BGR during Simulation

Transistors	Sizes(W/L)
M1, M2, M5	5µ/2µ
M3, M4	10µ/2µ
M6	1µ/2µ
M7	2µ/2µ
M8	80µ/20µ
Resistors	
R1	5KΩ
R2	135KΩ

3.6 Source Followers

The common drain amplifier is also known as the source follower (SF) or the buffer amplifier. The input signal is fed at the gate, and the output is taken from the source terminal. It is also termed as a voltage buffer as its voltage gain is almost equal to 1. It is termed as a source follower because the output voltage closely follows the input. The input resistance is very high and the output resistance is very low. Here some variations of source followers like source follower, flipped and folded flipped voltage followers are discussed and designed in detail.

3.6.1 Simple Source Follower

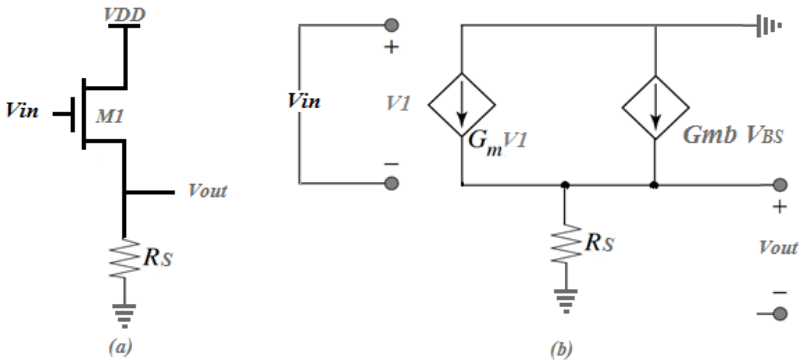


Figure 3-18 Source Follower (a) Circuit Diagram (b) Small signal model

The body terminal is connected to the lowest supply voltage (ground) to maintain source body junction reverse biased. Since source is connected to output, Vbs changes with output [9].

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right) \quad (3.47)$$

$$\frac{\partial V_{th}}{\partial V_{in}} = \eta \frac{\partial V_{Out}}{\partial V_{in}} \quad (3.48)$$

$$V_{out} = Id * R_s = \frac{\mu_n C_{ox} W}{2L}[(V_{in} - V_{out} - V_{th})^2] * R_s \quad (3.49)$$

$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{\mu_n C_{ox} W}{L}\left[(V_{in} - V_{out} - V_{th})\left(1 - \frac{\partial V_{out}}{\partial V_{in}} - \frac{\partial V_{th}}{\partial V_{in}}\right)\right] * R_s \quad (3.50)$$

$$g_m = \frac{\mu_n C_{ox} W}{L}[V_{in} - V_{out} - V_{th}] \quad (3.51)$$

When the Rs is very large, we have the following:

$$\text{Voltage Gain } A_V = \frac{g_m R_s}{1+(g_m+g_{mb})R_s} \cong \frac{g_m}{g_{m+g_{mb}}} = \frac{1}{1+\eta} \quad (3.52)$$

It is evident that the voltage gain (Av) of SF is never equal to 1 even if the value of R1≈ ∞. Here the value of resistor R1 is chosen as 1k 50k and 100k. I_D depends heavily on the input voltage, introducing nonlinearity in the input output characteristics. So, in order to alleviate this

nonlinearity, the resistance can be replaced by a current source. The circuit of source follower is formed with a load resistance replaced with a simple MOS current source. This current source offers high resistance if it operates in saturation region [5].

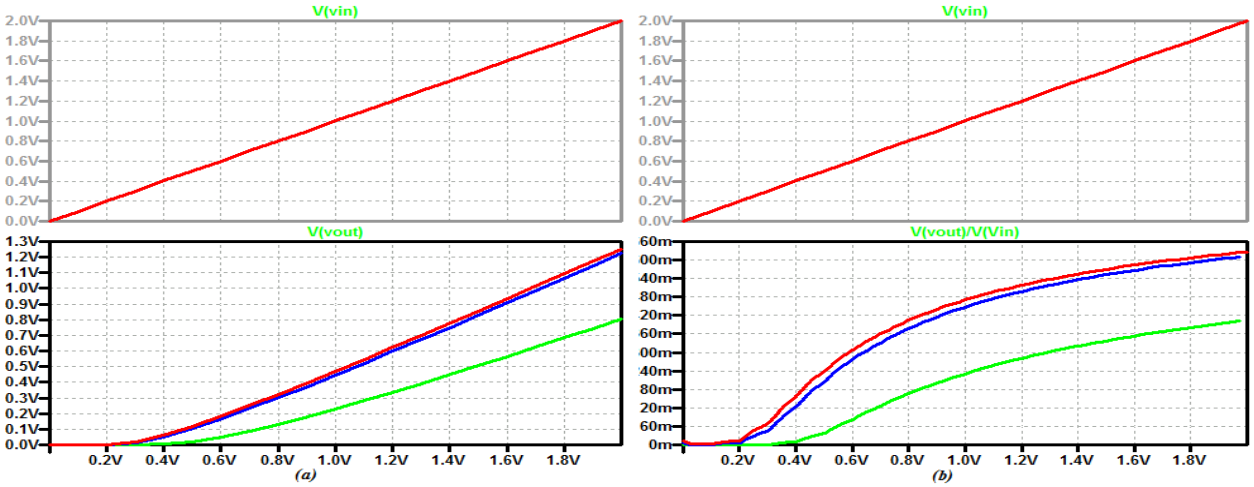


Figure 3-19 Simulation Results of Source follower (a) Output voltage for different values of Rs (b) Gain for different values of Rs

3.6.2 Flipped Voltage Follower and Folded Flipped Voltage Follower

The **"flipped voltage follower (FVF)** [10]**"** is an enhanced buffer cell widely employed for low-power and/or low voltage operation. The basic FVF cell is a modification of the source follower which gives a more precise copy of the voltage than a traditional source follower. It is basically a two-transistor source follower where the input MOSFET is forced to work at a constant dc current.

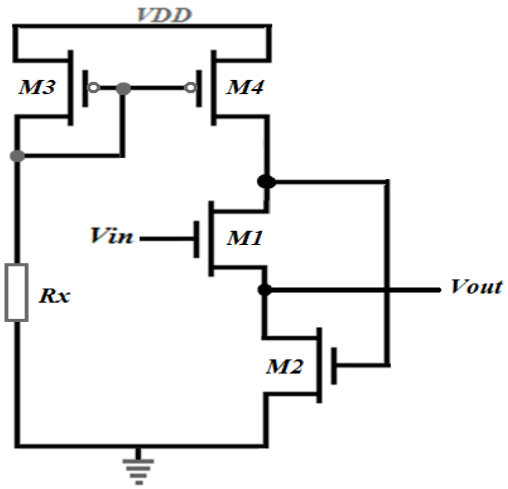


Figure 3-20 Flipped Voltage Follower Circuit

M1 and M2 are interconnected as drain to source. Gate of M1 is used as input terminal and its source as output terminal. M3 and M4 form a current mirror. The operating current is supplied by M3 and M4. The mirror current Ix is set by setting the appropriate value of Rx. M1 passes constant

current so that the incremental voltage gain is close to unity. M1 provides shunt feedback and form a two pole negative feedback loop. The output impedance of the control transistor is minimized by the feedback loop [9]. The linear region decreases with increase in Vth. For M1 to provide a constant current, M1 and M2 should be operated in linear region. Conditions for linear region of operation are

$$V_G \geq 2\sqrt{\frac{2I_x}{\mu nCox\left(\frac{W}{L}\right)}} + Vth \qquad (3.53)$$

And $V_G \leq \sqrt{\frac{2I_x}{\mu nCox\left(\frac{W}{L}\right)}} + 2Vth$ (3.54)

Or, $\Delta V_G = \text{Vth} - \sqrt{\frac{2I_x}{\mu nCox\left(\frac{W}{L}\right)}}$ (3.54)

The input and output voltage ranges are very small given by $Vth(M1) - Vds(M1)$. It has large sourcing capability thanks to the low output impedance $Ro = 1/gm2gm1ro1$. ΔVG may be unacceptably small at smaller values of Ix which causes nonlinearity

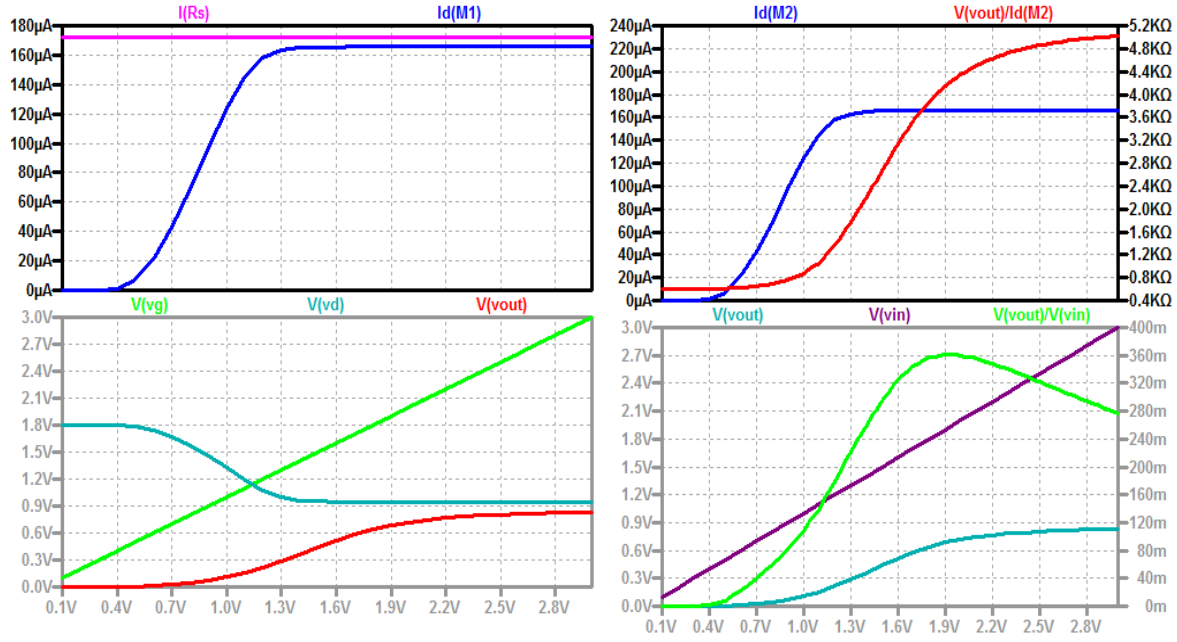


Figure 3-21 Simulation results of Flipped Voltage Follower

The direct connection of M1 and M2 of the basic FFV is replaced with a PMOS transistor M3 to form a "**folded flipped voltage follower**" (FFVF) circuit. The circuit diagram of the folded flipped voltage follower is shown in figure 3-22. M3 is also forced to operate at a constant current Iz. The current through M1 is $Iy - Iz$. The function of M3 is to keep the drain-source voltage of M1 constant at the minimum level for saturation. This can be achieved if

$$\sqrt{\frac{2Iz}{\beta p}} + |Vtp| \geq \sqrt{\frac{2(Iy-Iz)}{\beta n}} \qquad (3.55)$$

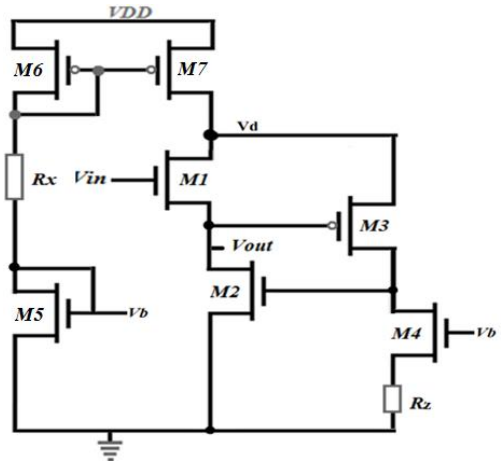


Figure 3-22 Circuit diagram of Folded Flipped Voltage follower

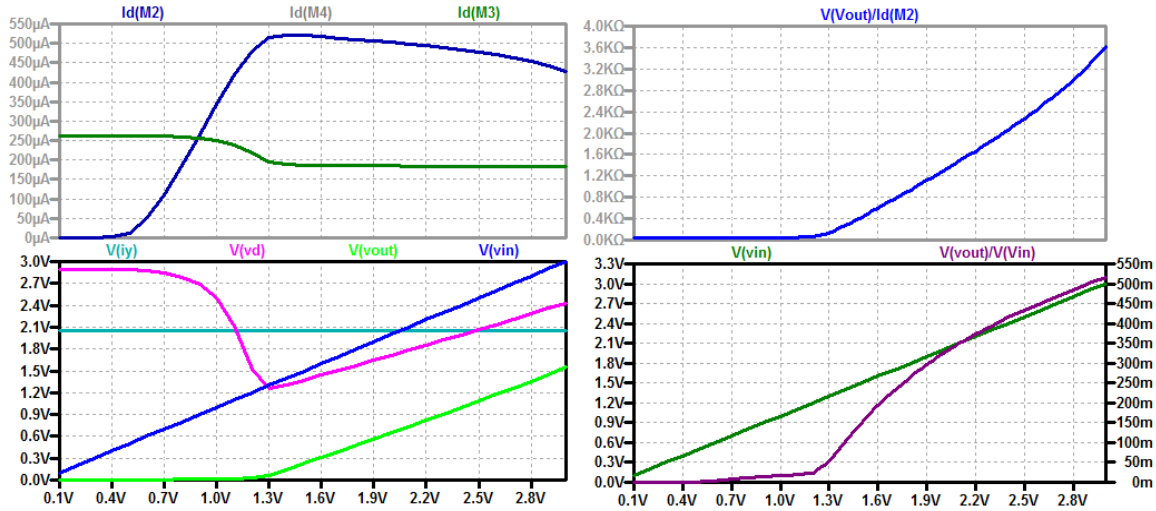


Figure 3-23 Simulation results of Folded Flipped Voltage follower

Table 3-4 Transistor and resistor sizes for FVF and FFVF

Transistors/Resistors	Size for FVF (W/L)	Size for FFVF (W/L)
M1	10µ/2µ	10µ/0.2µ
M2	10µ/2µ	10µ/0.2µ
M3	10µ/2µ	10µ/0.2µ
M4	10µ/2µ	10µ/0.2µ
M5	-	10µ/0.2µ
M6	-	10µ/0.2µ
Rx	1kΩ	2kΩ
Rz	-	0.5kΩ

The simulation results show that the FFVF gives increased gain with reduced output resistance in comparison with the FVF.

4

R-2R Ladder DAC

One of the most common building blocks for a DAC is an R-2R resistor ladder network. It uses only two values of resistors and it is in the ratio of 2:1. For an N-bit ladder DAC, it requires 2N resistors in alternate R and 2R arrangement. The R-2R ladder DAC is very popular because it is easy to design and use less components. However, it is vulnerable to glitches (voltage spikes). There are two ways in which the R-2R DAC can be used, Voltage mode or normal mode, and current mode or inverted mode.

4.1 Voltage Mode R-2R DAC

The R-2R DAC consists of R and 2R resistors, N Switches and an OPAMP. In the voltage mode R-2R ladder DAC, the arms containing 2R resistors are switched between two voltage values namely a reference voltage (VREF), and ground or a lower voltage level (VL). Also its output is taken from the end of the ladder. Since the switches operate between low impedance VREF and ground, so capacitive glitch currents does not flow to the load. The digital input determines whether each resistor is switched to the ground or to the OPAMP [11]. The output voltage is given by:

$$Vout = \frac{Vref}{2} b_{n-1} + \frac{Vref}{2^2} b_{n-2} + \cdots + \frac{Vref}{2^{n-1}} b_1 + \frac{Vref}{2^n} b_0 \qquad (4.1)$$

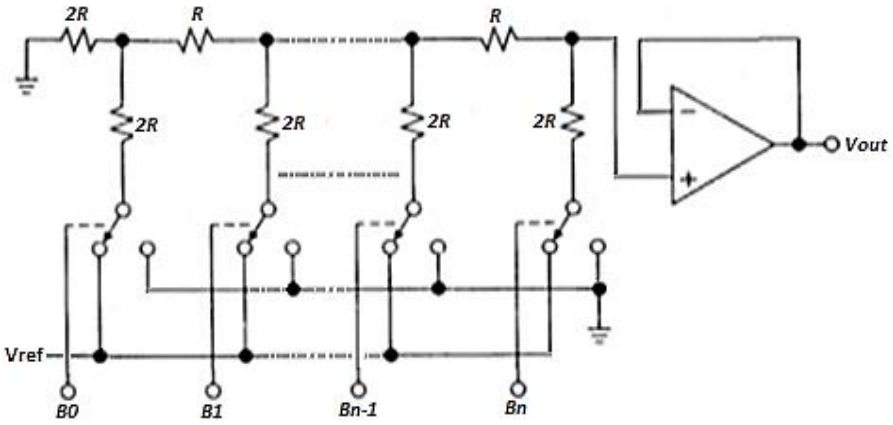
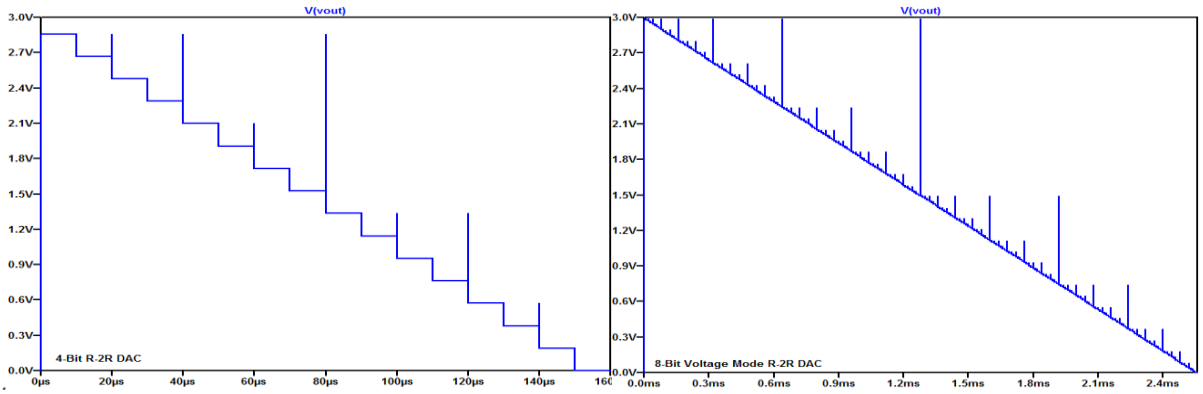


Figure 4-1 Voltage Mode R-2R DAC

The advantages of the voltage mode R-2R DAC are

- It allows interpolation between any two voltages, none of which must be zero.
- Accurate selection and design of R and 2R resistors are possible with simple construction.
- The resolution can be easily increased by just adding R-2R sections and corresponding switches.

Simulation results for 4-bit and 8-bit voltage mode DACs are shown in Figure 4-2.



(a) *(b)*

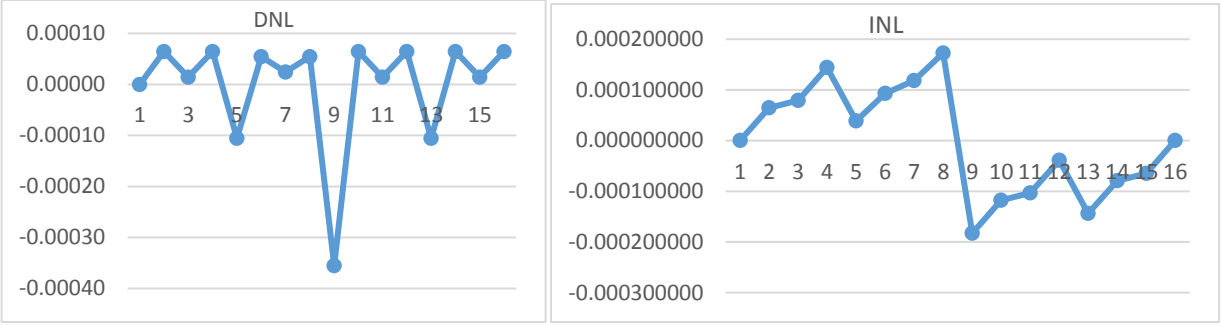
Figure 4-2 Simulation Results, (a) 4-bit R-2R DAC Output, (b) 8-bit R-2R DAC Output

The simulation results show that the output is monotonic but contains glitches. The glitch is the largest when the MSB transition occurs.

The ideal and simulated values and calculation of DNL and INL are shown in Table 4-1. The DNL and INL calculations were done using the end-point line fitting algorithm.

Table 4-1 Calculation of DNL and INL for 4-bit Voltage Mode R-2R DAC

BITS	SIMULATED	IDEAL	END POINTS LINE	DNL	INL	GLITCHES(V)
0000	0.00000	0	0.0000000000	-	0.000000000	0
0001	0.19068	0.1875	0.1906153333	0.0000647	0.000064667	0
0010	0.38131	0.375	0.3812306667	0.0000147	0.000079333	0.17859
0011	0.57199	0.5625	0.5718460000	0.0000647	0.000144000	0
0100	0.76250	0.75	0.7624613333	-0.0001053	0.000038667	0.55
0101	0.95317	0.9375	0.9530766667	0.0000547	0.000093333	0
0110	1.14381	1.125	1.1436920000	0.0000247	0.000118000	0.16869
0111	1.33448	1.3125	1.3343073333	0.0000547	0.000172667	0
1000	1.52474	1.5	1.5249226667	-0.0003553	-0.000182667	1.28776
1001	1.71542	1.6875	1.7155380000	0.0000647	-0.000118000	0
1010	1.90605	1.875	1.9061533333	0.0000147	-0.000103333	0.90645
1011	2.09673	2.0625	2.0967686667	0.0000647	-0.000038667	0
1100	2.28724	2.25	2.2873840000	-0.0001053	-0.000144000	0.52526
1101	2.47792	2.4375	2.4779993333	0.0000647	-0.000079333	0
1110	2.66855	2.625	2.6686146667	0.0000147	-0.000064667	0.14395
1111	2.85923	2.8125	2.8592300000	0.0000647	0.000000000	0



(a) *(b)*

Figure 4-3 (a) Differential Non-Linearity (b) Integral Non-Linearity of Voltage Mode R-2R Ladder DAC

The maximum DNL was found to be 0.000339252 and the minimum DNL was found to be -0.001864138. The maximum INL is 0.000905838 and the minimum INL is calculated to be -0.0009583. DNL and INL plots are shown in Figure 4-3.

4.2 MOSFET Only Voltage Mode R-2R DAC

The voltage mode R-2R DAC was implemented by using MOSFETs only in order to be implemented in IC technology. The switch is a SPST switch and was realized by using two cascaded inverters. The MOSFETs aspect ratio for R and 2R were calculated using equation 4.2.

$$R = \frac{V_{DS}}{Id_{SAT}} = \frac{V_{DS}}{\frac{u_n C_{ox}}{2} \times \left(\frac{W}{L}\right) \times (V_{GS} - V_{TH})^2} \qquad (4\text{-}2)$$

The aspect ratio for R was calculated to be L=2u W=1.2u. 2R is just the series combination of two MOSFETs with the values of R. The MOSFETs used for R and 2R are NMOS types. Figure 4-4 shows the schematics of MOSFET only voltage mode R-2R DAC. The 4-bit and 8-bit MOSFET only R-2R DACs were simulated and it was found out that the 8-bit DAC was non-monotonic and both DACs contain glitches. The glitches are due to the difference in switching, and the major glitch that occurs at the midway of the output signal is due to the switching of MSB since all the bits change at this position. So do the switches. Figure 4-5 shows the simulation results of the 4-bit and 8-bit MOSFET only voltage mode R-2R ladder DACs.

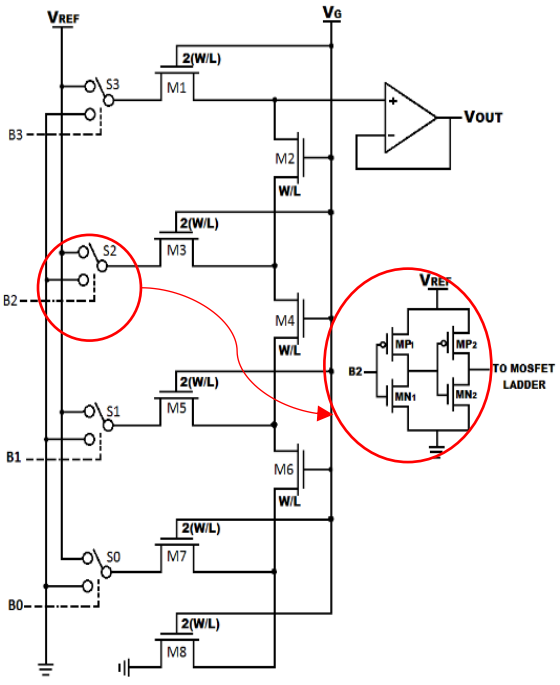
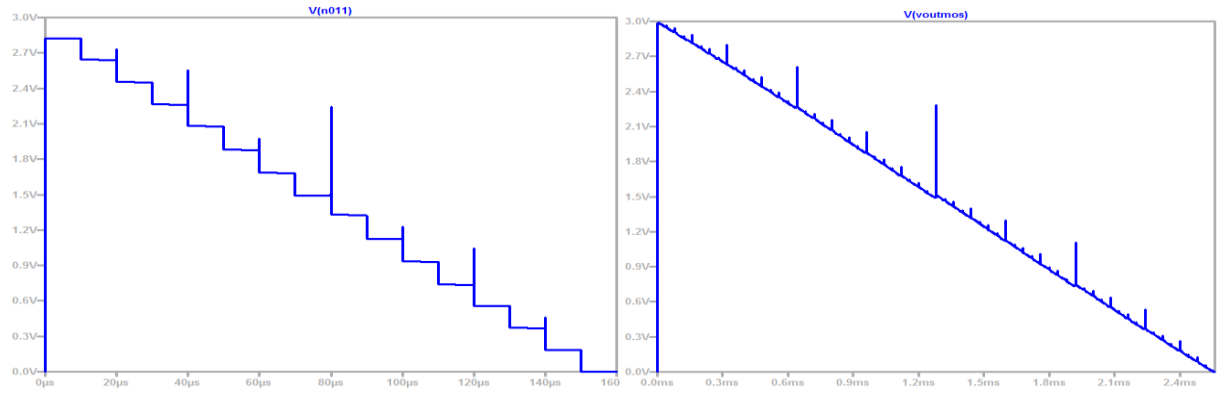


Figure 4-4 MOSFET Only Voltage Mode R-2R DAC



.(a) *(b)*

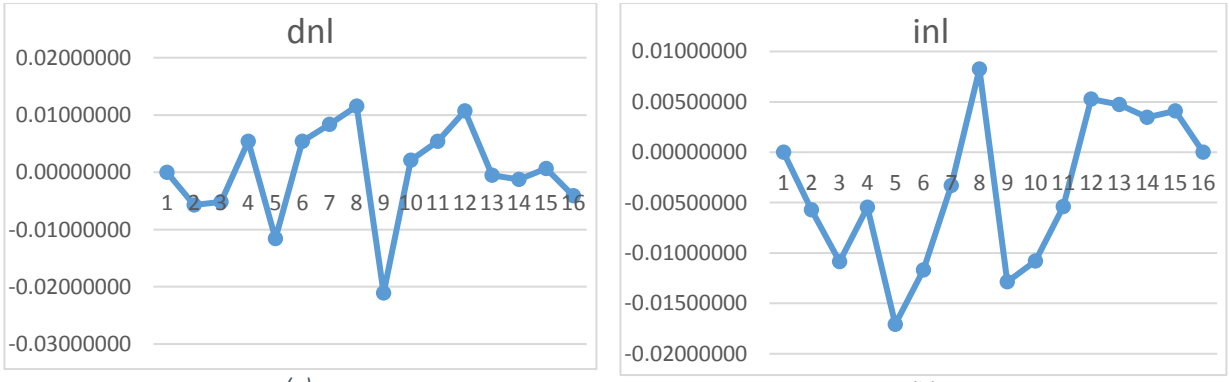
Figure 4-5 Simulation Results, (a) 4-bit R-2R DAC Output, (b) 8-bit R-2R DAC Output

The Table 4.2 shows the DNL and INL calculations for this DAC.

Table 4-2 Calculation of DNL and INL for MOSFET Only 4-bit Voltage Mode R-2R DAC

BITS	SIMULATED(VA)	IDEAL(VI)	END POINTS LINE	DNL	INL
0000	-6.869329E-07	0	-0.0000006869	-	0.00000000
0001	0.1823497	0.1875	0.1880515122	-0.00570181	-0.00570181
0010	0.36523821	0.375	0.3761037113	-0.00516369	-0.01086550
0011	0.55869652	0.5625	0.5641559105	0.00540611	-0.00545939
0100	0.73513517	0.75	0.7522081096	-0.01161355	-0.01707294
0101	0.9285794	0.9375	0.9402603087	0.00539203	-0.01168091
0110	1.1250138	1.125	1.1283125078	0.00838220	-0.00329871
0111	1.3246123	1.3125	1.3163647070	0.01154630	0.00824759
1000	1.4915565	1.5	1.5044169061	-0.02110800	-0.01286041
1001	1.681682	1.6875	1.6924691052	0.00207330	-0.01078711
1010	1.8751226	1.875	1.8805213044	0.00538840	-0.00539870
1011	2.0738546	2.0625	2.0685735035	0.01067980	0.00528110
1100	2.2613586	2.25	2.2566257026	-0.00054820	0.00473290
1101	2.4481521	2.4375	2.4446779017	-0.00125870	0.00347420
1110	2.6368409	2.625	2.6327301009	0.00063660	0.00411080
1111	2.8207823	2.8125	2.8207823000	-0.00411080	0.00000000

The maximum DNL was found to be 0.01154 and the minimum DNL was found to be -0.021108. The maximum INL is 0.0082475 and the minimum INL is calculated to be -0.01707. The plots of DNL and INL are shown in Figure 4-6.



(a) *(b)*

Figure 4-6 (a) Differential Non-Linearity (b) Integral Non-Linearity of Voltage Mode R-2R Ladder DAC

4.3 Current Mode R-2R DAC

As the name suggests, the current mode DAC operates on the ladder currents. The ladder is formed by R in the series path and 2R in the shunt path. The reference current IREF is divided into i1, i2…..iN in each arm. Currents through 2R resistors are of binary weight relationship. These currents are either diverted to the ground or to the inverting terminal of an OPAMP. The output voltage is given by:

$$Vout = -i_{tot} \times Rf \qquad (4.3)$$

Where,

$$i_{tot} = \sum_{K=0}^{N-1} \frac{B_K \times Vref}{2^{N-K}} \times \frac{1}{2R} \qquad (4.4)$$

The advantages of current mode R-2R DACs are

- The voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler.
- The stray capacitance does not affect the speed of response of the circuit due to constant ladder node voltages. So this improves speed performance.

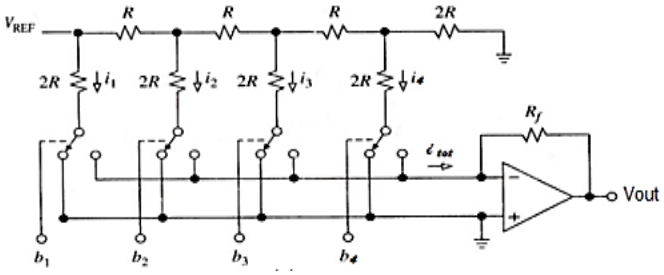
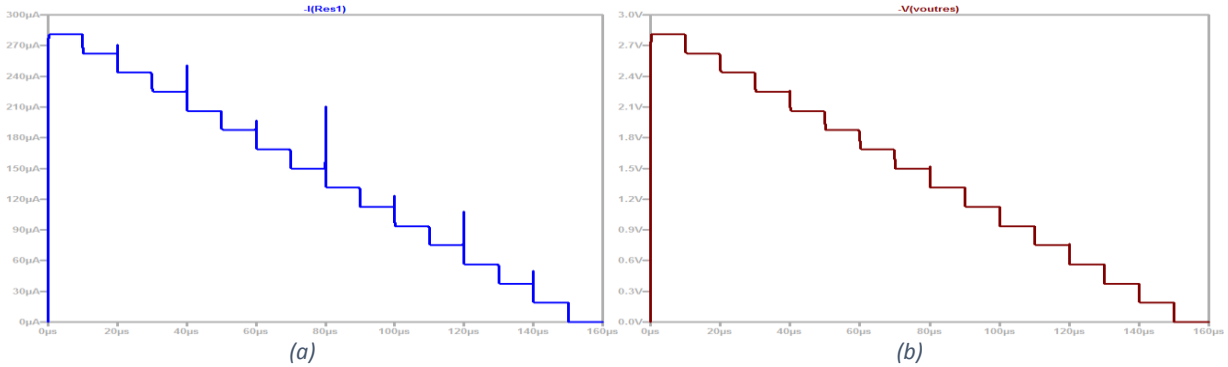


Figure 4-7 Current Mode R-2R DAC

The current steering mode R-2R DAC for 4-bit was simulated, and the simulation results for current output and voltage output are shown in Figure 4-8. Table 4-3 shows the calculation of DNL and INL using the end-point line fitting algorithm.



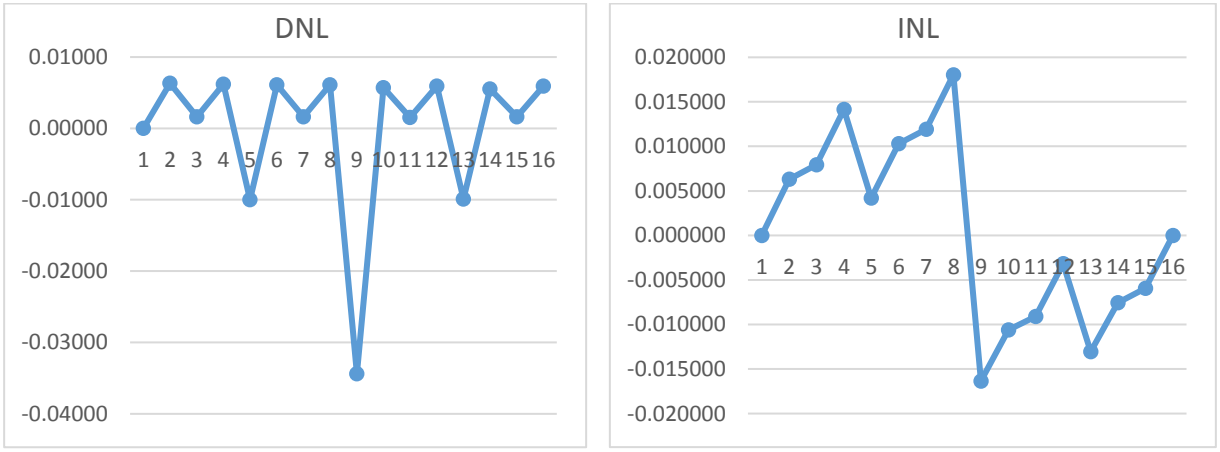
(a) *(b)*

Figure 4-8 Simulation Results of Current Mode R-2R DAC (a) Current Output (b) Voltage Output

Table 4-3 Calculation of DNL and INL for 4-bit Current Mode R-2R DAC

BITS	SIMULATED(µA)	IDEAL(µA)	END POINT LINE	DNL	INL	GLITCHES(µA)
0000	0	0	0.00000	0.00000	0.000000	0
0001	18.7489	18.75	18.74258	0.00632	0.006320	0
0010	37.4931	37.5	37.48516	0.00162	0.007940	8.6920137
0011	56.2419	56.25	56.22774	0.00622	0.014160	0
0100	74.9745	75	74.97032	-0.00998	0.004180	25.985087
0101	93.7232	93.75	93.71290	0.00612	0.010300	0
0110	112.4674	112.5	112.45548	0.00162	0.011920	9.4727004
0111	131.2161	131.25	131.19806	0.00612	0.018040	0
1000	149.9243	150	149.94064	-0.03438	-0.016340	60.76954
1001	168.6726	168.75	168.68322	0.00572	-0.010620	0
1010	187.4167	187.5	187.42580	0.00152	-0.009100	11.161406
1011	206.1652	206.25	206.16838	0.00592	-0.003180	0
1100	224.8979	225	224.91096	-0.00988	-0.013060	33.415006
1101	243.646	243.75	243.65354	0.00552	-0.007540	0
1110	262.3902	262.5	262.39612	0.00162	-0.005920	12.488973
1111	281.1387	281.25	281.13870	0.00592	0.000000	0

The maximum DNL was found to be 0.00632 and the minimum DNL was found to be -0.03438. The maximum INL is 0.01804 and the minimum INL is calculated to be -0.01634. The plots of DNL and INL are shown in Figure 4-9.



(a) *(b)*

Figure 4-9 (a) Differential Non-Linearity (b) Integral Non-Linearity of 4-Bit Current Mode R-2R Ladder DAC

4.4 MOSFET Only Current Mode R-2R DAC

An important task that has to be performed inside a DAC is accurate weighing of currents, voltages or charges. Typically, passive elements such as resistors and capacitors are used for this purpose because of their linear characteristics. The MOSFETs are inherently non-linear in all the operating

regions. The R-2R ladder DAC relies on the linearity of the passive elements that divides the input current by the factor of two.

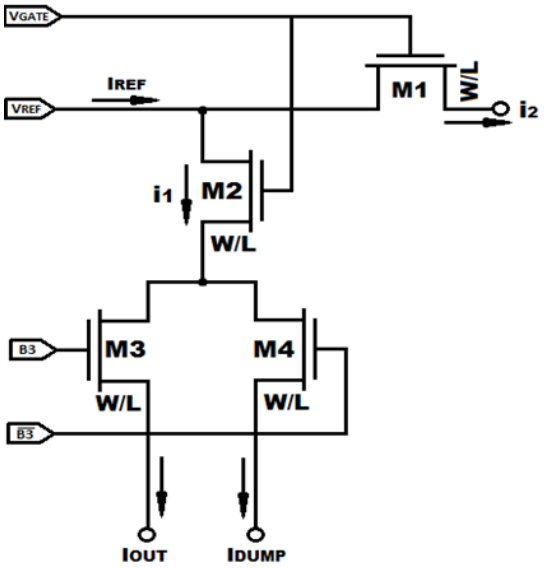


Figure 4-10 Current Division Principle Using MOSFETs

This current division can be accomplished by using MOSFETs despite their non-linear characteristics. The current mode DAC works based on the current division principle. The current division using MOS transistors is shown in the unit cell of the ladder network in Figure 4-10. Here, M1 acts as resistor R. The combination of M2 and M3 or M2 and M4 contributes the resistor 2R. The input current IREF gets divided by M1 and M2 into two parts one part goes through M1 and other goes through M2 [12]. The current in M2 is switched to IOUT by M3 or to IDUMP by M4. M16 and M17 form the terminal 2R resistor. The full 4-bit resolution of MOSFET only R-2R ladder DAC is obtained by cascading this cell as shown in Figure 4-11. The MOSFETs aspect ratio is calculated using the equation 4.5.

$$R = \frac{V_{DS}}{Id_{SAT}} = \frac{V_{DS}}{\frac{u_n C_{ox}}{2} \times \left(\frac{W}{L}\right) \times (V_{GS} - V_{TH})^2} \qquad (4.5)$$

The calculated values of W and L for MOSFETs are 1.29µ and 2.1µ respectively.

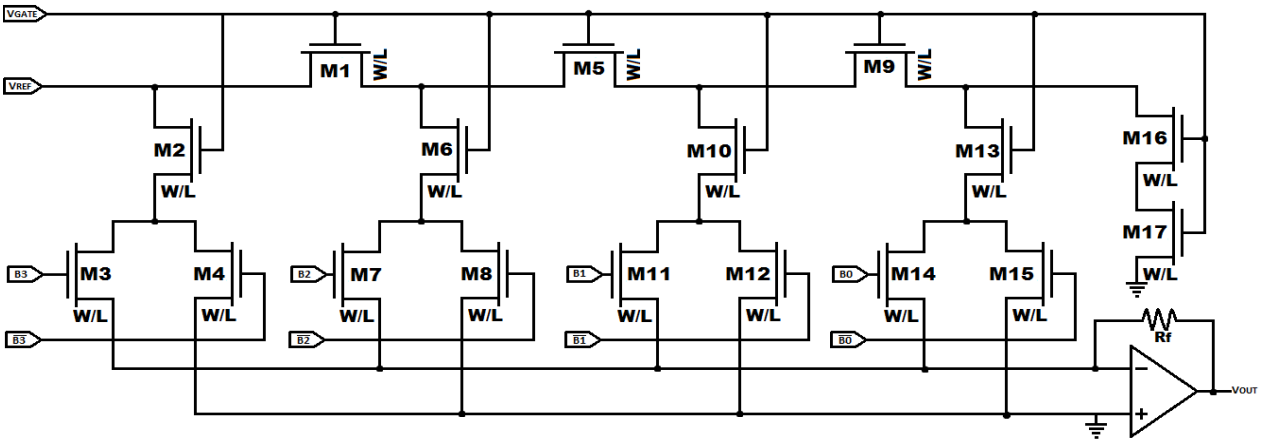
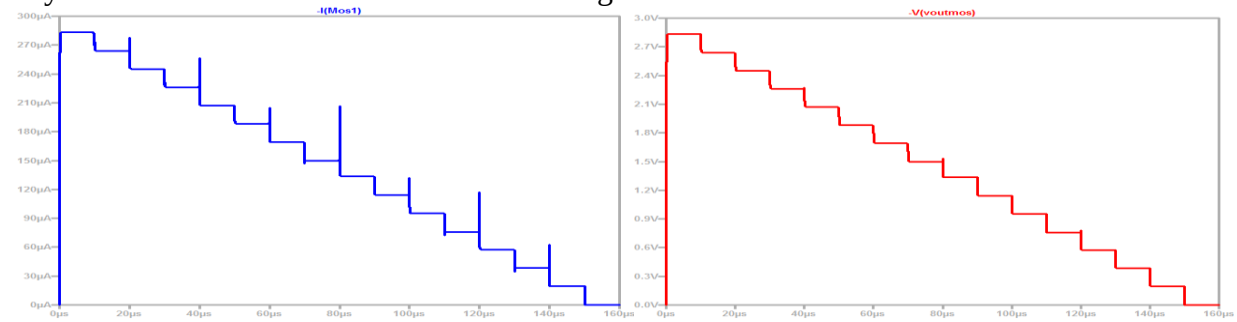


Figure 4-11 4 bit MOSFET only Current Mode R-2R DAC

The simulation was carried out using V_{REF}=3V and the current and voltage outputs of the MOSFET only current mode R-2R DAC are shown in Figure 4-12.



(a) *(b)*

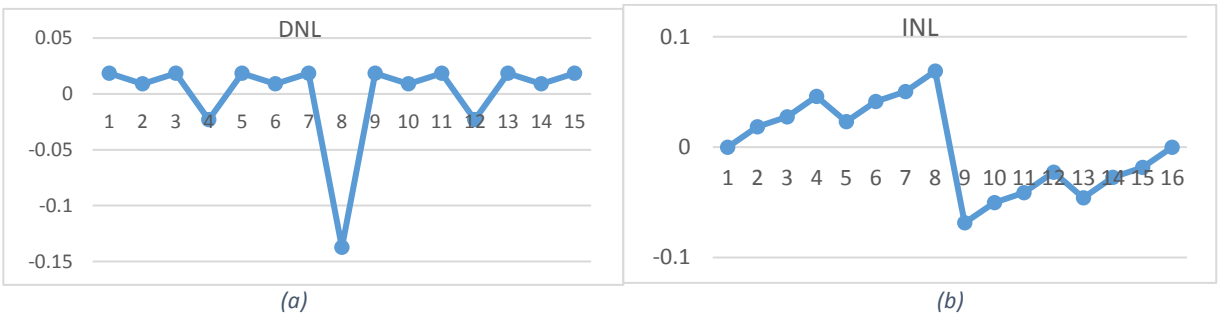
Figure 4-12 Simulation Results of 4-bit MOSFET only Current Mode R-2R DAC (a) Current Output (b) Voltage Output

Table 4-4 shows the calculations of DNL and INL for the MOSFET only current mode R-2R DAC.

Table 4-4 Calculations of DNL and INL for MOSFET only Current Mode R-2R DAC

BITS	SIMULATED(VA)	IDEAL(VI)	CORRECTED VALUES	DNL	INL
0000	0	0	0	-	0
0001	19.2324	18.75	19.0973301	0.018524	0.018524
0010	38.2832	37.5	38.01433559	0.008907	0.027431
0011	57.5153	56.25	57.11136779	0.018508	0.04594
0100	75.9631	75	75.42960817	-0.02303	0.022912
0101	95.1948	93.75	94.52624319	0.018487	0.0414
0110	114.2457	112.5	113.443348	0.008912	0.050312
0111	133.4776	131.25	132.5401816	0.018498	0.06881
1000	149.7654	150	148.7135917	-0.13742	-0.06861
1001	168.9964	168.75	167.8095317	0.01845	-0.05016
1010	188.047	187.5	186.7263386	0.008896	-0.04126
1011	207.2783	206.25	205.8225764	0.018466	-0.0228
1100	225.7265	225	224.1412139	-0.02301	-0.0458
1101	244.9571	243.75	243.2367567	0.018429	-0.02737
1110	264.0079	262.5	262.1537622	0.008907	-0.01847
1111	283.2392	281.25	281.25	0.018466	0

The maximum DNL was found to be 0.018498 and the minimum DNL was found to be -0.13742. The maximum INL is 0.06881and the minimum INL is calculated to be -0.06861. The plots of DNL and INL are shown in Figure 4-13.



(a) (b)

Figure 4-13 (a) Differential Non-Linearity (b) Integral Non-Linearity of MOSFET Only 4-Bit Current Mode R-2R Ladder DAC

Here from the above design and calculations, we conclude that the R-2R DAC has decent DNL and INL results. However, these DACs are prone to glitches. The glitches are further increased in higher resolution DACs. This is the main drawback of this type of DACs.

5

Purposed Gray Code Input DAC Architectures

We found in Chapter 4 that the R-2R DAC produces glitches. Be it in case of the voltage mode R-2R DAC or current mode R-2R DAC. Generally, DACs employing binary codes as input are prone to glitches. These glitches can be removed by using various kinds of reconstruction filters. But it also comes with a disadvantage of taking more space in IC, and requires more components and increases the cost of PCB. Hence, glitch reduction technique should be employed within the DAC. One of the methods is using Gray code input DAC which uses only one switch transition at a time. Since it is considered that Gray code input DAC is difficult to realize, this chapter attempts to show that it is possible to design it. The following text describes different terms related to Gray code input DAC design.

5.1 Number system

Number system is simply a way of expression of numbers. It is a mathematical notation of numbers using digits or other symbols in a consistent manner. There are different types of number system some of them are as follows.

- Decimal number system (Base- 10)
- Binary number system (Base- 2)
- Octal number system (Base-8)
- Hexadecimal number system (Base- 16)

5.1.1 Binary Number system

Binary code has been used in electronic circuits for a very long time. Numbers can be encoded in binary format and stored using switches. The digital technology which uses this system could be

a computer, calculator, digital TV decoder box, cell phone, burglar alarm, watch, etc. Values are stored in binary format in memory, which is basically a bunch of electronic on/off switches. Each switch could represent 1 or 0 depending on whether it is turned on or off. In the DAC, the binary number system is used to turn the switches on or off for a particular voltage level. While using the binary number system in the DAC, multiple bits change at a time which trigger multiple switches at once. This property of the binary code has advantages in some cases and disadvantages in others. Disadvantage is that when multiple switches are triggered at once, there is a possibility of spurious and glitch output. There are some variations of the binary number system among which Gray code is one code, which has an interesting property.

5.1.2 Gray Code

Gray code is a binary numeral system where the adjacent values differ in only one bit change. It is named after Frank Gray and is also known as Reflected Binary Code (RBC). It was originally designed to prevent spurious output from electromechanical switches. Bell Labs researcher Frank Gray introduced the term reflected binary code in his 1947 patent application, remarking that the code had no recognized name. He derived the name from the fact that it "may be built up from the conventional binary code by a sort of reflection process [13].

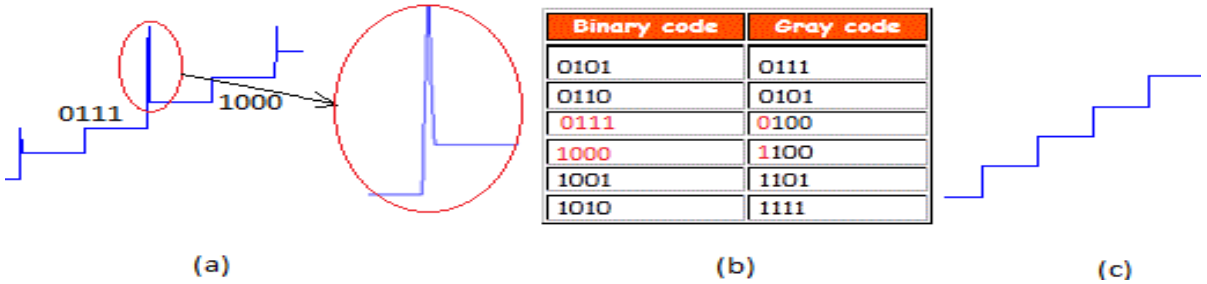
Table 5-1 Binary code and Gray code

DECIMAL	BINARY CODE	GRAY CODE
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

This code was later named after frank Gray by the people who used it. The Gray code is also termed as minimum error code and cyclic permutation code. Devices indicate position by opening and closing of switches. If a device is using binary code, regardless of positions 3 and 4 being

next to each other, every single bit changes its state. Physical switches are not ideal, so devices using binary codes, the problem of synchronicity between switches arises. It is unlikely that physical switches will change states exactly in synchrony. In the above shown states 3 and 4, all the three switches change its state in a brief period. During this period the switches will read some unwanted positions even without a key press and the transition will look like 011 — 001 — 101 — 100. Hence the observer cannot verify whether it is a transitional position or the real position. If this output is fed into a sequential logic or a combinational logic, then the system may store a false value.

But this is not true in case of Gray code. The Gray code solves this problem by changing only one switch at a time so there is no occurrence of ambiguity of position. For example, in case of the DAC, where natural binary codes are used, glitches tend to occur during the transition of MSBs. As multiple switches change their states from ON to OFF or OFF to ON, glitches appear during this transition. But the DAC using Gray code does not go through this problem as only a single switch change its state at a time. The glitches in binary code and glitch free Gray code DAC output are shown in Figure 5-1.



Binary code	Gray code
0101	0111
0110	0101
0111	0100
1000	1100
1001	1101
1010	1111

Figure 5-1 (a): Glitch Due to MSB change in R-2R DAC (b) Comparison of switching of Binary code and Gray code. (c) Gray code input DAC performance

We can see from Figure 5-1 (b) that the transition from 7 to 8 all the bits gets changed in case of binary code, but for Gray code, only the MSB gets changed. The result is switching of all 4 bits in binary, but only one in case of Gray code. This helps in minimizing or eliminating glitches in case of the Gray code input DAC.

5.2 Glitches

When designing a DAC, we expect the output to move from one value to the next monotonically, but real circuits do not always behave that way. It is not uncommon to see overshooting or

undershooting, quantified as glitch impulse, across certain code ranges. These impulses can appear in one of two forms as shown in Figure 5-2.

The Glitches in DAC occur mainly due to

- Capacitive coupling
- Differences in how fast the switches open and close

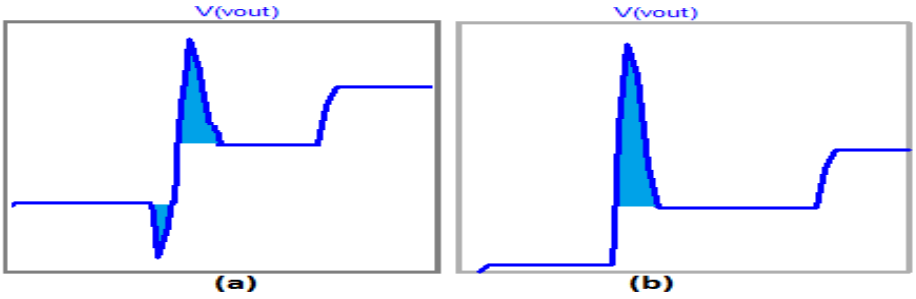


Figure 5-2 Glitches in DAC (a) two lobe Glitch (b) single lobe glitch

Typically, the glitch behaviour is dominated by the differences between the switching. Unlike capacitive coupling, which often leads to both positive and negative spikes, the glitch due to the switches is usually unipolar, meaning there is one voltage spike that is either positive or negative, not both. The area of the glitch spikes is often used as an estimate of the DAC glitch performance, and is sometimes referred to as glitch energy, although the correct unit is volt-seconds. The switching of the MSB causes most significant glitches [14]. For example, for a 4-bit DAC, binary code transitions of 0111 to 1000 or 1000 to 0111 cause major glitches in the D/A conversion. The glitch is caused due to number of switches changing their states at once.

In precision systems, these glitches can have serious drawbacks. Since the glitches are of higher voltage level than that of the required output, the system may read erroneous values. This may result in deterioration of pictures, videos or audio. In addition, when the output of DAC is to be written in memory or is used somewhere else, ambiguous data are written or the other devices may not respond according to the desired way.

5.3 Gray Code Input DAC Architecture

Little research has been done in this topic i.e. DAC architecture with Gray code input. There is one patent and some academic papers that utilize Gray code in some way, but they are application specific. The patent in [1] dates back to 1986, and has expired by now, so the topologies described in patent are free to be used. Because of the little attention that has been devoted to this topic, this

work seeks to explore the Gray code DAC and discover if it is an efficient method to eliminate glitches. We attempt to design and implement it with active elements.

Construction of Gray code DAC architectures involves in designing a current/voltage switch matrix, which is the main component to distinguish between the binary code input DAC architecture and Gray code input DAC architectures. Two architectures of the Gray code input DAC are designed and simulated, namely voltage mode Gray code input DAC (VMGCI DAC) and current mode Gray code input DAC (CMGCI DAC). Both are designed using passive elements as well as with MOSFETs.

5.3.1 Voltage Mode Gray Code Input DAC (VMGCI DAC)

The R-2R ladder network is the simplest form of DAC to build. So, by modifying it to take Gray code as input can lead to an architecture as we purposed. First terminal IN1 is supplied with a reference voltage (Vref) and the second input terminal IN2 is connected to the ground. The terminal X0 is connected to R-2R network and the other parts are completed as shown in Figure 5-6. The CTL signal is provided with the Gray code of the input signal. The end terminals are terminated by a combination of 1.5R and 0.5R resistors [1]. The first stage is termed as the Most Significant Bit (MSB) stage where the MSB of Gray code is applied to the CTL pin of the first switch S3. The last stage with combination of 1.5R and 0.5R resistors is the Least Significant Stage (LSB) where the LSB of Gray code G0 is applied to the CTL Pin of the switch S0. The output voltage is taken from the voltage follower configuration of the OPAMP.

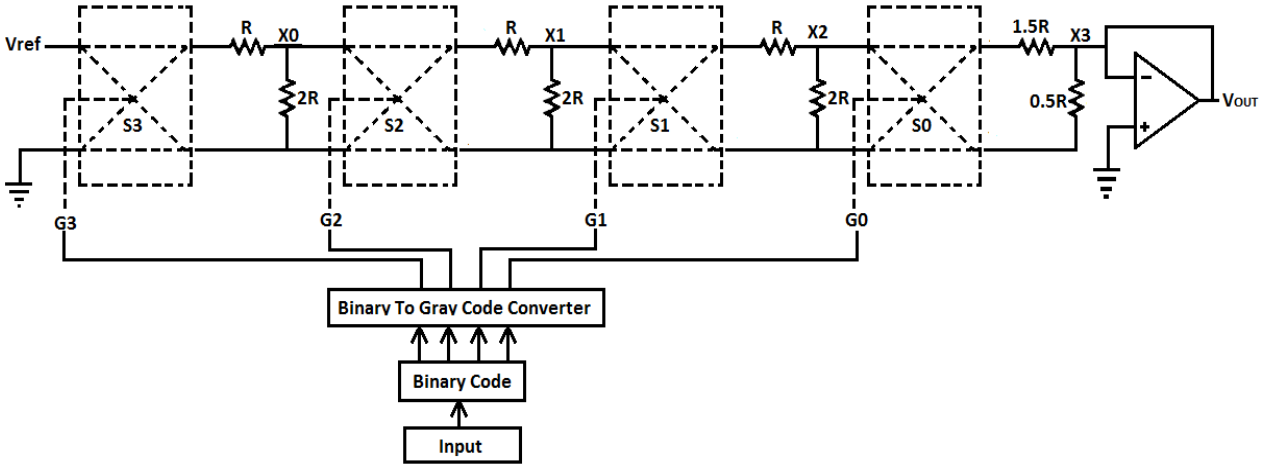


Figure 5-3 VMGCI DAC Architecture

5.3.1.1 Working Principle of VMGCI DAC

The input is converted into binary code and this binary code is converted to Gray code via the binary to Gray code converter. The converted Gray code is fed to corresponding switch CTL pins G3, G2, G1, G0. The resistor ladder performs a binary weighted voltage division at each stage. The voltage at X0 is VREF/2, X1 is VREF/4, X2 is VREF/8 and X3 is VREF/32.

When every Gray code bit is zero i.e. for Gray code 0000 every switch remains parallel. So the output is

$$Vout[0000] = \frac{VREF}{32} \quad \ldots \qquad (5.1)$$

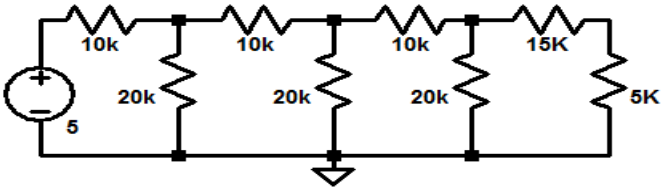


Figure 5-4 Configuration of Ladder Network when Gray Code is 0000

When G0 is 1 and all other bits are zero, if Gray code 0001, the switch S0 is crossed and other switches remain parallel. Hence the output is

$$Vout[0001] = \frac{VREF}{16} + \frac{VREF}{32} \quad \ldots. \qquad (5.2)$$

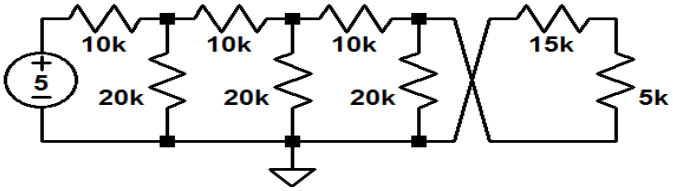


Figure 5-5 Configuration of the Ladder Network when Gray Code is 0001

Similarly, when G1 is 1 and all other bits are zero, i.e. Gray code 0010, S1 is crossed and other switches remain parallel, the output becomes,

$$Vout[0010] = \frac{VREF}{8} + \frac{VREF}{16} + \frac{VREF}{32} \quad \ldots. \qquad (5.3)$$

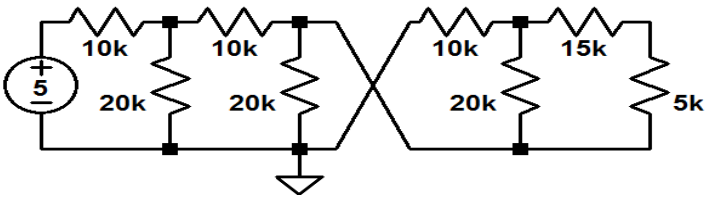


Figure 5-6 Configuration of Ladder Network when Gray Code is 0010

When G2 is 1 and all the other bits are zero, i.e. Gray code 0100, S2 is crossed and all other switches remain parallel, the output becomes,

$$Vout[0100] = \frac{VREF}{4} + \frac{VREF}{8} + \frac{VREF}{16} + \frac{VREF}{32} \ldots. \quad (5.4)$$

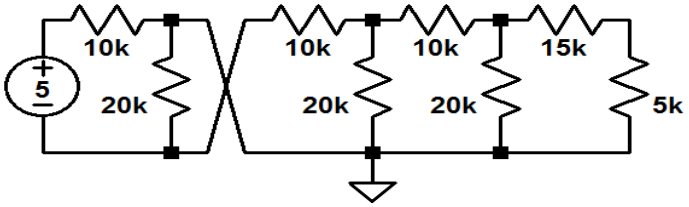


Figure 5-7 Configuration of Ladder Network when Gray Code is 0100

When G3 is 1 and all other bits are zero, i.e. Gray code 1000, S3 is crossed and all the other switches remain parallel, the output becomes,

$$Vout[1000] = \frac{VREF}{2} + \frac{VREF}{4} + \frac{VREF}{8} + \frac{VREF}{16} + \frac{VREF}{32} \quad (5.5)$$

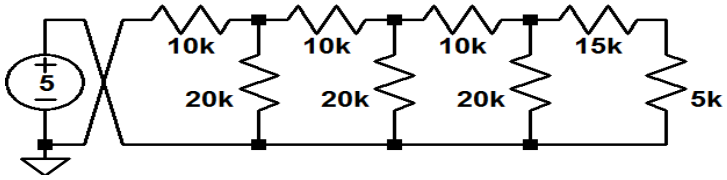


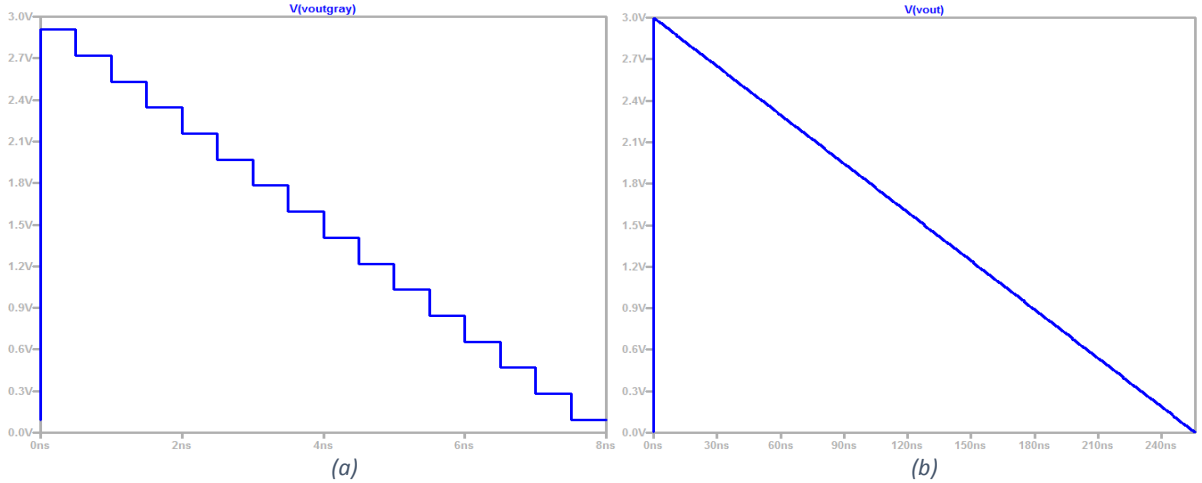
Figure 5-8 Configuration of Ladder Network when Gray Code is 1000

The general output is given by

$$Vout = \frac{VREF}{2^{N+1}} |2 * i - 1| \quad (5.6)$$

Where N=number of bits, and i=1, 2, 3…2^{N+1}

5.3.1.2 Simulation Results and Calculations of Errors



(a) *(b)*

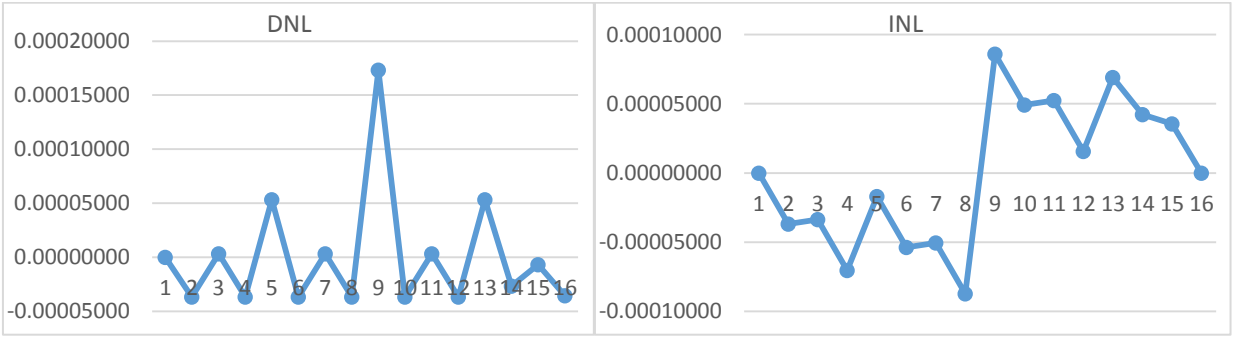
Figure 5-9 Simulation Results, (a) 4-bit Gray Code Input DAC (b) 8-bit Gray Code Input

DNL and INL calculations are based on the end-point line fit algorithm and shown in Table 5-2.

Table 5-2 Calculations of DNL and INL for VMGCI DAC

GRAY CODE	Vout	SIMULATED	IDEAL	END POINT LINE	DNL	INL
0000	VREF/32	0.09400	0.09375	0.094	0.00000000	0.00000000
0001	(3VREF)/32	0.28143	0.28125	0.281466753	-0.00003675	-0.00003675
0011	(5 VREF)/32	0.46890	0.46875	0.468933507	0.00000325	-0.00003351
0010	(7 VREF)/32	0.65633	0.65625	0.65640026	-0.00003675	-0.00007026
0110	(9 VREF) /32	0.84385	0.84375	0.843867013	0.00005325	-0.00001701
0111	(11 VREF)/32	1.03128	1.03125	1.031333767	-0.00003675	-0.00005377
0101	(13 VREF) /32	1.21875	1.21875	1.21880052	0.00000325	-0.00005052
0100	(15 VREF) /32	1.40618	1.40625	1.406267273	-0.00003675	-0.00008727
1100	(17 VREF) /32	1.59382	1.59375	1.593734027	0.00017325	0.00008597
1101	(19 VREF) /32	1.78125	1.78125	1.78120078	-0.00003675	0.00004922
1111	(21 VREF) /32	1.96872	1.96875	1.968667533	0.00000325	0.00005247
1110	(23 VREF) /32	2.15615	2.15625	2.156134287	-0.00003675	0.00001571
1010	(25 VREF) /32	2.34367	2.34375	2.34360104	0.00005325	0.00006896
1011	(27 VREF) /32	2.53111	2.53125	2.531067793	-0.00002675	0.00004221
1001	(29 VREF) /32	2.71857	2.71875	2.718534547	-0.00000675	0.00003545
1000	(31 VREF) /32	2.90624	2.90625	2.9060013	-0.00003545	0.00000000

The maximum INL was found to be 0.00008597 and the minimum INL was found to be -0.00008727. The maximum DNL is 0.00017325 and the minimum DNL is calculated to be -0.00003675. The plots of DNL and INL are shown in Figure 5-10.



(a) *(b)*

Figure 5-10 (a) Differential Non-Linearity (b) Integral Non-Linearity of 4-Bit VMGCI DAC

5.3.2 MOSFET Only VMGCI DAC

MOSFET implementation of the VMGCI DAC is simply the change of resistors to MOSFETs and is depicted in Figure 5-11. The values of R for MOSFETs are calculated by the equation for MOSFETs in saturation region.

$$R = \frac{V_{DS}}{Id_{SAT}} = \frac{V_{DS}}{\frac{u_n C_{ox}}{2} \times \left(\frac{W}{L}\right) \times (V_{GS} - V_{TH})^2}$$

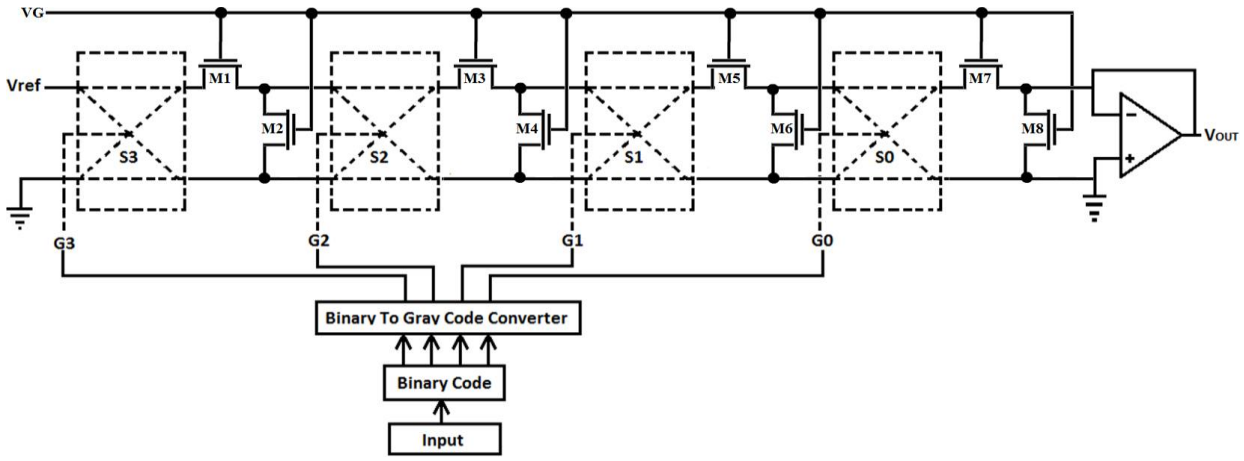


Figure 5-11 Design of MOSFET only VMGCI DAC

The comparison of simulation results for R-2R ladder DAC and MOS only Gray code DAC for both 4-bit and 8bit DAC is shown in figure 5-12. From the simulation results, we can see that the Gray code version of MOS only DAC is also affected by glitches, but as we compare with R-2R DAC, the glitches are much smaller.

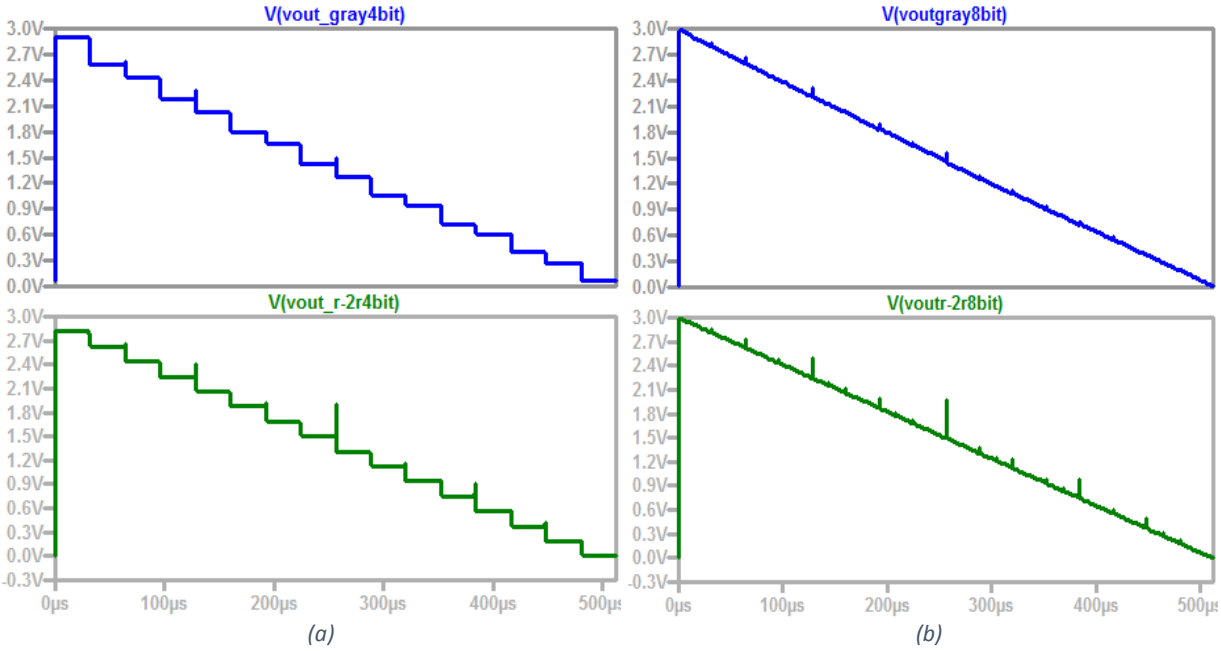


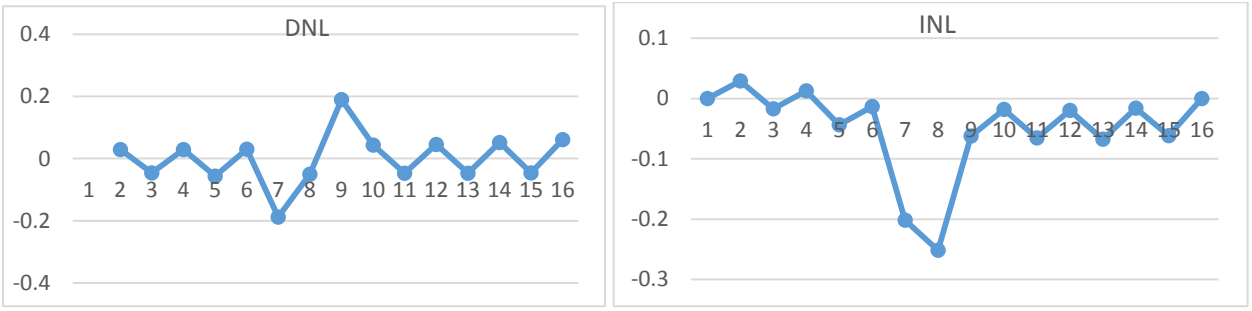
Figure 5-12 Comparison of Simulation Results of (a) 4-bit Gray Code and 4-bit R-2R DAC (b) 8 bit Gray Code and 8-bit R-2R DAC

Table 5-3 shows the ideal, simulated values of output and the calculated values of DNL and INL for MOSFET only VMGCI DAC.

Table 5-3 calculated values of DNL and INL for MOSFET only VMGCI DAC

GRAY CODE	VOUT	SIMULATED	IDEAL	END POINT LINE	DNL	INL
0000	VREF/32	0.07796154	0.09375	0.07796154	-	0
0001	(3VREF)/32	0.29628298	0.28125	0.267477477	0.028805503	0.028805503
0011	(5 VREF)/32	0.44004473	0.46875	0.456993415	-0.045754187	-0.016948685
0010	(7 VREF)/32	0.65889853	0.65625	0.646509352	0.029337863	0.012389178
0110	(9 VREF) /32	0.79246	0.84375	0.836025289	-0.055954467	-0.043565289
0111	(11 VREF)/32	1.01224	1.03125	1.025541227	0.030264063	-0.013301227
0101	(13 VREF) /32	1.0136312	1.21875	1.215057164	-0.188124737	-0.201425964
0100	(15 VREF) /32	1.1530998	1.40625	1.404573101	-0.050047337	-0.251473301
1100	(17 VREF) /32	1.5319527	1.59375	1.594089039	0.189336963	-0.062136339
1101	(19 VREF) /32	1.7653105	1.78125	1.783604976	0.043841863	-0.018294476
1111	(21 VREF) /32	1.9077945	1.96875	1.973120913	-0.047031937	-0.065326413
1110	(23 VREF) /32	2.1426682	2.15625	2.162636851	0.045357763	-0.019968651
1010	(25 VREF) /32	2.2847114	2.34375	2.352152788	-0.047472737	-0.067441388
1011	(27 VREF) /32	2.5258632	2.53125	2.541668725	0.051635863	-0.015805525
1001	(29 VREF) /32	2.6697245	2.71875	2.731184663	-0.045654637	-0.061460163
1000	(31 VREF) /32	2.9207006	2.90625	2.9207006	0.061460163	0

The maximum DNL was found to be 0.189337 and the minimum DNL was found to be -0.18812. The maximum INL is -0.02880550 and the minimum INL is calculated to be -0.2514733. The plots of DNL and INL are shown in Figure 5-13.



(a) *(b)*

Figure 5-13 (a) Differential Non-Linearity and (b) Integral Non-linearity of MOSFET Only VMGCI DAC

5.3.3 Current Mode Gray Code Input DAC (CMGCI DAC)

The CMGCI DAC is devised by removing the R resistor of CMGCI DAC and replacing the 2R resistor with the binary weighted current sources as shown in Figure 5-14. Glitches are a particular problem for current steering DACs without buffers, since the current is being routed directly to the output. It is not possible to use alternative deglitching techniques in current steering DACs, so it is interesting to see if this topology can produce high-speed glitch-free current-steering DACs. The current steering DACs have some advantages over resistor DACs,

a. They do not need buffers to drive resistive load

b. They are suitable for high frequency applications.

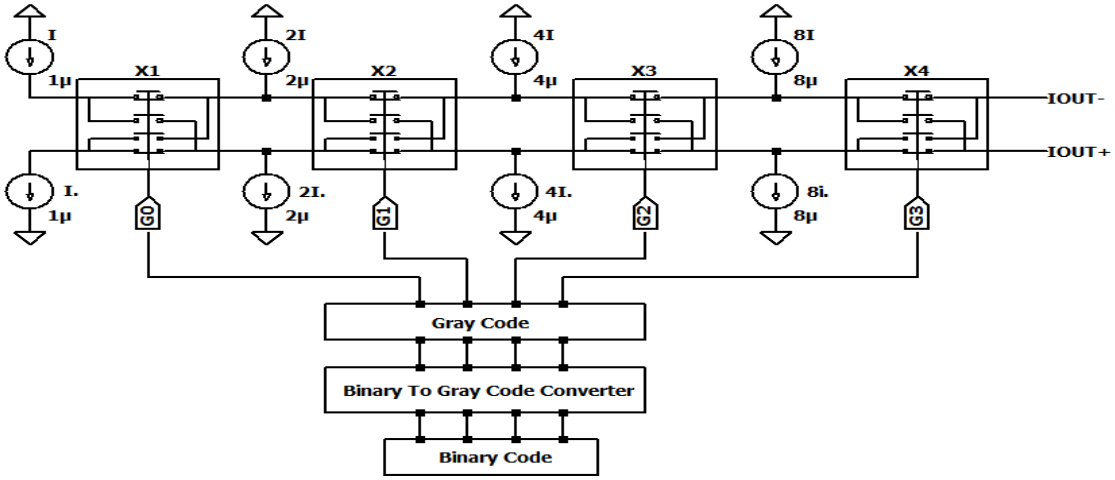


Figure 5-14 CMGCI DAC

5.3.3.1 Working Principle of CMGCI DAC

The input is converted to Gray code and this code is fed to corresponding switch CTL Pin G3, G2, G1, G0. Each stage is applied with binary weighted current sources. Some of the output for some values of input are analysed as follows.

When Gray code =0000, every switches remain parallel, the output at IOUT- is;

$Iout-= I + 2I + 4I + 8I = 15I$

And the output at IOUT+ is;

$Iout+= -I - 2I - 4I - 8I = -15I$

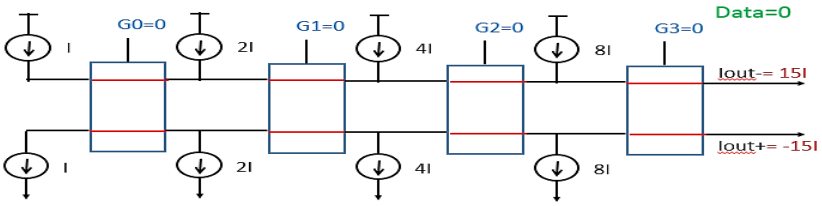


Figure 5-15 Configuration of Current Mode DAC for Gray Code Input 0000

When Gray code =0001, the first switch crosses and the other switches remain parallel

$Iout-= -I + 2I + 4I + 8I = 13I$

And the output at IOUT+ is;

$Iout+= I - 2I - 4I - 8I = -13I$

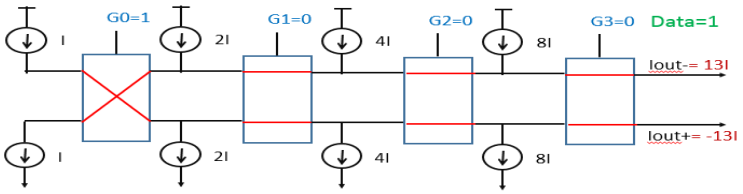


Figure 5-16 Configuration of CMGCI DAC for Gray Code Input 0001

When Gray code =0010, the second switch crosses and the other switches remain parallel

$Iout-= I + 2I - 4I + 8I = 9I$

And the output at IOUT+ is;

$Iout+= -I - 2I + 4I - 8I = -9I$

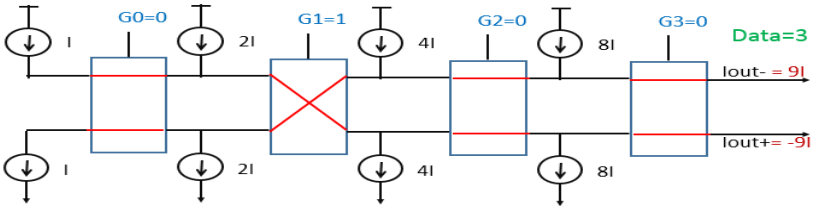


Figure 5-17 Configuration of CMGCI DAC for Gray Code Input 0010

When Gray code =0100, the second switch crosses and the other switches remain parallel

$Iout-= -I - 2I - 4I + 8I = I$

And the output at IOUT+ is;

$Iout+= I + 2I + 4I - 8I = -I$

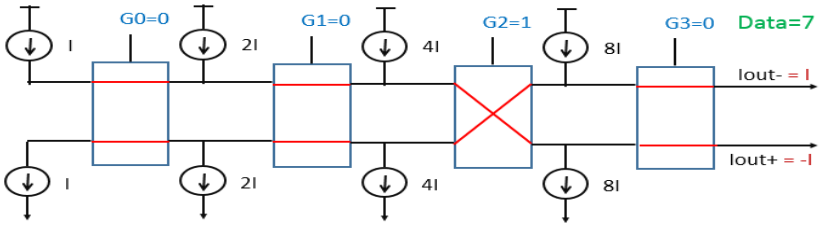


Figure 5-18 Configuration of CMGCI DAC for Gray Code Input 0100

When Gray code =1111, the second switch crosses and the other switches remain parallel

$Iout-= I - 2I + 4I - 8I = -5I$

And the output at IOUT+ is;

$Iout+= -I + 2I - 4I + 8I = 5I$

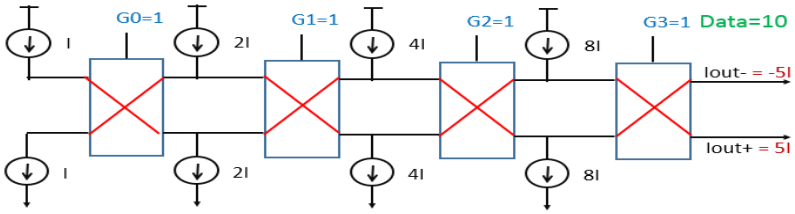


Figure 5-19 Configuration of CMGCI DAC for Gray Code Input 1111

When Gray Code =1000, the second switch crosses and the other switches remain parallel

$Iout-= -I - 2I - 4I - 8I = -15I$

And the output at IOUT+ is;

$Iout+= I + 2I + 4I + 8I = 15I$

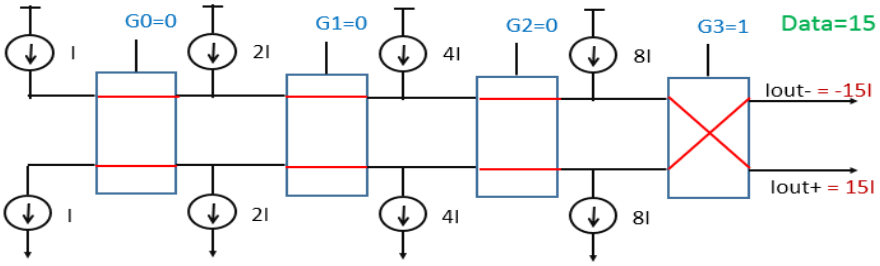


Figure 5-20 Configuration of CMGCI DAC for Gray Code Input 1000

Looking at the above expressions, we can generalize the output of CMGCI DAC as depicted in equations 5.7 and 5.8.

$I_{OUT}-= I * (2^N - 2D + 1)$ *(5.7)*

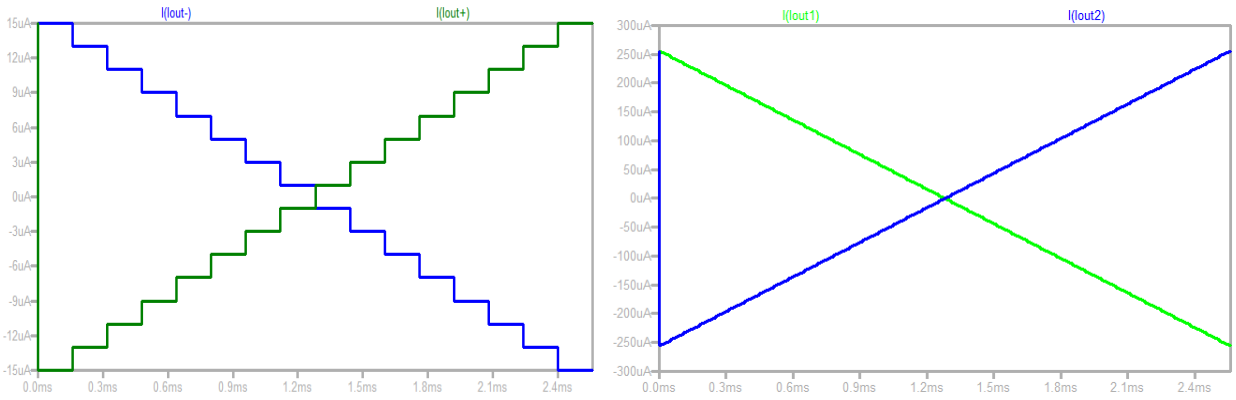
$I_{OUT}+= -I * (2^N - 2D + 1)$ *(5.8)*

5.3.3.2 Simulation Results

Table 5-4 shows the comparison of ideal DAC output and simulated DAC outputs along with the DNL and INL calculation.

Table 5-4 The Ideal and simulated outputs of CMGCI DAC with DNL and INL Calculations

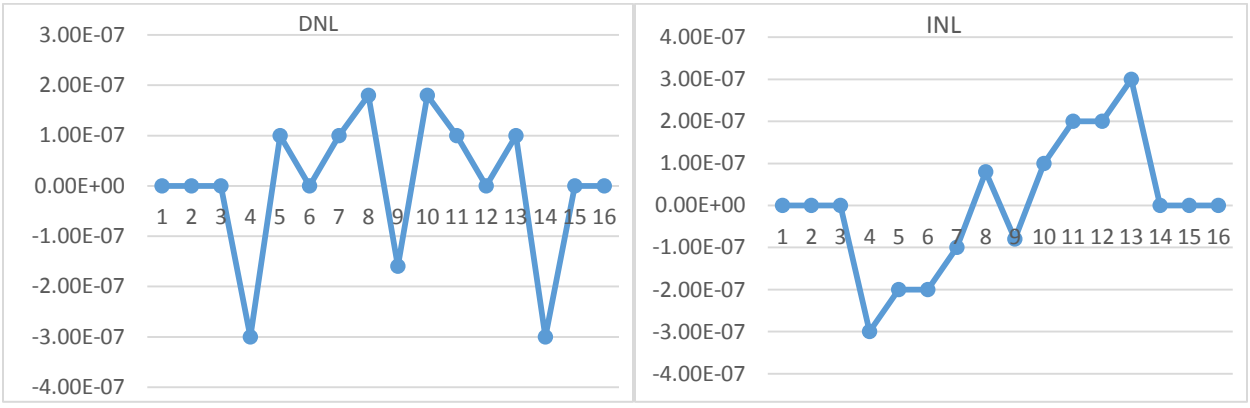
GRAY CODE	IDEAL	SIMULATED	END POINT LINE	DNL	INL
0000	15	14.99976	14.999760000	-	0.00E+00
0001	13	12.999792	12.999792000	0.00E+00	0.00E+00
0011	11	10.999824	10.999824000	0.00E+00	0.00E+00
0010	9	8.9998557	8.999856000	-3.00E-07	-3.00E-07
0110	7	6.9998878	6.999888000	1.00E-07	-2.00E-07
0111	5	4.9999198	4.999920000	0.00E+00	-2.00E-07
0101	3	2.9999519	2.999952000	1.00E-07	-1.00E-07
0100	1	0.99998408	0.999984000	1.80E-07	8.00E-08
1100	-1	-0.99998408	-0.999984000	-1.60E-07	-8.00E-08
1101	-3	-2.9999519	-2.999952000	1.80E-07	1.00E-07
1111	-5	-4.9999198	-4.999920000	1.00E-07	2.00E-07
1110	-7	-6.9998878	-6.999888000	2.66E-15	2.00E-07
1010	-9	-8.9998557	-8.999856000	1.00E-07	3.00E-07
1011	-11	-10.999824	-10.999824000	-3.00E-07	0.00E+00
1001	-13	-12.999792	-12.999792000	3.55E-15	0.00E+00
1000	-15	-14.99976	-14.999760000	-1.78E-15	0.00E+00



(a) (b)

Figure 5-21 Simulation Results (a) 4-bit Current Steering Mode Gray Code (b) 8 bit Current Steering Mode Gray Code and 8-bit R-2R DAC

Here we can see from the table and simulation results that the CMGCI DAC is free of glitches and the output is also very precise. So this topology can be used to design a very high speed DAC. The plots of DNL and INL are shown in Figure 5-26.



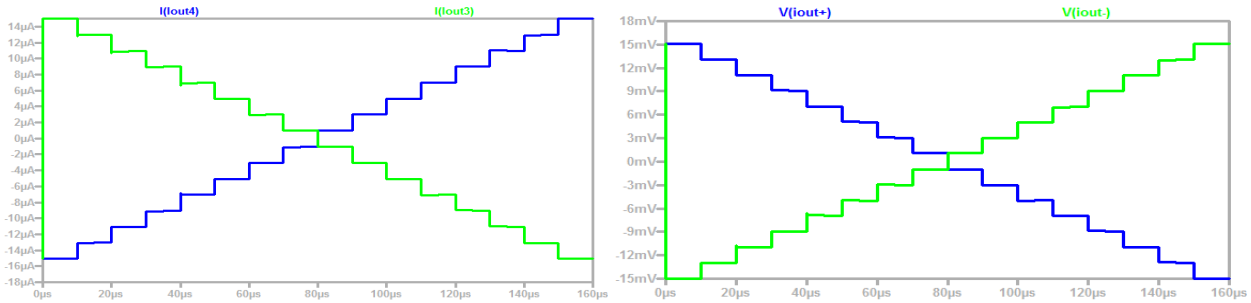
(a) (b)

Figure 5-22 (a) Differential Non-Linearity and (b) Integral Non-linearity of CMGCI DAC

The maximum DNL was found to be $1.8\times10^{-7}$and the minimum DNL was found to be -3×10^{-7}. The maximum INL is 3×10^{-7} and the minimum INL is calculated to be -3×10^{-7}.

5.3.4 MOSFET Only CMGCI DAC

MOSFET implementation of the CMGCI DAC is to design current source and sink circuits to replace the current sources of Figure 5-14. The current source is designed using the PMOS current mirror circuit and the current sinks are designed by using NMOS current mirror circuits. The detailed explanation of the current source and sink design is discussed in Chapter 3.



(a) *(b)*

Figure 5-23 Simulation Result of MOSFET only CMGCI DAC (a) Current Output (b) Voltage Output

Table 5-5 shows the DNL and INL calculations for MOSFET only CMGCI DAC.

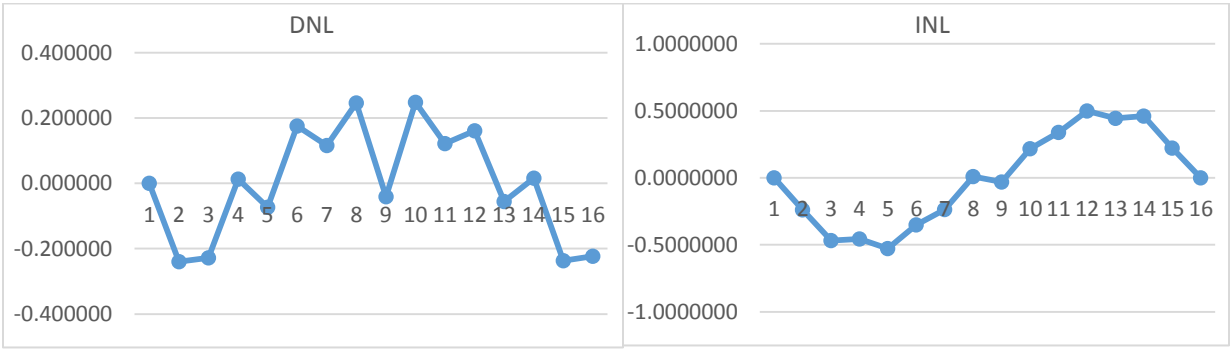
Table 5-5 Calculation of DNL and INL of MOSFET only CMGCI DAC

GRAY CODE	IDEAL	SIMULATED	END POINT LINE	DNL	INL
0000	15	14.99977	14.999770000	-	0.0000000
0001	13	12.7562	12.996045333	-0.239845	-0.2398453
0011	11	10.52459	10.992320667	-0.227885	-0.4677307
0010	9	8.533483	8.988596000	0.012618	-0.4551130
0110	7	6.45685	6.984871333	-0.072908	-0.5280213
0111	5	4.628826	4.981146667	0.175701	-0.3523207
0101	3	2.741234	2.977422000	0.116133	-0.2361880
0100	1	0.983211	0.973697333	0.245702	0.0095137
1100	-1	-1.0616	-1.030027333	-0.041086	-0.0315727
1101	-3	-2.81683	-3.033752000	0.248495	0.2169220
1111	-5	-4.69835	-5.037476667	0.122205	0.3391267
1110	-7	-6.54144	-7.041201333	0.160635	0.4997613
1010	-9	-8.60094	-9.044926000	-0.055775	0.4439860
1011	-11	-10.5885	-11.048650667	0.016165	0.4601507
1001	-13	-12.8291	-13.052375333	-0.236875	0.2232753
1000	-15	-15.0561	-15.056100000	-0.223275	0.0000000

The maximum DNL was found to be 0.248495 and the minimum DNL was found to be -0.239845.

The maximum INL is 0.4997613 and the minimum INL is calculated to be -0.5280213.

Figure 5-24 shows the plots of INL and DNL.



(a) *(b)*

Figure 5-24 (a) Differential Non-Linearity and (b) Integral Non-linearity of CMGCI DAC

6
Glitch Analysis of VMGCI DAC in Case of Sinusoidal Signals

The Gray code DAC performed exceptionally well in the context of glitch reduction for a ramp input. Analysis of the performance of this DAC in case of sinusoidal signal is done in this section. Test bench for comparing the R-2R DAC with VMGCI DAC is shown in Figure 6-1.

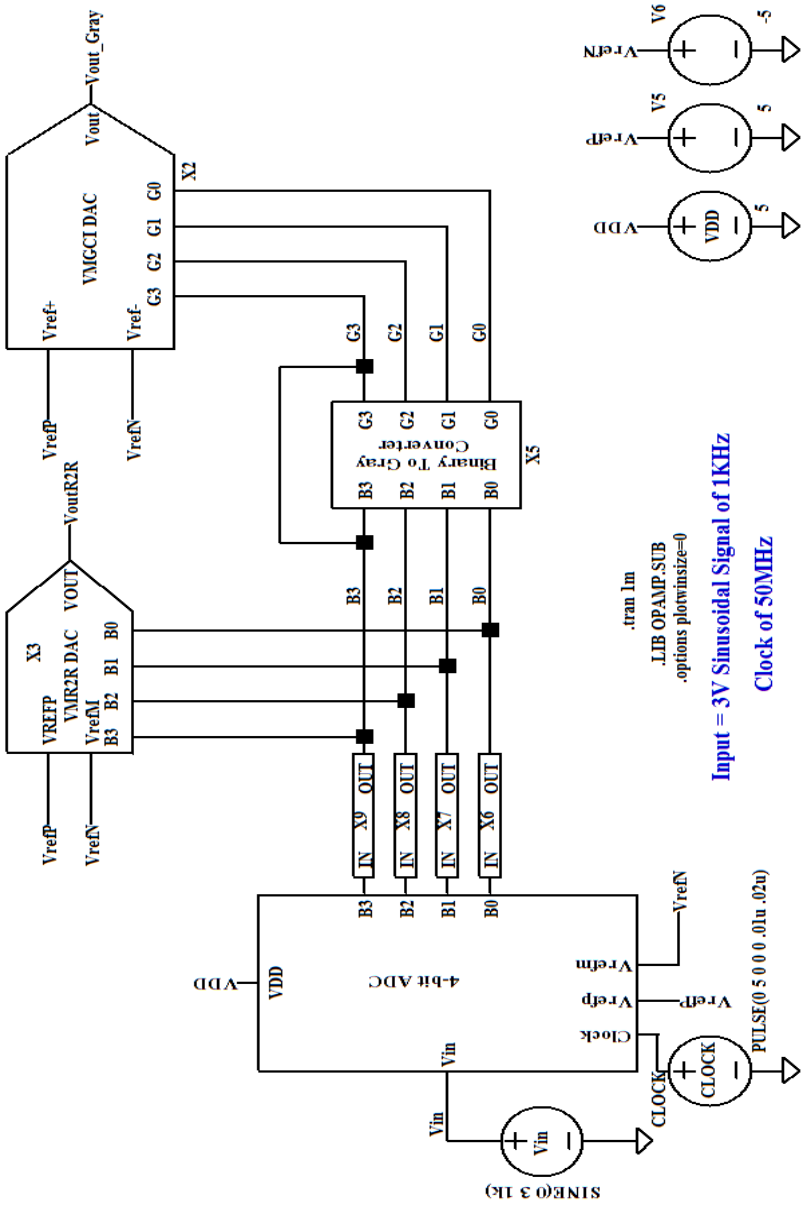


Figure 6-1 Test bench for Sinusoidal response for Gray code and R-2R DAC

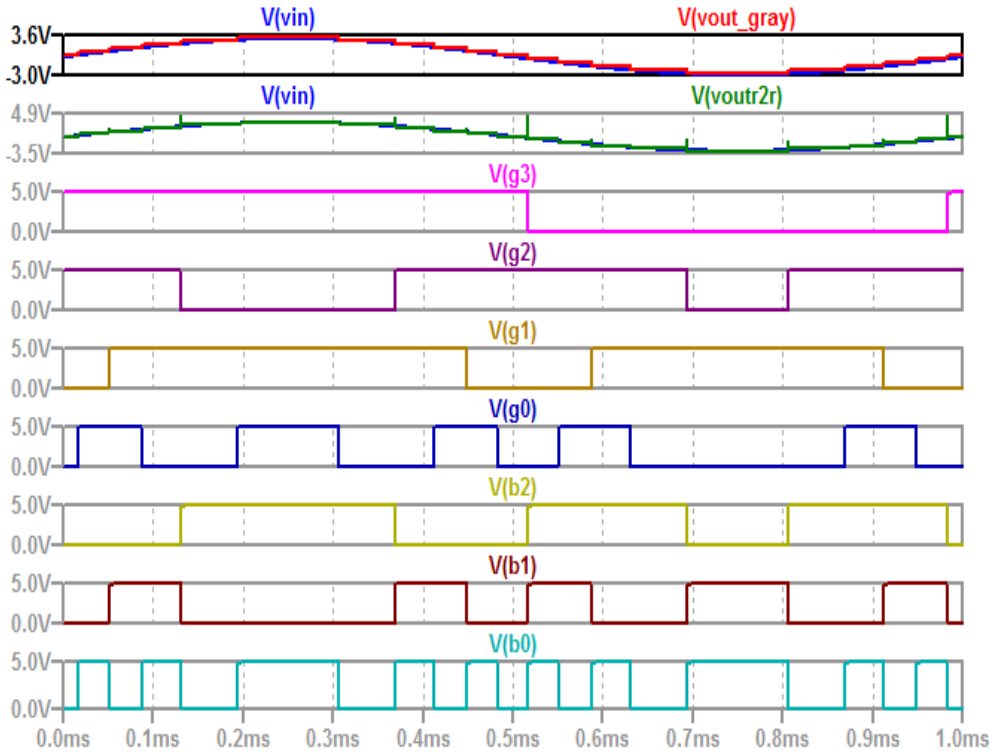


Figure 6-2 Sinusoidal response of VMGCI DAC and R-2R DAC for 1kHz

Figure 6-2 shows the waveforms when the sampling rate is 50 MHz and the input signal is a 3Volt sinusoidal signal of 1kHz, the R-2R DAC generates output with glitches but the VMGCI DAC does not produce any glitches. The following text analyses the DACs responses while changing the input frequency, keeping the sampling rate constant.

I. Keeping Sampling frequency constant to 50MHz and varying input signal

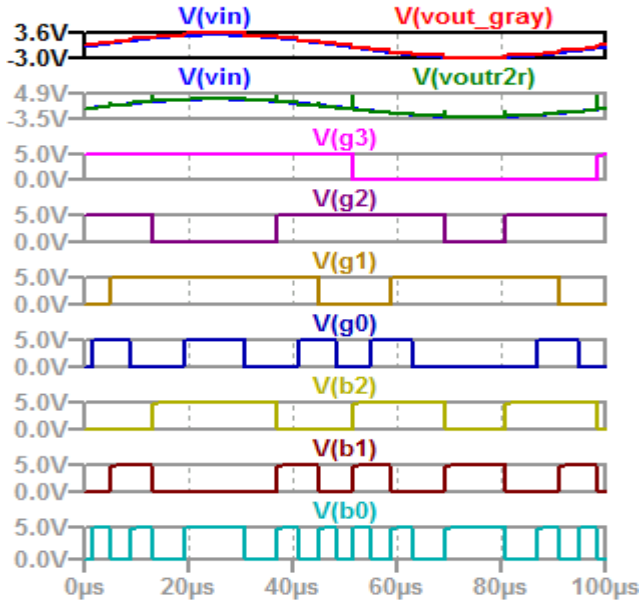


Figure 6-3 Input frequency of 10kHz

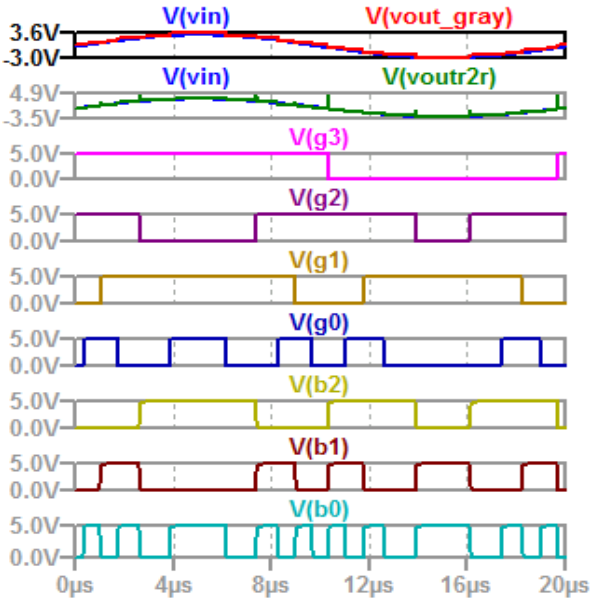


Figure 6-4 Input frequency of 100kHz

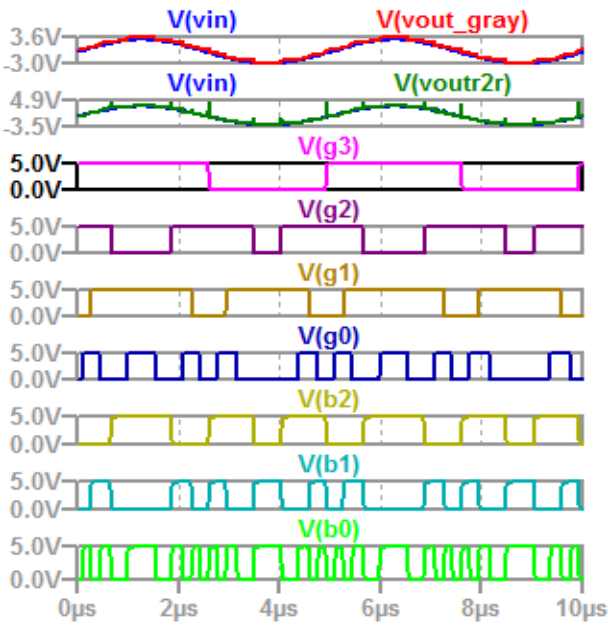


Figure 6-5 Input frequency of 200kHz

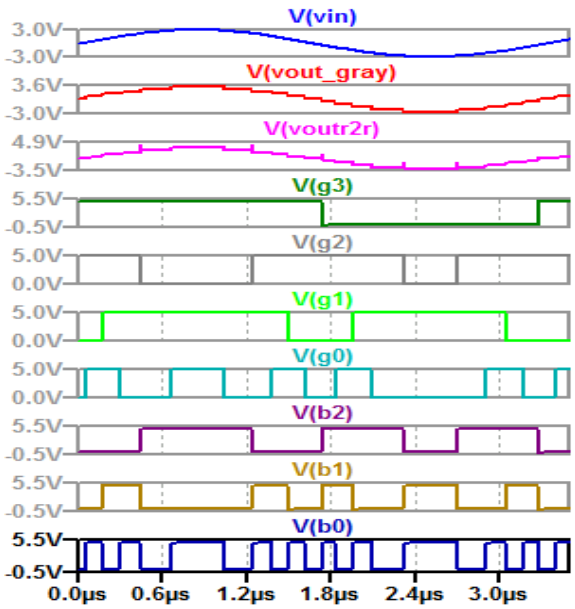


Figure 6-6 Input frequency of 300kHz

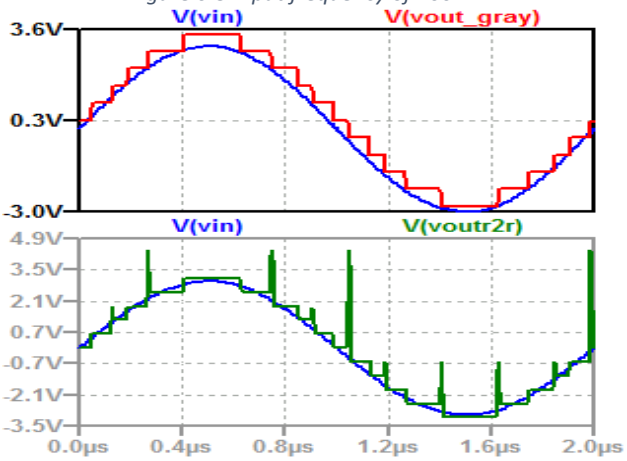


Figure 6-7 Input frequency of 500kHz

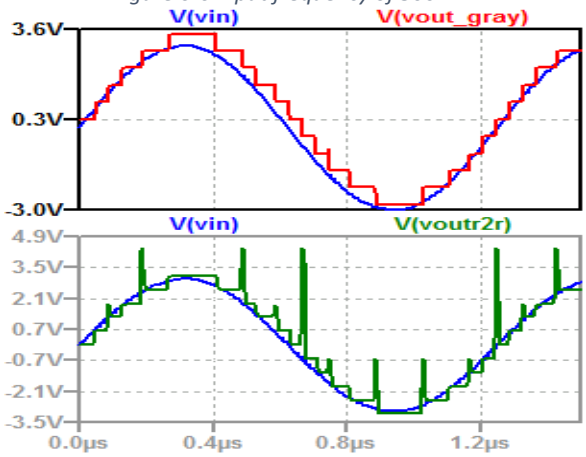


Figure 6-8 Input frequency of 800kHz

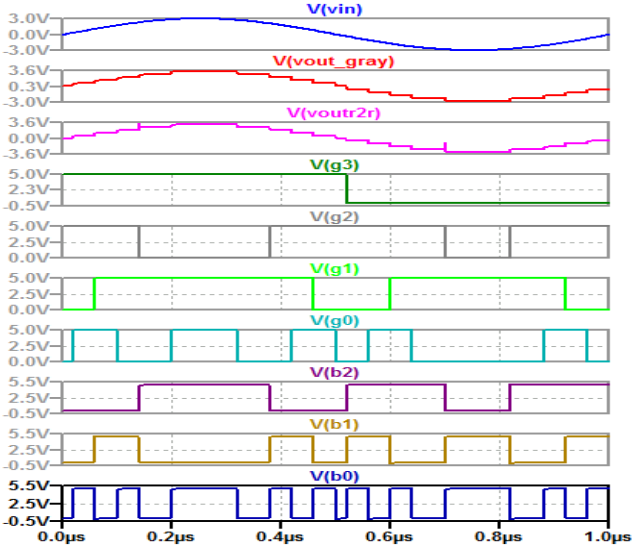


Figure 6-9 Input frequency of 1MHz

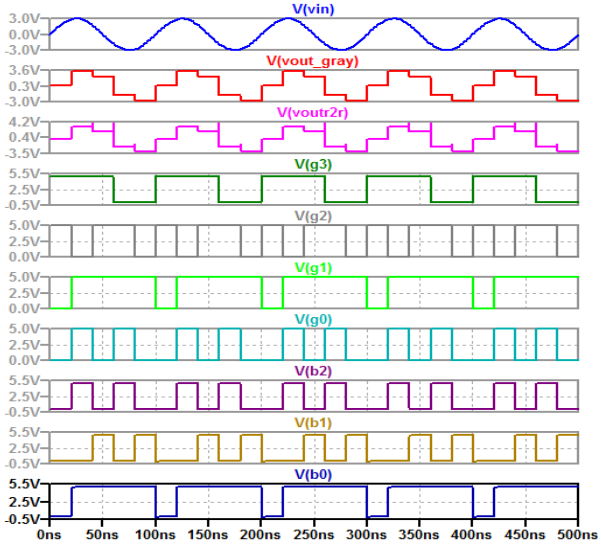


Figure 6-10 Input frequency of 10MHz

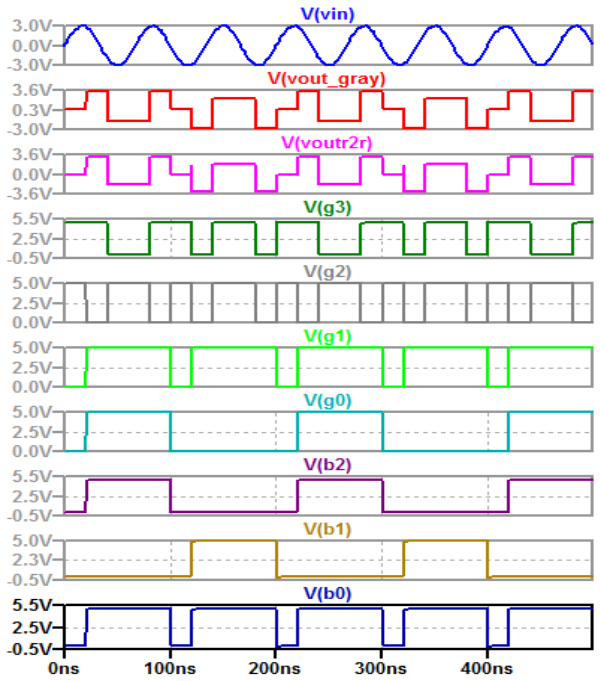


Figure 6-11 Input frequency of 15MHz

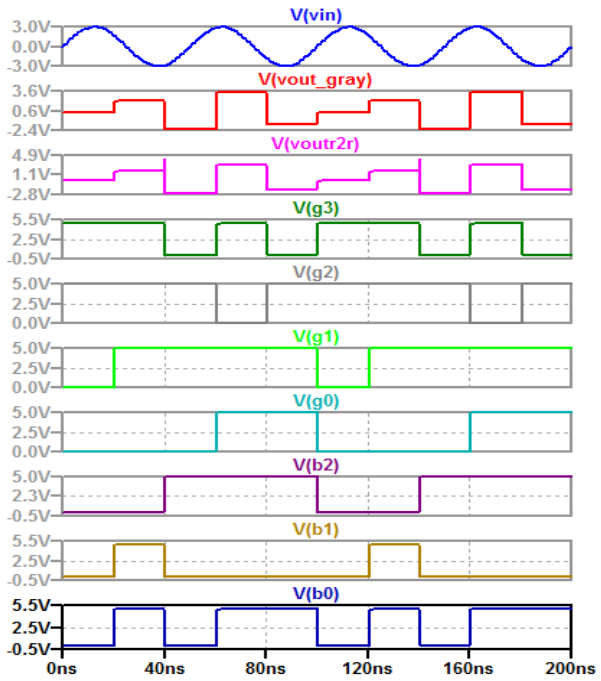


Figure 6-12 Input frequency of 20MHz

When the input frequency is nearer to the ½ of sampling frequency, the output is ideal, but the VMGCI DAC performs better in terms of glitch reduction in comparison to the R-2R DAC.

II. Keeping input frequency constant to 10kHz and varying the sampling frequency

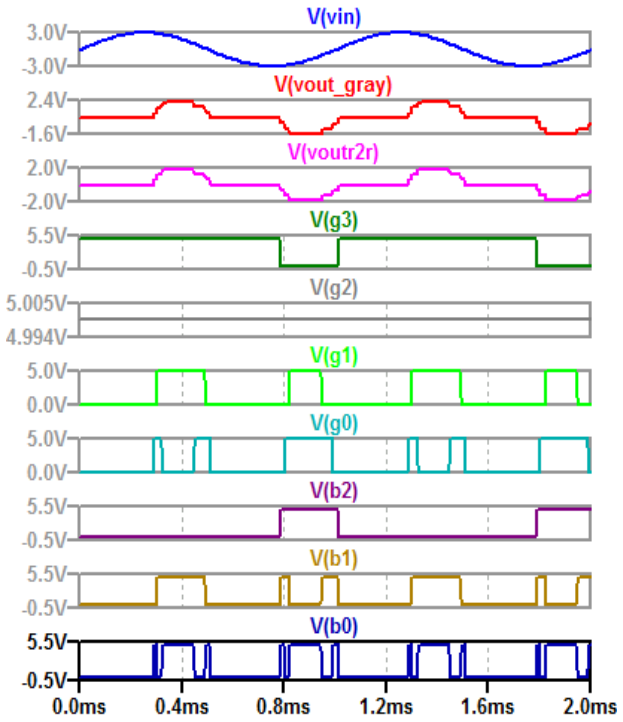


Figure 6-13 sampling frequency of 2kHz

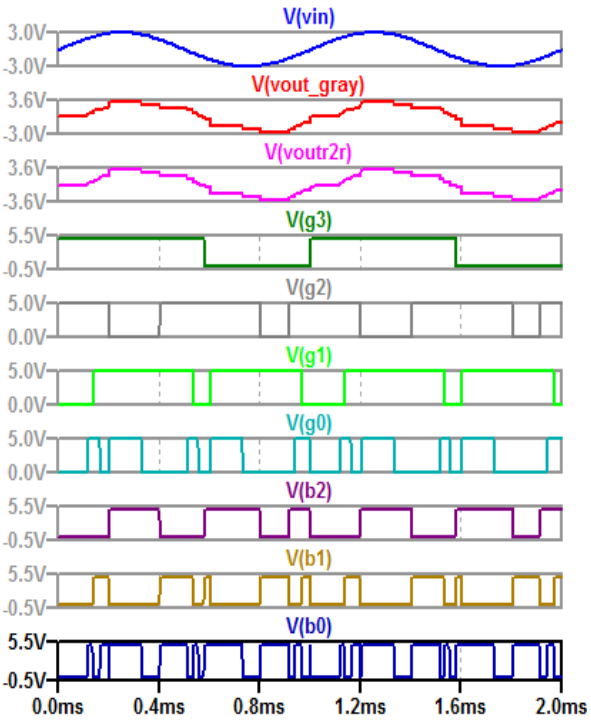


Figure 6-14 sampling frequency of 5kHz

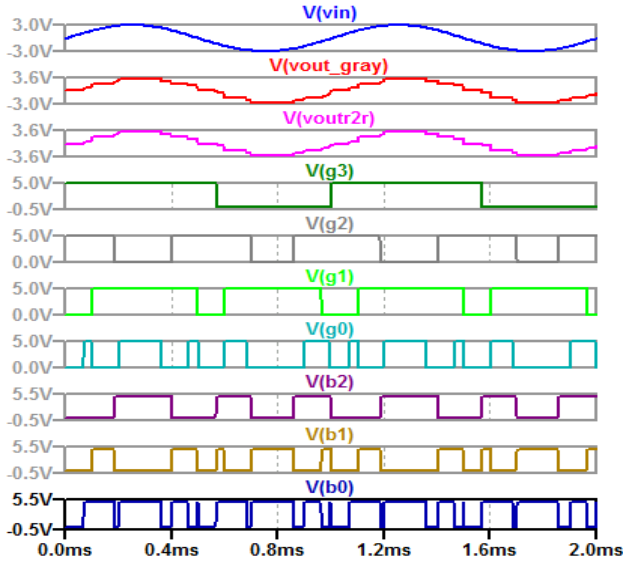


Figure 6-15 sampling frequency of 10kHz

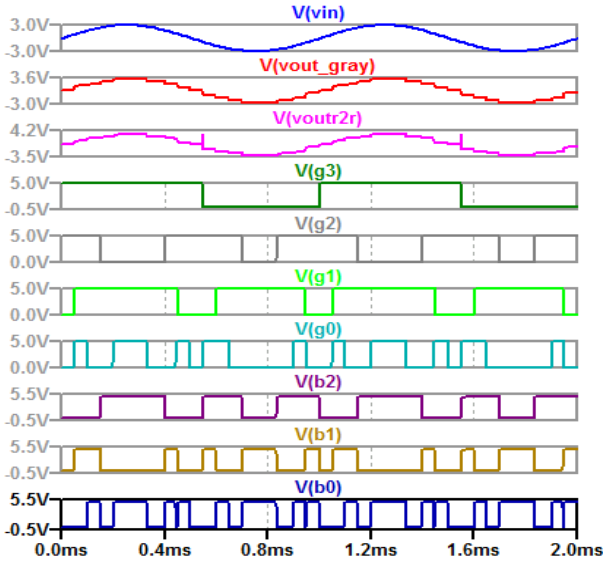


Figure 6-16 sampling frequency of 20kHz

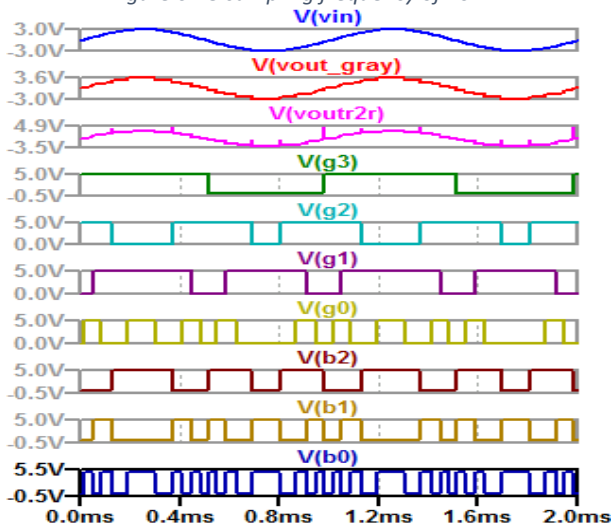


Figure 6-17 sampling frequency of 100kHz

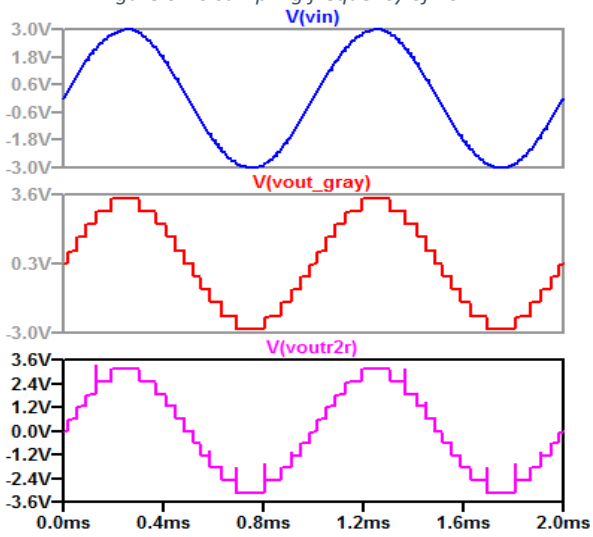


Figure 6-18 sampling frequency of 1MHz

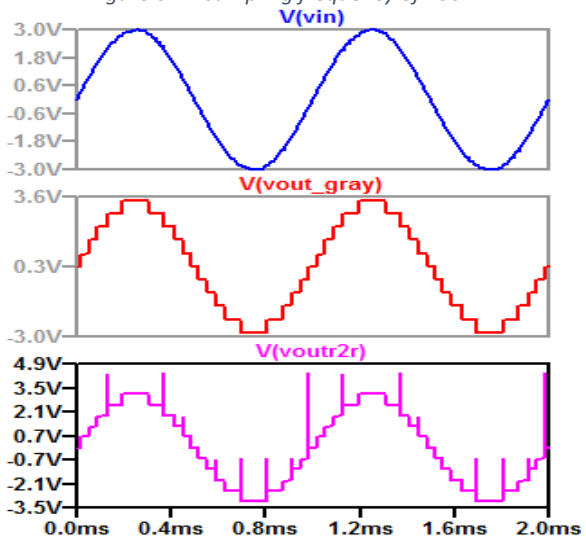


Figure 6-19 sampling frequency of 10MHz

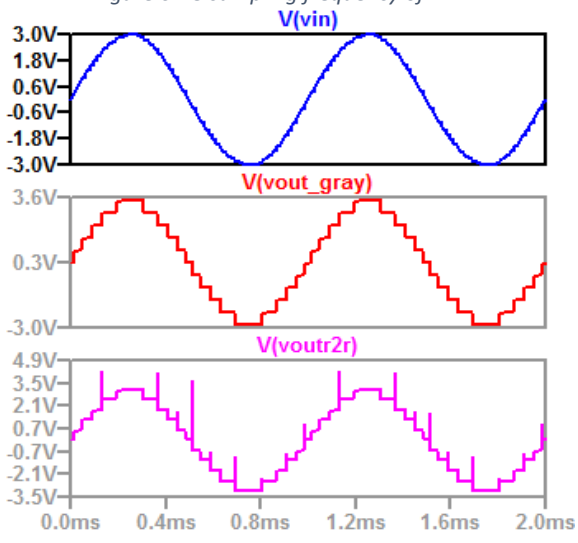


Figure 6-20 sampling frequency of 50MHz

For the sinusoidal signal, increasing the sampling frequency, does not affect the VMGCI DAC, whereas, the R-2R DAC contains glitches.

III. Delaying the bits to check how it affects the output of VMGCI DAC

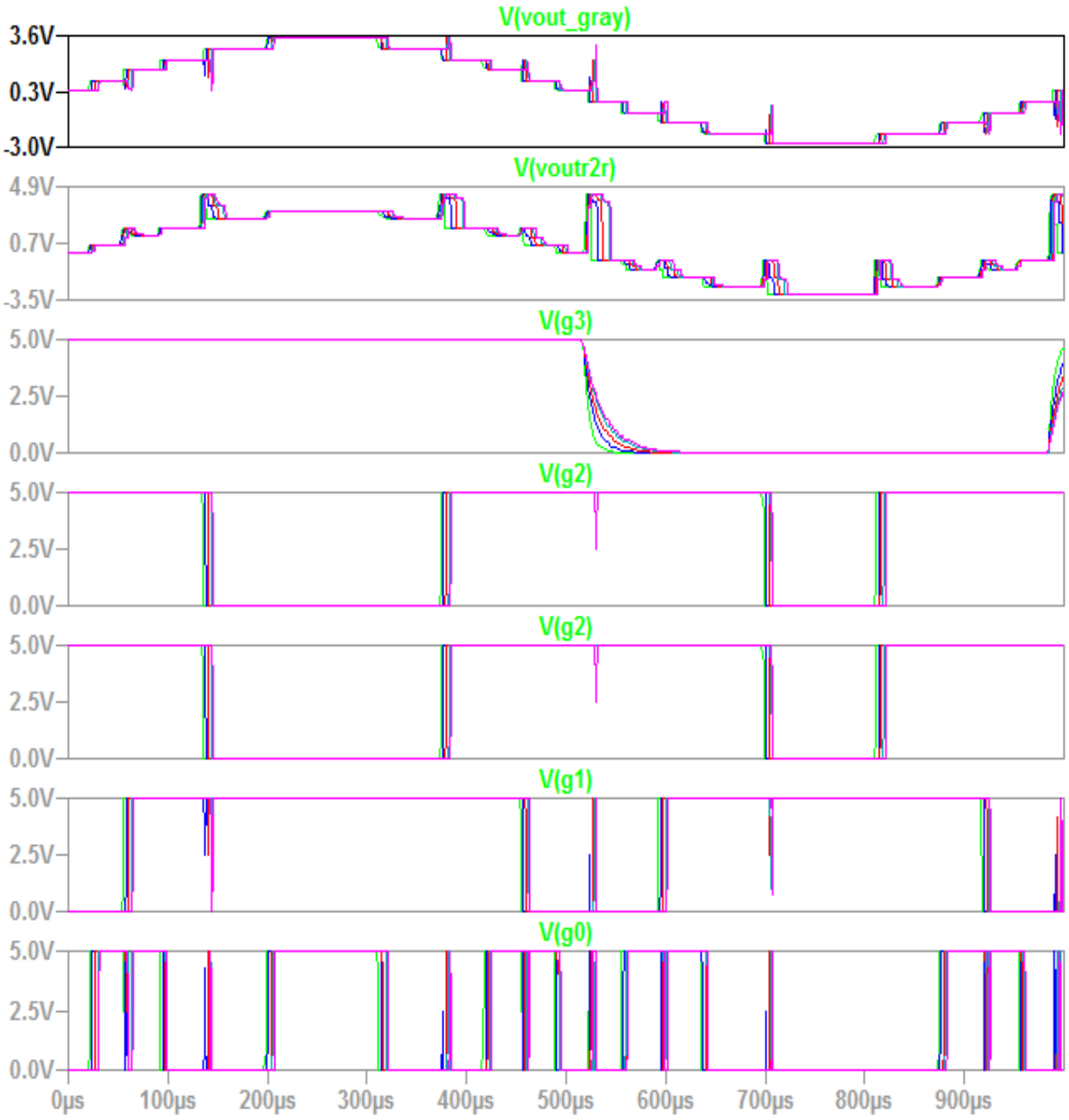


Figure 6-21 Response of VMGCI DAC when the bits are delayed.

Glitches start to appear in VMGCI DAC when the delay is above 3 micro seconds. The glitches appear because of the distortions in Gray code conversion. If the bits are delayed, the conversion of binary to Gray code is affected. Glitches are then transmitted to the DAC from binary to Gray code conversion.

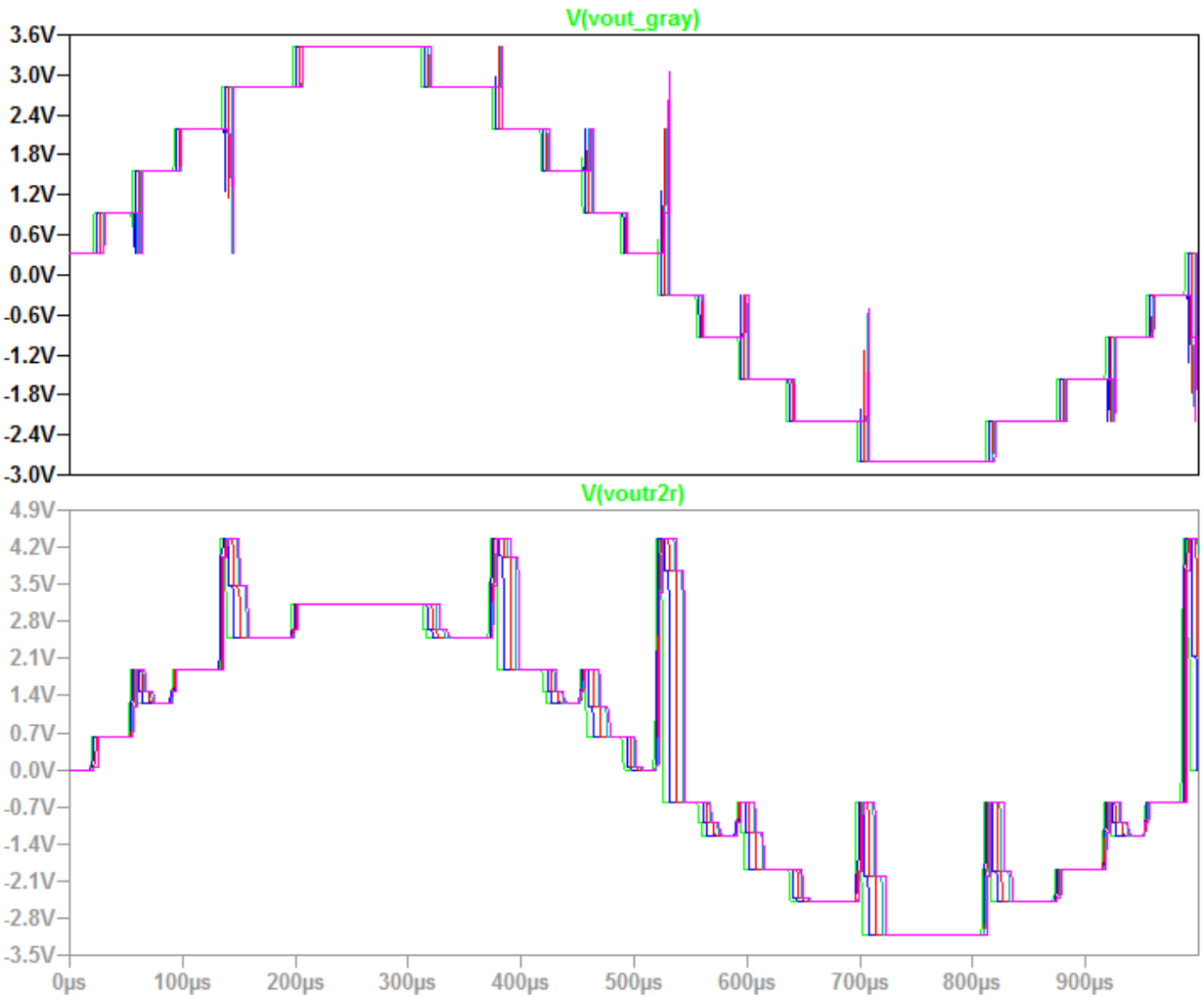


Figure 6-22 Response of VMGCI DAC when the bits are delayed

Occurrence of glitches in the Gray code DAC is very rare and appear under certain conditions only. The condition is the conversion and delay in bits should be very large. Since devices have become faster, this rare condition is assumed to occur even rarer. So for glitch reduction, the use of the Gray code input DAC is recommended.

7
Conclusion and Future works

The main objective of this dissertation is to introduce and demonstrate the feasibility of Gray code input DAC and thereby suggest a way to reduce glitches within the DAC rather employing other external circuitry for this purpose using CMOS transistors. Two types of DACs were proposed and the comparison of the purposed DACs with binary DACs of its corresponding modes were compared in terms of glitch performance and other static errors. Also the performance of this DAC with different inputs were questioned. It was assumed that the Gray code input DACs were very hard to design and implement. Only a few literatures are available in this topic till date. This worked as a motivating factor for this design.

In Chapter 4, we described the design of two modes of binary DACs employing R-2R Ladder. The designed DACs were tested for the reference of 3 Volts. These R-2R DACs contain glitches. The maximum glitch occurs at the mid-point of the output i.e. during the transition between codes 0111 and 1000. For the voltage mode R-2R DAC, the value of the glitch at this point is 1.28776 Volts. This is a very high value for a 3 Volt reference. Not only this, every alternating codes contains glitches. These glitches will somehow adversely affect the performance of other parts of the circuit where it is implemented. The DNL and INL of this DAC were pretty decent and were well under ±0.5 LSB range and ±1LSB range respectively. Similarly, for the current mode R-2R DAC, for a reference current of 300µA, the highest glitch was recorded to be 60.76954µA which is also a very high value of current.

In Chapter 5, the proposed DACs were designed and simulated. For VMGCI DAC, no glitches occurred for the ramp input. The DNL and INL were within the range for typical DAC. Also the CMGCI DAC also performed without glitches. And the DNL and INL errors were within the range for a typical DAC, i.e., well under ±0.5 LSB range and ±1LSB range respectively.

In case of the sinusoidal input signal, the Gray code DAC performed equally well. The glitches appear only when the bits are delayed up to 3micro seconds. This is a very large amount of time and is not expected to occur because todays devices have become very fast.

There is much less attention given in this type of DAC. But we have proven that Gray code input DACs can be designed and can readily remove or minimize glitches.

This work is merely based on simulations using LTSpice Simulator for transient simulations to detect glitches and calculations of DNL and INL. Further improvements are possible in case of DNL and INL improvements and accuracy. Other DAC parameters like settling time, stability, noise etc. should be considered before fabrication. Furthermore, layout analysis is not done in this work. If further analysis is done, this work may be beneficial to those designs which are suffering from glitches and are searching for a way to remove glitches reducing the chip area and cost.

List of Related Publications and Presentations

1. **Study of Gray code input DAC using MOSFETs for glitch reduction**
   Gopal Adhikari*, Richen Jiang, Haruo Kobayashi
   13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Year: 2016, Pages: 97 - 99, DOI: 10.1109/ICSICT.2016.7998849

2. **Study of R-2R Ladder DAC and Gray Code Input DAC using MOSFET for Glitch Reduction**
   Gopal Adhikari*, Richen Jiang, Haruo Kobayashi
   第 63 回システム LSI 合同ゼミ中央大学, Year: 2016

3. **Study of R-2R Ladder DAC and Gray Code Input DAC using MOSFET for Glitch Reduction**
   Gopal Adhikari*, Richen Jiang, Haruo Kobayashi
   電子回路研究会, Year: 2016, ECT-016-045

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List of abbreviations

Abbreviations	Full Forms
D/A	Digital to Analog
A/D	Analog to Digital
DAC	Digital to Analog Converter
ADC	Analog to Digital
LSB	Least Significant Bit
MSB	Most Significant Bit
SPICE	Simulation Program with Integrated Circuit Emphasis
DSP	Digital Signal Processing
VREF	Reference Voltage
DNL	Differential Non-Linearity
INL	Integral Non-Linearity
FSR	Full Scale Range
Vout	Output Voltage
OPAMP	Operational Amplifier
CSA	Common Source Amplifier
DC	Direct Current
GBW	Gain Bandwidth Product
ICMR	Input Common Mode Range
PSRR	Power Supply Rejection Ratio
CMRR	Common Mode Rejection Ratio
PMOS	P-type metal oxide semiconductor
NMOS	N-type metal oxide semiconductor
CMOS	Complementary Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Semiconductor
DPDT	Double Pole Double Throw
SPDT	Single Pole Double Throw
CTL	Control
W/L	W=Width, L=Length (Aspect Ratio)
XOR	Exclusive OR
BGR	Band Gap Reference
CTAT	Complementary to Absolute Temperature
PTAT	Proportional to Absolute Temperature
DRAM	Dynamic Random Access Memory
FVF	Flipped Voltage Follower
FFVF	Folded Flipped Voltage Follower
VL	Low Voltage Level
VH	High Voltage Level
IC	Integrated Circuit
RBC	Reflected Binary code
VMGCI	Voltage Mode Gray code Input
CMGCI	Current Mode Gray code Input
VM R-2R	Voltage Mode R-2R
CM R-2R	Current Mode R-2R

Appendix

a. The model file for TSMC 0. 18μm

.MODEL CMOSN NMOS (LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9
+XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.3694303
+K1 = 0.5789116 K2 = 1.110723E-3 K3 = 1E-3
+K3B = 0.0297124 W0 = 1E-7 NLX = 2.037748E-7
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 1.2953626 DVT1 = 0.3421545 DVT2 = 0.0395588
+U0 = 293.1687573 UA = -1.21942E-9 UB = 2.325738E-18
+UC = 7.061289E-11 VSAT = 1.676164E5 A0 = 2
+AGS = 0.4764546 B0 = 1.617101E-7 B1 = 5E-6
+KETA = -0.0138552 A1 = 1.09168E-3 A2 = 0.3303025
+RDSW = 105.6133217 PRWG = 0.5 PRWB = -0.2
+WR = 1 WINT = 2.885735E-9 LINT = 1.715622E-8
+XL = 0 XW = -1E-8 DWG = 2.754317E-9
+DWB = -3.690793E-9 VOFF = -0.0948017 NFACTOR = 2.1860065
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 2.665034E-3 ETAB = 6.028975E-5
+DSUB = 0.0442223 PCLM = 1.746064 PDIBLC1 = 0.3258185
+PDIBLC2 = 2.701992E-3 PDIBLCB = -0.1 DROUT = 0.9787232
+PSCBE1 = 4.494778E10 PSCBE2 = 3.672074E-8 PVAG = 0.0122755
+DELTA = 0.01 RSH = 7 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -0.11
+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WL = 0 WLN = 1 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 8.58E-10 CGSO = 8.58E-10 CGBO = 1E-12
+CJ = 9.471097E-4 PB = 0.8 MJ = 0.3726161
+CJSW = 1.905901E-10 PBSW = 0.8 MJSW = 0.1369758
+CJSWG = 3.3E-10 PBSWG = 0.8 MJSWG = 0.1369758
+CF = 0 PVTH0 = -5.105777E-3 PRDSW = -1.1011726
+PK2 = 2.247806E-3 WKETA = -5.071892E-3 LKETA = 5.324922E-4
+PU0 = -4.0206081 PUA = -4.48232E-11 PUB = 5.018589E-24
+PVSAT = 2E3 PETA0 = 1E-4 PKETA = -2.090695E-3
+AF = 0.9 KF = 2E-24)
*

```
.MODEL CMOSP PMOS (                    LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ     = 1E-7         NCH     = 4.1589E17     VTH0    = -0.3823437
+K1     = 0.5722049     K2      = 0.0219717     K3      = 0.1576753
+K3B    = 4.2763642     W0      = 1E-6         NLX     = 1.104212E-7
+DVT0W   = 0           DVT1W   = 0           DVT2W   = 0
+DVT0    = 0.6234839     DVT1    = 0.2479255     DVT2    = 0.1
+U0     = 109.4682454   UA      = 1.31646E-9    UB      = 1E-21
+UC     = -1E-10        VSAT    = 1.054892E5    A0      = 1.5796859
+AGS    = 0.3115024     B0      = 4.729297E-7   B1      = 1.446715E-6
+KETA   = 0.0298609     A1      = 0.3886886     A2      = 0.4010376
+RDSW   = 199.1594405   PRWG    = 0.5          PRWB    = -0.4947034
+WR     = 1           WINT    = 0           LINT    = 2.93948E-8
+XL     = 0           XW      = -1E-8        DWG     = -1.998034E-8
+DWB    = -2.481453E-9  VOFF    = -0.0935653    NFACTOR = 2
+CIT    = 0           CDSC    = 2.4E-4       CDSCD   = 0
+CDSCB   = 0           ETA0    = 3.515392E-4   ETAB    = -4.804338E-4
+DSUB   = 1.215087E-5   PCLM    = 0.96422      PDIBLC1 = 3.026627E-3
+PDIBLC2 = -1E-5        PDIBLCB = -1E-3        DROUT   = 1.117016E-4
+PSCBE1  = 7.999986E10   PSCBE2  = 8.271897E-10  PVAG    = 0.0190118
+DELTA   = 0.01         RSH     = 8.1          MOBMOD  = 1
+PRT    = 0           UTE     = -1.5         KT1     = -0.11
+KT1L   = 0           KT2     = 0.022        UA1     = 4.31E-9
+UB1    = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL     = 0           WLN     = 1           WW      = 0
+WWN    = 1           WWL     = 0           LL      = 0
+LLN    = 1           LW      = 0           LWN     = 1
+LWL    = 0           CAPMOD  = 2           XPART   = 0.5
+CGDO   = 7.82E-10      CGSO    = 7.82E-10      CGBO    = 1E-12
+CJ     = 1.214428E-3   PB      = 0.8461606     MJ      = 0.4192076
+CJSW   = 2.165642E-10  PBSW    = 0.8          MJSW    = 0.3202874
+CJSWG   = 4.22E-10      PBSWG   = 0.8          MJSWG   = 0.3202874
+CF     = 0           PVTH0   = 5.167913E-4   PRDSW   = 9.5068821
+PK2    = 1.095907E-3   WKETA   = 0.0133232     LKETA   = -3.648003E-3
+PU0    = -1.0674346    PUA     = -4.30826E-11  PUB     = 1E-21
+PVSAT   = 50          PETA0   = 1E-4         PKETA   = -1.822724E-3
+AF       = 1.0               KF        = 2E-25             )
*
```

b. 4-bit Voltage Mode R-2R DAC Netlist

```
* E:\simulations for thesis report\VMGCI DAC\R-2R DAC 4Bit.asc
S1 N002 VREFP B2 0 SW1
S2 N002 VREFM B2 0 _SW1
S3 N004 VREFP B1 0 SW1
S4 N004 VREFM B1 0 _SW1
S5 N003 VREFP B0 0 SW1
S6 N003 VREFM B0 0 _SW1
R1 N005 N006 10k
R2 N005 N002 20k
R3 N006 N007 10k
R4 N006 N004 20k
R5 N007 VREFM 20k
R6 N007 N003 20k
S7 N001 VREFP B3 0 SW1
S8 N001 VREFM B3 0 _SW1
R7 VOUT N005 10k
R8 VOUT N001 20k
.model _SW1 SW(Ron=10G Roff=10 Vt=1.2)
.model SW1 SW(Ron=10 Roff=10G Vt=1.8)
.backanno
.end
```

c. 4-Bit MOSFET only Voltage Mode R-2R DAC

```
* E:\simulations for thesis report\Voltage mode R-2R 8bit.asc
V1 VG 0 6.5
V3 B0 0 PULSE(0 3 0 1n 1n 10u 20u)
V4 B1 0 PULSE(0 3 0 1n 1n 20u 40u)
V5 B2 0 PULSE(0 3 0 1n 1n 40u 80u)
V6 B3 0 PULSE(0 3 0 1n 1n 80u 160u)
M25 B1 VG P001 0 CMOSN l=2u w=1.2u
M26 P001 VG N002 0 CMOSN l=2u w=1.2u
M27 N002 VG N001 0 CMOSN l=2u w=1.2u
M28 B0 VG P002 0 CMOSN l=2u w=1.2u
M29 P002 VG N001 0 CMOSN l=2u w=1.2u
M30 B3 VG P003 0 CMOSN l=2u w=1.2u
M31 P003 VG VoutMOS 0 CMOSN l=2u w=1.2u
M32 VoutMOS VG N003 0 CMOSN l=2u w=1.2u
M33 B2 VG P004 0 CMOSN l=2u w=1.2u
M34 P004 VG N003 0 CMOSN l=2u w=1.2u
M35 N003 VG N002 0 CMOSN l=2u w=1.2u
M36 0 VG P005 0 CMOSN l=2u w=1.2u
M37 P005 VG N001 0 CMOSN l=2u w=1.2u
V2 Vref 0 3
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\Gopal\Documents\LTspiceXVII\lib\cmp\standard.mos
.include tsmc018um.lib
.tran 2560u
.backanno
.end
```

d. 4-Bit Current Mode R-2R DAC

```
* E:\simulations for thesis report\Current Mode DAC\Current Mode R-2R DAC.asc
S1 N004 N008 B3 0 SW1
S2 N004 0 B3 0 _SW1
R1 Vref N004 20k
R2 Vref N001 10k
S3 N006 N008 B1 0 SW1
S4 N006 0 B1 0 _SW1
R3 N002 N006 20k
R4 N003 0 20k
Res1 Voutres N008 10k
S5 N005 N008 B2 0 SW1
S6 N005 0 B2 0 _SW1
R5 N001 N005 20k
R6 N001 N002 10k
XU1 N008 0 Voutres opamp Aol=100K GBW=10Meg
R7 N002 N003 10k
S7 N007 N008 B0 0 SW1
S8 N007 0 B0 0 _SW1
R8 N003 N007 20k
.backanno
.end
```

e. MOS Only 4-Bit Current Mode R-2R DAC

```
M1 N013 B3 Vref Vref CMOSP l=.18u w=15u
M2 N013 B3 0 0 CMOSN l=.18u w=10u
M3 N010 B2 Vref Vref CMOSP l=.18u w=15u
M4 N010 B2 0 0 CMOSN l=.18u w=10u
M5 N011 B1 Vref Vref CMOSP l=.18u w=15u
M6 N011 B1 0 0 CMOSN l=.18u w=10u
M7 N001 VG Vref 0 CMOSN l=2.1u w=1.29u
M8 N002 VG N001 0 CMOSN l=2.1u w=1.29u
M9 Vref VG N005 0 CMOSN l=2.1u w=1.29u
M10 N005 B3 N012 0 CMOSN l=2.1u w=1.29u
XU1 N012 0 VOutMos opamp Aol=100K GBW=10Meg
R§MOS1 VOutMos N012 10k
M11 N006 B2 N012 0 CMOSN l=2.1u w=1.29u
M12 N007 B1 N012 0 CMOSN l=2.1u w=1.29u
M13 N005 N013 0 0 CMOSN l=2.1u w=1.29u
M14 N006 N010 0 0 CMOSN l=2.1u w=1.29u
M15 N007 N011 0 0 CMOSN l=2.1u w=1.29u
M16 N008 VG 0 0 CMOSN l=2.1u w=1.29u
M17 N003 VG N008 0 CMOSN l=2.1u w=1.29u
M18 N002 VG N007 0 CMOSN l=2.1u w=1.29u
M19 N001 VG N006 0 CMOSN l=2.1u w=1.29u
M20 N003 VG N002 0 CMOSN l=2.1u w=1.29u
M21 N009 B0 Vref Vref CMOSP l=.18u w=15u
M22 N009 B0 0 0 CMOSN l=.18u w=10u
M23 N004 N009 0 0 CMOSN l=2.1u w=1.29u
M24 N003 VG N004 0 CMOSN l=2.1u w=1.29u
M25 N004 B0 N012 0 CMOSN l=2.1u w=1.29u
.model NMOS NMOS
.model PMOS PMOS
.backanno
.end
```

f. 4-Bit VMGCI DAC

```
R1 Vout N010 .5K
R2 Vout P001 1.5K
XX1 G3 Vref+ N001 Vref- N007 swfun
R3 N002 N007 2K
R4 N002 N001 1K
XX2 G2 N002 N003 N007 N008 swfun
R5 N004 N008 2K
R6 N004 N003 1K
XX3 G1 N004 N005 N008 N009 swfun
R7 N006 N009 2K
R8 N006 N005 1K
XX4 G0 N006 P001 N009 N010 swfun
* block symbol definitions
.subckt swfun CTL IO1 IO2 IO3 IO4
S1 IO1 IO2 CNC 0 NO
S2 IO1 IO4 CNO 0 NO
S3 IO3 IO2 CNO 0 NO
S4 IO3 IO4 CNC 0 NO
A1 CTL 0 0 0 0 CNC CNO 0 BUF VHigh=5 VLow=0
R1 CTL 0 1Meg
.model NO SW(Ron=1 Roff=1G Vt=0.5)
.param Ron=1
.param Roff=1G
.ends swfun
.backanno
.end
```

g. MOS Only4-Bit VMGCI DAC

```
* E:\Gray Code DAC\fINAL 4BIT gRAY CODE DAC.asc
V1 N001 0 6
M3 N010 N001 N011 0 CMOSN l=2.162u w=0.576u
M4 N011 N001 N015 0 CMOSN l=.5u w=0.57u
V2 N003 0 3
V3 A5 0 PULSE(0 5 320u 1n 1n 640u 1280u)
V4 A6 0 PULSE(0 5 640u 1n 1n 1280u 2560u)
V5 A7 0 PULSE(0 5 0 1n 1n 1280u 2560u)
V7 A4 0 PULSE(0 5 160u 1n 1n 320u 640u)
M11 N004 N001 N005 0 CMOSN l=1.35u w=0.58u
M12 N005 N001 N012 0 CMOSN l=3u w=0.576u
M13 N006 N001 N007 0 CMOSN l=1.35u w=0.58u
M14 N007 N001 N013 0 CMOSN l=3u w=0.576u
M15 N008 N001 N009 0 CMOSN l=1.35u w=0.58u
M16 N009 N001 N014 0 CMOSN l=3u w=0.576u
XU1 N002 N011 N002 opamp Aol=100K GBW=10Meg
XX5 A7 N003 N004 0 N012 switchnmos
XX6 A6 N005 N006 N012 N013 switchnmos
XX7 A5 N007 N008 N013 N014 switchnmos
XX8 A4 N009 N010 N014 N015 switchnmos

* block symbol definitions
.subckt switchnmos CTL IO1 IO2 IO3 IO4
M2 IO1 CNO IO4 0 CMOSN l=.4u w=80u
M3 IO3 CNO IO2 0 CMOSN l=.4u w=80u
A1 CTL 0 0 0 0 CNC CNO 0 BUF Vhigh=5 Vlow=0
```

```
R1 CTL 0 1Meg
M5 IO1 CNC IO2 0 CMOSN l=.4u w=80u
M6 IO3 CNC IO4 0 CMOSN l=.4u w=80u
.include tsmc018um.lib
.ends switchnmos

.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\Gopal\Documents\LTspiceXVII\lib\cmp\standard.mos
.tran 2560u
.include tsmc018um.lib
.LIB OPAMP.SUB
.backanno
.end
```

h. 4-Bit CMGCI DAC

```
* E:\Gray Code DAC\Current mode gray.asc
V1 A4 0 PULSE(0 3 16u 1n 1n 32u 64u)
V2 A5 0 PULSE(0 3 32u 1n 1n 64u 128u)
V3 A6 0 PULSE(0 3 64u 1n 1n 128u 256u)
V4 A7 0 PULSE(0 3 0 1n 1n 128u 256u)
I§2I 0 N002 2µ
I 0 N001 1µ
I§4I 0 N003 4µ
I§8I 0 N004 8µ
R1 0 N005 1k
R2 0 N010 1k
XX1 A4 N001 N002 N006 N007 swfun
XX2 A5 N002 N003 N007 N008 swfun
XX3 A6 N003 N004 N008 N009 swfun
XX4 A7 N004 N005 N009 N010 swfun
I1 N009 0 8µ
I2 N008 0 4µ
I3 N007 0 2µ
I4 N006 0 1µ
.subckt swfun CTL IO1 IO2 IO3 IO4
S1 IO1 IO2 CNC 0 NO
S2 IO1 IO4 CNO 0 NO
S3 IO3 IO2 CNO 0 NO
S4 IO3 IO4 CNC 0 NO
R1 CTL 0 1Meg
A1 CTL 0 0 0 0 CNC CNO 0 BUF Vhigh=5 Vlow=0
.model NO SW(Ron=1 Roff=1G Vt=0.5)
.param Ron=1
.param Roff=1G
.ends swfun
.tran 256u
.backanno
.end
```

i. Simple Source Follower

```
* E:\simulations for thesis report\Source followers\simple source
follower.asc
R1 Vout 0 {R}
V1 N001 0 1.8
V2 Vin 0 1.8
M1 N001 Vin Vout 0 NMOS
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\Gopal\Documents\LTspiceXVII\lib\cmp\standard.mos
.include tsmc018um.lib
.step param R 1k 50k 100k
.dc V2 .1 1.8 .1
.backanno
.end
```

j. Flipped Voltage Follower

```
* E:\simulations for thesis report\Source followers\FVF.asc
Mn ix ix N001 N001 CMOSP l=2u w=10u
Mx Vd ix N001 N001 CMOSP l=2u w=10u
M1 Vd Vin Vout 0 CMOSN l=2u w=10u
M2 Vout Vd 0 0 CMOSN l=2u w=10u
V1 N001 0 1.8
Rs ix 0 1k
V3 Vin 0 1.8
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\Gopal\Documents\LTspiceXVII\lib\cmp\standard.mos
.include tsmc018um.lib
.dc v3 0.1 3 .1
.backanno
.end
```

k. Folded Flipped Voltage Follower

```
* E:\simulations for thesis report\Source followers\FFVF.asc
Mn iy iy VDD VDD CMOSP l=.2u w=10u
Mx Vd iy VDD VDD CMOSP l=.2u w=10u
M1 Vd Vin Vout 0 CMOSN l=0.2u w=2u
M2 Vout iz 0 0 CMOSN l=.2u w=10u
V1 VDD 0 3
Rs iy N001 2k
V3 Vin 0 3
M3 Vd Vout iz VDD CMOSP l=.2u w=10u
M4 iz N001 N002 0 CMOSN l=.2U w=10U
M5 N001 N001 0 0 CMOSN l=.2U w=10U
Rs1 N002 0 .5k
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\Gopal\Documents\LTspiceXVII\lib\cmp\standard.mos
.include tsmc018um.lib
.dc V3 0.1 3 0.1
.backanno
.end
```

l. Conventional BGR

```
* E:\simulations for thesis report\voltage reference\conventionalBGR.asc
V1 VDD 0 PULSE(0 1.8 100u 100u 100u 1m 2m)
Q1 0 0 N002 0 PNP
M1 VA VB VDD VDD CMOSP l=2u w=5u
M2 VB VB VDD VDD CMOSP l=2u w=5u
M3 VA VA N002 0 CMOSN l=2u w=10u
M4 VB VA CTAT 0 CMOSN l=2u w=10u
R1 CTAT N004 5k
Q2 0 0 N004 0 PNP
M5 Ref VB VDD VDD CMOSP l=2u w=5u
R2 Ref N003 135k
Q3 0 0 N003 0 PNP
Q4 0 0 N004 0 PNP
M7 VB N001 0 0 CMOSN l=2u w=2u
M6 VDD VDD N001 0 CMOSN l=2u w=1u
M8 N001 VA 0 0 CMOSN l=20u w=80u
.model NPN NPN
.model PNP PNP
.lib C:\Users\Gopal\Documents\LTspiceXVII\lib\cmp\standard.bjt
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\Gopal\Documents\LTspiceXVII\lib\cmp\standard.mos
.tran 4m
.include tsmc018um.lib
.backanno
.end
```

m. Two stage OPAMP

```
* E:\simulations for thesis report\OPAMP\opamp.asc
M3 N001 N001 VDD VDD CMOSP l=.5u w=7u
M4 N002 N001 VDD VDD CMOSP l=.5u w=7u
M6 Vout N002 VDD VDD CMOSP l=0.5u w=88u
M1 N001 VINN N004 0 CMOSN l=0.5u w=2.5u
M2 N002 VINP N004 0 CMOSN l=0.5u w=2.5u
M5 N004 N005 0 0 CMOSN l=0.5u w=6u
M8 N005 N005 0 0 CMOSN l=0.5u w=6u
M7 Vout N005 0 0 CMOSN l=.5u w=38u
C1 Vout N003 600fF
I1 VDD N005 20µ
C2 Vout 0 2pf
Rc N003 N002 1k
V1 VDD 0 1.8
V2 VINN VINP AC 1
V3 VINP 0 0.8
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\Gopal\Documents\LTspiceXVII\lib\cmp\standard.mos
.include tsmc018um.lib
.ac dec 100 .1 1G
.backanno
.end
```

n. Current steering Circuits

```
* E:\simulations for thesis report\current mirror.asc
M2 VDD N002 0 0 CMOSN l=1u w=1.6u
V1 VDD 0 3
M3 VDD N002 0 0 CMOSN l=1u w=3.2u
M4 VDD N002 0 0 CMOSN l=1u w=6.5u
M5 VDD N002 0 0 CMOSN l=1u w=13u
M9 VDD VDD N002 0 CMOSN l=375u w=1u
M1 N002 N002 0 0 CMOSN l=1u w=2u
M6 N001 N001 vdd vdd CMOSP l=1u w=2u
M7 0 0 N001 vdd CMOSP l=77u w=1u
M8 0 N001 vdd vdd CMOSP l=1u w=3.3u
M10 0 N001 vdd vdd CMOSP l=1u w=6.6u
M11 0 N001 vdd vdd CMOSP l=1u w=14u
M12 0 N001 vdd vdd CMOSP l=1u w=1.65u
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\Gopal\Documents\LTspiceXVII\lib\cmp\standard.mos
.include tsmc018um.lib
.tran 1m
.backanno
.end
```