Negative Bias Temperature Instability (NBTI) Monitoring and Mitigation Technique for MOSFET

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Abstract

SEMICONDUCTOR reliability is a growing issue as device-critical dimensions shrink and transistor integration continues to roughly double every 24 months. Aggressive oxide thickness scaling has led to large vertical electric fields in MOSFET devices in which oxide breakdown is a critical issue. These high fields also lead to significant threshold voltage shift over time due to the negative bias temperature instability (NBTI) effect, creating additional uncertainty in device behaviour. In the presence of these degradation mechanisms, it is increasingly difficult to ensure the reliability of ICs over their lifetimes. Since the sensitivity of device lifetime to operating conditions has increased, dynamic control schemes that modulate the voltage, sleep state, and workload of processing elements and circuitry in large systems have been pro- posed. Dynamic control further complicates a priori reliability qualification and makes a case for on-chip structures to be used for real-time estimation of device and circuit degradation.

Although many physical details are still under investigation, it has been widely accepted[2][4] that the electrical field across the oxide causes continuous trap generation in Si-SiO2 interface of transistor. These traps usually originate from Si-H bonds in gate oxide layer [1][4]. These bonds can easily break with time and generate positive interfacial traps (donor-like state). This understanding is described by Reaction-diffusion (R-D) analytical models[1] [2][4]. Amongst of all consequences of generated traps, transistors threshold voltage shift has been most dominant. During the time transistor is under the stress Vth increases, while in the recovery time this Vth shift shrinks, but is never nullified. Due to these Vth shift, circuit operation faces

a significant operational delay for any analog circuits.

In this paper, we explain the influence of Negative Bias Temperature Instability (NBTI) in circuit operation and propose a method for detecting NBTI degradation of circuit in order to design a robust system. NBTI takes place when transistor is negative- biased, which is a usual biasing for PMOS. Due to the sever functional hazard caused by NBTI in an analog circuit operational state, it has become eminent to find a permanent solution for NBTI degradation. However so far the most widely used technology for NBTI degradation mitigation is guard banding, which is overly costly and highly power consuming for analog circuit. As new degeneration of electronic circuits needs to be costffective and at the same time reliable in performance, guard banding can no longer satisfy the demand of a stable and cost-effective circuit based solution for NBTI mitigation. Therefore, our research is based on finding the best possible solution for NBTI degradation. Here, we have proposed an new on chip detection method for NBTI degradation, and using the yield of the detecting circuit we tend to mitigate the NBTI dynamically using DVS (Dynamic voltage Scaling) Technology.

To ...

All my lab mates who sincerely supported my research throughout the whole time.

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Introduction

1.1 Motivation

Since the early days of microelectronics, integrated MOSFET (Metal Oxide Semiconductor Field Effect Transistor) technology has been continuously advanced by dimension shrink. Via the equivalent scaling of relevant processing parameters - channel area, oxide thick- ness and supply voltage - the fundamental device characteristic keeps the same with less area and power consumption. This general feature forms the basis of today ' s triumph of microelectronics and the initiation of the information era.
But MOSFET (Complementary Metal Oxide Semiconductor) - the processing of n- and p- type MOSFETS on one chip - technology scaling has to face some inheritable problems like device noise and process fluctuations, that are given by semiconductor physics, processing imperfections and its atomic limitations. For example, the circuit relevant SNR (Signal to Noise Ratio) reduces for every technology step as voltage headroom is reduced with decreased supply voltage, but device noise contributions remain constant. Since the 0.1 um regime, MOSFET processing migrates to the non-constant field scaling approach, by keeping the supply voltage at higher levels than would be required by the scaling factor, while all other parameters are scaled in the usual way. Here, raised electric fields in MOS devices are accepted at the cost of increased wear out, thus worsening device reliability but maintaining sufficient SNR. At the same time, higher integration rates with increased chip complexity demand for an enhanced device reliability

to maintain a stable and reliable system, which has to be further provided by the MOSFET processing. In the past, this was achieved by the continuing optimization of the chip processing, but the gap between the optimization window and limiting semiconductor physics reduces and device aging mechanisms come to the fore.

Condensed operation of MOSFET devices at only slightly reduced supply voltages further leads to increased on-chip operation temperatures, that even worsen device wear out. On the other hand, reduction in voltage headroom increases circuit sensitivity towards device aging. Advanced MOSFET processing options like the inclusion of novel high-κ materials into the MOS gate stack lowers gate leakage, but further debuts device aging effects that were nonexistent in classic SiO2 or SiON based MOSFET technologies. The general shrink of channel length further induces novel aging effects, that even occur for switched off de- vices. Increased circuit sensitivity and growing appearance of aging effects in magnitude and number involve the reliability topic as an emerging concern in today ' s and future MOSFET microelectronics [1, 2].

The impact of device wear out on circuit level was only rudimentary studied in the past, as occurring minor device parameter drifts were covered by design techniques like guard banding or mitigated by the operation in safe operation area. Contrary to the inherently robust digital circuits, where device wear out mainly leads to an increase of switching delay, analog circuitry is more sensitive towards a change of device characteristics like drive current, transconductance or noise behaviour. The requested compliance of numerous circuit performance specifications to maintain proper system functionality makes reliability proofs for analog circuits more challenging. With the increased appearance of device aging effects in advanced MOSFET technologies, their impact on circuit level demands for future research effort [3]. But also circuit level reliability measurement proofs arise as a challenging task, as an accelerated stress methodology to exactly reproduce equivalent end-of-lifetime states is still missing.

1.2 Aging in Deep-submicrometer MOSFET Technology

Integrated electronic systems with AMS circuits fabricated using MOS technology find a wide range of applications ranging from life critical field; aircraft, pacemaker and automotive, consumer electronics field; television systems, mobile, camera and gaming station, to non-critical field; toys and electronic greeting cards. MOS transistors used in these circuits are expected to degrade (age) with time. This causes the circuit performance to deviate from its specifications measured post fabrication. [3,6]So device and circuit reliability evaluation is of prime practical importance. The recent MOSFET technologies have witnessed slowing down or stopping of supply voltage (V_{DD}) and threshold voltage (V_{th}) scaling because of the non-scalability of sub-threshold slope whereas the transistor gate length (L) and thickness of gate oxide (tox) is continuing to scale down. This results into a net increase in lateral electric field, effective channel field and the vertical oxide field. Moreover, with scaling of device geometry and the increase in device number, power consumption rises resulting into rise in the operating temperature which produces another big issue with respect to device reliability. The introduction of first nitrogen and then high-κ in the gate oxide stack has lead to enhancement of oxide degradation in both pMOSFET and nMOSFET devices. This leads to enhancement of different aging degradation mechanisms in the integrated circuits fabricated using state-of-the-art deep sub-micrometer MOSFET technology.

Aging degradation mechanisms can be classified into destructive and non-destructive categories, depending on if it leads to transistor hard failure (e.g. gate-oxide breakdown) or wearout (e.g. bias temperature instability (BTI), conducting, non-conducting hot car- rier injection (CHCI, NCHCI)). Hard failures due to destructive stress are completely unacceptable since it can partially or completely disrupt the functionality of the circuit.[14]

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non-conducting hot carrier injection (CHCI, NCHCI)). Hard failures due to destructive stress are completely unacceptable since it can partially or completely disrupt the functionality of the circuit.[12]
On the other hand wearout mechanisms due to the non-destructive stress are acceptable unto a limit which is defined by the desired circuit accuracy and precision. So to pre- dict if the circuit meets the target lifetime expectation, performance degradation over lifetime under non-destructive stress effects must be analyzed by the designer. Accurate prediction of aging degradation is important to avoid expensive re-spins, for gaining the consumers trust and to correctly define the warranty period and cost of the product. In order to perform quick practical aging predictions to evaluate the lifetime reliability of an integrated circuit, it is necessary to map the end-of-life use case condition of the product (e.g. mobile phone use case of 4 Years, 85C, 105% of worst case VDD) to an meaningful and accurately mapped accelerated stress condition (e.g. 103s, 125C, 120% of worst case VDD). For these evaluations the AMS circuit is assumed to be well designed and functioning perfectly at time zero. This acceleration allows the stress conditions to shrink the 4 year product life to a 103s period so the reliability of the circuit can be studied in laboratory and guaranteed. The shrinking in lifetime of a MOSFET device is possible by elevating the stress temperature, bias voltages and time[3,9,28].

1.3 Impact of Aging on Analog and Mixed Signal Circuits

Current mirror, operational amplifier and bandgap reference circuits are some of the very basic building blocks of AMS systems. The precision and accuracy of these basic building blocks is linked to the matching of the transistor pairs as illustrated in figure 1.2. The reliability performance of all such matched pair circuits depends closely on their aging differential. Analog circuits always witness DC voltages for biasing purposes irrespective of the input signal unlike digital circuits. Further in addition to the applied DC bias voltages, a high temperature may also exist on the chip because of the high transistor density. Thus the failure

rate varies as a function of stress voltage, temperature and time. Further the maximum allowed margins of process and aging degradation induced parameter drifts and variations are lower for analog applications and high resolution mixed signal circuits [2].

The transistors in typical AMS circuit are operated either in active mode or power down mode. Operation in either of these modes can induce aging degradation in the transistors depending on the surrounding bias conditions [3]. In the circuit active mode,the transistors are usually operated in saturation region with gate to source overdrive voltage$V_{od} = |V_{gs} - V_{th}|$ of around several 100mV and drain to source voltages $|V_{ds}| > |V_{od}|$. Diode connected transistors are less prone to aging degradation due to their low biasing values with $|V_{gs}| = |V_{ds}|$. Other transistors can see high voltage conditions enough to induce aging degradation due to BTI and/or HCI depending on the input signals and the circuit configuration (closed loop, open loop, feedback, etc.). Asymmetrical input signals lead to aging degradation induced offset voltages in matched differential pairs [4].

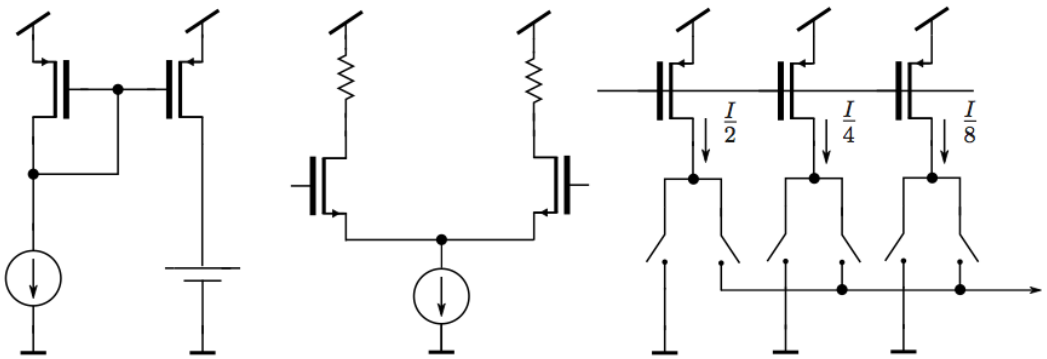

Figure 1.1: Matching sensitive analog and mixed signal circuits -

In a typical power down mode the bias currents are switched off to avoid power consumption of the inactive circuit, but the supply voltages are not driven down in order to allow for fast reactivation of the circuit. In this case the potentials of the internal nodes are determined by the input signals and the sub-threshold or off state leakage currents of the transistors. All the transistors connected in

the current mirror configuration are not prone to aging degradation in this case because the diode connected transistors lead to low gate voltages. The remaining transistors can be affected by BTI stress depending on the input signals.
In case of specific circuits like ring oscillator the transistors see high gate to source voltages ($|V_{gs}|$), being switched between VDD and VSS leading to BTI and NCHCI degra- dation. Also the transistor here experience high drain to source voltage ($|V_{ds}|$) during signal transition phase resulting into degradation due to CHCI. CMOS transistor switches with bi-directional current flow typically used in switched capacitor circuits experience similar stress conditions like the transistors in the ring oscillator circuit but with lower $|V_{ds}|$ values resulting into low CHCI and NCHCI degradation.
Thus accurate evaluation of aging degradation is required on circuit level to obtain realistic risk evaluation for precise reliability qualification. Simply sizing up devices, such as is done to reduce process variation and HCI effects offers little relief to NBTI and PBTI degradation effects on circuits. The AMS circuit designers need to move one step further to include device aging impact into consideration, so that the circuit can meet the specifications at end-of-life (E_{oL}). Special circuit techniques are needed as countermeasure for these aging degradation effects [5].

1.4 State-of-the-Art in Circuit Reliability Research

Previous circuit design mostly treated device aging as a side effect, that is covered by design margins applied for balancing PVT (Process Voltage Temperature) variations. Nowadays, device aging obtained an individual status as growing source of device vari- ability in the extension to PVTA (Process Voltage Temperature Aging) variations. Grow- ing interest on device degradation lead to several studies on the impact of device aging on circuit level. For digital logic circuits the general aging induced weakening of the de- vice characteristic increases logic gates' switching delay and so induces a time dependent degradation of the data evaluation. This increase of propagation delay can lead to a time dependent violation of timing constraints in the critical path and so to failure of the circuitry [4, 5,

6]. Several detection and sensing approaches, for example using replica circuits to provide a kind of aging odometer [7], are developed and countermeasures are proposed [8]. A general approach to detect and compensate for PVTA variation induced logic errors is treated in [9]. Another relevant field of research is the digital SRAM (Static Random Access Memory), as reliable data storage has to be guaranteed with minimum feature size devices for millions of cells. Reliability investigations revealed, that device degradation in the asymmetric storage state varies SRAM cell stability [10, 11]. Due to the minimum feature size devices, process variations and variations in the degradation effect as well play an important role for the reliability of the storage system. Transient components in device degradations additionally include a time dependent component for the cell stability [12]. For analog and mixed-signal circuits, performance characteristics and thus device aging impacts are more complex [13].

In the study on selected amplifiers of Martin-Martinez, variability is identified as the major concern for advanced MOSFET technologies, which is accompanied by aging induced drift contributions. Variability in the aging effect itself was found to be of minor concern. The study further reveals that aging impacts amplifier gain and GBW (Gain Band Width) dependent on the circuit topology [19]. A detailed investigation on the effect variability for the used devices as well as a general statement on aging sensitive topologies is still missing. In the fundamental work of Thaws, a state-of-the-art differential amplifier is used to study analog circuit reliability according to numerous aging effects. From the point of view of distinct circuit operation states, occurring device stress and resulting aging effects are determined. Aging effects are again expected to degrade circuit performance in offset, gain, noise and linearity. Here, BTI (Bias Temperature Instability) effects, induced by high oxide fields, are expected to arise as the most prominent challenges in future robust circuit design [10]. HCI (Hot-Carrier Injection) is beneficially used to perform calibration of an SRAM sense amplifier [11]. With an automated reliability simulator, an ADC (Analog to Digital Converter) circuit is studied with respect to the impact of device aging by Yan [2]. Several countermeasures like device sizing for improved HCI degradation or a reduction of power consumption to reduce NBTI (Negative Bias Temperature Instability)

aging are evaluated. Nevertheless, a deep understanding of the interaction between device degradation and circuit behaviour is still missing.
In [13], Jha investigated the impact of NBTI on selected basic analog circuit blocks like current mirrors, amplifiers and a current-steering DAC (Digital to Analog Converter). The study showed that device aging impact strongly depends on the circuit topology. For the current mirror circuits for example, huge differences in general aging sensitivity can be seen. Investigations on amplifier circuits reveal large aging induced offset generation for open-loop comparator operation. Due to stable current biasing, transconductance of the circuit remains stable and further impact on performance parameters like gain or GBW are small. For the current-steering DAC, NBTI degradation is expected to induce considerable gain errors, but only minor impact on its linearity. This study shows that sensitivity of the analog circuit strongly depends on its configuration. However, universal rules for aging robust circuitry are not provided.
Further analog circuit types, that are in the focus of reliability investigations, are LC based VCO (Voltage Controlled Oscillator) circuits. This is mainly due to the high volt- age swings during circuit operation [4, 5]. In his study, Lin revealed considerable VCO performance degradations related to HCI device degradation [6]. Sadat showed in [7] that degradation of active bridge devices impacts oscillation amplitude and thus the effective value of the tank capacitance, that further modifies oscillator Phase Noise and startup behaviour. Current-reusing MOSFET VCO designs are determined to be the most reliable oscillator topologies due to amplitude limitation by the voltage supply. In [8], Reedy reported a significant VCO Phase Noise degradation in the close-in region related to a NCHCI (Non-Conductive Hot-Carrier Injection) induced worsening in device flicker noise - a device characteristic, that is typically not considered in todays aging prediction models.

Several studies in the past years showed the increasing impact of device aging on analog circuit blocks and further brought up the most critical analog circuit types. Nevertheless, a throughout and universal study performed on state-of-the-art analog circuit designs, providing insight into the mechanisms of the circuit related impact of device aging, is still missing. Analog circuit related device aging taking into consideration typical device dimensions and operation states has to be

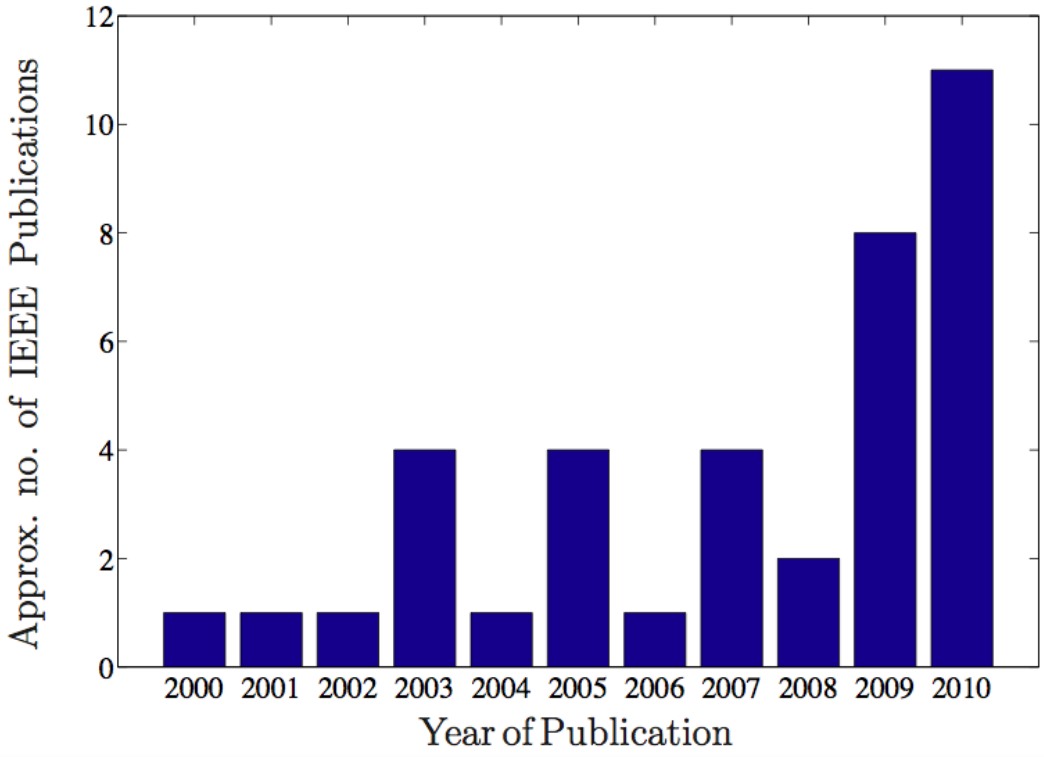

Figure 1.2: IEEE publications in the field of analog and mixed signal circuit reliability -

investigated in detail for advanced MOSFET technologies, to reveal analog related degradation behaviour as well as expected variations of the aging mechanisms. Selected circuit designs have to be investigated with respect to their general aging sensitivity to establish approaches for future robust circuit designs. Novel circuit aging modelling approaches, expanding results from circuit reliability simulations, will provide deep understanding of device aging and circuit interaction and will break new ground for aging countermeasures and circuit stress testing as well.

1.5 NBTI degradation

As the device dimensions in metal-oxide-silicon (MOS) technologies have been continuously scaled down, a phenomenon called negative bias temperature instability (NBTI), which refers to the generation of positive oxide charge and interface traps in MOS structures under negative gate bias at elevated temperature, has been gaining in importance as one of the most critical mechanisms of MOS field effect transistor (MOSFET) degradation. NBTI effects are manifested as the changes in device threshold voltage (V_T), transconductance (gm) and drain current (ID), and have been observed mostly in p-channel MOSFETs operated under negative gate oxide fields in the range 2 - 6 MV/cm at temperatures around 100 $^\circ$ C or higherThe phenomenon itself had been known for many years, but only recently has been recognised as a serious reliability issue in state-of-the-art MOS integrated circuits. Several factors associated with device scaling have been found to enhance NBTI: i) operating voltages have not been reduced as aggressively as gate oxide thickness, leading to higher oxide electric fields and increased chip temperatures; ii) threshold voltage scaling has not kept pace with operating voltage, resulting in larger degradation of drain current for the same shift in threshold voltage; and iii) addition of nitrogen during the oxidation process has helped to reduce the thin gate oxide leakage, but the side effect was to increase NBTI .
Considering the effects of NBTI related degradation on device electrical parameters, NBT stress-induced threshold voltage shift (ΔV_T) seems to be the most critical one, and a couple of basic questions, which are to be addressed now, are why the NBTI appears to be of great concern only in p-channel devices, and why the negative bias causes more considerable degradation than positive bias.

The bias temperature stress-induced V_T shifts are generally known to be the consequence of underlying buildup of interface traps and oxide-trapped charge due to stress-initiated electrochemical processes involving oxide and interface defects, holes and/or electrons, and variety of species associated with presence of hydrogen as the most common impurity in MOS devices . An interface trap is an interfacial trivalent silicon atom with an unsaturated (unpaired) valence electron at the SiO2/Si interface. Unsaturated Si atoms are additionally found in SiO2 itself, along with other oxide defects, the most important being the oxygen vacancies.

Si atoms in the oxide are concentrated mostly near the interface and they both act as the trapping centres responsible for buildup of oxide-trapped charge. Interface traps readily exchange charge, either electrons or holes, with the substrate and they introduce either positive or negative net charge at interface, which depends on gate bias: the net charge in interface traps is negative in n-channel devices, which are normally biased with positive gate voltage, but is positive in p-channel devices as they require negative gate bias to be turned on. On the other hand, charge found trapped in the centres in the oxide is generally positive in both n- and p-channel MOS transistors and cannot be quickly removed by altering the gate bias polarity. The absolute values of threshold voltage shifts due to stress-induced oxide-trapped charge and interface traps in n- and p-channel MOS transistors, respectively, can be expressed as :

$$\Delta V_{Tn} = \frac{q\Delta N_{at}}{C_{ox}} - \frac{q\Delta N_{it}}{C_{ax}} \tag{1.1}$$

$$\Delta V_{Tp} = \frac{q\Delta N_{at}}{C_{ox}} - \frac{q\Delta N_{it}}{C_{ax}} \tag{1.2}$$

where q denotes elementary charge, Cox is gate oxide capacitance per unit area, while ΔN_{to} and $\Delta N_{ti}$are stress-induced changes in the area densities of oxide-trapped charge and interface traps, respectively. The amounts of NBT stress-induced oxide-trapped charge and interface traps in n- and p-channel devices are generally similar[2], but above consideration clearly shows that the net effect on threshold voltage, ΔV_T, must be greater for p-channel devices, because in this case the positive oxide charge and positive interface charge are additive.

As for the question on the role of stress bias polarity, it seems well established that holes are necessary to initiate and/or enhance the bias temperature stress degradation[4], which provides straight answer since only negative gate bias can provide holes at the SiO2/Si interface. Moreover, this is an additional reason why the greatest impact of NBTI occurs in p-channel transistors since only those devices experience a uniform negative gate bias condition during typical MOSFET circuit operation.

Several models of microscopic mechanisms responsible for the observed degradation have been proposed, but in spite of very extensive studies in recent years, the mechanisms of NBTI phenomenon are still not fully understood, so technology optimisation to minimise NBTI is still far from being achieved. With reduction in gate oxide thickness, NBT stress-induced threshold voltage shifts are getting more critical and can put serious limit to a lifetime of p-channel devices having gate oxide thinner than 3.5 nm, so accurate models and well established procedure for lifetime estimation are needed to make good prediction of device reliable operation.

Though the gate oxide in nanometre scale technologies is continuously being thinned down, there is still high interest in ultra-thick oxides owing to widespread use of MOS technologies for the realisation of power devices. Vertical double-diffused MOSFET is an attractive device for application in high-frequency switching power supplies owing to its superior switching characteristics which enable operation in a megahertz frequency range.

High-frequency operation allows the use of small-size passive components (transformers, coils, capacitors) and thus enables the reduction of overall weight and volume, making the power MOSFETs especially suited for application in power supply units for communication satellites, but they are also widely used as the fast switching devices in home appliances and automotive, industrial and military electronics. Degradation of power MOSFETs under various stresses (irradiation, high field, and hot carriers) has been subject of extensive research (, but very few authors seem to have addressed the NBTI in these devices [3]. However, power devices are routinely operated at high current and voltage levels, which lead to both self heating and increased gate oxide fields, and thus favour NBTI. Accordingly, NBTI could be critical for normal operation of power MOSFETs though

they have very thick gate oxides.
Given the above considerations, this chapter is to cover the NBTI implications on reliability of commercially available power MOSFETs. In the next section, we will describe the experimental procedure for accelerated NBT stressing applied in our study and analyse typical results for the threshold voltage shifts observed in stressed devices. Applicability of some empirical expressions for fitting the dependences of stress-induced threshold voltage shifts on stress conditions (voltage, temperature, time) to our experimental data will be discussed as well. Third section is to describe in details the results of the procedure applied to fit the experimental data and estimate the device lifetime by means of several fitting and extrapolation models. Impacts of stress conditions, failure criteria, models used for fitting and extrapolation, and intermittent annealing on lifetime projection will be discussed as well. The extrapolation models available in the literature offer only extrapolation along the voltage (or electric field) axis and provide lifetime estimates only for the temperatures applied during the accelerated stressing, so in the next section we propose a new approach, which requires double extrapolation along both voltage and temperature axes, but can estimate the device lifetime for any reasonable combination of operating voltages and temperatures, including those falling within the ranges normally found in usual device applications. Finally, most important findings presented in the chapter will be summarised in the conclusion section.

1.6 Contribution of this work

In this work a detailed overview over major device NBTI aging effects, leading to parametric drifts of device characteristics, but not to a hard destruction of the device is provided. Most recent findings on distinct effect physics and resulting aging prediction model approaches are discussed. Options for consideration of device degradation in classic circuit simulations are reviewed with respect to analog circuit simulation suitability.
Device NBTI degradation for typical analog operation scenarios for an advanced MOSFET process technology is studied by simulation and stress measurements. In doing so, analog related device NBTI ageing degradation not entirely covered

by state-of-the-art modelling is investigated in detail, taking into consideration typical operation states, device dimensions and analog relevant effect properties. Operation modes like accumulation, which are not considered so far and potentially occur during circuit standby, are shown to be another significant reliability issue. Further investigations on aging effect variability as well as transient recovery re- veal the need for novel aging models, that are close to the basing physics. Additionally, it is shown that degradation effects can be beneficially used also for passive reliability improvement.

Throughout investigations on device aging impact on a wide area of analog circuit build- ing blocks are the foundation for a general overview of major circuit aging monitors and the behaviour dependent on the operation state. For instance, current mirror circuits experience current mismatch, amplifiers offset and oscillators power degradation. Further case studies on distinct device and circuit types like varactors and reference generation circuits showed a minor impact of device wearout.

Circuit level aging is very complex, due to the simultaneous interaction of distinct device degradation effects and distinct dominant effects are not per se detectable. A general methodology to accurately predict aging on circuit level is performed via fully analytic modeling of circuit behaviour, that further provides a deep insight into major effect contributions. This approach allows to derive further aging related design concepts and to easily account for circuit level degradation in future MOSFET process technologies.

Via circuit degradation models, a methodology to accurately determine end-of-lifetime equivalent circuit states for accelerated stress test is developed and validated via meaurement for selected circuit types. Furthermore, customized circuit type specific stress testbenches are developed and described providing the ability to stress and measure cir- cuit performance in one test setup. This novel approach allows to use analog circuits ' signal sensitivity for further aging effect characterisation, like device flicker noise degra- dation in oscillator Phase Noise behavior or short-time recovery in fast amplifier circuits. Design related aging countermeasures for reliable analog circuit operation are proposed and evaluated. Furthermore, a novel method to suppress device aging and simultaneously use the induced device parameter drift for circuit calibration is proposed and verified

via measurements. From the overall findings and circuit investigations, guidelines for design of reliable analog circuits are established.

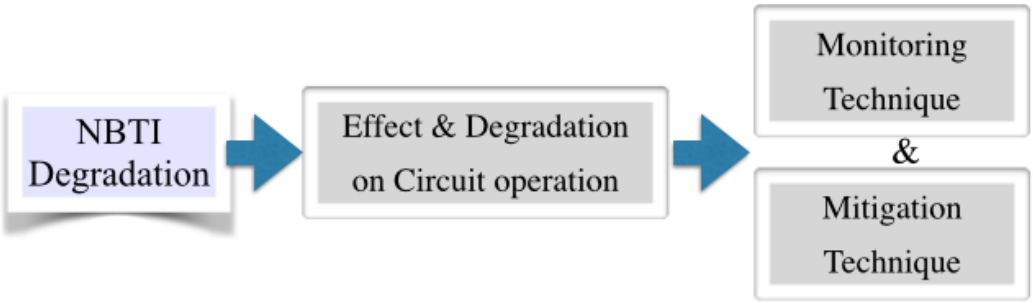

Figure 1.3: Aim of this work - flow of research

In this research we have emphasise on NBTI degradation model and its effect on circuit (analog circuit) operation. As it is obvious that NBTI degradation have a sever effect on circuit operation and parameters, i derives that operational mismatch can certainly be the target criteria to measure NBTI circuit degradation. In this research we have come to the conclusion that the most mentionable NBTi degradation effect an anolog circuit have on its operation is the slew rate degradation and by measuring the rate of slew rate degradation, we can not only determine the existence of NBTI but also the rate of the degradation. As rate of NBTI degradation differs from chip to chip, it can never be predicted accurately while designing the circuit, Therefore an on-chip detection circuit is necessary, which we have proposed using TTC (Time Transient Circuit) monitoring circuit. As shown in fig 1.3, we have stretched our research from on chip monitoring to mitigation technique as well. As we will describe the process in the later part of this paper, we have used DVS (dynamic Voltage Scaling) System to compensate the effect of NBTI degradation on chip. As a system we proposed a new NBTI robust system for analog circuit in this research.

2

Aging Physics

2.1 MOSFET Device Wearout

As most technical products, also integrated MOS (Metal Oxide Semiconductor) devices suffer from wearout due to their usage in electronic devices. High integration in today's ICs (Integrated Circuits), with billions of MOS transistors on one die, demands MOS (Metal Oxide Semiconductor) insulator thickness of a few nanometers between the controlling gate and the channel. Electric fields across the oxide reach MV/cm although operating in the 1V regime. Those lead to a time dependent wearout of insulators' properties inducing changes in the device characteristics or in worst case to its breakdown. As mentioned in 1.3, technology scaling by inducing non-constant field scaling and inclusion of new materials in the gate stack worsens this wearout from technology node to node.
Aging mechanisms can be separated in two groups: mechanisms leading to drift of device characteristics, but not to an immediate malfunction of the transistor - the so called non- destructive aging mechanisms, including BTI and HCI effects. And the destructive mechanisms like TDDB (Time Dependent Dielectric Breakdown)[29, 30] leading to a permanent malfunction of the device. Precursors to the TDDB are the SBD (Soft Breakdown) effects inducing a temporary breakdown of the device. After stress removal, device is working again.
Our investigation on analog circuit aging addresses the non-destructive aging mechanisms, as those are able to change circuit behaviour during lifetime operation. In advance to a dielectric breakdown a huge amount of parameter drift

occurs, also acting as a precursor to the hard breakdown. From the system point of view it is not only the hard break- down of an incorporated device leading to malfunction, but also drifts in performance specifications of the analog circuit can lead to failure of the overall system.

2.2 Impact on Device Parameters

All non-destructive aging mechanisms have in common that insulator wearout is due to inclusion of charge into the insulator region. This additional charge changes device characteristic in several ways. As derived in lots of semiconductor textbooks, threshold voltage V_{th} of an exemplary nMOS (see fig.) with zero Bulk-Source voltage $V_{BS} = 0$ is defined as the inversion mode Gate voltage where electron (minority carrier) density in the inversion region is equal to hole (majority carrier) density of the bulk in thermal equilibrium [31, 32].

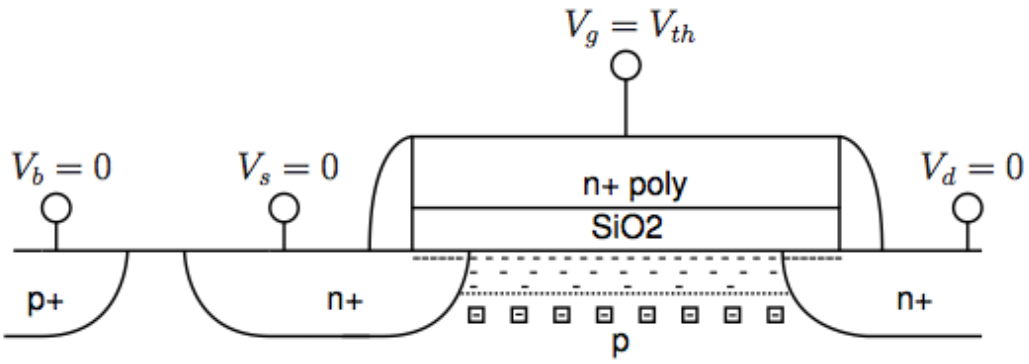

Figure 2.1: nMOS: threshold voltage virgin device -

The physical representation of the threshold voltage condition is given by:

$$V_{th} = V_{FB} + 2\Phi_F + \gamma_n\sqrt{(2\Phi_F)} \tag{2.1}$$

with VF B the flatband voltage, Φ F the Fermi level from intrinsic Fermi level and γ n the Body factor for a nMOSFET, that is dependent on the bulk doping and the dielectric constant of the insulator.A uniformly distributed charge Qdeg

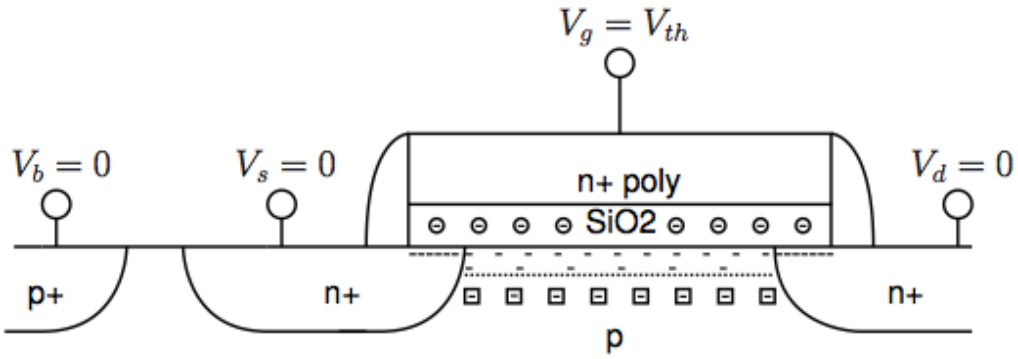

Figure 2.2: nMOS: threshold voltage degraded device -

in the interface to the insulator, as depicted in fig.2.2 would shift the flatband voltage to

$$V_{FB} = \Phi_{MS} + \frac{Q_{deg}}{C_{oxide}} \tag{2.2}$$

with Φ_{MS} the workfunction difference between gate material and bulk and C_{oxide} the gate oxide capacitance. Depending on the amount of generated charge, V_{FB} and so V_{th} is shifted by

$$V_{th,n} = \Delta V_{FB} = -\frac{Q_{deg}}{C_{oxide}} \tag{2.3}$$

Equation (2.3) also shows that the direction of the V_{th} shift depends on the polarity of the generated charge. Furthermore, induced oxide charges also impact field dependent effective channel mobility μ_{eft}.Equation(2.4) shows there lation of μ_{eff} with respect to device operation condition.

$$\mu_{eff} = \frac{\mu_0}{1 + \Theta(V_g - V_{th,n})} \tag{2.4}$$

with μ_0 the low field surface mobility, Θ the mobility degradation coefficient and V_g the gate voltage.Equation(2.4)revealsadirectrelationof μ eff to a drift in thresholdvoltage [33]. But also μ_0 can be affected by oxide charges at the Si $-$ SiO2 interface acting as Coulomb scattering centers and changing the interface roughness and hence μ_0 and Θ [34]. The often discussed degradation of further device parameters as drain current ID , transcon- ductance gm, subthreshold

swing SS or MOS C − V characteristic can be related to the drift of basic MOS parameters V_{th} and μ_0 . These general impacts of device wearout were derived for an exemplary nMOS device, but are also valid for the pMOS counterpart.

2.3 Bias Temperature Instability (BTI)

NBTI for pMOS as well as PBTI (Positive Bias Temperature Instability) for nMOS transistors are derived from the typical inversion mode operation of CMOS devices and their degradation behavior under elevated temperatures. Both effects lead to a general weakening of the transistor characteristic. BTI degradation is strongly dependent on the oxide field given by eq. (2.5) for strong inversion,

$$F_{el,ox} = \frac{V_g - V_{FB} - 2\Phi_F}{t_{ox}} \tag{2.5}$$

with V_{FB} the flat band voltage, Φ F the Fermi Potential defined by the well doping and the lattice temperature and tox the insulator thickness. As shown by eq. (2.5), Vg and tox are key parameters for the BTI degradation.
BTI effects, especially the NBTI in pMOS transistors, were already observed in the early days of MOSFET development [35]. In this decade NBTI was not concerned as a major reliability issue as impact on the formerly buried channel with n+ poly gate for the pMOS was small. Due to constant field scaling in CMOS technology development, that means a similar scaling of Vg and tox, NBTI was well controlled. Changeover to surface channel p+ poly gate pMOSFET increased the NBTI sensitivity. Particularly, the introduction of non-constant field scaling in sub-0.1 μ CMOS technologies, typically keeping or slightly decreasing Vg but scaling tox in the classic manner, enhanced NBTI as one major degradation mechanism. A corresponding PBTI for nMOS transistor was negligibly small for SiO2 based oxides, but emerged with the introduction of high-κ materials in advanced CMOS technologies also for the nMOS transistor [36].

2.3.1 NBTI in pMOSFETs

Figure 2.3 shows the inversion mode NBTI stress condition and the resulting oxide degradation for an exemplary pMOSFET - the transistor ' s deep triode region with zero voltage drop over the channel. Source, Drain and Substrate are connected to ground and Vg is set to a high negative value inducing an inversion layer in the n-well and an accumulation layer in the Source and Drain overlap regions. The electric field in the insulator on the inverted channel is given by eq. (2.5). Under high $F_{el,ox}$, oxide quality degrades by the trapping of charge. Insulator degradation also happens in the Source/Drain overlap regions, but with minor impact due to the distance to the controlled inversion channel. Fig. 2.4 shows the situation for a pMOS device in saturation region. Also in this operation mode NBTI degradation occurs, but due to the decreasing electric field from the Source to the Drain region with smaller total degradation [34].

Lots of literature on NBTI and its involved mechanisms for differing CMOS gate stacks is available. Due to strong sensitivity towards processing and included materials, lots of differing degradation numbers and effect explanations exist. The general accepted mech- anisms are the generation of interface states at the substrate oxide interface and the electric activation of oxide charges, that is due to the activation of pre-existing defects or generation of new defects in the insulator [37]. According to one theory, an interface state is created by the release of hydrogen saturating an open Si bond at the substrate oxide interface. The remaining dangling bond is an electrically active defect with an en- ergy distribution throughout the Si bandgap. It can be occupied by an electron or hole, but for pMOS in inversion mode it is positively charged [38]. The electric field induces a diffusion of the remaining hydrogen through the insulator. As this interface state gen- eration process was believed to be the dominant NBTI contributor, the widely-used RD (Reaction Diffusion) model was developed for NBTI prediction [39]. More recently, oxidecharges were believed to be dominant to NBTI. These traps are neutral when discharged and are positively charged when occupied by holes. Former modeling explained positive oxide charge is due to trapping of H+ from the RD process, but recent findings revealed that hole

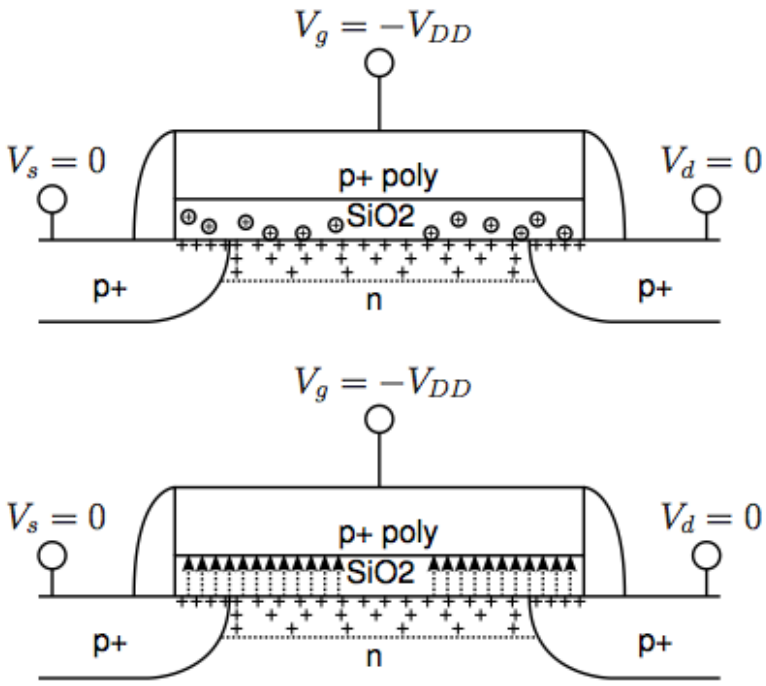

Figure 2.3: pMOS in triode operation - : NBTI stress generated defects and arising electric field under NBTI stress

traps and their precursors already exist in the oxide before stress is applied [40].

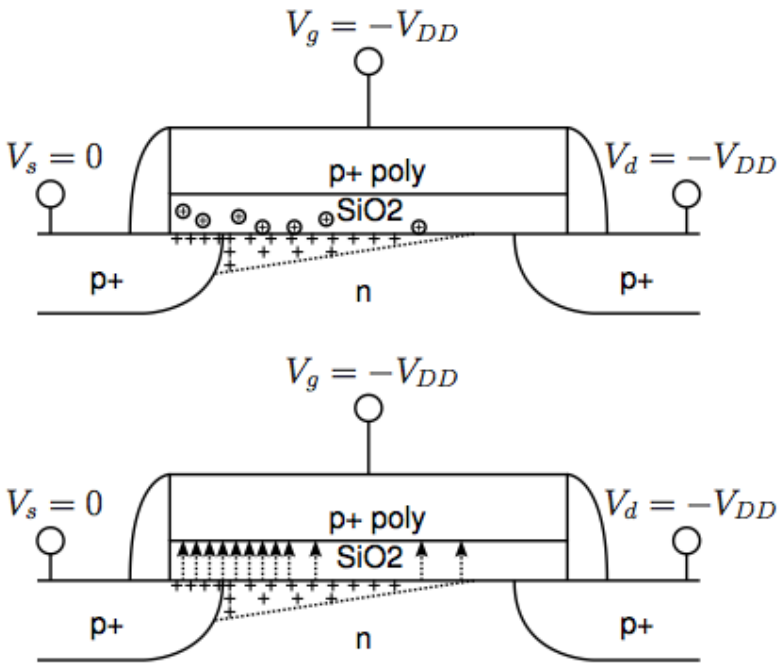

Figure 2.4: pMOS in saturation operation: - NBTI stress generated defects and arising electric field under NBTI stress

NBTI recovery was controversially discussed for long times, but its investigations revealed a deeper understanding of NBTI degradation mechanisms. As recovery immediately sets in when stress is removed, the time delay between stress and aging monitor measurement is very important. This undefined delay in published NBTI data is also one origin of the lack in NBTI understanding. In recent years a lot of effort was performed measuring degradation during stress to find the whole amount of contributing effects [41, 42, 43, 44]. Early understandings divided NBTI characteristic into two components, a recovering one and a permanent part. Controversial results assigned effect recovery to passivation of interface traps [45] or hole detrapping [42]. Also investigations for enhanced recovery under accumulation mode did not reveal a distinct recovery origin [46, 47]. Reisinger ' s ultra-fast Vth measurement method to monitor recovery after

stress, revealed for small dimension devices a stepwise recovery curve indicating the discharge of single defects with differing contributions in step size, which can be related to the random position of channel dopants and insulator defects. In a large area device this single defect recovery is masked by the huge number of defects and the small impact of each defect recovery to the overall device Vth, leading to the classic log(t) NBTI recovery behavior, which is in- compatible with the RD model [48]. Defect relaxation behavior was related to the model of low frequency noise/flicker noise or its manifestation as RTN (Random Telegraph Noise) and extended to the BTI timing range with individual capture and emission times for each defect [49, 50, 48]. With the adapted RTN characterisation technique TDDS (Time Dependend Defect Spectrocopy) from Grasser, it was shown that general BTI isdue to a thermally activated capture and emission of holes and electrons in oxide traps - called SOT (Switching Oxide Traps) [40, 51]. Capture and emission time constants are vastly distributed from nanoseconds to months or even longer. Investigations revealed that metastable states of these defects contribute an additional noise portion and scaling to nanometer devices can lead to very large induced variations due to high defect step sizes of a very small number of defects per device.
Changing the insulator materials from SiO2 to SiON or high-κ stacks also changes the NBTI degradation. For SiON devices nitrogen portions should be located rather to the Gate/insulator than to the substrate/insulator interface for improved NBTI degradation [38]. High-k based gate stacks also show similar NBTI degradations compared to SiO2 and SiON data [52]. Fernandez showed that NBTI is strongly DF (Duty Factor) depen- dent, but shows a flat AC degradation behavior up to the GHz range [53], which is in line with SOT model from Grasser. From recent findings, Kaczer proposes to migrate to SiGe buried channel pMOSFETs to guarantee limited NBTI/pMOS degradation in future CMOS technology nodes [37].

2.3.2 PBTI in nMOSFETs

Corresponding to pMOSFET ' s NBTI, a PBTI arise in nMOSFETs in inversion operation. PBTI degradation was negligibly small in SiO2 and SiON technologies, but arises with similar orders of magnitudes in high-k technologies. Fig. 2.5 shows the inversion

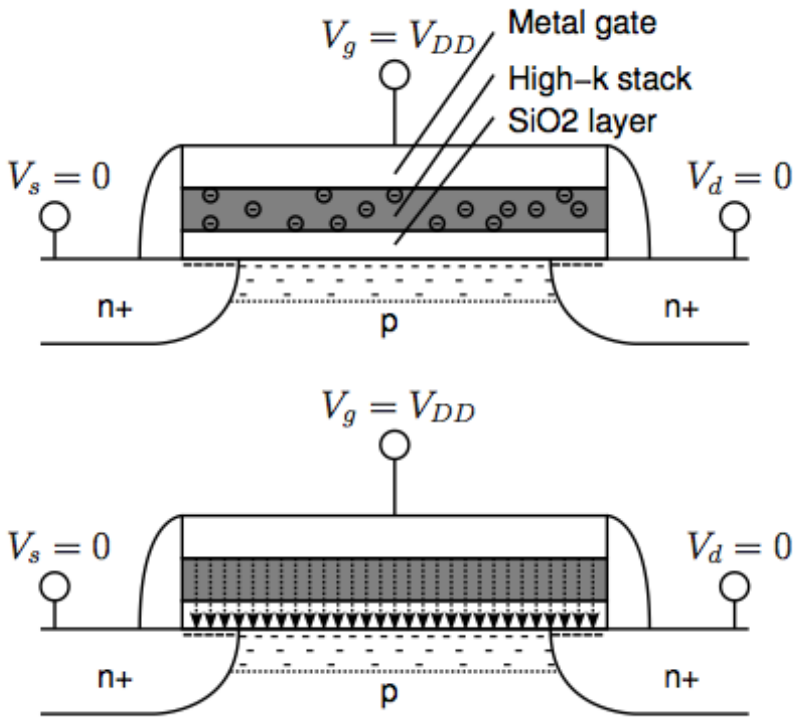

Figure 2.5: High-κ nMOS in triode operation: - PBTI stress generated defects and arising electric field under PBTI stress

mode stress condition and its degraded insulator in deep triode region for an exemplary high-κ nMOS. Contrary to classic pMOS/NBTI, oxide degradation occurs in the high-κ portion of the Gate stack [36]. Due to intermediate SiO2 layers at the substrate insulator interface, nMOS/PBTI degradation is located in a certain distance from the inversion channel, thus mainly impacting threshold voltage V_{th} with almost no effect on channel mobility μ_0 [24]. Similarly to NBTI/pMOS degradation, also PBTI/nMOS shows a concentrated degradation near the Source in saturation operation resulting in a reduced total degradation

compared to the deep triode region operation (see fig. 3.6).

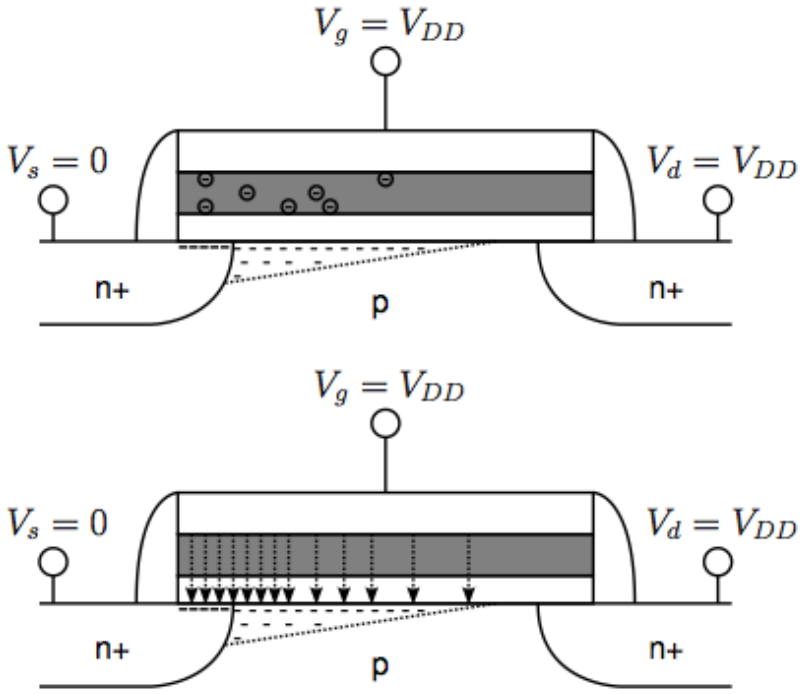

Figure 2.6: High-κ nMOS in saturation operation: - PBTI stress generated defects and arising electric field under PBTI stress

As nMOS/PBTI in high-κ processes compared to pMOS/NBTI is a very new type ofdegradation mechanism and due to the controversial discussion and explanation for the classic pMOS/NBTI, most BTI related investigations concentrate on a deeper under- standing of pMOS/NBTI. Nevertheless, there is a general consensus that nMOS/PBTI degradation is due to charge trapping in the high-κ or related capping layers [25, 26, 27, 26]. High-κ CMOS processing - especially the gate stack with its specific arrangement of interface and capping layers - is a very confidential matter of semiconductor companies. Due to specific processing, differing nMOS/PBTI degradation results are available. Some investigations report a PBTI turnover phenomenon - an enhancement or weakening of the nMOS characteristic as a function on time depending on the bias and tem-

perature stress condition. This observation indicates a multiple polarity defect trapping [38, 39]. Recent results for HfO2 based high-κ processes linked the major parts of PBTI degradation to electron trapping at oxygen vacancies [37]. Early investigations on nMOS/PBTI tried to model PBTI degradation with an adapted RD explanation from NBTI modeling, but neglected PBTI relaxation phenomena [58]. nMOS/PBTI relaxation is similar to pMOS/NBTI behavior, showing defect relaxation in a vast timescale from sub-microseconds to months. The promising SOT approach also fits well for PBTI degra- dation, its relaxation behavior and AC voltage stress degradation dependency [40, 25]. A possible option to reduce nMOS/PBTI degradation in HfO2 based processes is the inclusion of group III elements to passivate oxygen vacancies [30].

2.3.3 BTI degradation trend in MOSFETs

Aging investigations in this work restrict to some application relevant EOL (End-of- Lifetime) use cases. Thereby operation conditions representing a typical use case or worst case scenario according to the intended application are assumed and circuit performance is evaluated in the corresponding end-of-lifetime state. For simplicity, only few use cases are used in this work, given in tab. 2.1. A good overview of commonly used ones for industrial applications are given in the JEDEC standard [29].

EOL Use Case	**V**	**T**	t
General	VDD	125 ° C - 85 ° C	10y
MP (Mobile Phone)	VDD,WC +5%	85 ° C	4y
Combined	VDD,WC +5%	85 ° C	10y

Table 2.1: Application related aging use cases

A reason for the accomplishment of this work can be determined from the following evaluation of aging effects ' evolution. Here, major degradation mechanisms and their behavior towards selected stress parameters are depicted and compared for the most recent CMOS technology nodes.

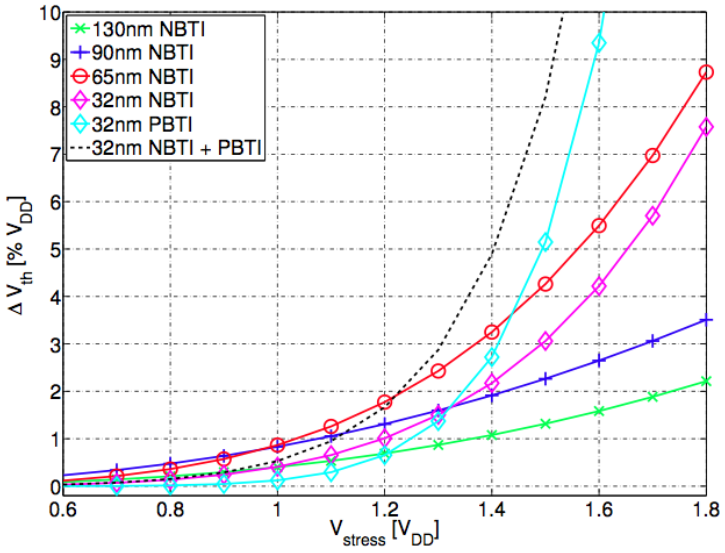

Figure 2.7: BTI aging behavior for selected MOSFET - technology nodes for mobile phone

Fig.2.7 depicts BTI aging behavior for the mobile phone end-of-lifetime use caseandin dependence of the stress voltage. For comparison reasons, stress voltages and Vth degradations are given with respect to the corresponding supply voltage given in [2]. Especially for voltages much higher than nominal supply, the effect of the non-constant field scaling transistor design from 130nm CMOS down to 32nm appears in an increased voltage sensitivity: for each technology step, degradation values increase and the slopes of the curves are getting more steep. In the region of nominal supply, process optimization dominates and limits absolute drift values to certain margins. Nevertheless, the 32nm node bases on a high-κ, metal gate process and besides the classic NBTI in pMOS, an additional PBTI in the nMOS device occurs. In fact, in the allowed supply region, single NBTI and PBTI degradations for the 32nm process are smaller than the 65nm NBTI. But from the circuit point of view, NBTI and PBTI drifts have to be summed up aspMOS and nMOS devices are typically stacked and both contribute to the proper circuit operation.

3

Negative Bias Temperature Instability (NBTI) Model

3.1 Negative Bias Temperature Instability (NBTI) Effect

The aggressive scaling down of the MOSFETs results in an increase of the internal electric field both in the channel and the gate oxide. Moreover, in order to reduce the gate leakage and enhance the carrier mobility, high-K dielectrics, strain engineering and high mobility channel materials are applied. However, they are accompanied with inevitable high concentration of defects within the materials as well as at the interface [1.2-1.9]. It has been reported that, when the gate of p-MOSFET is negatively biased (Fig. 3.1), the NBTI effect is caused by positive charged oxide traps and interface states. This increases the delay time of the circuit critical path with increased operation time, which reduces the circuit speed and lifetime. In long term operation conditions, p-MOSFETs suffer from continuous stress and recovery cycle, and 20% delay increase during 5-10 years ' operation is expected [1.10]. In order to avoid the impact of degradation to logic functions, the design tolerance may increase to 30% under the worst case. However, the increased design tolerance inevitably results in higher complexity and area of the circuit design. Therefore, analysing the NBTI sensitive partof the circuit and developing accurate predictive model is the key for approach cost

saving and optimisation design.

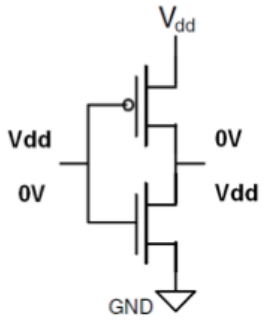

Figure 3.1: Bias conditions during circuit operation of a CMOS inverter - With input is 0V, output is high and the p-MOS device (top) is under uniform negative gate bias, which causes NBTI degradation.

During circuit operations, carriers have great opportunity to be captured by such defects or generate new traps under high electric field. The charged traps are quite possible to degrade the threshold voltage, subthreshold slope, current, and transconductance. The degradation of current characteristics induced by the NBTI effect is shown in Fig. 3.2 [11]. After 10000s stress, the threshold voltage, On-state current and transconductance exhibit evidentdegradation. The above degradation deteriorates the lifetime and speed of the circuit and system [1.12], and even leads to logic failure.

3.2 Overview of Existing NBTI Model

At present, numerous NBTI predictive models based on different concepts have been developed, including the hydrogen reaction-diffusion theory, hole-trapping theory and the energy transfer based theory. However, none of them are able to balance both the consistency of the theory as well as the practical application. An efficient NBTI model must be able to accurately predict the following features: 1) Long term degradation under DC stress conditions. 2) AC degradation with various frequencies and duty cycle. 3) The recovery characteristic in short term and long term regions. 4) Temperature dependence. In the following part, the

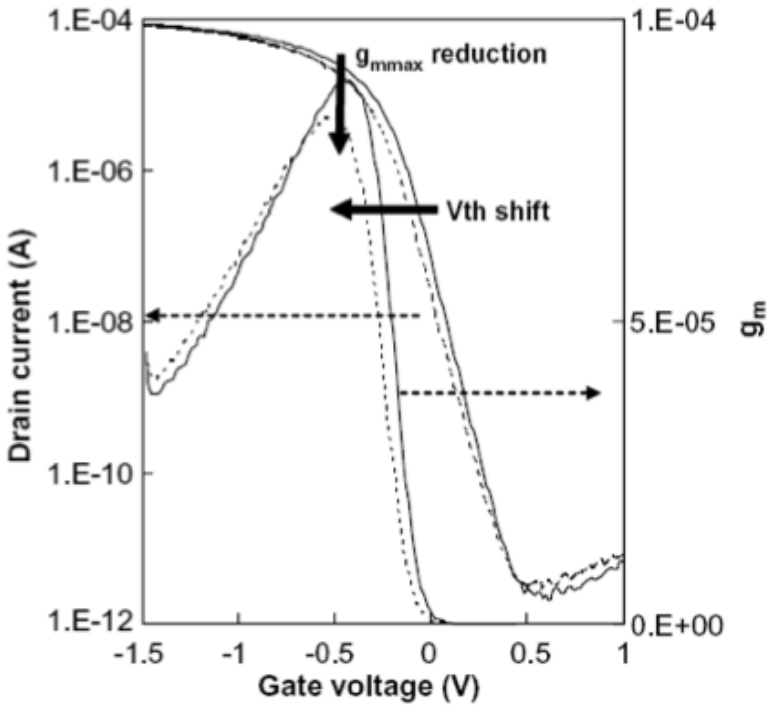

Figure 3.2: The degradation of Id-Vg and gm-Vg curves of p-MOSFET - before and after 10000s NBTI stress. The gate oxide thickness is 2nm,and temperature is 125 ° C. Solid and dashed lines indicate the characteristic before and after stress, respectively.

significant published NBTI predictive models, such as the reaction-diffusion (RD) model, the hole-trapping model, the interface-state generation model and energy transfer hole-trapping model, are simply reviewed from principle, verification, advantage and drawback.

3.2.1 Classical Reaction-Diffusion Model

Principle of the reaction-diffusion (RD) model is simply described as follows: when a negative bias is applied to the gate of p-MOSFET, high density holes are injected into the gate oxide from the substrate. Holes with high energy possibly react with the Si-H bonds located at the Si/SiO2 interface, generating a Si dangling bonds and hydrogen atoms. When the Si dangling bonds are occupied by holes, such positively charged states will act as interface-states and results in the threshold voltage shift (deltaV_{th}). At the same time, H atoms released from the Si-H bonds diffuse towards gate electrode [2.1]. The diffusion concentration determines the reaction rate of the Si-H bonds. The schematic view of Si-H bond reaction and hydrogen diffusion is shown in Fig. 3.3. The generation of interface state is determined by both Si-H bond reaction rate.

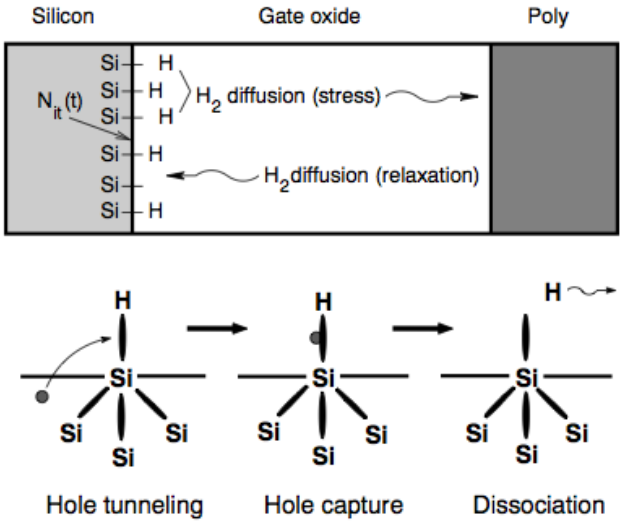

Figure 3.3: Schematic view of the RD model under stress and recovery conditions -

Eq. (3.1) describes the process of interface generation [2.1]. Here kF and kR are forward and reverse reaction rate respectively, N0 is the initial trap density at the interface, NH is the hydrogen concentration, and Nit is the interface-state density. Eq. (3.2) indicates the diffusion process, where DH is the hydrogen atom diffusion constant.

$$\frac{dN_{it}}{dt} = k_F(N_0 - N_{it}) - k_R N_H N_{it} \tag{3.1}$$

$$\frac{dN_H}{dt} = -D_H \frac{d^2 N_H}{dx^2} \tag{3.2}$$

During the initial period of the reaction process, the generated interface-state density is much lower than the total density of Si-H bonds. Therefore, $dN_{it}0$, and $N_0¿¿N_{it}$. Eq. (3.1) is simplified as

$$\frac{k_F N_0}{k_R N_{it}} = N_H \tag{3.3}$$

According to the diffusion equation (3.2), the hydrogen diffusion front x_D is solved as

$$x_D = \sqrt{(}D_H t) \tag{3.4}$$

As mentioned in Fig. 2.2. hydrogen atoms diffused into the gate oxide is supposed forming a triangle distribution. Thus the generated interface-state density is concentration is calculated by integrating the hydrogen within the gate oxide.

$$N_{it} = \frac{1}{2} N_{it0} x_D = \frac{1}{2} N_H x_D = \frac{1}{2} \frac{k_F N_0}{k_r N_{it}} \sqrt{(}D_H t) \tag{3.5}$$

The final expression of the interface-state density is

$$N_{it} = (\frac{1}{2} \frac{k_F N_0}{k_r})^{(1/2)} (D_H t)^{(1/4)} \tag{3.6}$$

The traditional RD model was validated by comparing with the measurement result, as shown in Fig. 3.4. The Vth shifts following a power-law relationship with the stress time, and the time exponent is about 0.25 0.3, which is consistent with the model result [23, 24].

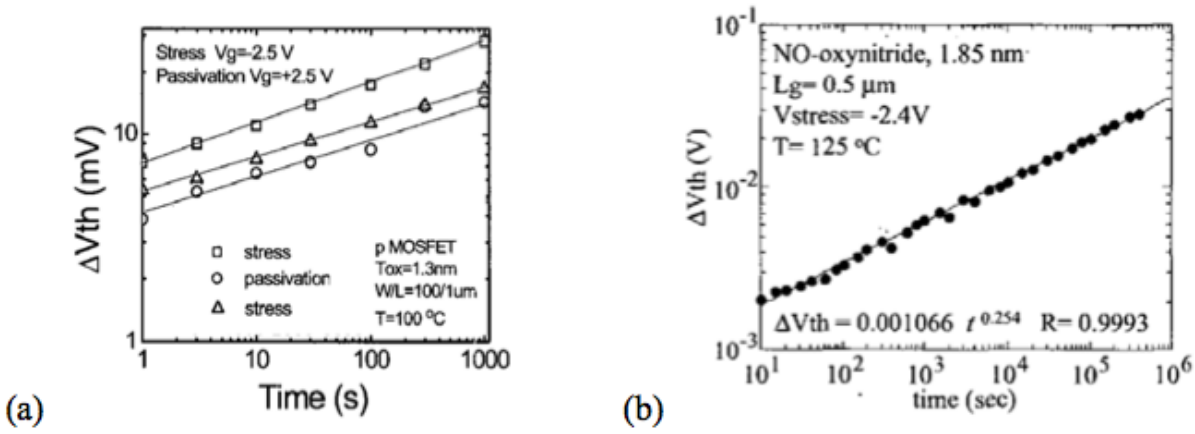

Figure 3.4: Typical time dependence of NBTI - The log-log Vth shift versus stress time shows 0.25 time exponent. Data is from (a) [23] and (b) [24]

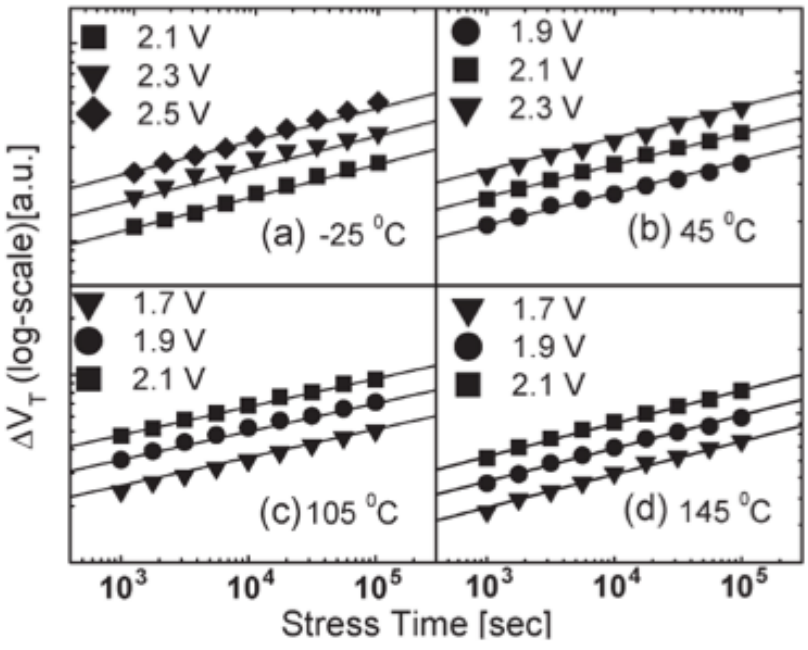

Figure 3.5: Fitting delVth (measured by ultra-fast On-The-Fly technology -

The time exponent of 1/4 is obtained based on numerous hypotheses, for example, slow reaction in the initial period, infinite gate oxide thickness and hydrogen atom diffusion process. However, soon after the proposed classical RD model, many measurement results obtained using advantage technologies showed that the time exponent featured 1/6 [25, 26], as shown in Fig. 3-5 [27].

Such phenomenon indicated that H atom diffusion is not the only element responsible for the NBTI degradation. In order to make a correct explanation to such phenomenon, A. Alam et al improved the classical RD model and assumed that part of the hydrogen atoms are possible to transfer into H2 molecule during the diffusion procedure [28].

In Eq. (3.1), the H atom concentration is supposed as NH. If the diffusion of H2 is considered, the transfer between H2 molecule and H atom is described as

$$N_H^{(0)} \propto \sqrt{(N_{H_2}^{(0)})} \tag{3.7}$$

The diffusion process of H2 molecule is

$$\frac{dN_{H_2}}{dt} = D_{H_2}\frac{d^2N_{H_2}}{dy^2} \tag{3.8}$$

Similar to the classical RD model, the H2 molecule diffusing in the gate oxide still follows the triangle distribution. Note that one H2 molecule results in two Si dangling bonds, the interface state density (NIT) is written as

$$N_{IT} = 2\frac{1}{2}N_{H_2}^{(0)}\sqrt{(D_H t)} = N_{H_2}^{(0)}\sqrt{(D_H t)} \tag{3.9}$$

Substituting Eq. (3.3) into Eq. (3.7) and Eq. (3.9), the interface-state associated to the H2 diffusion is derived as

$$N_{IT} \propto [\frac{k_F N_0}{k_R}]^{\frac{2}{3}}(D_{H_2}t)^{\frac{1}{6}} \tag{3.10}$$

The relationship between Vth shift and stress time is described using power-law equation in the RD model. The time exponent is insensitive to neither electric field nor temperature, but only determined by the diffusion series. If the diffusion series is H atom, the timeexponent is 1/4. Otherwise, the time exponent is 1/6

3.2.2 Improved RD Model

As mentioned in Section 3.2, the development of the RD model is based on numerous assumptions, such as slow generation of the interface state in the initial stage, infinite gate oxide thickness, and so on. Therefore, the classical RD model is insufficient in describing the NBTI effect in nanoscale MOSFETs with ultra thin gate oxide and special device structure. New mechanisms are needed to be considered and added to the RD model [29]. The schematic view of the silicon nanowire is shown in Fig3.5. The nanowire diameter is 10nm, gate oxide thickness is 3.5nm with a TiN metal gate, gate length of the device is 427nm, and Vth is about 0.22V [10].

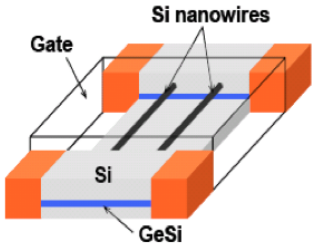

Figure 3.6: The 3-D schematic view of the Twin Silicon Nanowire MOSFET -

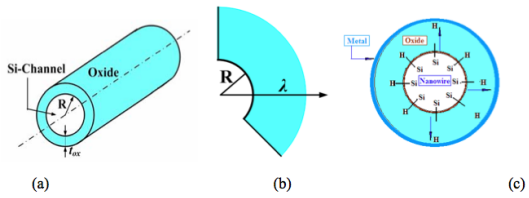

Figure 3.7: Cylindrical MOSFET with channel radius R -

In purpose of simplifying the theory derivation, the studied SNWFET is considered equivalent to a small scaled gate-surrounded MOSFET. Fig. 2.3.2(a) is a Cylindrical MOSFET with gate oxide surrounds the channel. R is channel radius and tox is the thickness of gate oxide. Fig. 2.3.2(b) shows a sketch view of Hydrogen diffuse from the Si-oxide interface along the radius of the nanowire,

and the diffusion constant is λ. Hydrogen atoms are supposed diffusing along the radius to the gate dielectric, as shown in Fig. 2.7(c).
Based on the classical RD model from Eq. (3.1)-(3.4), hydrogen diffusion distance $\lambda(t)=\sqrt{(}D_H t)$, the density of H atom at the interface due to the diffusion expressed in cylindrical coordinates [2.11] is

$$N_{it}^0(t) = \frac{1}{2\pi RL}\int_R^{R+\lambda(t)} N_H(1-\frac{r-R}{\sqrt{(}D_H t)})2\pi L dr \tag{3.11}$$

Combining the integral result in Eq. (3.11) with (3.7) and supposing $\lambda(t)=\sqrt{(}D_H t)$ concentration of H atom generated during stress process is

$$N_{it}^0(t) = \sqrt{\frac{k_f N_0 P}{R k_r}}(\frac{R\lambda(t)}{2}+\frac{\lambda(t)^2}{6})^{\frac{1}{2}} \tag{3.12}$$

Different from the assumption of the infinite oxide thickness, the H atoms diffusing into the gate oxide tends to saturate in the ultra thin gate oxide. The saturation rate Rsat is expressed as eqn 3-12. Here τ is the H atom capture time constant in the gate oxide. A good agreement is obtained by comparing the modeling result with the measured data under stress bias of Vgs=-2.4V and -2.2V, as shown in Fig. 3-8.

The recovery model is derived as an inverse process of the stress period. The V_{th} during the recovery process is written as the difference between the maximum V_{th} shift (V_{th}_max) and the recoverable V_{th} (V_{th} R).

Here ts is the stress time period, and τ r is the time constant for H atoms released from the oxide traps. If the recovery model is developed based on the classical RD theory, the Δ Vth during the recovery process is derived as 15] Fig. 3.9 compares the experimental data with both R-D model and newly developed model. It is obviously that, the improved model has evidently improved the quality and accuracy in matching with experimental data, especially in the recovery process. Such phenomenon indicates that the classical RD model is not sufficient for describing the NBTI degradation in nanoscale device. The limitation of the structure and hydrogen diffusion saturation effect should be considered in the predictive model.

$$\Delta V_{th}(t) = \frac{qN_{it\_max}}{C_{ox}} \cdot R_{sat} = \frac{qt_{ox}}{\varepsilon_{ox}\varepsilon_0}\sqrt{\frac{k_f N_0}{Rk_r} C_{ox}(V_{gs} - V_{th})}\left(\frac{R\lambda(t_1)}{2} + \frac{\lambda(t_1)^2}{6}\right)^{\frac{1}{2}} \cdot (1 - e^{-\frac{t}{\tau}})$$

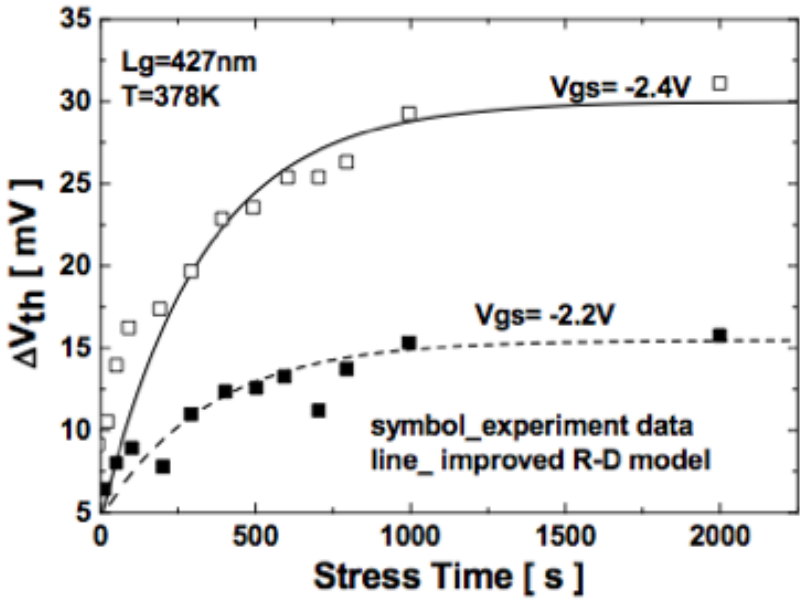

Figure 3.8: Comparison between modeling result and the measured data under stress bias of Vgs=-2.4V and -2.2V -

$$\Delta V_{th}^{R}(t) = \frac{qN_{it}^{0}(t)}{C_{ox}} = \frac{q}{C_{ox}}(N_{it}^{str} - N_{it}^{rec})$$

$$= \frac{qN_{it}^{str}}{C_{ox}}(1 - \frac{N_{it}^{rec}}{N_{it}^{str}}) = \frac{qN_{it}^{str}}{C_{ox}}\left[1 - \frac{\frac{R\sqrt{\xi D(t-t_1)}}{2} + \frac{\xi D(t-t_1)}{6}}{\frac{R\sqrt{Dt}}{2} + \frac{Dt}{6}}\right]$$

$$\Delta V_{th}^{R}(t) = \Delta V_{th\_max} - \Delta V_{th}^{R}$$

$$= \Delta V_{th\_max} - \frac{qt_{ox}}{\varepsilon_{ox}\varepsilon_0}\sqrt{\frac{k_f N_0}{Rk_r}C_{ox}(V_{gs} - V_{th})}\left(\frac{Rt_{ox}}{2} + \frac{t_{ox}^{2}}{6}\right)^{\frac{1}{2}} \cdot e^{\frac{t-t_1}{\tau_r}}$$

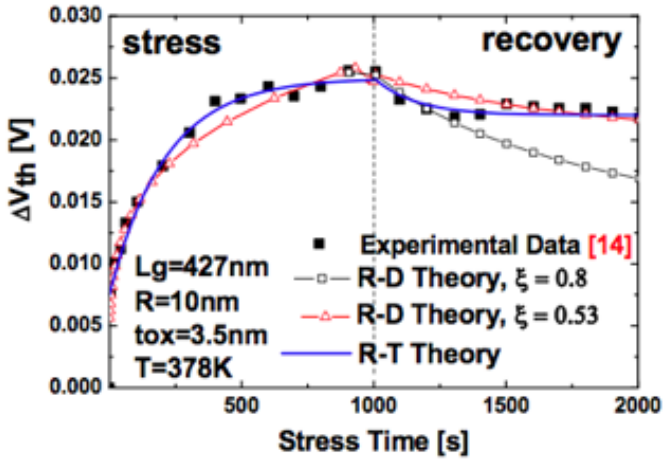

Figure 3.9:]
Comparison of the experiment data (solid symbol) with both Standard RD model (open symbol) and improved RD model (line)[38] -

3.3 NBTI Model with Temperature Variation

RD model assumes that NBTI degradation is temperature dependent, but does not give any physical basis for such dependency [21]. Similarly, the origin of temperature increment in scaled PMOS transistors and its impact on NBTI degradations have not been explored in the model. In this subsection, we describe our previous work related to the origin of temperature increment in scaled PMOS transistors and accommodate its impact in RD model sub-processes [15].
In order to meet the 30% delay reduction in each successive technology generation, the hole speed in PMOS inversion layer has to increase. The fast moving holes come closer to ≡ Si-H bonds at Si-SiO2 interface. Approximately, 0.2- 0.3eV energy is consumed to bring a hole close to ≡ Si-H bond [14]. The interaction results in breaking of ≡ Si-H bond, producing an interface trap and H atom with 1.3eV energy release. Therefore, the net energy gain in a single interface trap production is 1.1eV [14]. The gain raises temperature to Tmax from a reference temperature Tref (25C). Some of the released energy is consumed by recovery of the broken ≡ Si- bonds. Therefore, temperature T(t) at any stress instant t can be modeled as [9]:

$$T(t) = [(1/2)(T_{max} + T_{ref})] + [(1/2)(T_{max} - T_{ref})sin(2\pi ft)] \tag{3.13}$$

where f is the thermal frequency. The impacts of temperature increments on rate coefficients e.g. DH, DH2 , kH, kH2 , kf and kr of RD model are described below. The diffusion sub-processes in oxide layer follow Fick ' s law, e.g., DH decreases linearly with decreasing H density from Si- SiO2 interface as shown in Fig 1(b) [3]. Temperature variation strongly affects the diffusion rates DH and DH2 . The effect is based on Arrhenius relation, which can be written as [3]:

$$D_H = D_{H_0} exp(-\frac{E_a}{kT}) \tag{3.14}$$

As an effect of temperature the life time of MOSFET is significantly hampered as shown in fig3.10.

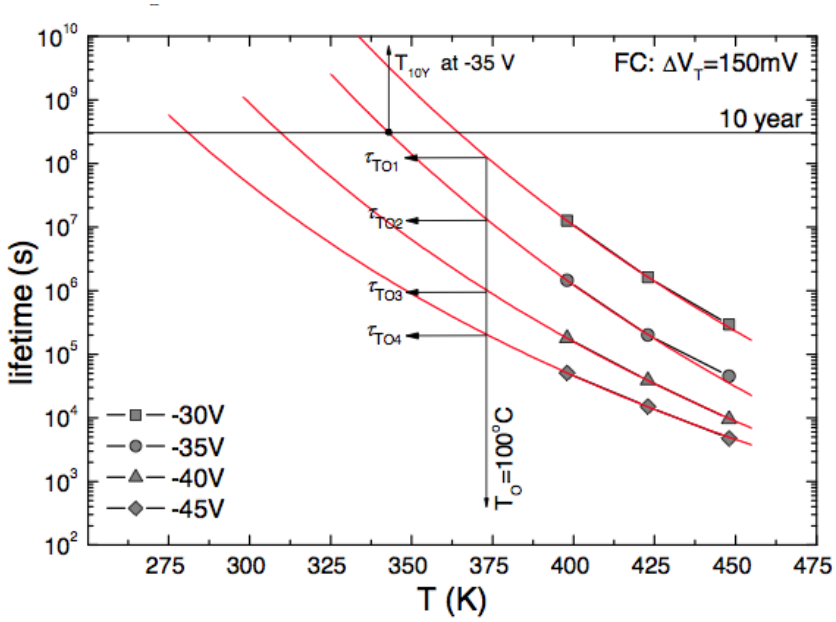

Figure 3.10: MOSFET lifetime decrement due to temperature increament -

4

MOSFET Degradation Due to NBTI

4.1 Threshold Voltage degradation

As shown in precious section the effect of previous section, NBTI is characterized by the threshold voltage increment of the PMOS transistor under negative gate stress. NBTI originates from Silicon Hydrogen bonds (Si-H) breaking that occur at Silicon-Silicon dioxide (Si-SiO2) interface as shown in Fig. 1(a). The broken Silicon bonds (Si-) act as interface traps at the Si-SiO2 interface and the H atoms/molecules diffuse toward the poly gate. The number of interface traps (NIT) depends on Si-H bond breaking rate (kf) and Si- bond recovery rate (kr).Schematic view of (a) Si-H bond breaking, H and H2 diffusions toward poly gate and their interconversion at Si/Si02 interface and inside oxide dielectric under negative gate stress (b) H and H2 diffusions toward the Si-SiO2 interface and Si- bond recovery under positive gate stress In recent times, exhaustive efforts has been put to understand NBTI [4,6,20]. Kackzer et al. in [20] have analyzed NBTI reasonably well but have not extended their analysis to deal with NBTI at a higher level. Alam et al. in [4] have modeled NBTI and presented the overall dynamics of NBTI as a reaction diffusion process. The model is usable at a higher level such as circuit level. Since in this work, NBTI analysis is done at the circuit level, model of [4] will be used that relates NIT with time (t) as follows [4]:

$$N_{it}(t) = (\frac{k_f N_0}{k_r})^{(2/3)}(\frac{k_H}{k_{H_2}})^{(1/3)}(6D_{H_2}t)^{1/6} \tag{4.1}$$

where No, kH, kH2, and DH2 represent initial bond density, H to H2 conversion rate, H2 to H conversion rate, and H2 diffusion rate inside SiO2 layer, respectively. Interface traps are assumed to be positive charges remaining at the Si-SiO2 interface that oppose the applied gate stress resulting in the threshold voltage increment . The relation between N_{it} and ΔV_{th} is

$$\Delta V_{th} = (1+m)qN_{IT}/C_{ox} \tag{4.2}$$

where m, q, and Cox are the holes mobility degradation that contribute to theΔV_{th} increment [5,23], electron charge, and oxide capacitance respectively. On the other hand, NBTI annealing takes place under the positive gate stress; in this case, the H atoms anneal back towards the Si-SiO2 interface .

Considering that is the stress time Vs threshold voltage graph is plotted, are shown in fig4-1

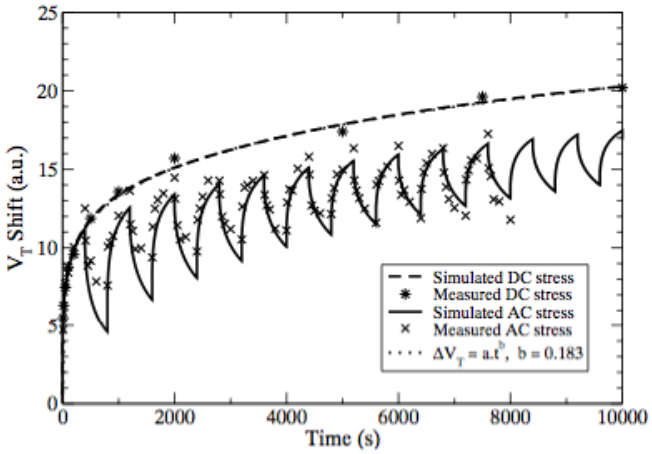

Figure 4.1: Threshold voltage shift due to NBTI considering RD model
-

However for simplification, only considering the shift in Vth over a longer time span the graph becomes similar to fig4-2

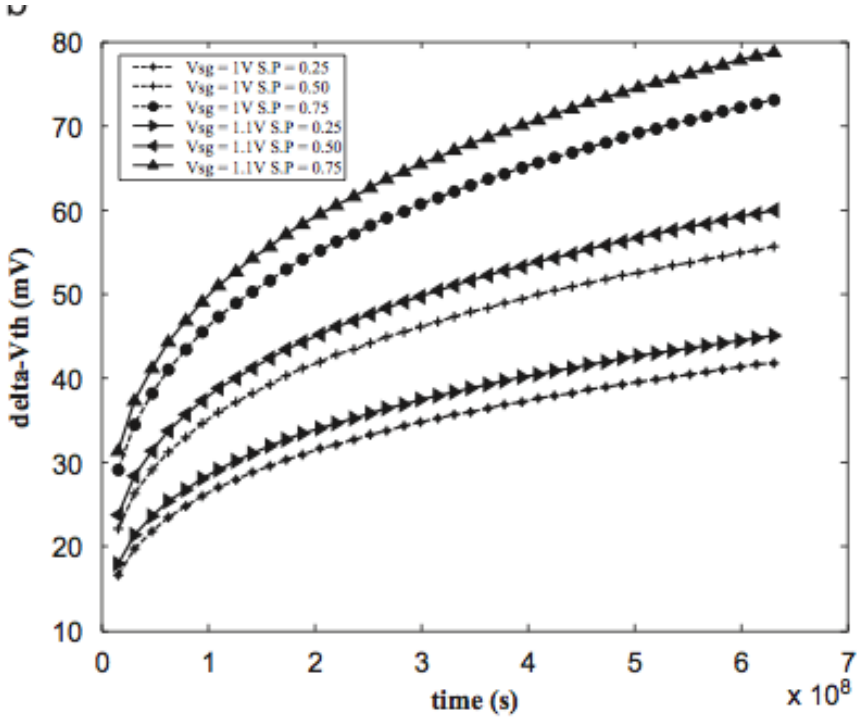

Figure 4.2: shifted threshold voltage of a 32 nm pMOS transistor versus timel -

4.2 Drain current decrement due to NBTI degradation

As it is shown in previous section NBTI degradation on a MOSFET device directly affects shift in threshold voltage Vth. As a result MOSFET parameters changes and the MOSFET operation gets affected severely. one of the biggest effect of Vth shift is drain current decrement. As shown in figure4-3

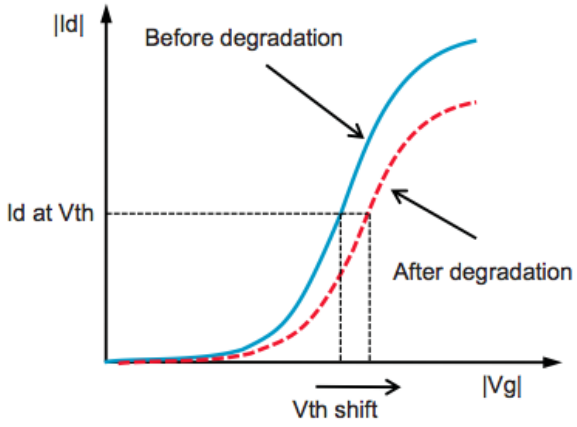

Figure 4.3: Shift in Id (drain current) due to shifted threshold voltage -

Typical transfer I-V characteristics of p-channel MOSFETs measured during the NBT stressing are shown in Fig. 4-4. It can be seen that, as the stressing progresses, the characteristics are being shifted along the VGS axis towards the higher voltage values, which is the consequence of stress-induced buildup of oxide-trapped charge. The shifts are more significant in the early phase of stressing and gradually become smaller with tendency to saturate in the advanced stress phase. At the same time, the slope of the curves slightly decreases, indicating that interface traps are being generated as well.

4.3 Transistor Delay Model

So far, we have analyzed temperature impact on NBTI induced threshold voltage increment and hole mobility degrada- tion. But, to analyze temperature impact

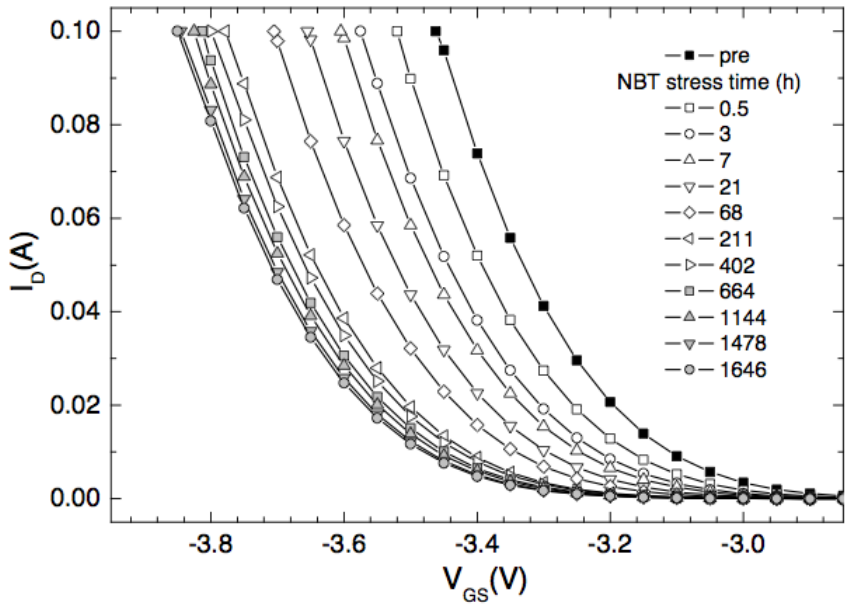

Figure 4.4: ID-VGS characteristics of p-channel MOSFETs during NBTI stressing -

at the circuit level, it is important to make a link e.g. between transistor parameters such as threshold voltage and mobility and transistor ' s delay. The NBTI induced Δ Vth and $\Delta\,\mu$ eff degradations, effect the delay of the PMOS transistor. Generally, the delay (td) dependence on threshold voltage and mobility degradation can be written as [11]:

$$t_d = \frac{C_L V_{ds}}{I_D} = \frac{\mu_{eff}\beta}{(V_g - V_{th})^{\alpha}}; \beta = \frac{LC_L V_{dd}}{WC_{ox}} \tag{4.3}$$

Vg and Vdd are gate and drain voltages of the transistor respectively, α is the velocity saturation index; CL, Ceff, and Weff are load capacitance, effective capacitance, and channel width respectively. In order to get the additional delay due to threshold voltage and mobility degradation, we expand the delay equation. After neglecting the higher order terms we get:

$$t_d(T(t)) = \frac{\alpha \Delta\mu_{eff} \Delta V_{th}}{(V_g - V_{th})} t_{d_o}; \tag{4.4}$$

where tdo is the transistor delay at Tref , and Δ td(T (t)) PMOS transistor delay that consider threshold voltage and mobility degradations under temperature variation.

4.4 NBTI Induced Delay

NBTI degradation significantly effects PMOS transistor delay. The delay results from threshold voltage increment and inversion layer mobility degradation. We divided our experiment into two steps. First, we performed the simulation by ignoring the mobility degradation and then by including its impact. The results are described below.

4.4.1 NBTI Induced Delay

We measured the PMOS transistor delay at time t = 0sec and after 105sec stress for each technology (e.g. 90nm, 65nm and 45nm) at 25C, 75C and 125C are shown in Fig. 4-5. The figure shows time and temperature dependencies of the delay degradation. From the figure we can observe two obvious trends:

- For a given PMOS technology and temperature the delay degradation increases with increase in stress time. For example, after $10 - 3$sec the degradation of 90nm PMOS transistor at 25oC is 0.0%. However, if the stress is maintained for 10+5 sec at 25o C, this reaches to 2.63%.

- For a given stress time and temperature the delay degra- dation is very significant for smaller PMOS transistors. For instance, after 105sec stress at 125C temperature, the degradation for 90nm PMOS is approximately 4.87%. However, under the same temperature, the delays for65nm and 45nm technologies are approximately 7.35% and 9.70%, respectively. Our analysis is consistent with Paul ' s analysis [11] and showed that percent of delay is approximately 4 times less than that of the threshold voltage shift. However, both results are optimistic because the impact of mobility degradation are neglected in these analyses.

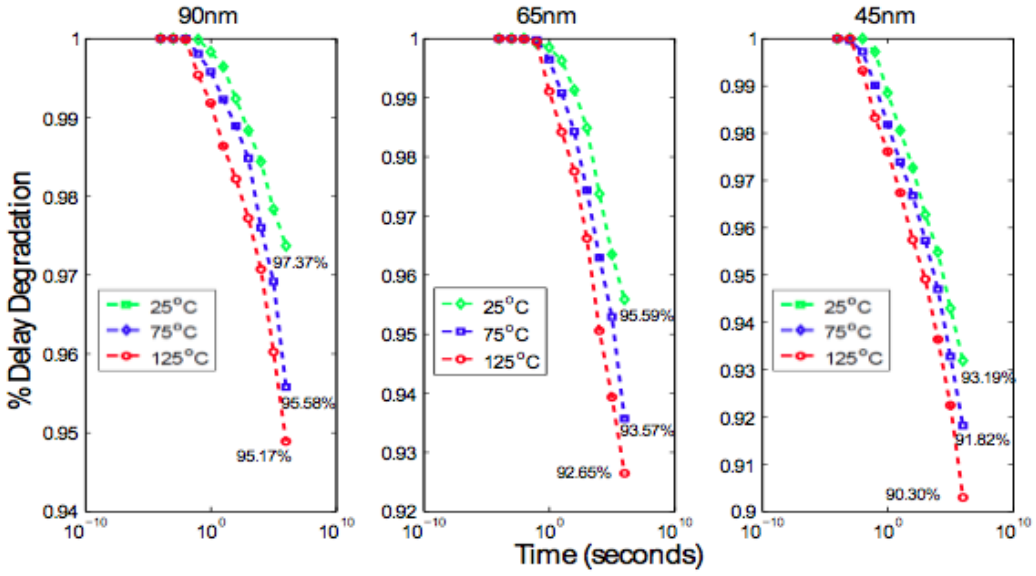

Figure 4.5: Percent delay degradation due to threshold voltage shift -

5

Effect of NBTI degradation on Analog circuit

5.1 Transition time increment of circuit due to NBTI

The gate output rise and fall transition times depend on the threshold voltages of the PMOS and NMOS transistors, respectively. Since NBTI affects PMOS transistor threshold voltage, only gate rise transition time has to be considered [8,23].
On the other hand, [24] that Trise is a function of the load capacitance (CL), PMOS and NMOS transistors aspect ratio (k) and PMOS transistor strength, i.e., drain saturation current (Idsat). These dependencies are combined to get Trise as:

A simple CMOS inverter was synthesized using 45nm Predictive Technology Model (PTM) transistor models [21] and simulated using HSPICE for 10 years operation. To focus on NBTI, we assume that other failure mechanisms, e.g. Hot Carrier Degradation, Electro migrations and Time Dependent Dielectric Breakdown are not affecting the inverter. Throughout the simulation, Fig. 5-1 (a) gives the threshold voltage increment of PMOS transistor due to NBTI. It shows that threshold voltage approaches 47.81mV after 10 years of operation. The curve follows the 1/6 trend and have a good match with the experimental results pre-

$$I_{dsat} = B(V_g - V_{th})^{\alpha}, \qquad B = \frac{\mu C_{ox} L_{eff}}{W_{eff}}$$

$$\Delta T_{rise} = C\frac{\Delta V_{th}}{(V_g - V_{th})^{\alpha}}, \qquad C = \frac{C_L k \alpha}{B}.$$

$$T_{rise} = \frac{C_L k}{B(V_g - V_{th})^{\alpha}}$$

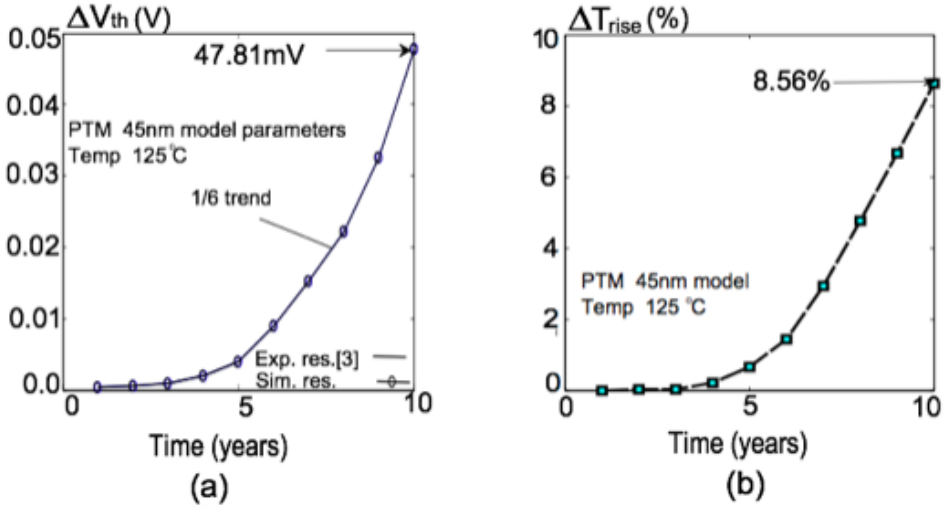

Figure 5.1: (a)NBTI induced V_{th} increment of PMOSFET as a function of time (b) inverter output δT_{rise} increment as a function of time -

sented in [3]. Fig. 5-1(b) shows increment of the inverter output that approaches 8.56% after 10 years operation. T rise increment trend due to NBTI for the other gates in the circuit. The T rise increment follows a similar trend as NBTI induced threshold voltage increment. Therefore,T rise can be used as a metric to monitor NBTI in nanoscale circuits.

5.2 Delay degradation due to Transition time increment of circuit

As the previous section describes the effect of NBTI as Transition time increment which directly added to Delay degradation of analog circuits. such as inverter of comparator circuits. As a result slew rate degrades and becomes a hazard to circuit operation. Which eventually cause the circuit to break down. As the figure5-2 below shows effect of delay degradation to a inverter due to NBTI threshold voltage degradation.

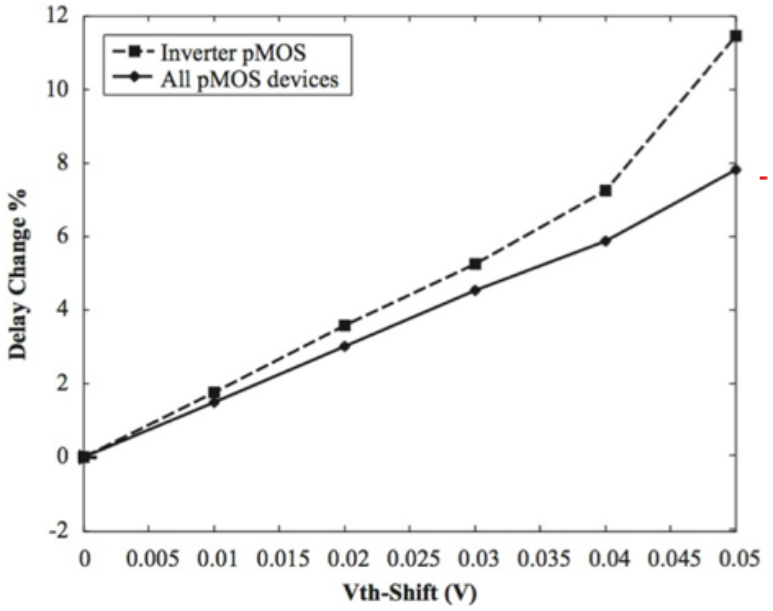

Figure 5.2: Delay degradation of Inverter circuit due to Vth shift caused by NBTI degradation -

As we can see from the figure for all inverter circuit 50mV of threshold voltage shift caused 12% delay change in an inverter circuit where as 7% in al pMOS devices. As a circuit operation the effect of slew rate degradation is shown in figure5-3.

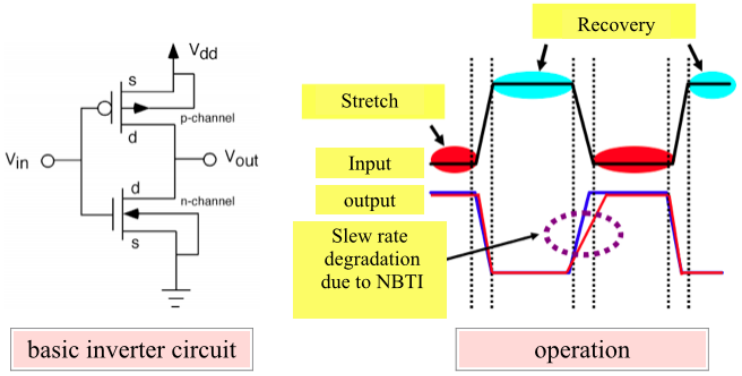

Figure 5.3: slew rate degradation of Inverter circuit (operational state)
-

5.3 slew rate degradation of comparator circuit

Comparator circuit is a widely used analog circuit consists of several pMOSFET that are easily be victimised by NBTI. As the previous section describes the effect of NBTI slew rate degradation on inverter circuit in this section we have simulated the operational consequences of comparator circuit with NBTI degradation. here in figure5-4 we have shown a general comparator circuit. The red circle shows the most affected or easy to be affected by NBTI pMOSFETs.

We have simulated the circuit operation using Cadance simulation software, as a model we have used 90nm TSMC MOSFET as a standard issue. the general simulation result are shown in figure 5-5.where the normal comparator circuit operation is shown. However if we look closely at the rising edge of the comparator output signal we can see the huge gap between fresh MOS and 10y old MOSFET slew rate degradation. with is 9.6% for a single comparator circuit. For a more complex circuit the result can be even sever.

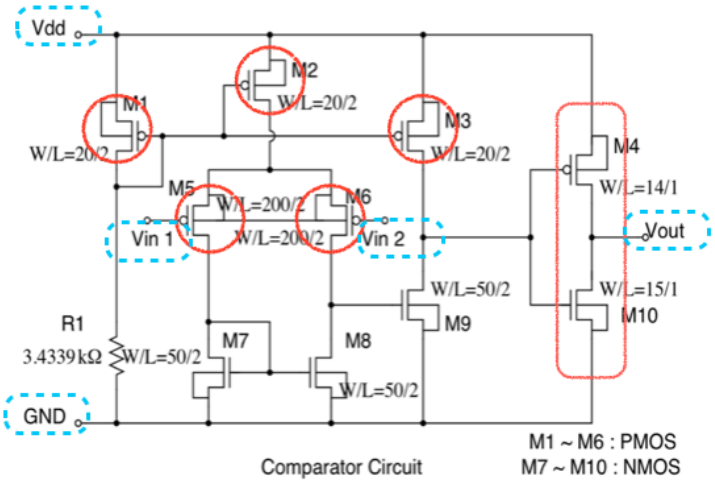

Figure 5.4: comparator circuit) -

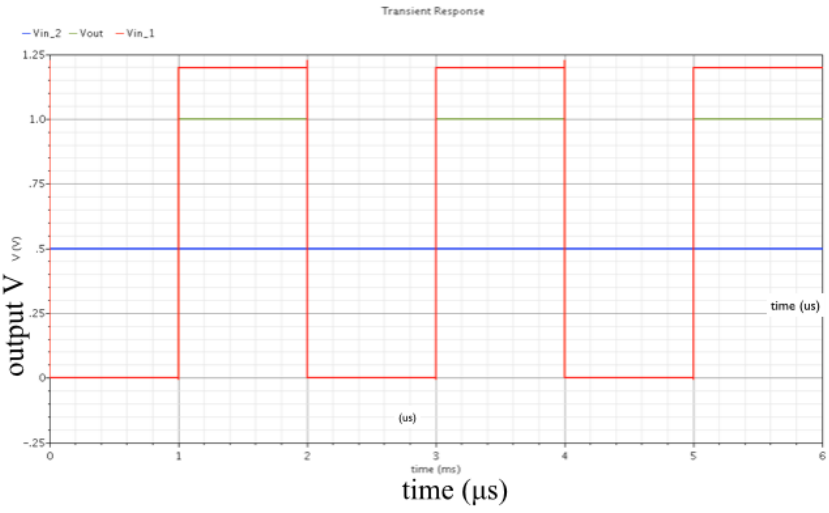

Figure 5.5: comparator circuit output simulation) -

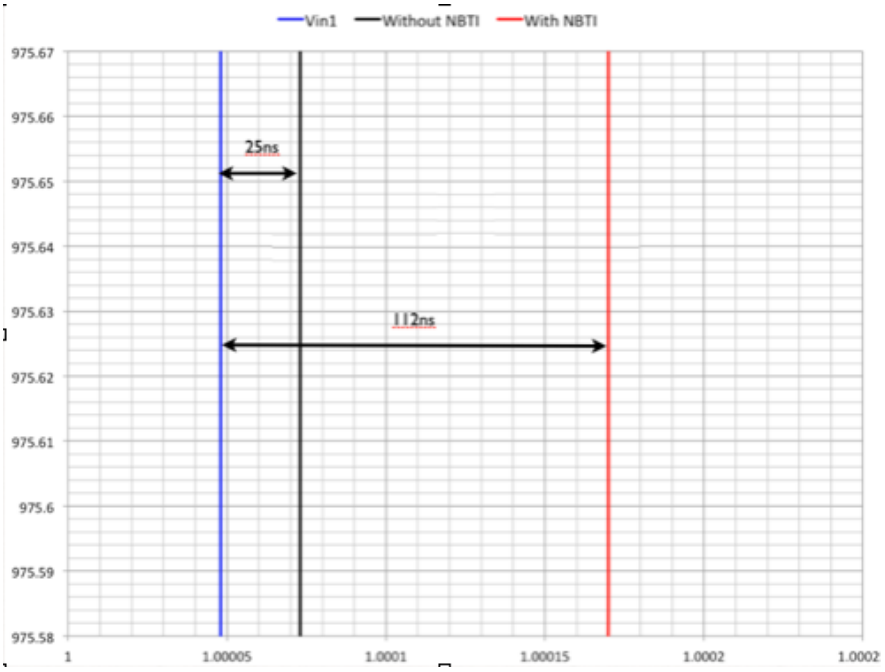

Figure 5.6: comparator circuit output simulation: NBTI degradation -

6

NBTI Monitoring Technique

6.1 NBTI detection method

This section presents the concept of NBTI monitoring using the gate output transition time as the metric and proposes a scheme for implementing the concept. Several techniques have been proposed in the literature to monitor NBTI in the circuits [14,16]. However, their results contain the overall degradations and do not isolate NBTI impact. The technique proposed in this paper focuses on the rise transition of a gate output that is effected only by NBTI in the PMOS transistors.

6.1.1 Conventional method and its limitations

A conventional way of measuring NBTI effect on circuits is to use ring oscillators [4-5]. Fig. 6-1 shows a conventional ring oscillator that is widely adopted for measuring NBTI- induced frequency degradation. During the stress mode, supply voltage is raised to stress voltage (Vstr) to accelerate the NBTI, and the input of the ring oscillator is connected to a fixed level, GND or Vstr. Regardless of the input selection, half of the PMOS and NMOS transistors in the ring oscillator are stressed. During the measure mode, supply voltage is pulled down to a nominal level, and the free-running frequency of the ring oscillator is measured. However, in high-k dielectrics and metal-gate technology, both NBTI and PBTI are prominent. Therefore, the measurement result from the conventional ring oscillator (Fig. 1) shows a mixed result of NBTI and PBTI. Therefore, the

conventional ring oscillator cannot be used for monitoring the NBTI and PBTI effects independently. Ketchen et al. proposed a ring oscillator based test structure for measuring NBTI in inverter- driven PMOS pass-gates [8]. By changing the gate voltage of PMOS pass-gates, the amount of threshold voltage degradation after stress is directly measured. The structure can also measure PBTI after minor modification. However, it requires a negative voltage to stress the pass-gates under test, and the negative bias needs to be well controlled for stressing the ring oscillator with high accuracy. In addition, the internal nodes are biased through off-current. The control of the drain and source bias voltage will be lost if the gate leakage fromthe stressed device becomes comparable to the leakage current in the keepers, generating unreliable measurement results. Kim et al. presented ring oscillator circuit structures to separate out the NBTI/PBTI effects [9-10]. Additional devices are added to cut the device under test from the rest of circuits and bias the rest circuits free of stress. The NBTI/PBTI isolation capability of the ring oscillators including the structure shown in Fig. 2 was successfully demonstrated in hardware. However, the measured results didn ' t address the equivalence between the proposed ring oscillator and the conventional structure. In this work, we explain the equivalence of the proposed ring oscillator structure to the conventional one through mathematical derivation and Hspice simulation. We also introduce an alternative ring oscillator structure for direct Vth degradation measurement. Due to the hight power consumption and ineffective on-chip function it is always consider a useless precautionary measurement. At due to the huge circuit area necessary for this kind of circuit it is consider to be a bulk in the circuit. Also it is costly to construct. Beside NBTI is veritable from chip to chip and varies due to operational condition. So instead of a fixed monitoring circuit we have proposed a new on chip monitoring system.

6.1.2 NBTI New Monitoring Concept

Fig. 6-2(a) shows the rising transition in output voltage (Vgout) of the last gate in a critical path. The figure shows that in the absence of NBTI (NoNBTI), Vgout starts the rising transition from 0V at time t0 and approaches Vdd at time t1.

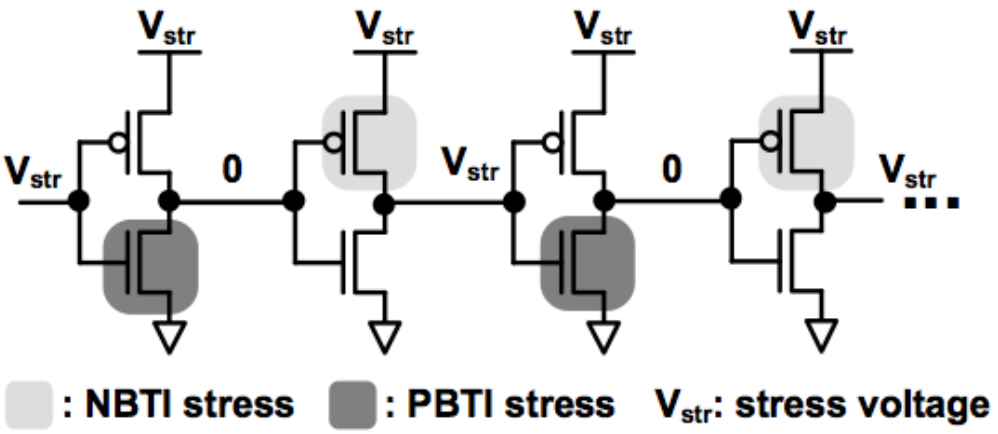

Figure 6.1: Conventional ring oscillator based NBTI monitor) -

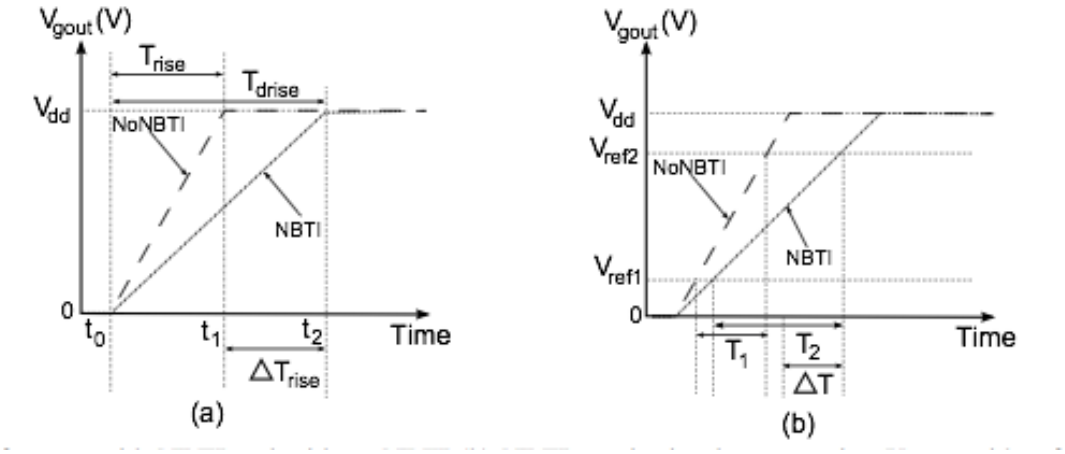

Figure 6.2: (a) Trise of a gate with NBTI and without NBTI (b) NBTI monitoring by comparing Vgout with reference voltages Vref1 and Vref2) -

Let's now consider two reference voltages Vref1 and Vref2 as shown in Fig. 6-2(b). In the absence of NBTI, Vgout will require a transition time T1 to proceed from Vref1 to Vref2. However, in the presence of NBTI, Vgout will require a transition time T2 to proceed from Vref1 to Vref2.

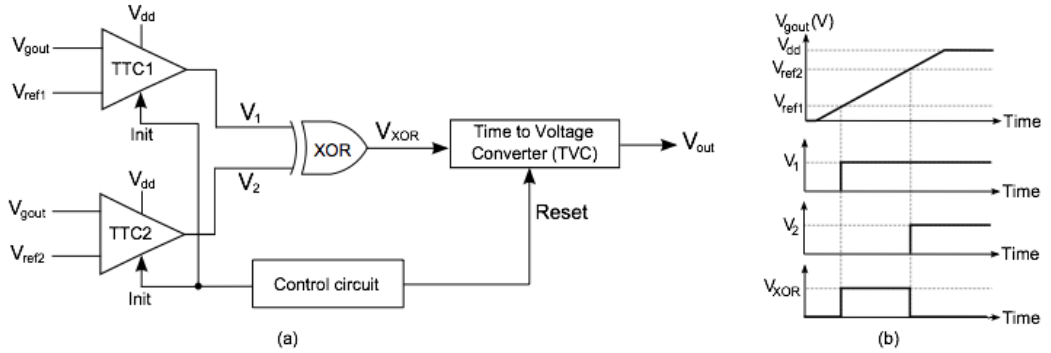

Figure 6.3: (a) (a) Block diagram of the proposed NBTI monitoring scheme that compares gate output with two reference voltages (b) Timing diagram of NBTI monitor) -

6.1.3 NBTI Monitoring Scheme

A block diagram of the scheme for implementing the concept proposed in the previous section is shown in Fig. 4(a). It consists of a Transition Time Comparator (TTC) pair (i.e. TTC1 and TTC2), a XOR gate, a Time-to-Voltage Converter (TVC) and a control circuit. The TTC pair compares the gate output transition (Vgout) with two reference voltages (i.e. Vref1 and Vref2). TTC1 compares Vgout with Vref1 =10% Vdd, and TTC2 compares Vgout with Vref2=90%Vdd. The output of TTC1 (V1) goes high when Vgout exceeds Vref1 as shown in Fig. 6-3(b). Similarly, the output of TTC2 (V2) goes high when Vgout crosses Vref2. For Vgout rise transition, V1 should go high earlier than V2. Both V1 and V2 are inputs to a XOR gate. The active high duration of the XOR output (VXOR) represents the interval between V1 and V2 low-to-high transitions as shown in Fig. 6-3(b). VXOR is fed to the Time-to-Voltage Converter (TVC) that converts its high duration into a voltage. The amplitude of the TVC output Vout is proportional to the transition time of Vgout of the gate. The entire operation of the

monitoring circuit is controlled by the control circuit. The control circuit sends a Reset signal to the TVC block before the comparison. It is important to reset TVC before the comparison, so that Vout is not affected by the previous results. It also initates and terminates the comparison by setting and resetting Init signal respectively.

In the rest of this section, the design structures and operating principles of the main blocks of Fig. 6-3 are described.

6.2 Transition Time Comparator (TTC)

The accuracy of the NBTI monitoring scheme depends on performance of the TTC pair. The schematic of a TTC that compares Vgout with Vref1=10%Vdd is shown in Fig. 6-4(a). The PMOS transistors M5 and M6 manifest the decision making latch for the comparison, while the NMOS transistors M1 and M2 are the decision controlling elements. The currents through M1 and M2 produce a differential current in the latch and switches it accordingly. The NMOS transistors M3 and M4 connect and isolate the latch from the controlling elements. The outputs of the latch (i.e., Node1 and Node2) are fed to the inputs of an RS latch that holds the decision till the next comparison. The comparison between Vgout and Vref1 is initiated andterminated by Init signal. The PMOS transistors M7 and M8 charge drain capacitances of M3 and M4 during low Init signal that speed-up the next comparison.
To initiate the comparison, Init signal gets high and connects the latch to the controlling elements. When Vref1 is larger than Vgout, the current flow through M1 (I1) surmounts the current through M2 (I2), causing M5 to turn on while M6 is turned off; this results in setting Node2 to high. However, when Vgout exceeds Vref1 during the rise transition, I2 becomes larger than I1. Now the drain-source voltage of M5 is large enough to switch M6 on. The temporary on states of both M5 and M6 causes metastability in the latch. However, due to the current regeneration in the latch, the Node1 voltage gets a stable high level and is fed to the RS latch that memorize the decision. The second TTC has been designed such that it produces high V2 when Vgout exceeds 90% of Vdd. Both V1 and V2

are fed into the XOR gate inputs. The interval between V1 and V2 low-to-high transitions is obtained from the active high duration of the XOR output.
The functionality of the TTC1, TTC2 and XOR gate is verified through timing simulations using HSPICE. The 45nm PTM transistor models [21] are used to synthesize the comparators and XOR gate. A Vgout with Trise of 0.7ns was applied to the TTC pair. The simulation results are shown in Fig. 5(b). In the absence of NBTI, Vgout takes T1=0.59ns to proceed from Vref1 to Vref2. Under this condition, the interval between low-to-high transitions of V1 and V2 is 0.74ns (the extra time is due to the internal delays of the comparators) as shown in the top part of Fig. 5(b). The XOR gate converts this interval to a active high logical value with a duration of 0.66ns (see the bottom part of Fig. 5(b)). On the other hand, in the presence of NBTI, the transition time of Vgout to proceed from Vref1 to Vref2 increases up to T2=0.64ns as shown in top part of Fig. 5(c), about 9% higher. The increment extends the interval between low-to-high transitions of V1 and V2 that approaches 0.92ns. Now the active high duration of XOR gate is 0.84ns as shown in the bottom part of Fig. 5(c), i.e., 27% more than the previous case.

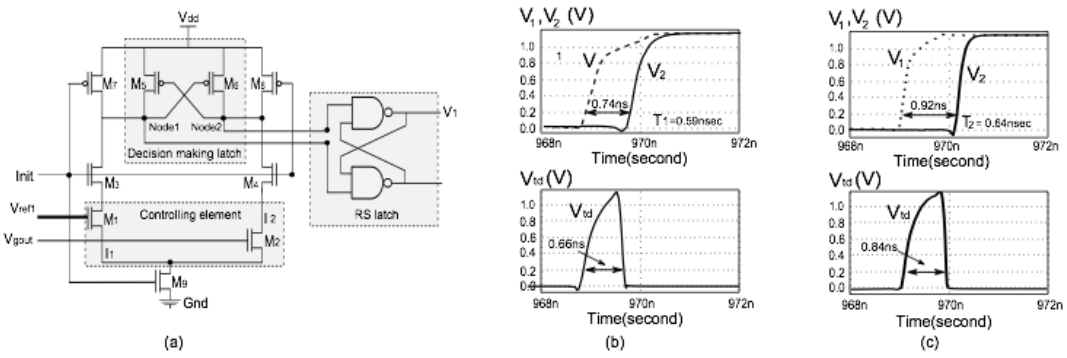

Figure 6.4: (a) Schematic of transition time comparator (b) Low-to-high transitions of TTC1 and TTC2; Active high duration of XOR without and (c) with NBTI) -

6.3 Time-to-Voltage Converter (TVC)

The active high duration of XOR gate (i.e VXOR in Fig. 4(a)) represent Trise/Tdrise of the gate. Time-to-Voltage Converter (TVC) converts this representation into a voltage. Fig. 6(a) shows an implementation of a simple charge pump based TVC that comprises two NMOS transistors N1 and N2, and a capacitor Cint. N1 acts a control switch that controls voltage build across Cint. N2 is used to discharge Cint before initiating NBTI measurement. Cint is main entity of the TVC that produces the TVC output voltage (i.e. Vout). Vout depends upon VXOR high duration, Cint capacitance and time constant of N1. W/L of N1 are adjusted to get smaller time constant and Cint is kept such that the voltage developed is substantial yet not so high to saturate to the Vdd.

Before asserting Init signal (see Fig. 6) to measure NBTI impact, VReset in the control circuit is set to high. The signal turns on the transistor N2 and discharge Cint to the ground. VReset is kept high for a longer duration to ensure full discharge of Cint. Once the capacitor is fully discharged, Init signal is set high and the output of the XOR gate (VXOR in Fig. 4) is applied to N1 that acts as a control switch. The high value of VXOR will allow charge pumping from Vdd that builds a voltage across Cint. The amplitude of the voltage across Cint depends on VXOR high duration.

The TVC is synthesized with 45nm NMOS transistor PTM models [21] with Cint=0.62pF. Fig. 6(b) shows that the amplitude of the TVC output (Vout) has almost a linear relationship with XOR output (VXOR) high duration width. The figure suggests that 24% increment in VXOR high duration causes 25% increment in the Vout voltage with a sensitivity of 0.50mV/psec.

At this point it can be observed that NBTI induced Trise increment of the gate is represented by the increment in voltage, i.e. TVC output voltage Vout. The Vout can be used directly or indirectly to initiate an NBTI tolerating scheme. In this paper, the VXOR is used to modify substrate (body) bias voltage of the PMOS transistors as will be discussed in the next section.

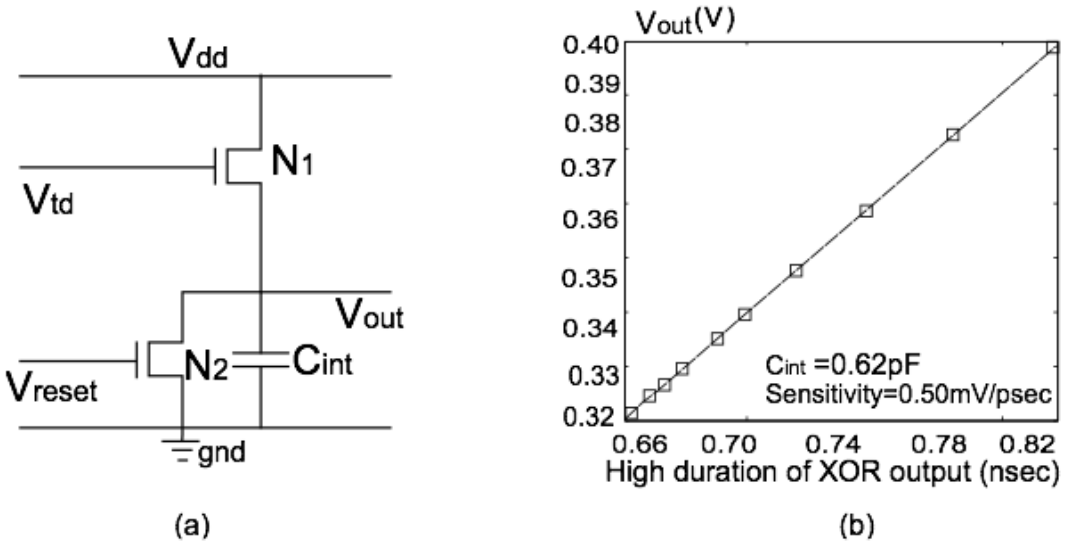

Figure 6.5: (a) Schematics of TVC, (b) Output characteristics of TVC

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6.4 Control Circuit)

Control circuit decides the initiation and termination of the monitoring. There are many ways of implementing the circuitry to initiate monitoring, but optimally the circuit should periodically reset the TVC and then initiate the comparison and monitoring. Due to space constraints, the complete design and operating principle of the control circuit is omitted from the paper and only its signals used for the monitoring are discussed.

6.5 Simulation result

simulation result using TSMC 90nm model is shown in fig6-6

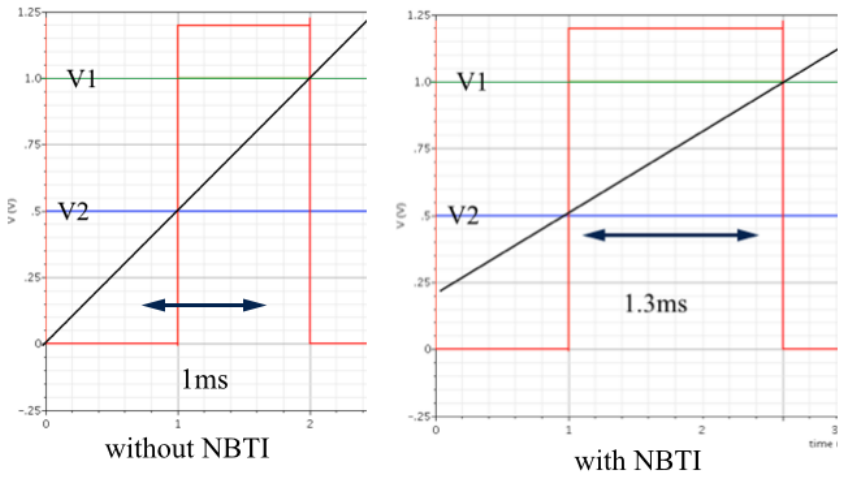

Figure 6.6: Simulation result of TTC circuit sung TSMC90nm process

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7

NBTI Mitigation Technique

This section proposes a technique to improve the reliability in the NBTI effected circuits. It starts by illustrating that dynamic body biasing is an effective technique for redressing NBTI induced Vth increment of PMOS transistors. Thereafter, it proposes a Self Adjusting Threshold Voltage (SATV) technique that applies body biasing to redress the NBTI impact.

7.1 Limitations Conventional NBTI mitigation method

Conventional method of NBTI mitigation is Guard banding and adaptive body biassing. Which is prediction the total amount of expected Vth degradation in advance depending on wafer behaviour. Which is mostly unreliable.Power savings for DVS follow the same trend. Figure 7 also shows the power reduction of DVS compared to guardbanding. Savings are significant during early lifetime, but limited afterward. Using the DVS strategy, we observed a total (10 year) lifetime energy savings of 7% with respect to guardbanding. Note that this is an optimistic upper bound on energy savings, since we do not add any implementation overhead for DVS hardware and control. Although we must pay the area and potentially the control overhead for the entire lifetime of the processor, we only receive significant power benefits during the early lifetime. These results show significantly less

benefits than several previous works suggested. Discrepancies in results are due to the previously discussed limitations in previous modeling approaches.

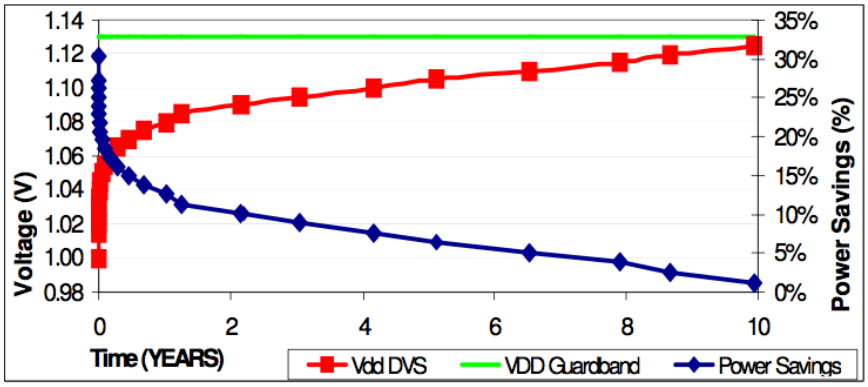

Figure 7.1: Significance in operation of DVS compared to Guardbanding) -

7.2 Proposed NBTI mitigation method : DVS (Dynamic Voltage Scalling)

Transistor can be body biased by applying a voltage between the source/drain and the substrate. The body bias affects Vth and therefore the speed and leakage current of the transistor. A negative body biasing increases Vth causing a slower and less leaky transistor. On the other hand, a positive body biasing decreases Vth resulting in faster and more leaky transistor [29]. Body bias can be applied in two difference ways: (a) all the transistors on a chip have the same bias voltage and (b) transistors are grouped in different groups and each particular group has the same bias voltage. Note that the second method ensures different but optimum Vth for all transistors on the chip. Body biasing is an effective industrial technique to mitigate process variations of transistors within the same die or in different dies across the wafer. After fabrication, transistors in same/different dies may have different Vth. Applying body bias voltage to the transistors shifts the Vth of the transistors to an acceptable margin [28]. Similarly, body biasing the PMOS transistors can be used to redress NBTI induced Vth increment. As

illustrated in section II, NBTI causes 47.81mV Vth increment to the PMOS transistors. For this reason, applying a positive bias to the PMOS is considered to redress the increment.
As NBTI in the PMOS transistors anneals during positive gate stress, it is desirable to have a dynamic bias voltage that redresses NBTI impact yet ensure minimum leakage currents in the circuit. Applying dynamic bias voltage is common in modern chips; e.g., Narendra et al. [27] proposed a dynamic biasing scheme that produced 24 different biasing voltages based on the results of monitoring circuits. Next, we propose a Self Adjusting Threshold Voltage (SATV) technique to adjust body bias voltage according to the output of the monitoring scheme.

7.2.1 Self Adjusting Threshold Voltage (SATV)

The main idea of SATV is to redress NBTI induced Vth increment. In presence of NBTI in the circuit, SATV lowers Vth by body biasing. However, in absence of NBTI, SATV applies no body biasing to the circuit. Fig 7(a) shows the proposed SATV scheme for a circuit consisting of an inverter that represents a gate in the circuit. The inverter output is monitored by the NBTI monitoring scheme proposed in the previous section. The monitoring circuit senses NBTI in the gate in terms of Vout increment. In absence of NBTI, Vout=0.32V and it increases with NBTI as shown in Fig. 6. The Vout is applied to SATV that produces the modified body bias voltage (Vbb) when Vout¿0.32V. Fig. 7(b) shows that the modified Vbb has a linear relationship with Vout. The modified Vbb is applied to the substrate of the PMOS transistor that decreases its Vth.
The inverter shown in Fig. 7(a) was synthesized using 45nm transistor models [21] and simulated for an operation time of 10 years. NBTI monitoring circuit measures the NBTI impact and SATV produces the corresponding body bias voltage. To show effectiveness of the method, the NBTI indicator (i.e. rise transition time) Tdrise is measured under two conditions: (a) no body bias was applied to the PMOS transistor, and (b) body bias was applied to PMOS transistor. Fig 7(c) shows Trise increment due to NBTI under these two cases. The figure shows that when no body bias was applied, NBTI causes 8.16% increment to the rise

transition time. However, when body biasing was applied, the increment in Trise reduces to only 6.20%. Therefore, it can be deduced that the proposed technique reduces the NBTI impact by 31%.

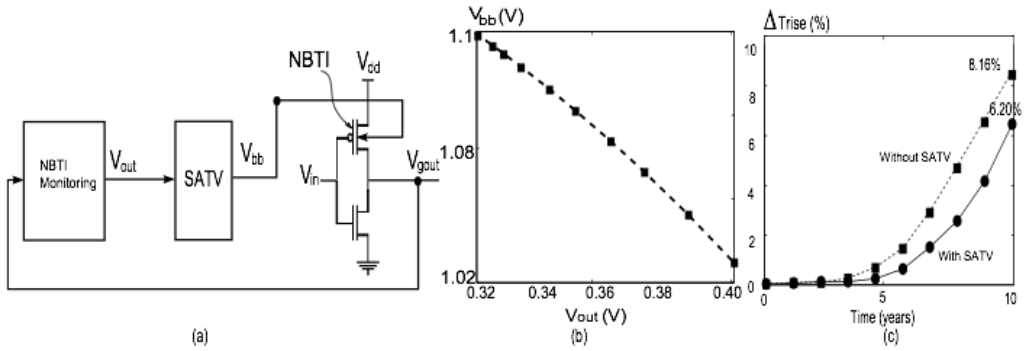

Figure 7.2: (a) Schematic of the self adadjusting threshold voltage scheme (b) The modified Vbb due to the TVC output (Vout) variation (c) Trise increment due to NBTI with and with our SATV) -

7.3 Circuit diagram and Simulation of SATV

figure 7-4 shows the block diagram of SATV circuit while figure 7-5 shows the circuit diagram. Using both circuit we have simulated the operation of DVS system which is shown in figure 7-6. Where bulk voltage for both NMOSFET and PMOSFET is shown against the calculation result. Simulation result is quite similar to the approximate value.

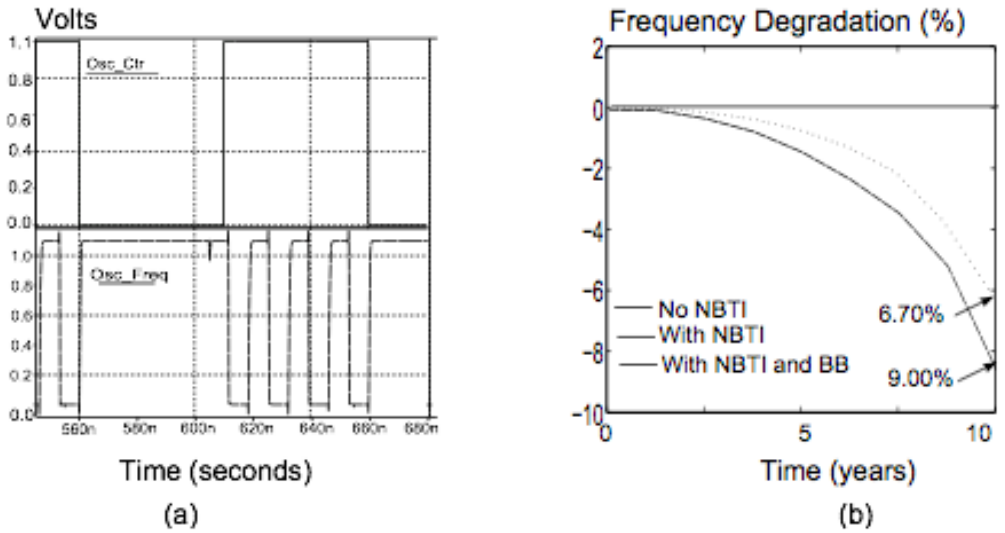

Figure 7.3: (a) Samples of Osc Ctr and Osc Freq waveforms (b) Frequency degradation due to NBTI with and without body biasing) -

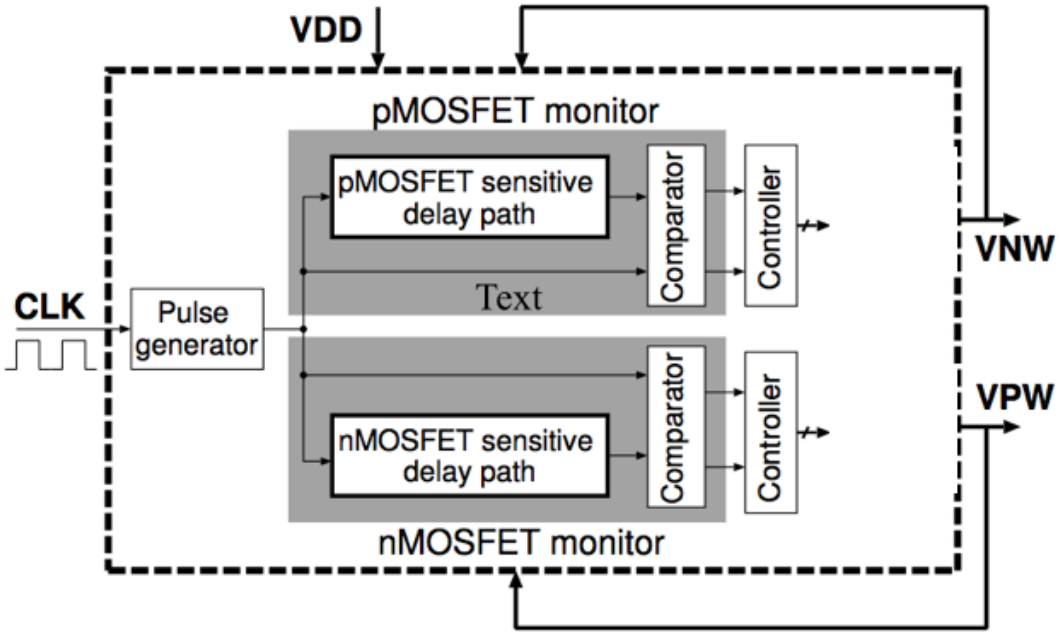

Figure 7.4: Block diagram of SATV (DVS) system) -

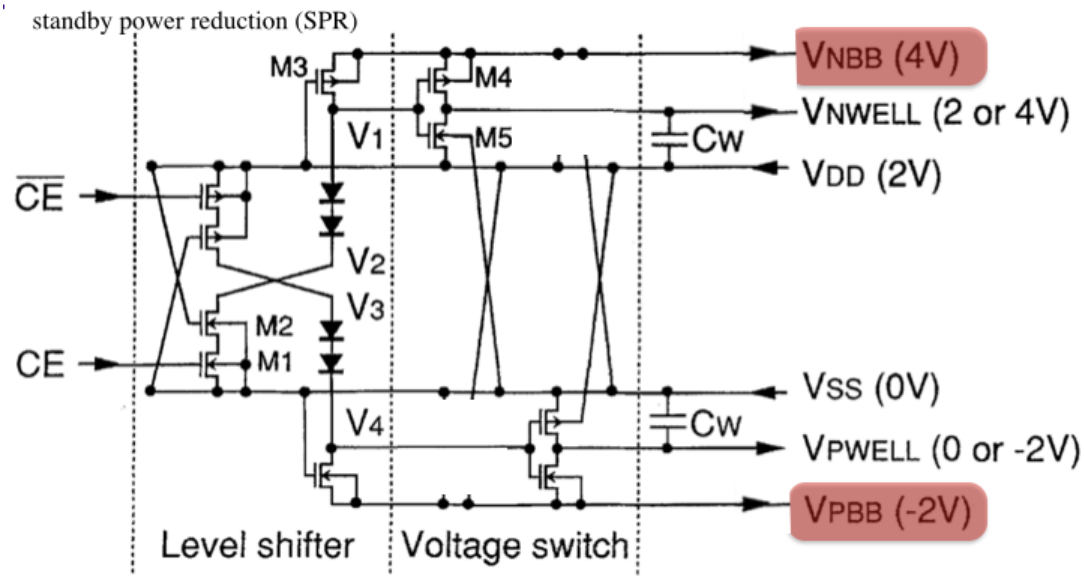

Figure 7.5: Circuit diagram of SATV (DVS) system) -

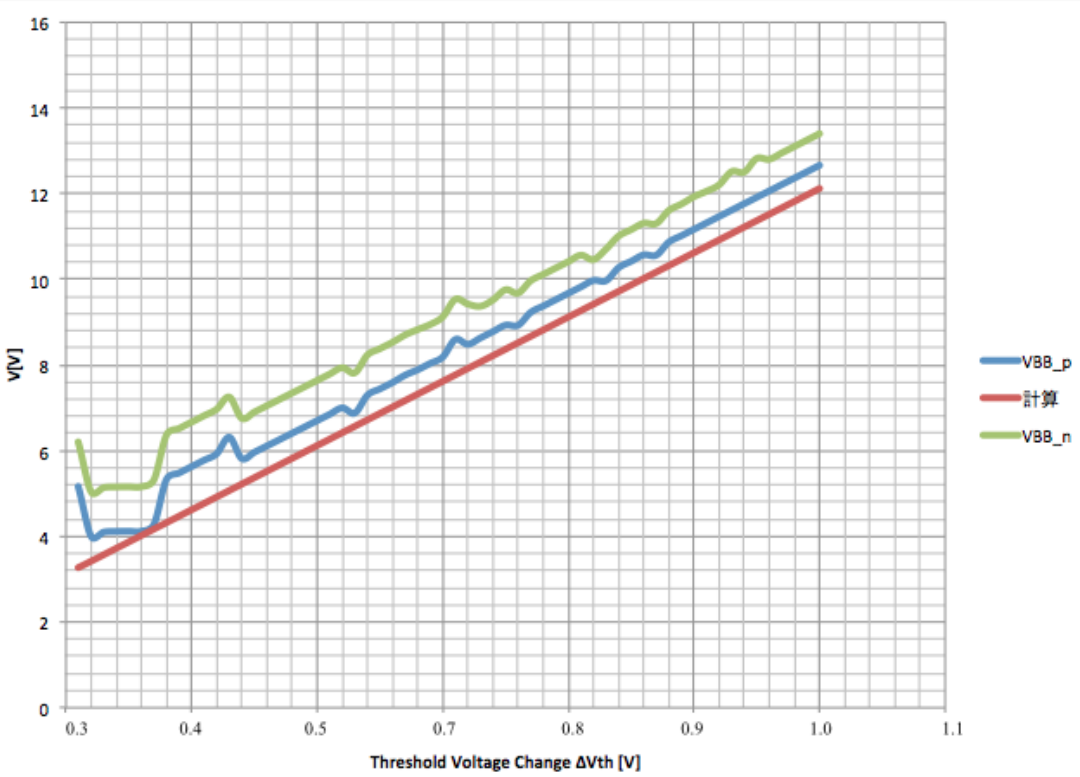

Figure 7.6: simulation result of SATV (DVS) system) -

8

Discussion

This paper has presented a scheme to monitor NBTI impact in nanoscale circuits and proposed a design technique for the circuit reliability improvement. Firstly, the impact of NBTI on gate output transition time is modeled. The analysis of the model showed that NBTI causes up to 8.56% increment in the gate output transition time. Secondly, a technique to monitor the NBTI impact is proposed; the technique is based on the measurement of the gate output transition time delay. The proposed technique converts the transition time increment into a voltage with a sensitivity of 0.50mV/ps. Thirdly, an NBTI mitigating technique that applies a dynamic biasing voltage to redress NBTI in the circuit is proposed. The technique ensures 34% reduction in NBTI impact on the circuit in 10 years operational life. Finally, it has been shown that the leakage current overhead of the proposed technique does not exceed 4.09% for an operational life of 10 years.

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Declaration

I herewith declare that I have produced this paper without the prohibited assistance of third parties and without making use of aids other than those specified; notions taken over directly or indirectly from other sources have been identified as such. This paper has not previously been presented in identical or similar form to any other Japanese or foreign examination board.

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