Flexible hybrid integration of photonic and electronic chips using aerosol-jet printing

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Traditionally, photonic chips are electrically interfaced using wire bonding technology, which is still considered the most flexible and cost-effective method. However, there are some drawbacks for the wire bonding technology which need to be considered such as the electrical parasitics of the wires and the difficulty to control the wire dimensions. On the other hand, flip-chip and through-silicon via are good alternatives in particular for high frequency operation, but are much less flexible than wire bonding. Hence, there is a need for interconnecting chips with a higher degree of freedom, comparable to traditional wire bond technologies, but at the same time providing high frequency capabilities. Therefore, in this paper we present a 3D flexible face-up packaging technology using aerosol-jet printing which enables hybrid integration of high-speed photonic and electronic chips at 50 Gbps and beyond. The aerosol-jet printing technology allows depositing features directly on planar and non-planar surfaces, with micrometer resolution, and can deposit an extremely wide range of materials, including metals and dielectrics, enabling co-planar transmission lines from "pad-to-pad" with the freedom to tune the characteristic impedance. In this work, we demonstrate the technology by printing high-frequency silver electrical interconnects (pad-to-pad distance ≈ 200 µm) between 4-channel driver and two 1x2 single-mode vertical cavity surface emitting laser (VCSEL) arrays. The technology was electrically and optically proven at 50 Gbps to interconnect the driver chip and the VCSELs. In addition, the printed silver interconnects showed a low sheet resistance of 0.03 Ω/square. Furthermore, a standard 85°C/85 RH test was performed to investigate the reliability of the printed interconnects and no failure or degradation was observed over 700 hours.

Introduction

The conventional packaging technologies for electro-photonic integration such as wire bonding techniques are reaching their limits. New packaging techniques which can be flexible, reliable and effective at higher frequencies are essential. Some reports were presented to replace the wire-bonding technology with a 3D stacking method [1] by placing the optoelectronic chips (vertical cavity surface emitting laser (VCSEL) or photodiode (PD)) on top of the electronic chips (driver or TIA). A 12-channel Optical transmitter and receiver subassembly was recently demonstrated at 10 Gbps based on wet etched silicon interposer [2]. In this work, we developed a process based on aerosol-jet printing (AJP) which flexibly integrates photonic and electronic chips at 50 Gbps and beyond. The aerosol-jet printing technology has already been reported to enable 3D printed electronics such as resistors, capacitors, antennas, sensors and thin-film transistors [3]. The technology is mainly based on creating an aerosol from a functional liquid ink by means of atomization, then transporting the aerosol to the

deposition head and finally focusing the aerosol stream on the substrate by a nitrogen gas flow (sheath flow) as shown in Fig. 1 (a) (source: Optomec). The aerosol-jet process uses aerodynamic focusing to precisely deposit functional inks in a direct way as defined in a CAD model. The inks can consist of metals or dielectric materials. The ink is placed into an atomizer, which creates a dense aerosol of droplets between 1-5 microns diameter. Drops larger than ca. 5 microns cannot overcome the force of gravity and drop back into the ink and are recycled. Then, the aerosol is transported by a gas flow to the deposition head. Within the deposition head, the aerosol is focused by the sheath gas which surrounds the aerosol as an annular ring. The resulting high-velocity converging particle stream is deposited onto the substrate creating the very fine features.

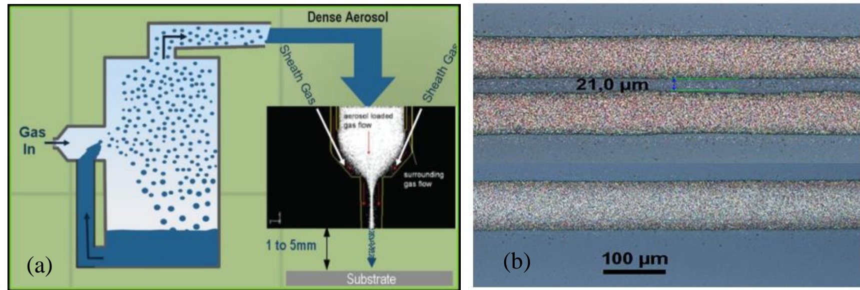

Fig. 1 (a) the aerosol-jet process (source: Optomec) (b) an example for the aerosol-jet printed traces on glass substrate.

Experimental process flow

As a material for the electrical interconnects, we used a silver nanoflakes ink from Novacentrix (Metalon HPS-030 AE1) which is originally developed for aerosol-jet printing. The parameters of the aerosol-jet process were optimized in order to obtain uniform traces as shown in Fig 3(b). These parameters include carrier gas flow, exhaust flow, sheath flow, substrate temperature, the working distance and the printing speed. After printing, the samples of the printed traces were sintered in the convection oven at 210 °C for 2 hours as recommended by the ink supplier. The complete process flow is shown in Fig. 2. It can be summarized in 3 main steps; creating a mechanical polymer support by covering the gap between the photonic and electronic chips, making opening to the contact pads, and aerosol-jet printing of interconnects between the chips. First, the chips were die-bonded to the PCB followed by an epoxy polymer dispensing (Epotek OG 142-112). The epoxy was locally dispensed on the chip by a fine needle. Next, a flat PDMS stamp (residing on glass substrate) was gently pressed onto the dispensed epoxy. Then, the epoxy was cured using an UV lamp at 30 mW/cm^2 for 2 minutes. The stamp can be released after UV exposure since the epoxy does not adhere to PDMS. The thickness of the epoxy layer on top of the chips is less than 10 µm. Hence vias can be easily opened on the contact pads by excimer laser ablation. At last the electrical interconnects were precisely printed between the chips (pad-to-pad) using aerosol-jet printing.

Interconnection between daisy-chain test chips

The functionality of the technology was proven first on test chips (daisy chain). The interconnection between the two daisy-chain chips was successfully printed and tested. The resulting printed interconnects have a width of about 50 µm and thickness of 5 µm per pass. The total length of the aerosol-jet printed tracks for the complete daisy-chain was about 7.5 mm and 30 vias were opened. The printed tracks has a resistance of

around 6 Ω/mm. Pictures of the top view for the connection between the test chips and the cross-section view from pad-to-pad are shown in Fig. 3.

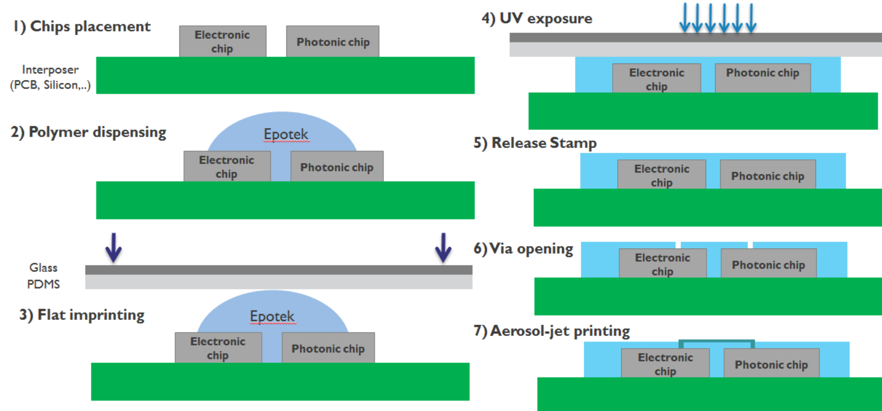

Figure 2: The fabrication process flow

Moreover, the printed interconnects showed no failure even after running 85°C/85 RH tests for 700 hours. The reliability test was performed for 4 different daisy-chain links and the complete daisy-chain resistance was measured every 100 hours as illustrated in Fig.4. Due to the fact that there is a polymer covering the chips, the sintering temperature for the sample was decreased from 210 °C to 150 °C to avoid any CTE mismatch that could occur if the temperature exceeded 150 °C. This means that the printed interconnects didn't reach the complete conductivity and hence the 85 °C temperature of the test gradually contributed to evaporate the remaining solvents and increasingly joins the silver flakes in the printed traces. Therefore, the resistance was decreasing during the first 500 hours of the reliability test as shown in the graph until it stabilizes more or less after 500 hours.

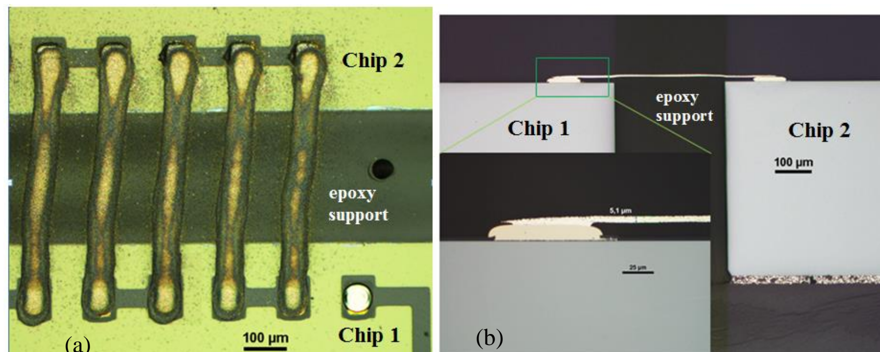

Figure 3: The aerosol-jet printed interconnects between the test chips (a) top view (b) cross-section view

Driver-VCSEL interconnection

The driver chip [4] has a thickness of 375 µm and the VCSEL is 75-µm thick. So, the VCSEL was mounted on a spacer with thickness of 300 µm in order to obtain the same height for all chips. The chips were glued to the PCB by non-conductive adhesive and decoupling capacitors were glued to the PCB by an electrical conductive adhesive. High-speed interconnects were printed from the driver to the VCSEL and also from the VCSELs anode to the decoupling capacitor as shown in Fig. 5 (a). The high-speed measurements proved the functionality of the assembly by demonstrating clear open eye-diagrams at 50 Gbps as illustrated in Fig. 5 (b).

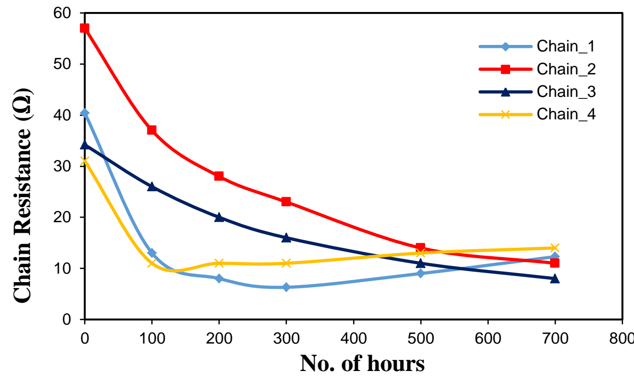

Figure 4: the effect of performing 85°C/85 RH reliability test for 700 hours on the daisy-chain resistance

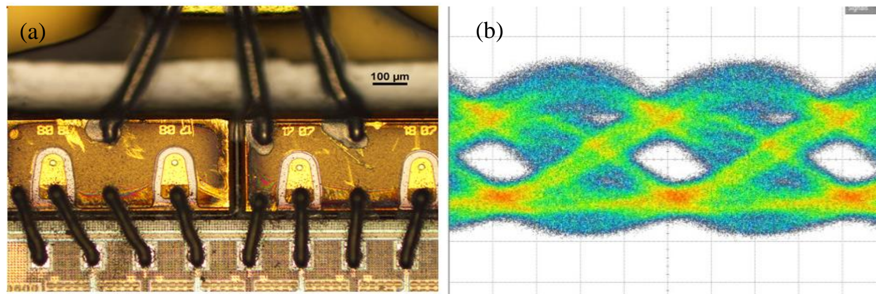

Figure 5: (a) The assembly of the 4-channel driver and two 1x2 single-mode TUM VCSELs using AJP
(b) Eye diagram at 50 Gbps per channel.

Conclusion

We have presented a flexible technology for electro-photonic integration using aerosol-jet printing. The technology was demonstrated at 50 Gbps by printing high-speed interconnects between a 4-channel driver and two 1x2 single-mode VCSELs. We are currently working towards optimizing the process with a vector network analyzer to tune the characteristic impedance of the printed interconnects while experimenting with low-loss dielectrics.

Acknowledgements

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