UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH
Escola Tècnica Superior d'Enginyeria
de Telecomunicació de Barcelona

CHARACTERIZATION OF 28 NM FDSOI MOS AND APPLICATION TO THE DESIGN OF A LOW-POWER 2.4 GHZ LNA

A Master's Thesis

Submitted to the Faculty of the

Escola Tècnica d'Enginyeria de Telecomunicació de Barcelona

Universitat Politècnica de Catalunya

by

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In partial fulfilment

of the requirements for the degree of

MASTER IN ELECTRONICS ENGINEERING

Advisor: Xavier Aragonés Cervera

Barcelona, May 2017

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Abstract

IoT is expected to connect billions of devices all over world in the next years, and in a near future, it is expected to use LR-WPAN in a wide variety of applications. Not all the devices will require of high performance but will require of low power hungry systems since most of them will be powered with a battery.

Conventional CMOS technologies cannot cover these needs even scaling it to very small regimes, which appear other problems. Hence, new technologies are emerging to cover the needs of this devices. One promising technology is the UTBB FDSOI, which achieves good performance with very good energy efficiency.

This project characterizes this technology to obtain a set of parameters of interest for analog/RF design. Finally, with the help of a low-power design methodology (gm/Id approach), a design of an ULP ULV LNA is performed to check the suitability of this technology for IoT.

Keywords

IoT, UTBB FDSOI, LNA, ULP, ULV, gm/Id, IC

Acknowledgements

I want to thank my supervisor, Xavier Aragonés, for all the help and given support during this thesis.

Revision history and approval record

Revision	Date	Purpose
0	19/05/2017	Document creation
1	22/05/2017	Document revision

Written by:		Reviewed and approved by:	
Date	23/05/2017	Date	23/05/2017
Name	Jaume del Rio Jimenez	Name	Xavier Aragonés Cervera
Position	Project Author	Position	Project Supervisor

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1. Introduction and objectives

An introduction on the IoT paradigm and a definition of the main objectives of the thesis as well as the thesis organization are commented in this chapter.

1.1. Motivation

The Internet of Things (IoT) has emerged in the recent years as the new paradigm that will revolutionize a wide range of sectors. Although some IoT applications are already present today, forecasts predict a fast grow in the near future, thus increasing exponentially the number of connected devices in the next years. According to [1, 2], companies are going to make an economic effort spending over $5 trillion on these technologies in the next five years, and an increase from the 6.6 million devices existing in 2016 to almost 22 billion in 2021. The estimation of the worldwide growth of the usage of these devices by category is shown in Figure 1.

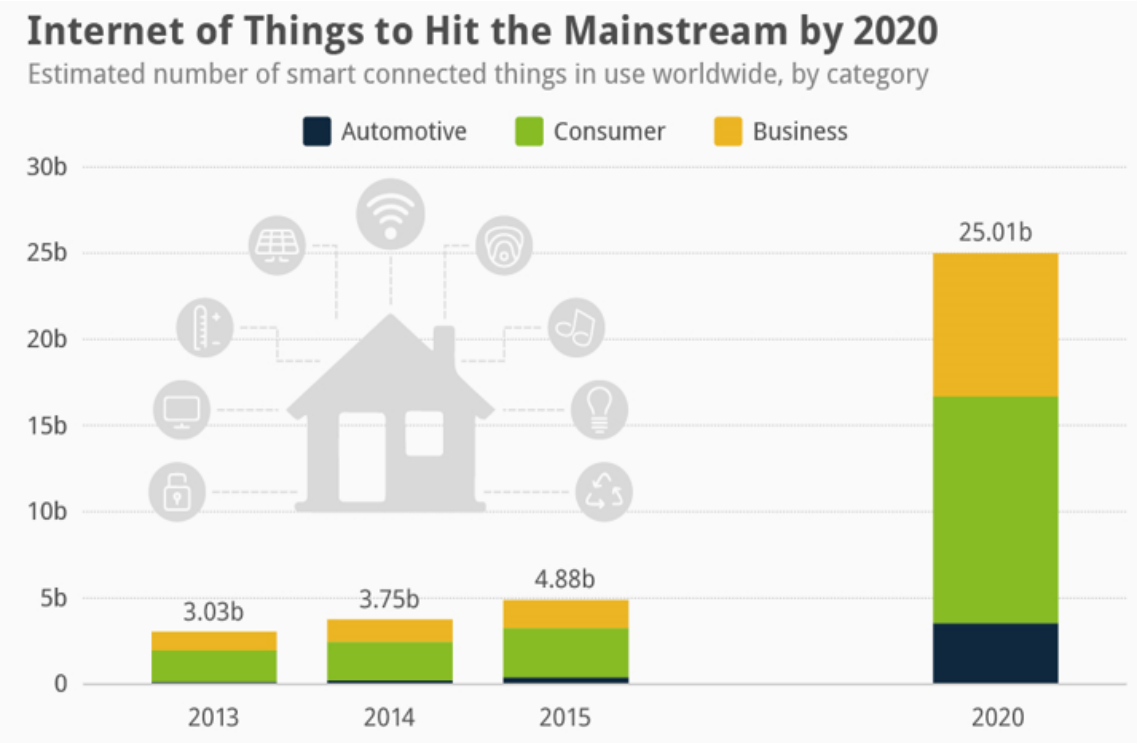

Figure 1 - Estimated number (in billions) of smart connected things in use worldwide, by category [2]

For this trend to be accomplished, a fundamental need is to make use of new technologies that enable connectivity between such a huge amounts of devices while keeping a low cost, small volume and reduced power consumption. Although bulk Complementary Metal-Oxide-Semiconductor (CMOS) technology is the predominant one for integrated circuits (IC) due to its high integration capability and affordable among other properties, a transition to other "unconventional" MOS-based technologies is being produced these years. The evolution towards down-scaled sizes of transistors gates has reached its limits with the conventional bulk CMOS, and a promising technology for overcoming its drawbacks is the Ultra-Thin Body and Buried-oxide Fully Depleted Silicon-On-Insulator (UTBB FDSOI) technology, developed by STMicroelectronics.

Small nodes suffer from small-geometry effects and the UTBB FDSOI technology minimizes many of them and comes with improvements providing a boost to speed

performance and power-efficiency compared with the regular bulk CMOS technology. Its flexibility to adapt to different operation modes such as high performance, low power or low leakage makes it the perfect replacement for current technologies. In addition, it offers many advantages for the low power Radio Frequency (RF) design [3, 4] becoming a well suited technology for IoT applications.

1.2. IoT – CMOS nanometer technology as enabler

The term “IoT” refers to the idea where the capability of computing and the access to network connectivity is extended to objects which are not normally considered computers but can have the ability to communicate between each other without or with minimal human interaction. A “thing”, on IoT context, could be literally anything such as any type of sensor implanted on a human body or a car, or any human created object with the ability to generate, exchange and consume data over a network without human intervention [5].

IoT technologies allow each one of these devices to work as an “intelligent node” in the network, acting smartly and making collaborative decisions in order to benefit certain applications. These nodes collect information and also can process/adapt low level signals received by them, so they can retransmit these signals creating a communication network between nodes. The nodes should establish a secured communication link with a centralized “cloud” in order to protect, process and store the data and then be able to offer this data to users/applications who require it.

Nowadays, some market applications based on the IoT concept can be found in [6], but in a quite near future, it is expected that Low Rate Wireless Personal Area Networks (LR-WPAN) will be used in a wide different embedded applications, including smart home systems automations, industrial sensing and control, environmental monitoring and sensing, which will connect thousands of millions of devices and services anytime and anywhere. A small picture of an overview example of an IoT environment can be found in Figure 2.

Within the wide variety of devices inside the IoT concept not all of them need complex operating systems compared with smartphones or computers. Most of them are only deployed to one specific purpose such as physical magnitude sensing in a remote area, which turns out in basic needs of coverage or minimum power consumption. Based on this principle, IoT applications can be divided into two main categories, Critical and Massive IoT deployments [7].

Critical IoT deployments require more complex systems with different properties depending on its usage, such as high reliability, low latency, low delay or a high date rate. On the other hand, Massive IoT deployments, referred as massive since billions of theses sensors will be deployed globally, typically don’t need high complexity with less power-hungry systems extending the battery life, specifications of data rate or latency much more relaxed and being very cost effective devices. New machine communication standards for massive Low Power Wide Area (LPWA) devices were released recently, allowing for example the launch of the ICT industry’s first complete cellular LPWA offering of Ericsson in 2016 in collaboration with AT&T [8].

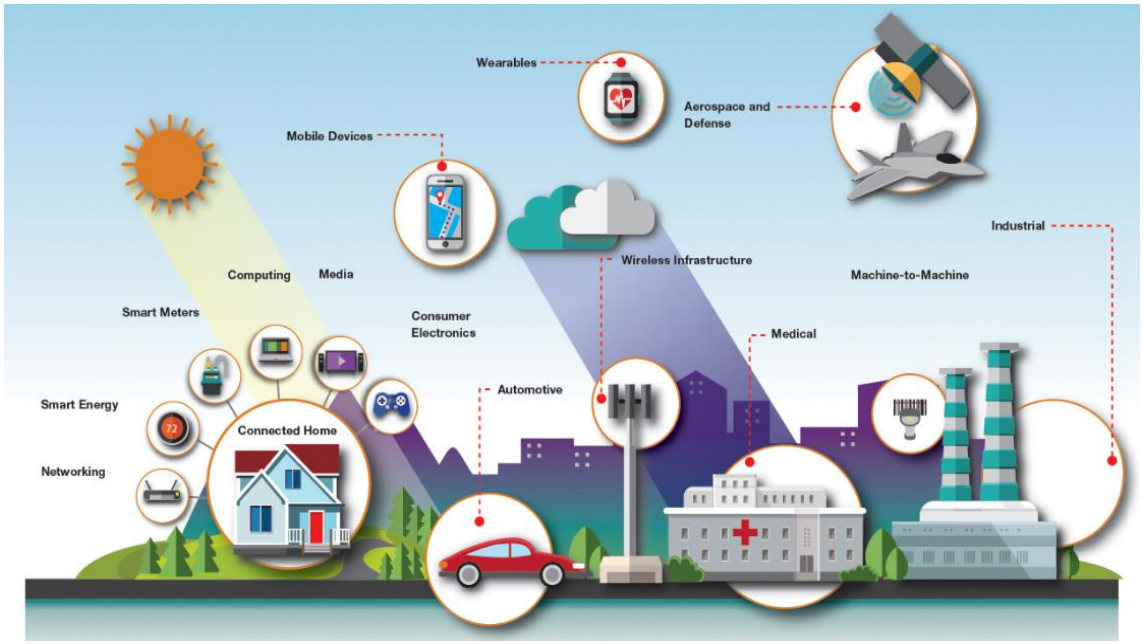

Figure 2 - Overview example of an IoT environment [9]

There's a coexistence of a multitude of wireless standards because of the different requirements of the environment or the big variety of use cases. On one side, the sensors networks work over relatively short distances (i.e. tens of meters) with low data rates and with a low power consumption protocols (i.e. ZigBee, Bluetooth, RFID…), which has driven a significant interest in investigation of low power wireless technologies. On the contrary, the connection between these networks and other systems has the need to cover long distances with high throughput which normally means higher consumptions and using other types of standards (i.e. GPRS, LTE, WiMAX…) with other requirements. The choice of the correct standard among the big variety available on the market is a challenging task since many things have to be taken into account (application, software used, type of network, security…).

Nowadays, devices like IoT nodes, mobiles, wearables… require of certain capabilities at limited power. The reduction of voltages, associated with each new generation of advanced CMOS to move towards ultra-low power and ultra-low voltage requirements of some systems, has degraded the performance of many analog/RF circuits in a way of lower noise margins, lower linearity and reduced output power among others. As deeply scaled CMOS technologies have become available, circuit design has required more innovative approaches to make the most of their scaling benefits in power and performance while keeping the reduction in price of the product.

The need of low power energy efficient technologies, which is a key requirement in the market, is because many of IoT devices must survive on a single battery and they typically require long lifetimes. To extend the battery life without decreasing the receiver's performance, the reduction of the current consumption in active or idle state of the device is challenging. Figure 3 shows an example of the power levels needed by autonomous Wireless Sensor Node (WSN), which typically range from the pW to mW area depending on the type of the application, e.g. a simple tracking and monitoring application will require less energy than a full system of video surveillance smart cameras. Some more information about maximum average power consumption as function of battery size can be found in [10].

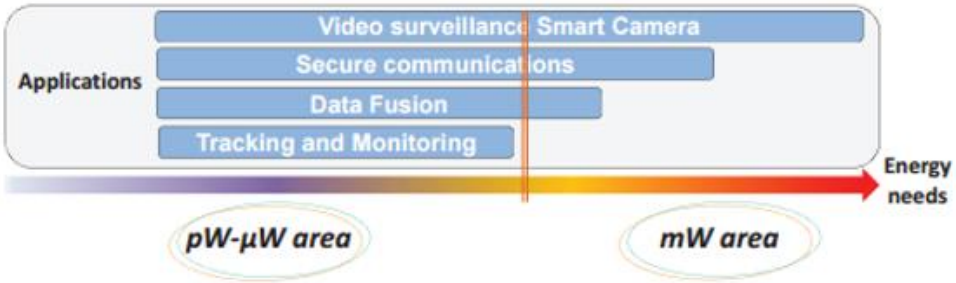

Figure 3 - IoT applications: power needs [11]

Besides the batteries, alternative sources of energy must be considered to avoid problems with powering the device and minimize the device maintenance. A key solution to allow the spread of these technologies is acquiring the energy from the environment close to the sensor, instead of a battery with finite charge capacity. This is known as energy harvesting, the process which captures this energy, and converts it into electrical current, being able to accumulate the charge in order to use it when needed. This enables self-powered IoT devices using this energy on demand, removing their dependence on batteries. Some examples and extended information about energy harvesting systems can be found in [12 - 16]. These energy harvesting systems will not generate either high power or high voltages, and given the scenario, the interest of evolution towards very low voltage and very low power consumption devices makes great sense. Table 1 lists various energy harvesting methods and their power generation capabilities.

Energy source	Power density	Advantages	Disadvantages
Solar	15 mW/cm^3	Sufficient energy in the daytime, high output voltage	Disappear at night
Vibration (piezoelectric)	200 µW/cm^3	Without voltage source	fragile materials
Thermoelectric	40 µW/cm^2	Long life, reliable with low maintenance	Low energy conversion efficiency
Acoustic noise	960 nW/cm^3	High energy conversion efficiency	Rare environments with high acoustic noise levels
Airflow	1 mW/cm^2	Sufficient in certain place and time	Big size
Radio frequency	1 µW/cm^2	Sufficient in urban areas	Few in suburbs

Table 1 - Comparison of different harvesting methods [17]

Energy harvesting raises more challenges to the power supply of the circuit. In fact, the autonomous wireless sensor nodes that get their energy from the environment (solar, thermic, vibration…) will probably suffer from changing energetic environments. This fact implies that the energy level available for the receiver will change along the device life, what entails that the energy supply system will require any type of adaptive scheme. These systems will need to be functional to different supply voltages, which can possibly reach energies around transistors' threshold levels. The presumption of performance at very low speed for low voltage supplies can compromise the correct functioning of the application,

and for this reason, a solution that increases the performance of the circuit for a determined task becomes mandatory.

Although IoT applications may differ from one another, the various requirements demanded in the devices to be extremely small, low cost, and efficient and to have low energy consumption will remain basically the same with certain commitments. Because of this, IoT devices have become highly integrated devices, often including all devices within a module or chip.

In the VLSI era, CMOS became the prevailing technology for manufacturing billions of chips. Nowadays, the electronic systems are adapted to the customers' expectations of better and increasing features with smaller sizes at reduced cost. The continuous advance in CMOS technology has allowed this fact for the last years with the shrinking trend of the transistors achieving better properties with smaller transistors at the cost of power. Besides the feature size reduction, other innovations such as new transistor architectures and the use of new materials have opened new opportunities and challenges for circuit designers. Scaling the technology is no longer just a matter of a geometrical issue but the implementation of these innovations in architectures and materials.

Under the premise that a great number of highly energy efficient small electronic devices are needed for the IoT era, nanometer CMOS technology is the best candidate for these applications because of its low cost, availability and highly integration capability developing new strategies to integrate all the functions (RF, analog, digital…) on a single chip. All this evolution has resulted in different technologies depending on the strategy used such as the already commercially available 22 nm FDSOI technology [18] maintaining the planar structure reaching the 12 nm node by 2019 [19] or going to non-planar structures like the 14 nm FinFET technology [20].

This work will focus on the RF part of the connectivity affected by the physical layer (PHY) of the protocol. As a reference for targeted performance, this work uses the IEEE 802.15.4 standard, which suits the basis of a low power consumption communication between sensors with low data rates for IoT applications. This standard only defines the physical and medium access control (MAC) layers of LR-WPAN. The others layers can be implemented by others standards compatible with this one such as ZigBee, ISA100.11a, WirelessHART, MiWi, SNAP, and Thread [21, 22].

1.3. Design challenges for CMOS RF

RF design is linked to a multitude of disciplines, and it has become a very challenging task to coordinate all these subjects. Figure 4, on the left part, shows and overview of different fields integrated in the RF design.

When the time to design comes there are some trade-offs to take into account in order to obtain the best suited system for your requirements. It is impossible to design a system adapted to be the best in every environment. Figure 4, on the right part, shows a basic idea how the figures of merit of the RF designs are linked and the trade-offs they involve. As an example, if you need a low power consumption design, the noise or frequency attributes will have to be sacrificed to obtain the desired consumption.

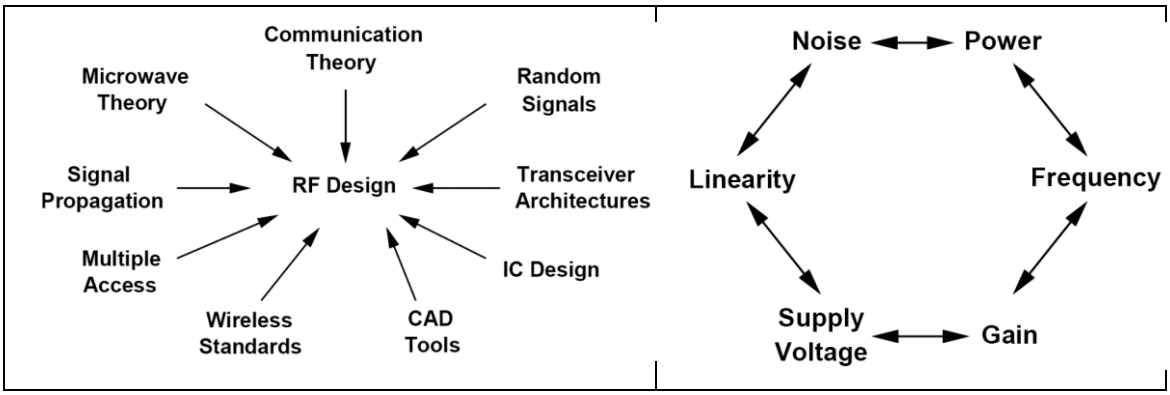

Figure 4 - RF Disciplines and Design hexagon [23]

1.4. MOS scaling limitations and trends

The technology scaling following the Moore's law is getting harder to keep on. In deeply scaled MOSFETs, as they have very narrow channels, small-geometry effects start to affect their behavior. All this phenomena are collective referred to as Short Channel Effects (SCE) and tend to increase standby leakage currents, e.g., the potential of the drain starts to impact the electrostatics of the channel, which makes the gate to lose the adequate control over it. As a consequence, the gate cannot completely shut down the transistor and big sub-threshold leakage currents appear between the drain and the source [24-26]. To alleviate this issue, the use of thinner oxide layers and high-k materials have helped so far but the required gate oxide thickness in current technology nodes is so thin that it is not able to ensure the necessary isolation, implying too big gate and Gate-Induced Drain Leakages (GIDL) [27-29].

Among others evolutions strategies to overcome such problems, one is based on the implementation of a fully depleted channel. Big companies like Intel and STMicroelectronics are already manufacturing these devices and even though both use technologies with the channel fully depleted, they have a different philosophy. While Intel prefers to evolve towards a 3D technology like the Fin Field Effect Transistor (FinFET), STMicroelectronics has kept the planar concept, which makes it simpler to manufacture than FinFETs, with the FDSOI FET technology. The comparison of a cross-section of the different transistors is shown in Figure 5.

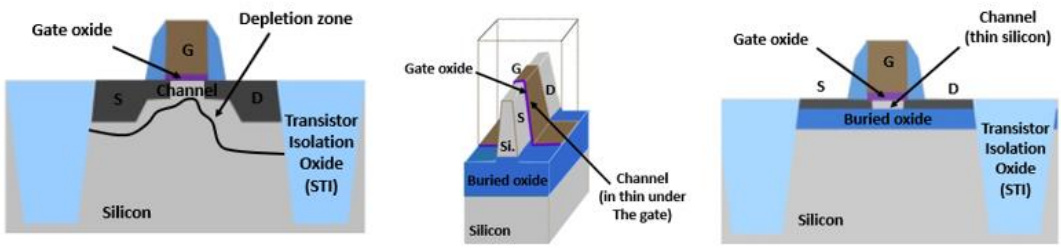

Figure 5 - Cross section of conventional bulk MOS transistor (left), FinFET on SOI (center) and planar fully-depleted (FDSOI) transistor (right) [30]

The basic principle of FinFETs is that the channel is formed on a thin semiconductor fin, which has to be thin enough to obtain a fully depleted channel, perpendicular to the substrate surface. They have a gate that wraps around the channel not only by one surface, which improves the electric characteristics. The substrate can be the conventional one or SOI, which entails some improvements on the performance [31], and they can have more

than one fin to reduce the total parasitic resistance and have more current flowing through it. These devices has already been widely studied for the last decade and a large amount of papers have been published demonstrating the enhancements in SCE behavior compared to bulk MOSFETs [32-35, 36-38].

On the other hand, STMicroelectronics' device consist in an ultra-thin layer, in order to have the channel fully depleted, above an extremely thin oxide isolation layer, so no current can circumvent the channel. This guaranties no floating body effect [39, 40] and the fact that the channel is undoped brings less manufacturing process variations. This technology is simpler to manufacture than the FinFETs and provides better yield at lower cost [11].

The performance at high speed, power consumption and the low cost are very important requirements for RF circuits in which bulk MOS technology is lagging behind. FDSOI CMOS technology seems to satisfy the need of the low power devices, combining high performance and low energy consumption, and at the same time shows good behavior at low supply voltages [30], which makes this technology a good candidate for the RF environment.

1.5. FDSOI as a technology candidate for IOT

Prior to choose any technology, some analysis on the IoT application requirements have to be performed. As commented before, there is a wide range of energy levels needed depending on the applications, so an efficient energy flexibility is a key requirement.

Another issue is where this energy comes from because a lot of this devices will work autonomously in a distributed network harvesting the energy to perform their tasks within a changing energetic environment. This involves a very wide scenario of working conditions over the time for each node of the network, so an adaptive scheme that allows proper function at different voltage supplies, even at very low voltages around threshold levels, is needed. FDSOI has this flexibility to work with proper performance from normal voltage operation mode to low voltage levels.

Moreover, is known that IoT devices will not be continuously sending data and will remain in idle state most of the time. During the idle phases is interesting to have a very low consumption in order to extend the battery life or increase their autonomy, which is achieved by very low leakage systems. The application of a back biasing voltage in FDSOI allows to have a compromise between very low leakage and high speed, changing the operating conditions depending on the phase of the device as demonstrated in [43].

Finally, IoT devices are generally microsystems with a combination of digital and analog mixed signals and RF (RF transceivers, sensors, voltage converters…), and to make them profitable there is the need of having everything fully integrated in a single System on Chip (SoC). FDSOI allows this full integration, as demonstrated in [44], of digital and analog sub-modules maintaining the digital performance and an efficient analog design thanks to the property of threshold voltage (V_{th}) modulation, besides it is less sensitive to noise [45].

Therefore, taking into account all the flexibility needs for the IoT, the properties of the FDSOI technology cover all these points making this technology the most appropriate one for a wide range of IoT applications.

1.6. Objectives

This thesis tries to verify the suitability of the 28 nm UTBB FDSOI technology developed by STMicroelectronics for designing IoT RF blocks. The main points are listed below:

- Get familiar with UTBB FDSOI technology.
- Characterization of 28 nm UTBB FDSOI transistors, with the compact models provided by ST Microelectronics.
- Design of a simple CS LNA with 1V supply fulfilling IEEE 802.15.4 requirements, making use of the capabilities of the UTBB FDSOI technology.
- Design of a simple CS LNA with sub-1V supply fulfilling IEEE 802.15.4 requirements, making use of the capabilities of the UTBB FDSOI technology.

1.7. Thesis organization

To fulfill these objectives the thesis is divided in 5 chapters:

- **Chapter 1**: This is the introduction chapter where the motivation for this project is explained. There is an explanation of what the IoT is and which are some of the basic requirements of the devices that allow this concept. Additionally, the limitations of regular bulk CMOS for this purpose are commented and how other technologies are suitable for IoT. Finally, the main objectives and the thesis structure are included in this chapter.
- **Chapter 2**: This chapter reviews the state of the art in low power and low voltage RF designs. Some examples of papers of RF blocks already published are revised and an introduction to the gm/Id methodology for low power analog circuit optimization is included in this chapter.
- **Chapter 3**: This chapter starts with an overview of the UTBB FDSOI 28 nm developed by STMicroelectronics with its main properties covered. The simulation performed to characterize this technology is presented in form of some representative graphics and tables with the most relevant parameters, comparing some of the different transistors available in this technology that can be part of IoT systems. Finally, the characterization of a transistor in accordance with its inversion degree is presented.
- **Chapter 4**: This chapter presents two CS-LNA designs with this technology in different operating conditions. The first design is supplied by 1 V, the other design is supplied by 250 mV and tries to recover the specifications from the first one using the back bias technique. All these designs come with their proper simulations of the main figures of merit of an LNA.
- **Chapter 5**: In this last chapter the conclusions of the thesis are presented and the possible future work lines to keep on checking the suitability of this technology are mentioned.

2. State of the art on low-power low-voltage LNA design and gm/Id methodology

This section reviews some low power and low voltage Low Noise Amplifiers (LNA) designs extracted from the literature and a brief analysis of the gm/Id approach for low-power analog circuit optimization is performed.

2.1. Case reviews

In the receiving path, the RF signal received is often very small and surrounded by interferers so the Signal to Noise Ratio (SNR) is easily degraded impacting negatively in the receiver performance. Hence, the first stages of an RF receiver should amplify the received weak signal with minimal noise added to the system in order to increase the sensitivity of the receiver. The Noise Figure (NF), or its lineal form noise factor (F), is a metric used to quantify this noise contribution, which describes the amount of noise a component or entire radio receive chain adds to the RF signal received. Therefore, the NF is a key measurement of the performance of an RF receiver and have to be kept as low as possible.

The cascaded values for the overall receiver NF for the system budget of the typical chain of the Figure 6 can be calculated by the Friis's formula (2.1) [46].

$$F_{TOTAL} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \qquad (2.1)$$

Where F_n is the noise factor and G_n is the gain of the n-th stage in the receive chain.

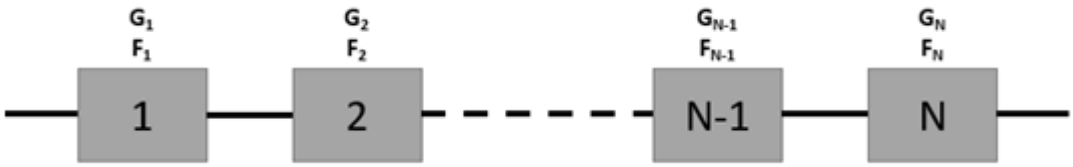

Figure 6 - Typical chain of cascaded components

As the equation shows, the stages closest to the input of the system are the ones that affects the most to the total noise. Consequently, the noise factor of the first stage should be minimum and its gain should be large enough to decrease the total noise contribution of the following stages, but it should be small enough not to saturate the following stages and jeopardize the receiver's linearity. For this reason, normally, the first active stage in a receiver after the antenna is a low noise amplifier (LNA), which have a moderate gain and a low noise figure.

Besides the NF and gain are the main candidates to ensure a receiver performance, other important characteristics involved in a LNA design are shown in Figure 7 [47-52].

Normally, good performance in terms of noise, gain, linearity… of a LNA entails a high power consumption. As a consequence, a lot of effort has been put in low power consumption LNAs design research (<1mW) [53 - 55]. The trade-offs between all this parameters can be taken into account through the FoM commonly used for benchmarking the low power LNA, which consists on the ratio of power gain to the Direct Current (DC)

power consumption (Gain/P_{DC}). Furthermore, it can be extended including the effect of noise figure, linearity (IIP3) and the operation frequency (f_c) with equation (2.2) [56].

$$FoM_{LNA} = \frac{Gain[abs]IIP3[mW]f_c[GHz]}{(F-1)[abs]P_{DC}[mW]} \quad (2.2)$$

Figure 7 - Important features in LNA design

As a first example of LNA designed for very low power consumption, the Figure 8 shows a low-power Ultra Wide Band (UWB) common-gate (CG) LNA implemented in a standard 1P6M 0.18 µm CMOS process presented in [54]. This LNA consists of a cascode CG stage followed by a buffer stage. This LNA has an operating bandwidth from 3 GHz to 10 GHz.

The drawbacks of the traditional input matching network (i.e. L_{S1} only) of CG LNAs include poor input impedance matching at low frequencies and non-flat NF over the frequencies of interest. A wideband input impedance matching is achieved thanks to a T-match input network composed of series resistances and inductances, which improve the matching at low frequencies (S_{11}). The peaking inductor L_C resonates in parallel at the lower corner frequency 3 GHz with the parasitic capacitances at the drain from M_1 and at the source of M_2, while the peaking inductor L_{D2} resonates in series at the upper corner frequency (10 GHz) with the parasitic gate capacitance of M_4. This peaking inductor helps to have a flat and high response of S_{21} and a flat and low response of NF.

In addition, to achieve the low power consumption it uses the self-body-bias technique, which consists on connecting body terminals of M_1 and M_2 by a resistor (R_B), to reduce the threshold voltage of M_1 and M_2. This V_{th} reduction results in a smaller supply voltage, 1.1 V in this case, for a fixed bias current.

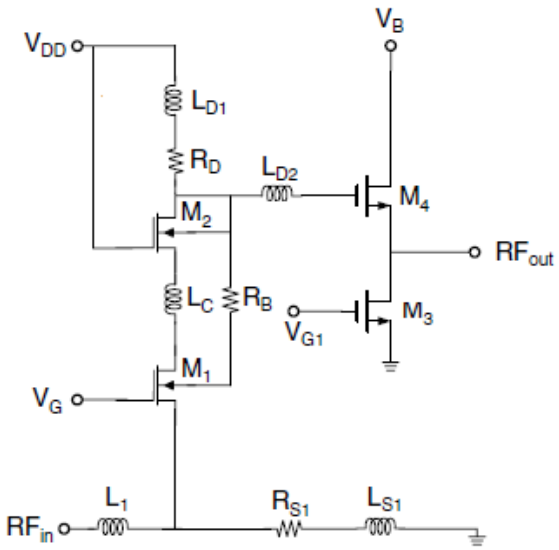

Figure 8 - Schematic of a low power LNA from [54]

The overall performance summary of this LNA can be found in Table 2.

Technology	180 nm
Consumption [µW]	990
Supply [V]	1.1
S11 [dB]	<-10.3
IIP3 [dBm]	NA
Gain [dB]	7.9
NF [dB]	6

Table 2 - Main characteristics of LNA from [54]

A second example is presented in [57]. Figure 9 shows this Ultra-Low-Power (ULP) Ultra-Low-Voltage (ULV) UWB resistive-shunt feedback LNA implemented in a 90 nm CMOS technology. Its frequency operation range goes from 100 MHz to 7 GHz.

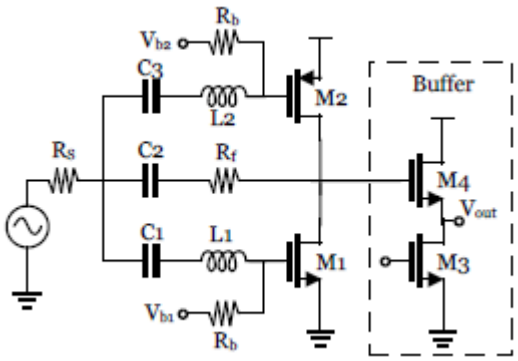

Figure 9 - Schematic of an ultra-low power, ultra-low voltage LNA with buffer for measurement purposes from [57]

This LNA circuit uses the current-reuse technique to improve the overall RF performance for a given power consumption. Current-reuse is an important technique in the

implementation of ultra-low power circuits. The basic idea is to share the DC current between two or more transistors while each transistor contributes to the total gain, thereby reducing the overall power and increasing the current efficiency. This technique has been widely used to reduce the power consumption [58 - 60]. Moreover, the complementary characteristics of transistors M_1 and M_2 (NMOS and PMOS) gives an advantage to ULP designs with additional benefits, such as better distortion and noise cancellation.

Another characteristic of this work is the presence of the gm/Id approach for designing a low-power amplifier. It introduces an extended ULP ULV biasing metric, which takes into account the current efficiency, the intrinsic gain and the transit frequency, to optimize transistor performance. Finally, the biasing metric shows that the transistor working on the MI region maximizes it. This metric also shows the impact of lowering the supply voltage. Lower supply voltages degrades the overall performance but continues showing the MI region as the optimum region to work in.

The input matching is achieved using a shunt-feedback resistor, which provides of wideband matching. However, some restrictions on the design have been taken into account due to the low voltage and low power requirements. In addition, the use of series peaking inductors (L_1 and L_2) in the feedback loop alleviate the gate-source capacitance (C_{gs}) and the miller effect due to the gate-drain capacitance (C_{gd}) extending the input matching and bandwidth. The use of this inductor is a conventional technique to resonate with the parasitic capacitances of the transistors increasing the bandwidth without burning extra power.

Regarding the stability, the presence of a feedback network and boosting inductors rise the instability problem but, in this case, the simulations demonstrated its unconditionally stability.

The performance summary of this LNA can be found in Table 3.

Technology	90 nm
Consumption [µW]	750
Supply [V]	0.5
S11 [dB]	<-10
IIP3 [dBm]	>-9
Gain [dB]	12.6
NF [dB]	5.5 – 6.5

Table 3 - Main characteristics of LNA from [57]

Figure 10 shows the ULP ULV CG LNA implemented in an IBM 0.13 µm 1P8M CMOS technology presented in [61] with a frequency range from 600 MHz to 4.2 GHz.

This work also uses the current-reuse technique. A complementary current-reuse structure can be seen where the input stage transistor M_1 and M_4 share DC current with the cascoded devices M_2 and M_3, respectively, leading to an improvement on the DC current efficiency.

Inductor L_3 at the gate of M1 provides inductive gm-boost [53] increasing the effective gm of the device at the resonant frequency of the inductor with the C_{gs} of M_1 enhancing the bandwidth, gain and input matching without additional power consumption.

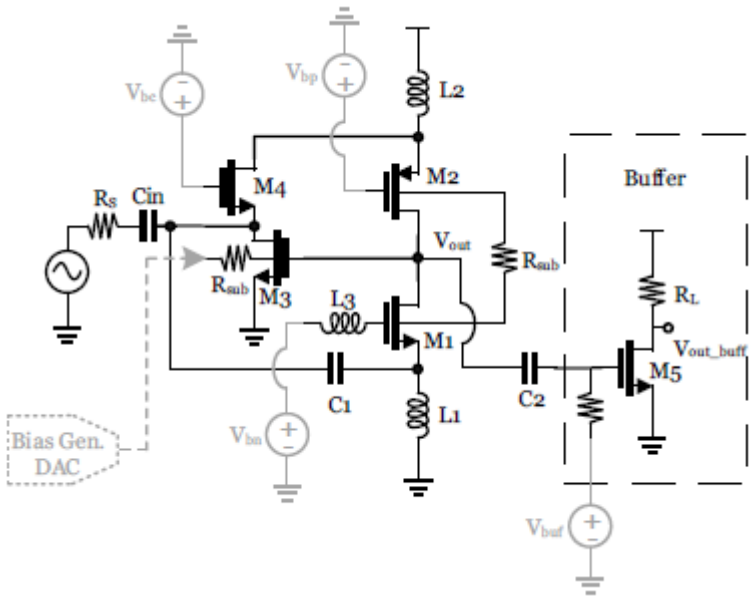

Figure 10 - Schematic of the proposed ULV and ULP LNA along with a buffer stage for measurement purposes from [61]

This LNA uses the forward body bias (FBB) technique which is attractive for ULP ULV circuit designs. The use of ULV supplies limits the choice of biasing voltages and achievable performances such as gain, linearity, operating frequency… The increment of the bulk-to-source voltage (V_{bs}) have a direct impact on V_{th}, reducing it so a lower bias voltage is required to work on the desired region of operation. This work also shows how the use of FBB improves the intrinsic characteristics by mitigating some SCE; as the body potential increases, the drain depletion region decreases, so the control that the drain has over the channel is reduced reducing the drain- induced barrier lowering (DIBL). The FBB is implemented by adding R_{sub} between bodies of M_1 and M_2 [62]. This connection, which includes the source-to-body diodes, creates an ULP self-bias loop. R_{sub} controls the current in this loop, which is in the order of a few µA. Summarizing, this technique improves the output resistance of the transistors increasing the intrinsic gain of the transistor and lower the V_{th} allowing a reduction in the voltages needed.

The same previously commented biasing metric is used in this design, but introducing the effect of the FBB on this metric. It shows that the FBB improves the performance providing further validation of the suitability of this technique for ULV circuits without additional power consumption. It should be noted that transistors M_1 and M_2 are biased in the middle of the MI region and M_3 and M_4 are biased in the WI region.

A folded-cascode structure is used with M_4 and M_2 providing ULV isolation between the feedback node and the output. This isolation is necessary to have a flat gain and good input matching.

The broadband input matching is also obtained with the active shunt-feedback techniques. The transistor M_3 reduces the current needed for this matching paying the price of slightly reduced overall gain and higher NF. Hence, this technique plays a crucial role in the low power LNAs design.

The performance summary of this LNA can be found in Table 4.

Technology	130 nm
Consumption [µW]	250 / 160
Supply [V]	0.5 / 0.4
S11 [dB]	<-9
IIP3 [dBm]	-10 / -12
Gain [dB]	14 / 13
NF [dB]	4 / 4.5

Table 4 - Main characteristics of LNA from [61]

Figure 11 shows the single stage ULP LNA implemented in a standard 0.13 µm CMOS technology presented in [63] dedicated to the 2.4 GHz ISM band.

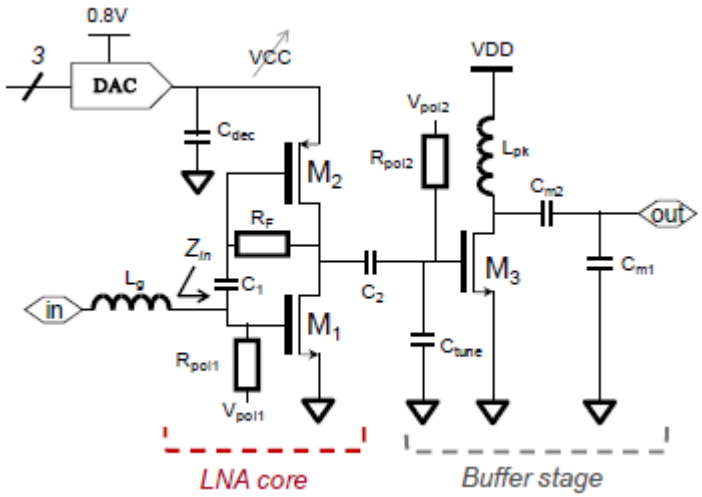

Figure 11 - Simplified schematic of a ULP LNA along with a buffer stage for measurement purposes from [63]

The starting point of this LNA design is based on the FoM $\frac{gm*f_T}{I_D}$. This figure takes into account the current efficiency (gm/Id) and the effect of parasitic such the capacitances, which impact negatively in the RF performance and are represented by f_T. This figure represents a trade-off between them and shows an optimum point when the transistor is biased in the MI region.

The not so high gm performed in this region requires of active topologies, such as a self-biased inverter topology, to compensate the gain. The core of the LNA is based in a self-biased inverter whose supply voltage is controlled by a 3-bit Digital to Analog Converter (DAC). This digital tuning allows maximizing the FoM of the LNA. An additional decoupling capacitor (C_1) is placed between gates of M_1 and M_2 to further decrease the supply voltage.

The buffer stage provides the matching at the output (50 Ω) through L_{pk}, C_{m1} and C_{m2}. It holds on the LNA gain and is only used for measurement purposes.

The performance summary of this LNA can be found in Table 5.

Technology	130 nm
Consumption [µW]	60 / 90 / 130
Supply [V]	0.4 / 0.5 / 0.6
S11 [dB]*	<-10/<-10/<-10
IIP3 [dBm]	-12.2 / -12.6 / -13.1
Gain [dB]	13.1 / 15.2 / 15.7
Min NF [dB]	5.3 / 4.9 / 4.6

Table 5 - Main characteristics of LNA from [63]

*Estimated from the curves.

The last LNA reviewed in this section is shown in Figure 12. It is an ULP LNA with inductive feedback fabricated in a standard 0.18 µm CMOS technology operating at 1 GHz presented in [64].

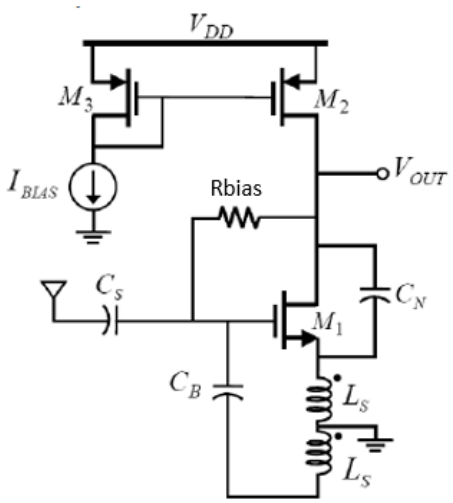

Figure 12 - Schematic of the proposed ultra-low power LNA with inductive feedback and C_{GD} neutralization from [64]

It uses the same FoM as the previous LNA to bias the M_1 transistor, which is biased in MI region to achieve maximum FoM.

A gm-boosting inductive feedback [65] technique is used. The differential inductor feedback the signals at the gate and at the source to follow each other by 180º phase shift. This doubles the gm of the input transistor and provides the input impedance matching to 50 Ω. This technique along with an active load configuration increases the gain at very low bias currents.

The neutralization of C_{gd} is critical in LNA without a cascode structure [66] to maintain the input-output stability. The neutralization capacitance (C_N) is implemented with a dummy NMOS device identical to M_1. Taking into account that the voltages at the gate and at the source are 180ª phase shifted, making C_N equal to C_{gd} cancels out the currents that passes through them to the output node, therefore, neutralizing the feed-forward path through C_{gd}.

R_{bias} connected between the gate and drain of M_1 bias the circuit. This resistor has to be high enough so to not impact on the NF and gain of the proposed LNA. In this case, the designer has taken a value of 100 KΩ.

The performance summary of this LNA can be found in Table 6.

Technology	180 nm
Consumption [µW]	100
Supply [V]	1
S11 [dB]	-25
IIP3 [dBm]	-11.2
Voltage gain [dB]	16.28
Min NF [dB]	3.9

Table 6 - Main characteristics of LNA from [64]

2.2. Gm/Id approach for low-power analog circuit optimization

The electronics development toward smaller technology sizes has been pushed mostly by the digital electronics to have a high density transistors packed. At the same time, the analogue design has suffered this evolution with smaller headroom voltages, dynamic range, gains among other characteristics.

At these technologies dimensions the well-known long channel equations describing the transistors behavior are not accurate anymore. The short channel effects and the need of developing more agile and intuitive new design methodologies imply of a whole technology characterization.

The gm/Id methodology is based on the universal shape of the technology transconductance efficiency (gm/Id) in function of the inversion degree in which the device is [67, 68], and this ratio is obtained by the whole characterization of the transistor process. This methodology is attractive because integrates the operating region of the MOSFET in the design (i.e. from weak through strong inversion) [69, 70] and is currently used for the modern analogue design [71, 72].

2.2.1. Introduction to the gm/Id approach

The DC response of a transistor in saturation can take place in 3 different regions; weak inversion, moderate inversion and strong inversion region.

The weak inversion region appears when the MOSFET works with sufficiently low values of effective voltage. The channel is considered weakly inverted and the drain current is dominated by the carrier's diffusion current. This saturation current, which is expressed in equation (2.1), grows exponentially with the gate-to-source effective voltage (V_{gs}-V_{th}).

$$I_D(WI) = 2n\mu C_{ox} U_T^2 \left(\frac{W}{L}\right)\left(e^{\frac{V_{gs}-V_{th}}{nU_T}}\right) \qquad (2.1)$$

The strong inversion region appears when the MOSFET works with sufficiently high effective voltage values. The channel is strongly inverted and the drain current is mostly related with the drift current. This saturation current is proportional to the squared gate-to-

source effective voltage and excluding geometrical effects, such as the saturation velocity, can be expressed with equation (2.2).

$$I_D(SI) = \frac{1}{2}\left(\frac{\mu C_{ox}}{n}\right)\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2 \tag{2.2}$$

The region between these two is called the moderate inversion region and have no defined current expression or is too complex to calculate. For this reason, to design in an efficient and intuitive way is necessary an all-regions unified model like the EKV Model [73]. This model proposes an inversion coefficient (IC) which is an inversion degree's metric which defines the region where the transistor is operating in quantifying the inversion degree. This coefficient is determined by equation (2.3) [68].

$$IC = \frac{I_D}{I_o \frac{W}{L}} \tag{2.3}$$

Where I_D is the drain current, W is the width, L is the length and I_O is the normalization current named the technology's specific current defined in equation (2.4).

$$I_o = 2n\beta U_T^2 \tag{2.4}$$

Where n is the substrate factor, $\beta=\mu C_{ox}$ is the transfer parameter, $U_T=KT/q$ is the thermal voltage, μ is the carriers' mobility factor and C_{ox} is the oxide capacitance per unit area. In this way, normalizing the drain current removes any size or technology dependence of the inversion coefficient.

The center of the moderate inversion region, assuming long channel behavior, is defined where the drain current is exactly the same to the technology's current and is equivalent to IC=1 [70]. From this point, the boundaries of the regions are defined as follows [74]:

- Weak inversion region – IC < 0.1
- Strong inversion region – IC > 10
- Moderate inversion region – 0.1 < IC < 10

The gm/Id Figure of Merit (FoM) is one of the most important figures for low power applications. This FoM, which is very useful for the transistors sizing [75, 76], basically measures how much transconductance can be obtained for a fixed bias current and is closely linked with the IC. A simple expression of gm/Id is given by the equation (2.5) [74, 77]:

$$\frac{gm}{Id} = \frac{1}{nU_T}\frac{1}{(0.5 + \sqrt{IC + 0.25})} \tag{2.5}$$

The transconductance efficiency has two clearly recognizable regions; the weak inversion region and the strong inversion region. The weak inversion region behavior boundary is defined by a close to the thermal level flat asymptote, and the strong inversion region boundary is defined by an asymptote which is approaching in a square law relation to the gm/Id response [70]. As previously commented, as long as the short channel effects are neglected, the strong inversion current follows a squared law dependence, therefore, the asymptote has a -1/2 slope; on the other hand the weak inversion asymptote is simply a flat line with slope 0. The point where both asymptotes cross matches the middle of the moderate inversion region as Figure 13 shows.

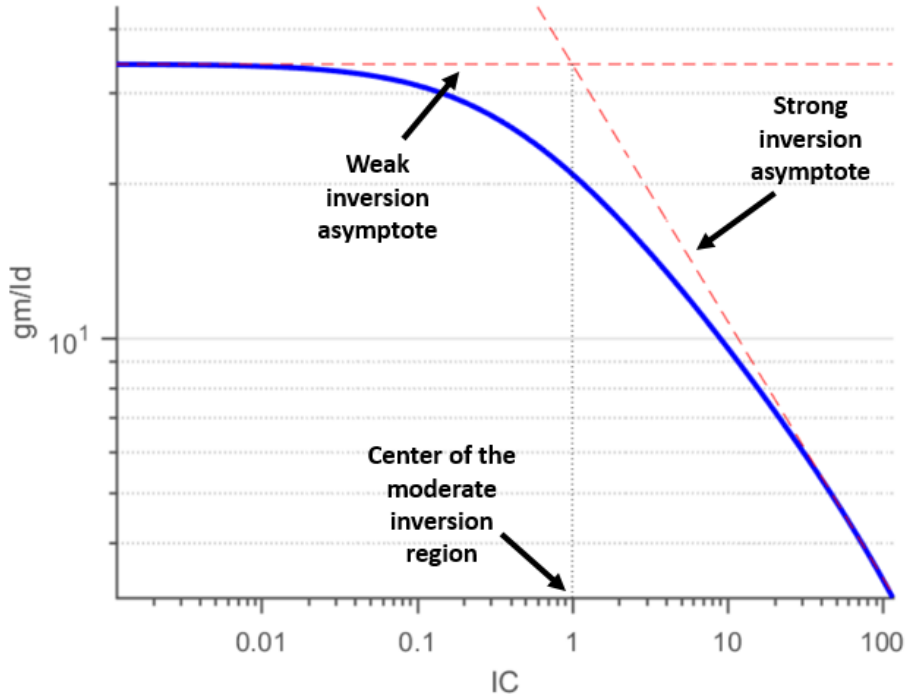

Figure 13 - Transconductance efficiency vs. inversion coefficient (IC)

2.2.2. Determining the specific current

Looking the equation (2.3), the extraction of the technology current to calculate the inversion coefficient is needed. An easy direct method to obtain it through simulations is explained in [78], which is based on the properties of gm/Id commented before.

The weak inversion asymptote is a horizontal line where the transconductance efficiency approaches the thermal limit. The strong inversion asymptote, assuming saturation and long channel conditions, is a line with -1/2 slope on a logarithmic scale. The reason why it has to be performed in a long channel transistor is because in short channel devices, its strong inversion response is degraded much faster due to the velocity saturation effect, so the asymptote in those cases have a steeper slope [79]. Therefore, this method must be performed in a long channel transistor and biased in saturation region.

Figure 14 shows the flowchart of the method to obtain the specific current of a transistor, which has been implemented with MATLAB after the extraction of the gm/Id vs. Id/W/L data from CADENCE simulations using the Process Design Kit (PDK) of this STMicroelectronics technology. The MATLAB code can be found in appendix 1. This algorithm basically plots

these two asymptotes and moves the strong asymptote horizontally until it coincides with the gm/Id curve. The point where the two asymptotes coincides determines the specific current (I_o=Id/W/L).

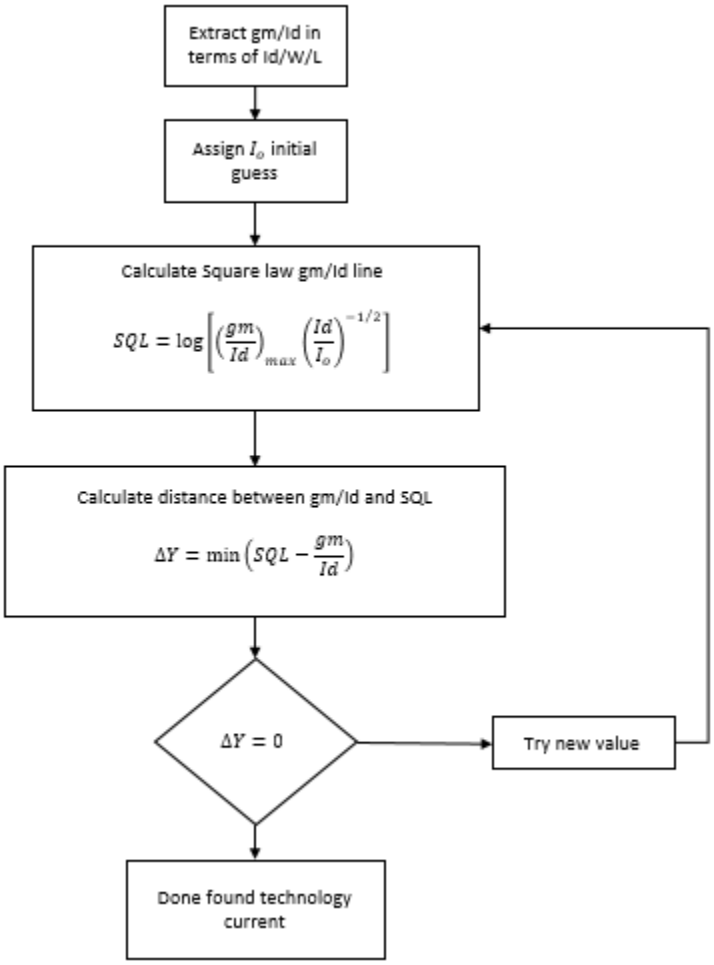

Figure 14 - Technology Current (I_0) Determination Flowchart [78]

The steps are the following:

- First the curves of gm/Id in terms of current density have to been extracted from the model.
- Then, an initial guess of the technology current have to be determined. In this thesis case, it is determined as a current in the strong region behavior.
- The next step is to calculate the square law gm/Id line and calculate the distance between the line and the gm/Id curve. The gm/Id_{max} is obtained in the weak inversion region.
- If the distance is zero or close to zero the I_o used to calculate the SQL is the correct one. In other case it is slightly modified and the process is repeated. In the case of this thesis it is decreased in steps of 10 nA.

Although n, μ and C_{ox} are not constant along all gate lengths [79, 80], they are assumed constant for simplicity purpose, and hence the same specific current will be used for the narrow channel devices.

2.2.3. Gm/Id design methodology

This method relies on the relationship between the gm/Id ratio and the inversion coefficient to explore the design space. The knowledge of the inversion level allows proper evaluation of the design trade-offs among the performance such as gain, bandwidth… [68]. Considering that the relationship is independent of transistors sizes [75], it gives a unique technology characteristic for all the same type transistors of a given batch providing an easy way to determine their dimensions.

The maximum current efficiency is achieved at WI regions and it decreases as the transistor moves to stronger inversions. However, low levels of inversion implies lower performance of the transistors in term of gains, frequency…, so a trade-off between efficiency and performance have to be assumed. This trade-off shows the existence of an optimum in the compromise bandwidth-consumption which generally appears in the MI region. Figure 15 shows the tradeoffs between inversion regions and channel length for a fixed drain current.

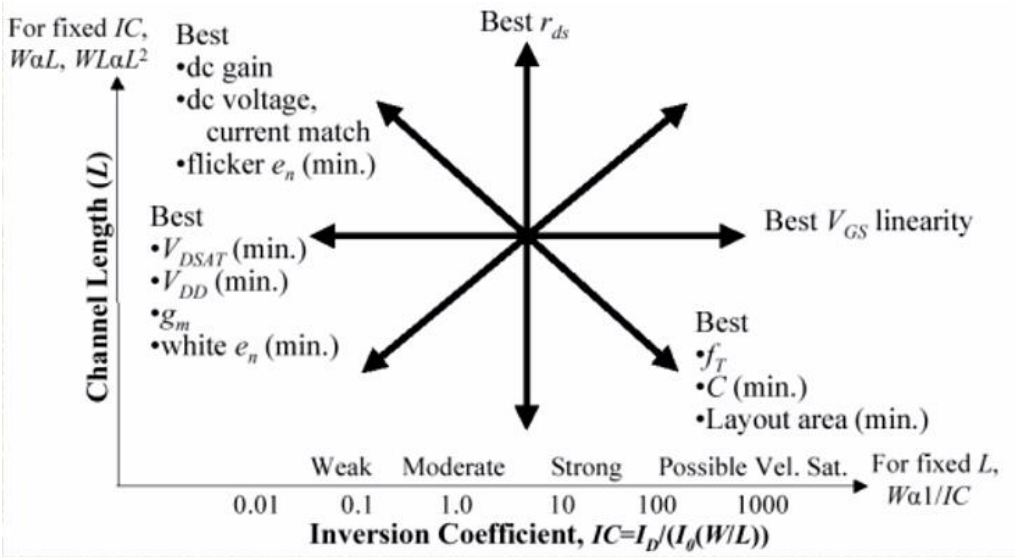

Figure 15 - MOSFET operating plane [8]

The basic design flow with this methodology used in this thesis would be as follows:

First the relationship between gm/Id and the IC needs to be extracted from simulations or using a transistor model valid in all inversion regions. Then the inversion degree of the transistor is chosen to fulfill the frequency requirements, while at the same time trying to maximize the current efficiency. The IC selection implies the selection of the current density (Id/W/L) of the transistor.

Once the gm required is calculated for the application, the current needed is determined from the ratio. From this current along with the IC previously defined, the aspect ratio of the transistor is easily obtained. Then the sizing of the transistor only requires the decision of which gate length is used. The length is selected depending on the characteristics desired; shorter lengths imply higher f_T (high speed) and larger lengths bring higher intrinsic gains for example.

The results obtained are an initial guess of the final design so they have to be adapted or fine-tuned to reach the best solution.

This thesis is focused on using the minimum channel length to achieve higher operating frequencies at lower IC for power concerns, in other applications the length choice is

another parameter to take into account for other characteristics, i.e. for minimizing the power [81].

3. UTBB FDSOI CHARACTERIZATION

This section has a description of the UTBB FDSOI 28 nm technology, the characterization of the transistors with the relevant parameters in terms of voltages and dimensions, the characterization of a Low threshold Voltage (LVT) NMOS transistor in terms of inversion degree, the effect of the back-gate bias on its overall performance and the characterization of the inductors of this technology.

3.1. UTBB FDSOI 28 nm technology

The Fully Depleted Silicon on Insulator technology architecture is a planar Field Effect Transistor (FET) technology manufactured on silicon, with some modifications focused to overcome the short channel effect limitations of conventional bulk CMOS technology. Among the FDSOI architectures, the UTBB FDSOI is one of the most promising technologies to keep valid the Moore's law with the planar paradigm avoiding more complex manufacturing processes like de 3D FinFet technology [82]. The device structure is shown in Figure 16 and consists of a substrate with 10-12 nm silicon layer on a 25 nm buried oxide [83]. It has a high-K metal gate and the raised source/drain are needed to reduce source/drain and contact resistances [83]. A hybrid section has been introduced enabling the co-integration of bulk and SOI devices on the same die to be compliant with the already existing design developed in bulk technology [84].

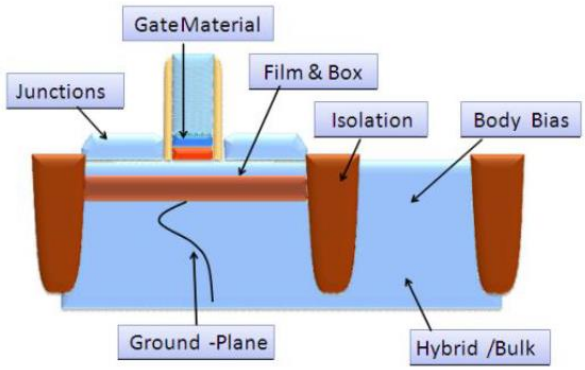

Figure 16 - 28 nm UTBB device structure [84]

The main differences between this technology and the conventional CMOS are shown in Figure 17. The ultra-thin buried oxide layer (BOX) isolates the bulk from an extremely thin layer of silicon where the channel is formed under the gate.

The BOX reduces the source/drain capacitances and the leakage current to the substrate providing electrical isolation of the source and drain from its well and substrate confining the channel between source and drain and close to the gate. The presence of a BOX allows the suppression of fringing electric fields, thus further improving SCE control, reducing the sub-threshold slope and the DIBL [85, 86]. As a result and FDSOI shows superior electrostatic gate control characteristics and performances compared to bulk transistors [87]. Bulk MOSFETS scaling relies on halo increment and well doping, resulting in increase of leakage currents, GIDL and device variability, in contrast, the thin SOI channel in FDSOI remains undoped to achieve the control of the short-channel effects, thus the Random Dopant Fluctuations (RSD) issues are eliminated reducing the impact of process variability [88] and improves the channel mobility as well as device matching [89].

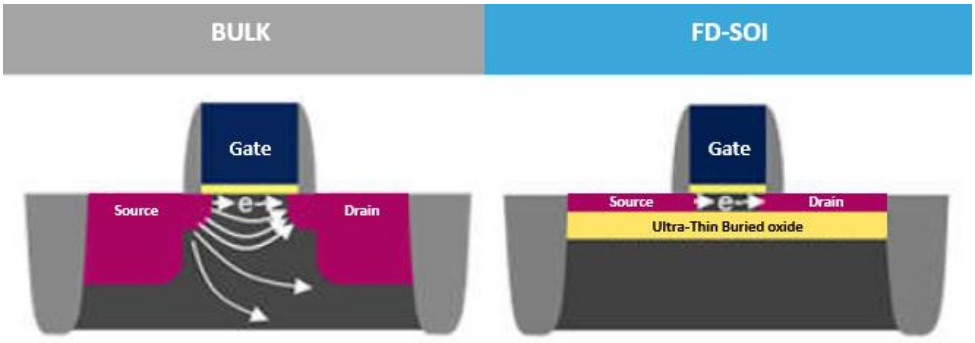

Figure 17 - Architectural difference between bulk and FDSOI transistor [40]

Although FDSOI was first developed for high-speed at low voltage digital application, it could give important enhancements in analog design with higher performance and energy-efficiency than conventional bulk technology. 28 nm UTBB FDSOI CMOS, which is fully compliant with the bulk CMOS, is available from STMicroelectronics and is a perfect candidate for high speed and very low operation voltage [90].

The 28 nm FDSOI PDK contains various types of transistors and passive elements which some of them will be reviewed in this chapter, such as the thin oxide Regular Threshold Voltage transistor (RVT), thin oxide Low Threshold Voltage transistor (LVT) and high-Q inductors.

3.1.1. Body Bias

The body effect or the back gate effect describes the impact of the source to bulk voltage (V_{SB}) on the V_{th}, which can be expressed as equation (3.1). When the body is not tied to the source the body can be considered as a second gate which changes the V_{th} [91]

$$V_{th} = V_{tho} + \gamma\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|} \tag{3.1}$$

where V_{tho} is the threshold voltage with zero source to body voltage, $\gamma = \sqrt{2q\epsilon_{si}N_{sub}}/C_{ox}$ is the body effect coefficient, q is the electron charge, ϵ_{si} is the dielectric constant of silicon, N_{sub} is the doping concentration of the substrate, C_{ox} is the gate oxide capacitance per unit area, $\Phi_F = (kT/q)\ln(N_{sub}/n_i)$ is the bulk potential, k is the Boltzmann constant, T is the temperature, n_i is the material's intrinsic carrier concentration, and V_{SB} is the source-body potential.

This impact can be exploited to obtain some benefits. The application of voltages to the body that increases V_{sb} implies a V_{th} increment. This is a technique called Reverse Body Bias (RBB) and reduces leakage but lowers the overall performance of the transistor (less current, less gm…). On the other hand, if the voltage applied reduces V_{sb}, then V_{th} is reduced as well. This technique is called Forward Body Bias (FBB) and increase the overall performance (more current, more gm…) at expenses of higher leakage [92].

Bulk technologies presents a very limited voltage range when this technique is applied. On the RBB the voltage can't be under -300 mV due to the GIDL, and on FBB the voltage is limited to +300 mV to not turn the diode formed in the junction between the drain/source and the substrate [84]. Moreover it becomes inefficient for reduced sizes [93].

The body biasing is one of the strong points of UTBB FDSOI technology, where different voltage levels can be applied dynamically at the gate and below the oxide independently acting each other as independent gates controlling the channel behavior. The combination of both levels can be optimized to tune the transistor either high-performance or low-power transistors. Due to the isolation from the substrate, bulk-source and bulk-drain junction diodes are eliminated, which enables a wider voltage range that can be applied on the back-plane going from -3 V to 3 V depending on the transistor as shown in Figure 18.

Although other co-integration schemes based on single-well (SW) approach appearing new V_{th} flavors are available in 28 nm UTBB FDSOI technology [94], this thesis will only focus on two flavors of V_{th} that appear depending on the combination of the wells showed in Figure 18 [95], which are the following:

- Low Threshold Voltage (LVT) devices are built on a flip well, the NMOS stays on a P-well and the PMOS stays on an N-well. LVT devices are focused on the Forward Body Bias (FBB) which enables a strong improvement in the switching speed at the cost of higher leakage. The maximum back biasing voltage should be higher than half of the breakdown voltage of the P-N diode that appears between wells. The diode voltage is nearly 0.7 V, so the figure illustrates the -300 mV inferior limit. Although the theoretical maximum is 3 V, the ST Microelectronics literature tells that the LVT models are only qualified up to 1.3 V.

- Regular Threshold Voltage (RVT) devices are built on a conventional well, the NMOS stays on a P-well and the PMOS stays on an N-well. RVT devices are focused on the Reverse Body Bias (RBB) which enables a strong reduction effect on the transistor quiescent leakage current. The maximum back biasing voltage should be less than half of the supply voltage and the breakdown voltage of the P-N diode that appears between wells to not turn it on and have excessive leakage. The diode voltage is nearly 0.7 V, so the figure illustrates the $V_{DD}/2$ + 300 mV superior limit. Although the theoretical minimum is -3 V, the ST Microelectronics literature tells that the RVT models are only qualified up to -1.3 V.

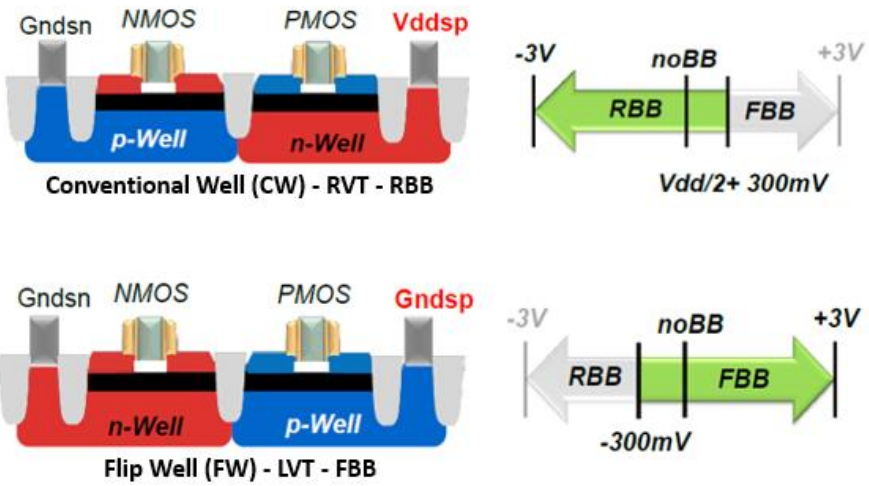

Figure 18 - Cross-sectional view of UTBB FDSOI NMOS and PMOS devices with different wells [96]

Figure 19 shows the V_{th} modulation performance of this technology for a LVT NMOS which offers a higher body-factor over bulk MOSFETS of 85 mV/V against 25 mV/V [84]. This

flexibility allows designers to optimize the performance and leakages of the transistors depending on the design specifications [97, 98].

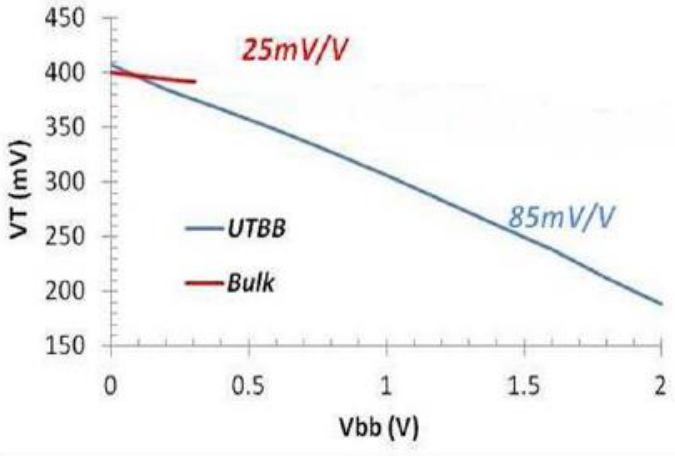

Figure 19 - Body bias efficiency of 28 nm UTBB FDSOI vs. Bulk [96]

The impact of the body biasing in performance of the transistor can be seen in Figure 20. On the left of the picture the FBB effect shows how the operating frequency is increased. The maximum boost happens for the lower supply voltage because the V_{dd}-V_{th} headroom is decreased, meanwhile for higher ones the boost is not so outstanding due to back-bias effect saturation trending. The right part shows the effect of the RBB on leakage power reduction. When performance is not required, RVT transistors can achieve a drastic leakage reduction by a factor of 50.

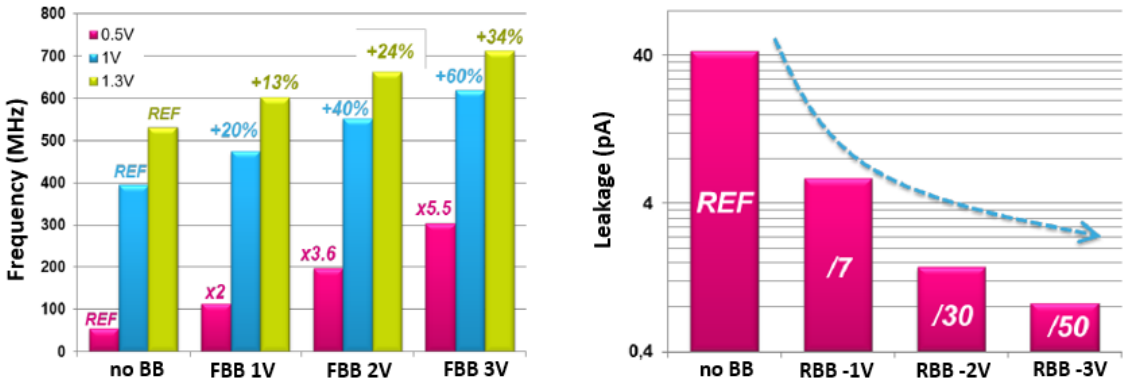

Figure 20 - Speed leakage benefits of FDSOI over Bulk technology [96]

Summarizing, to draw the maximum benefits of FDSOI technologies they have to be applied in low voltage operations which perfectly fits the ultra-low power IoT scenarios. The flexibility offered by FDSOI in choosing the biasing range depending on the performance needs of the moment is showed in [99] where the system can achieve energy efficiency from 1.4x to 3.7x greater that other low power processors with comparable performance. The use of the forward back-bias voltages can increase the performance by 300% at 500 mV of supply voltage as [43] shows. Furthermore, another way to modulate the V_{th} is with the poly biasing (PB) technique which modulates the gate length of the transistor. The range spans from 24 to 40 nm with a 2-nm step [100]. Even though PB increases the length, the active area remains the same but it will have a small impact on the Cgs and Cgd

capacitances. A small increment of the gate length can effectively reduce the leakage power. In [101,102] some applications of this technique are shown.

3.2. UTBB FDSOI 28 nm technology transistors characteristics

This section shows the basic DC characteristics of the different transistors provided. Figure 21 shows the basic test circuit used to extract these characteristics of a LVT NMOS transistor. It consists of a LVT NMOS transistors and three voltage sources to control the drain, gate and bulk voltages.

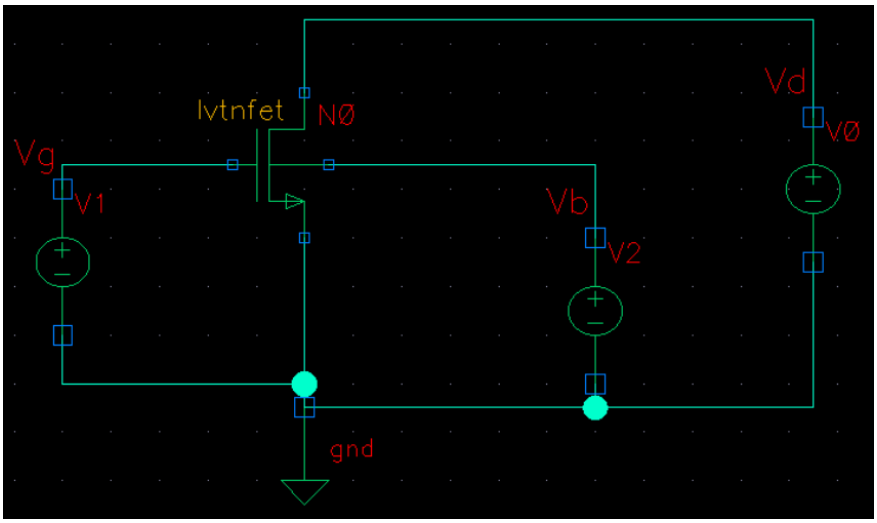

Figure 21 - Test circuit for LVT NMOS characteristics characterization

The experimental drain current in terms of gate voltage of LVT NMOSFET is plotted in Figure 22. The left side of the figure shows the Id-Vg relationship with a V_{gate} sweep from 0 V to 1 V with different V_{drain} (0 V, 0.2 V, 0.4 V, 0.6 V, 0.8 V and 1 V) and V_{bulk} = V_{source} = 0 V for a 30 nm gate length transistor with an aspect ratio of 10.

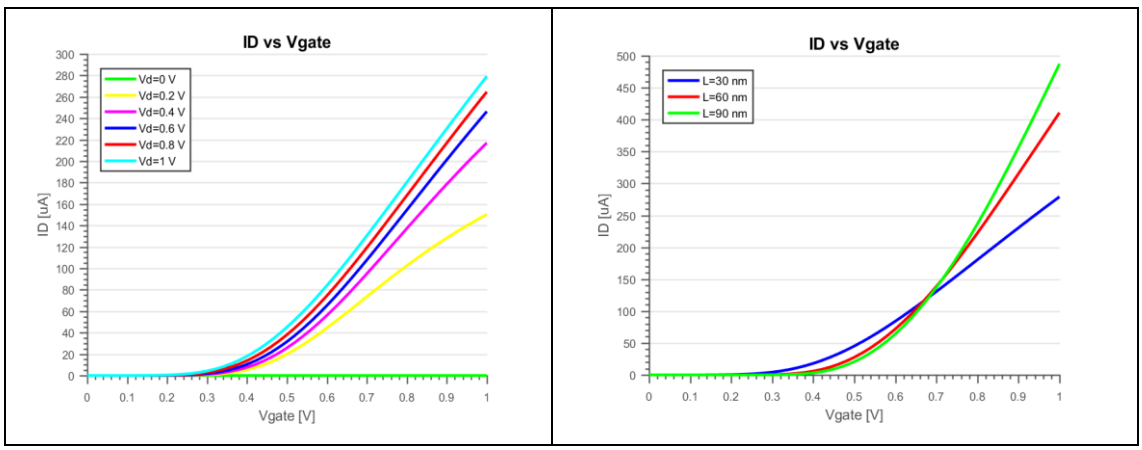

Figure 22 - Id vs Vgate characteristic of a LVT NMOS with W/L=10

The right side shows the effect of the gate length on the Id-Vg relationship. The V_{gate} sweep is the same as before, but with a fixed V_{drain} of 1 V to ensure the saturation of the device for three different gate lengths (30 nm, 60 nm and 90 nm) keeping the aspect ratio of 10.

The fact that a 30 nm length gate it does not show the quadratic relationship with the gate voltage manifest that it has a short channel behavior, and how the increment of gate length starts to change the behavior to long channel regime. It is seen that as long as the gate

length is increased the slope is as well, confirming an increment of current and transconductance.

Figure 23 presents the drain current characteristic in terms of drain voltage of LVT NMOSFET. The left side of the figure shows the Id-Vd relationship with a V_{drain} sweep from 0 V to 1 V with different V_{gate} (0 V, 0.2 V, 0.4 V, 0.6 V, 0.8 V and 1 V) for a 30 nm gate length transistor with an aspect ratio of 10.

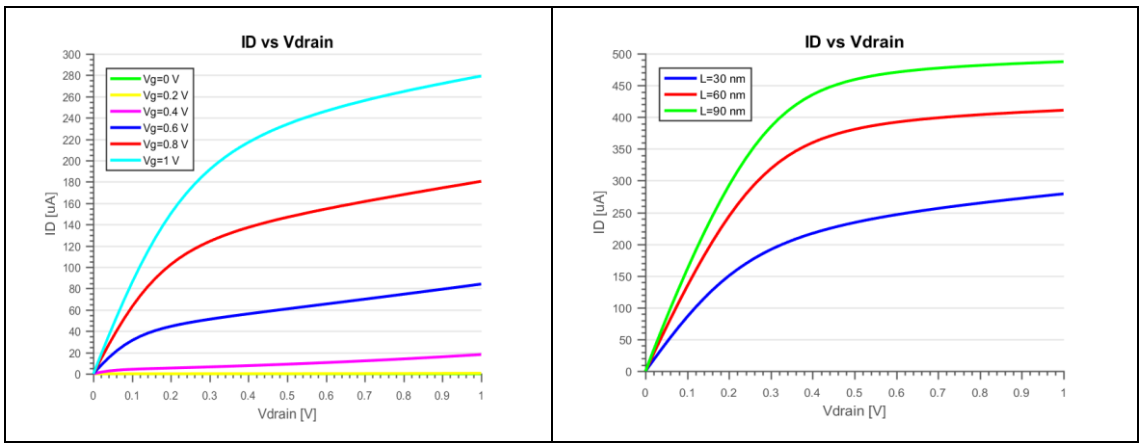

Figure 23 - Id vs Vdrain characteristic of a LVT NMOS with W/L=10

The right side shows the effect of the gate length on the Id-Vd relationship. The V_{drain} sweep is the same as before, but with a fixed V_{gate} of 1 V for three different gate lengths (30 nm, 60 nm and 90 nm) keeping the aspect ratio of 10.

The transfer curves matches the conventional behavior in linear and saturation regimes. As expected, they show a significant dependence of Id with Vdrain in short channel regimes, in other words, a low small-signal output resistance. The increment of gate length enhances the control over the channel, thus the drain voltage have less effect on current, decreasing the DIBL and the Channel Length Modulation (CLM) increasing small-signal output resistance.

Table 7 shows different values of the 4 types of transistors in strong inversion for Vgs = 1 V, Vds = 1V, L= 30 nm with an aspect ratio of 10. The following facts can be extracted from this table.

- LVT transistors have lower threshold voltage than the RVT ones, which indicates that the first ones are more suitable for applications with higher performance requirements while the RVT are more suitable for low leakage applications.
- LVT devices have a higher current density and transconductance than RVT transistors for the same bias conditions which enforces the previous suitable applications commented. Furthermore, LVT transistors have higher transconductance efficiency, so for low power applications, LVT MOSFETS are better.
- RVT devices have lower V_{DSsat} than LVT MOSFETs. The fact that for applications that need lower supply voltages and do not need require high gains RVT devices are a good choice.
- Regarding the capacitances, the LVT transistors present slightly lower parasitic capacitances than RVT transistors, which involves that LVT devices are more suitable for high frequency applications than the RVT.

The choice of which kind of transistor to be used will be made depending on the requirements of the final application. To make this decision the fact that LVT are focused to FBB and RVT to RBB shall be reminded.

	LVT		RVT	
	NMOS	**PMOS**	**NMOS**	**PMOS**
Id [µA]	279.22	121.94	254.62	107.07
gm [µS]	477.4	300.9	424.4	230.8
gds [µS]	67.59	35.72	52.04	38
V_{th} [mV]	272.05	326.45	324.82	331.77
Cgg [aF]	246.24	222.47	246.51	226.41
V_{DSsat} [mV]	338.15	443.03	297.08	428.27
gm/Id [V^{-1}]	1.71	2.47	1.67	2.16
λ [V^{-1}]	0.24	0.29	0.2	0.35

Table 7 - MOSFET characteristics values in saturation region for the 4 types of transistors

The one stage CS-LNA design requirements for this thesis are commented in the next chapter, but they will require of a moderate frequency, moderate gain, low power consumption and a low supply voltage. Therefore, the most adequate transistor for this applications is the LVT NMOS transistor.

3.2.1. Width dependence

The gm/Id methodology is used to obtain the optimum IC to have a good trade-off between f_T and current efficiency. Once determined this point, in case more gm is needed, the total width is increased affecting not only the gm but other parameters. In appendix 2 the simulations of the main parameters in terms of total width for a NMOS LVT transistor are shown.

The width sweep has been performed from 80 nm to 90 µm.

- We can observe in Figure 24 that gm is lineally proportional to the total width.
- gds is also lineally proportional to the total width. The gm and gds have similar slope so the intrinsic gain will be maintained constant as the graph with gm/gds shows.
- V_{DSsat} slightly changes at the beginning with thinner sizes but we can assume it is constant.
- V_{th} decreases 20 mV from thinner devices to wider ones but then it also is kept constant.
- Thinner transistors have slightly better transconductance efficiency but not too much to take into account.
- The total Cgg is also lineally proportional, which is normal since it is proportional to the total gate area.
- The f_T is proportional to gm, which is proportional to W, and inversely proportional to Cgg, which is also proportional to W, then f_T is expected to be width independent. However, as Figure 24 shows this does not hold in experiments due to strong parasitic effects and, while the width reduces, the fringing field effect at the perimeter of the transistor becomes relatively important, hence the gate

capacitance does not proportionally reduces with width [103, 104]. This is the main reason to size the width with the number of fingers, which ideally will increase the total width but without affecting the frequency as is shown latter.

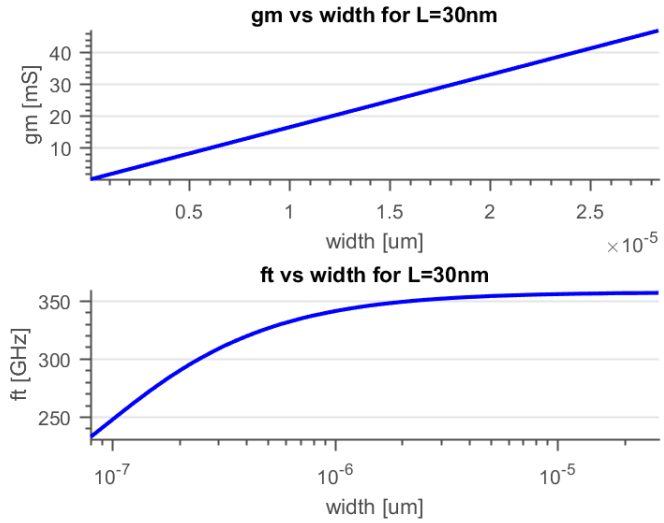

Figure 24 - NMOS LVT gm and f_T vs. Total width for a 30 nm gate length transistor. The measurements correspond to a RF DUT having an aspect ratio of 10, gate length of 30 nm, Vgate = 1 V and Vdrain = 1 V.

3.2.2. Fingers dependence

In appendix 2 the simulations of the main parameters in terms of number of fingers for a NMOS LVT transistor are shown. The number of finger has been swept from 1 to 30 fingers.

- Figure 25 shows that gm is lineally proportional to the number fingers.
- gds is also lineally proportional to the number of fingers with the same slope as gm, and thus the intrinsic gain will be maintained constant as the gm/gds graph shows.
- V_{DSsat} slightly increases (few mV) with the number of fingers but it is not a big impact.
- The gm/Id and the V_{th} are kept constant with the number of fingers.
- The Cgg is also lineally proportional, which is normal since it is proportional to the total area of the gate.
- Figure 25 shows that initially f_T slightly decreases with the number of fingers but seems that the trend is to keep the frequency constant as the number of fingers increase.

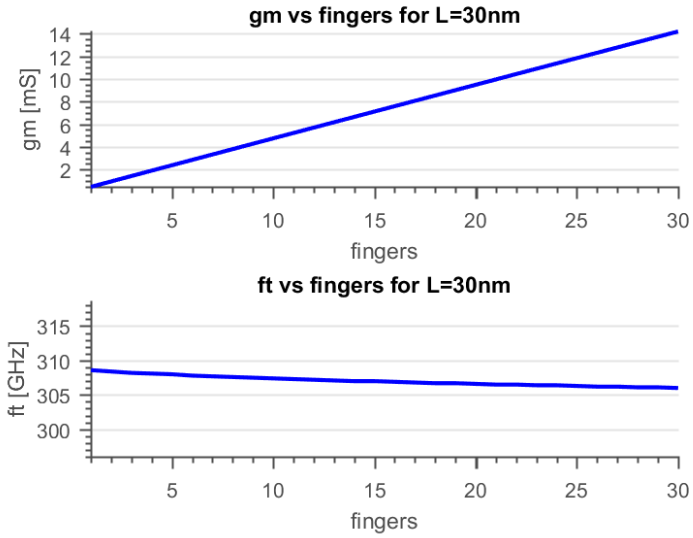

Figure 25 - NMOS LVT gm and f_T vs. Number of fingers for a 30 nm gate length transistor and 300 nm of finger width. The measurements correspond to a RF DUT having an aspect ratio of 10 and gate lengths of 30 nm and finger width of 300 nm, at Vdd = 1 V.

3.3. LVT transistor characterization as function of its inversion degree

Figure 26 shows the basic test circuit used to extract the IC characterization for all the parameters showed of a LVT NMOS transistor. It consists of a LVT NMOS transistors, two voltage sources to control the drain and gate voltages, a current source on the source terminal to make the current sweep, and a buffer to maintain constant the differential voltage of V_{ds} at 1 V.

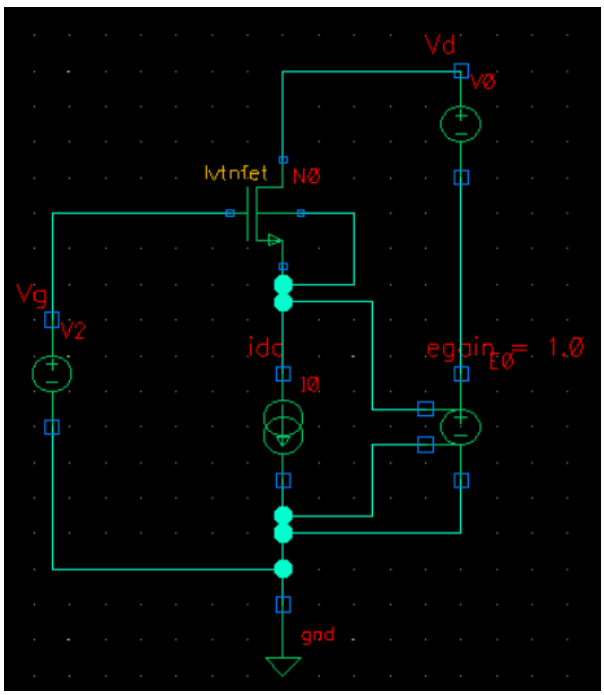

Figure 26 -Test circuit for IC characterization of the LVT NMOSFET

In this section the characterization in terms of the inversion coefficient is performed for the LVT NMOSFETs with the evolution of the main parameters of the transistor in terms of the inversion degree. Most of the explanations of the parameters evolution are extracted from

the reference [103]. To perform this characterization and define a reference boundaries between regions, as explained in chapter 2, the specific current of the transistor is needed. The extraction of Ispec is performed in a wide and long-channel device so it behaves apparently close to an ideal device with no SCE. Following the methodologies explained in chapter 2, section 2, the Ispec of the device has been found to be 858.2 nA as Figure 27 shows.

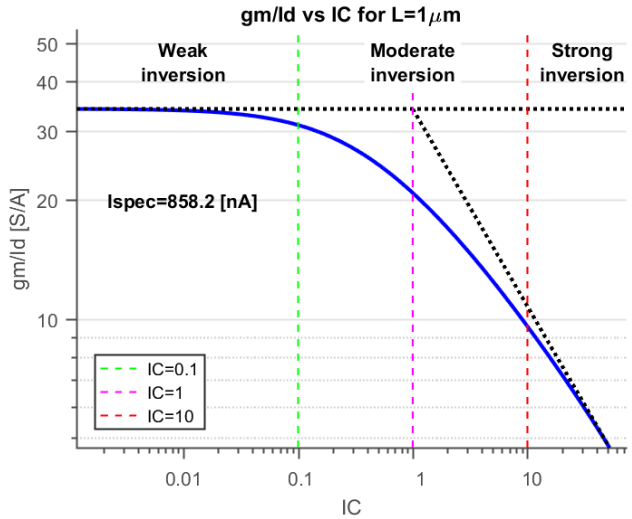

Figure 27 - Extraction of the specific current Ispec, which corresponds to the value of Id at which the SI asymptote is equal to gm/Id in WI. The measurement corresponds to an RF DUT having W=1 µm and L= 1 µm, at Vdd = 1 V.

3.3.1. Transconductance efficiency

Figure 28 shows the transconductance efficiency in terms of inversion coefficient in saturation for a short-channel device (L= 30 nm) with an aspect ratio of 10 with the same specific current previously obtained. As shown, the conductance efficiency degrades faster in SI for a short-channel device having a steeper slope on this region, which means that a higher current is required to obtain the same transconductance for a short-channel device.

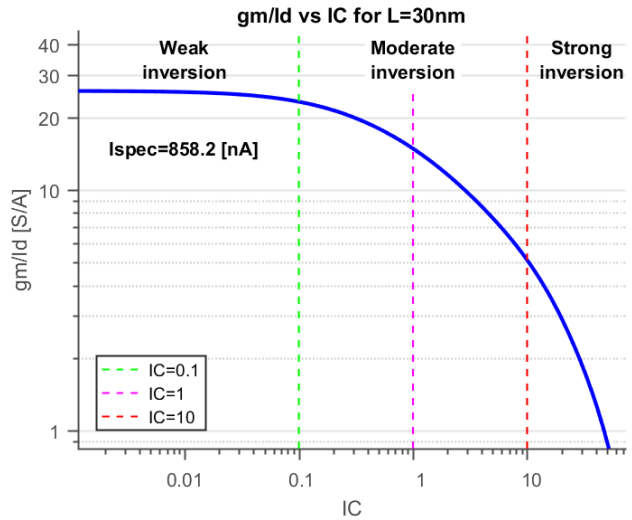

Figure 28 - Transconductance efficiency vs. inversion coefficient for a short-channel device. The measurement corresponds to an RF DUT having W=300 nm and L= 30 nm, at Vdd = 1 V.

On Figure 29 the relative conductance efficiency in terms of inversion coefficient for various channel lengths devices (1 µm, 90 nm, 60 nm and 30nm) with an aspect ratio of 10 are

shown. This figure manifest how the behavior in SI is degraded as long as the channel length is reduced. However, the trend of the transconductance efficiency remains invariant in WI even though the SCE have a strong impact on the drain current and the transconductance. According to [105], the transconductance is proportional to the drain current in the WI region so, gm and Id are affected in the same way, which is why the trend of the ratio is the same.

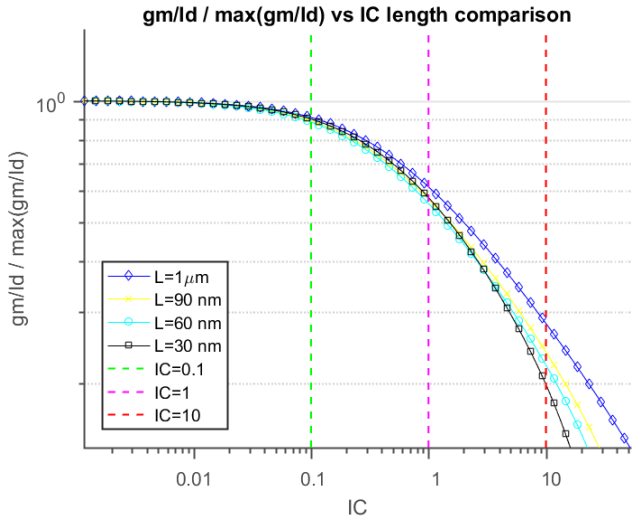

Figure 29 - Normalized transconductance efficiency vs. inversion coefficient for different channel lengths. The measurements correspond to RF DUTs having an aspect ratio of 10 and different lengths (1 µm, 90 nm, 60 nm and 30 nm), at V_{dd} = 1 V. We can observe how the transconductance efficiency for a short-channel device degrades much faster in SI compared to a long-channel device, due to the velocity saturation effect.

3.3.2. Transconductance

Basically, the transconductance (gm) is a measure of the ratio of the change in drain current to the change in gate voltage. Figure 30 shows the transconductance in terms of inversion coefficient for various channel lengths devices (90 nm, 60 nm and 30nm) with an aspect ratio of 10.

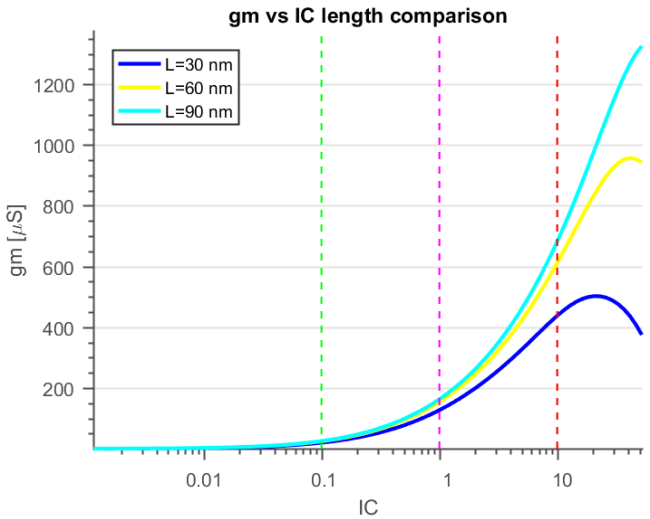

Figure 30 - Transconductance vs. inversion coefficient for different channel lengths. The measurements correspond to RF DUTs having an aspect ratio of 10 and different lengths (90 nm, 60 nm and 30 nm), at V_{dd} = 1 V. We can observe how gm increases along with the channel length and IC.

As long as the velocity saturation (VS) effect increases the gm reduces, so higher gm are achieved with longer channels. When current density increases, for a fixed aspect ratio, the current increases, and for large bias current, the voltage drop across the series source resistance cause the transistor to enter the triode region [106]; hence, gm drops.

3.3.3. Output conductance

The output conductance (gds) is desired to be low in analog design because it is directly related to the intrinsic voltage gain of the transistor with equation (3.2) [68]:

$$Av = \frac{gm}{gds} \tag{3.2}$$

gds increases as the inversion coefficient increases, but as long as the channel is short enough to suffer from DIBL effect, it increases more rapidly as the device goes into stronger inversion regions. For longer channel lengths, the CLM becomes less significant [68], which turns in less gds for longer channels. These facts explain Figure 31 where the output conductance in terms of inversion coefficient for various channel lengths devices (90 nm, 60 nm and 30nm) with an aspect ratio of 10 are shown. We can observe how for shorter channels, where the SCE have a strong impact, the gds increases faster as the devices enters stronger inversions regions.

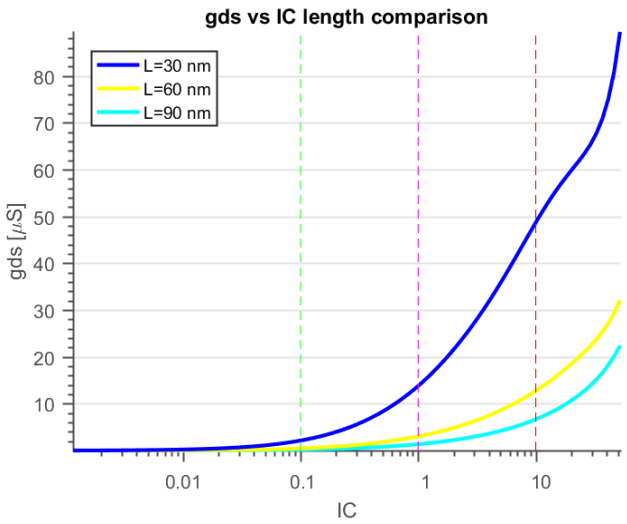

Figure 31 - Output conductance vs. inversion coefficient for different channel lengths. The measurements correspond to RF DUTs having an aspect ratio of 10 and different lengths (90 nm, 60 nm and 30 nm), at Vdd = 1 V.

3.3.4. Effective gate-source voltage

The effective gate-source voltage (V_{GSeff}) is the voltage that falls across the gate-source terminal (V_{GS}) minus the V_{th} and tells how much the V_{GS} is above (in case on NMOS) the MOS V_{th}. Figure 32 shows the V_{GSeff} in terms of inversion coefficient for various channel lengths devices (90 nm, 60 nm and 30nm) with an aspect ratio of 10.

V_{GSeff} increases as the inversion coefficient increases, in WI it is increased logarithmically with IC, then it is increased modestly in MI and finally it is increased as the square root of IC in SI [68]. Short-channel transistors suffer from VS which makes a higher increment than long-channel devices which also increments due to VFMR effect. So, for high inversions

degree the increment is higher for narrower devices. The fact that for 30 nm gate length the values for higher density currents are no longer valid since Vgate are higher than Vdd should be noted.

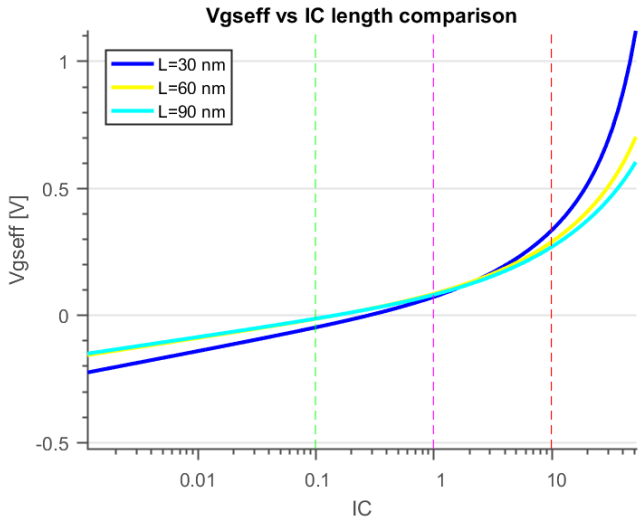

Figure 32 - Effective gate-source voltage vs. inversion coefficient for different channel lengths. The measurements correspond to RF DUTs having an aspect ratio of 10 and different lengths (90 nm, 60 nm and 30 nm), at Vdd = 1 V.

3.3.5. Drain-source saturation voltage

The drain-source saturation voltage (V_{DSsat}) is the minimum voltage at which the MOS transistor enters the saturation regime, which is important to keep it low for ULV designs. For long channel devices it is equal to the V_{GSeff}, but for short channel devices it can be approximated by equation (3.3) [68]:

$$V_{DSsat} \approx \begin{matrix} 4U_T \ in \ WI \\ V_{GSeff}/n \ \ in \ SI \end{matrix} \qquad (3.3)$$

Figure 33 shows V_{DSsat} in terms of inversion coefficient for various channel lengths devices (90 nm, 60 nm and 30nm) with an aspect ratio of 10. For low inversion regimes the V_{DSsat} is unchanged confirming the dependence in WI of equation (3.3), and it increases for higher inversion regimes. With the dependence in SI of recalling the V_{GSeff} graph, and since the substrate factors are comparable (similar gate lengths), we can see the high increment trend of V_{DSsat} for high IC at the shortest length.

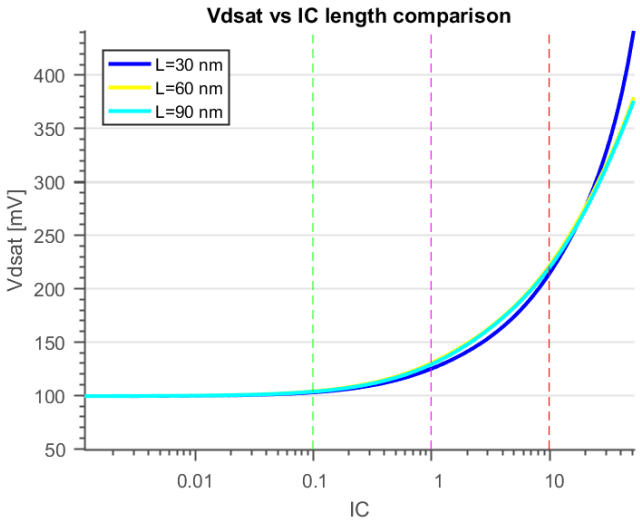

Figure 33 - Drain-source saturation voltage vs. inversion coefficient for different channel lengths. The measurements correspond to RF DUTs having an aspect ratio of 10 and different lengths (90 nm, 60 nm and 30 nm), at Vdd = 1 V.

3.3.6. Threshold voltage

One of the SCE is the threshold voltage roll-off, which varies the threshold voltage of the devices. One of the critical device parameter that defines this variation is the gate length since it is inversely proportional to it. Figure 34 shows the threshold voltage (V_{th}) in terms of inversion coefficient for various channel lengths devices (90 nm, 60 nm and 30nm) with an aspect ratio of 10. We can observe how the threshold voltages is reduced for shorter channel lengths but is invariant with IC. The DIBL also affects this threshold variation reducing the difference as the drain voltage increases. Therefore, this difference between threshold voltages of different channel length devices will be exacerbated with higher values of Vds.

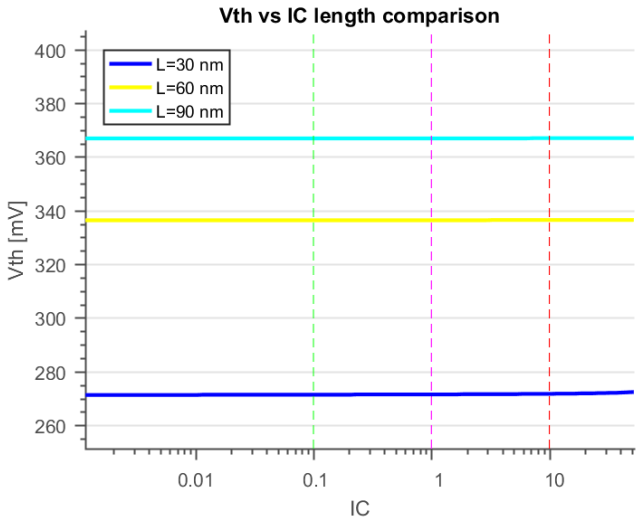

Figure 34 - Threshold voltage vs. inversion coefficient for different channel lengths. The measurements correspond to RF DUTs having an aspect ratio of 10 and different lengths (90 nm, 60 nm and 30 nm), at Vdd = 1 V.

3.3.7. Intrinsic voltage gain

MOS intrinsic voltage gain, represents the maximum voltage gain achievable for a single device, and is a quality factor related to low-frequency voltage gain. Figure 35 shows the intrinsic voltage gain (gm/gds) in terms of inversion coefficient for various channel lengths

devices (90 nm, 60 nm and 30nm) with an aspect ratio of 10. As equation (3.2) shows, it is the ratio between the transconductance and the output conductance. At higher inversion regimes it decays since the gds increases and the gm decreases. Shorter channel transistors are affected by the VS effect and DIBL, the DIBL increments gds and VS reduces the transconductance, hence they have lower gain than longer channel ones.

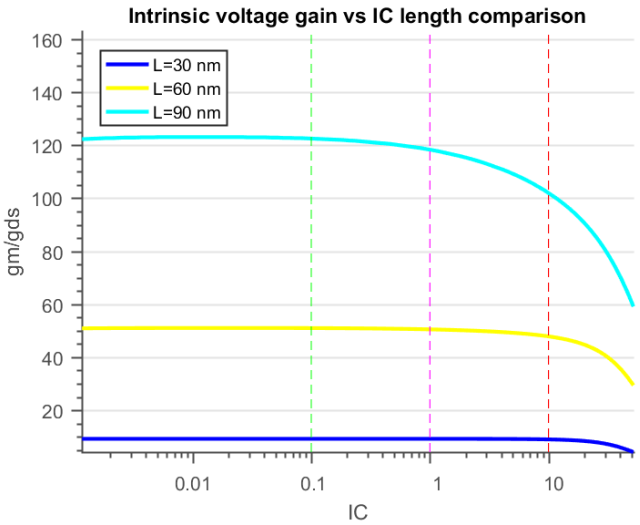

Figure 35 - Intrinsic voltage gain vs. Inversion coefficient for different channel lengths. The measurements correspond to RF DUTs having an aspect ratio of 10 and different lengths (90 nm, 60 nm and 30 nm), at Vdd = 1 V.

3.3.8. Gate capacitances

Figure 36 shows the parasitic gate capacitances (C_{gg}) in terms of inversion coefficient for various channel lengths devices (90 nm, 60 nm and 30nm) with an aspect ratio of 10. As expected, they increase as the gate length increases since it implies bigger area. This total C_{gg} includes the extrinsic and intrinsic capacitances, and for narrower devices (Lg<45 nm) the extrinsic capacitances dominate over the intrinsic ones, so the total measured C_{gg} does not keep the proportional ratio to the gate length as it would do for larger channel transistors [103,107].

On the other hand, the thin isolation film on the bulk diminishes a lot the gate-to-bulk capacitance (C_{gb}) making it negligible, so at low inversions regimes the contributors will be the gate-to-source capacitance (C_{gs}) and the gate-to-drain capacitance (C_{gd}), and for higher inversion regions the maximum contributor will be C_{gs}. Hence, as long as the inversion coefficient increases the C_{gs} starts to grow until is comparable with the Cox, so the total parasitic gate capacitances increases as the device enters to higher inversion regions.

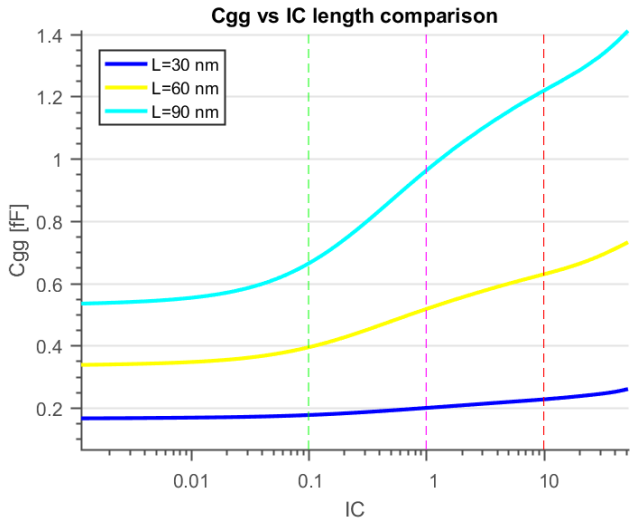

Figure 36 - Gate capacitances vs. Inversion coefficient for different channel lengths. The measurements correspond to RF DUTs having an aspect ratio of 10 and different lengths (90 nm, 60 nm and 30 nm), at Vdd = 1 V.

3.3.9. Transition frequency

The transition frequency (f_T) is a figure of merit defined as the frequency where gate-to-drain current gain (h_{21}) is unity for a CS amplifier. Figure 37 shows f_T in terms of inversion coefficient for various channel lengths devices (90 nm, 60 nm and 30nm) with an aspect ratio of 10. It increases as the device gets to higher inversion regions but for shorter channel lengths, as explained before, for high bias currents the transistor enters the triode region. So a decrement in gm and an increment in parasitic capacitances result in a drop of f_T. Longer channels have higher total parasitic capacitances, which turns out in lower frequencies. Although the f_T increases with Lg scaling, it does not increases as strong as it theoretically should [107].

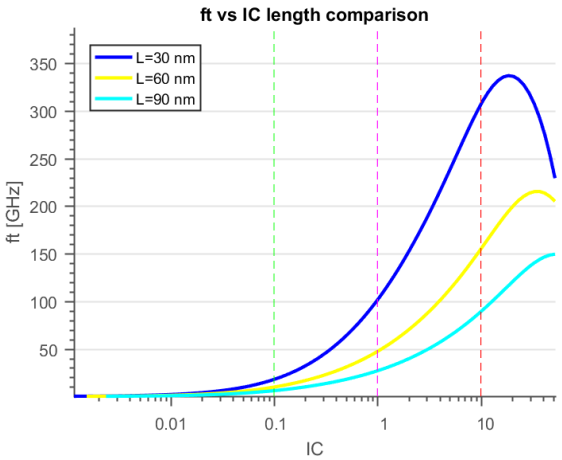

Figure 37 - Transition frequency vs. Inversion coefficient for different channel lengths. The measurements correspond to RF DUTs having an aspect ratio of 10 and different lengths (90 nm, 60 nm and 30 nm), at Vdd = 1 V.

3.3.10. Low power RF FoM

Gm/Id and f_T are very important FoMs from an analog/RF design point of view. One characterizes the DC performance of a device while the other one characterizes its high-frequency behavior. The way to have the trade-off between both metrics is with the product of them defining the FoM for low power RF as equation (3.4) [106].

$$FoM_{RFLP} = \frac{gm}{id} f_T \tag{3.4}$$

Figure 38 shows the FoM_{RFLP} in terms of inversion coefficient for various channel lengths devices (90 nm, 60 nm and 30nm) with an aspect ratio of 10. We can observe how this FoM is maximized in the moderate inversion region. From this graph we can extract that for low power RF optimization it is better to move toward shorter gate lengths since they can reach the desired operating frequency for lower inversion coefficients which are more energy efficient.

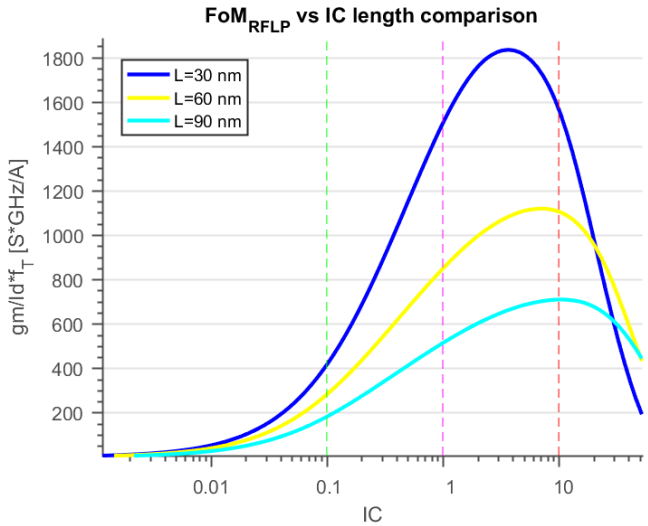

Figure 38 - FoMRFLP vs. Inversion coefficient for different channel lengths. The measurements correspond to RF DUTs having an aspect ratio of 10 and different lengths (90 nm, 60 nm and 30 nm), at Vdd = 1 V.

3.3.11. Noise

Figure 39 shows the noise current density in terms of inversion coefficient for various channel lengths devices (90 nm, 60 nm and 30nm) with an aspect ratio of 10.

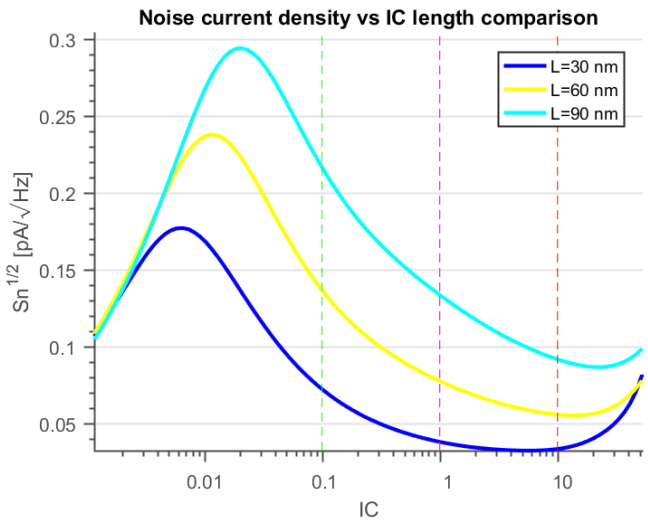

Figure 39 - Noise current density vs. Inversion coefficient for different channel lengths. The measurements correspond to RF DUTs having an aspect ratio of 10 and different lengths (90 nm, 60 nm and 30 nm), at Vdd = 1 V.

The noise decreases as the inversion coefficient increase from WI inversion to SI, maybe because the drain-referred thermal noise dominates in this region, and its decrease is due to the transconductance reduction. After entering the SI region starts to increase. Noise increases with the increment in gate length. The best region to work for the shortest length is MI region.

3.4. Passive devices performance – Inductors at 2.4 GHz

The impedance of an inductance ideally should be purely imaginary with no losses of energy. However, in reality they present some resistance due to the metal wire forming the coils, which can be modeled as a series resistance to the ideal inductance. So, the impedance of an inductor taking into account a series resistance is expressed in equation (3.5).

$$Z_L = R_S + j2\pi fL \tag{3.5}$$

The quality factor (Q) of an inductance, which is a metric of its efficiency, can be expressed as the ratio of its inductive reactance to its series resistance at a given frequency as equation (3.6) shows.

$$Q = \frac{imag(Z_L)}{real(Z_L)} = \frac{2\pi fL}{R_S} \tag{3.6}$$

So in terms of Z parameters with a single ended configuration the equation would be (3.7).

$$Q = \frac{imag(Z_{11})}{real(Z_{11})} \tag{3.7}$$

This method has been performed extracting the one-port Z-parameter measurements with one terminal of the inductor grounded [108] as show in Figure 40, then the input impedance is equivalent to Z_{11}.It consists of an inductor and an input port to obtain the S-parameters. These integrated planar inductors characterized have a width coil of 11 μm, and the diameter and length depends on the inductance which are auto calculated during the simulations when the inductance value is swept. They also are characterized in function of the number of turns of the coil, which in this model can range from 2 to 6 turns.

Figure 41 shows the quality factor (Q) of the inductors provided on the design kit. The final design is a LNA working on the 2.4 GHz ISM band so they have only been characterized

at this frequency and the inductors values swept has been defined before they present a self-resonant behavior.

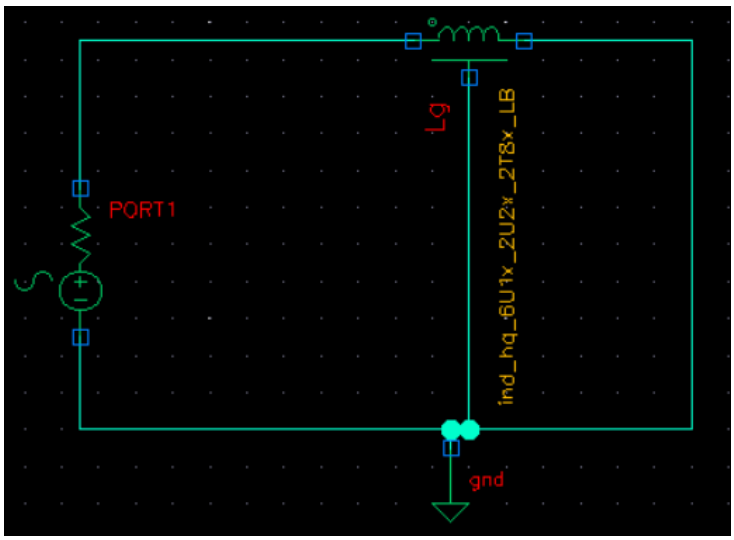

Figure 40 - Test circuit for inductance characteristics

Their maximum quality factor in this case can reach 30, and depending on the value of the inductor is better to increase the number of turns represented in the figure as n. In terms of Q, for lower values of inductance is better to use low number of turns, and for higher values of inductance, even though have lower maximum Q, is better to use more turns per inductance as can be seen on the figure.

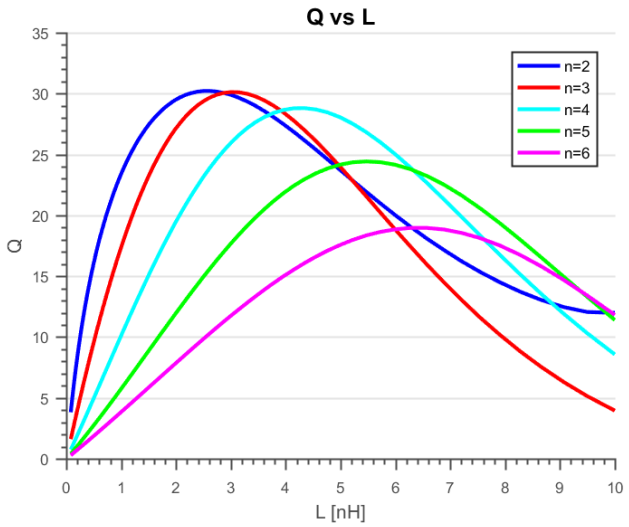

Figure 41 - Quality factor vs. Inductor values for various number of turns of the inductor. The measurements have been performed with the same model of the inductor but for the different number of turns (n) that the design kit allows, from 2 to 6 turns.

3.5. Back gate Bias effect

The schematic used to obtain this characteristics is the same as the one on Figure 21. All the simulations have been performed in saturation (V_{ds}= 1 v) for a LVT NMOS transistor with a gate length of 30 nm and an aspect ratio of 10. The range of the back-gate voltage (V_{bulk}) goes from 0 V to 2 V with a resolution of 0.5 V.

Figure 42 shows the measured transfer characteristics and as expected the higher the back-gate voltage becomes the higher the drain current gets. The maximum drain-source current varies from 279.2 µA to 368.6 µA which is a 32 % increment.

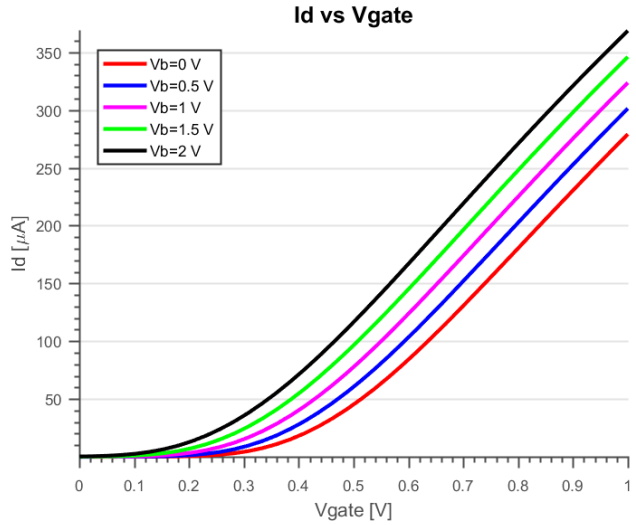

Figure 42 - Transfer characteristics of LVT NMOS with a 30 nm gate length and aspect ratio of 10 as a function of gate-source voltage and back-gate voltage (0 V to 2V) at Vds=1V.

The corresponding transconductance is shown in Figure 43. The first apparent thing is that the maximum gm is higher for higher back bias voltage. Another fact is that the peak is shifted to lower gate voltages as the V_{bs} is increased. The peak for V_{gs} = 2 V is approximately at V_{gate} = 650 mV and for V_{gs} = 0 V is approximately at V_{gate} = 800 mV, so the peak can be tuned by 150 mV.

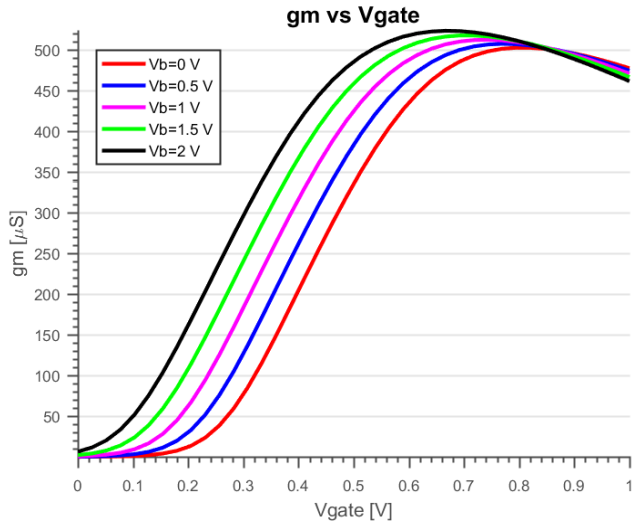

Figure 43 - transconductance of LVT NMOS with a 30 nm gate length and aspect ratio of 10 as a function of gate-source voltage and back-gate voltage (0 V to 2V) at Vds=1V.

The output conductance is shown in Figure 44. As explained before, in short-channel devices, the gds rapidly increases due to the SCE for high inversion levels, so as the back-gate becomes strongly inverted the gds is increased.

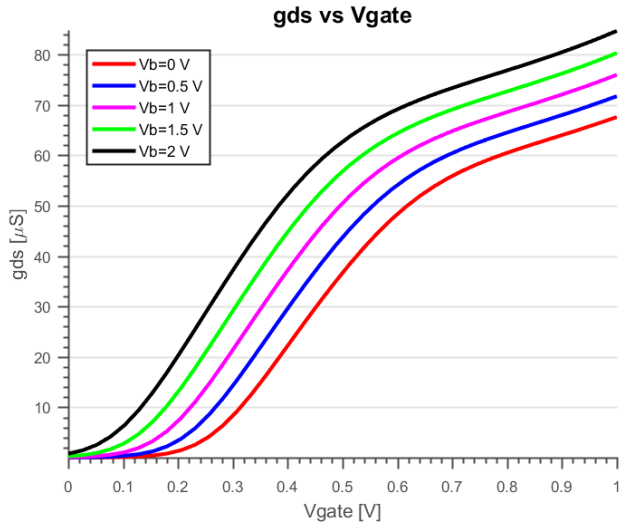

Figure 44 - Output conductance of a LVT NMOS with a 30 nm gate length and aspect ratio of 10 as a function of gate-source voltage and back-gate voltage (0 V to 2V) at Vds=1V.

The transit frequency is shown in Figure 45. The back bias affects it the same as it does with gm. The maximum f_T is higher for higher V_{bs}. The peak is also shifted to lower gate voltages as the V_{bs} is increased. The peak for V_{bs} = 2 V is approximately at V_{gate} = 600 mV and for V_{bs} = 0 V is approximately at V_{gate} = 750 mV, so the peak can also be tuned by 150 mV.

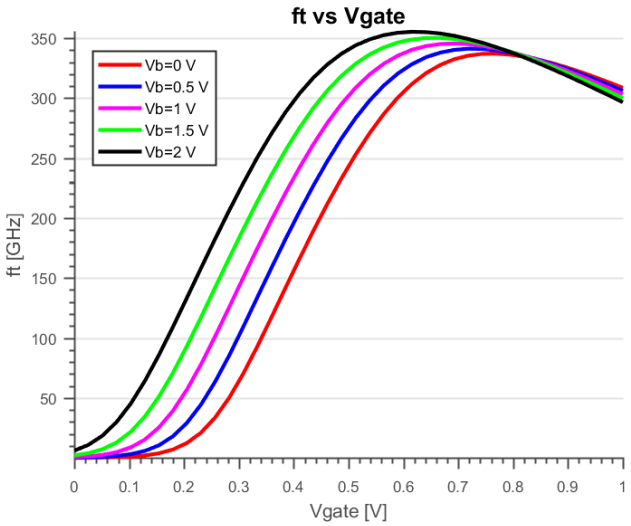

Figure 45 - Transit frequency of a LVT NMOS with a 30 nm gate length and aspect ratio of 10 as a function of gate-source voltage and back-gate voltage (0 V to 2V) at Vds=1V.

Figure 46 shows the intrinsic gain of the transistor. Proportionally, gds increases more with V_{bs} than gm, so as the back-gate voltage increases the intrinsic gain decreases.

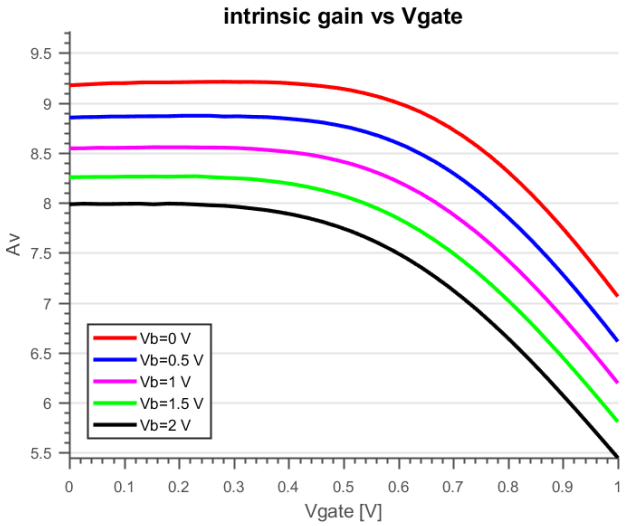

Figure 46 - Intrinsic gain of a LVT NMOS with a 30 nm gate length and aspect ratio of 10 as a function of gate-source voltage and back-gate voltage (0 V to 2V) at Vds=1V.

Figure 47 shows the transconductance efficiency of the transistor. The more strong inverted the back-gate is the lower the efficiency gets. It is normal since, as explained before, the maximum efficiency is obtained in WI regimes.

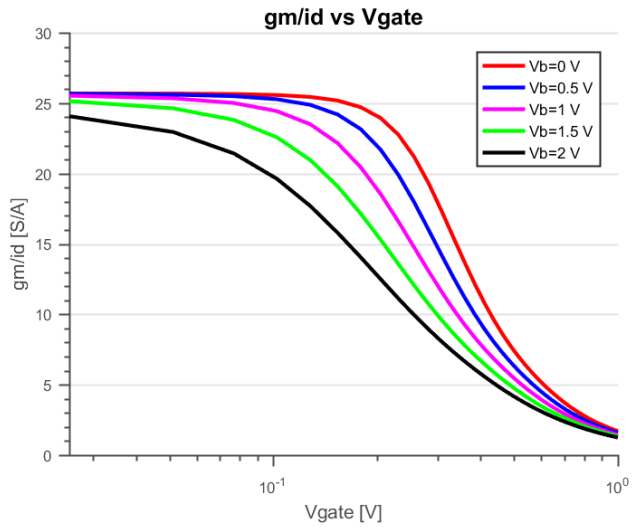

Figure 47 - Transconductance efficiency of a LVT NMOS with a 30 nm gate length and aspect ratio of 10 as a function of gate-source voltage and back-gate voltage (0 V to 2V) at Vds=1V.

Figure 48 shows the low power RF FoM. The peak is maintained approximately constant since the fall of transconductance efficiency is compensated with the increment in f_T. Moreover, the peak for V_{bs} = 0 V is 1.83 GHz/mV at V_{gs} = 460 mV and for V_{bs} = 2 V is 1.85 GHz/mV at V_{gs} = 300 mV, so it can be tuned for about 160 mV.

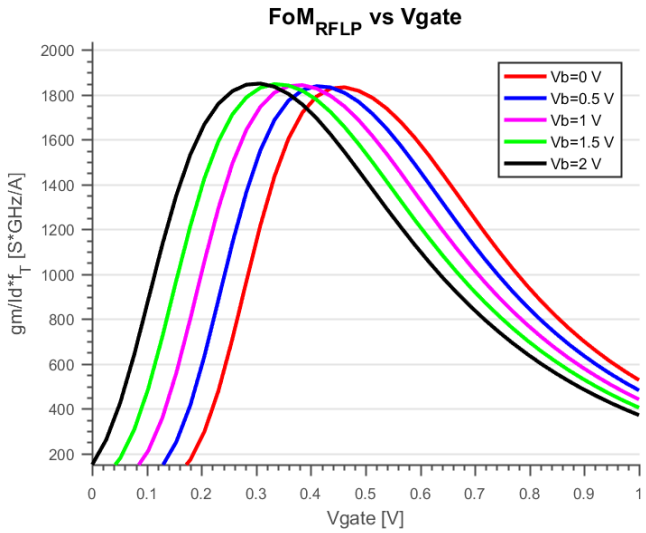

Figure 48 - Low power RF FoM of a LVT NMOS with a 30 nm gate length and aspect ratio of 10 as a function of gate-source voltage and back-gate voltage (0 V to 2V) at V_{ds} =1V.

Finally, Figure 49 shows the noise current density. The measured noise current density gets higher as the back-gate voltage increases, which may be caused by the increment in drain current that affects directly to the drain-referred noise.

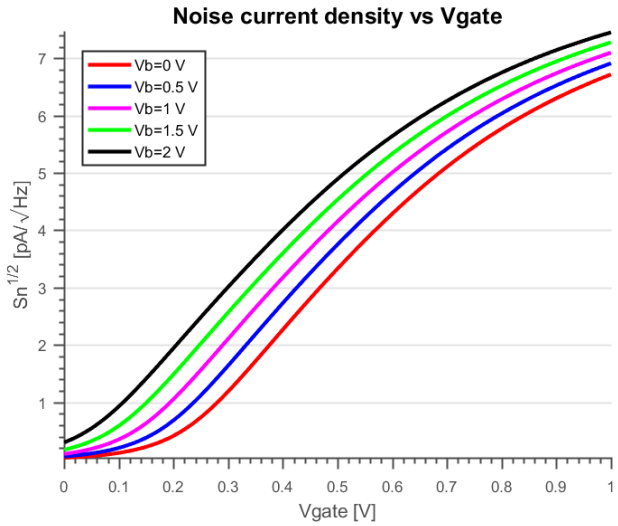

Figure 49 - Noise current density at 2.4 GHz of a LVT NMOS with a 30 nm gate length and aspect ratio of 10 as a function of gate-source voltage and back-gate voltage (0 V to 2V) at Vds =1V.

4. LNA design

This section describes the procedure to obtain the specifications of an LNA for a low power application. First the RF specifications for a certain standard are reviewed, then the specification for a receiver fully compliant with the standard are calculated. Finally, the LNA requirements are extracted from the receiver chain specifications.

4.1. Specifications

An LNA will be designed to validate the advantages of this technology for ULV and ULP applications that may fit the IoT devices requirements. One standard that can fit on the IoT paradigm is the IEEE 802.15.4, which is a LR-WPAN standard optimized for low data rate and low power applications used for building autonomous, low-power devices that may be battery powered and require the ability to go to sleep mode or shut down. This standard was designed to operate in unlicensed RF bands, which are shown in Table 8.

RF band	Frequency range	Data rate	Channel number(s)	Geographical area
868 MHz	868.3 MHz	20 Kbps	0 (1 channel)	Europe
915 MHz	902 – 928 MHz	40 Kbps	1-10 (10 channels)	America, Australia
2400 MHz	2400 – 2483.5 MHz	250 Kbps	11-26 (16 channels)	Worldwide

Table 8 - IEEE 802.15.4 RF bands [109]

Although the 868 MHz and 915 MHz bands offer certain advantages such as fewer users, less interference, and less absorption and reflection, the 2400 MHz band is more widely adopted for various reasons:

- Worldwide availability for unlicensed use.
- Higher data rate and more channels.
- Transmitter and receiver are on for a shorter time due to higher data rates resulting in lower power consumption.
- RF band more commonly used and accepted by the market place (Bluetooth and the IEEE 802.11 standard also uses this band).

Therefore, the specifications to achieve on the design are extracted from this standard at the 2.4 GHz band, which are shown on Table 9.

Parameter	IEEE 802.15.4 for PHY 2400 MHz band
Frequency band	2400-2483.5 MHz
Channel Bandwidth	2 MHz
Channel spacing	5 MHz
Modulation	Offset Quadrature Phase Shift Keying (O-QPSK)
Bit Rate	250 Kbits/s
PER (packet error rate)	<1%
Receiver Sensitivity	-85 dBm
Max. Receiver Input	-20 dBm
Adjacent channel rejection	0 dB
Alternate channel rejection	30 dB

Table 9 - IEEE 802.15.4 RF specifications [109]

4.1.1. NF specification

The base specifications for the front-end RF receiver are modified to work not on the edge of operation conditions. The targeted sensitivity, which is defined as the minimum level of the input signal that is able to receive and decode successfully with a given error rate, will be 3 dB lower than the required one as a design margin, as shown in equation (4.1).

$$S_{i\_min} = -85\ dBm - 3\ dB = -88\ dBm \tag{4.1}$$

The first performance parameter for the receiver is the overall NF, which is given by equation (4.2) where k is the Boltzmann's constant (1.38 * 10^{-23} J/K), T is the absolute temperature (298 K), BW is the effective noise bandwidth and SNR_{o_min} is the minimum signal to noise ratio to successfully demodulate the signal referred at the output.

$$NF = S_{i\_min} - 10\log(kT) - 10\log(BW) - SNR_{o\_min} \tag{4.2}$$

Then SNR_{o_min} is defined by equation (4.3) where Eb/No is the energy bit to the noise density ratio and Rb is the data rate.

$$SNR_{o\_min} = 10 * log_{10}\left(\frac{Eb}{No} * \frac{Rb}{BW}\right) \tag{4.3}$$

Equation (4.4) relates the Packet Error Rate (PER) with the Bit Error Rate (BER). Given that, for a PER of 1 % with a frame of 32 digits the obtained BER is 0.03%. As we use a

QPSK modulation, the theoretical curve from Figure 50, which relates Eb/No with BER, gives an Eb/No of approximately 7.7 dB.

$$PER = 1 - (1 - BER)^N \tag{4.4}$$

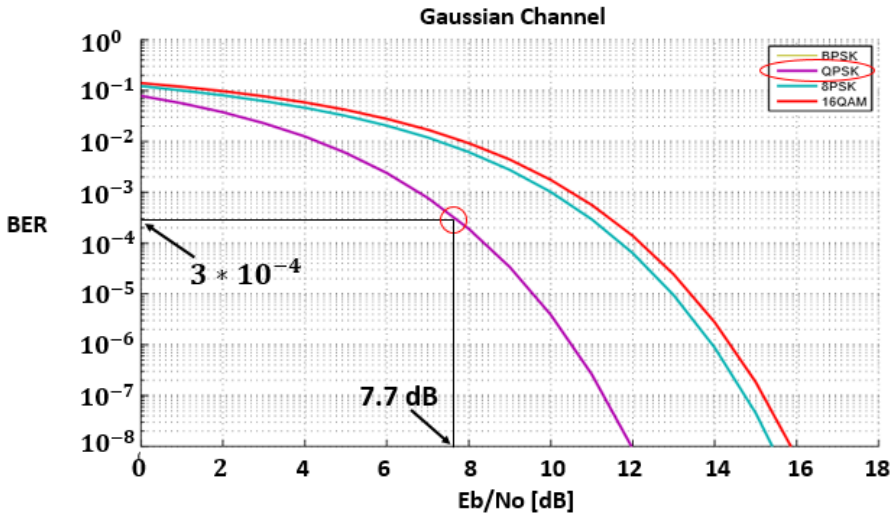

Figure 50 - BER over AWGN channel for BPSK, QPSK, 8PSK and 16QAM [110]

This Eb/No entails that for a data rate of 250 Kbps, a minimum SNR at the output (SNR_{o_min}), which is expressed in equation (4.5), of -1.33 dB is needed. Adding to the overall NF another 2 dB of margin to account for the dependency between non idealities, its maximum possible value is defined in equation (4.6).

$$SNR_{o\_min} = 10 * log_{10}\left(\frac{Eb}{No} * \frac{Rb}{BW}\right) = 7.7 + 10 * log_{10}\left(\frac{250e3}{2e6}\right) = -1.33\ dB \tag{4.5}$$

$$NF = -88\ dBm + 174\ dBm - 10 * log_{10}(2e6)\ dB - (-1.33\ dB) - 2\ dB = \mathbf{22.32\ dB} \tag{4.6}$$

4.1.2. Gain specification

The signal at the input is amplified by the gain chain and needs to fulfill the requirements of the demodulator, and since it is difficult to use power terms due to the saturated waveforms and unknown node resistances, the dynamic range will be determined by the voltage swing at the input of the demodulator. The minimum and maximum rms voltage at the receiver input are defined in equations (4.7) and (4.8):

$$V_{i\_min} = \sqrt{R_s * 10^{S_{i\_min}/10}} = 8.9\ \mu V \tag{4.7}$$

$$V_{i\_max} = \sqrt{R_s * 10^{S_{i\_max}/10}} = 31.6\ mV \quad (4.8)$$

Since the target is a low power receiver, the supply voltage for the design is initially 1 V (nominal VDD voltage in the FDSOI 28nm technology). The chain gain will be calculated under the assumption of a demodulator with 10-bits Analog to Digital Converter (ADC) supplied by the 1 V. Since it is a 10 bit converter, it has a resolution of 1023 (2^N-1), thus the minimum input rms voltage is 691.2 µV (least significant bit voltage). The maximum input voltage is the full scale reference ($1V_p$ – 0.707 V_{rms}). So the maximum and minimum chain gain are defined in equations (4.9) and (4.10).

$$G_{max} = 20\log\left(\frac{V_{LSB}}{V_{i\_min}}\right) = 20\log\left(\frac{691.2\ \mu V}{8.9\ \mu V}\right) = 37.8\ dB \quad (4.9)$$

$$G_{min} = 20\log\left(\frac{V_{fs}}{V_{i\_max}}\right) = 20\log\left(\frac{0.707\ V}{31.6\ mV}\right) = 27\ dB \quad (4.10)$$

4.1.3. IIP3 specification

This standard has not specified a two tone test to measure IIP3. It identifies two different interferers, only one at a time.

- The first adjacent channel interferer, with the same power level as the signal power at 5 MHz away from the signal.
- The alternate channel interferer, with a 30 dB power level higher than the signal power at 10 MHz away from the signal.

If a two tone test is defined where there are two interferers at the same time, an in band IM3 results defined in equation (4.11). The desired signal power level is -85 dBm and the addition of -3 accounts for the fact that IIP3 should be measured with the desired signal 3 dB above the sensitivity level.

$$IIM3 = S_i - SNR_{o\_min} - 3 = -85 - (-1.33) - 3 = -86.67\ dBm \quad (4.11)$$

Since the two interferes are not of the same power level, simple IIP3 equation is not holding anymore. The alternative equation (4.12) can be derived, where the worst case is assumed with the two interferers with the same power level. P_{int} is 30 dB higher than the input signal (-55 dBm).

$$IIP3 = S_i + \frac{P_{int} - IIM3}{2} = -85 + \frac{-55 + 86.67}{2} = -69.165\ dBm \quad (4.12)$$

4.1.4. Receiver specifications

Table 10 holds the summary of the receiver requirements to be fully compliant with IEEE 802.15.4 in the 2400 MHz band.

Parameter	Value
V_{dd}	1 V
Gains	27/37.8 dB
NF	< 22.32dB
IIP3	> -69.165 dBm

Table 10 - Receiver specifications

4.1.5. LNA specifications

The most suitable architecture to provide a trade off in power and performance is a typical low-IF receiver [111] which can be seen in Figure 51. The RF signal is mixed down to a non-zero low or moderate frequency, typically a few megahertz for IEEE 802.15.4 in the 2400 MHz band signals. The previous stage of the ADC is a Variable Gain Amplifier (VGA) to adapt the signals to the dynamic range of the ADC.

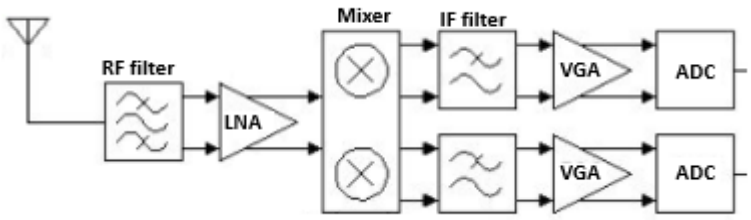

Figure 51 - low-IF topology [112]

This topologies have the properties of zero-IF architectures, but avoid some of their problems such as, the dc offset and 1/f-noise. However, it suffers from other problems like the image frequency issue. Fortunately, a carefully designed receiver can overcome this problems in this standard, due to the relaxed image and neighboring channel rejection requirements [113].

The software SysCalc has been used to specify the block level specifications. The distribution of the parameters over the whole receiver chain is shown in Figure 52 and the LNA specifications on Table 11.

Figure 52 - Level plan for the low-IF receiver

Parameter	Value
V_{dd}	1 V
Gain	15 dB
NF	10 dB
IIP3	-30 dBm

Table 11 – LNA design specifications

Even though the specifications defines the voltage gain, the parameter S_{21} (forward transmission coefficient) is going to be used instead. The voltage gain can be expressed as equation (4.13), where V_o is the output voltage, V_i the input voltage, R_{out} the output resistance and R_{in} the input resistance. When the input and output resistance are the same, the voltage gain is exactly to $S_{21} = G_T$.

$$G_T = 10\log\left(\frac{\left(\frac{Vo^2}{Rout}\right)}{\left(\frac{Vi^2}{Rin}\right)}\right) = 20\log\left(\frac{Vo}{Vi}\right) + 10\log\left(\frac{Rin}{Rout}\right) = G_v + 10\log\left(\frac{Rin}{Rout}\right) \quad (4.13)$$

4.2. LNA design methodology

This section contains the procedure used to design the LNA with the specifications previously obtained. Design techniques for ULP LNAs can either based on specific circuit topologies (current-reuse, inductor feedback...) or on optimizing the performance of transistors in a given technology.

Since the design is only to check the suitability of the 28 nm UTTB FDSOI technology for ULV and ULP RF blocks, the chosen topology is a simple inductively degenerated CS shown in Figure 53.

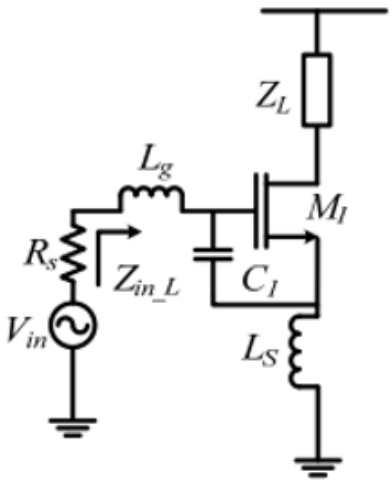

Figure 53 - Inductive source-degeneration CSLNA [115]

It uses inductive source degeneration to match the input impedance to 50 Ω at the operating frequency. This topology is the dominating for narrowband systems due to its advantages providing a low NF, ease of input matching, moderate-high gain and low-power consumption. It has some disadvantages such as a difficult simultaneous matching for optimum power transfer and minimum noise [114]. The use of only one transistor allows a high reduction of the supply voltage (ULV) while keeping it in saturation reducing the overall power consumption. C1 is added in parallel to C_{gs1} in order to achieve a lower NF and is helpful to the impedance input matching network. It introduces another freedom degree besides L_s, L_g and the transistor itself. Z_L is formed by a LC-tank, which resonates on the operating frequency, increasing the impedance, hence providing higher gain.

The gm/Id design approach helps to reduce power consumption for a given set of specifications, which basically are NF and gain in the case of the LNA. The basic idea is to bias the transistor to fulfill the specifications without an unnecessary exceeded performance which implies a waste of power. Then, it is expected that biasing the transistor in MI region a good trade-off between current efficiency and speed performance could be obtained.

4.2.1. LNA design for 1 V

First of all, we need to ensure that the transistor can work as an amplifier at the operating frequency needed, the 2400 MHz ISM band. In this topology the NF and gain are related with the f_T therefore it should be determined in accordance with the specifications; however the addition of a parallel capacitance much higher than the gate capacitance makes gain and NF more dependent of this added capacitance than the frequency chosen. This gives more freedom to select the f_T without impacting to the other parameters. A general guideline for matching the technology speed to the system speed requirement is to choose a f_T 10 times greater than the application operating frequency [116]. Hence, the f_T should be higher than 24 GHz and in this thesis it has been decided to work initially with a f_T of 30 GHz.

From the graphs presented in chapter 3, the main parameters of a single finger transistor with L = 30nm and an aspect ratio of 10 when the transistor is biased to achieve the desired cut-off frequency are extracted and summarized in Table 12.

Parameter	value
IC	0.1847
Id [µA]	1.585
V_{gseff} [mV]	-21.4
V_{dsat} [mV]	105.1
gm/Id [S/A]	21.62
gm [µS]	34.27
gds [µS]	3.72
f_T [GHz]	30.06
Cgg [fF]	0.18
gm/gds	9.21
Vth [mV]	271.400

Table 12 - Main parameters of the transistor when f_T is 30 GHz

From the parameters we can observe that the transistor will be biased in the MI region (0.1<IC< 10) and close to the WI bound which means that it will have a good current efficiency. The voltage to apply at the gate to bias the transistor is $V_{gs} = V_{gseff}+V_{th}$ = -21.4 + 271.4 = 250 mV.

The voltage gain of the amplifier has a dependence on the transconductance gain (Gm), the output resistance (rds) and the load. rds can be neglected if the assumption of a load much bigger than rds is taken giving the expression in (4.14), where rds is the output resistance, R_L the load resistance and Gm the transconductance gain. At resonance, Gm of this topology can be expressed as equation (4.15), where R_s is the resistance at the source, L_g is the inductance at the gate, L_s is the inductance at the source, gm the transistor transconductance and ω_o the operating frequency.

$$Av = Gm * (rds||R_L) \xrightarrow[rds \gg R_L]{} Av \approx Gm * R_L \tag{4.14}$$

$$|Gm(j\omega_o)|_{matching} = \frac{\omega_o * (L_g + L_s) * gm}{2 * R_s} \xrightarrow[R_s = 50\,\Omega]{} \approx 10^8 * (L_g + L_s) * gm \tag{4.15}$$

The range of inductor values used is limited from 0.45 nH to 8.6 nH, which are the inductors with a quality factor above 15 at 2.4 GHz extracted from previous simulations in chapter 3. If we assume the restriction that the total inductance of the gate and source is close to 10 nH, from equation (4.15) we can approximate Gm to gm, giving the simple voltage gain expression of (4.16).

$$Av \approx gm * R_L \tag{4.16}$$

An inductance is used as a load to maximize the gain. Inductors can be modeled as a RLC equivalent circuit where its impedance peaks at resonance. The parallel equivalent resistance is showed in equation (4.17) where Q is the quality factor, ω_o the resonant frequency and L is the inductance value.

$$R_p = Q * \omega_o * L \tag{4.17}$$

The NF of the amplifier is negatively impacted by the parasites of the passive components, and since inductors present more problems than capacitor, the design will try to focus on the inductors choice rather than capacitances, so maximum Q inductors will be used when possible. The models of real inductors provided by the library, which have been characterized in chapter 3, are used, so the inductor at the drain is chosen as the inductor with the highest Q, which is 30.22 for an inductor of 2.6 nH with 2 coil turns. Given that, the load resistance is R_L=1.185 KΩ.

The resonance frequency of the parallel RLC tank is defined in equation (4.18) where L_d is the inductance and C_L is the capacitance. With the value of the inductor, the capacitance needed to resonate at the desired frequency is C_L=1.69 pF.

$$\omega_{o\_out} = \frac{1}{\sqrt{L_d C_L}} \tag{4.18}$$

Then, initially considering that rds is much bigger than the load, for a voltage gain of 15 dB (5.623 in linear units) specified on the requirements gives a transconductance of gm=4.75 mS.

The inductors at the source and gate should resonate with the total capacitance in parallel at the gate. The parasitic capacitances of this technology are very low, so as a first approximation, they can be assumed negligible compared with the externally added capacitance C_1 at the gate. Therefore, the resonant frequency at the input is given by equation (4.19) where and C1 is the externally added capacitance.

$$\omega_{o\_in} = \frac{1}{\sqrt{(L_g + L_s) * C_1}} \tag{4.19}$$

At resonance, the input impedance of the transistor is expressed in equation (4.20) where gm is the transistor transconductance and C_{T1} is the total capacitance at the gate (C_1 and C_{gg} of the transistor). The source inductor, as already commented, is used to match the input to a source resistance (50 Ω in this case).

$$Z_{in} = \frac{gm * L_s}{C_{T1}} \tag{4.20}$$

From equations (4.19) and (4.20) the relation between the inductors at the gate and at the source can be expressed as the equation (4.21). This equation is graphically represented in Figure 54. This figure in conjunction with Figure 41 from chapter 3 are helpful to choose their values and have a balanced quality factor.

$$L_s = \frac{-L_g \pm \sqrt{{L_g}^2 - 4\frac{Z_{in}}{\omega_o^2 * gm}}}{2} \tag{4.21}$$

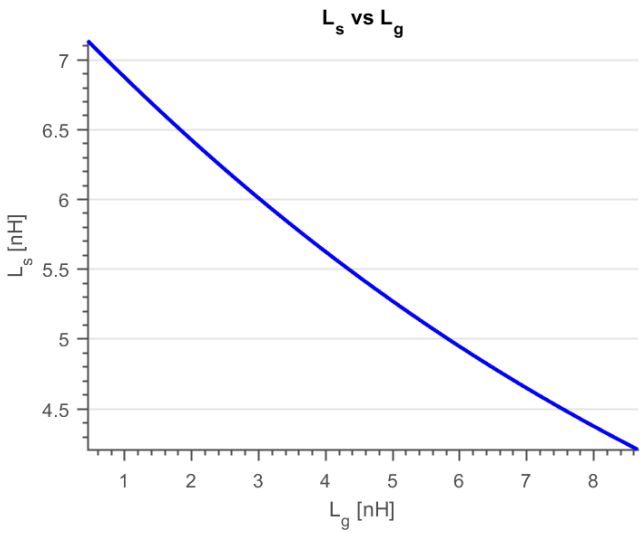

Figure 54 - Source inductor vs. gate inductor

Finally, taking into account previous restrictions, the values of the passive components are:

- L_g = 4.985 nH with Q_g = 28.07
- L_s = 5.276 nH with Q_s = 27.53
- $C_{T1} = C_1 + C_{gg}$ = 501.22 fF

As evident from Table 12, the reference transistor with optimum biasing does not provide the required gm value, so an increment of the width of the transistor is needed. The Id needed to obtain the required gm can be calculated from the gm/Id giving a drain current of 219.7 µA. The sizing of the transistor needs of the previously calculated Ispec of the transistor. The current density can be obtained from equation (2.3) and gives and I_d/W/L=158.51 nA. The length used for this amplifier is 30 nm, so the required total width is 41.6 µm. Since the gate resistance introduces noise to the system, it should be reduced by design. The total gate resistance in inversely proportional to the square of the number of the gate fingers as equation (4.22) shows, where $R_{\blacksquare}$ is sheet resistance of the gate, W_f is gate finger width, n is number of gate fingers and L is gate length. When the number of fingers is high enough, it is common to ignore the effects of the gate resistance. Hence,

sizing the transistor with fingers instead of total width is mandatory. The finger width is decided to be 300 nm, so the number of fingers to achieve the total width is n= 139.

$$R_g = \frac{R_{\blacksquare} * W_f}{3 * n^2 * L} \tag{4.22}$$

The R_{bias} has to be large enough that its equivalent noise current is small enough to be ignored. In a 50 Ω system, values of several hundred Ω to KΩ or so are adequate. It has been decided to use R_{bias} = 5 KΩ.

Once the main parameters are calculated, the simulation of the LNA have been performed to observe the behavior taking into account the parasites. The schematic used to obtain the simulations is the one on Figure 55. Almost all the passive components used (L_d, L_s, L_g, R_{bias}, C_1, C_L) are the ones provided by the STMicroelectronics PDK. The buffer, which isolates the output impedance from the port impedance, has been used to drive the 50 Ω output port so the gain is not modified. S_{11}, S_{21}, NF, IIP3 and P1dB have been extracted with the buffer. The rest of the parameters (S_{12}, S_{22}, Kf and B1f) have been verified without the buffer, connecting the port directly to the output after de decoupling capacitor (C_{out}).

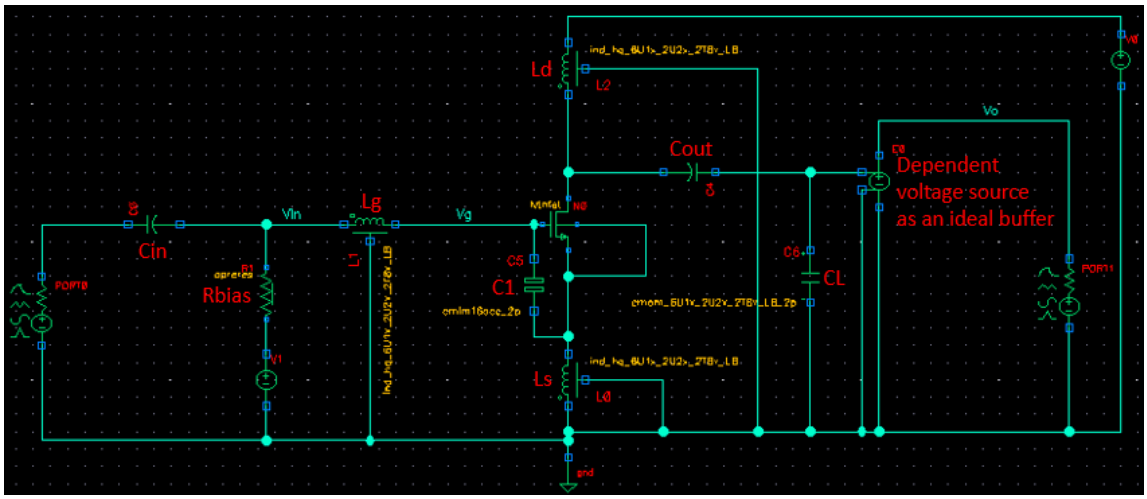

Figure 55 - LNA schematic supplied with 1 V

Finally, the values of the parameters have been tuned to center the resonant frequencies and achieve the specifications. All the parameters of the LNA design, initially calculated and then tuned, are summarized in Table 13.

Figure 56 shows the input reflection coefficient (S_{11}) and the forward gain (S_{21}) parameters over the frequency. On the operating frequency band, S_{11} shows a quite good maximum value of -14.906 dB that implies a good input matching. Parameter S_{21}, which relates the power available from the source and the power delivered to the load, shows values slightly above the required 15 dB of gain.

Parameter	Calculated values	Tuned values
Vdd [V]	1	
L_d [nH]	2.6	2.495
L_g [nH]	4.985	3.8
L_s [nH]	5.276	5.5
C_1 [fF]	501.22	425
C_L [pF]	1.69	1.58
C_{in}/C_{out} [nF]	10	10
R_{bias} [KΩ]	5	5
gm [mS]	4.75	4.3
Id [µA]	219.7	198.926
fingers	139	139

Table 13 - LNA design parameters when supplied with 1 V

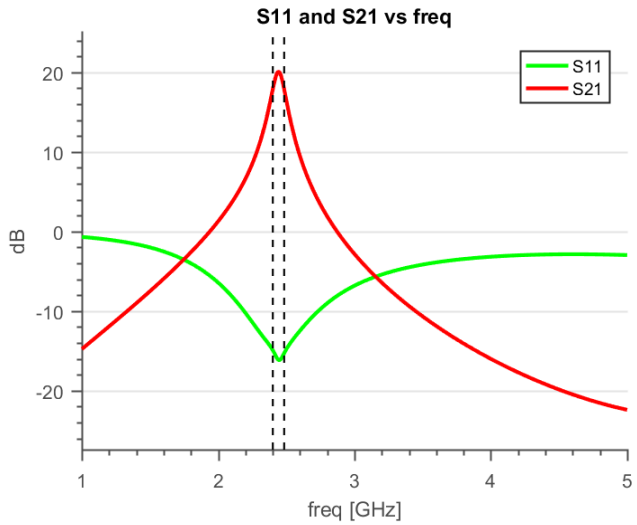

Figure 56 – S_{21} and S_{11} parameters over the frequency for the LNA supplied with 1 V

Figure 57 shows the reverse isolation coefficient (S12) and the output reflection coefficient (S22). S12 have to be low enough to prevent signal leakage from subsequent blocks that might be reradiated by the antenna [117]. Even though an amplifier without cascode transistor has not the best isolation, its value is close to -30 dB, quite a good value. S22 is related with output matching, but since it should be integrated with the mixer, it does not have to be impedance matched, so the bad values of S22 are not representative.

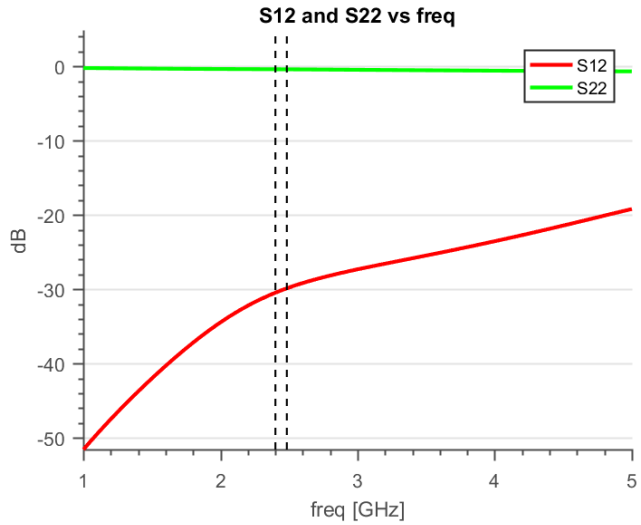

Figure 57 - S_{12} and S_{22} parameters over the frequency for the LNA supplied with 1 V

Figure 58 shows the minimum NF achievable and the actual NF of the LNA. They are close to each other in the band of interest indicating a good matching. The NF is way below the maximum allowed on the specifications, approximately slightly more than 6 dB lower than the specification, verifying the compliance of the LNA with the noise requirements.

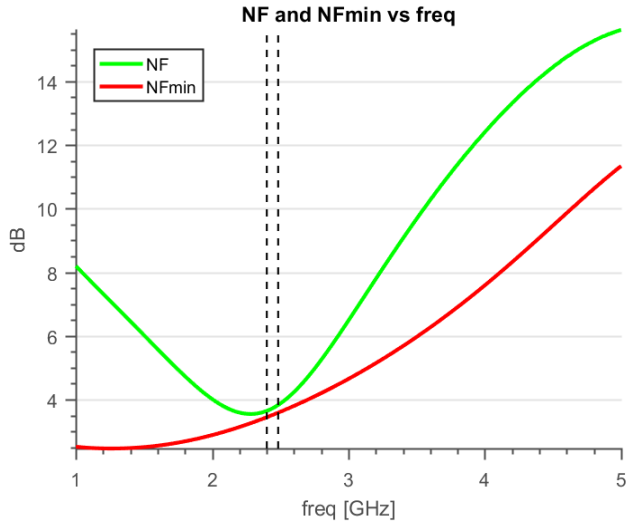

Figure 58 - NF and minimum NF over the frequency for the LNA supplied with 1 V

Figure 59 shows the Rollet stability factor (Kf) and an alternative stability factor (as defined by Spectre simulator, B1f=Delta) verified for the band of interest. A dashed line appears in the figure to indicate visually where the stability boundary is. When Kf > 1 and B1f < 1, the circuit is unconditionally stable. That is, the LNA will remain stable with any combination of source and load impedances. The LNA keeps the stability over the 1 GHz to 5 GHz frequency range as the figure shows.

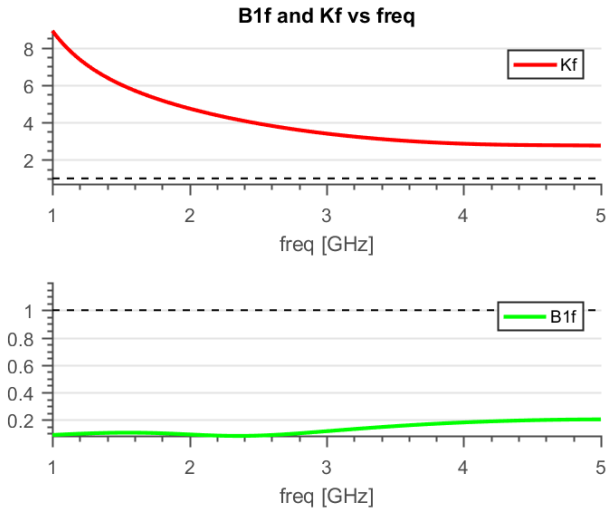

Figure 59 - Stability parameters over the frequency for the LNA supplied with 1 V

Figure 60 shows the 1 dB compression point simulation where a P1dB=-12.1955 dBm is achieved.

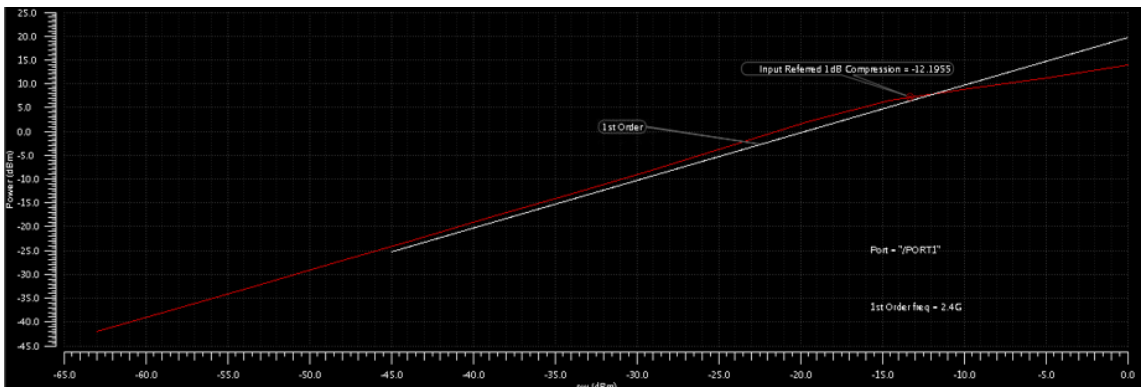

Figure 60 - P1dB of the fundamental tone (2.4 GHz) for the LNA supplied with 1 V

Figure 61 shows the third-order interception point simulation where an IIP3=-7.22802 dBm is achieved. It is well above the IIP3 required for the LNA. The IIP3 was measured using a two-tone test, with the tones spaced 5 MHz apart.

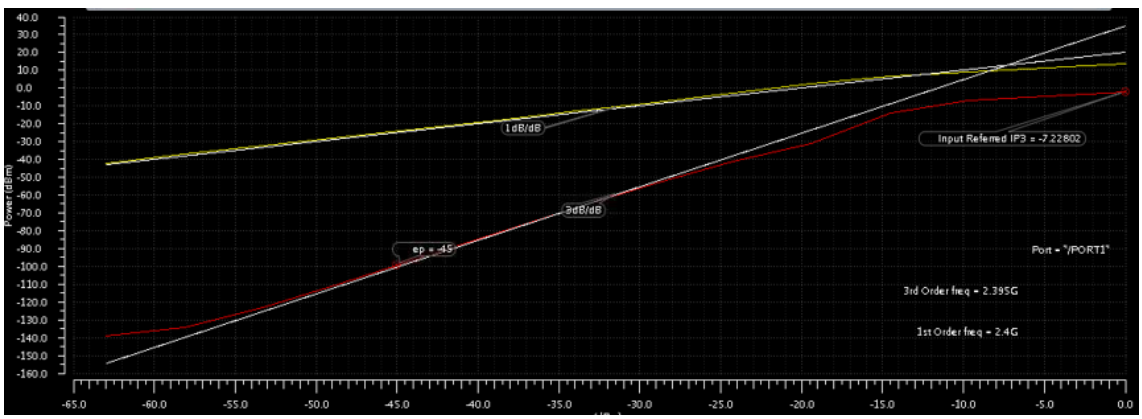

Figure 61 – IIP3 for the test with one tone at fo=2.4GHz and a second tone at f1= 2.405 GHz for the LNA supplied with 1 V

Table 14 shows the values of all the reviewed parameters of the LNA supplied by 1 V at three frequency points of the operating frequency band defined as follows:

- f_{min} – at the beginning of the operating band (2.4 GHz).
- f_{center} – at the center of the operating band (2.44175 GHz).
- f_{max} – at the end of the operating band (2.4835 GHz).

Parameter	f_{min} (2.4 GHz)	f_{center} (2.44175 GHz)	f_{max} (2.4835 GHz)
S_{11} [dB]	-14.906	-16.124	-15.282
S_{21} [dB]	17.872	20.075	17.869
S_{22} [mdB]	-382.7	-386.99	-391.44
S_{12} [dB]	-30.463	-30.159	-29.873
NF_{min} [dB]	3.4454	3.5158	3.5882
NF [dB]	3.6446	3.7257	3.8303
Kf	4.0759	4.0178	3.9616
B1f	0.083342	0.083971	0.084972
IIP3 [dBm]	-7.22802		
P1dB [dBm]	-12.1955		
Pdc [µW]	198.926		

Table 14 – Detailed values of the parameters at the frequency points of the 2400 MHz band for the LNA supplied with 1 V.

4.2.2. LNA design for sub-1 V

Once checked the design with Vdd of 1 V, it is modified reducing the Vdd to 250 mV. As consequence of the strong dependency of the current with Vds, which can be checked with a high slope of the current in Figure 23 of the chapter 3, there is an important loss in the overall performance of the amplifier. Figure 62 shows this loss on the input matching and how the gain does not fulfills the specifications.

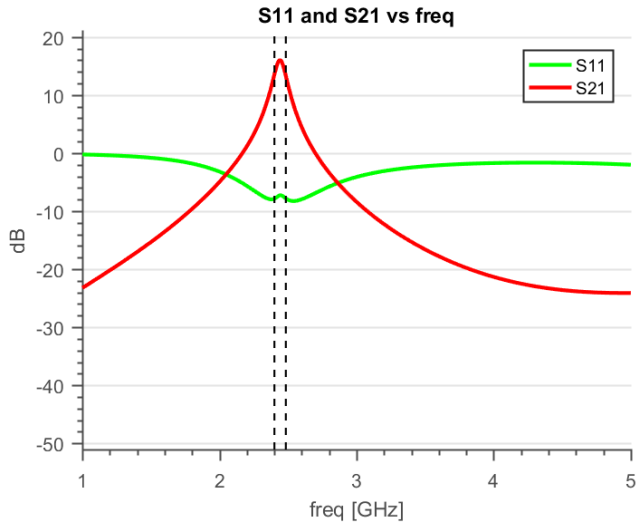

Figure 62 - S21 and S11 parameters over the frequency for the LNA supplied with 250 mV without FBB

Figure 63 also shows how the performance in noise has been decreased as well, but still fulfills the requirements.

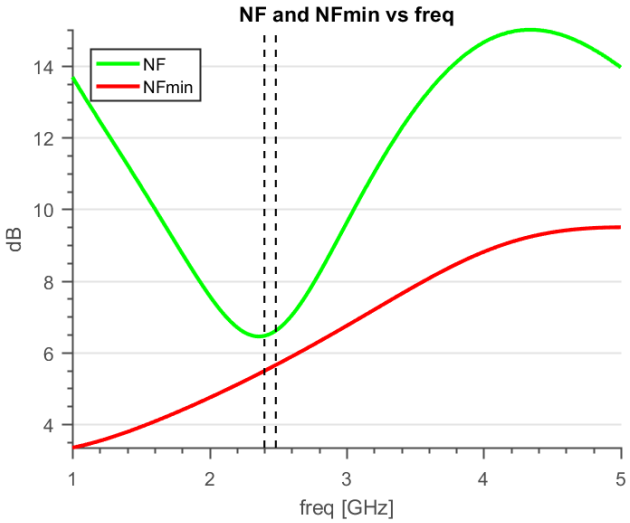

Figure 63 - NF and minimum NF over the frequency for the LNA supplied with 250 mV without FBB

To recover the same specifications the FBB technique is used. The Vdd is the same as the voltage to bias the transistor, this way the design can save an extra voltage reference. The schematic of the design is shown in Figure 64.

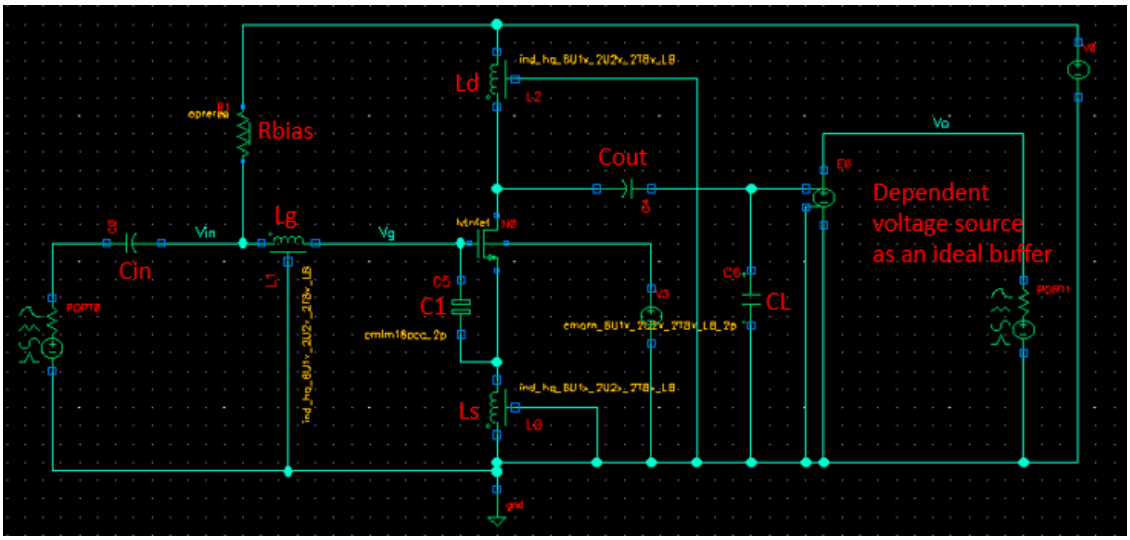

Figure 64 - LNA schematic supplied with 250 mV

Then the voltage at the bulk is swept to recover the f_T needed for the design. The f_T is 25.7 GHz for a voltage of 1 V at the bulk. The number of fingers have been adjusted to 142 to recover the previous gm of 4.3 mS. The V_{dsat} of the transistor is 104.04 mV, so even with a voltage supply of 250 mV the transistor will keep its saturation region. Since the parameters of the transistor have been recovered and the values of the passive components have been picked according to the parameters of the transistor, their values coincide with the values of the previous design. The final values of the schematic are shown in Table 15.

Figure 65 shows the input reflection coefficient (S_{11}) and the forward gain (S_{21}) parameters over the frequency. The values are similar to the previous design, with a maximum S_{11} value of -14.659 and S_{21} above the required 15 dB.

Parameter	Values
V_{dd} [mV]	250
V_{bulk} [V]	1
L_d [nH]	2.495
L_g [nH]	3.8
L_s [nH]	5.5
C_1 [fF]	425
C_L [pF]	1.58
C_{in}/C_{out} [nF]	10
R_{bias} [KΩ]	5
gm [mS]	4.3
Id [µA]	199.522
fingers	142

Table 15 - LNA design parameters when supplied with 250 mV

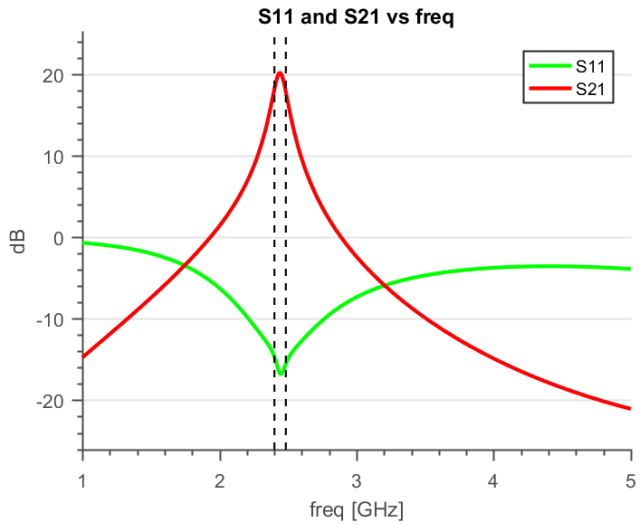

Figure 65 - S_{21} and S_{11} parameters over the frequency for the LNA supplied with 250 mV with FBB

S_{12} and S_{22} of the modified LNA are shown in Figure 66. S_{12} is close approximately -26 dB, a little worse than the previous case. S_{22} is not representative either.

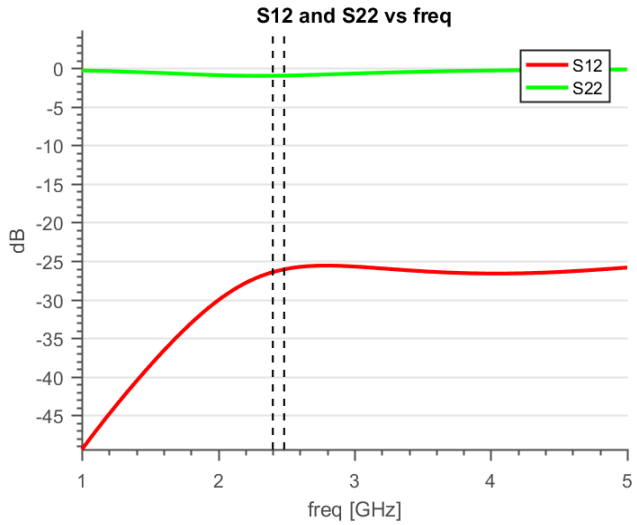

Figure 66 - S_{12} and S_{22} parameters over the frequency for the LNA supplied with 250 mV with FBB

Figure 67 shows the NF parameters of the second LNA. The values are similar to the ones of the previous design, fulfilling the noise specifications.

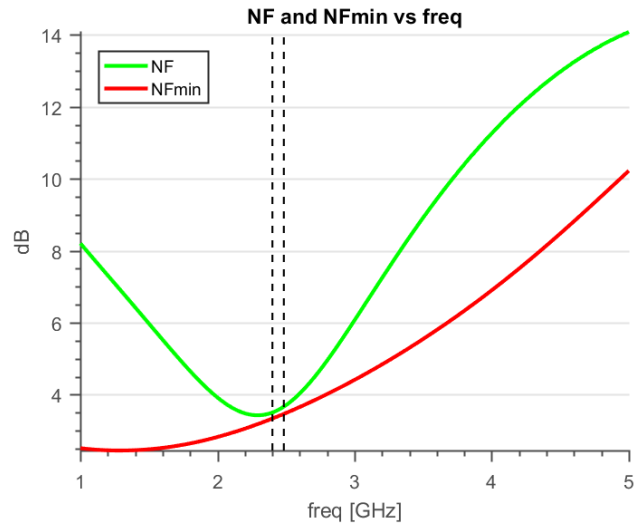

Figure 67 - NF and minimum NF over the frequency for the LNA supplied with 250 mV with FBB

Figure 68 shows Kf and B1f of the second design. The dashed line also appears in the figure to indicate visually where the stability boundary is. The LNA stability is verified over the 1 GHz to 5 GHz frequency range.

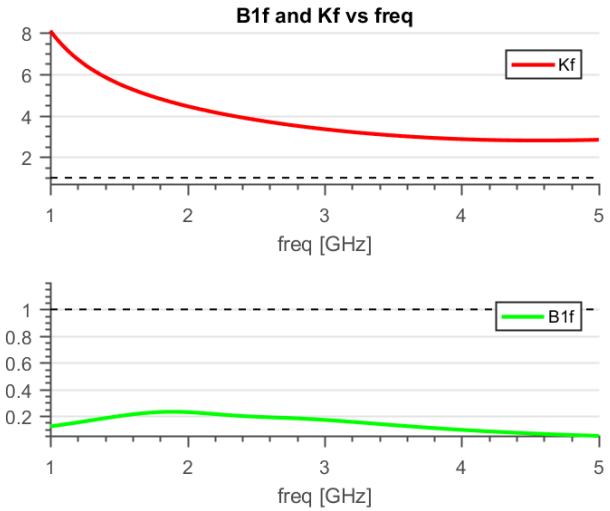

Figure 68 - Stability parameters over the frequency for the LNA supplied with 250 mV

Figure 69 shows its 1 dB compression point simulation where a P1dB=-26.5248 dBm is achieved.

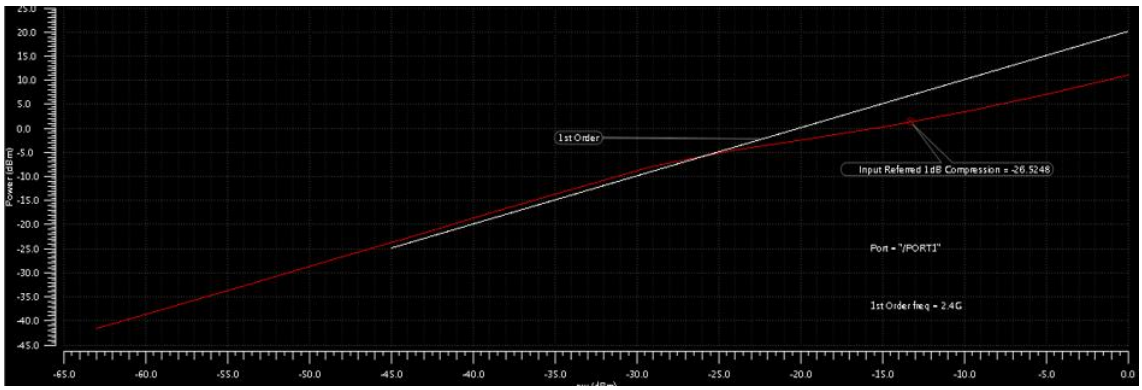

Figure 69 - P1dB of the fundamental tone (2.4 GHz) for the LNA supplied with 250 mV

Figure 70 shows the third-order interception point simulation where IIP3=-6.42319 dBm is achieved. It is well above the IIP3 required for the LNA. The test is exactly the same as before.

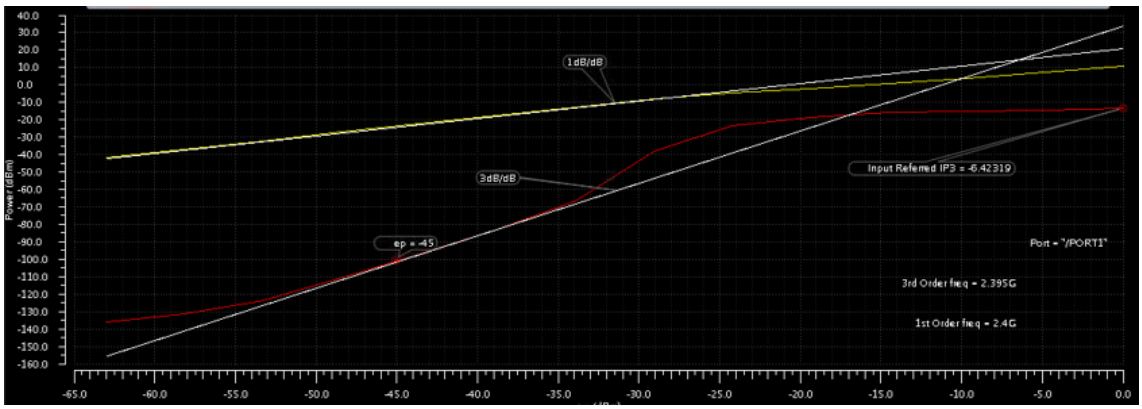

Figure 70 - IIP3 for the test with one tone at fo=2.4GHz and a second tone at f1= 2.405 GHz for the LNA supplied with 250 mV

Table 16 shows the values for all the interesting parameters of the LNA supplied by 250 mV at the same three frequency points defined before.

Parameter	f_{min} (2.4 GHz)	f_{center}(2.44175 GHz)	f_{max} (2.4835 GHz)
S_{11} [dB]	-14.659	-16.75	-15.533
S_{21} [dB]	18.162	20.171	17.84
S_{22} [mdB]	-979.61	-970.23	-957.98
S_{12} [dB]	-26.43	-26.234	-26.069
NF_{min} [dB]	3.3402	3.404	3.4695
NF [dB]	3.5077	3.5785	3.6713
Kf	3.9086	3.861	3.8148
B1f	0.19916	0.1968	0.19469
IIP3 [dBm]	-6.42319		
P1dB [dBm]	-26.5248		
Pdc [µW]	49.8805		

Table 16 - Detailed values of the parameters at the frequency points of the 2400 MHz band for the LNA supplied with 250 mV

Finally, a comparison of these designs with some state of the art LNAs is shown in Table 17. Two make a fair comparison of the overall performance of the LNAs, a figure of merit has been used [118]. This FoM is expressed in equation (4.23), where gain is the voltage gain, IIP3 is the input referred intermodulation point of Third Order, fc is the operating frequency, F is the noise factor and P_{dc} is the DC power consumption.

$$FoM\ [GHz] = \frac{Gain[abs] * IIP3[mW] * fc[GHz]}{(F-1)[abs] * Pdc[mW]} \quad (4.23)$$

The designs on this work, achieve almost the higher gains with the lower power consumption. They also show almost the better performance in noise terms with a comparable linearity. The LNAs from [54, 57 and 61] are Wideband amplifier, so it may be the reason why there is so much difference between FoMs. The work from [119] has better overall performance but pays the price in power, so it could not be taken into account on ULP applications. Although the FoM uses the voltage gain, it is not available in some of the works compared, so in these cases the gain published is used.

Ref	This work [design 1]	This work [design 2]	[120]	[61]	[55]	[54]	[119]	[64]
Tech.	UTBB FDSOI 28 nm		130 nm CMOS	130 nm CMOS	90 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS
fo [Ghz]	2.4	2.4	2.4	4.2	7	10	2.4	1
Vdd [V]	1	0.25	0.4	0.4	0.5	1.1	0.5	1
Pdc [mW]	0.199	0.0499	0.06	0.16	0.75	0.99	2.1	0.1
Gain [dB]	17.87	17.84	13.1	13	12.6	7.9	18.7	16.8
IIP3 [dBm]	-7.22	-6.42	-12.2	-12	-9	-	-4.9	-11.2
NF [dB]	3.8	3.67	5.3	4.5	6.5	6	1.5	3.9
FoM [GHz]	100.1	502.21	20.6	18.17	6.17	-	66.46	24.96

Table 17 - Performance summary and comparison with state-of-the-art LNAs

5. Conclusions and future works

5.1. Conclusions

This thesis has described and characterized the MOS transistors of the 28 nm UTBB-FDSOI technology obtaining the main parameters of the different V_{th} flavored transistors (LVT and RVT) of both type of transistors (NMOS and PMOS). It has showed that LVT transistors are preferred for higher performance systems, due to higher current and transconductance capabilities. The inductors used for this technology have also been characterized showing their quality at 2.4 GHz, where they have shown a good performance with quality factors of 30.

The gm/Id methodology approximation has been introduced to design energy efficient and low power blocks. The LVT NMOS transistor has also been characterized in terms of its inversion degree to apply this methodology on the final designs. It showed that transistors achieve better energy efficiency on weak inversion bias but with low overall performance. The region between the weak and strong inversion regions are the best to obtain energy efficiency blocks with moderate overall performance.

The LNA amplifier designed with the gm/Id approach with this technology is based on a common source topology. Only one LVT NMOS transistor has been used to the amplifier because the design was focused to check this technology suitability for IoT devices requirements, concretely devices with ULV and ULP needs. The standard used for this scenario is the IEEE 802.15.4 standard, which is a LR-WPAN standard optimized for low data rate and low power applications, and could fit on the IoT environment. The LNA has to work on the 2.4 GHz ISM band and its requirements for this standard are very relaxed with a gain of 15 dB, NF lower than 10 dB and IIP3 higher than -30 dBm.

The first design, which was made for a 1 V supply source, has been sized and properly biased with the gm/id graphs extracted on chapter 3. It achieves, on the operating frequency band, a minimum gain of 17.8 dB, with a maximum NF of 4.07 dB and an IIP3 of -7.22 dBm. It fulfills the requirements previously calculated while it is unconditionally stable with only a power consumption of 198.9 µW.

The first design has been used as a starting point for the second LNA. The main aim is to reduce the power consumption of the LNA but still fulfilling the requirements. The strategy used is the supply voltage reduction to levels close to the transistor voltage saturation levels. The use of the FBB technique, which is one of the strong points of this technology, has been adopted to recover the figures of merit of the LNA. The LNA supplied by 0.25 V source and applying 1 V to the body has shown similar but slightly better figures of merit than the previous design. It achieves a minimum gain of 17.8 dB, maximum NF of 3.67 dB and IIP3 of -6.42 dBm. The amplifier remains unconditionally stable and the power consumption has been reduce at only 49.9 µW.

The comparison with other LNA from other works showed that the LNAs from this work have a superior figure of merit when performance and power consumption are being taken into account. The results verifies this technology suitability to IoT environments suggesting it as a very good candidate to handle the IoT RF requirements.

5.2. Future works

This thesis has reviewed only the basics of the UTBB-FDSOI technology, so several future works can be extracted.

The work has shown the basic behavior of this technology, which could be extended with a more detailed study to justify their behavior.

Although the LNA has been designed with component models provided by the manufacturer, post-layout simulations including e.g. Routing parasitics would provide a more realistic performance estimation. In particular, it would be interesting to check whether the outstanding FoM is preserved after considering layout parasitics.

The effects of PVT variability should also be evaluated. It is assumed that, given the voltage-mode biasing and operation at weak inversion, the LNA designed would be highly sensitive to PVT variations, thus implementing techniques to minimize that variability is also a necessary future work.

The proposed work has shown how the aggressive forward body biasing can be used to design amplifiers of a good overall performance with supply voltages as small as 250 mV. Nevertheless, the body bias needed is as large as 1 V. Thus another future work is to design efficient circuitry able to generate those voltages from the small supply. Currently, a body-bias generator standard cell is provided with the design kit of this technology, but it is a power-hungry solution that clearly needs an alternative in the ULP scenario.

There are other components from this technology not showed in this thesis that can be characterized. The characterization in terms of inversion degree could be extended for the rest of the transistors. Once all the characterizations have been performed, other LNA topologies more complex can be explored focusing on the ULV and ULP requirements.

Another possible work can explore other important RF blocks besides the LNAs, i.e. mixers, filters, VCO, PA …, implementing them with this technology to extend further their suitability for RF blocks of low power consumption.

Finally, a full receiver/transmitter can be designed with this technology for a defined IoT scenario. This would fully verify the integration of this technology into the IoT paradigm.

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Appendix 1

MATLAB technology current calculation algorithm code

```
%%%%Technology current calculation

AY10=100; %%distance between SQL and gm/id
Io10 = 1e-6; %%% initial guess of Io
Io_final_1u = Io10;
error = 0.001;

%%%% loop that changes the Io to reach a solution
while 1
      %%% SQL calculation
      strong_line10=max(GmoverId_1u)*((ID_W_L_1u/Io10).^(-0.5));
      %%%distance calculation
      AY110=min(abs(GmoverId_1u-strong_line10));
      Io10 = Io10-0.01e-8;
      if(AY110<AY10)
            AY10=AY110;
            Io_final_1u=Io10+0.01e-8;
      end
      if AY10<error
            Io_final_1u=Io10+0.01e-8;
    break
      end
      if Io10 < 1e-9
            'finish'
    break
      end
end
```

Appendix 2

Width and finger dependences

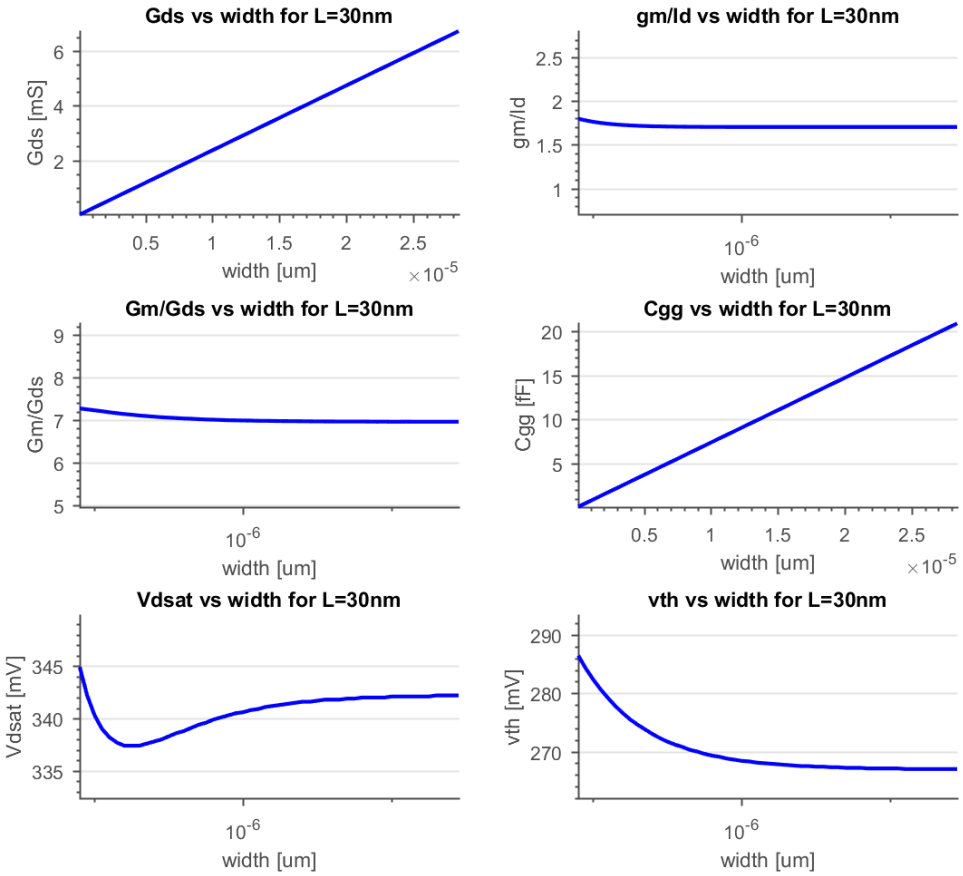

Figure 71 - NMOS LVT parameters vs. Total width for a 30 nm gate length transistor. The measurements correspond to a RF DUT having an aspect ratio of 10, gate lengths of 30 nm, Vgate = 1 V and Vdd = 1 V.

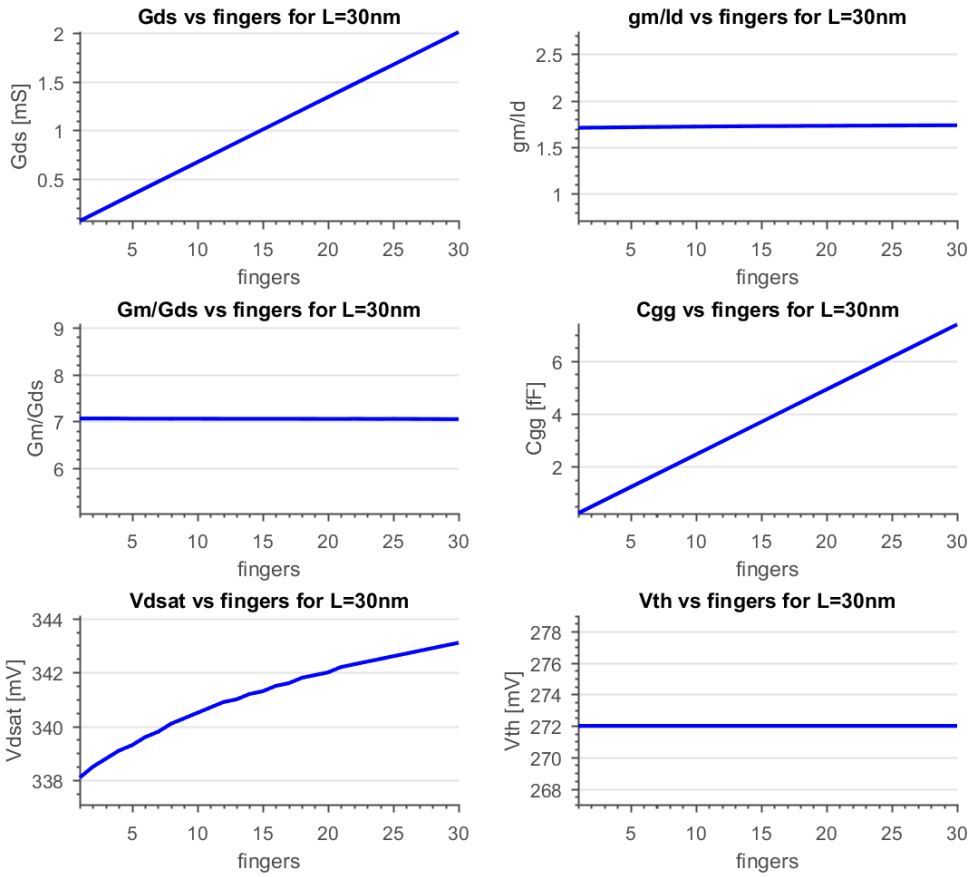

Figure 72 - NMOS LVT parameters vs. number of fingers for a 30 nm gate length transistor and 300 nm of finger width. The measurements correspond to a RF DUT having an aspect ratio of 10, gate lengths of 30 nm, finger width of 300 nm, Vgate = 1 V and Vdd = 1 V.

List of Terms and Abbreviations

ADC	Analog to digital converter
BOX	buried oxide
CG	common gate
CLM	Channel Length Modulation
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
DAC	Digital to Analog Converter
DC	Direct current
DIBL	Drain induced barrier lowering
F	Noise Factor
FBB	Forward Body Bias
FDSOI	Fully Depleted Silicon-On-Insulator
FET	Field Effect Transistor
FinFET	Fin Field Effect Transistor
FoM	Figure of Merit
GIDL	Gate-Induced Drain Leakages
GPRS	General Packet Radio Service
IC	Integrated Circuit or Inversion coefficient
ICT	Information and communication technology
IEEE	Institute of Electrical and Electronics Engineers
IoT	Internet of Things
LNA	Low Noise Amplifier
LPWA	Low Power Wide Area
LR-WPAN	Low Rate Wireless Personal Area Networks
LTE	Long-Term Evolution
LVT	Low threshold Voltage Transistor
MI	Moderate inversion
MAC	Medium Access Control
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NF	Noise Figure
PDK	Process Design Kit
PHY	Physical Layer
RBB	Reverse Body Bias

RF	Radio Frequency
RFID	Radio Frequency IDentification
RSD	Random Dopant Fluctuations
RVT	Regular threshold Voltage Transistor
SCE	Short Channel Effects
SI	Strong inversion
SNR	Signal to Noise Ratio
SoC	System on Chip
SOI	Silicon-On-Insulator
SW	single-well
ULP	Ultra Low Voltage
ULV	Ultra Low Power
UTBB	Ultra-Thin Body and Buried-oxide
UWB	Ultra Wide Band
VGA	Variable Gain Amplifier
V_{th}	Threshold voltage
VLSI	Very-large-scale integration
VS	Velocity saturation
WI	Weak Inversion
WiFi	Wireless fidelity
WiMAX	Worldwide Interoperability for Microwave Access
WSN	Wireless Sensor Node