Growth of III-V solar cells on silicon by Molecular Beam Epitaxy: towards monolithic III-V/Si tandem multijunction devices

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Statement of originality

I, Arthur Onno, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

Signed: _____

Date: _____

To Molly,

My Californian Sunflower.

Abstract

Epitaxial growth of III-V materials on silicon (Si) presents an elegant pathway in order to develop high efficiency III-V/Si multijunction solar cells. Such devices could overcome the 29.4 % efficiency limit inherent to single-junction crystalline silicon (c-Si) solar cells while maintaining the comparatively low cost associated with Si substrates.

The main challenge of this technology lies in the difference of lattice parameters between Si and suitable III-V materials. This lattice mismatch results in the formation of Threading Dislocations (TDs), which propagate upwards to the active regions of the devices. There, they act as recombination centres, hence reducing the minority carrier lifetime and greatly limiting the performance of the devices.

A model has first been developed in order to assess the impact of the Threading Dislocation Density (TDD) on the efficiency of GaAsP/Si dual junction devices. We demonstrate that a TDD below 10^6 cm^{-2} should be targeted in order to achieve efficiencies over 30 %.

1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells, with an ideal bandgap for a top cell in III-V/Si dual-junction architectures, have then been grown on Si substrates by Molecular Beam Epitaxy (MBE). Direct AlGaAs nucleation has been performed on Si, followed by the growth of Dislocation Filter Layers (DFLs) coupled with Thermal Cycle Annealing (TCA) steps in order to reduce the TDD. Notably, a TDD of $8(\pm2)\times10^6$ cm^{-2} has been demonstrated. However, the performance of the cells is limited by the bulk material quality of the $Al_{0.2}Ga_{0.8}As$, independently of TDs.

An optimisation study of the growth conditions of 1.7 eV $Al_{0.22}Ga_{0.78}As$ solar cells on GaAs has, thus, been carried out, leading to a strong improvement in performance when increasing the growth temperature from 580 °C to 620 °C. In particular, an open-circuit voltage (V_{oc}) of 1212 mV has been demonstrated. Transfer of this improved growth recipe to Si substrates should yield devices with a V_{oc} above 1 V.

Impact Statement

This PhD research project focuses on the demonstration of a high material quality, low Threading Dislocation Density (TDD) III-V photovoltaic solar cell epitaxially grown on silicon (Si), with a bandgap of approximately 1.7 eV. Such a cell would produce a short-circuit current (J_{sc}) of approximately 20 $mA.cm^{-2}$, in the range required to ensure current-matching with a Si bottom subcell in a two-terminal dual-junction architecture. The medium-term goal is the development of III-V/Si multijunction devices, with efficiencies in excess of 30 % at a comparatively low cost, thanks to the use of a Si substrate.

Such high-efficiency low-cost devices would have a decisive impact on the photovoltaic industry, as increasing the efficiency is an important lever to reduce the Levelised Cost Of Electricity (LCOE) of photovoltaic projects. Total Gas, Renewables & Power – a major global energy company present in the photovoltaic market through its subsidiary SunPower – is a partner and a sponsor of the research project, thus indicating the importance of the technology for the industry. Moreover, our work has been highlighted in high profile photovoltaic conferences: we have been nominated as finalist for the Student Award at the 44th IEEE PVSC conference and we have been awarded the Student Award at EU PVSEC 2017.

The potential impact of the pathway investigated – specifically the use of Dislocation Filter Layers (DFLs) to reduce the TDD – is similarly high, not only for the photovoltaic academic community but also for the general III-V on Si industry. Indeed, the use of DFLs allows for thin (≈2.5 µm) buffers, particularly in comparison with more common metamorphic buffers. This leads to a reduced growth time and a limited material consumption, hence ultimately lowering the cost of the grown devices. Furthermore, the issues related to thermal mismatch between the substrate and the epilayers, potentially leading to cracking of the material epitaxially grown, are reduced when using such thin buffers.

Our simulation work is also of non-negligible impact for the photovoltaic academic community, as it provides a relatively simple method to model dual-junction devices using a limited amount of material parameters. Thus, other research groups have used the approach we have developed to model perovskite/Si dual-junction devices. The model has also been extended to the study of InGaAs thermophotovoltaic devices.

Finally, our work on the improvement of the growth conditions of 1.70 eV $Al_{0.22}Ga_{0.78}As$ presents an interest not only for the demonstration of III-V/Si tandem hybrid devices, but also for the pure III-V multijunction community. Indeed, III-V solar cells lattice-matched with GaAs and with a bandgap between 1.42 eV and 1.9 eV are needed for the development of multijunction devices with 4 or more junctions. Such higher efficiency devices could be used in terrestrial concentrator or space applications.

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List of Abbreviations, Elements and Materials

Abbreviations

AFM: Atomic Force Microscopy

AM1.5G: Air Mass 1.5 Global spectrum

APB: Anti-Phase Boundary

APD: Anti-Phase Domain

ARC: Anti-Reflection Coating

BF: Bright Field

BSF: Back Surface Field

CMP: Chemically-Mechanically Polished

CPV: Concentrated Photovoltaic

DF: Dark Field

DFL: Dislocation Filter Layer

ELO: Epitaxial Lift-Off

EPD: Etch Pit Density

EQE: External Quantum Efficiency

FM: Franck-Van der Merwe growth mode

J-V: Current Density Versus Voltage

LC: Luminescent Coupling

LCN: London Center of Nanotechnology

LCOE: Levelised Cost of Electricity

LED: Light Emitting Diode

LPE: Liquid Phase Epitaxy

MBE: Molecular Beam Epitaxy

MD: Misfit Dislocation

MEE: Migration Enhanced Epitaxy

MOCVD: Metal-Organic Chemical Vapour Deposition

MPP: Maximum Power Point

NREL: National Renewable Energy Laboratory

OPV: Organic Photovoltaic

PERC: Passivated Emitter Rear Contact

PL: Photoluminescence

PV: Photovoltaic

RGA: Residual Gas Analyser

RHEED: Reflection High Energy Electron Diffraction

RIE: Reactive Ion Etching

RMS: Root Mean Square

SK: Stranski-Krastanov growth mode

SLS: Strained Layer Superlattice

SRH: Shockley-Read-Hall

SSMBE: Solid-Source MBE

TCA: Thermal Cycle Annealing

TD: Threading Dislocation

TDD: Threading Dislocation Density

TEM: Transmission Electron Microscopy

UHV: Ultra High Vacuum

UNSW: University of New South Wales

UV: Ultraviolet

VW: Volmer-Weber growth mode

XRD: X-Ray Diffraction

Chemical Elements

Al: Aluminium

Ar: Argon

As: Arsenic

Au: Gold

B: Boron

Be: Beryllium

Ge: Germanium

Ga: Gallium

In: Indium

Mo: Molybdenum

Ni: Nickel

O: Oxygen

P: Phosphorus

Pt: Platinum

Sb: Antimony

Si: Silicon

Sn: Tin

Ti: Titanium

W: Tungsten

Zn: Zinc

Materials

AlGaAs: Aluminium Gallium Arsenide

AlInP: Aluminium Gallium Phosphide

a-Si: Amorphous Silicon

AuGe: Gold Germanium

AuZn: Gold Zinc

CdS: Cadmium Sulphide

CdTe: Cadmium Telluride

CIGS: Copper Indium Gallium Selenide

CIS: Copper Indium Selenide

c-Si: Crystalline Silicon

GaAs: Gallium Arsenide

GaAsP: Gallium Arsenide Phosphide

GaInP: Gallium Indium Phosphide

GaNAsP: Gallium Nitride Arsenide Phosphide

GaP: Gallium Phosphide

H_2O: Water

H_2O_2: Hydrogen Peroxide

H_2SO_4: Sulphuric acid

InAlAs: Indium Aluminium Arsenide

InAs: Indium Arsenide

InGaAs: Indium Gallium Arsenide

InP: Indium Phosphide

ITO: Indium Tin Oxide

NH_4OH: Ammonia

mc-Si: Multicrystalline Silicon

SiGe: Silicon Germanium

List of Symbols

Roman Alphabet

a: Absorptivity of the cell

a_0: Lattice parameter

c: Speed of light

C: Ambipolar Auger coefficient

$C_{n/p}$: Auger coefficient of electrons/holes

d_{hkl}: Interplanar spacing between crystal reflection planes of Miller indices (hkl)

$D(E)$: Density of states

$D_{n/p}$: Diffusion coefficient of electrons/holes

E: Energy

$\vec{E}$: Electric field

E_A: Acceptor impurity energy level

E_c: Minimum of the conduction band

E_D: Donor impurity energy level

E_F: Fermi level

$E_{F,n/p}$: Pseudo Fermi level of electrons/holes

E_g: Bandgap

E_{ph}: Photon energy

E_v: Maximum of the valence band

$f(E)$: Fermi-Dirac distribution

FF: Fill Factor

G: Generation rate of charge carriers

h: Planck constant

(hkl): Miller indices of the considered crystal plane

I: Irradiance on the surface of a cell

J_0: Saturation current density of a diode

$J_{0,all}$: Total saturation current density, inclusive of all recombination pathways

$J_{0,Auger}$: Saturation current density associated with Auger recombination

J_{0e}: Surface saturation current density

$J_{0,SRH,TD}$: Saturation current density associated with SRH recombination on TDs

$J_{0,rad}$: Saturation current density associated with radiative recombination

$J_{diff,n/p}$: Diffusion current density for electrons/holes

$J_{drift,n/p}$: Drift current density for electrons/holes

J_{mpp}: Current density at the MPP

$J_{n/p}$: Total current density for electrons/holes

J_{ph}: Photo-generated current density

J_{sc}: Short-Circuit Current density

$\boldsymbol{k}$: Wave vector

k_B: Boltzmann constant

L: Thickness of the cell

$L_{n/p}$: Diffusion length of electron/holes

L_{TD}: Diffusion length of minority carriers associated with SRH recombination on TDs

M: Spectral mismatch coefficient

$m^*_{n/p}$: Effective mass of electrons/holes

n: Density of electrons in the conduction band

N_A: Acceptors doping density

N_c: Effective density of states in the conduction band

N_D: Donors doping density

n_i: Intrinsic carrier concentration

n_{oc}: Electron occupancy of a defect level

n_{ref}: Real part of the refractive index

N_v: Effective density of states in the valence band

p: Density of holes in the valence band

p_{oc}: Hole occupancy of a defect level

P: Power

P_{in}: Incoming power on the surface of the cell

P_{mpp}: Power extracted from a solar cell at the MPP

q: Elementary charge

R: Recombination rate

R_{Auger}: Auger recombination rate

$R_{non\text{-}rad}$: Non-radiative recombination rate

R_{rad}: Radiative recombination rate

$R_{rad,dark}$: Radiative recombination rate in the dark, under thermodynamic equilibrium

R_{RMS}: Root mean squared surface roughness

R_S: Series resistance

R_{SH}: Shunt resistance

R_{SRH}: Shockley-Read-Hall recombination rate

$R_{SRH,TD}$: Shockley-Read-Hall recombination rate associated with TDs

R_{surf}: Surface recombination rate

T: Temperature

V: Electric potential

V_0: Built-in electric potential in a diode

V_{ext}: External voltage applied to a diode

V_{mpp}: Voltage at the MPP

V_{oc}: Open-Circuit Voltage

$V_{oc,lim}$: Theoretical upper limit for the V_{oc}

$v_{th,n/p}$: Thermal velocity of electrons/holes

W_D: Width of the depletion zone

$W_{emit/base}$: Width of the emitter/base

W_{oc}: Bandgap-voltage offset

W_{TDD}: Average distance between two threading dislocations

x: percentage composition for compound materials

z: distance within the device

Greek Alphabet

α: Absorption coefficient

Δn: Excess electron concentration

Δp: Excess hole concentration

ε_0: Vacuum permittivity

ε_r: Relative permittivity

η: Efficiency of a solar cell ($=P_{mpp}/P_{in}$)

η_{ext}: External radiative efficiency

θ: Angle

θ_{esc}: Escape angle

λ: Wavelength

$\mu_{n/p}$: Mobility of electrons/holes

ρ_D: Defect density

ρ_{TDD}: Threading Dislocation Density

$\sigma_{n/p}$: Capture cross-section of a defect for electrons/holes

$\tau_{n/p}$: Lifetime of electrons/holes in the conduction/valence band

$\tau_{coll,n/p}$: Mean free time between collisions for electrons/holes

φ_0: Photon flux at the surface of the cell

$\varphi_{n/p}$: Flux of electrons/holes

Ω_{emis}: Solid angle of reemission of the cell

Ω_{sun}: Solid angle of the sun

Other

$\vec{\nabla}$: Gradient operator

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Journal publications

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Chapter 1

Introduction

1.1 History of photovoltaic science and technology

The photovoltaic (PV) industry has seen an extremely fast development in the last decade, reaching at least 75 GW of new installations in 2016 and a total installed capacity of about 300 GW at the start of 2017 [1.1]. More than 60 years of combined research, engineering and commercial development have enabled this achievement.

The first PV devices were created in the 19th century when, in 1883, Charles Fritts used selenium coated with a very thin transparent layer of gold – thus forming a Schottky junction – to produce a photo-voltage and a photo-current [1.2]. Werner von Siemens confirmed the effect [1.3] and Fritts already envisioned the possibilities offered by such devices to produce power at industrial scale and to replace fossil fuels in the long term. However, the efficiency of these early solar cells was too low (around 1 to 2 %) to define them as “practical devices”. Moreover, the understanding of semiconductors and of the photovoltaic phenomenon was very limited at that time.

Research on selenium-based PV cells was pursued during the first part of the 20th century, without noteworthy improvement.

The next breakthrough came in the middle of the 20th century, with the early developments of the semiconductor industry. Russell Ohl discovered the p-n junction in 1939 at Bell Labs and demonstrated its photovoltaic properties. He filed the first silicon solar cell patents in 1941 [1.4-1.5] but, again, the efficiency of such early devices was too low to develop useful applications.

Chapin, Fuller, and Pearson created the first practical PV cells in 1954 [1.6] – again at Bell Labs – with an efficiency of around 4-6 %. They also developed the first PV module from small strips of cells. Their progress mainly came from a good understanding of semiconductor materials and of the processes at play in silicon solar cells. Although Bell Labs did not find commercial success with these early solar cells, this discovery opened the modern era of photovoltaics.

With the rapid expansion of the semiconductor industry and the development of new semiconductor materials, PV cells made of these novel materials were also fabricated. The first cadmium sulphide (CdS) cell was created at the US Air Force Laboratory in Dayton, Ohio in 1954 [1.7]. In 1956 the first III-V solar cells – referring to the elements in the columns III and V of the periodic table from which the compound semiconductor material is made of – were fabricated at RCA Laboratories and Siemens [1.8-1.9]. Both cells were made of gallium arsenide (GaAs). Cells made from indium phosphide (InP), another III-V material, and cadmium telluride (CdTe), a II-VI material, were also fabricated at RCA Laboratories at that time [1.10]. Additionally, in 1955, Jackson of Texas Instruments conceptualized a new type of solar cell made by stacking materials of increasing bandgaps [1.11]. The concept of multijunction, or tandem, solar cells was born. Nevertheless, for years, none of these technologies achieved efficiencies as high as the ones obtained with silicon-based cells, and silicon stayed the material of choice for photovoltaics.

Given the very high cost of silicon purification and semiconductor fabrication processes at that time, power generation through photovoltaics for terrestrial applications proved to be too expensive. However, another emerging industry had

applications for such lightweight autonomous sources of power: the space industry. The Vanguard I satellites, equipped with silicon solar cells on top of traditional electrochemical batteries, was launched in 1958. Though the electrochemical batteries ran out of power after a few weeks, the satellite operated for more than 6 years thanks to its 6 PV cells.

Though still very expensive, the benefits of photovoltaic power (reliable for long time periods, lightweight, autonomous) outweighed the cost issue for critical applications such as powering spacecrafts. With the expansion of the space industry, PV cells became the main source of power for space applications, giving birth to the photovoltaic industry. Thanks to the impetus and capital from space applications, silicon-based PV technology improved at a fast rate to reach 14.5 % efficiency in 1961 [1.12].

PV cells proved to be too expensive for terrestrial application until the early 1970's. At that time Elliot Berman, funded by Exxon, realised that silicon quality for PV applications did not need to be as high as for other semiconductor devices such as transistors. He also realised that scrap wafers from the semiconductor industry exhibited antireflective properties due to their patterned surface. He directly used these scrap wafers for solar cells manufacturing, replacing the expensive high quality polished silicon wafers on which antireflection coatings were needed [1.13]. This innovation reduced the price of PV cells by a factor of 5 – from around 100 $\$.W^{-1}$ to 20 $\$.W^{-1}$ – and opened the field for terrestrial applications of photovoltaics, especially in remote areas such as navigation warning lights, offshore or isolated oil and gas rigs, and lighthouses [1.14].

With the 1973 oil crisis, multiple countries began to support research on alternatives to market-dominant fossil fuels in order to support energy independence. In the United States, the Solar Energy Research Institute was established in 1974 and began operations in 1977. Renamed the National Renewable Energy Laboratory (NREL) in 1991, it is still one of the leading research centres on photovoltaics today. Similarly, the Solar Photovoltaic Group at University of New South Wales (UNSW) in Australia created its first solar cell in 1975. UNSW later established multiple world records for

silicon-based PV cells and has been instrumental in the development of advanced PV technologies.

This political support for research on photovoltaics spurred a new wave of technology improvement in the 1970's. Zhorev Alferov and his team created the first high-efficiency III-V-based solar cell in the USSR in 1970 [1.15]. In that case, the cells were made of a GaAs/AlGaAs heterostructure and their relative high efficiency made them the choice technology to power Soviet satellites. Woodhall and Hovel, from IBM Laboratories, reported the fabrication of a similar GaAs/AlGaAs heterostructure in 1972, with an efficiency of 17 % [1.16]. In 1974, Carlson and Wronski from RCA Corporation fabricated the first amorphous silicon (a-Si) based PV cell with an efficiency of 2.4 % [1.17]. These cells were made of an amorphous thin film of silicon (around 1 μm thick) and, therefore, used far less material than the standard crystalline silicon-based technology. Multi-crystalline silicon (mc-Si) solar cells also gained traction in the second part of the 1970's, especially with the contributions from Lindmayer [1.18] and Fischer and Pschunder [1.19]. Multi-crystalline silicon avoids the recrystallization by Czochralski process and is, thereby, less expensive than fully crystalline silicon (c-Si) though PV cells made from mc-Si exhibit lower efficiencies. This cost advantage has made it the dominant technology for the PV industry, representing about 65 % of the c-Si market in 2016 [1.20].

During the 1980's and the 1990's, with the improvement of the technology and the decrease of costs, the use of PV systems became widespread for consumer electronics such as calculators. Simultaneously, the first high-scale demonstration photovoltaic power plants were developed. The first 1-megawatt-peak (1 MWp) photovoltaic power plant, built by ARCO Solar in Hesperia, California, started operations in 1982. A 6 MWp plant in San Luis Obispo County, California, followed in 1983 [1.21]. When taking residential installations into account, global photovoltaic module shipments reached 46.5 MW in 1990 [1.22], mainly manufactured and installed in 3 geographic areas: North America (and in particular the United States), Europe, and Japan. Deployment accelerated during the 1990's – thanks to favourable incentive mechanisms and large-scale pilot programmes in these regions – and the total installed capacity topped more than 1 GW by 2000 [1.23], representing a 10-fold expansion from its size a decade earlier.

The technology also kept improving, with UNSW fabricating the first silicon photovoltaic solar cell with an efficiency over 20 % in 1985 [1.24] and over 25 % in 1999 [1.25-1.26]. New concepts were also developed: in 1986, at Stanford, Richard Swanson fabricated concentration systems, demonstrating an efficiency of 27.5 % from a silicon solar cell under 100-suns concentration [1.27]. In 1995, NREL developed the first photovoltaic solar cell to overcome the 30 % efficiency limit with a 30.2 % efficient GaInP/GaAs multijunction cell under a concentration of around 150 suns [1.28]. From there, III-V multijunction solar cells improved at a pace of nearly one additional absolute per cent per year. Concurrently, Michael Graetzel and Brian O'Regan fabricated the first practical photovoltaic solar cells based on organic materials in 1991 [1.29], opening the way to a wide range of new possible materials for photovoltaic solar cells.

The photovoltaic industry represented a cumulative installed capacity of over 1 GW in 2000 with an added capacity of more than 400 MW that year [1.23]. With a strong manufacturing base emerging, a mature technology, and a dynamic market, photovoltaic energy was ready for the next big phase of its global development: becoming a mainstream electricity generation technology competitive with conventional power generators.

1.2 The photovoltaic market in 2017: domination of crystalline silicon (c-Si) technologies

From 2000 to 2016, the photovoltaic market has grown 190-fold: industry experts expect 77 to 85 GW of new installations in 2017 alone, with a general consensus around 80 GW. This would represent a total installed capacity of 380-390 GW at the end of 2017. This impressive growth over only 17 years has profoundly impacted the structure of the industry, with a series of boom-and-busts due to supply-demand imbalances along the industrial value chain. The main outcomes of this transition from a MW-level industry to a GW-level industry are the domination of crystalline silicon (c-Si) based technologies and the displacement of manufacturing capabilities towards Asia, in particular China, Taiwan and Southeast-Asian countries.

During the first 60 years (1940-2000), the development of the PV industry had mainly been fuelled by technological innovation and conquest of a few niche markets such as powering spacecrafts or offshore oil exploration. In strong contrast, the recent progress is primarily due to public policy support and cost reductions through economies of scale and building of a strong industrial supply chain, with technological innovation taking the back seat. Public policy support has been particularly critical in Germany with the *Energiewende*, the German energy transition from fossil fuels and nuclear power to renewable energies and energy efficiency. The first stable GW-scale market emerged in Germany in 2007, soon followed by Italy in 2010 and the United States, China, and Japan in 2011 [1.23]. All of these markets are supported by a political will to reduce greenhouse gases emissions and accelerate the transition toward renewables. India is poised to become the next photovoltaic super power with a plan to deploy 100 GW of PV between 2015 and 2022 [1.30].

To answer this booming but still subsidy-driven market, the PV community has explored multiple technological pathways to continually decrease system price and improve cost competitiveness, with the medium-to-long-term goal of reaching subsidy-free grid-parity. A considerable paradigm shift sparked this new wave of research for a disruptive technology: in 2006, while the PV market boom was taking shape, PV manufacturing overtook the microelectronics industry as the number one consumer of polysilicon, whereas for years the PV industry had used silicon leftovers from microelectronics as its main feedstock. This reversal led to a shortage of polysilicon, that in turn sparked a steep increase in wafers price, slowing down the cost reduction curve of PV solar cells. As a result, numerous alternatives to the 50-year old c-Si p-n junction, especially thin-film technologies, started to gain traction among academics, entrepreneurs and venture capitalists. This led to the creation of dozens of PV start-ups, mainly in the United States, trying to disrupt the c-Si domination of the market with breakthrough technologies.

Dr. Richard Swanson, founder of SunPower and former Professor at Stanford University, accurately predicted the future evolution of the photovoltaic industry and technologies as early as 2006 [1.31]. In particular, he showed that the cost of c-Si PV has historically been reduced by 20 % for every doubling of the cumulative production – which is a common learning curve for the industrialisation of goods –

and that the slow down in cost reductions due to polysilicon feedstock shortage was just a temporary setback. As of 2013 this cost reduction rule, sometimes called the "Swanson Law", is still verified [1.32] as shown in FIGURE 1.1. On top of the challenge of building the industrial supply chain needed to unlock economies of scale already enjoyed by c-Si incumbents, emerging technologies face a fast-moving target when it comes to cost.

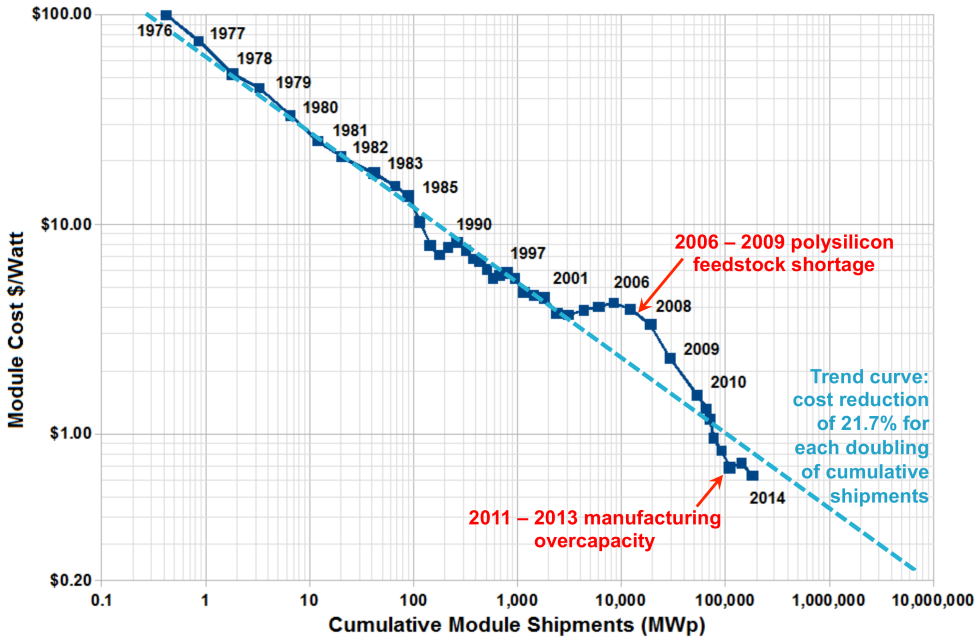

FIGURE 1.1. *Cost reduction in c-Si photovoltaic modules manufacturing: module cost in $.W^{-1} as a function of the cumulative module shipments in MW-peak (log-log plot). Adapted from Ref. [1.33] – Data from Ref. [1.32] – No permission required (CC0 1.0).*

In his paper, Dr. Richard Swanson also highlighted the importance of efficiency on the cost of the final system. Indeed, the cost of a certain number of elements of a full system is related to the area deployed rather than the power capacity installed. It is particularly the case for the balance-of-system (cabling, inverters, junction boxes…) and installation labour costs. Consequently, lower efficiency modules will produce a lower amount of energy for the same fixed cost, increasing the overall cost-per-watt of the system. Thus, imagining an 8 %-efficient "free" PV technology, where the cells manufacturing is free and module lamination is the only manufacturing cost taken into account, Richard Swanson shows that the final cost of such a system would be on

par with a standard 18 %-efficient c-Si system. In other terms, higher efficiency technologies can enjoy a cost premium over low efficiency ones and, although cell cost-per-watt is a useful metric, it tends to skip crucial information regarding the full system cost. As a result, low-cost low-efficiency emerging technologies face a higher entry barrier than the one projected when only considering cost-per-watt.

Adding to these two main obstacles a general over-optimism regarding the scalability of emerging technologies and the associated required capital – as well as possible issues regarding module lifetime – start-ups trying to disrupt the c-Si industry faced challenging times once new polysilicon production plants were on line and the c-Si cost reduction resumed its path. Moreover, starting in 2011, an imbalance in the supply-demand for PV modules, due to a manufacturing overcapacity, provoked a steep drop in module average selling price. This led to a series of high-profile bankruptcies, particularly in Silicon Valley where venture capital funds had fuelled the PV start-up boom. GreenTech Media, a specialised media company, has covered the phenomenon, releasing a significant list of deceased companies between 2009 and 2015, most of them having gone bankrupt [1.34].

As Dr. Richard Swanson had predicted, c-Si technologies kept and even extended their domination of the market. Only two thin-film companies, both of them backed by decades of R&D, have been able to survive at the GW-scale: First Solar (Cadmium Telluride – CdTe) and Solar Frontier (Copper Indium Selenide – CIS). No other emerging technology, be it organic photovoltaics (OPV), concentrated photovoltaics (CPV) or other thin films (a-Si, CIGS, GaAs…), has been able to succeed at the needed GW-scale. The only start-ups to survive, most of the time through acquisition, were the ones focusing on c-Si technology improvements or on the system itself and its installation (balance-of-system, monitoring, project financing and development…), not on a new potentially disruptive photovoltaic cell technology. Additionally, an overcapacity wave – due to massive manufacturing expansions mainly in China and Taiwan – hit the industry in 2011-2013. The concentration of the market around a few big players accelerated, eliminating most of the less strongly capitalized occidental manufacturers. In order to succeed in the current PV market, new cell technologies need to be extremely cheap, efficient, and rapidly scalable; able to capitalize on the industrial c-Si platform; or combine both of these approaches.

1.3 Higher efficiency: a key for cost reduction

The PV industry has experienced a rapid and sustained development in recent years, to the point where photovoltaic energy has become a key technology to accelerate the transition from fossil fuels and to decarbonize electricity production. However, a central barrier still remains: although costs have reduced drastically since 2000 (see FIGURE 1.1), PV is still not fully competitive with best-in-class fossil fuels without subsidies in most markets [1.35]. In order to accelerate the development of PV, as well as to offset the impacts of a future decrease in subsidies in numerous markets, further cost reduction is needed.

Multiple levers exist in order to reduce the cost of a PV system, such as decreasing the cost and the amount of materials used, increasing manufacturing line productivity through automation, or decreasing installation costs through labour optimisation. So far, the main cost reductions have come from an optimisation of production tools (larger cells, screen-printing of the contacts, automation, economies of scale…) and a reduction in the cost of materials (strong decrease in the cost of polysilicon, use of multi-crystalline silicon wafers, reduction in wafer thickness so that less silicon is used per cell, thinner metal contacts…). However, these strategies only target one particular element of the production chain and have a limited impact on the overall system cost, especially when non-module costs (balance-of-system, installation and other downstream "soft costs") represent, on average, more than 80 % of the cost for residential systems [1.36].

In contrast, one lever plays a particularly significant role in overall cost reduction: increasing system efficiency. Thus, instead of reducing the cost of one particular piece of the system, a larger amount of power is produced for a similar price and the cost-per-kilowatt-hour of electricity produced is decreased. This approach has been a core strategy for companies such as SunPower, which can sell higher efficiency c-Si cells and modules at a premium due to their higher power output. Similarly mainstream c-Si companies have been incrementally increasing their cell efficiency over the recent years through advanced back-surface field and passivation techniques (PERC architecture). In other words, among the multiple levers for cost reduction,

efficiency is a very critical parameter as it impacts the cost per unit of energy produced of the whole system.

1.4 III-V on silicon: a promising pathway to achieve high efficiency solar cells on a low cost substrate

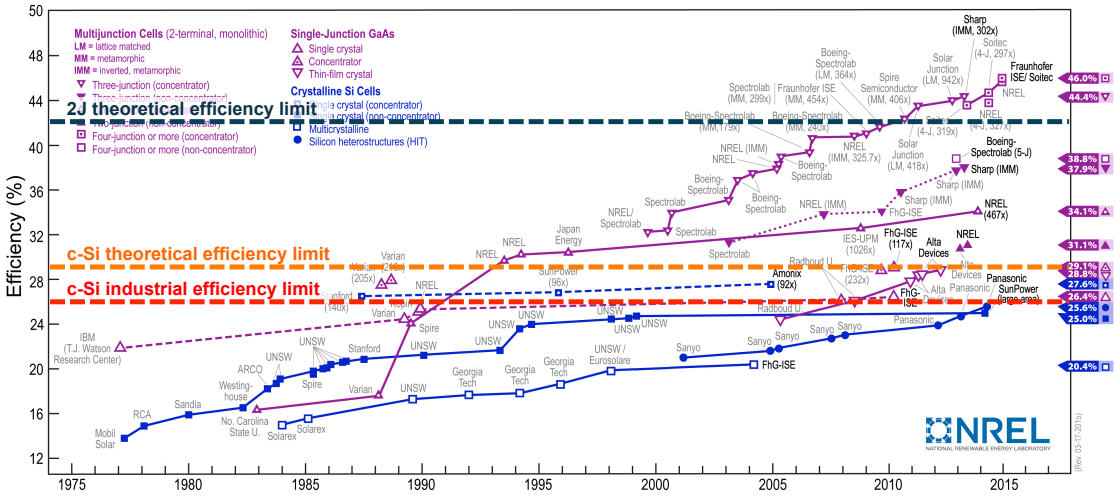

FIGURE 1.2. *Research cell record efficiency chart, with the theoretical efficiency limits for crystalline silicon (c-Si) and dual junction (2J) displayed, as well as the industrial efficiency limit calculated by Smith et. al. [1.37]. Original plot courtesy of the National Renewable Energy Laboratory (NREL), Golden, CO [1.38]. No permission required.*

With 25.6 % record efficiency and 25.0 % efficiency achieved with processes used for industrial production of solar cells [1.37-1.39], c-Si technology is already very close to its theoretical maximal efficiency of about 29 % [1.40-1.41], and the margin for further improvement is very small, as illustrated on FIGURE 1.2. In order to overcome this efficiency barrier, a new approach is needed. III-V based multi-junction solar cells, made of a stack of cells each converting a different part of the solar spectrum, as shown in FIGURE 1.3, have been able to achieve efficiencies close to 40 % without concentration [1.42-1.43]. However, the need for expensive substrates makes their high scale development unlikely. Although Epitaxial Lift-Off (ELO) process – where the epilayers are separated from their growth substrate, for example through etching

of a sacrificial layer – is a solution pathway to overcome this issue and has shown very good results at the laboratory scale [1.44], uncertainties remain regarding the costs and limits of substrate reuse.

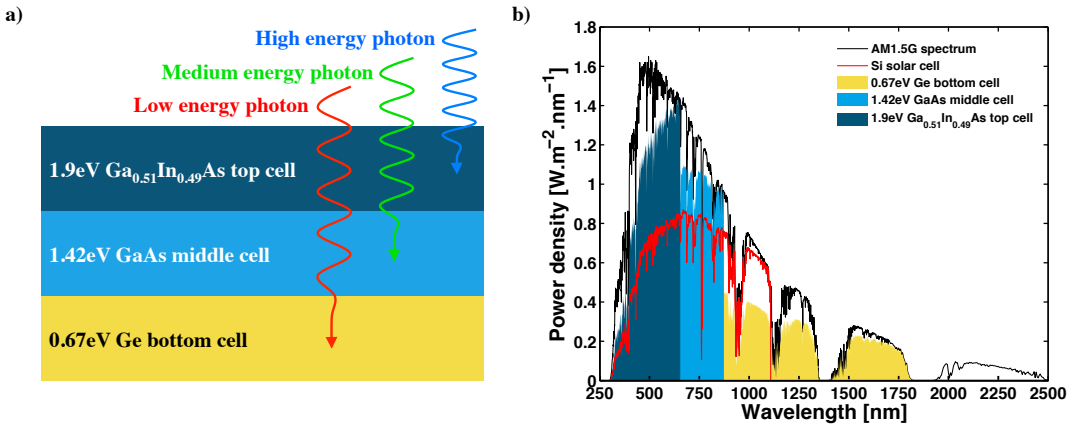

FIGURE 1.3. a) *Schematic of a classic $Ga_{0.51}In_{0.49}P$/GaAs/Ge triple junction solar cell, representing the absorption of different energy photons.* ***b)*** *Comparison between the energy collection ability of Si (red line) and a classic $Ga_{0.51}In_{0.49}P$/GaAs/Ge triple junction solar cell (yellow, light blue and dark blue areas).*

A promising candidate for low-cost high-efficiency solar cells is the integration of III-V single- or multi-junction solar cells on a comparatively low-cost silicon substrate. As III-V materials are polar crystals, where elements III and V fill different sites in the lattice, their direct growth is challenging on non-polar c-Si, where all Si atoms are interchangeable. Moreover, most III-V materials have a lattice parameter (representing the spacing between atoms in the crystal lattice) larger than the one of Si, creating stress and eventually dislocations in the grown III-V layers. Wafer bonding – where the III-V device is grown on a dedicated III-V wafer and then bonded to a Si wafer before separation from its initial substrate – circumvents these issues and has resulted in high efficiency devices [1.45]. However, the fabrication of III-V cells on distinct substrates involves a step of separation in a process akin to ELO. Challenges pertaining to this technology are, thereby, still a concern for wafer bonding pathways.

In the case of monolithic growth of III-V on Si, a lot of work has been carried out for the past 30 years [1.46] in order to overcome the issues mentioned above. The

technology has not only been investigated for solar cells applications [1.47] but also for the direct integration of lasers on the mature c-Si integrated circuit platform [1.48]. The first III-V solar cells on Si, made of GaAs on a thin Ge film, were grown at MIT in 1981 by Gale *et. al.* [1.49]. Following these early results, Yamaguchi *et. al.* from NTT Laboratories [1.50-1.51] improved the material quality and the efficiency of GaAs solar cells directly grown on Si in the late 1980's. They also developed a model for the impact of dislocations in the III-V layers on the efficiency of the cell [1.47]. In the early 1990's, a team from Nagoya Institute of Technology expanded the technology to higher bandgap III-V compounds such as AlGaAs [1.52] and GaAsP [1.53]. With these higher bandgap materials, the first III-V/Si dual-junction solar cells, where the Si substrate acts as a low bandgap bottom cell current-matched with the III-V top cell, were fabricated [1.52].

This technology, combining a current-matched III-V top cell grown on a Si bottom cell, represents a straightforward approach to fabricating high efficiency low cost solar cells. The possible use of a unique piece of equipment to perform the growth of the top cell, be it by Molecular Beam Epitaxy (MBE) or Metal-Organic Chemical Vapour Deposition (MOCVD), makes it a very elegant and industrially relevant pathway. As a result, since the early 2000's, multiple teams have been investigating the growth of relatively high bandgap (≈1.7 eV) III-V solar cells on Si for III-V/Si tandem dual junction solar cells [1.54-1.57]. Contrary to the early work by Shimizu *et. al.* [1.52], most of the current work concentrates on metamorphic structures. In these structures the lattice-mismatch between the Si substrate and the III-V top cell is accommodated by a metamorphic $GaAs_xP_{1-x}$ [1.54-1.56] or $Si_{1-x}Ge_x$ [1.57] graded buffer where the ratio x is progressively increased, gradually shifting the lattice parameter from the one of Si to the required final one. Although this approach has yielded compelling results, relatively thick and slowly grown buffers are needed to ensure good material quality, increasing the final cost of the technology.

In parallel, Professor Huiyun Liu at University College London (UCL) has been investigating direct growth of III-V on Si for quantum dots laser applications [1.58]. Excellent progress has been reported over the past few years [1.59]. As will be more extensively detailed in Chapter 3, instead of using a metamorphic buffer, Professor Liu's team developed direct MBE growth of AlGaAs on Si in combination with

dislocation filters to block the propagation of dislocations. One key advantage of this pathway, on top of the excellent results reported, is a lower buffer thickness needed to achieve high material quality compared with metamorphic approaches, where the best results are obtained with a progressive metamorphic grading and, therefore, thick buffers.

The objective of the present thesis is to expose the research carried out at UCL under the supervision of Professor Huiyun Liu to transfer the results achieved on lasers to the growth of high efficiency III-V/Si multijunction solar cells. In particular, the goal is to demonstrate high material quality 1.7 eV III-V photovoltaic solar cells grown on Si, suitable as a top cell in a III-V/Si dual junction architecture.

1.5 Thesis structure

This thesis contains 7 chapters.

This 1st introduction chapter presents the history of the photovoltaic industry and gives the general background of the research carried out. In particular, it describes where the need for high efficiency low cost solar cells stems from. In this frame, the III-V/Si tandem PV cell technology is introduced and the objectives of the research performed under the direction of Professor Huiyun Liu are presented.

The 2nd chapter gives an introduction to the physics of solar cells, presents the major intrinsic and extrinsic losses limiting the efficiency of photovoltaic devices, and introduces the concept of multijunction solar cells.

An introduction to the facilities and equipment used to grow, fabricate, and characterise experimental III-V on Si solar cells is given in the 3rd chapter. MBE growth, photolithography fabrication techniques, and material quality and optoelectronic properties characterisation tools are in particular detailed. The challenges related to state-of-the-art III-V/Si heteroepitaxy, and the techniques available to overcome these obstacles, are also presented.

The 4th chapter details the numeric model developed to simulate III-V/Si tandem junction solar cells in the case of a GaAsP/Si solar cell, including the impact of threading dislocations on the performance of the dual junction cell.

The 5th chapter presents the experimental results obtained on the growth of AlGaAs solar cells on Si using Dislocation Filter Layers (DFLs). Improvements in the material quality of AlGaAs solar cells grown on Si are achieved by performing a Thermal Cycle Annealing (TCA) step after the growth of each DFL. Finally, a comparison between AlGaAs and GaAs solar cells grown on Si using DFLs and TCA steps is presented. The issues hindering the efficiency of AlGaAs devices are further discussed, as the comparison with GaAs solar cells offers additional insights.

The 6th chapter details efforts to improve the material quality of reference 1.70 eV $Al_{0.22}Ga_{0.78}As$ solar cells grown lattice-matched on GaAs, by optimising the $Al_{0.22}Ga_{0.78}As$ growth temperature. Strong improvements in the open-circuit voltage and the short-circuit current of the devices are demonstrated.

The final 7th chapter is a conclusion on the work performed during the past 3 years and a half of this PhD project and outlines the research to be carried out in the future to further improve the efficiency of 1.70 eV AlGaAs solar cells monolithically grown on Si and achieve high efficiency III-V/Si dual junction devices.

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Chapter 2

Physics of Solar Cells

This chapter presents some basic science behind the physics of solar cells. In order to be as coherent as possible, the chapter opens on fundamentals of semiconductor science and technology, starting with the implications of the crystalline structure of semiconductors on their energy band behaviour before expanding on the difference between intrinsic and doped semiconductors. The chapter then concentrates on p-n junctions, explaining their functioning under thermal equilibrium and under bias before deriving the basic equations ruling their operations. A more detailed section is dedicated to the photovoltaic effect and light absorption in semiconductors, explaining how a photocurrent and a photovoltage are generated in a basic p-n junction photovoltaic solar cell. In the last section, the main intrinsic and extrinsic sources of losses in PV cells and the corresponding efficiency limitations are explored. Finally, the concept of multijunction solar cells is described and the basic operation of this particular technology is briefly explained.

2.1 Basics on semiconductors science

2.1.1 Crystalline structure of semiconductors

Usually, semiconductors are highly crystalline materials where atoms are organised in a periodic structure. Although some semiconductors can be amorphous, we focus here on the simple case of crystalline ones, as they are the general rule. The most commonly found crystalline structure in semiconductors is the diamond type for pure element semiconductors such as the ones from the group IV (Si, Ge…) and the zinc-blende structure for binary compound semiconductors such as the ones from groups III-V (GaAs, InP…) or II-VI (CdTe, CdS…). Both structures are very similar, the difference residing in how atoms of different natures will occupy definite sites of the crystal in the case of binary compounds, as shown in FIGURE 2.1. The structure consists of a face-centred cubic lattice, where atoms reside at each corner of a cube and in the middle of each face, with additional atoms in 4 of the 8 tetrahedral sites. In the case of a zinc-blende structure, these tetrahedral sites are occupied by one particular species of atoms, for example Ga, while the sites at the corners and in the middle of the faces are occupied by the other atomic element, for example As.

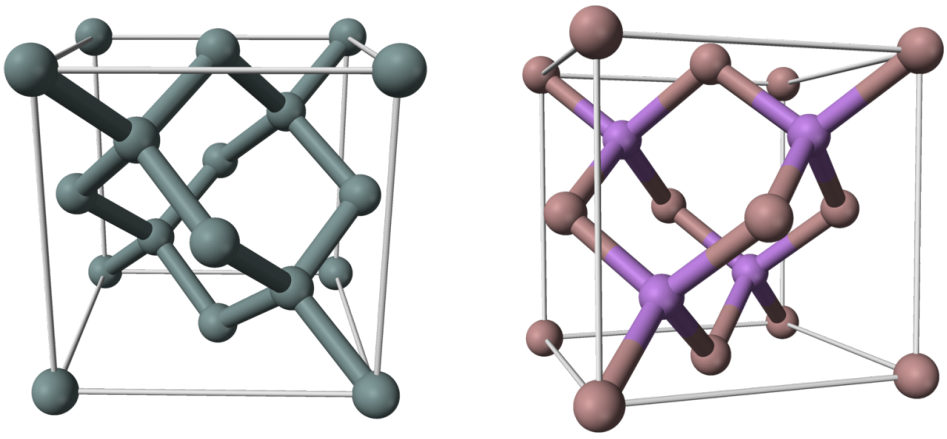

FIGURE 2.1. *Diamond cubic (left) and zinc-blende (right) crystalline structures. In the diamond cubic structure, all atoms are identical and are interchangeable in the lattice. In the zinc-blende structure, different atoms are occupying the peripheral sites (in pink) and the internal tetrahedral sites (in purple). Reprint from Ref. [2.1-2.2] – No permission required (public domain).*

Given the relative difference of mass between electrons (9.1×10^{-31} kg) and atomic nuclei (4.7×10^{-26} kg in the case of silicon) in such a crystal, nuclei can be considered immobile, one at each site of the crystal, while electrons can travel more or less freely. It is important to note that, given this very periodic organisation, electrons will not "see" the same thing depending on their position in the lattice and the direction. This will lead to important anisotropic properties in crystalline semiconductors.

2.1.2 Energy band structure

If each atom were isolated from the others, its electrons would behave in a quantised way and organise on separate finite energy levels, with limited possibilities to move from one energy level to the other. However, in the case of a crystal, each electron will be under the influence of the billions of atoms surrounding it. As a result, the energy levels are split and the finite energy level structure switches to an energy band structure where each band consists of the concatenation of the levels from all the surrounding atoms.

Given that the number of atoms in the crystal is extremely large, the bands can be considered as continuous as the individual energy levels constituting it are infinitesimally close to one another. Therefore, electrons can move freely inside an energy band. Similarly to individual atoms, the bands are separated by forbidden energy states forming forbidden bands where the atoms cannot reside. Moreover, electrons will populate the energy bands by increasing level of energy.

Depending on how the last electrons of an atom – called the valence electrons – fill up their band, the properties of the material will be extremely different. If the last band is not fully occupied, then, even at 0 K, an infinitely small electric field will still be able to create a current, as the electrons will be able to move freely by accessing an infinitesimally close unoccupied level of energy in the same energy band. The material is then a metal. However, if the last band is already full, electrons will need to jump to the next band to move freely and carry a current at 0 K. Therefore, a much larger electric potential is needed to provoke this leap over the forbidden band and create a current. The material is then an insulator. This energy needed to jump from the last fully occupied energy band, called the valence band, to the following

unoccupied one, called the conduction band, is named the bandgap E_g and is of foremost importance to semiconductor science.

Depending on the value of the bandgap, the properties of the material at room temperature (300 K) will be very different. Indeed, at 300 K, the occupation of the bands is modified, as some electrons can be thermally excited to higher energy states. If the bandgap is wide (E_g>4 eV), as it is the case for diamond (E_g=5.5 eV), the probability of an electron to get enough energy to jump over the bandgap to the conduction band is extremely low and the material is a true insulator at room-temperature. However, if the bandgap is small (E_g<4 eV), as it is the case for silicon (E_g=1.12 eV) or GaAs (E_g=1.42 eV), a significant number of electrons can be thermally excited from the valence to the conduction band at 300 K, leading to a non-negligible conductivity, and the material is a semiconductor. Therefore, at room temperature, semiconductors can conduct current although they cannot at 0 K. The term "semiconductor" is, thus, slightly misleading, as "not-that-good-of-an-insulator-at-room-temperature" would be more appropriate.

2.1.3 Direct and indirect semiconductors

As explained above, due to the anisotropy of their crystalline structure, the properties of semiconductors are direction-dependent. It is particularly the case for the band structure, which has to be considered in 3 dimensions. Given the symmetries in the crystal structure, the 3D-band structure can be described using dominant wave vectors $\boldsymbol{k}$, representing the momentum of the electron in the reciprocal space. For diamond cubic or zinc-blende structures, the dominant vectors are the null vector $\boldsymbol{k}$=(0,0,0), also called the Γ-valley, the vector perpendicular to a face of the cube $\boldsymbol{k}$=(1,0,0), also called the X-valley, and the vector pointing toward a corner of the cube $\boldsymbol{k}$=(1,1,1), also called the L-valley. The band structures of Si and GaAs along these dominant $\boldsymbol{k}$ vectors are presented in FIGURE 2.2.

As can be seen in FIGURE 2.2, the maximum of the valence band and the minimum of the conduction band are not along the same wave vector $\boldsymbol{k}$ in an indirect semiconductor such as Si while they are along the same wave vector $\boldsymbol{k}$=(0,0,0) in the Γ-valley in the case of a direct semiconductor such as GaAs. As a result, while in

GaAs electrons can easily jump from the valence to the conduction band if they receive an energy higher than the bandgap, this transition cannot directly happen in Si as the momentum ***k*** of the electron needs to be conserved. Thus, interaction with the crystal lattice – in the form of a quasiparticle, called a phonon, representing the collective vibration of atoms in the lattice – is needed to jump over the bandgap. In order to transition from the valence band to the conduction band, an electron needs to absorb energy from a photon and to interact with a phonon so that its momentum is modified toward the right direction. When both conditions are satisfied (high enough energy and right value of the momentum), only then can the electron jump to the conduction band. The semiconductor is therefore called "indirect". This can even lead to negative bandgaps, with the maximum of the valence band being higher than the minimum of the conduction band. It is the case, for example, in diamond cubic Sn, called grey tin or α-tin, and the material is then called a semimetal.

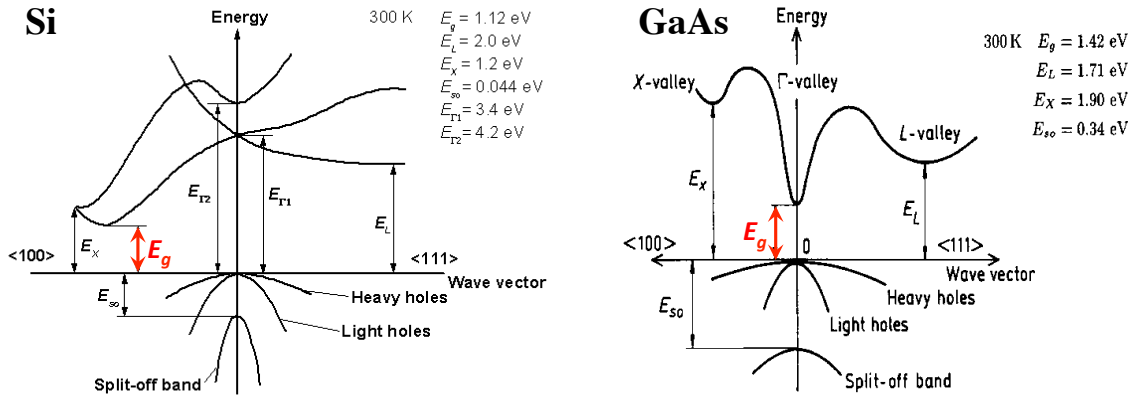

FIGURE 2.2. *Band structure of Si (left) and GaAs (right) in the E-**k** space. The wave vector k represents the momentum of the electron in the reciprocal space. Adapted from Ref. [2.3-2.4]).*

This less than straightforward transition over the bandgap will have two major consequences on the optoelectronic properties of indirect semiconductors. First, light absorption – when a photon is the source of energy provoking the transition of an electron over the bandgap – will be relatively weak in indirect semiconductors such as Si, as a three particle interaction (electron, photon and phonon) is needed. As a result, Si solar cells need to be more than 100 μm-thick to efficiently absorb light while direct bandgap GaAs solar cells can be as thin as 2 μm. Secondly, the opposite

process, called radiative emission – when an electron in the conduction band transitions back to the valence band releasing the excess energy as a photon, and eventually a phonon – will be a much less probable event in indirect bandgap semiconductors, and other sources of non-radiative recombination will dominate. Light emitting devices such as LEDs or lasers are, thereby, mostly made of direct bandgap semiconductors such as GaAs or InP. Another important consequence is that, in the case of indirect semiconductors, electrons in the conduction band will have a much longer radiative lifetime as recombination to the valence band is less probable.

2.1.4 Intrinsic carrier concentration and doping

As explained above, at room temperature semiconductors will naturally have a certain number of electrons thermally excited from the valence band to the conduction band. These electrons will leave a hole behind them in the valence band. Both electrons and holes can travel in the crystal when they are respectively in the conduction and valence band and, therefore, are negative and positive charge carriers. The density of electrons in the conduction band and holes in the valence band are generally noted n and p, respectively. Considering the Boltzmann approximation ($E_g >> k_B T$), the density of electrons in the conduction band and of holes in the valence band can be calculated using the Fermi-Dirac distribution $f(E)$, which describes the probability for an electron to have an energy E, and the equation of the density of state $D(E)$:

$$n = \int_{E_c}^{+\infty} f(E)D(E)dE = N_c e^{-\frac{E_c - E_F}{k_B T}} \tag{2.1}$$

$$p = \int_{0}^{E_v} [1 - f(E)]D(E)dE = N_v e^{-\frac{E_F - E_v}{k_B T}} \tag{2.2}$$

where E_c is the energy level of the minimum of the conduction band, E_v is the energy level of the maximum of the valence band, E_F is the Fermi level, N_c is the effective density of states in the conduction band, N_v is the effective density of states in the valence band, k_B is the Boltzmann constant, and T is the temperature (around 300 K for room temperature). The Fermi level is the highest energy level filled at T=0 K, corresponding, for T>0 K, to an occupation probability of 50 % in the Fermi-Dirac distribution, independently of the density of state $D(E)$. At any given time, under thermal equilibrium, the number of empty states under the Fermi level E_F is exactly

equal to the number of filled states above it. Thus, it represents the "average energy level" of the valence electrons population, also called the chemical potential of the electrons in the considered material.

In a pure, intrinsic, and uncharged semiconductor, as every electron in the conduction band will create a hole in the valence band, both densities will be equal and $n=p=n_i$:

$$n_i = \sqrt{n_i^2} = \sqrt{np} = \sqrt{N_c N_v} e^{-\frac{E_g}{2k_B T}} \tag{2.3}$$

n_i , called the intrinsic carrier concentration, is the density of free electrons and free holes in an intrinsic (pure) semiconductor under thermal equilibrium. Logically, this intrinsic carrier concentration depends mainly on the bandgap and the temperature. In silicon at 300 K, $n_i \approx 10^{10}$ cm^{-3} while the atom density of the crystal is about 10^{22} cm^{-3}. Therefore, the intrinsic carrier concentration is very small and will not yield very good conduction properties. It is also worth noting that the Fermi level lies close to the middle of the bandgap at T=0 K and stays close to there at room temperature.

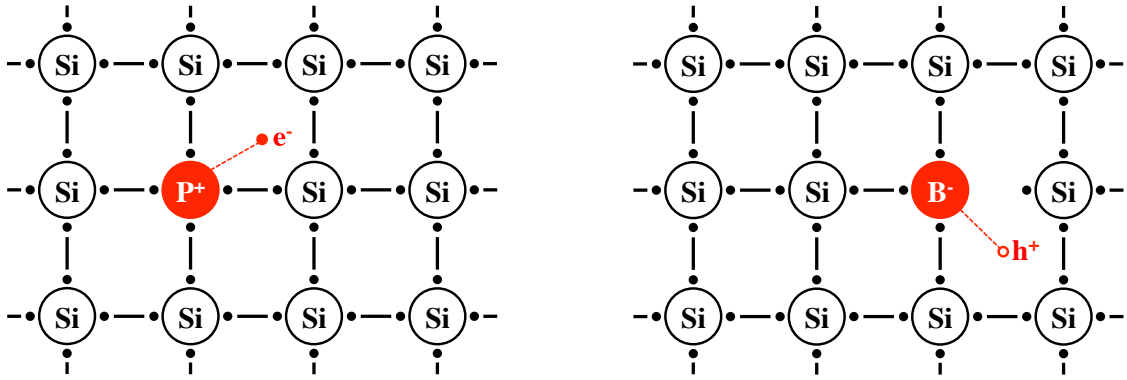

FIGURE 2.3. *2-dimensionnal representation of doping by incorporation of phosphorus (left) to create n-type Si or incorporation of boron (right) to create p-type Si.*

In order to increase the number of charge carriers (free electrons and free holes) under thermal equilibrium, impurities can be added to the crystal in order to add extra free electrons or extra free holes. This is called doping. For example, phosphorus atoms can replace some silicon atoms in a Si crystal. As P has 5 valence electrons, 4 of them will combine with neighbouring Si atoms to form covalent bonds and the last one will be left free, creating an additional negative charge carrier. The crystal will then be a

donor of electrons and will be called phosphorus-doped or n-type Si. Similarly boron, which has 3 valence electrons, can be added in a Si crystal were it will leave a hole, creating a positive charge carrier. The crystal will be an electron acceptor and will be called boron-doped or p-type Si, as detailed in FIGURE 2.3.

The doping density of donor atoms in an n-type semiconductor (P atoms in the case of an Si crystal) is commonly noted N_D. The doping density of acceptor atoms in a p-type semiconductor (B atoms in the case of an Si crystal) is commonly noted N_A. Typically, the doping densities will be much larger than the intrinsic carrier concentration so that the intrinsic carrier concentration will be negligible compared with the doping and, in an n-type semiconductor, $n=n_i+N_D\approx N_D$. Similarly, in a p-type semiconductor $p=n_i+N_A\approx N_A$.

Thermal excitation from room temperature is independent of the doping as long as the doping is not too high. Moreover, thermal equilibrium requires reemission of the absorbed energy. As the emission rate, equal to the absorption rate, is logically linearly dependent on the product $n\times p$, once again independently of the doping, the law of mass action $np=n_i^2$ presented in Equation (2.3) is not only valid for intrinsic semiconductors but also for doped ones. Consequently, in an n-type semiconductor, we have $np=N_D\times p=n_i^2$ and $p=n_i^2/N_D$. Similarly, in a p-type semiconductor $n=n_i^2/N_A$.

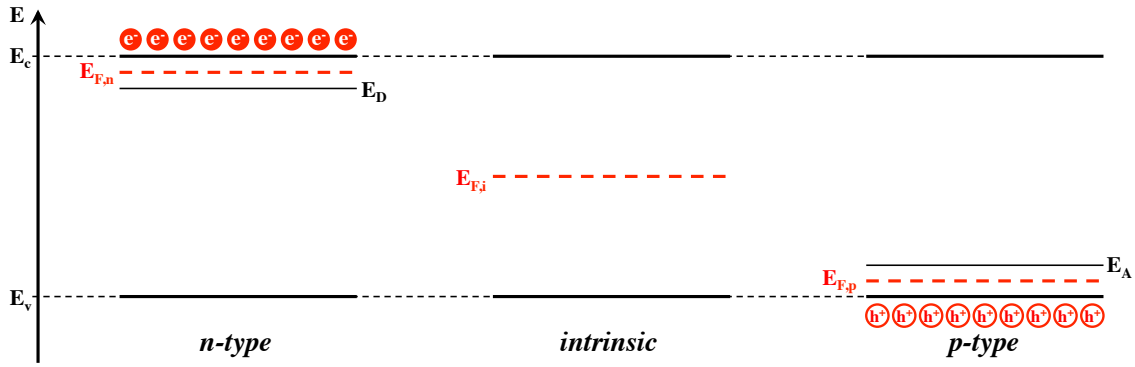

FIGURE 2.4. *Band diagram, impurity levels and Fermi level of highly doped n-type, intrinsic and highly doped p-type semiconductors.*

In a band diagram perspective, the bandgap as well as the maximum/minimum of the valence/conduction band will stay unchanged, all of them being only dependent on

the temperature. However, an extra impurity energy level, corresponding to the additional donors/acceptors from the n/p-doping, will appear close to the conduction/valence band. Thus, the Fermi level will be displaced from the middle of the bandgap. In n-type semiconductors the Fermi level will move upward to sit closer to the new donor impurity energy level E_D. In p-type semiconductors the Fermi Level will move downward to lay closer to the extra acceptors energy level E_A. For highly doped semiconductors, as shown in FIGURE 2.4, the Fermi level lays between the impurity level and the valence/conduction band. The difference of Fermi level between n-type and p-type semiconductors represents the difference of electrochemical potential between the two materials.

2.2 The p-n junction

2.2.1 Movement of charge carriers in semiconductors: diffusion and drift

Under thermal equilibrium, the total current in a homogeneous semiconductor is by definition null. Yet, due to thermal excitation, electrons and holes will have a non-null momentum. As the direction of this momentum is arbitrary and variations of direction following collisions with atoms are random, the average movement of charge carriers is null and, at the macro-level, there is no current.

Organised movement of charge carriers in semiconductors leading to a current can be induced by two phenomena: drift, where an electric field forces charge carriers into a particular direction; and diffusion, where a non-homogenous concentration of carriers will tend to homogenise thanks to the constant random movement of carriers discussed above.

Drift caused by an electric field is described by the Drude model, developed for metals but also valid for semiconductors. In this model, the acceleration of carriers due to the electric field is counterbalanced by a resistive force of friction due to collisions between electrons/holes and the surrounding atoms. The current then easily derives from the equilibrium speed of the carriers:

$$\overrightarrow{J_{drift,n}} = q\vec{v}_{th,n}n = \frac{q^2\tau_{coll,n}}{m_n^*}n\vec{E} = q\mu_n n\vec{E} \tag{2.4}$$

$$\overrightarrow{J_{drift,p}} = q\vec{v}_{th,p}p = \frac{q^2\tau_{coll,p}}{m_p^*}p\vec{E} = q\mu_p p\vec{E} \tag{2.5}$$

with q the elementary charge, E the electric field, $J_{drift,n/p}$ the drift current of electrons/holes, $v_{th,n/p}$ their equilibrium speed, $m^*_{n/p}$ their effective mass, $\tau_{coll,n/p}$ the mean free time between two collisions for the type of carriers considered, and $\mu_{n/p}=q\tau_{coll,n/p}/m^*_{n,p}$ the electron/holes mobility. Thus, the Ohm's law is verified with the direct proportionality between the current and the electric field.

In the case of diffusion, the classic diffusion equation associated with a gradient of concentration gives the flux $\phi_{n/p}$ of charge carriers:

$$\overrightarrow{\Phi_n} = -D_n\vec{\nabla}n \tag{2.6}$$

$$\overrightarrow{\Phi_p} = -D_p\vec{\nabla}p \tag{2.7}$$

where $D_{n/p}$ is the diffusion coefficient of electrons/holes. The diffusion current due to electrons/holes is then given by $J_{diff,n/p}=\pm q\phi_{n/p}$ depending on the charge of the carriers considered. The total current due to electrons/holes is, thus:

$$\overrightarrow{J_n} = \overrightarrow{J_{drift,n}} + \overrightarrow{J_{diff,n}} = q\mu_n n\vec{E} + qD_n\vec{\nabla}n \tag{2.8}$$

$$\overrightarrow{J_p} = \overrightarrow{J_{drift,p}} + \overrightarrow{J_{diff,p}} = q\mu_p p\vec{E} - qD_p\vec{\nabla}p \tag{2.9}$$

Under thermal equilibrium, both currents are null so that $J_n=J_p=0$, giving:

$$q\mu_n n\vec{E} = -qD_n\vec{\nabla}n \tag{2.10}$$

$$q\mu_p p\vec{E} = qD_p\vec{\nabla}p \tag{2.11}$$

Thus, under thermal equilibrium, an electric field will create a gradient of density and, reciprocally, a gradient of carrier concentration will create an electric field: both a diffusion and a drift current will appear and balance each other.

Moreover, considering that the electric field derives from a potential V, we have:

$$\frac{\mu_n}{D_n}\vec{\nabla}V = \frac{\vec{\nabla}n}{n} \tag{2.12}$$

$$\frac{\mu_p}{D_p}\vec{\nabla}V = -\frac{\vec{\nabla}p}{p} \tag{2.13}$$

As this potential V moves the conduction and valence bands by a quantity $-qV$, Equations (2.1-2.2) become:

$$n = N_c e^{-\frac{E_c - qV - E_F}{k_B T}} \tag{2.14}$$

$$p = N_v e^{-\frac{E_F - E_v + qV}{k_B T}} \tag{2.15}$$

Equations (2.12-2.13) can then be rewritten:

$$\frac{\mu_n}{D_n}\vec{\nabla}V = \frac{1}{n}\vec{\nabla}n = \frac{1}{n}\vec{\nabla}\left(N_c e^{-\frac{E_c - qV - E_F}{k_B T}}\right) = \frac{1}{n}\frac{k_B T}{q}\vec{\nabla}V \times \left(N_c e^{-\frac{E_c - qV - E_F}{k_B T}}\right) = \frac{k_B T}{q}\vec{\nabla}V \tag{2.16}$$

$$\frac{\mu_p}{D_p}\vec{\nabla}V = -\frac{1}{p}\vec{\nabla}p = -\frac{1}{p}\vec{\nabla}\left(N_v e^{-\frac{E_F - E_v + qV}{k_B T}}\right) = \frac{1}{p}\frac{k_B T}{q}\vec{\nabla}V \times \left(N_v e^{-\frac{E_F - E_v + qV}{k_B T}}\right) = \frac{k_B T}{q}\vec{\nabla}V \tag{2.17}$$

As a result, we obtain the Einstein relation for semiconductors:

$$\mu_n = D_n \frac{k_B T}{q} \tag{2.18}$$

$$\mu_p = D_p \frac{k_B T}{q} \tag{2.19}$$

2.2.2 The p-n junction under thermal equilibrium

A p-n junction is a semiconductor structure with a very sharp transition from an n-type region to a p-type region. We consider the transition to be so abrupt that it is immediate: at x=0, doping densities shift at once from $N_A >> n_i$ and N_D=0 for x<0 (p-type region) to $N_D >> n_i$ and N_A=0 for x>0 (n-type region).

As shown previously in FIGURE 2.4, because the density of electrons and holes are different on both sides of the interface, the two regions have different electrochemical potentials represented by different Fermi levels. As it is, the system is not in thermal equilibrium and the carrier density gradient at x=0 is infinite. Therefore, the system will transition toward equilibrium through diffusion of carriers across the interface. Free electrons will migrate from the n-region to occupy acceptors in the p-region and,

reciprocally, free holes will migrate from the p-region to occupy donors in the n-region, creating a diffusion current, as shown in FIGURE 2.5.

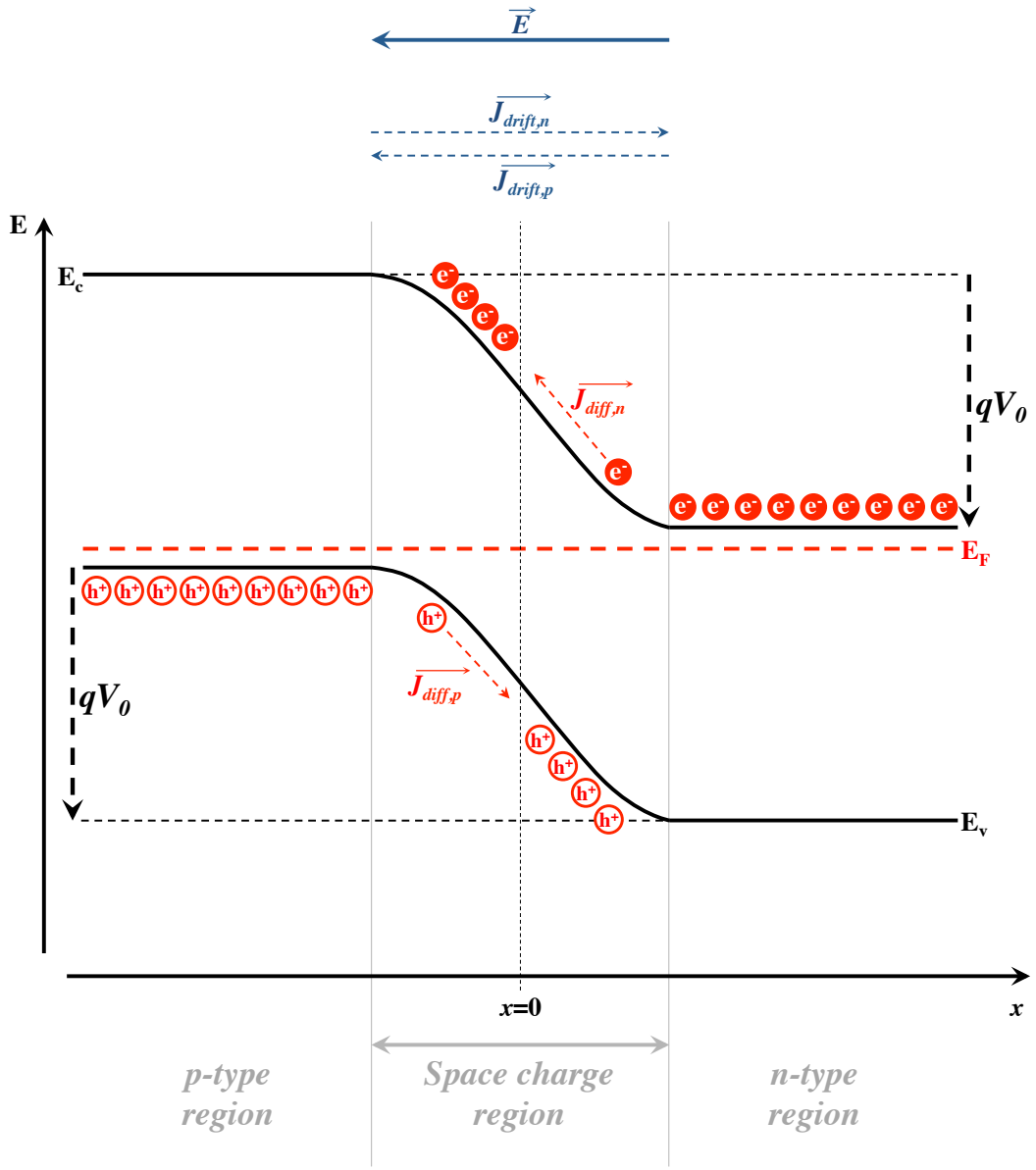

FIGURE 2.5. *Band diagram of a p-n junction under thermal equilibrium representing the diffusion current of holes and electron, the resulting electric field $\vec{E}$ and the subsequent drift current and band bending.*

By doing so, positive charges will accumulate close to the interface on the n-side and negative charges will accumulate close to the interface on the p-side, breaking the local electric neutrality and, thus, inducing an electric field and consequently a drift current. At thermal equilibrium, the drift and diffusion currents will equilibrate,

verifying Equations (2.10-2.11). The resulting difference of potential across the junction due to the built-in electric field V_0 will shift the conduction and valence bands on one side of the junction so that the Fermi level is constant across the interface.

The region around the interface, where the electric neutrality is broken because of excess electrons/holes, is called the space charge region. The electron density n in the n-type region of this space charge region will be extremely low, as nearly all the electrons will have migrated to the p-type region. There, they will recombine by ionizing the acceptors so the electron density n will also be low. Reciprocally, the density of free holes p will be very low across the space charge region. Consequently, the space charge region is depleted from its carriers with $n \approx p \approx n_i$. The space charge region is, thereby, sometimes called the depletion zone. Outside the space charge region the potential is quasi-constant and these zones are called quasi-neutral regions.

2.2.3 The p-n junction under bias

If an external voltage V_{ext} is applied to the junction, the thermal equilibrium will be broken and the Fermi levels will be different on both side of the p-n junction. As a result, a current will flow through the junction. Depending on the sign of the applied voltage, the carriers will react very differently, causing the current to react non-linearly to the external voltage. Two cases are possible: reverse bias and forward bias.

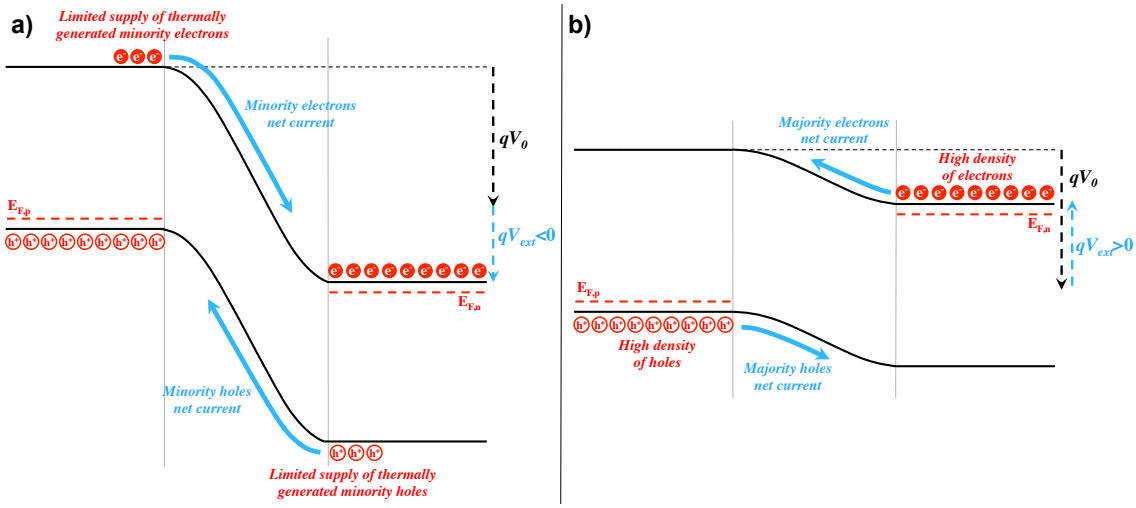

FIGURE 2.6. *Band diagram of a p-n junction reverse (a) and forward (b) bias.*

As shown in FIGURE 2.6a), under reverse bias, the external voltage V_0 and the built-in voltage V_{ext} are of the same sign. Consequently, the field across the space charge region will increase, opposing the diffusion of majority carriers (electrons in the n-region and holes in the p-region) through the junction. Thus, the diffusion current will be reduced and, at high reverse voltage, the only carriers able to cross the p-n interface will be the minority carriers (electrons in the p-region and holes in the n-region) thermally excited at the edge of the space charge region and swept through it by the electric field. As the densities of minority carriers are very small ($n=n_i^2/N_A$, $p=n_i^2/N_D$), most of them will drift through the junction even with a relatively small reverse bias voltage and, thus, the current will be mostly independent of the voltage and reach a limit current, called the saturation current. This saturation current is directly proportional to the minority carrier densities and, therefore, is very small.

Under forward bias, illustrated in FIGURE 2.6b), the external voltage V_0 and the built-in voltage V_{ext} are of different signs. The net electric field across the space charge region is subsequently decreased. As a result, the diffusion of majority carriers is less impeded and the diffusion current will take over the drift current. The carriers diffusing across the space charge region will become minority carriers and will recombine at a fast rate with majority carriers provided by the external circuit. Contrary to the reverse bias case, this time the number of carriers available for transport is very high and, at moderate external voltages (smaller than the built-in voltage), the current will respond very strongly to variations in voltage. Thus, a small voltage will create a very high current.

2.2.4 General equations of the p-n junction

Under equilibrium, with a built-in potential V_0 across the junction, Equation (2.14) for electrons becomes:

$$n = N_D = N_c e^{-\frac{E_C - E_F}{k_B T}} \text{ in the n-type region} \tag{2.20}$$

$$n = \frac{n_i^2}{N_A} = N_c e^{-\frac{E_C + qV_0 - E_F}{k_B T}} = N_D e^{-\frac{qV_0}{k_B T}} \text{ in the p-type region} \tag{2.21}$$

Similarly, for holes, Equation (2.15) becomes:

$$p = N_A = N_v e^{-\frac{E_F - E_C}{k_B T}} \text{ in the p-type region} \tag{2.22}$$

$$p = \frac{n_i^2}{N_D} = N_v e^{-\frac{E_F - E_V + qV_0}{k_B T}} = N_A e^{-\frac{qV_0}{k_B T}} \text{ in the n-type region} \tag{2.23}$$

Both equations give the value of the built-in voltage V_0, which can be further derived using Equation (2.3):

$$V_0 = \frac{k_B T}{q} ln\left(\frac{N_A N_D}{n_i^2}\right) = \frac{E_g}{q} + \frac{k_B T}{q} ln\left(\frac{N_A N_D}{N_c N_v}\right) \tag{2.24}$$

When a moderate external voltage V_{ext} is applied on top of the built-in voltage V_0, as the diffusion and drift current in the space charge region are extremely large, the current induced by the external voltage can be neglected in Equations (2.8-2.9) and Equations (2.10-2.11) are still mostly verified. Equations (2.21) and (2.23), describing the minority carrier concentrations at both edges of the space charge region, then become:

$$n = N_D e^{-\frac{q(V_0 - V_{ext})}{k_B T}} = \frac{n_i^2}{N_A} e^{\frac{qV_{ext}}{k_B T}} \text{ in the p-type region} \tag{2.25}$$

$$p = N_A e^{-\frac{q(V_0 - V_{ext})}{k_B T}} = \frac{n_i^2}{N_D} e^{\frac{qV_{ext}}{k_B T}} \text{ in the n-type region} \tag{2.26}$$

As the density of majority carriers are still mostly equal to the doping densities ($n \approx N_D$ in the n-type region, $p \approx N_A$ in the p-type region), the law of mass action, verified everywhere in the semiconductor, becomes:

$$np = n_i^2 e^{\frac{qV_{ext}}{k_B T}} \tag{2.27}$$

If we now define Δn and Δp as the excess minority carrier concentrations induced by the external voltage, we obtain:

$$\Delta n = n(V_{ext}) - n(0) = \frac{n_i^2}{N_A}\left(e^{\frac{qV_{ext}}{k_B T}} - 1\right) \tag{2.28}$$

$$\Delta p = p(V_{ext}) - p(0) = \frac{n_i^2}{N_D}\left(e^{\frac{qV_{ext}}{k_B T}} - 1\right) \tag{2.29}$$

Depending on the sign of V_{ext}, the excess minority concentration will represent an injection of carriers to be recombined ($V_{ext}>0$) or an extraction of generated carriers ($V_{ext}<0$). More precisely, the voltage-independent part of the equation corresponds to

the density of thermally excited minority carriers that will be swept from the edge of the space charge region by the net electric field. Thus, it is a drift current. The voltage-dependent part of the equation corresponds to majority carriers diffusing through the space charge region and recombining as they exit it and become minority carriers. Hence, it is a diffusion current.

As these excess carriers are minority carriers, they will quickly recombine with majority carriers supplied by the external circuit. If we note $\tau_{n/p}$ their lifetime and $L_{n/p}$ their associated diffusion length, diffusion laws give us that, between t and $t+\tau_{n/p}$, minority carriers will have on average travelled a distance $L_{n/p}$. Subsequently the electrons and holes currents through the junction are:

$$J_n = q\Delta n \frac{L_n}{\tau_n} = qn_i^2 \frac{L_n}{\tau_n N_A}\left(e^{\frac{qV_{ext}}{k_B T}} - 1\right) \tag{2.30}$$

$$J_p = q\Delta p \frac{L_p}{\tau_p} = qn_i^2 \frac{L_p}{\tau_p N_D}\left(e^{\frac{qV_{ext}}{k_B T}} - 1\right) \tag{2.31}$$

According to diffusion laws $L_{n/p}=\sqrt{(D_{n/p}\tau_{n/p})}$, so that the total current through the junction is:

$$J(V_{ext}) = J_n + J_p = qn_i^2\left(\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}\right)\left(e^{\frac{qV_{ext}}{k_B T}} - 1\right) = J_0\left(e^{\frac{qV_{ext}}{k_B T}} - 1\right) \tag{2.32}$$

J_0 is clearly the saturation current defined in section 2.2.3 and is the limiting current of a p-n junction under reverse bias.

Although this simple model describes pretty well silicon p-n junction diodes, it only considers one source of recombination, namely Shockley-Read-Hall (SRH) recombination at the edge of the space charge region due to doping impurities, and omits other important sources of recombination such as radiative recombination (very important for III-V LEDs), Auger recombination, or SRH recombination due to other types of defects. Moreover, using this model, the performance of the diode can be virtually unlimited just by adjusting the doping levels, something that is physically impossible for evident reasons. Sections 2.3-2.4 answer this inconsistency by introducing additional sources of recombination, in particular radiative recombination, which define the limiting performance of the diode, LED, or solar cell considered.

2.3 The photovoltaic effect and solar cell operation

2.3.1 The photovoltaic effect

A classic p-n photovoltaic solar cell is a p-n junction optimised to harvest photogenerated carriers under sunlight radiation. The thermal equilibrium and bias conditions presented in Section 2.2 correspond to a diode in a radiative equilibrium: the diode is at room temperature and the only radiation received from the surrounding blackbody environment is balanced by the cell's own blackbody emission. Hence, the only source of energy to break the thermal equilibrium is the external voltage applied to the cell.

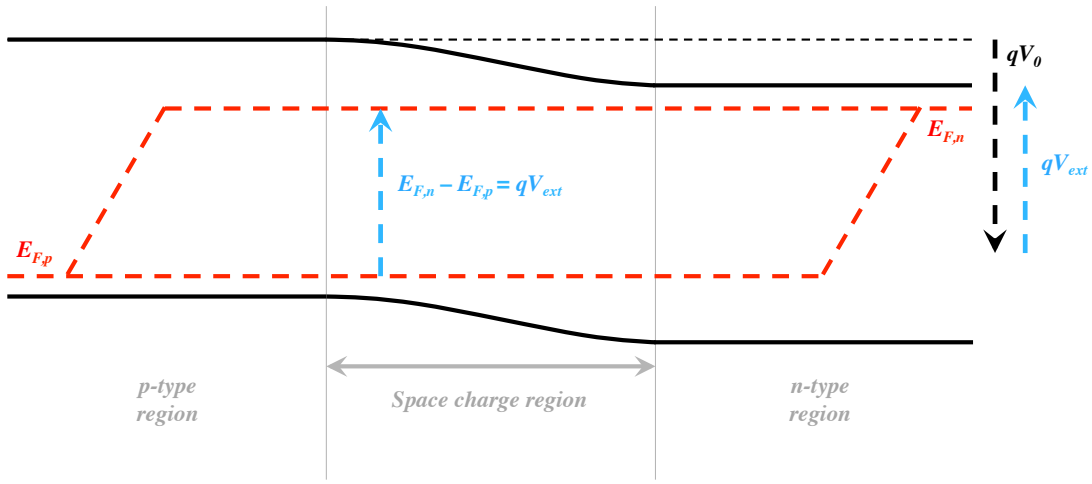

FIGURE 2.7. *Band diagram of a p-n junction under illumination in open-circuit conditions (J=0), showing the splitting of the Fermi level into distinct quasi-Fermi levels for electrons ($E_{F,n}$) and holes ($E_{F,p}$). On each side, recombination with free carriers from the electrodes leads to the quasi-Fermi levels merging back together.*

However, when the diode is immersed in an external radiation such as sunlight, photons with an energy higher than the diode bandgap will provide enough energy for electrons in the valence band to jump to the conduction band and, thus, create free electron/hole pairs. This will split the Fermi levels in the entire device, with electron and holes having different quasi-Fermi levels, as shown in FIGURE 2.7. Because of the difference in conductivities between the n-type and p-type regions, due to the difference in electrons/holes concentrations, electrons and holes are selectively

transported to their respective electrode [2.5]. Carriers generated close enough to the space charge region will, thus, be separated and preferentially driven in opposite directions, consequently participating in the total current. As the quasi-Fermi level of electrons is higher than the quasi-Fermi level of holes, the difference of free energy $E_{F,n}-E_{F,p}=qV_{ext}$ between carriers collected on both sides of the junction is positive and power is produced by harvesting them.

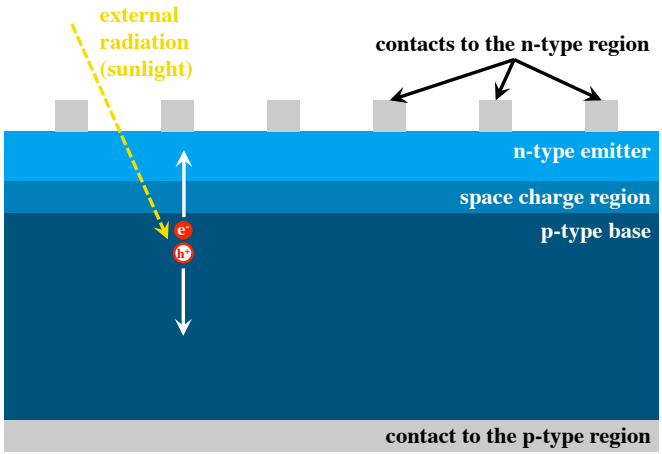

FIGURE 2.8. *Structure of a classic p-n photovoltaic solar cell.*

Photovoltaic solar cells are usually made of a thin highly doped n-region called the emitter, by reference to the similar structure used in LEDs, and a thicker p-type region called the base, as shown in FIGURE 2.8. Light is absorbed from the top surface (n-type emitter). On the emitter side, the contact is usually a metal grid to reduce shadowing. Transparent conductive materials, such as Indium Tin Oxide (ITO), can also be used as a front contact. However, achieving the optimal trade-off between conductivity and transparency over the full absorption spectrum of the cell is challenging. As a result, the use of such materials is in practice limited to cells with limited lateral conductivity. On the base side a full metallisation is typically used. Cells with an n-type base and a p-type emitter exist too.

2.3.2 Light absorption in a semiconductor and photocurrent generation

In order to participate in the photocurrent J_{ph}, photogenerated electrons and holes need to be separated – as a result of the difference of electron and hole conductivities

between the n-type and p-type regions [2.5] – and collected. More precisely, carriers will be harvested if they are generated at a distance z from the space charge region smaller than the diffusion length $L_{n/p}$. Considering a uniform generation rate G and defining the width W_D of the depletion zone we have:

$$J_{ph} = q \int_{L_n+W_D+L_p} G dz = qG\left(L_n + W_D + L_p\right) \tag{2.33}$$

In the case of solar cells with thin base/emitters or large diffusion lengths so that, with a p-type base and an n-type emitter, $L_p > W_{base}$ and/or $L_n > W_{emit}$, with $W_{base/emit}$ the thickness of the quasi-neutral region in the base/emitter, the photocurrent becomes logically $J_{ph}=qG(W_{emit}+W_D+W_{base})=qGL$ with L the thickness of the cell.

In practice, the generation rate is not uniform and depends on the distance x into the material and the wavelength λ. It is determined by the wavelength-dependent absorption coefficient $\alpha(\lambda)$ of the material using the classic relation:

$$G(z,\lambda) = \alpha(\lambda)\Phi_{0,\lambda}e^{-\alpha(\lambda)z} \tag{2.34}$$

where $\phi_{0,\lambda}$ is the photon flux with a wavelength λ at the surface of the cell. Consequently, the photocurrent is:

$$J_{ph} = q \int_{L_n+W+L_p} \int_{0}^{+\infty} G(z,\lambda) d\lambda dz = q \int_{0}^{+\infty} \Phi_{0,\lambda}\left(1 - e^{-\alpha(\lambda)\left(L_n+W_D+L_p\right)}\right) d\lambda \tag{2.35}$$

The absorption coefficient $\alpha(\lambda)$ is directly related to the wavelength-dependent optoelectronic properties of the semiconductor. A simple approach consists in considering the absorption null for photons with energy lower than the bandgap ($\alpha(\lambda)=0$ for $\lambda > hc/E_g$) and infinite for photons with energy higher than the bandgap ($\alpha(\lambda)=+\infty$ for $\lambda < hc/E_g$), where h is the Planck constant and c the speed of light in vacuum. We therefore have, with $E=hc/\lambda$ the energy of the considered photon:

$$J_{ph} = q \int_{0}^{\frac{hc}{E_g}} \Phi_{0,\lambda} d\lambda = q \int_{E_g}^{+\infty} \Phi_{0,E} dE \tag{2.36}$$

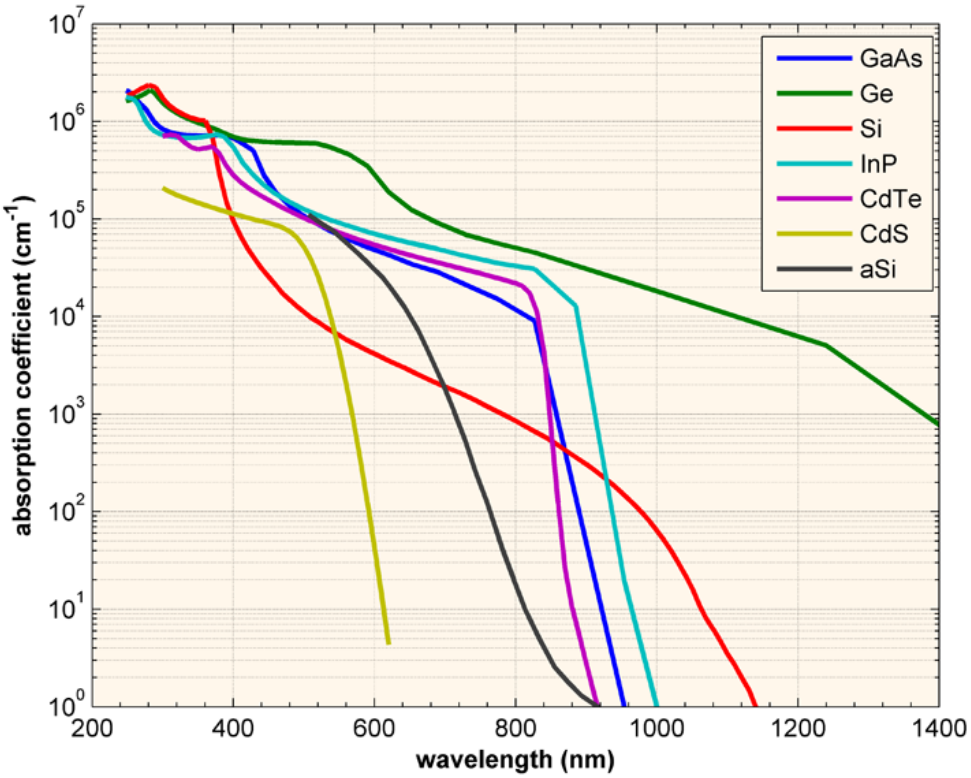

FIGURE 2.9. *Wavelength-dependent absorption coefficient of a range of usual semiconductors. Reprint from Ref. [2.6].*

This approximation is valid for thick cells with very long diffusion lengths but does not fully describe the case of thin cells. Indeed, photons with energy slightly above the bandgap will only be able to interact with electrons already very close to the valence band edge, which are in restricted density. Therefore, the absorption of these near-bandgap photons is limited and the absorption coefficient $\alpha(\lambda)$ is strongly related to the band structure for $\lambda \approx hc/E_g$. This is apparent in FIGURE 2.9, with stark differences between direct semiconductors (GaAs, InP…), indirect semiconductors (c-Si, Ge…) –for which absorption of photons and charge carrier generation involve interaction with phonons – and amorphous semiconductors (a-Si). Moreover, below bandgap absorption is possible for a range of reasons such as impurities or temperature-induced disorder in the crystal. As a result, absorption decreases exponentially below the bandgap, in an Urbach tail, instead of dropping at once to zero. Equation (2.35), using experimentally determined values for the absorption coefficient, is therefore the best way to calculate the potential photocurrent of a solar cell. Absorption coefficients do not depend on light polarisation because of the

symmetries in the crystalline lattice of classic photovoltaic materials. Moreover, the almost all of sunlight energy consists of its direct component, which is unpolarised. As a result, polarisation is generally neglected in photovoltaic science and engineering.

In application of the superposition principle [2.7], this generated photocurrent will add to the dark current equation from Equation (2.32) and, switching to generator convention, the diode equation becomes:

$$J(V) = J_{ph} + J_0 \left(1 - e^{\frac{qV}{k_B T}}\right) \tag{2.37}$$

Therefore, there will be a current through the cell in short-circuit at V=0. This short-circuit current, noted J_{sc}, will be equal to the photocurrent J_{ph} in the approximation of no recombination under short-circuit conditions. Moreover, the diode will generate a positive power for P=J×V>0, and hence for 0<V<V_{oc}; with the open-circuit voltage V_{oc} defined as:

$$V_{oc} = \frac{k_B T}{q} ln\left(\frac{J_{sc}}{J_0} - 1\right) \tag{2.38}$$

2.3.3 Photovoltage across a p-n junction under illumination

As explained above in Section 2.3.2, photons with energy greater than the bandgap are absorbed and generate an electron in the conduction band and a hole in the valence band. The difference of energy between the two particles is initially equal to the energy absorbed from the photon, and eventually the associated phonon. However, as there is a continuum of accessible energy states between the energy level of the electron/hole and the miniumum of the conduction band/maximum of the valence band, the particles will lose energy to the crystal lattice, emitting single phonons, until the lowest accessible state in the conduction band/highest accessible state in the valence band is reached. In this process, called thermalisation, the excess energy is lost to the crystal lattice in the form of heat carried by the phonons and, in a first approximation, the energy of the electron-hole pair is close to the bandgap E_g of the material. As this process is faster by orders of magnitude than the extraction of carriers, this excess energy cannot be recovered with classic devices.

In open-circuit conditions, at J=0, the carriers in the cell are in dynamic equilibrium and the quasi-Fermi levels of electrons and holes are nearly constant across the device, as illustrated in FIGURE 2.7. The open-circuit voltage V_{oc} introduced earlier is consequently equal to the difference of potential between the quasi-Fermi levels of electrons and holes. Hence, the V_{oc} of a cell directly represents the pseudo-equilibrium under illumination.

As photo-generated carriers thermalise very quickly to the conduction and valence band edges, the upper limit for $q \times V_{oc}$ will be the bandgap E_g of the cell. However, in practice, $q \times V_{oc}$ is lower than E_g, usually by about 0.4 eV for the best Si cells [2.8-2.10] with the best GaAs solar cells reaching 0.3 eV [2.10-2.11]. This is related to the production of entropy in the photovoltaic process, caused by an increase in the disorder of the directions of photons and the associated loss of information. Indeed, photons coming from the sun will enter the cell with a limited distribution of direction. At $V=V_{oc}$ all the generated carriers will recombine so that J=0. These recombinations will lead to a loss of information on the original direction of incoming photons and, thus, to a production of entropy. In the best-case scenario, all of the photons will be reemitted through radiative recombination, limiting the entropy creation. However, these photons will still be reemitted in random directions and the information about their original direction will be lost, leading to the irreversibility of the process. As a result, the V_{oc} can be approximated by:

$$V_{oc} \approx \frac{E_g}{q} + \frac{k_B T}{q} ln\left(\frac{\Omega_{sun}}{\Omega_{emis}}\right) \tag{2.39}$$

where Ω_{sun} is the solid angle of the sun and Ω_{emis} is the solid angle under which photons are reemitted. In a basic solar PV cell $\Omega_{emis}=4\pi$ str but, using a highly reflective back mirror, $\Omega_{emis}=2\pi$ str can be approached. Concentration systems also enable a decrease in the value of Ω_{emis} and, hence, an increase in V_{oc}. Using a terrestrial PV cell with a back mirror, $\Omega_{sun}=6.83\times10^{-5}$ str and $\Omega_{emis}=2\pi$ str, so the bandgap-V_{oc} offset will be at minimum 0.29 V, in strong agreement with the best GaAs cells [2.10-2.11].

For cells where non-radiative recombination is the dominant recombination process, the V_{oc} will be further reduced, as the information on the system is decreased and,

thus, the entropy production rate is increased with random non-radiative recombination. As a result, Equation (2.39) becomes:

$$V_{oc} \approx \frac{E_g}{q} + \frac{k_B T}{q} ln\left(\frac{\Omega_{sun}}{\Omega_{emis}}\right) + \frac{k_B T}{q} ln(\eta_{ext}) \tag{2.40}$$

with η_{ext} the external luminescent efficiency of the cell, defined as the ratio of the radiative emission rate of the cell R_{rad} on the total recombination rate $R=R_{rad}+R_{non\text{-}rad}$, with $R_{non\text{-}rad}$ the non-radiative recombination rate, so that:

$$\eta_{ext} = \frac{R_{rad}}{R} = \frac{R_{rad}}{R_{rad} + R_{non-rad}} \tag{2.41}$$

2.3.4 Solar cells operation

Using the ideal diode Equation (2.37), the current density-voltage characteristic and the power density-voltage curve of an ideal high efficiency silicon photovoltaic solar cell are presented in FIGURE 2.10.

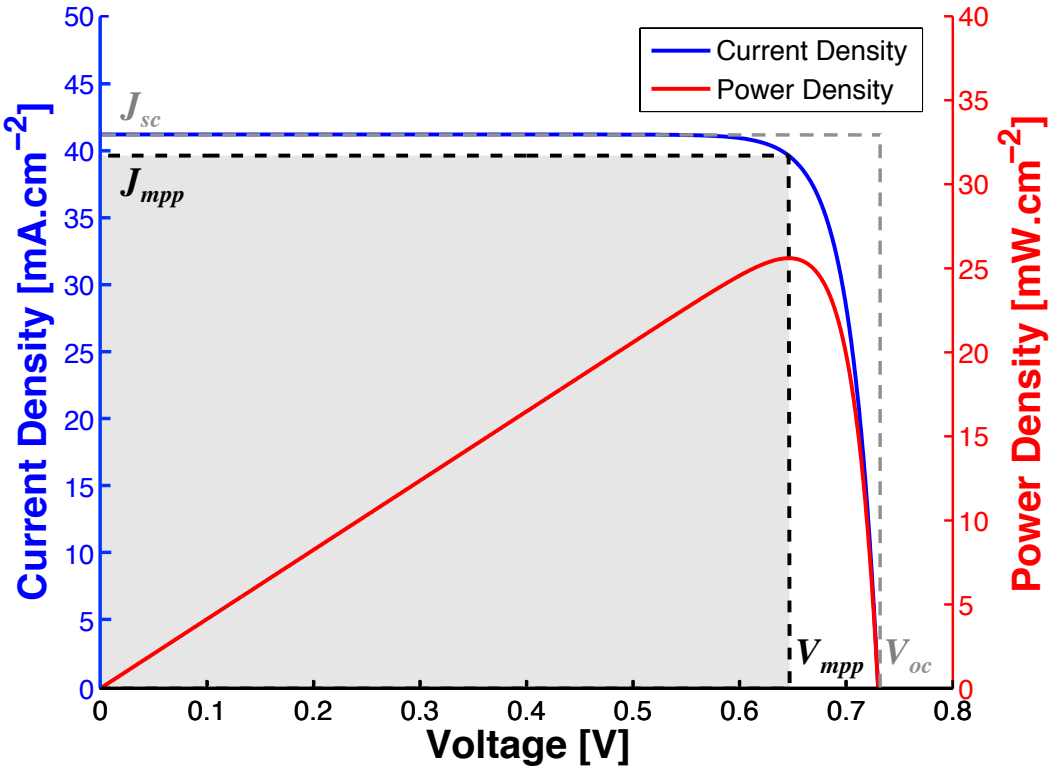

FIGURE 2.10. *Current density-voltage characteristic (blue – left scale) and power density-voltage curve (red – right scale) of a high efficiency Si solar cell.*

The current density is relatively flat for low voltages (up to 0.5 V) and decreases rapidly when the voltage approaches the V_{oc}. As a result, the power density of the cell will increase steadily with the voltage up to a maximum before quickly falling. A voltage and a current density can be associated with this Maximum Power Point (MPP). Hence, we can define the maximum power point voltage V_{mpp} and the maximum power point current density J_{mpp}, both of them represented in black dashed lines in FIGURE 2.10. The maximum power density of the PV cell is, therefore, $P_{mpp}=V_{mpp}\times J_{mpp}$ and we can define its efficiency as $\eta=P_{mpp}/P_{in}=V_{mpp}\times J_{mpp}/P_{in}$, where P_{in} is the incoming power on the surface of the cell.

Another important metric for PV cells is the fill factor FF. The fill factor is defined as $FF=P_{mpp}/(V_{oc}\times J_{sc})=(V_{mpp}\times J_{mpp})/(V_{oc}\times J_{sc})$. Geometrically, it is the ratio between the two squares delimited by black and grey dashed lines in FIGURE 2.10, with the grey filled area representing the maximum power P_{mpp}. Therefore, the fill factor is a metric of the "squareness" of the J-V characteristic and, at V_{oc} and J_{sc} fixed, the higher the FF will be, the higher the maximum power P_{mpp} and consequently the efficiency η will be. Although ideal PV cells behaving according to Equation (2.37) will have a fill factor mainly related to their V_{oc}; non-ideal processes such as non-radiative recombination in the depletion zone, high series resistance or low shunt resistances will decrease the fill factor and, hence, the efficiency without necessarily impacting the V_{oc} and J_{sc}. This is presented in more detail in Section 2.4.1.

2.4 Losses, efficiency limits and multijunction solar cells

2.4.1 Sources of losses in solar cells

Sources of losses in solar cells can be divided in two categories: intrinsic losses, inherent to the photovoltaic effect and semiconductor materials and, thus, unavoidable; and extrinsic losses, related to unoptimised cell structures or fabrication processes and reducible to some extent.

a) Intrinsic losses

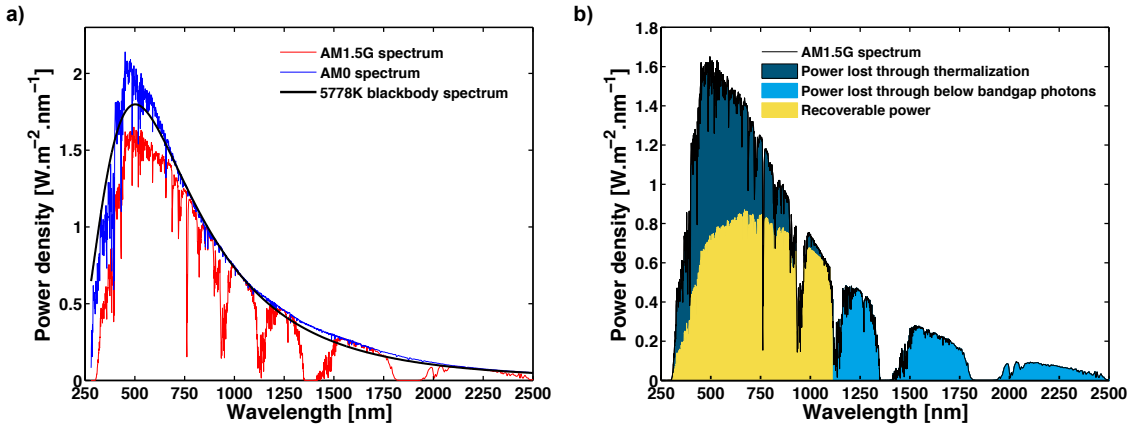

FIGURE 2.11. a) *AM0 (blue), AM1.5G (red) and 5778 K blackbody (black) spectrums.* ***b)*** *Detail of the losses due to thermalisation (dark blue), unabsorbed below bandgap photons (light blue) and recoverable power (yellow) by a crystalline silicon PV cell on AM1.5G spectrum*

The main source of intrinsic loss in solar cells is inherent to the photovoltaic effect: as photons with energy below the bandgap are not absorbed and photons with energy above the bandgap get their excess energy thermalised, a sizable portion of the solar spectrum is not exploited. Indeed, the sun can be approximated by a blackbody source at 5778 K. As a result, the solar spectrum spans from about 250 nm to more than 4000 nm with a long exponential tail. FIGURE 2.11a) shows the perfect black body at 5778 K, the measured AM0 spectrum – corresponding to the real solar spectrum in space in orbit around Earth – and the AM1.5G spectrum – corresponding to the solar spectrum on Earth when the solar zenith angle equals 48.2 °. The AM0 spectrum in space closely matches the 5778 K-blackbody spectrum. However, the Earth surface AM1.5G spectrum presents multiple gaps due to absorption bands of the atmosphere, in particular water vapour absorption. FIGURE 2.11b) shows, on AM1.5G, which portion of the spectrum is recoverable using a crystalline Si solar cell, which portion is lost through thermalisation of the above bandgap energy and which portion is lost because of unabsorbed below bandgap photons. Losses due to below bandgap photons represent about 19 % and losses due to thermalisation represent about 32 %. Hence, the recoverable power of a c-Si PV cell represents only about 49 % of the incoming power.

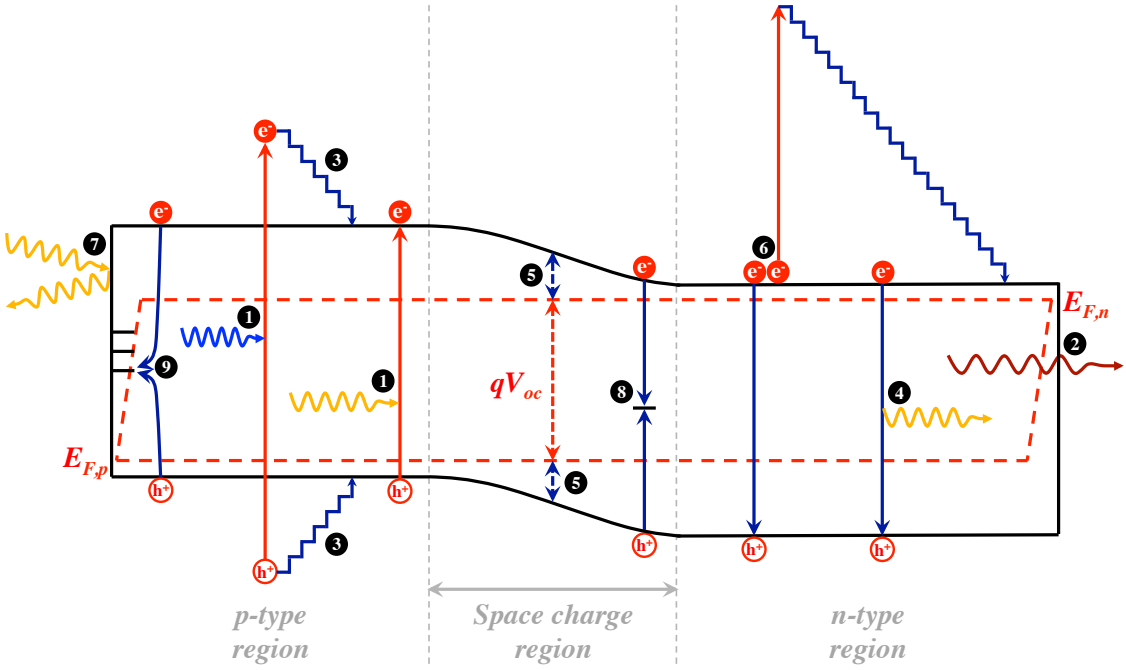

FIGURE 2.12. *Generation, recombination and other sources of losses in p-n junction photovoltaic solar cells:* ***1)*** *electron-hole pair generation through above bandgap photon absorption,* ***2)*** *unabsorbed below bandgap (deep infrared) photons,* ***3)*** *thermalisation of excess energy for high energy (blue) photons,* ***4)*** *radiative recombination,* ***5)*** *loss of energy related to entropy production due to the asymmetry between mono-directional light absorption and isotropic light reemission,* ***6)*** *Auger recombination,* ***7)*** *reflection of incoming photons on the front surface,* ***8)*** *SRH recombination on a bulk defect,* ***9)*** *surface SRH recombination.*

Losses due to non-absorbed below bandgap photons and thermalisation of above bandgap photons are represented in FIGURE 2.12, processes 2) and 3).

A second source of intrinsic loss has already been described: it is the loss of energy related to entropy production when the cell reemits photons isotropically at V_{oc}. Due to this entropy production, the separation between the quasi Fermi levels of electrons $E_{F,n}$ and $E_{F,p}$ holes is smaller than the bandgap, as shown in FIGURE 2.12-5). Indeed, radiative recombination, shown in FIGURE 2.12-4), is an unavoidable source of recombination as free carriers have a limited lifetime and will radiatively recombine without assistance of crystal defects when an electron encounters a hole. In the best-case scenario, all recombination will, thereby, be radiative. The radiative

recombination rate can be quantified from the absorption spectrum of the cell. Indeed, in the dark at room temperature and without non-radiative recombination, the thermal equilibrium in the cell imposes that radiative emission exactly balances the absorption from the surrounding blackbody environment. Peter Würfel has shown [2.12] that the radiative recombination rate $R_{rad,dark}$ under thermal equilibrium is equal to:

$$R_{rad,dark} = \int_0^{+\infty} \frac{2\pi a(E)E^2}{h^3c^2} e^{-\frac{E}{k_BT}} dE = \int_0^{+\infty} \frac{2\pi c a(\lambda)}{\lambda^4} e^{-\frac{hc}{\lambda k_BT}} d\lambda \qquad (2.42)$$

where $a(\lambda)$ is the wavelength-dependent absorptivity of the cell, determined by its absorption coefficient $\alpha(\lambda)$ and its geometry. As the radiative recombination rate is directly proportional to the product $n \times p/n_i^2 = exp(qV/k_BT)$, the voltage-dependent radiative recombination rate is given by:

$$R_{rad}(V) = R_{rad,dark} e^{\frac{qV}{k_BT}} \qquad (2.43)$$

We can then define a radiative saturation current $J_{0,rad} = q \times R_{rad,dark}$ and, taking into account radiative recombination, the ideal diode Equation (2.37) becomes:

$$J(V) = J_{sc} + (J_0 + J_{0,rad})\left(1 - e^{\frac{qV}{k_BT}}\right) \qquad (2.44)$$

where J_0 has been defined in Equation (2.32) and depends on doping and diffusion lengths. Although J_0 can be reduced by carefully engineering the doping profile of the cell, $J_{0,rad}$ is an intrinsic limit on cells performance and the upper limit of the V_{oc} without concentration can be expressed as:

$$V_{oc,lim} = \frac{k_BT}{q} ln\left(\frac{J_{sc}}{J_{0,rad}} - 1\right) \approx \frac{E_g}{q} + \frac{k_BT}{q} ln\left(\frac{\Omega_{sun}}{2\pi}\right) \qquad (2.45)$$

This upper limit $V_{oc,lim}$ can be increased using concentration. The electronic approach from Equation (2.44) and the thermodynamic approach from Equation (2.39) are coherent, as concentration multiplies J_{sc} and Ω_{sun} by the same factor.

A third source of intrinsic loss is the Auger recombination process. Auger recombination happens when the excess energy from the recombination of a free carrier (electron in the conduction band or hole in the valence band) is dissipated by transmission to another free carrier instead of emission of a photon. The carrier

receiving this excess energy will move higher in its energy band before being thermalised, as shown in FIGURE 2.12-6). Auger recombination is especially important in indirect semiconductors, where radiative emission is an inefficient process, and in low bandgap semiconductors with high intrinsic carrier densities. The general recombination rate per unit volume for Auger recombination is given by:

$$R_{Auger}(V) = C_n n^2 p + C_p p^2 n = \left(C_n n + C_p p\right) n_i^2 e^{\frac{qV}{k_B T}} \tag{2.46}$$

where C_n and C_p are the Auger coefficients of electrons and holes, respectively. In the simplification hypothesis of an intrinsic concentration or light doping we have $n \approx p \approx n_i exp(qV/2k_BT)$ and Equation (2.46) becomes:

$$R_{Auger}(V) = \left(C_n + C_p\right) n_i^3 e^{\frac{3qV}{2k_B T}} = C n_i^3 e^{\frac{3qV}{2k_B T}} = \frac{J_{0,Auger}}{qL} e^{\frac{3qV}{2k_B T}} \tag{2.47}$$

where $C=C_n+C_p$ is the ambipolar Auger coefficient, $J_{0,Auger}=qLCn_i^3$ is the saturation current density associated with Auger recombination and $L=W_{emit}+W_D+W_{base}$ is the thickness of the cell. The diode Equation (2.44) then becomes:

$$J(V) = J_{sc} + \left(J_0 + J_{0,rad}\right)\left(1 - e^{\frac{qV}{k_B T}}\right) + J_{0,Auger}\left(1 - e^{\frac{3qV}{2k_B T}}\right) \tag{2.48}$$

b) Extrinsic losses

The first source of extrinsic loss is related to optical inefficiencies in the cell, in particular reflections at the front surface, as shown in FIGURE 2.12-7), unabsorbed photons with an energy close to the bandgap (red), as shown in FIGURE 2.12-2), and recombination of carriers created by short wavelength (blue) photons close to the top surface, because of surface recombination and/or high doping of the emitter. The External Quantum Efficiency (EQE) is a good metric of the optical efficiency of a cell. It quantifies, for each wavelength, the percentage of photons converted to electrons and then collected, as shown in FIGURE 2.13. The reflection at the front surface can be drastically reduced, and, therefore, the EQE increased, using an Anti-Reflection Coating (ARC) – similar to the ones used for other optics such as camera lenses – and surface texturing. The EQE directly impacts the J_{sc} with the relation:

$$J_{sc} = q \int_0^{+\infty} EQE(\lambda) \times \Phi_{0,\lambda} d\lambda \tag{2.49}$$

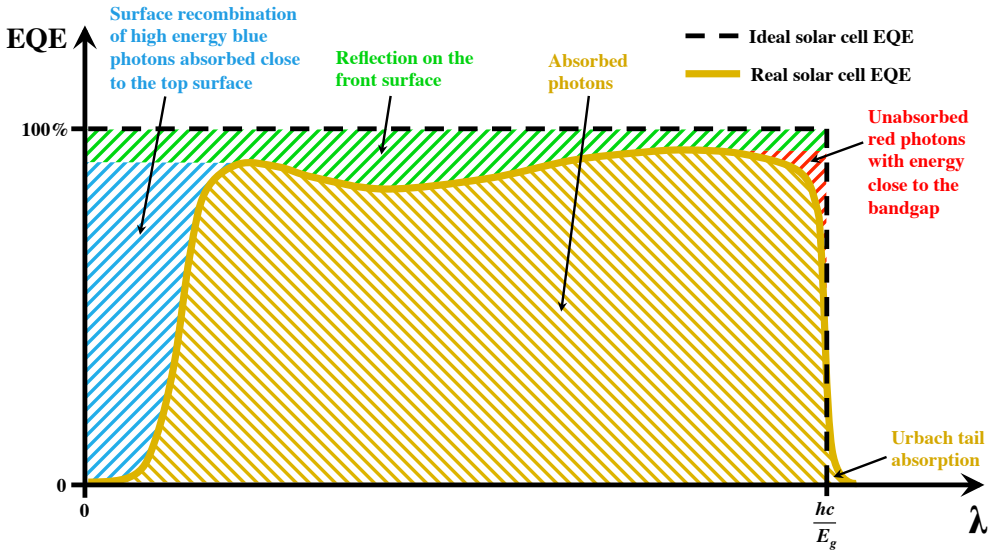

FIGURE 2.13. *External Quantum Efficiency (EQE) of an ideal and a real solar cell, showing the different sources of optical losses.*

Defects in the semiconductor material will also be a source of non-radiative recombination leading to losses. Specifically, defects act as recombination centres where carriers can be trapped and later recombine with an opposite carrier, as shown in FIGURE 2.12-8). This defect-assisted recombination process is called Shockley-Read-Hall (SRH) recombination. The general per unit volume SRH recombination rate is given by:

$$R_{SRH} = \frac{np}{\frac{n+n_{oc}}{\rho_D \sigma_n v_{th}} + \frac{p+p_{oc}}{\rho_D \sigma_p v_{th}}} = \frac{np}{\tau_n(n+n_{oc}) + \tau_p(p+p_{oc})} \qquad (2.50)$$

where n_{oc} and p_{oc} are the electron and hole occupancy of the defect levels, ρ_D is the defect density, $\sigma_{n/p}$ the capture cross-section for electrons/holes, v_{th} the average thermal velocity of carriers, and $\tau_{n/p}=1/(\rho_D \sigma_{n/p} v_{th})$ the lifetime of carriers associated with SRH recombination due to the considered defect. Depending on the type of defect and the zone of the cell (space charge region or quasi-neutral regions) studied, the SRH recombination rate will take different forms.

For example, when considering doping in the p-region of the depletion zone, as nearly all the doping atoms are ionized, we have $n_{oc} \approx N_A >> n$ and $n_{oc} \approx N_A >> p+p_{oc}$. Consequently:

$$R_{SRH,doping} = \frac{np}{\tau_n(n+n_{oc})+\tau_p(p+p_{oc})} \approx \frac{n_i^2}{\tau_n N_A} e^{\frac{qV}{k_B T}} = \frac{n_i^2 D_n}{L_n^2 N_A} e^{\frac{qV}{k_B T}} \quad (2.51)$$

By applying the same reasoning to the n-type region of the depletion zone we easily obtain the results from Equations (2.30-2.32). The saturation current defined in section 2.2.4 is, thus, the SRH recombination associated with doping in the space charge region.

If now we consider deep energy levels located in the middle of the bandgap – such as threading dislocations – in the space charge region, we can assume that the traps are barely occupied so that $n \approx n_i exp(qV/2k_BT) >> n_{oc}$ and $p \approx n_i exp(qV/2k_BT) >> p_{oc}$. As a result:

$$R_{SRH,deep\ defects} = \frac{np}{\tau_n(n+n_{oc})+\tau_p(p+p_{oc})} \approx \frac{n_i}{\tau_n+\tau_p} e^{\frac{qV}{2k_B T}} \quad (2.52)$$

For basic p-n junction solar cells, a sizable amount of SRH recombination happens at the top and bottom surfaces because of the abrupt termination of the crystal: each dangling bond at the interface acts as a defect and, therefore, is a recombination centre, as shown in FIGURE 2.12-9). In order to reduce the impact of surface recombination, a thin passivation layer, such as silicon dioxide or silicon nitride in the case of silicon solar cells, can be used to provide termination to the dangling bonds. Using a thin highly doped and possibly higher bandgap layer at the top and bottom surfaces of the cell also reduces surface recombination by letting majority carriers through but stopping minority carriers from reaching the surface. Such an apparatus is called a "window layer" on the front surface of the cell and a "back surface field" on the rear surface.

In order to take into account all these alternative recombination pathways, the general diode Equations (2.37), (2.44) and (2.48) can be rewritten in a form inclusive of all recombination processes (radiative, Auger, SRH) as:

$$\begin{aligned} J(V) = J_{sc} &+ J_{0,rad}\left(1 - e^{\frac{qV}{k_B T}}\right) + J_{0,Auger}\left(1 - e^{\frac{3qV}{2k_B T}}\right) \\ &+ \sum^{m} J_{0,SRH,m}\left(1 - e^{\frac{qV}{n_m k_B T}}\right) \end{aligned} \quad (2.53)$$

where m represents the different types of defects in the different zones of the cell, $J_{0,SRH,m}$ is the associated non-radiative recombination saturation current, and n_m is the associated factor in the exponential, called the ideality factor. As a general rule, radiative recombination and recombination due to doping have an ideality factor of n=1, non-radiative recombination due to other defects in the depletion zone has an ideality factor n=2, and Auger recombination has an ideality factor n=(2/3).

The general equation for solar cells (2.53) can then be approximated by:

$$J(V) = J_{sc} + J_{0,all}\left(1 - e^{\frac{qV}{nk_BT}}\right) \tag{2.54}$$

where $J_{0,all}$ is a saturation current inclusive of all recombination processes and n is an average ideality factor. The value of n is then a good metric of the dominant recombination processes in the cell. When radiative recombination and recombination due to doping dominate, the ideality factor is close to 1 or even slightly lower. When non-radiative recombination due to defects other than doping in the depletion zone dominates, the ideality factor will be higher than 1 and closer to 2 for high non-radiative recombination rates.

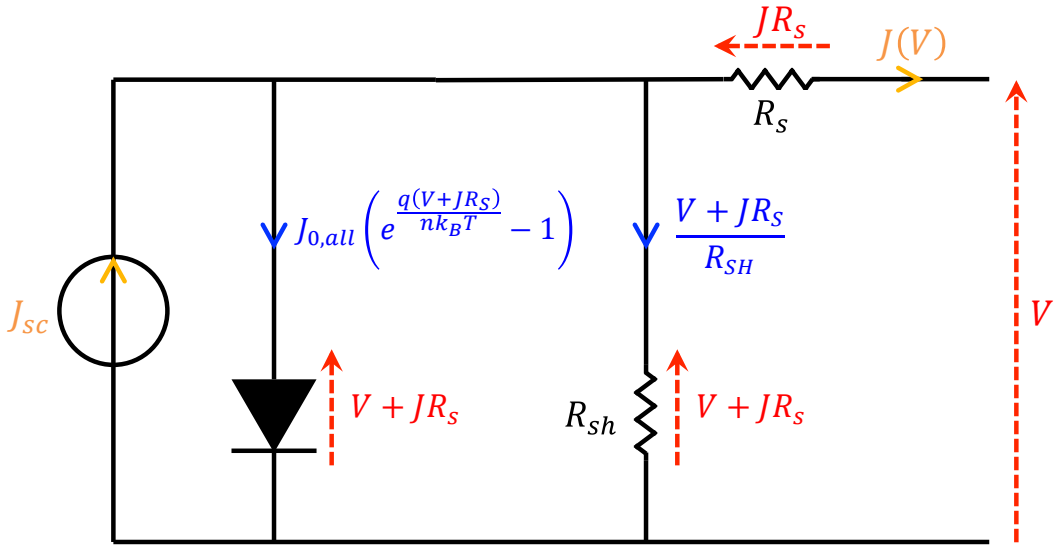

FIGURE 2.14. *Simplified electric circuit of a photovoltaic solar cell, taking into account series and shunt resistances. Capacitances are neglected.*

Finally, purely electric losses due to series and shunt resistances will add up to the losses caused by optical inefficiencies, entropy production, and non-radiative recombination. Series resistance R_S is due to the bulk resistance of the wafer and additional parasitic resistance at the semiconductor/metal interface on the contacts. Ideally, the series resistance should be null. Shunt resistance R_{SH} is related to carriers finding an alternate pathway through the wafer, in parallel to the p-n junction – for example along defects or along surface states on the unpassivated edge of the cell – thus shorting the diode. Ideally, the shunt resistance should be infinite. A simplified diagram of the equivalent circuit is presented in FIGURE 2.14.

Taking series and shunt resistances into account, the generalized steady-state diode Equation (2.54) becomes:

$$J(V) = J_{sc} + J_{0,all}\left(1 - e^{\frac{q(V+JR_S)}{nk_BT}}\right) - \frac{V + JR_S}{R_{SH}} \qquad (2.55)$$

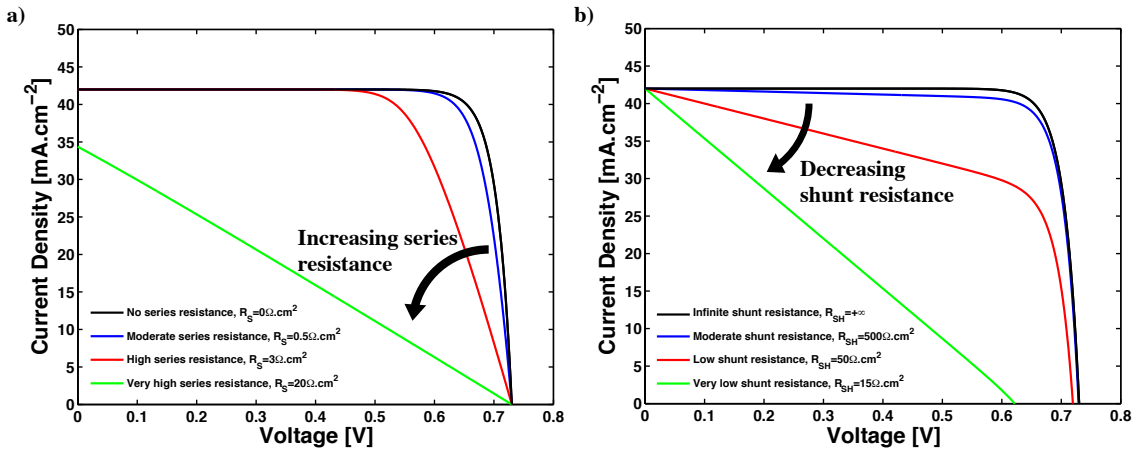

FIGURE 2.15. a) *Impact of different values of series resistance on the J-V characteristic of a high efficiency silicon solar cell.* ***b)*** *Impact of different values of shunt resistance on the J-V characteristic of an optimised silicon solar cell.*

As shown in FIGURE 2.15, series and shunt resistances will have a different impact on the J-V characteristic of the cell. As series resistance only impacts the cell when a current is delivered, it will not influence the V_{oc} but can reduce the J_{sc} for high R_S values, as shown in FIGURE 2.15a). For low R_S values, the series resistance will mainly reduce the fill factor of the cell. The series resistance value can be estimated by calculating the slope of the *J-V* curve at V=V_{oc}. On the contrary, as the shunt

resistance only impacts the cell when the voltage is non-null, it will not influence the J_{sc} but can reduce the V_{oc} for low R_{SH} values, as shown in FIGURE 2.15b). For high R_{SH} values, the shunt resistance will mainly reduce the fill factor of the cell. The shunt resistance value can be estimated by calculating the slope of the *J-V* curve at V=0.

2.4.2 The detailed balance limit

As presented in Section 2.4.1, losses in solar cells can be classified into two categories: intrinsic, tied to the nature of the physics of photovoltaic devices, and extrinsic, related to the actual architecture of the cell and reducible to some extent. By only considering intrinsic loss mechanisms, a theoretical upper limit on the efficiency of photovoltaic solar cells can be calculated. The particular case of medium to high bandgap (1 eV<E_g<2 eV) direct semiconductors, where Auger recombination is low enough to be neglected, is an interesting case study. In that case, electron-hole pairs generated by absorption of photons can either recombine, reemitting a photon in the process, or be collected. This approach, developed by Shockley and Queisser in 1961 [2.13], is called the "detailed balance limit", by reference to the fact that every absorbed photon needs to escape the cell as a reemitted photon or a charge carrier, ensuring the balance between particles entering and exiting the device.

Ross later unveiled the impact of non-radiative recombination on the open-circuit voltage [2.14], introducing the concept of luminescent efficiency, as presented here in Equation (2.40). The detailed balance limit was then refined by Tiedje *et. al.* [2.15], to include the impact of Auger recombination, leading to the calculation of a maximal efficiency of 29.8 % for silicon solar cells. Further work using a refined approach, particularly regarding the Auger recombination model, has confirmed an efficiency limit around 29 % [2.16]. More recently, Miller *et. al.* [2.17] applied the same detailed balance limit to GaAs solar cells, calculating a maximum efficiency of 33.5 %. Finally, Smith *et. al.* have estimated that the industrially achievable efficiency of silicon solar cells is limited to around 26 % [2.9]. In the end, the upper practical efficiency for classic p-n junction photovoltaic solar cells lies around 30 %, even using highly luminescent direct bandgap materials such as GaAs, and an alternate strategy is needed to overcome this 30 % efficiency limit.

2.4.3 Multijunction solar cells: overcoming the limit

As presented in Section 2.4.1, the biggest source of losses in solar cells is intrinsic to the physics of semiconductors and of the photovoltaic effect: below bandgap photons are not absorbed and above bandgap photons are thermalised, representing losses of about 50 % for Si solar cells. As the bandgap of the cell is unique, reducing these losses is impossible using a classic monojunction architecture.

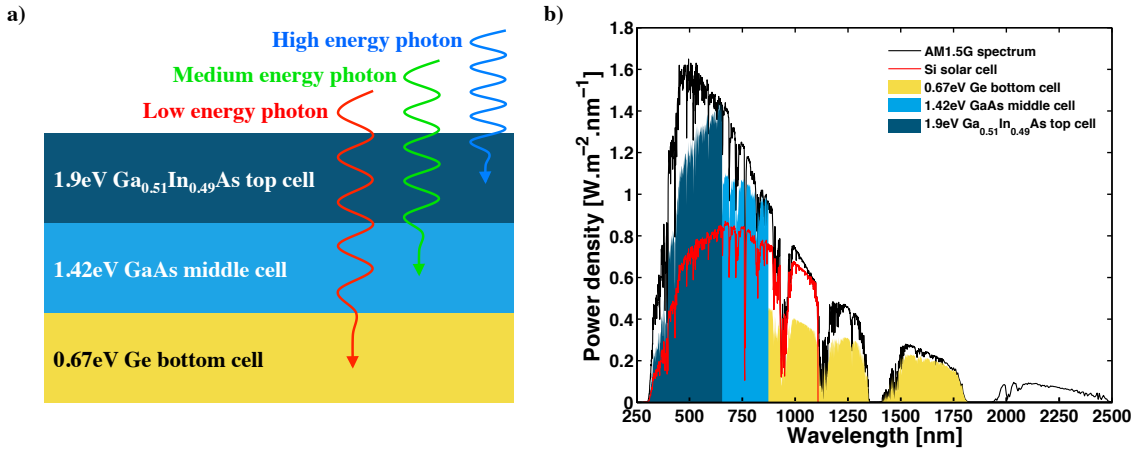

FIGURE 2.16. a) *Schematic of a classic $Ga_{0.51}In_{0.49}P$/GaAs/Ge triple junction solar cell, representing the absorption of different energy photons.* ***b)*** *Comparison between the energy collection ability of Si (red line) and a classic $Ga_{0.51}In_{0.49}P$/GaAs/Ge triple junction solar cell (yellow, light blue and dark blue areas).*

The multijunction approach, presented for the first time by Jackson in 1955 [2.18], proposes using multiple p-n junctions with different bandgaps to increase the harvestable portion of the solar spectrum. In a standard multijunction architecture, p-n junctions of increasing bandgaps are stacked vertically, with the highest bandgap junction closest to the top surface. As shown in FIGURE 2.16a), showing a schematic of a classic lattice-matched $Ga_{0.51}In_{0.49}P$/GaAs/Ge triple junction solar cell, high energy photons will be absorbed in the top junction/subcell while lower energy photons will go through it and be absorbed in lower junctions/subcells. The impact on the collectable energy out of the AM1.5G spectrum is displayed in FIGURE 2.16b). In a multijunction architecture, compared with a standard monojunction solar cell such as classic Si, junctions with a higher bandgap than Si will increase the amplitude of

the collected energy, harvesting more energy out of every photon, while junctions with a lower bandgap than Si will increase the width of wavelengths collected, harvesting a higher number of photons in total.

2.4.4 Design and operation of multijunction solar cells

As each junction in a multijunction solar cell produces its own current and its own voltage, the way the junctions are contacted and connected will strongly influence their design and operation. Contacting architectures are usually classified depending on the number of contacting terminals used: 2-terminal, 3-terminal, 4-terminal, etc. FIGURE 2.17 shows the different contacting architectures possible as well as the simplified equivalent electric circuits in the case of a 2-junction solar cell.

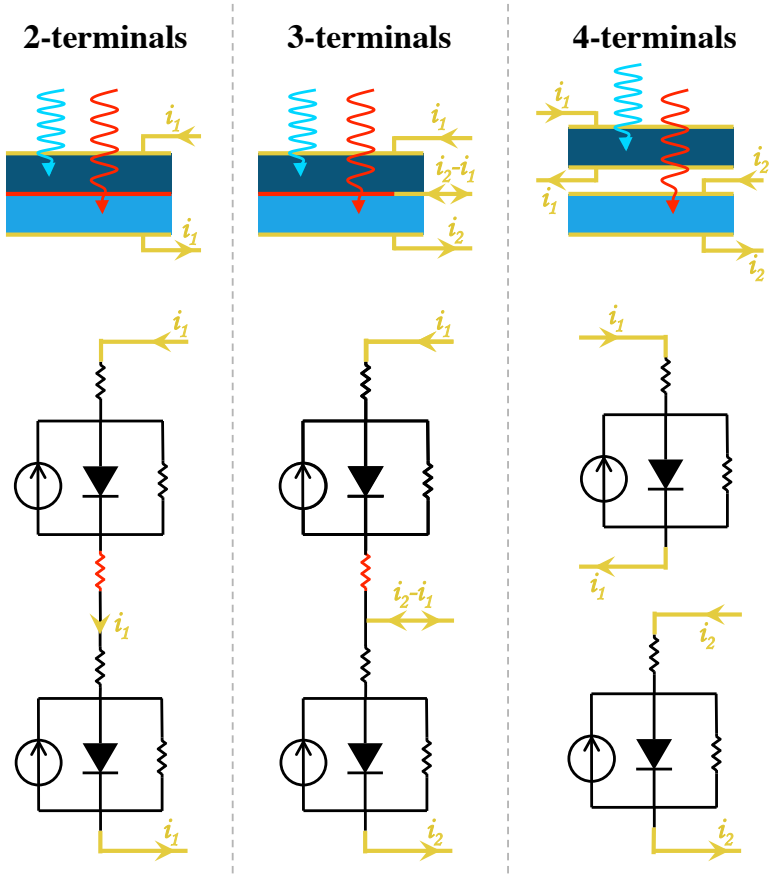

FIGURE 2.17. *Schematic of 2-terminal (left), 3-terminal (middle) and 4-terminal (right) contacting architectures for a 2-junction solar cell with the equivalent electric circuits. Contacts are shown in yellow, tunnel junctions and their equivalent resistance are shown in red.*

In a 2-terminal architecture, it is important to note that, as the junctions are connected in series, their currents have to match. This adds a significant design constraint on the multijunction architecture. Indeed, to perform optimally, both cells need to produce the same current at their respective maximum power point and, thus, need to have very close short-circuit currents. As a result, the bandgaps and thicknesses of each subcell need to be engineered so that all subcells produce matching currents. Moreover, the subcells need to be connected using tunnel junctions so that the p-type region of a given subcell is not in direct contact with the n-type region of an adjacent subcell, causing an opposite p-n junction lowering the photovoltage of the multijunction cell.

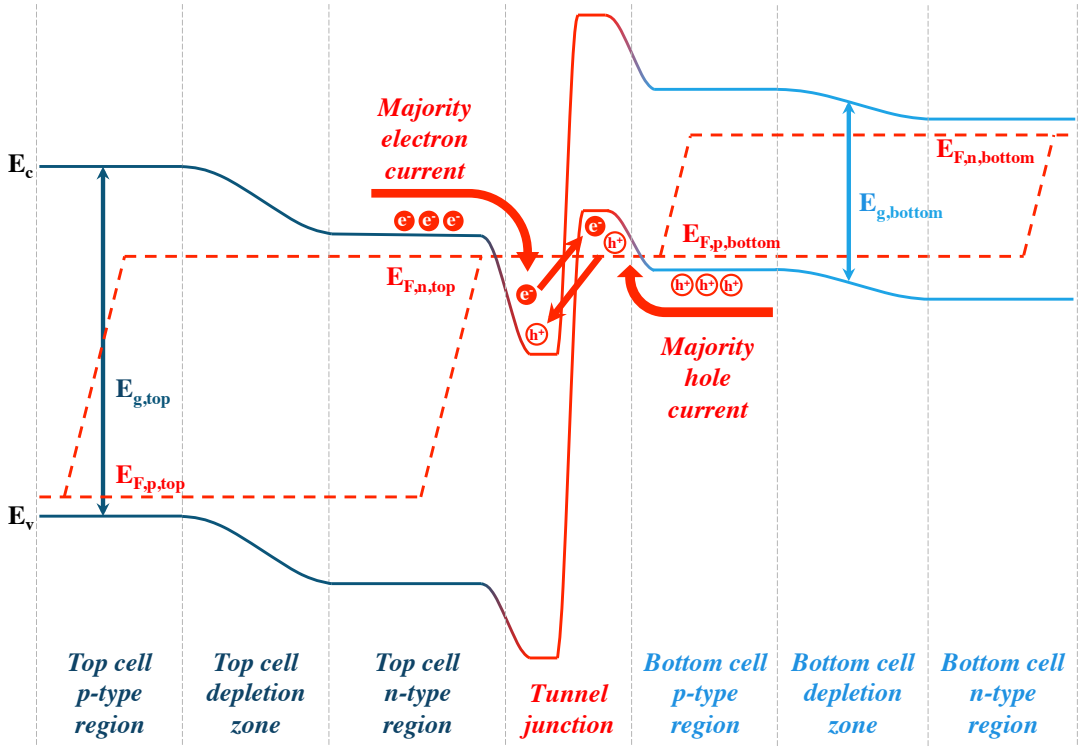

FIGURE 2.18. *Band diagram of a 2-junction solar cell with both cells connected in series through a tunnel junction.*

Tunnel junctions are extremely highly doped and very thin opposite p-n junctions, as shown in FIGURE 2.18. They allow electrons in the conduction band of the n-type region of a subcell to travel to the valence band of the p-type region of the adjacent subcell, where they recombine with excess holes, by tunnelling through the junction

with minimal resistance and voltage reduction. Reciprocally, holes in the valence band in the p-type region can tunnel to the conduction band in the n-type region, where they recombine with excess electrons without reducing the voltage. The majority electron current in the n-type region on the left subcell represented in FIGURE 2.18 can, thus, become a majority hole current in the p-type region of the right subcell. The tunnel junction and its associated resistance are displayed in red in FIGURE 2.17.

In order to ensure a greater flexibility in the design of the cell, contacting each junction independently from the others in a 3-terminal or 4-terminal architecture is the best solution to avoid issues arising from current matching or tunnel junctions. However, separately contacting each junction of a multijunction solar cell presents serious fabrication challenges, especially for large-area cells. Moreover, shadowing due to the contacts of higher subcells will reduce the absorption in the bottom subcells. Even using transparent electrodes, for example made of ITO, achieving reasonable conductivity and high transparency across the full absorption spectrum of the lower subcells is challenging. As this approach is harder to industrialise, 2-terminal architectures are preferred for commercial multijunction solar cells.

One last important element in the design of multijunction solar cells is related to luminescent coupling between the cells, as highlighted in Chapter 4. Luminescent coupling refers to photons emitted by radiative recombination in an upper subcell and cascading to a lower subcell where they participate in the photocurrent. This current boost can greatly improve the flexibility in the design of current-matched multijunction solar cells when the upper cells present high luminescent efficiencies [2.19].

The goal of this thesis is to present the progress made by the team of Professor Huiyun Liu at UCL towards the development of high efficiency (>30 %) low cost III-V/Si dual-junction solar cells. The basic theoretical elements reviewed in the present chapter are particularly relevant to the understanding of Chapter 4, which concentrates on the modelling of such architectures. The characterisation techniques presented in Chapter 3 are also naturally related to the theoretical elements presented here.

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Chapter 3

Experimental Methods

This research project focuses on the experimental demonstration of high material quality, high efficiency III-V on Si photovoltaic solar cells grown, fabricated and characterised using University College London amenities, in particular its Molecular Beam Epitaxy (MBE) facilities. This chapter details the experimental methods employed to develop the experimental devices presented in Chapters 5 and 6. The MBE growth technique is outlined: we present the basics of the technology, the structure of MBE reactors, the equipment used to in-situ monitor the growth conditions and the epitaxial deposition process, and finally the different possible growth modes. The particular case of III-V on Si heteroepitaxy is outlined with a focus on the challenges pertaining to such an approach and how to circumvent them. The characterisation techniques used to assess the material quality of the grown material are then detailed. Finally, the processing steps employed to fabricate solar cells from grown wafers and the device characterisation techniques used to determine the performance of these solar cells are explained.

3.1 Molecular Beam Epitaxy (MBE) growth

3.1.1 Basics on epitaxial growth and MBE operation

Epitaxy refers to the deposition of a material upon a crystalline substrate, under conditions allowing the deposited material to replicate the crystalline structure of the underlying substrate, leading to a highly crystalline grown epilayer. The deposition process is called homoepitaxy when the epilayers and the substrate are of the same composition, such as growth of GaAs on GaAs, and heteroepitaxy when the deposited material and the substrate are of different natures, such as growth of GaAs on Si. Multiple epitaxial growth techniques exist, such as Liquid Phase Epitaxy (LPE), Molecular Beam Epitaxy (MBE), and Metal-Organic Chemical Vapour Deposition (MOCVD). Owing to their versatility and precision, MBE growth techniques have been instrumental in the development of pioneering new materials and structures. All of the experimental devices presented in this thesis have been grown by MBE by Dr. Jiang Wu and Dr. Mingchu Tang, using the facilities available at UCL, as detailed hereafter.

Molecular Beam Epitaxy (MBE) is an Ultra High Vacuum (UHV) epitaxial growth technology developed by Al Cho and John Arthur at Bell Laboratories in the late 1960's [3.1-3.2]. The overall concept is relatively simple: high purity materials are evaporated with precise flux rates on a crystalline substrate maintained at a controlled temperature under UHV conditions, in a process akin to thermal evaporation. The difference resides in the extremely high precision, purity and flexibility of the MBE growth process.

Thanks to the UHV environment in the growth chamber, the mean free path of homoatomic chemical species evaporating from the ultra-high purity source materials (Ga, As_2, As_4…) will be orders of magnitude longer than the distance to the substrate. Evaporation from the sources, maintained in effusion cells, can therefore be considered rectilinear, hence the "Molecular Beam" qualification of the technology. These molecular beams are directed towards the substrate and, upon collision with the substrate surface, chemical species can be weakly adsorbed on the surface and

dissociated into individual atoms. These individual atoms will then migrate to a suitable lattice site and be incorporated into the growing film, leading to the epitaxial growth. Depending on the adsorption, migration and incorporation conditions, the surface morphology will be different, as detailed in Section 3.1.4.

The UHV environment inside the growth chamber, coupled with ultra-high purity elemental source materials and proper preparation of the substrate to obtain a clean surface at the atomic level, ensures a minimal contamination of the epitaxially grown film. Careful monitoring of the effusion cells' temperatures and of the opening and closing sequence of the shutters in front of them allows for a very accurate control over each molecular beam flux rate. Thus, the deposition rates can be precisely controlled from the beam flux rates and the substrate temperature. In particular, Arthur [3.3] demonstrated that, in the case of III-V growth under suitable conditions, group III atoms (Ga, Al, In…) possess a sticking coefficient on the substrate close to unity, meaning that nearly all impinging atom will be incorporated into the film, whereas group V elements (As_2, Sb_2…) barely stick to the surface by themselves and are desorbed in the absence of group III elements. As a result, MBE growth is performed under excess group V flux rates and the growth rate is solely dictated by group III flux rates.

Very slow deposition rates (1 to 2 monolayers per second) can be achieved by adjusting the effusion cells temperature. The individual shutters of the effusion cells, if properly designed, present much shorter opening and closing times, typically below a tenth of a second. This allows for extremely sharp interfaces, with abrupt modification of the epilayer composition at the atomic layer scale. Very precise architectures can, thereby, be engineered, leading to devices exploiting the quantum properties of such very low dimension structures. In order to provide the purity, the precision, and the flexibility required for such a fine-tuning of growth parameters, a specific reactor architecture is needed, as detailed hereafter.

3.1.2 MBE reactor architecture

An MBE system consists of interconnected modular building blocks under high or ultra high vacuum. A typical system will at least comprise a load-lock, a preparation

chamber, and a growth chamber. The III-V MBE system used at UCL also includes a phosphorus recovery system in order to collect hazardous phosphorus residues from P-based III-V compounds growth. As P-based III-V compounds have not been used in the work presented in this thesis, we will leave out a detailed description of the phosphorus recovery system. The chambers are separated using UHV gate valves to avoid cross contamination between them and allow different pressures in each chamber when loading and preparing wafers.

Under standard MBE operations, the load-lock is the only chamber not continuously maintained under vacuum. Its role is to enable the loading and unloading of wafers in and out the MBE system while keeping the UHV environment in the other chambers. It is equipped with a high vacuum pump, to pump down from atmosphere to high vacuum pressures levels (about 10^{-7} torr). The load-lock of the MBE system used at UCL is also equipped with a cryogenic pump in order to provide better vacuum capabilities. Inside the load-lock, two quartz infrared tube lamps are used to heat up newly loaded wafers to about 100 °C to 200 °C in order to perform a preliminary outgassing of water and other volatile chemical species from the surface of the wafers. Contamination of the preparation and growth chambers from the wafer surface is, thus, avoided. Once the wafers are outgassed and the high vacuum is reached in the load-lock, the samples can be transferred to the preparation chamber.

The preparation chamber acts as a buffer between the high vacuum reached in the load-lock and the UHV inside the growth chamber. It is equipped with an ion pump to pump down from high to ultra high vacuum. Similar to the load-lock, the preparation chamber is equipped with a heating stage, which can heat wafers up to 600 °C. This second pre-growth high temperature outgassing ensures desorption of almost all the evaporable contaminants from the surface of the wafers before entering the growth chamber. Removal of the thin oxide layer present on the surface of wafers may also be performed in the preparation chamber, although most growers prefer to perform this step inside the growth chamber where a better control over the oxide removal process can be achieved.

The growth chamber is the most important and the most sensitive part of the MBE system, as the high-precision high-quality epitaxial growth process is performed

there. FIGURE 3.1 shows the usual configuration of a growth chamber. The substrate wafer is placed in the centre of the chamber on a substrate holder. The substrate holder rotates perpendicularly to the growth direction in order to ensure homogenous deposition. A substrate heater, mounted behind the substrate holder, is used to heat up the sample wafer. Temperatures over 1000 °C, suitable for Si oxide removal, can be reached. An ion gauge is mounted on the back of the substrate holder and the substrate heater to measure the pressure within the growth chamber and calibrate flux rates. The growth stage – consisting of the substrate holder and substrate heater – and the ion gauge are mounted together on a manipulator used to precisely position them inside the chamber. Three positions are usually used during MBE operation:

1. Base position: substrate holder facing the effusion cells during growth, with the ion gauge protected behind the growth stage,
2. 90 ° from base position: substrate holder facing the exchange port to load/unload wafers from/to the preparation chamber,
3. 180 ° from base position: ion gauge facing the effusion cells for calibration of the flux rates, with the substrate holder protected behind the growth stage.

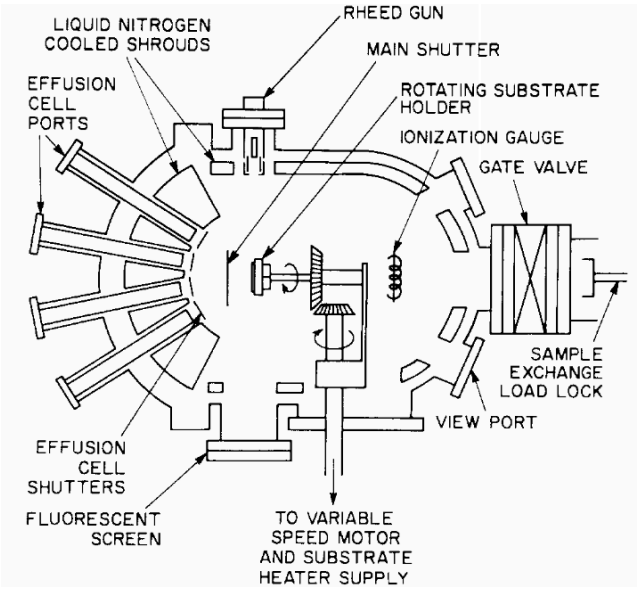

FIGURE 3.1. *Standard configuration of a growth reactor. The configuration presented here differs slightly from the MBE system used in our work, as – in the case of UCL's MBE growth reactor – the load lock is perpendicular to the effusion cells rather than in line with them. It is to be noted that the ion gauge is attached to the growth stage and rotates with it. Adapted from Ref. [3.4] with permission from ALP Publishing.*

Effusion cells are mounted opposite to the substrate holder in its growth position so that the growth substrate sits at the focal point of the cells. In order to avoid contamination from flakes falling into them or onto the wafer, the effusion cells are attached as horizontally as possible. On top of the ion pump and cryogenic pump ensuring the UHV environment, with background pressures in the 10^{-10} to 10^{-11} torr, a cryopanel surrounds the chamber and separates the effusion cells in order to avoid possible cross-contamination between the sources and to trap contaminants such as water and hydrocarbons on the walls of the growth chamber. The cryopanel consists of a shroud in which a very low temperature coolant, such as liquid nitrogen, circulates.

The III-V MBE system used at UCL has eleven effusion cells: two Ga, two Al, two In, one As, one Sb, and one P cell for growth plus one Si and one Be cell for doping. As mentioned above, the growth rate is governed by the group III elements' flux rates. Having two cells for each group III element enables different cell temperatures and, therefore, different growth rates for the same element during one growth run. For high growth rates, both group III cells can be opened at once with a high flux rate from the group V cell at high temperature. The high-purity source materials are placed in pyrolitic boron-nitride crucibles inside the effusion cells where their temperature is controlled with an accuracy of ±1 °C. Each material requires a specific effusion cell architecture – involving one, two, or three temperature zones – with the design of the effusion cell varying widely depending of the type of material used in the cell. Fast actuation time mechanical shutters are placed in front of each cell to abruptly start or interrupt the deposition of a given material, enabling brusque modifications of material composition and sharp interfaces within the grown sample. Instantaneous in-situ monitoring of the conditions within the growth chamber and of the growth itself are performed using a set of analytical instruments, as detailed in the following section.

3.1.3 Control of growth chamber conditions and epitaxy monitoring

The background pressure inside the growth chamber is monitored using the ion gauge placed at the back of the growth stage, as described earlier. Using the manipulator, the ion gauge can also be directed toward the effusion cells where it can be used to

calibrate beams' flux rates. In this configuration, one cell is calibrated at a time by opening the shutter in front of it and observing the difference between the background pressure and the beam-on pressure measured by the ion gauge.

Thermocouples are used to measure the temperatures of the different zones of the effusion cells as well as the temperature of the substrate. Over 450 °C, a pyrometer mounted outside of the growth chamber is also used to measure the temperature of the substrate. The pyrometer performs an optical measurement of the substrate temperature by analysing the blackbody radiation from the growth wafer, thus enabling a remote measurement through a viewport. During each growth run, the oxide desorption temperature of the wafer is recorded and compared with the known value from the literature to add precision to the substrate temperature measurements from the thermocouple and the pyrometer.

A Reflection High-Energy Electron Diffraction (RHEED) system is used during growth to monitor the morphology of the growth surface in-situ as well as to determine the growth mode. The RHEED system consists of an electron gun firing high-energy electrons (10-20 keV) onto the substrate surface at a grazing angle (0.5 ° to 3 °). An opposite fluorescent screen records the constructive and destructive interferences from the reflected beam of electrons, diffracted by the atoms on the surface of the sample. Depending on the crystalline structure and the morphology of the surface, different diffraction patterns will be observed. Hence, RHEED measurements enable a direct observation of the growth process, in particular the crystalline structure of the material being grown. Regarding the morphology of the film, it has been shown [3.5] that a streaky pattern corresponds to the growth of a flat 2-dimensional film while a spotty pattern corresponds to a 3-dimensional islanding growth. RHEED measurements can also be used before growth to monitor the oxide removal process, as the reading switches from a hazy to a clear diffraction pattern when an atomically clean substrate surface is reached. Additionally, when a smooth 2-dimensional growth is performed at a relatively slow growth rate, the growth rate can be extracted from the oscillation of the RHEED intensity. Indeed, growth of a monolayer is not immediate: coverage of the growth surface by a new monolayer will gradually increase from 0 to 100 %. When about 50 % of the surface is covered,

reflections from the covered and non-covered portions of the surface interfere, thus reducing the RHEED intensity. On the other hand, when the surface is fully covered, such parasitic interference does not happen and the RHEED intensity reaches a maximum. The period between two intensity maxima or minima is, thus, the time needed to grow one monolayer. This process is detailed in FIGURE 3.2.

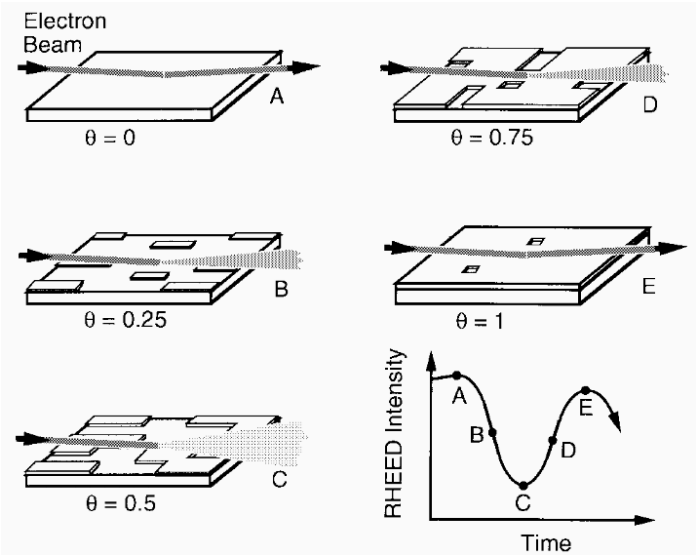

FIGURE 3.2. *Representation of the deposition process of a monolayer with the corresponding RHEED intensity oscillation. The parameter θ represents the coverage fraction of the surface. Reprinted from Ref. [3.6] © 1997 IEEE – No permission required.*

Finally, a Residual Gas Analyser (RGA) is used to monitor the background conditions within the growth chamber. An image of the gas residuals inside the chamber, including the partial pressure of each chemical species, can be deduced from RGA measurements, making it a powerful diagnostic tool in case of a leak or background contamination.

3.1.4 MBE growth modes

Under standard operation, MBE growth modes can usually be classified into three categories: Franck-Van der Merwe (FM), Volmer-Weber (VW) and Stranski-Krastanov (SK). The growth mode of an epitaxial film will depend on the interaction between the growth interface and the incoming adatoms, in particular their migration

length and their preferential incorporation sites. FIGURE 3.3 represents the three different growth modes.

The Franck-Van der Merwe (FM) growth mode, shown in FIGURE 3.3a), corresponds to a purely 2-dimensional layer-by-layer growth where adatoms have long migration length and preferably incorporate directly on the growth interface instead of attaching to other recently deposited adatoms. On the contrary, the Volmer-Weber (VW) growth mode, shown in FIGURE 3.3b), corresponds to a 3-dimensional islanding growth where adatoms preferably attach to other recently deposited adatoms. This leads to the growth of separate islands that later coalesce, resulting in a wavy growth interface. This growth mode favours the nucleation of defects where islands coalesce and makes the fine engineering of low dimension structures with abrupt interfaces – such as quantum wells or quantum dots – difficult. The growth temperature plays an important role in the growth mode as it governs the migration length. At low temperature, the migration length is short and a VW growth mode is more probable. At high growth temperature, the migration length is longer and the FM growth mode is energetically more favourable.

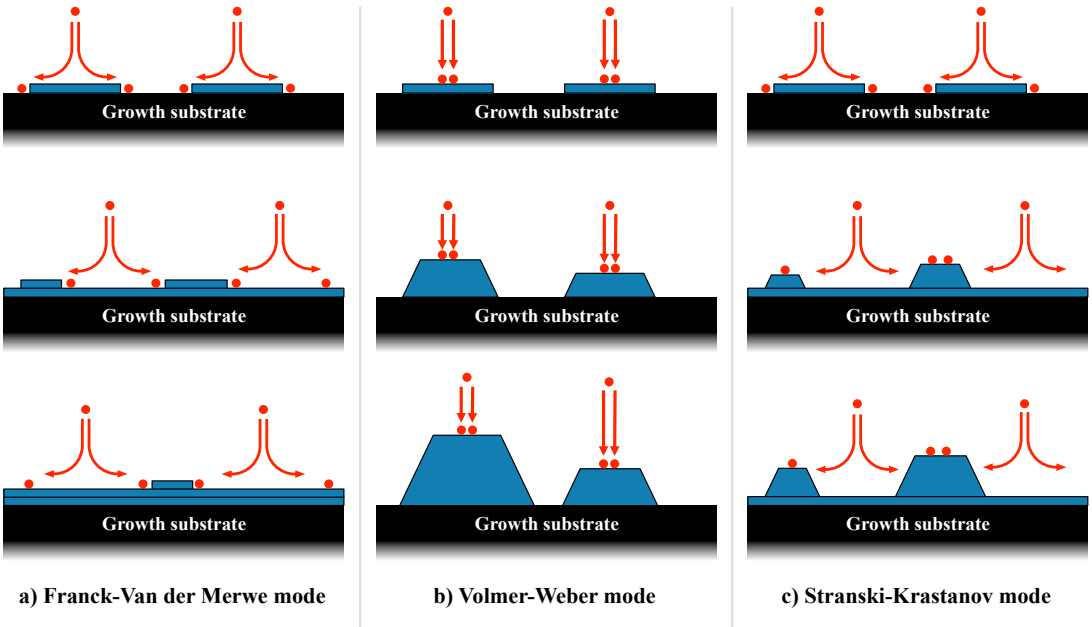

FIGURE 3.3. *Illustration of the three common MBE growth modes: a) Franck-Van der Merwe (FM) mode, b) Volmer-Weber (VW) mode, c) Stranski-Krastanov (SK) mode.*

The Stranski-Krastanov growth mode, shown in FIGURE 3.3c), is somewhat halfway between the FM and VW modes. The growth begins with a smooth 2D layer-by-layer growth mode but, above a certain critical thickness, the preferential incorporation sites of adatoms switches from the growth interface to recently deposited adatoms and an islanding growth mode develops. From the point of view of the energy, there is a change of sign of the free energy associated with the incorporation of an adatom on the surface, equivalent to a shift in the force balance between the surface tension and the contact angle of the film. SK growth mode is particularly common during lattice-mismatched growth: as a 2D film with a different lattice parameter is deposited on a substrate, strain due to the lattice-mismatch will build up in the epilayers and will eventually overtake the surface tension of the film. Thus, the growth transitions to an islanding mode. SK growth mode can have some advantages, in particular for the growth of quantum dots using highly mismatched materials such as InAs/GaAs. However, in the case of bulk monolithic lattice-mismatched growth of III-V materials on Si, SK growth mode is an obstacle, as the interfaces between coalesced islands will provide nucleation sites for structural defects in the crystal, in particular threading dislocations.

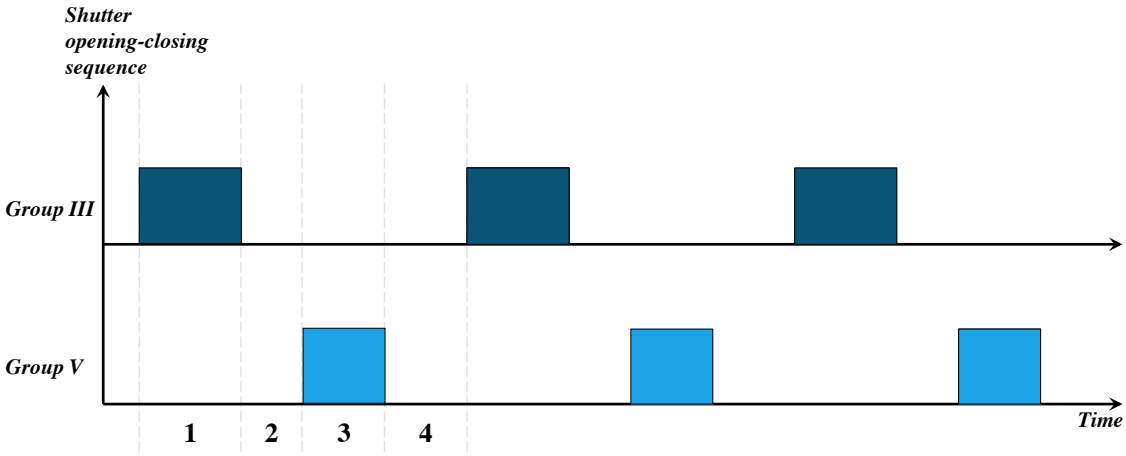

FIGURE 3.4. *Illustration of the group III and V shutters basic sequence repeated in order to obtain Migration Enhanced Epitaxy (MEE): 1) Group III shutter open, 2) Group III shutter closed and migration of the adatoms, 3) Group V shutter open, 4) Group V shutter closed and desorption of the excess adatoms.*

In order to influence the growth mode adopted by the epitaxial film, a special MBE technique called Migration Enhanced Epitaxy (MEE) has been developed by Horikoshi *et. al.* in the 1980's [3.7]. This technique uses the fact that group III elements such as Ga and Al have long migration lengths on the growth interface under a group V-free atmosphere. As a result, in the absence of group V adatoms, group III adatoms will fully cover the growth surface. By carefully engineering the opening and closing sequence of group III and group V effusion cells shutters, an alternate supply of group III and group V adatoms is achieved, resulting in a smooth 2D growth. The MEE sequence, presented in FIGURE 3.4, consists of repeating the four following steps:

1. Opening the group III shutter just long enough to deposit the exact quantity of material required for the growth of a monolayer,
2. Closing the group III shutter and letting enough time for group III adatoms to migrate and fully cover the growth surface,
3. Opening the group V shutter to deposit enough material to complete the monolayer,
4. Closing the group V shutter and letting enough time for the excess group V adatoms to be desorbed from the surface and pumped out.

Although resulting in relatively slow growth rates, this technique enables a very smooth 2D growth even at low substrate temperatures. Therefore, it is particularly helpful for challenging growth sequences such as the nucleation step in the case of lattice-mismatched heteroepitaxy.

3.2 Heteroepitaxy of III-V on Si for solar cells applications

3.2.1 Main challenges: APD formation, threading dislocations and thermal expansion mismatch

The subject of study of this thesis is the development of epitaxially grown III-V on Si multijunction solar cells, in particular III-V/Si double junction architectures where the Si bottom cell acts as a substrate. Multiple theoretical studies of dual junction solar

cells have shown that, when using a Si bottom cell, a top cell bandgap of about 1.7 eV is required for optimal performance [3.8-3.10]. FIGURE 3.5 shows the bandgap of usual III-V materials and some group IV materials (Si, Ge) as a function of their lattice constant. There is no conventional III-V material with a bandgap close to 1.7e V and lattice-matched with Si: the usual materials with the closest lattice-match to Si are GaP and AlP, both indirect semiconductors with bandgaps of 2.27 eV and 2.49 eV at 300 K, respectively [3.12]. Dilute nitride materials such as GaNAsP, with some nitrogen incorporated in the crystal lattice, can be lattice-matched with Si but their epitaxial growth is extremely challenging – with miscibility and phase separation being major issues, among others – and high quality GaNAsP has not yet been demonstrated [3.13]. Therefore, we did not focus on dilute nitride materials. A lattice-mismatched approach is consequently needed for dual junction III-V/Si architectures.

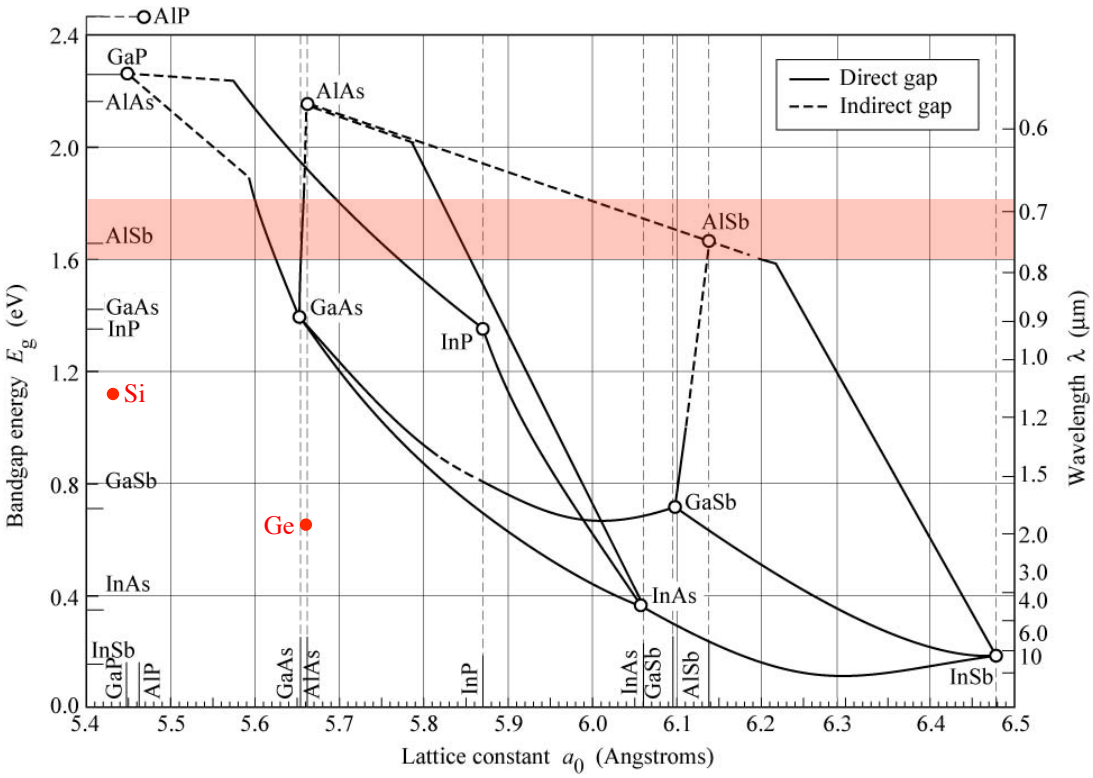

FIGURE 3.5. *Bandgap as a function of the lattice parameter for usual III-V materials as well as some common group IV materials. The 1.6-1.8 eV target window for a top cell in a III-V/Si dual junction architecture is highlighted in red. Adapted from Ref. [3.11] – No permissions required.*

Lattice-mismatched epitaxial growth of III-V materials on Si leads to three challenges:

1. Anti-phase domains (APDs) due to polar-on-nonpolar growth,
2. Misfit and threading dislocations due to lattice mismatch,
3. Thermal cracks due to the difference of thermal expansion coefficients.

Thermal cracks can be reduced and even eliminated by limiting the total thickness of the lattice-mismatched epilayers. Indeed, thermal cracks appear during the last step of the epitaxial growth, when the cell is cooled down to room temperature, because of the difference in thermal expansion between the Si substrate and the III-V epilayers. By reducing the thickness of the lattice-mismatched epilayers and controlling the cooling rate, the residual strain can be controlled, leading to fully relaxed epilayers with a reduced density, or even an absence, of thermal cracks. Growth techniques using thin buffers are, thus, highly beneficial.

Although thermal cracks can be avoided to some extent, APDs and dislocations are more complex defects and their reduction or elimination requires more sophisticated strategies, as detailed in Sections 3.2.2 to 3.2.5.

3.2.2 Strategies to reduce APD formation

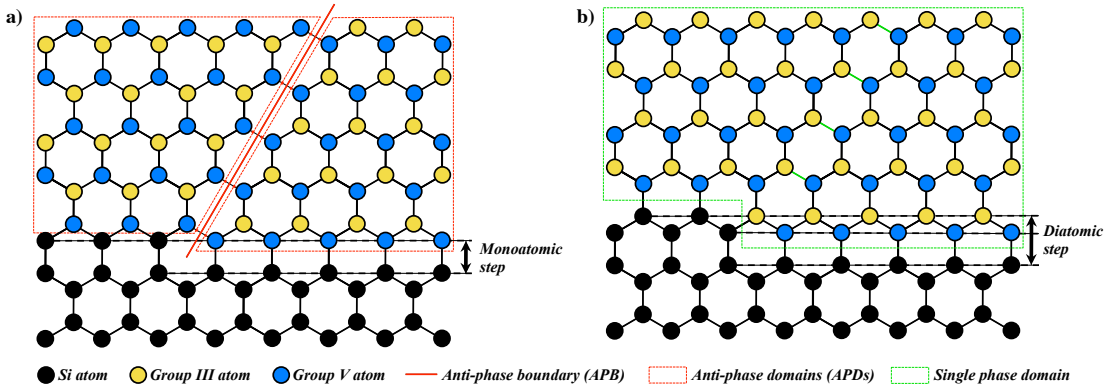

FIGURE 3.6. a) *Growth of III-V on (001)-Si with one-step terraces, leading to the formation of Anti-Phase Domains (APDs) separated by an Anti-Phase Boundary (APB).* ***b)*** *Growth of III-V on (001)-Si with two-step terraces, without APDs.*

Anti-Phase Domains (APDs) are defects directly related to the nature of the substrate and the epilayers: III-V materials are binary crystals where atoms from 2 successive layers are not interchangeable, whereas Si and other group IV materials are monoatomic crystals where any atom can occupy any site in the lattice. As native (001)-Si surface consists of terraces separated by monoatomic steps, direct integration of a binary III-V material will result in opposite crystalline domains in the epilayer, as shown in FIGURE 3.6a). Between these APDs, an Anti-Phase Boundary (APB) will act as a recombination surface, leading to a serious reduction in device performance. In order to ensure the growth of a single-phase domain III-V material, a Si surface with two-step terraces is required, as shown in FIGURE 3.6b).

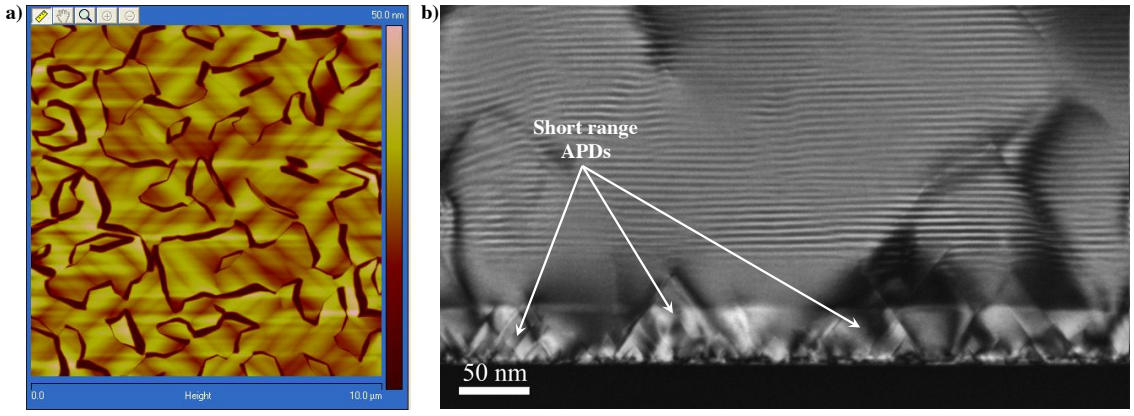

FIGURE 3.7. a) *Top-view Atomic Force Microscopy (AFM) image of an APD-rich sample. Each dark line is an Anti-Phase Boundary (APB).* ***b)*** *Side-view Transmission Electron Microscopy (TEM) image of a III-V on Si sample exhibiting short-range self-annihilating APDs.*

Fischer *et. al.* have shown that, using (001)-Si wafers with a 4 ° to 6 ° offcut toward the [110] direction annealed at high temperature (>900 °C) just prior to growth, such a surface with two-step terraces can be achieved [3.14]. Kroemer has presented a more complete description of the issue, explaining the origin of this two-step structure on offcut wafers after annealing [3.15]. However, it is important to note that, even if the upper epilayers of III-V materials grown on Si present no APDs using this technique, short-range APDs can still appear at the III-V/Si interface and self-annihilate after a few nanometres. Although these short-range APDs will not directly impact the devices grown in the upper epilayers, they will be nucleation centres for

threading dislocations and, therefore, will contribute to a lower material quality. Eliminating these short-range APDs is, thus, still an important concern. FIGURE 3.7a) shows a top-view AFM image of the surface of a III-V on Si sample exhibiting a high density of APDs, each dark line being an APB between two APDs. FIGURE 3.7b) shows a side-view Transmission Electron Microscopy (TEM) image of a III-V on Si sample exhibiting short-range self-annihilating APDs.

3.2.3 Impact of threading dislocations on solar cells' performance

Misfit and threading dislocations are line defects due to the difference of lattice parameters between two materials. As a III-V material with a different lattice constant – such as GaAs – is epitaxially grown on Si, the first epilayers will follow the crystalline pattern of the underlying Si substrate with the same lattice constant. As a result, in the first steps of the epitaxial growth, the epilayers will be strained but dislocation-free thanks to the elasticity of the material. However, the strain will increase with the thickness of the deposited layer, up to a point where the elasticity of the material alone cannot accommodate the strain and dislocations appear.

Dislocations can be classified in two main categories: misfit dislocations and threading dislocations. As shown in FIGURE 3.8a), misfit dislocations propagate in straight line in a plane parallel to the III-V/Si interface. Therefore, they are contained in the interface between the materials and do not directly impact the material quality of the active epilayers. However, misfit dislocations cannot extend indefinitely into that plane and they bend at a 60 ° angle into a more energetically favourable configuration called a Threading Dislocation (TD), as shown in FIGURE 3.8b). TDs propagate upwards within the (111) plane into the active region of the devices. There, they act as recombination centres for minority carriers. As a result, the lifetime and diffusion length of minority carriers are reduced and the performance of the devices is impaired. The main metric when considering materials with TDs is the Threading Dislocation Density (TDD), counted in unit per square centimetre (cm^{-2}).

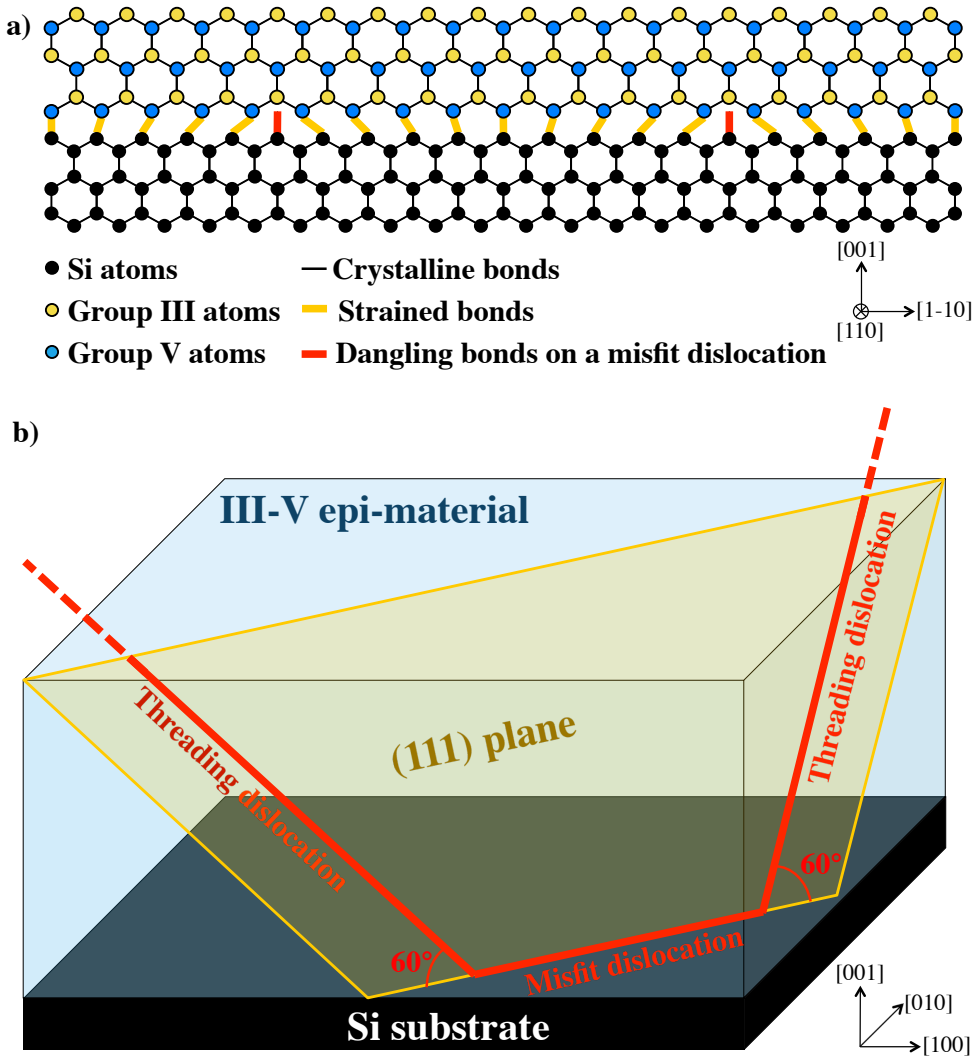

FIGURE 3.8. a) *Side view of the III-V/Si interface, showing the strained crystalline bonds and the dangling bonds on a misfit dislocation.* ***b)*** *Misfit and threading dislocations nucleating at the III-/Si interface and propagating in the (111) plane.*

Yamaguchi *et. al.* have developed a relatively simple model for the impact of TDs on the performance of III-V solar cells [3.16]. Considering a TDD ρ_{TDD} with TD perfectly uniformly spaced, the average spacing W_{TDD} between two TDs is given by:

$$W_{TDD} = \frac{1}{\sqrt{\pi \rho_{TDD}}} = (\pi \rho_{TDD})^{-\frac{1}{2}} \tag{3.1}$$

The classic diffusion equation for electrons (similar for holes) is then given by:

$$\frac{\partial n}{\partial t} = D_n \frac{\partial^2 n}{\partial^2 z} \tag{3.2}$$

Solving the one-dimensional diffusion equation using a classic separation of variables with the boundary conditions $n(z=0)=0$ and $n(z=W_{TDD})=0$, we obtain:

$$n(z,t) = n_0 sin\left(\sqrt{\frac{\pi^3 \rho_{TDD}}{4}} z\right) exp\left(-\frac{\pi^3 \rho_{TDD} D_n}{4} t\right) = n_0 sin\left(\frac{z}{L_n}\right) e^{-\frac{t}{\tau_n}} \quad (3.3)$$

where $L_n=\sqrt{(4/\pi^3 \rho_{TDD})}$ is the diffusion length and $\tau_n=4/\pi^3 \rho_{TDD} D_n$ is the lifetime of electrons associated with non-radiative recombination on TDs. The same relations are valid for holes.

Considering TDs as non-saturated deep defects, the SRH recombination rate per volume unit associated with TDs, dominated by recombination in the depletion zone of the cell, can be derived from equation (2.52):

$$R_{SRH,TD}(V) = \frac{n_i}{\tau_n + \tau_p} e^{\frac{qV}{2k_B T}} = \frac{\pi^3 \rho_{TDD} n_i}{4\left(\frac{1}{D_n} + \frac{1}{D_p}\right)} e^{\frac{qV}{2k_B T}} \quad (3.4)$$

with the corresponding recombination saturation current density given by:

$$J_{0,SRH,TD} = qW_D R_{SRH,TD}(0) = q\frac{\pi^3 \rho_{TDD} n_i W_D}{4\left(\frac{1}{D_n} + \frac{1}{D_p}\right)} \quad (3.5)$$

As the saturation current density is directly proportional with ρ_{TDD}, reducing the TDD to a minimum is extremely important for optimal cell performance.

It is also important to note that, as TDs nucleate at the III-V/Si interface, any imperfection on this interface, such as short-range APDs, will promote the formation of additional TDs. Similarly, the nucleation conditions of the initial III-V epilayers on Si will strongly impact the final TDD, in particular the coalescence of islands in the transition from a Stranski-Krastanov (SK) growth mode back to a Frank-Van Der Merwe (FM) growth mode. The size and the density of islands during coalescence are especially important. Therefore, good control of the nucleation sequence is key to a low TDD.

Two conjugated TDs can also lock together and self-annihilate or merge into a unique TD when they meet. This can be promoted using thick buffers or dislocation filters, as

detailed in Section 3.2.5. Moreover, dislocations can glide when subjected to changes in temperatures. Thermal cycling of samples can, therefore, help reduce the TDD by encouraging conjugated TDs to meet and lock together.

3.2.4 Reducing the threading dislocation density through metamorphic buffers

In order to reduce the TDD, the straightforward solution is to grow a thick III-V buffer until most of the TDs self-annihilate or merge together. However this technique requires extremely thick buffers (up to tens of micrometres), leading to very long growth times and high material consumption. As a result, thick buffers are expensive. Moreover, the thicker the grown material, the harder it is to avoid thermal cracks.

Metamorphic buffers are a technique to achieve a moderately thick buffer with a low TDD. Instead of direct growth of highly mismatched materials one on top of the other, metamorphic buffers start with a lattice-matched nucleation layer and gradually adjust the ratio of materials in the III-V compound. The lattice parameter of the grown material is progressively modified to end up with relaxed active layers of the desired lattice parameter with a moderate TDD. As the lattice mismatch between two successive epilayers is small, the TDD is kept relatively low throughout the metamorphic buffer, as shown in FIGURE 3.9.

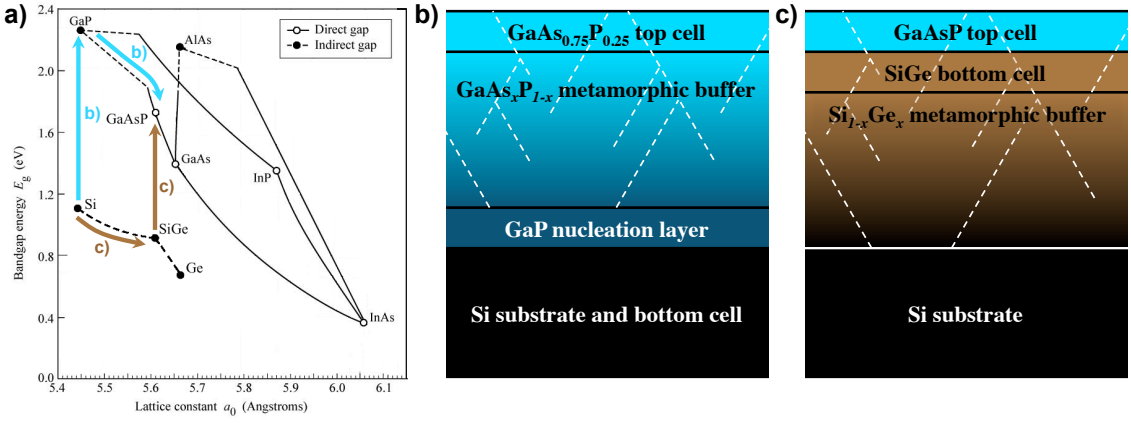

FIGURE 3.9. a) *Illustration of the metamorphic pathways for the growth of 1.7 eV GaAsP solar cells on Si. Adapted from Ref. [3.11] – No permissions required.* ***b)*** *III-V/Si dual junction solar cell using the GaAsP/GaP/Si metamorphic pathway.* ***c)*** *III-V/Si dual junction solar cell using the GaAsP/SiGe/Si metamorphic pathway.*

When considering the growth of III-V on Si for dual junction photovoltaic applications, two metamorphic pathways are possible:

a) Growth of a GaP nucleation layer nearly lattice-matched to Si followed by a $GaAs_xP_{1-x}$ metamorphic buffer with a gradual increase of the As content *x* until 1.7 eV $GaAs_{0.75}P_{0.25}$ active layers are reached, as shown in FIGURE 3.9b). This pathway has mainly been investigated by teams at Ohio State University [3.17] and Yale University [3.18]. The lowest TDD achieved so far using this technique is 4.0×10^6 cm^{-2} [3.18].
b) Growth of a $Si_{1-x}Ge_x$ metamorphic buffer on Si with an increasing Ge content *x* until the required lattice parameter is reached for the lattice-matched integration of a SiGe bottom cell and a GaAsP top cell, as shown in FIGURE 3.9c). This pathway has mainly been investigated at University of New South Wales (UNSW) with a TDD of 3×10^5 cm^{-2} obtained in the SiGe bottom cell and 2.8×10^6 cm^{-2} in the GaAsP top cell [3.19].

The main challenge using this pathway consists in reducing the TDD by an additional order of magnitude to get under 10^6 cm^{-2}. Indeed, recent progress has been limited using metamorphic buffers and few improvements have been achieved over the past 10 years. The thickness of the buffer is another issue of this pathway: as the final TDD can be improved by using a slower grading, better results will be achieved with thicker metamorphic buffers. Although thinner than the direct thick buffers described earlier, metamorphic buffers of 3 to 5 µm are still required to achieve TDDs in the 10^6 cm^{-2}.

3.2.5 Reducing the threading dislocation density through Strained Layer Superlattice Dislocation Filter Layers

Another pathway to reducing the TDD by an order of magnitude, to get to 10^5 cm^{-2} or lower, is the use of Strained Layer Superlattice (SLS) Dislocation Filter Layers (DFLs). As opposed to metamorphic buffers, the leap in lattice constant is executed at once, using direct integration of AlGaAs materials on Si with a relatively large lattice-mismatch (around 4 %). Because of this sizable lattice-mismatch, the first epilayers will grow following a Stranski-Krastanov (SK) mode before coalescence of the

islands. This will lead to a relatively wavy growth surface, non-ideal for the fine engineering of low dimensional structures. Therefore, an AlAs/GaAs superlattice buffer is grown, in FM mode, after the nucleation layer in order to smooth out the deposition and achieve a flat growth surface, thanks to the particular wetting properties of Aluminium leading to the high surface tension of AlAs.

Once a flat growth surface is reached, the SLS DLFs can be grown. SLS DFLs consist of very thin (usually a few nanometres or less) strained layers, for example InAlAs, separated by AlGaAs layers, as shown in FIGURE 3.10. A dislocation filter usually consists of a Strained Layer Superlattice (SLS) made of about 20 alternating AlGaAs/InAlAs layers before the growth of a thicker AlGaAs separation buffer, also called spacer. As the InAlAs strained layers are thinner than their critical thickness, they are in an elasticity regime and are compressively stressed without generating new dislocations. As a result, TDs from the bulk of the material do not have enough energy to counterbalance this strain and bend back into misfit dislocations in the SLS DFL. As shown in FIGURE 3.11, a TD can eventually self-annihilate (a) or merge (b) with another conjugated TD, be pushed to the side of the wafer (c) or build up enough strain in the DFL to go through it (d). If properly engineered, each DFL can reduce the dislocation by half to a full order of magnitude.

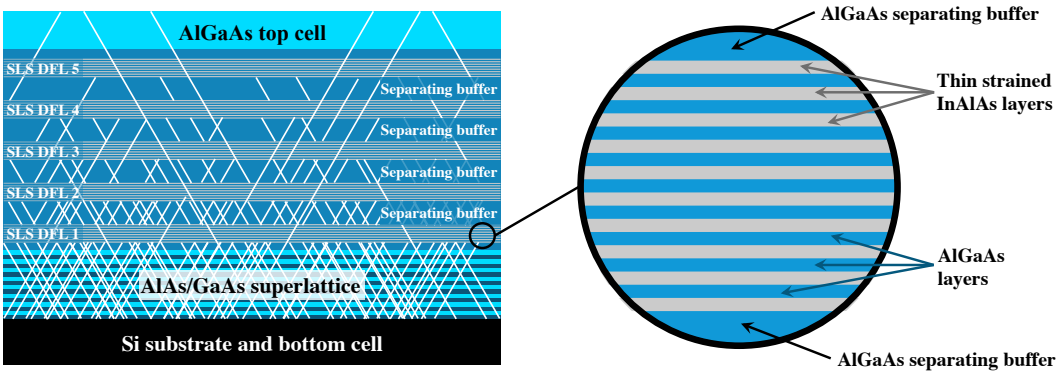

FIGURE 3.10. *Structure of an AlGaAs solar cell grown on Si using an AlAs/GaAs superlattice followed by 5 SLS DFLs divided by AlGaAs spacers. Detail of the DFL structure is given on the right.*

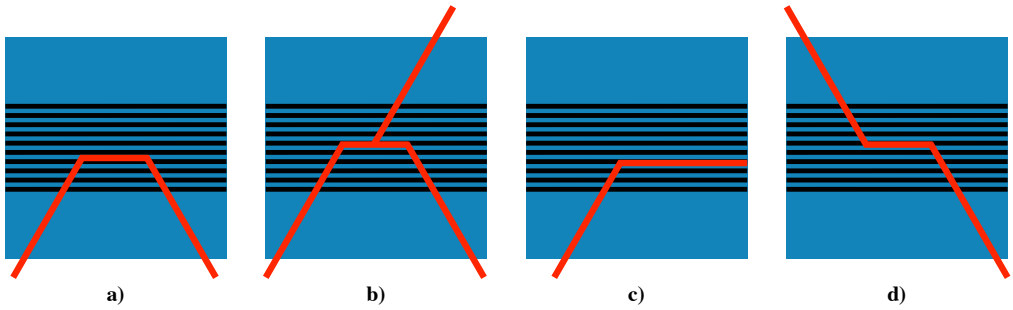

FIGURE 3.11. *Interaction of Threading Dislocations (TDs) with Strained Layer Superlattice (SLS) Dislocation Filter Layers (DFLs).* ***a)*** *Self-annihilation of two conjugated TDs.* ***b)*** *Merging of two conjugated TDs.* ***c)*** *TD pushed to the side of the wafer.* ***d)*** *TD breaking through the SLS DFLs.*

Because of the large lattice-mismatch between the substrate and the nucleation layer, the TDD will be high before the DFLs, in the 10^9 cm^{-2} to 10^{10} cm^{-2} range, as shown in FIGURES 3.10 and 3.12. Each DFL will then reduce the TDD 2 to 10 times. Thermal Cycle Annealing (TCA) can also be performed after the growth of each SLS DFL in order to increase the mobility of misfit and threading dislocations. The chances of conjugated threading and/or misfit dislocations encountering each other, leading to self-annihilation or merging, are thus increased and the TDD is further reduced throughout the buffer.

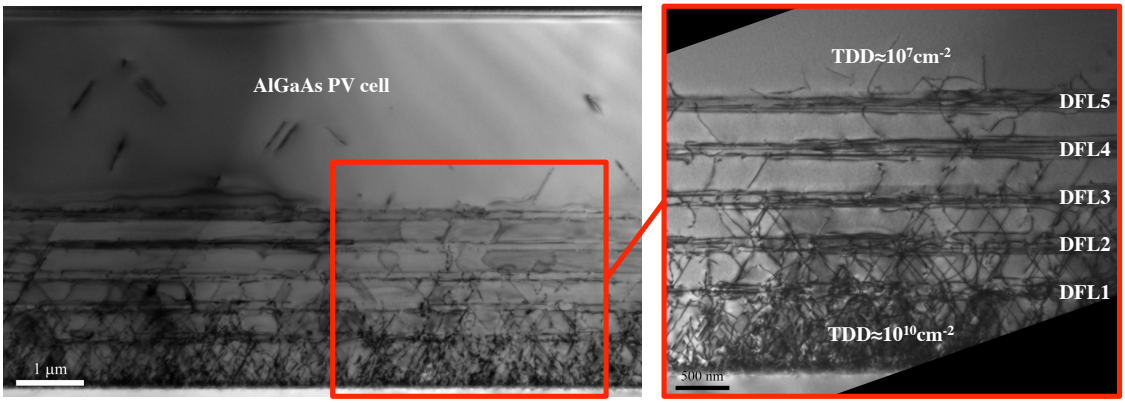

FIGURE 3.12. *Bright-Field cross-sectional TEM imaging of an AlGaAs solar cell monolithically grown on Si using five SLS DFLs, showing the TDD reduction from about 10^{10} cm^{-2} to about 10^7 cm^{-2}. Right image shows a detail of the five DFLs and the associated TDD reduction.*

The team of Professor Huiyun Liu at UCL has been able to achieve TDD values under 10^6 cm^{-2} this way, using only 4 DFLs coupled with TCA steps, opening the way to high performance III-V lasers monolithically grown on Si [3.20]. The goal of this PhD is to extend these excellent laser results to III-V on Si photovoltaic solar cells. FIGURE 3.12 shows TEM imaging of the TDD reduction using SLS DLFs on early experimental AlGaAs on Si solar cells. This experimental work is further detailed in Chapter 5.

3.3 Material characterisation

With the exception of TEM measurements, mainly carried out by the team of Professor Gregory J. Salamo at University of Arkansas, the material characterisation methods presented hereafter have been performed at UCL by myself, with the help of Dr. Mingchu Tang for AFM and XRD measurements.

3.3.1 Atomic Force Microscopy (AFM)

Atomic Force Microscopy (AFM) is a non-optical microscopy technology – using scanning-probe techniques to provide an image of the morphology of a surface – with a resolution below one nanometre. This allows for a precise mapping of the surface of a grown sample, giving an idea of the growth regularity, smoothness and uniformity. It enables the detection of some defects such as APDs, as shown in FIGURE 3.7a).

Operating principles of AFM systems in contact mode are relatively simple: a sharp tip fixed to a flexible cantilever is put in contact with the surface to be analysed. A laser is shone on the cantilever and a photodiode detector measures the deflection of the laser due to the bending of the cantilever. The stage on which the sample is mounted slowly moves in the horizontal plane, under the tip-cantilever ensemble, so that the tip slowly brushes the surface. A feedback loop ensures a constant bending of the cantilever by moving the sample up and down, depending on the position of the tip on the surface, thus recording the measured height of the sample surface. The main issue of this operation mode is possible damage to the surface due to the tip grazing it, as well as possible distortions in the final image.

Tapping mode, used in this work, is slightly subtler. Instead of direct contact of the tip with the surface, the cantilever is set to oscillate vertically at a determined frequency. As the tip-cantilever ensemble is brought down on the surface, the oscillating tip will tap the surface, leading to a reduced oscillation amplitude because of the energy dissipated with each tapping. Similar to the contact mode, a feedback loop ensures constant oscillation amplitude by moving the stage and the sample vertically, thus recording the surface morphology of the sample. With this technique, a vertical resolution of about 0.1 nm can be achieved, with a lateral resolution of about 30 nm due to the geometry of the tip.

3.3.2 X-Ray Diffraction (XRD)

X-Ray Diffraction (XRD) is a characterisation technique used to assess the crystalline properties of the external layers of a material. It is based on the diffraction of an X-ray beam, reflected by the atoms of the surfacing layers of the sample, as shown in FIGURE 3.13. With θ the angle of the incident/reflected beam, λ the wavelength of the beam, d_{hkl} the interplanar spacing for (hkl) reflection planes – with (hkl) the Miller indices of the considered crystal planes, in our case (100) – and n an integer, the condition for constructive interference in the reflected beam is $2d_{hkl}\sin\theta=n\lambda$ according to Bragg's law. As X-rays have wavelengths in the order of magnitude of the lattice parameters of studied semiconductors materials, in the tenths to tens of nanometres, they are particularly suited to this kind of analysis.

Crystallographic information – in particular the lattice parameter $a_0=d_{hkl}/\sqrt{(h^2+k^2+l^2)}$ – can then be extracted from the peaks in the measured reflected beam intensity, corresponding to constructive interferences. As the lattice parameter is a function of the semiconductor composition, the composition of relaxed III-V compound materials can be measured using XRD. With materials of known composition grown on lattice-mismatched substrates, XRD can be used to assess the degree of relaxation and the residual stress in the epilayer, by comparing the diffraction pattern with the one of a lattice-matched sample.

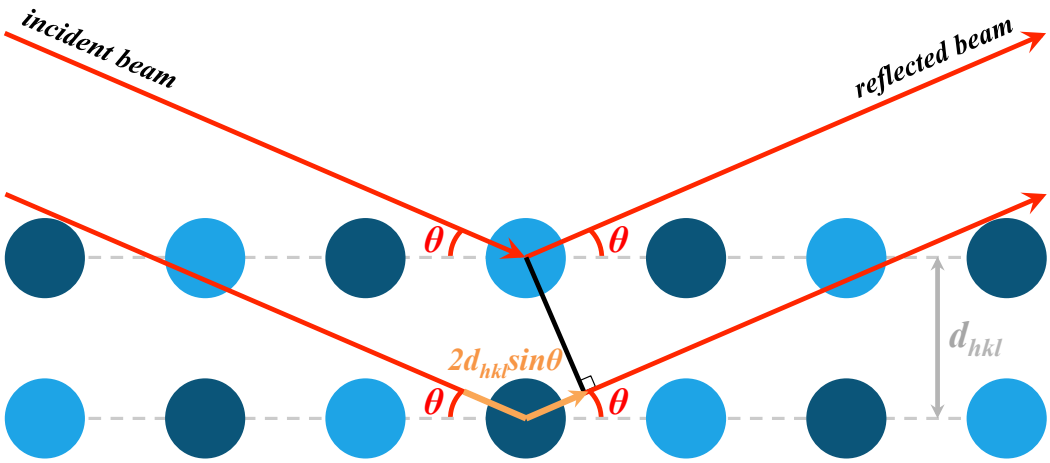

FIGURE 3.13. *Illustration of Bragg's law on which X-Ray Diffraction (XRD) measurements are based.*

An XRD system consists of an X-ray source and an X-ray detector able to move around a central stage on which the sample lays flat. The source and the detector are tilted at the same angle θ from the sample plane. The intensity of the reflected beam is recorded as a function of the variable incidence/reflection angle θ.

3.3.3 Transmission Electron Microscopy (TEM)

Transmission Electron Microscopy (TEM) is the most powerful tool used in this work to assess the structure and material quality of grown samples. Unlike AFM and XRD, which only inform us about the surface of the sample and the atomic layers immediately under it, TEM gives direct crystallographic information about the bulk of the epilayers. Thus, TEM can show a wide range of structures inside the epitaxial film, including superlattices, quantum wells and quantum dots, interfaces between materials, and defects such as APDs and TDs. Therefore, it is the main analysis tool to determine the TDD of III-V samples grown on Si. For the work presented in this thesis, TEM measurements have been carried out at University of Warwick using a JEOL 2100 system and at University of Arkansas Institute for Nanoscience and Engineering in a FEI Titan 80–300 S system.

Cross-sectional TEM, used for the work presented here, is obtained by bombarding, under vacuum, a very thin slice of the sample – cut perpendicularly to the growth plan

– with an electron beam. A substantial amount of preparation is, hence, needed in order to obtain this thin slice from the sample, using for example ion milling. During the measurement, electrons fired on the sample can then pass through it or interact with its atoms, eventually leading to electron diffraction. A detector on the other side of the sample will then collect the information from the transmitted or diffracted electrons. By adjusting the focus point of the detector, these transmitted or diffracted electrons can be collected, leading to Bright-Field (BF) and Dark-Field (DF) imaging modes.

Under BF conditions, transmitted electrons are directly analysed. Electrons interacting with the crystal lattice are, thus, ignored and the image is directly derived from the blocking of electrons within the sample, similarly to how X-ray medical images are obtained. As a result, the image will be brighter where lots of electrons are transmitted and darker where few electrons are able to pass through the sample. DF conditions use diffracted electrons as the source of information and, therefore, are particularly sensitive to defects impacting the crystal lattice. FIGURE 3.14 shows examples of the same III-V on Si sample, grown using dislocation filters, under BF (a) and DF (b).

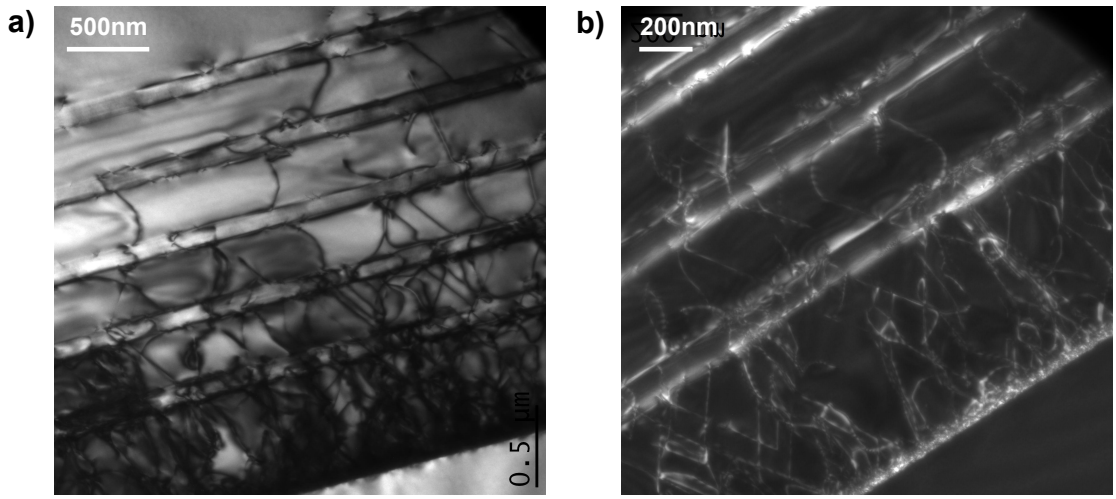

FIGURE 3.14. *Cross-sectional TEM images of AlGaAs grown on Si using dislocation filters under Bright-Field (a) and Dark-Field conditions (b). Defects are shown with a brighter contrast under DF.*

3.3.4 Photoluminescence (PL)

Photoluminescence (PL) is an important analysis technique as, contrary to structural characterisation tools such as AFM, XRD and TEM, it gives direct information on the optoelectronic properties of the grown sample, before the fabrication of devices. PL uses the absorption and reemission characteristics of semiconductors, presented in Chapter 2, in order to access parameters such as the bandgap of the device or the number of defects in it.

A PL measurement apparatus usually consists of a laser with photon energy higher than the expected bandgap of the measured sample, a sample stage or holder, an optical system including lenses and a monochromator, and a detector coupled with a signal analyser software. The laser is shone on the sample, exciting electrons from the valence to the conduction band and leading to a high concentration of free electrons and holes in the sample. These free carriers will recombine after some time, in particular through band-to-band radiative emission. These reemitted photons are collected by the optical system and focused on the detector. The monochromator decomposes the incoming emitted light by wavelength, giving access to the spectral response of the sample. The peak of the wavelength-dependent intensity of the PL spectrum gives the bandgap of the sample. In the case of a more complex structure including multiple materials or low dimension structures such as quantum wells or quantum dots, multiple peaks will be observed, each peak corresponding to a different structure or material.

Moreover, as radiative recombination compete with non-radiative recombination inside the photo-excited sample, comparing the amplitude of the PL peaks between different samples gives information on the relative material quality and defect densities between the samples. Indeed, the non-radiative recombination rate is directly related to the defect density whereas the radiative recombination rate is mainly governed by the material band structure. As a result, the PL peak amplitude informs about the ratio between the radiative and the non-radiative recombination rates. Comparing different samples made of the same material; the sample with the highest material quality can be determined, as it will exhibit the strongest PL peak intensity.

3.4 Device fabrication

The full device fabrication process was performed by me at the London Centre of Nanotechnology (LCN), with the help of Dr. Qi Jiang, Dr. Siming Chen, and Dr. Sabina Hatch.

3.4.1 General process

Once grown, samples possess the semiconductor structure of solar cells but are not yet photovoltaic devices, as they need contacts to be connected to an external circuit in order to produce power and be characterised. Device fabrication is performed in a cleanroom environment in order to obtain working devices from which a photocurrent and a photovoltage can be extracted. In the work presented here, devices are AlGaAs and GaAs solar cells grown on Si and GaAs. In order to probe the solar cell without interference from the underlying buffer and substrate, directly contacting the sample from both top and bottom surfaces is excluded. As a result, an additional wet etching step is required to access the contacting layer grown between the buffer and the active layers of the device. This is particularly important for samples grown on Si, as the highly defective III-V/Si interface can greatly impact the performance of devices.

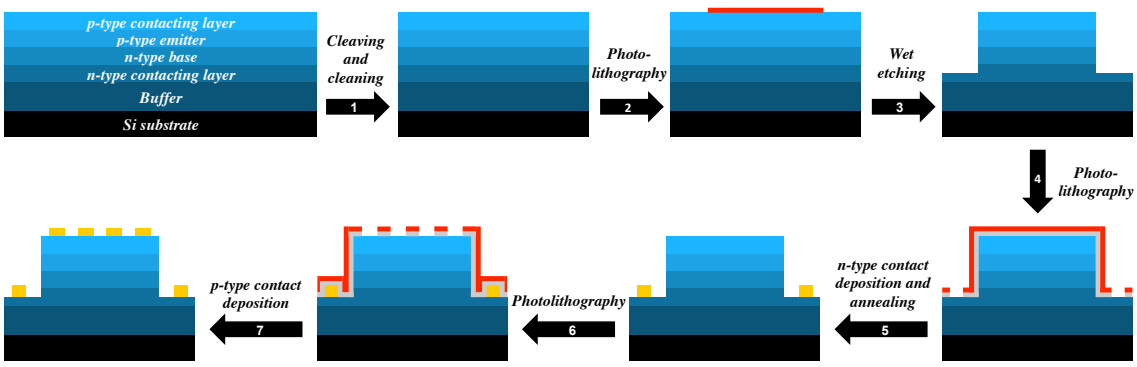

FIGURE 3.15. *Simplified flow-chart of the standard processing steps for device fabrication of III-V photovoltaic solar cells grown on Si.*

The standard processing steps, shown in FIGURE 3.15, are the following:

1. Preparation of samples for device fabrication: cleaving and cleaning,

2. Photolithography for wet etching and device separation,
3. Wet etching and device separation,
4. Photolithography for deposition of n-type contacts,
5. Deposition and annealing of n-type contacts,
6. Photolithography for deposition of p-type contacts,
7. Deposition of p-type contacts.

3.4.2 Photolithography

Photolithography is a microfabrication technique consisting in selectively covering parts of the sample by patterning a thin layer of a photosensitive chemical – called photoresist – previously deposited on top of it. After photolithography, some areas of the sample are, thus, protected by the photoresist while other areas are exposed and can be processed during subsequent fabrication steps, such as etching or metal contact deposition.

In the present work, positive photoresists, which are degraded when exposed to UV light, have been used. Negative photoresists, which, on the contrary, become polymerized and consequently harder to dissolve once exposed to UV light, can also be used. In the present case, we limit ourselves to the presentation of processes using positive photoresist, as they are the ones used throughout our work.

The photoresist is spin-coated on top of the clean, dry sample in order to obtain a very uniform and thin layer (about 2000 nm-thick). The main property of positive photoresists is to become soluble in specific solvents, called developers, after exposure to UV light. Using this property, the photoresist-coated sample can be exposed to UV light through an optical mask, thus transferring the geometric pattern of the mask onto the sample. The developing step then removes the exposed photoresist, revealing the areas to be processed. A mask aligner is used to accurately align the mask to the sample with a precision of less than a micrometre. After processing (wet etching or contact deposition), the resist is cleaned using a special remover solvent.

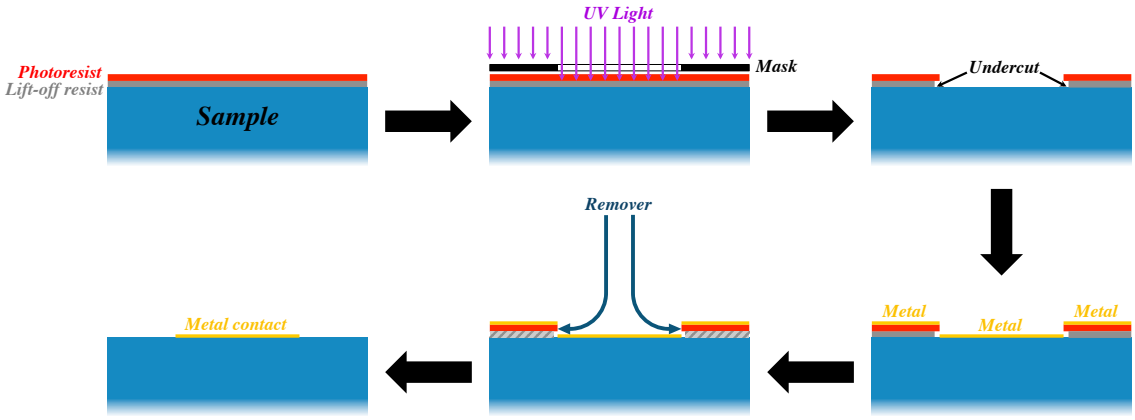

FIGURE 3.16. *Flow-chart of the photolithography, metallisation and lift-off process using a lift-off resist.*

When performing photolithography before deposition of metal contacts, an additional lift-off resist is spin-coated on the sample before deposition of the photoresist. The role of the lift-off resist is to create an undercut beneath the photoresist. This undercut allows the remover solvent to penetrate underneath the evaporated metal covering the sample and to dissolve the resist. As shown in FIGURE 3.16, a lift-off of the metal contact is, thus, achieved.

3.4.3 Wet etching

Wet etching is used to access the underlying n-type contacting layer of the samples, by creating a vertical cavity into the material using an acid solution. The process also enables a physical separation and isolation between the devices, creating "mesa" structures. In order to obtain a sharp structure profile with vertical sidewalls, a solution with anisotropic etch rates is used so that the preferential direction of the etching is vertical. Solutions with multiple orders of magnitude between the etch rates in the [100] direction and the [111] direction are, thus, required. When etching different materials within the same sample, such as AlAs/GaAs structures, a solution with a similar etch rate for all the etched materials is used for precise fabrication. In our case a H_2SO_4:H_2O_2:H_2O (1:10:80) solution has been used. The etch depth can then be measured using a profilometer, which records the topography of the surface with a grazing stylus. Alternatively, dry etching techniques, such as Reactive Ion Etching

(RIE), can be used. In this case, a chemically reactive plasma is created in order to etch a material.

Selective wet etching of defects can also be performed to calculate the defect density at the top surface of the sample. This is done using a selective wet etchant that will dig around the defect, resulting in a pit in the surface. The Etch Pit Density (EPD) can then be calculated to find out the defect density at the surface of the wafer.

3.4.4 Contact deposition

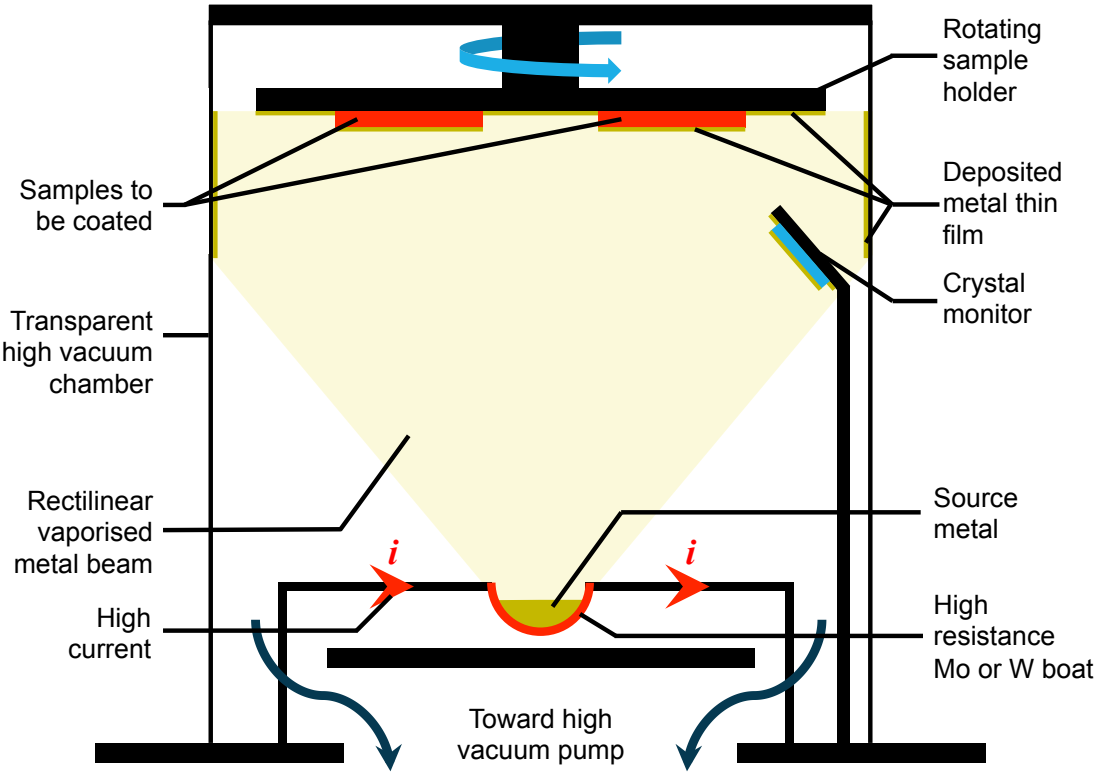

FIGURE 3.17. *Schematic of a thermal evaporator during metal contact deposition.*

Metal contacts are deposited on the grown samples using thermal evaporation or magnetron sputtering. As shown in FIGURE 3.17, thermal evaporation is achieved under high vacuum in an evaporator. The metals to be evaporated are cleaned and loaded in the evaporator in tungsten (W) or molybdenum (Mo) boats, facing the samples. Once a proper high vacuum (10^{-6} mbar to 10^{-7} mbar) is obtained, the metal is heated up by resistive heating, thanks to a very high current going through the boat,

until it reaches its evaporation temperature. Because of the high vacuum in the evaporator, metal atoms or molecules have a long mean free path and can travel unimpaired to the sample surface where they deposit and solidify. The deposition rate can be monitored using a quartz crystal monitor. In order to obtain good ohmic contacts, a high crystallinity is required. A slow deposition rate is, thus, recommended, especially during deposition of the first layers.

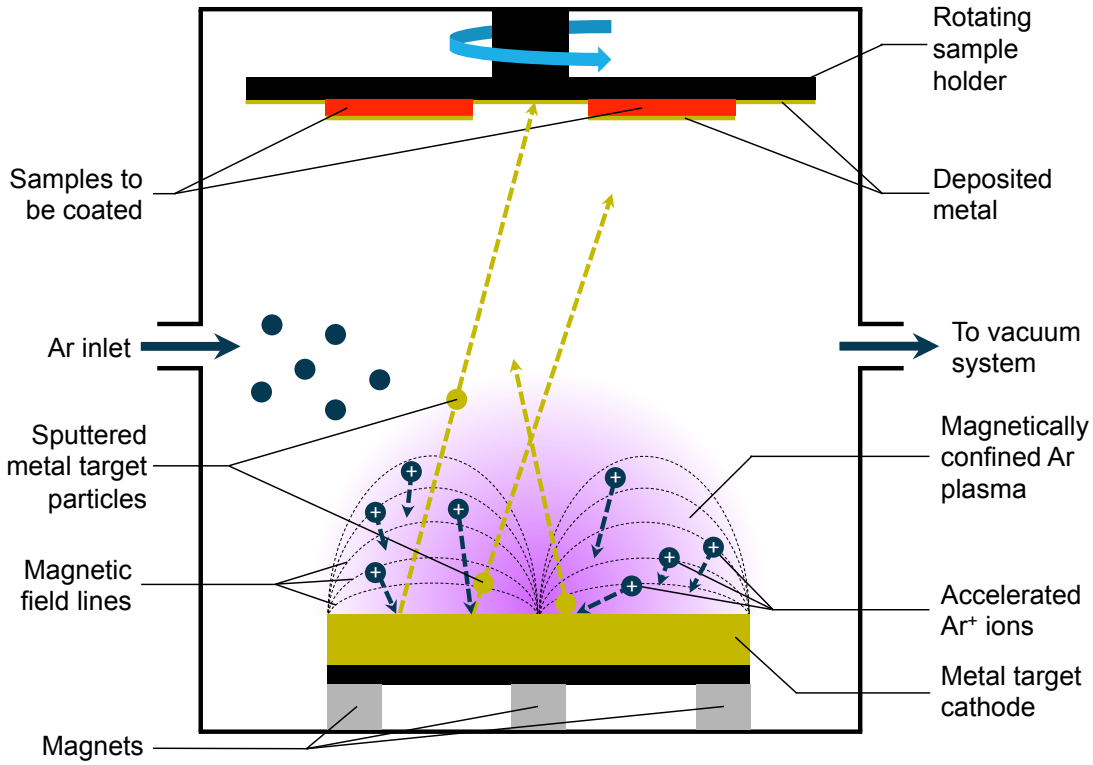

FIGURE 3.18. *Schematic of a sputterer during metal contact deposition.*

Magnetron sputtering of metal contacts takes place in a sputtering system, as shown in FIGURE 3.18. After loading the samples and the metal sources, the system is pumped down to working pressure. An inert sputtering gas, in our case argon (Ar) at low pressure (3×10^{-6} mbar), then fills the deposition chamber. Strong magnetic and electric fields are created by a magnetron under the selected source of material. Ar atoms are consequently ionized and accelerated. These high-energy Ar^+ ions bombard the source of material, called a target, ejecting material from it in the process. These ejected "sputtered" particles travel to the surface of the sample where they are deposited. The advantage of sputtering over thermal evaporation is that sputter

deposition of materials with a very high melting point, such as platinum or titanium, is relatively easy while they are close to impossible to deposit using thermal evaporation.

Different metals or combinations of metals are used depending on the type of contact (n-type or p-type), the type of semiconductor to be contacted, and the requirements of the contact (very low resistivity, ease of deposition, adherence to the semiconductor…). A low difference of electron affinity between the metal and the semiconductor is required in order to reduce the energy barrier for carriers at the metal-semiconductor junction and to obtain a good ohmic contact. Highly doped semiconductor contacting layers are, thus, preferable. In some cases, annealing of the contact is performed after thermal evaporation to force the diffusion of metal atoms into the semiconductor, hence lowering the energy barrier, and to improve the contact crystallinity. As a thin insulating oxide layer is present on the surface of the semiconductor, an oxide removal step is needed just prior to metal evaporation, using for example an ammonia-based solution.

3.5 Device characterisation

All the device characterisations presented in this thesis were performed by me using UCL facilities.

3.5.1 J-V curves in the dark and under illumination

J-V curve tracing is the most important characterisation technique for photovoltaic solar cells, as it gives access to information on the true performance of a device, including its possible sources of extrinsic inefficiencies such as defects or series/shunt resistances. A J-V curve is obtained by contacting the n-type and the p-type regions of the cell to a source-meter, using a four point probe to avoid parasitic probe/cell resistances. A voltage is then applied to the cell and the current flowing through it is recorded. As the performance of photovoltaic solar cells is impacted by the temperature, the measured cell is mounted on a temperature-controlled stage, keeping

it at a standard test temperature of 25 °C. J-V curves can be acquired under illumination or in the dark, leading to valuable insight into a cell's parameters.

The J-V curve under illumination is traced using a calibrated solar simulator lighting up the cell. The solar simulator approximates the AM1.5G spectrum by way of a filtered xenon arc lamp. A calibrated reference cell is used to set the power density on the cell stage to 1000 $W.m^{-2}$. The short-circuit current density J_{sc}, the open-circuit voltage V_{oc}, the fill factor, and the efficiency of the cell can be easily extracted from the J-V curve. Series and shunt resistances can also be estimated from it, as explained in Chapter 2.

However, because of small variations in the light power over time, a relatively important noise is recorded, in particular at low voltages. Therefore, extraction of detailed performance parameters – such as the saturation current density or the ideality factor – from the illuminated J-V curve is challenging. Acquisition of the J-V curve in the dark is a powerful technique to access these subtler cell parameters and to examine the diode behaviour of the cell, making it a very good tool to diagnose cells limitations. For cells with relatively small series and shunt resistances, a 2-diode model can even be fitted on the dark J-V curve, giving valuable information on the competition between recombination processes in the cell.

3.5.2 Suns-V_{oc}

Suns-V_{oc} is a characterisation technique pioneered by Ron Sinton at Stanford [3.21] to circumvent issues caused by parasitic series resistances, due to non-optimal cell processing, when acquiring J-V curves. To do so, the evolution of the open-circuit voltage V_{oc} of the cell is measured under variable illumination. As a result, no current flows through the cell during the measurement and the impact of series resistances is eliminated. Knowing the number of suns equivalent to the illumination source for each data point acquired, a pseudo J-V curve can be reconstructed assuming the superposition principle is valid. This pseudo J-V curve is in fact a calculated equivalent of the J_{sc}-V_{oc} curve under variable illumination.

As inefficiencies related to cell fabrication are removed, the pseudo J-V curve is an excellent image of the material limitations of the cell. Cell parameters such as the saturation current density J_0 and the ideality factor n can be easily and precisely extracted even with a suboptimal cell fabrication process. The lifetime of minority carriers can even be precisely extracted from Suns-V_{oc} measurements, provided that a few hypotheses are verified.

In practice, the Suns-V_{oc} curve is acquired using a flash lamp with an exponential decay and the V_{oc} is measured with a fast-response voltmeter. A reference Si cell, integrated into the system, measures the equivalent suns from the decaying flash. For cells with long lifetimes in the order of magnitude of the flash lamp decay time, such as high-quality Si solar cells, some mathematical correction is needed to take into account transient states [3.22]. As we work with direct III-V materials, the minority carrier lifetime is orders of magnitude shorter than the decay time of the lamp and this kind of correction is unnecessary.

The main challenge in characterising III-V photovoltaic cells with a Suns-V_{oc} system comes from the spectral mismatch between the reference cell and the measured cell. Indeed, as the flash lamp does not display an AM1.5G spectrum but instead a relatively infrared-rich spectrum, the measured cell and the reference cell "see" a different number of incoming suns. Filtering the reference cell can fix this issue [3.23] but an appropriate shortpass filter is then needed for each measured cell. Alternatively, using the V_{oc} extracted from a standard J-V curve under calibrated illumination, the spectral mismatch M [3.23] can be easily calculated, leading to a straightforward solution.

3.5.3 External Quantum Efficiency (EQE)

External Quantum Efficiency (EQE) provides the spectral response of a PV cell. Therefore, it is a valuable technique to examine the optical properties of a cell and a powerful diagnostic tool in case of poor J_{sc} performance. EQE is measured by focusing a monochromatic light beam onto the cell in a dark chamber and by measuring the induced current. Using a wide spectrum light source coupled with a monochromator, the wavelength of the incoming light beam can be modified and,

after calibrating the system with a cell of known absorption spectrum, the measured cell's relative quantum efficiency can be acquired. An absolute EQE can then be calculated from the cell's J_{sc}, measured separately using a solar simulator. Sources of optical inefficiencies can then be assessed. For example, a high recombination rate in the emitter due to high doping or strong surface recombination will cause a weak blue response, whereas an excessively thin base or a short minority carrier diffusion length due to a high defect density will result in a weak red response.

3.6 References

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Chapter 4

Modelling of III-V/Si Dual Junction Solar Cells

This chapter presents our efforts toward the development of an inclusive yet simple model to assess the potential performance of III-V/Si dual junction solar cells. The goal of this study was to prove the potential of the technology, as well as to evaluate some limitations in the design of the cells, in particular regarding the Threading Dislocation Density (TDD) in the top cell material. Some of the results presented here have already been published in *Solar Energy Materials and Solar Cells* [4.1]. Additional results, in particular regarding the impact of the TDD on luminescent coupling between the cells, have been presented at Photonics West OPTO 2016 – Physics, Simulation, and Photonic Engineering of Photovoltaic Devices V in San Francisco, California [4.2].

4.1 Research background and purpose

As presented in the preceding chapters, the combination of III-V single- or multi-junction solar cells integrated on a comparatively low-cost silicon substrate is a promising candidate for the low-cost fabrication of high efficiency solar cells. In particular, direct epitaxial growth of a III-V top cell on a silicon bottom cell acting as a substrate is a very elegant and potentially industrially relevant way to produce high-efficiency tandem solar cells on a low-cost substrate. Following the initial developments by Hayashi *et al*. in the 1990's [4.3] and the work carried out at NREL by Geisz *et al.* [4.4-4.5] in the 2000's, the technology has seen progress in recent years with contributions from teams at Ohio State University [4.6-4.8] and Yale University [4.9-4.10].

These recent results [4.6-4.10] have in common the buffer architecture used between the Si bottom cell and the III-V top cell: a $GaAs_xP_{1-x}$ metamorphic approach has been developed, starting with the growth of a nearly lattice-matched GaP nucleation layer directly on Si followed by a $GaAs_xP_{1-x}$ metamorphic buffer leading to a relatively low TDD in the $GaAs_{0.75}P_{0.25}$ top cell. A strong advantage of this pathway lies in the high bandgap of the $GaAs_xP_{1-x}$ metamorphic buffer, making it transparent to lower energy photons to be absorbed in the Si bottom cell. Although our experimental work presented in Chapter 5 focuses on the monolithic growth of 1.7 eV AlGaAs top cells on Si using Strained Layer Superlattice (SLS) Dislocation Filter Layers (DFLs), the $GaAs_xP_{1-x}$ metamorphic pathway was initially considered as a promising research area and our modelling work concentrated on this specific architecture. However the modelling method presented in this chapter is relatively versatile and could easily be adapted to AlGaAs/Si dual junction solar cells monolithically grown using SLS DFLs.

Multiple generic dual-junction models [4.11-4.14] have shown that, in a III-V/Si dual junction architecture, the top cell bandgap should lie between 1.6 eV and 1.8 eV. However few material-specific and architecture-specific detailed models of such structures have been developed so far to determine the exact bandgap needed for the top cell and the parameters influencing the efficiency of the dual-junction cell. Most

of the modelling work on dual-junction solar cells, including the aforementioned contributions, suffers from the lack of architecture-specific features and relies on theoretical absorption spectra, infinite cell thickness hypotheses, or dark-current calculations based on theoretical electronic parameters or empirical relations built on outdated cell performance. Moreover, the impact of crystal imperfections on dual-junction III-V/Si solar cells performance has not been considered in the modelling works reported in the literature, although the formation of defects is inevitable for nitrogen-free 1.6-1.8 eV III-V materials monolithically grown on silicon substrates.

The main hurdle in accurately simulating bandgap-dependent, material-specific and architecture-specific dual-junction solar cells lies in the lack of data regarding the chosen material ($GaAs_xP_{1-x}$ in the present work). In order to approximate the expected behaviour of the real material without using an extensive number of electronic parameters, we simulate the device performance as a result of the flow equilibrium in the cells, adapting the Shockley-Queisser detailed balance model [4.15], presented in Chapter 2, Section 2.4.2. We consider the radiative limit as the upper thermodynamic boundary on the cells' performance [4.16-4.17] and use simple models to calculate non-radiative recombination rates, such as Auger and Shockley-Read-Hall (SRH). The need for specific electronic parameters is, thus, limited to a minimum, as the main input in the model is the absorption spectrum of the top cell material.

As an important improvement over already existing models, the impact of threading dislocations (TDs), the main source of inefficiencies for lattice-mismatched III-V solar cells, has been integrated using the NTT model [4.18], presented in Chapter 3, Equations (3.1-3.5). Additionally, luminescent coupling between the cells due to photons from radiative recombination in the top cell cascading to the bottom cell has also been taken into account. The impact of two geometrical architectures for the front surface (flat and Lambertian) has also been investigated. Finally, other sources of non-idealities such as non-perfect EQE and surface recombination are added in Section 4.3.4 in order to give an evaluation of the long-term potential performance of the technology. This inclusive model allows for quantitative insights in the design of $GaAs_xP_{1-x}$/Si dual-junction solar cells such as the ones currently being developed [4.6-4.10], highlighting the processes limiting the efficiency of this device architecture.

Moreover, targets are set regarding the maximum threading dislocation density (TDD) needed in order to achieve very high efficiency devices (>35 %).

4.2 Methods

4.2.1 General considerations about the model

The model presented hereafter has been developed using MATLAB® R2014a. All the calculations are wavelength-dependent with rectangular integration on the wavelength between 280 nm and 1450 nm with a 0.5 nm step. The efficiencies were calculated for Air Mass 1.5 Global (AM1.5G) without concentration using data from the ASTM G173-03 reference spectrum [4.19]. The percentage of arsenic x in the top $GaAs_xP_{1-x}$ cell can vary from x=0.55 to 1, representing the direct bandgap domain of $GaAs_xP_{1-x}$ [4.20].

Electronic Parameter	Formula	Source
Bandgap [eV]	$E_g(GaAs_xP_{1-x}) = 1.42x + 2.78(1-x) - 0.19x(1-x)$	[4.20]
Density of states in the conduction band [cm^{-3}]	$N_c(GaAs_xP_{1-x}) = 5.6\times10^{19}(0.08 - 0.039x)^{\frac{3}{2}}$	Extrapolated from [4.21] and [4.22]
Density of states in the valence band [cm^{-3}]	$N_v(GaAs_xP_{1-x}) = 2.9\times10^{19}(0.6 - 0.18x)^{\frac{3}{2}}$	Extrapolated from [4.21] and [4.22]
Diffusion coefficient of electrons [$cm^2.s^{-1}$]	$D_n(GaAs_xP_{1-x}) = 39 - 57x + 108x^2$	Extrapolated from [4.21] and [4.22] with corrections from [4.23]
Diffusion coefficient of holes [$cm^2.s^{-1}$]	$D_p(GaAs_xP_{1-x}) = 5 - 10x + 12.5x^2$	Extrapolated from [4.21] and [4.22]
Relative permittivity	$\varepsilon_r(GaAs_xP_{1-x}) = 12.9$	[4.22]

Table 4.1 *Formulae used for the calculation of the electronic parameters of the materials investigated with the respective sources*

The main challenge in accurately simulating a bandgap-dependent $GaAs_xP_{1-x}$/Si dual-junction solar cell lies in the lack of data regarding the electronic parameters of $GaAs_xP_{1-x}$ for varying percentages of arsenic x. Using the blackbody theory applied to semiconductors from Würfel [4.24] and the flow equilibrium in the cells [4.15-4.17], our model reduces the number of electronic parameters needed to a limited number, namely the bandgap $E_g(GaAs_xP_{1-x})$, the densities of states in the conduction and valence bands $N_c(GaAs_xP_{1-x})$ and $N_v(GaAs_xP_{1-x})$, the diffusion coefficient of electrons and holes $D_n(GaAs_xP_{1-x})$ and $D_p(GaAs_xP_{1-x})$ and the relative permittivity $\varepsilon_r(GaAs_xP_{1-x})$. The formulae used for the calculation of these electronic parameters and their sources are summarized in TABLE 4.1. The hypothesis behind the extrapolations presented in TABLE 4.1 is that GaAsP presents the same dependencies on the P content x as InGaAsP [4.21], using GaAs parameters from the literature [4.22-4.23] to calibrate the extrapolation at x=0. The last five electronic parameters are moreover solely used to model the impact of TDs [4.18]. Hence, the bandgap is the single parameter needed for the determination of the defect-free theoretical maximal efficiency.

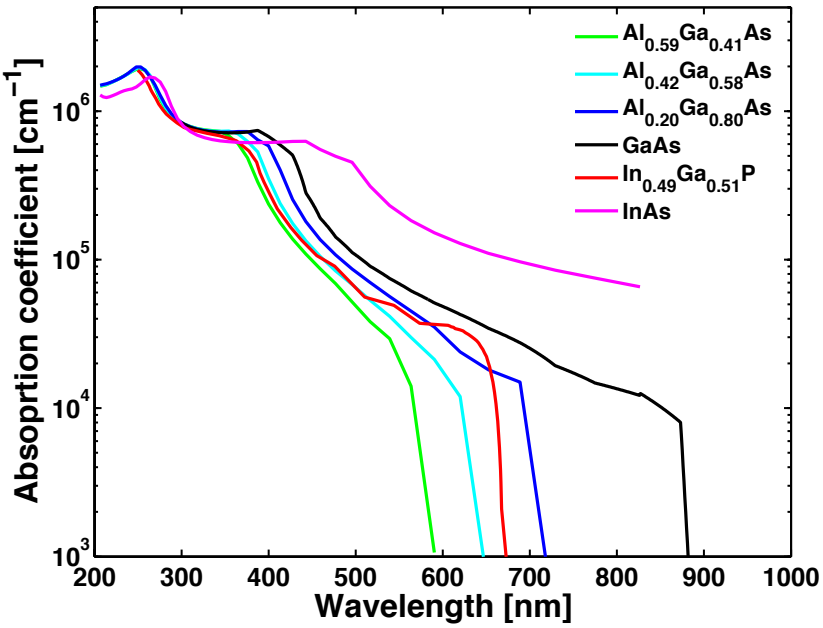

FIGURE 4.1. *Absorption coefficient spectra of $Al_{0.59}Ga_{0.41}As$, $Al_{0.42}Ga_{0.58}As$, $Al_{0.20}Ga_{0.80}As$, GaAs, $In_{0.49}Ga_{0.51}P$ and InAs. For InAs, the data stops at 826 nm. Even for a widely different alloy like $In_{0.49}Ga_{0.51}P$, the shape of the absorption spectrum is similar.*

This is possible through the use of Würfel's thermodynamic approach [4.24], presented in Chapter 2, Equations (2.42-2.44), allowing the calculation of the radiative recombination rate of a semiconductor device from its absorption spectrum. In order to determine the absorption spectrum of $GaAs_xP_{1-x}$ for different percentages of arsenic x, we make the hypothesis that the main consequence of the incorporation of phosphorus is a blue-shift from the absorption spectrum of GaAs. This blue-shift is assumed equal to the difference in bandgap between $GaAs_xP_{1-x}$ and GaAs. Given the very similar shape of absorption spectra of III-V direct bandgap materials – in particular close to the band-edge – as shown on FIGURE 4.1, this is a rational hypothesis. The GaAs absorption reference spectrum has been extrapolated based on experimental data from Ref. [4.25] between 280 nm and 826.5 nm and from the fitted model from Ref. [4.17], based on experimental data from Ref. [4.26], above 826 nm. For the bottom Si solar cell, the absorption spectrum has been extrapolated from Ref. [4.27].

4.2.2 Cell architecture

The architecture investigated is presented in FIGURE 4.2. The dual-junction GaAsP/Si cell is a two-terminal series-connected tandem structure with current-matched subcells. The subcells are connected through a high bandgap window buffer similar to the metamorphic GaAsP buffer on a GaP nucleation layer presented in Refs. [4.6-4.10]. Due to its high bandgap, absorption is neglected in this buffer. We assume that the series resistance from the tunnel junction between the two subcells is negligible.

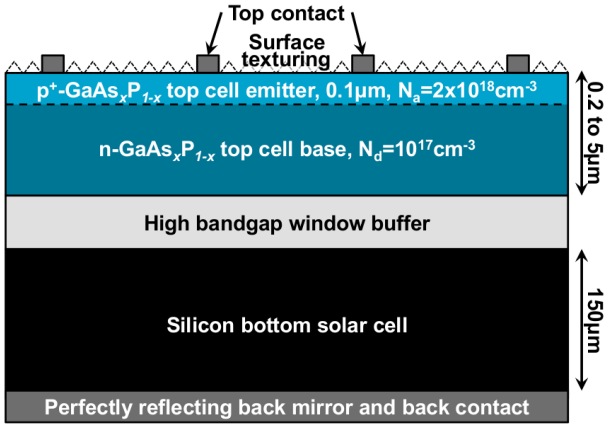

FIGURE 4.2. *Detail of the architecture of the $GaAs_xP_{1-x}$/Si dual-junction investigated.*

The top cell composition varies in the direct bandgap domain of $GaAs_xP_{1-x}$, with the As content varying from x=0.55 (E_g=1.98 eV) to 1 (E_g=1.42 eV). Its thickness varies from 0.2 µm to 5 µm, with a fixed emitter thickness of 0.1 µm. A p^+/n architecture has been chosen in order to reduce the impact of TDs, as the diffusion coefficient of holes D_p is approximately an order of magnitude smaller than the diffusion coefficient of electrons D_n in $GaAs_xP_{1-x}$. Dopings of the n-type base and p^+-type emitter have been set at $N_d=10^{17}$ cm^{-3} and $N_a=2\times10^{18}$ cm^{-3}, respectively. Given the relatively high direct bandgap of $GaAs_xP_{1-x}$ in the range of arsenic content considered, the dominant bulk non-radiative recombination process is SRH type and Auger recombination is neglected in the top cell.

Charge transfer along TDs in the top cell is possible, inducing a low shunt resistance. However, a review of the literature [4.5-4.7, 4.9-4.10, 4.28] shows that experimental III-V on Si solar cells for the range of TDDs investigated (up to 2×10^8 cm^{-2}) do not exhibit a significant efficiency reduction due to low shunt resistances, with reported J-V characteristics displaying relatively flat current densities at low voltage and no evident degradation of the diodes characteristics with higher TDDs. For simplification purposes, the shunt resistances of both cells are, thus, assumed infinite.

The Si bottom cell thickness is fixed at 150 µm, representative of high-efficiency c-Si solar cells industry standards. As the goal of this study is to investigate the upper limits on the efficiency of $GaAs_xP_{1-x}$/Si dual junction solar cells, we assume an optimised high-quality, perfectly mono-crystalline and defect-free Si cell. Thus, we neglect SRH recombination and only use Auger recombination as bulk non-radiative recombination in the bottom cell. The ambipolar Auger coefficient has been set at $C_{Auger}=1.66\times10^{-30}$ cm^6.s^{-1} with an intrinsic carrier concentration of $n_i=9.7\times10^9$ cm^{-3} [4.29].

We ignore surface recombination in both cells in the first part of the study as we focus on the impact of the Threading Dislocation Density (TDD) on the theoretical efficiency of perfect $GaAs_xP_{1-x}$ on Si dual-junction solar cells. In Section 4.3.4, the impact of surface recombination is added to evaluate the real-world efficiency potentially achievable by such a structure.

Two surface geometries are investigated: flat surface, with specular reflection, on one hand; and Lambertian surface, ideally textured and perfectly scattering the incoming light into a Lambertian distribution, on the other hand. The refractive index inside the device is supposed constant at n_{ref}=3.6, which is a reasonable approximation for the materials considered. A perfectly reflecting mirror on the back of the Si bottom cell is assumed, doubling the optical path in the Si cell and eliminating radiative reemission from its back side. As a result, the cell re-emits only in the upwards half space in a solid angle $\Omega_{emis}=2\pi$ str, as presented in Chapter 2, Section 2.3.3. Shading from the front contact and reflection at the front surface are neglected in the first part of the study. An average External Quantum Efficiency (EQE), taking into account the effect of such optical losses, is added in Section 4.3.4 to assess the real-world potential of the cell architecture.

4.2.3 Blackbody theory and flow equilibrium model basics

For each cell, we consider the general diode equation presented in Chapter 2:

$$J(V) = J_{sc} + J_{0,rad}\left(1 - e^{\frac{qV}{k_B T}}\right) + \sum^{m} J_{0,m}\left(1 - e^{\frac{qV}{n_m k_B T}}\right) \quad (4.1)$$

where J is the current density, V the voltage, q the elementary charge, k_B the Boltzmann constant, T the cell temperature set at 300 K, J_{sc} the short-circuit current density, $J_{0,rad}$ the radiative saturation current density, $J_{0,m}$ the saturation current density associated with different non-radiative recombination mechanisms m (SRH and Auger included), and n_m the associated ideality factors.

As described in Chapter 2, Würfel has shown that, considering the Boltzmann approximation ($E>>k_BT$), the emission rate of a photovoltaic cell under thermal equilibrium (*i.e.* in the dark) is given by [4.24]:

$$\int_0^{+\infty} \frac{2\pi a(E)E^2}{h^3c^2} e^{\frac{qV-E}{k_B T}} dE = e^{\frac{qV}{k_B T}} \int_0^{+\infty} \frac{2\pi c a(\lambda)}{\lambda^4} e^{-\frac{hc}{\lambda k_B T}} d\lambda \quad (4.2)$$

where $a(\lambda)$ is the wavelength-dependent absorptivity of the cell, E the energy of the considered photons, λ their wavelength, h the Planck constant, and c the speed of light.

With R_{rad} the saturation radiative recombination rate, we have:

$$J_{0,rad} = qR_{rad} = q\int_0^{+\infty} \frac{2\pi c a(\lambda)}{\lambda^4} e^{-\frac{hc}{\lambda k_B T}} d\lambda \tag{4.3}$$

Under the initial hypothesis that at V=0 the recombination contributions are null, the short-circuit current density J_{sc} is equal to the photocurrent density J_{ph}. Assuming perfect external quantum efficiency, this is given by basically counting the number of photons absorbed within each cell:

$$J_{ph,top} = q\int_0^{+\infty} \left(\frac{\lambda}{hc}\right) I(\lambda) a_{front,top}(\lambda) d\lambda = qG_{top} \tag{4.4}$$

$$J_{ph,bot} = q\int_0^{+\infty} \left(\frac{\lambda}{hc}\right) I(\lambda)\left(1 - a_{front,top}\right) a_{front,bot}(\lambda) d\lambda = qG_{bot} \tag{4.5}$$

where $I(\lambda)$ is the wavelength-dependent AM1.5 irradiance, $a_{front,top/bot}(\lambda)$ is the absorptivity from the front of the top/bottom cell, and G is the photo-generation rate.

It is to be noted that the assumption of $J_{sc}=J_{ph}$ does not take into account possible recombination at short-circuit. The underlying hypothesis is that the diffusion length of minority carriers is longer than the thickness of the base and of the emitter so that charges can travel freely to the depletion zone under short-circuit conditions. Though this hypothesis is valid to some extent when the crystal is assumed perfect, defects such as threading dislocations can reduce the diffusion length to the point that the short-circuit current density J_{sc} gets smaller than the photocurrent density J_{ph}, especially at high TDD. A solution to this issue is proposed and implemented in Section 4.2.5. Also note that, for the bottom cell, the total absorptivity and the absorptivity from the front surface are equal due to the presence of a back mirror so that $a_{back,bot}=0$ and $a_{bot}(\lambda)=a_{front,bot}(\lambda)$. However, for the top cell, the total absorptivity is the sum of the front and back absorptivities: $a_{top}(\lambda)=a_{front,top}(\lambda)+a_{back,top}(\lambda)$; only the former is taken into account in the calculation of $J_{ph,top}$.

As specified in section 4.2.2, Auger recombination is neglected in the top cell, SRH recombination is neglected in the bottom cell and other sources of recombination, such as surface recombination, are neglected in both cells so that:

$$J_{top}(V_{top}) = q\left(G_{top} + R_{rad,top}\left(1 - e^{\frac{qV_{top}}{k_BT}}\right) + R_{SRH}(V_{top})\right) \quad (4.6)$$

$$J_{bot}(V_{bot}) = q\left(G_{bot} + R_{rad,bot}\left(1 - e^{\frac{qV_{bot}}{k_BT}}\right) + R_{Auger}(V_{bot})\right) \quad (4.7)$$

where $R_{SRH}(V)=J_{0,SRH}(V)/q$ is the voltage-dependent SRH recombination rate in the top cell and $R_{Auger}(V)=J_{0,Auger}(V)/q$ is the voltage-dependent Auger recombination rate in the bottom cell.

4.2.4 Front surface geometry-dependent absorptivity model

As shown in FIGURE 4.3, absorptivities of both cells depend on the front surface geometry. Two geometries, planar and Lambertian, are investigated. As stated in section 4.2.3, the absorptivities $a_{front,top}$ and $a_{back,top}$ from the front and back of the top cell need to be calculated, whereas only the front absorptivity $a_{front,bot}=a_{bot}$ is needed for the bottom cell due to the assumption of a perfect back mirror.

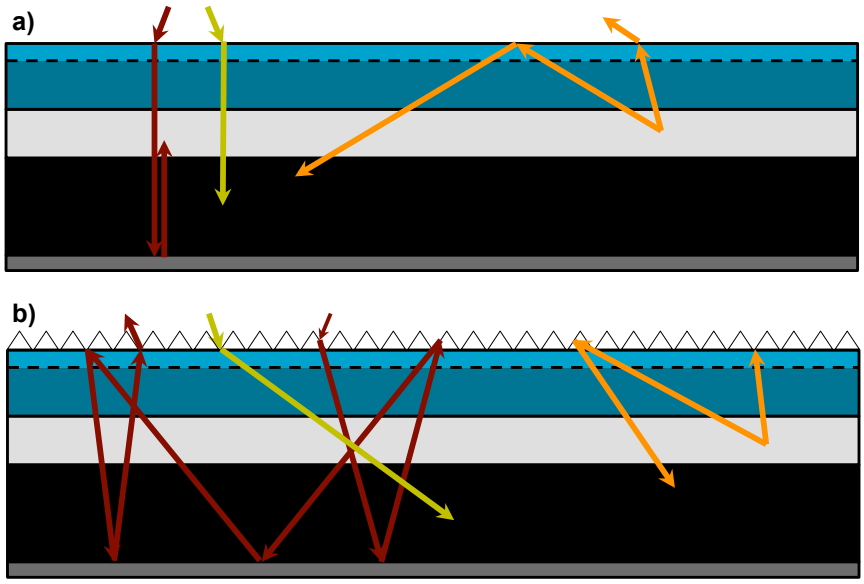

FIGURE 4.3. *Schematic of the two different absorptivity models used: flat surface (a) and Lambertian surface (b). The impact of the randomly textured surface is greater on the bottom cell absorptivity than on the top cell one, as perfect light trapping occurs in the bottom cell whereas, in the top cell, the optical path is only multiplied by a factor 1/cos(θ) from the Lambertian distribution.*

a) Planar front surface

Because of the large refractive index of $GaAs_xP_{1-x}$, the incident light is refracted with an angle very close to perpendicular within the cell. The wavelength-dependent front surface absorptivity of the top cell is, thus, well known:

$$a_{front,top}(\lambda) = 1 - e^{-\alpha_{GaAsP}(\lambda)L_{top}} \tag{4.8}$$

where $\alpha_{GaAsP}(\lambda)$ is the wavelength-dependent absorption coefficient of $GaAs_xP_{1-x}$ and L_{top} is the top cell thickness. Similarly, the wavelength-dependent front surface absorptivity of the bottom cell is:

$$a_{front,bot}(\lambda) = 1 - e^{-2\alpha_{Si}(\lambda)L_{bot}} \tag{4.9}$$

where $\alpha_{Si}(\lambda)$ is the wavelength-dependent absorption coefficient of Si and L_{bot} is the bottom cell thickness. The factor 2 originates from the doubling of the optical path in the Si bottom cell because of the back mirror.

As previously shown in Ref. [4.17], absorptivity from the back side of the top cell has to take into account the increase due to the possible total internal reflection on the front side of the cell. This internal reflection happens when the incident angle is greater than the critical escape angle $\theta_{esc}=arcsin(1/n_{ref})$ and doubles the effective optical path length. A factor n_{ref}^2 is also added, as the density of states of the internal blackbody radiation at the back surface of the top cell is increased by this factor. This leads to:

$$a_{back,top}(\lambda) = 2n_{ref}^2 \left(\int_0^{\theta_{esc}} \left(1 - e^{-\alpha_{GaAsP}(\lambda)\frac{L_{top}}{cos\theta}}\right) cos\theta sin\theta d\theta + \int_{\theta_{esc}}^{\frac{\pi}{2}} \left(1 - e^{-2\alpha_{GaAsP}(\lambda)\frac{L_{top}}{cos\theta}}\right) cos\theta sin\theta d\theta \right) \tag{4.10}$$

b) *Lambertian front surface*

In the case of a randomly textured surface, the assumption of perpendicular light entering the cell is no longer valid and the absorption in the top cell is dependent on the polar angle θ. If we consider that the textured front surface is ideal and perfectly randomizes the incident light into a Lambertian distribution, the top cell front absorptivity is then:

$$a_{front,top}(\lambda) = 2\int_0^{\frac{\pi}{2}} \left(1 - e^{-\alpha_{GaAsP}(\lambda)\frac{L_{top}}{cos\theta}}\right) cos\theta sin\theta d\theta \tag{4.11}$$

For the bottom cell, as the top cell and buffer are windows for the wavelengths in the weakly absorbing limit, the light trapping can be considered ideal and, as shown in [4.30], we have:

$$a_{front,bot}(\lambda) = \frac{4n_{ref}^2\alpha_{Si}(\lambda)L_{bot}}{1 + 4n_{ref}^2\alpha_{Si}(\lambda)L_{bot}} \tag{4.12}$$

Again, the absorptivity from the back of the top cell has to take into account the possible total internal reflection on the front side of the cell. However, this time, the angle at which the incident light encounters the surface and the angle at which it is reflected are both random so that:

$$\begin{aligned} a_{back,top}(\lambda) = 2n_{ref}^2 \Bigg(& \frac{2\theta_{esc}}{\pi}\int_0^{\frac{\pi}{2}} \left(1 - e^{-\alpha_{GaAsP}(\lambda)\frac{L_{top}}{cos\theta}}\right) cos\theta sin\theta d\theta \\ & + \left(1 - \frac{2\theta_{esc}}{\pi}\right)\int_0^{\frac{\pi}{2}}\int_0^{\frac{\pi}{2}} \left(1 - e^{-\alpha_{GaAsP}(\lambda)\left(\frac{L_{top}}{cos\theta} + \frac{L_{top}}{cos\theta'}\right)}\right) cos\theta cos\theta' sin\theta d\theta d\theta' \Bigg) \end{aligned} \tag{4.13}$$

4.2.5 Model for bulk non-radiative recombination

We consider an intrinsic or a very low doping density Si bottom cell in order to simplify the model and reduce the Auger recombination rate, although this hypothesis does not exactly correspond to state-of-the-art high-efficiency Si solar cells currently available. The voltage-dependent Auger recombination rate is then given by [4.16]:

$$R_{Auger}(V) = C_{Auger}L_{bot}n_{i,Si}^3\left(1 - e^{\frac{3qV}{2k_BT}}\right) = R_{Auger}\left(1 - e^{\frac{3qV}{2k_BT}}\right) \tag{4.14}$$

where L_{bot} is the thickness of the bottom cell.

We consider that the only source of SRH recombination in the top cell is the presence of TDs due to the lattice mismatch between Si and $GaAs_xP_{1-x}$, other crystal defects being neglected. As described in Chapter 3, Yamaguchi *et al.* have shown that, for both types of carriers, the minority-carrier diffusion length associated with a TD density ρ_{TD} is [4.18]:

$$L_{TD} = \sqrt{\frac{4}{\pi^3 \rho_{TD}}} \tag{4.15}$$

Although this model is very basic and does not describe in detail the SRH recombination process on a TD, in particular possible inelastic processes during capture on deep TD energy levels, it has shown excellent agreement with experimental data in predicting the minority carrier lifetime, the open-circuit voltage and the efficiency of III-V on Si solar cells [4.18, 4.31-4.37]. The voltage-dependent recombination rate associated with TDs in the depletion zone is then given by [4.18]:

$$\begin{aligned} R_{SRH,DZ}(\mathrm{V}) &= \frac{n_{i,GaAsP} W_D}{2} \frac{D_p}{L_{TD}^2} \left(1 - e^{\frac{qV}{2k_B T}}\right) \\ &= \frac{\pi^3 D_p \rho_{TD} n_{i,GaAsP} W_D}{8} \left(1 - e^{\frac{qV}{2k_B T}}\right) \\ &= R_{SRH,DZ} \left(1 - e^{\frac{qV}{2k_B T}}\right) \end{aligned} \tag{4.16}$$

where D_p is the minority-carrier diffusion coefficient of holes and W_D is the depletion width of the top cell given by:

$$W_D = \sqrt{\frac{2\varepsilon_0 \varepsilon_r}{q} \frac{k_B T}{q} ln\left(\frac{N_a N_d}{n_{i,GaAsP}^2}\right)\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \tag{4.17}$$

and n_i is calculated using the usual relationship from Equation 2.3 of Chapter 2:

$$n_{i,GaAsP} = \sqrt{N_c N_v} e^{-\frac{E_g}{2k_B T}} \tag{4.18}$$

In the base and in the emitter, the voltage-dependent recombination rates associated with TDs are given by [4.38]:

$$\begin{aligned} R_{SRH,base}(V) &= \frac{n_{i,GaAsP}^2 W_{base}}{N_d}\frac{D_p}{L_{TD}^2}\left(1-e^{\frac{qV}{k_BT}}\right) \\ &= \frac{\pi^3 D_p \rho_{TD} n_{i,GaAsP}^2 W_{base}}{4N_d}\left(1-e^{\frac{qV}{k_BT}}\right) \\ &= R_{SRH,base}\left(1-e^{\frac{qV}{k_BT}}\right) \end{aligned} \quad (4.19)$$

$$\begin{aligned} R_{SRH,emit}(V) &= \frac{n_{i,GaAsP}^2 W_{emit}}{N_a}\frac{D_n}{L_{TD}^2}\left(1-e^{\frac{qV}{k_BT}}\right) \\ &= \frac{\pi^3 D_n \rho_{TD} n_{i,GaAsP}^2 W_{emit}}{4N_a}\left(1-e^{\frac{qV}{k_BT}}\right) \\ &= R_{SRH,emit}\left(1-e^{\frac{qV}{k_BT}}\right) \end{aligned} \quad (4.20)$$

where D_n is the minority-carrier diffusion coefficient of electrons, W_{base} is the top cell base width, and W_{emit} is the top cell emitter width.

The SRH recombination rate in the quasi-neutral regions can then be derived from Equations (4.19) and (4.20):

$$\begin{aligned} R_{SRH,QNR}(V) &= R_{r,SRH,base}(V) + R_{r,SRH,emit}(V) \\ &= \left(R_{r,SRH,base} + R_{r,SRH,emit}\right)\left(1-e^{\frac{qV}{k_BT}}\right) \\ &= R_{SRH,QNR}\left(1-e^{\frac{qV}{k_BT}}\right) \end{aligned} \quad (4.21)$$

The reduced diffusion length will also impact the photon collection and, therefore, the short-circuit current density, as only a portion of the photo-generated carriers will be able to reach the depletion zone. We can assume that the photon collection efficiency will not be impacted in the emitter as its thickness is smaller than the diffusion length, even for very high TD densities (up to ρ_{TD}=10^9 cm^{-2}). The carriers generated in the depletion zone will also all be collected.

However, under the approximation of a uniform generation rate, the carriers generated in the base at a distance from the depletion zone larger than the diffusion length will not contribute to the short-circuit current density. This means that, for the calculation of the top cell photo-generated current in absorptivity equations (4.8-4.13), the actual thickness of the cell L_{top} must be replaced by an effective thickness $L_{top}'=W_{emit}+W_D+L_{TD}$ when $L_{TD}<W_{base}$. Therefore, the reduction of the J_{sc} at higher TDDs, due to the reduced minority carriers diffusion length, is integrated by

evaluating the photocurrent over a thickness smaller than the actual geometrical thickness of the top cell. For a 2 µm-thick cell, this correction will happen for a TDD ρ_{TD}>4×10^6 cm^{-2}. As shown in Ref. [4.39], for a cell with a 2.5 µm-thick base, a lower TDD (ρ_{TD}=0.8-1.5×10^6 cm^{-2}, L_{TD}=2.9-4 µm) already has a strong impact on the open-circuit voltage but no noticeable effect on the external quantum efficiency and, therefore, on the short-circuit current density.

Current-voltage characteristics in the top and bottom cells are, thus, given by:

$$J_{top}(V_{top}) = q\left(G_{top} + \left(R_{rad,top} + R_{SRH,QNR}\right)\left(1 - e^{\frac{qV_{top}}{k_BT}}\right) + R_{SRH,DZ}\left(1 - e^{\frac{qV_{top}}{2k_BT}}\right)\right) \quad (4.22)$$

$$J_{bot}(V_{bot}) = q\left(G_{bot} + R_{rad,bot}\left(1 - e^{\frac{qV_{bot}}{k_BT}}\right) + R_{Auger}\left(1 - e^{\frac{3qV_{bot}}{2k_BT}}\right)\right) \quad (4.23)$$

4.2.6 Luminescent coupling between the cells

An additional process taken into account is Luminescent Coupling (LC) between the subcells, as photons emitted through radiative recombination in the top cell can cascade to the bottom cell. This process has been extensively documented and modelled by Friedman, Geisz and Steiner [4.40-4.42]. In a first approximation, regardless of the surface geometry, the probability of a reemitted photon escaping through the top surface is θ_{esc}/π so the probability of a photon cascading to the bottom cell is $1-(\theta_{esc}/\pi)$. These photons have energies close to the bandgap of the top cell, in the very high absorption region of the bottom cell absorption spectrum. Therefore, we can assume that all these photons will contribute to the photocurrent in the bottom cell. The boost to the bottom cell photocurrent density from LC is then:

$$J_{ph,LC,bot}(V_{top}) = q\left(1 - \frac{\theta_{esc}}{\pi}\right)R_{rad,top}e^{\frac{qV_{top}}{k_BT}} \quad (4.24)$$

The cells being series-connected, we have $J=J_{top}=J_{bot}$. V_{top} and V_{bot} can then be expressed as a function of one another through:

$$G_{top} + \left(R_{rad,top} + R_{SRH,QNR}\right)\left(1 - e^{\frac{qV_{top}}{k_BT}}\right) + R_{SRH,DZ}\left(1 - e^{\frac{qV_{top}}{2k_BT}}\right)$$
$$= G_{bot} - \left(1 - \frac{\theta_{esc}}{\pi}\right)R_{rad,top}\left(1 - e^{\frac{qV_{top}}{k_BT}}\right) + R_{rad,bot}\left(1 - e^{\frac{qV_{bot}}{k_BT}}\right) \quad (4.25)$$
$$+ R_{Auger}\left(1 - e^{\frac{3qV_{bot}}{2k_BT}}\right)$$

The efficiency of the tandem cell can subsequently be calculated by finding the maximum of $J\times(V_{top}+V_{bot})$ corresponding to the maximum power point of the dual-junction cell.

4.2.7 Model flowchart

A flowchart of the model, annotated with the equations used, is presented in FIGURE 4.4. Variable input parameters (top cell P content x, top cell thickness L_{top}, TDD ρ_{TD}, surface geometry, and bottom cell surface saturation current density $J_{0e,Si}$) are in light blue, fixed input parameters are in dark blue, material constants and spectral data from the literature are in orange, outputs are in red. The MATLAB® code is presented as an Appendix.

The top cell's electronic parameters, including the bandgap $E_{g,top}$, are first calculated based on the P content x. From there, the absorption coefficient $\alpha_{GaAsP}(\lambda)$ and the intrinsic carrier concentration $n_{i,GaAsP}$ of the top cell's material are determined. The width of the depletion zone W_D is derived from Equation (4.17) using the calculated intrinsic carrier concentration. Depending on the surface geometry considered, the front and back absorptivities of the top cell are determined from Equations (4.8, 4.10) or (4.11, 4.13), using the calculated GaAsP absorption spectrum $\alpha_{GaAsP}(\lambda)$ and the top cell thickness L_{top}. Similarly, the bottom cell absorptivity is calculated from the Si absorption coefficient $\alpha_{Si}(\lambda)$, the bottom cell thickness L_{bot}, and the surface geometry considered, using Equations (4.9) or (4.12). Using Equation (4.3), both cells radiative recombination rates are integrated.

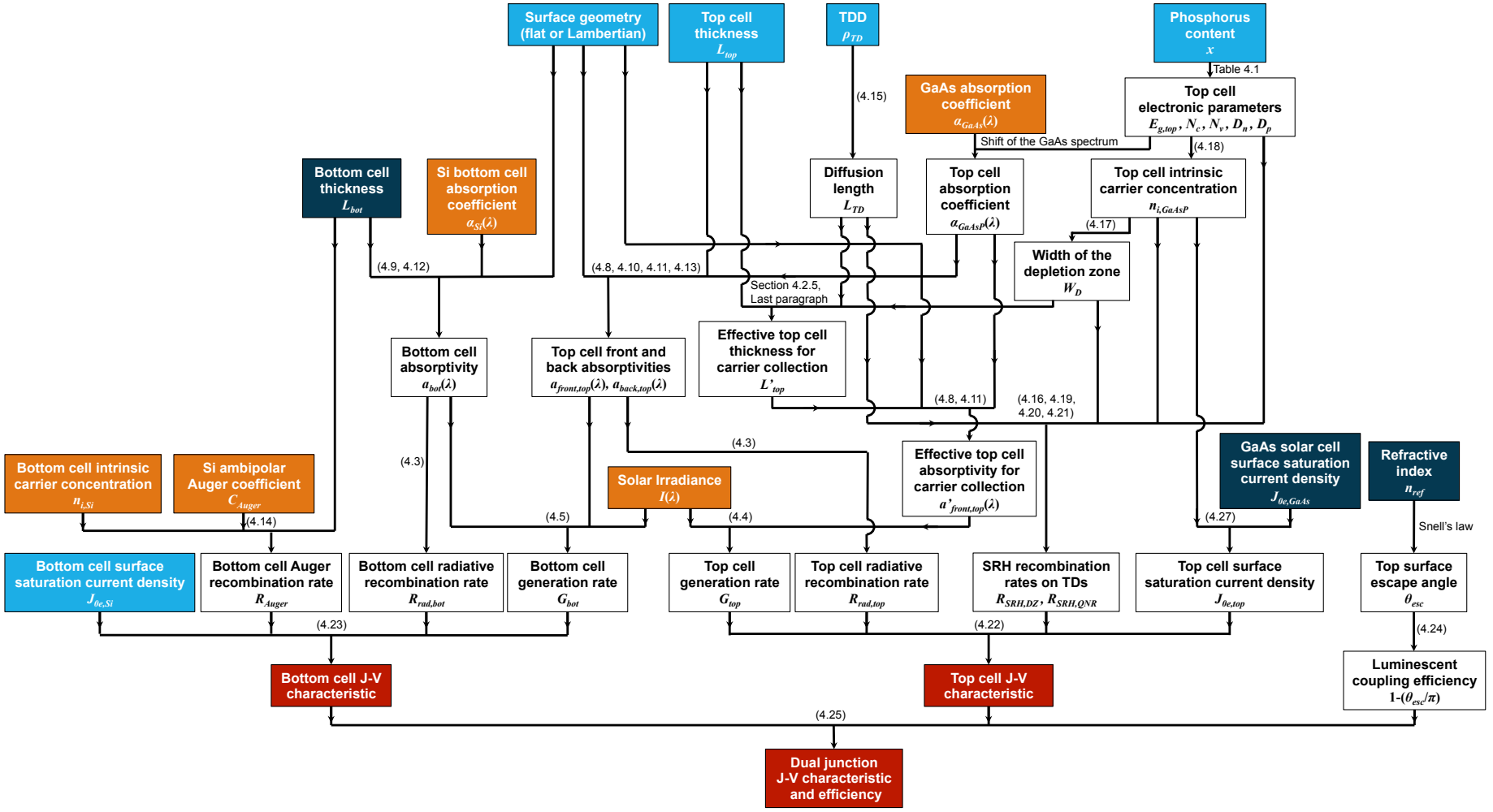

FIGURE 4.4. *Flowchart of the model used to simulate GaAsP/Si dual junction solar cells. Variable input parameters are in light blue, fixed input parameters are in dark blue, material constants and reference data from the literature are in orange, outputs are in dark red. Equations from which the different variables are calculated are shown in brackets.*

The Shockley-Read-Hall (SRH) recombination rate from TDs in the top cell are calculated from Equations (4.16, 4.19, 4.20, 4.21) using the previously calculated depletion zone width W_D, diffusion length in the top cell L_{TD}, and top cell's electronic parameters. The Auger recombination rate in the bottom cell is calculated from the Si intrinsic carrier concentration, the Si ambipolar Auger coefficient, and the bottom cell thickness. As explained in Section 4.3.4, surface saturation recombination rates can be added for both cells, adjusted to the intrinsic carrier concentration for the top cell.

All the generation and recombination rates for both cells diode Equations (4.22, 4.23) are, thus, independently calculated. From the front surface escape angle, determined from Snell's law, the luminescent coupling efficiency is calculated. The Maximum Power Point (MPP) is then obtained by maximizing the product $J\times(V_{top}+V_{bot})$ with the constraint of verifying Equation (4.25), established from the current matching between the cells. LC can be taken into account or ignored, by setting or not the luminescent coupling efficiency to zero. Thus, the impact of LC and be assessed. FOR loops are built in the model in order to simulate a space of parameters (variable P content x, top cell thickness L_{TD}, and TDD ρ_{TD}) at once.

A list of the assumptions used in the model is presented in TABLE 4.2. A number of assumptions are made in order to calculate the theoretical maximum efficiency of the device architecture considered – by minimising the possible losses – and to assess the impact of TDs on this theoretical limit. Due to the logarithm in the diode equation, the impact of possible inaccuracies in the evaluation of parameters is relatively limited, leading to variations in V_{oc} of a couple tens of mV. The most sensitive approximation is probably related to the shape of the absorption spectrum for GaAsP, especially regarding the shape of the Urbach tail. However, as GaAsP is not a widely studied material, no data regarding the absorption spectrum of GaAsP as a function of the phosphorus content was available in the literature. Blue-shifting of the GaAs spectrum is, thus, an acceptable solution.

Surface recombination and External Quantum Efficiency (EQE) parameters, calculated from reported experimental data, are added in Section 4.3.4. Other sources of losses (series and shunt resistance, absorption in the metamorphic buffer…) are

neglected in Section 4.3.4, as they can be strongly reduced with reasonable engineering and their impact on the dual junction performance is limited compared with the influence of non-perfect EQE and surface recombination.

Assumptions	Justification and implications
Boltzmann approximation	Energies of importance are larger than $3k_BT$
Similar dependencies on the P content for the electronic parameters of GaAsP and InGaAsP	GaAsP and InGaAsP are similar materials. Moreover, due to the logarithm in the diode equation, the impact of inaccuracies in the evaluation of parameters is reduced. As an example, even an error of 50 % on a parameter would only lead to a difference in V_{oc} below 30 mV
Constant refractive index n_{ref}=3.6 throughout the device	Si and GaAsP refractive indexes between 3 and 4 for the wavelengths considered [4.25,4.27], limiting reflection at the interface between the two cells. Refractive index n_{ref} only used for the calculation of the critical angle and the multiplication coefficient for the back absorptivity, so the value close to the band-edge of the top cell [4.27] is a good approximation. Low sensitivities of the V_{oc} and of LC to variations of the refractive index. As an example, with n_{ref} varying between 3 and 4, the difference in V_{oc} is below 15 mV and the probability of photons cascading from the top cell to the bottom cell only varies from 89 % to 92 %.
Simple blue-shift of the GaAs absorption spectrum with increasing P content	Similar shapes of absorption coefficient spectra close to the band-edge for direct bandgap III-V materials (see FIGURE 4.1). For the range of bandgaps of interest (1.65 eV to 1.85 eV), the P content is relatively limited (20 % to 35 %) and an absorption coefficient similar in shape with GaAs is even more justified. The shape of the absorption coefficient at lower wavelength matters less as, even with thin cells, nearly all the light is absorbed when the absorption coefficient is above 10^5 cm^{-2}.
No absorption in the metamorphic buffer	Optimal conditions to calculate the theoretical maximum efficiency of the devices: high bandgap buffer and top cell optically thick for higher energy photons.
NTT Model	Uniform distribution of dislocations across the wafer (no clusters), defect energy state in the middle of the bandgap, independence of the recombination pathways [4.18]
Auger recombination neglected in GaAsP top cell	High direct bandgap makes the contribution from Auger recombination negligible
Other sources of bulk SRH recombination neglected in GaAsP top cell	High bulk material quality assumed, making SRH recombination on TDs the dominant recombination pathway

Low doping of the c-Si bottom cell.	Optimal conditions to calculate the theoretical maximum efficiency of the devices (impact of Auger recombination is limited)
Bulk SRH recombination neglected in the bottom Si cell	Optimal conditions to calculate the theoretical maximum efficiency of the devices. Additionally, we assume a very high material quality c-Si material, with SRH recombination negligible in comparison with other sources of losses (surface recombination, Auger recombination…)
Negligible series and shunt resistance	Optimal conditions to calculate the theoretical maximum efficiency of the devices. Furthermore, with reasonably good engineering, resistance losses can be made negligible in comparison with other sources of losses (surface recombination, SRH recombination…)
Perfectly reflecting back mirror on the back of the device	Optimal conditions to calculate the theoretical maximum efficiency of the devices. Very high reflection can be obtained using metallic contact back reflectors, with rear optical losses below 4 % achievable [4.43].
Perfect EQE in the first part of the study	Optimal conditions to calculate the theoretical maximum efficiency of the devices.
Average EQE in the second part of the study	First order approximation of the real world current densities achievable
Surface recombination neglected in the first part of the study	Optimal conditions to calculate the theoretical maximum efficiency of the devices.
Approximation of the surface recombination in the second part of the study	First order approximation of the real-world voltages achievable, assuming a good passivation of the GaAsP top cell and two scenarios for the bottom cell: good passivation or highly doped emitter
Uniform generation rate for the calculation of the short-circuit current density	First order approximation of the impact of high TDDs on the carrier collection. As, in reality, more carriers are generated closer to the top of the cell, the impact of TDDs on the photocurrent is overestimated.
Probability of a photon generated in the top cell and cascading to the bottom cell equal to $1-(\theta_{esc}/\pi)$=0.91	Top cell assumed to be optically thin for photons with energy close to the band-edge. In case of an optically thick cell, the probability is then $n_{ref}^2/(n_{ref}^2+1)$=0.93 [4.40]. Consequently, the difference is close to negligible.

Table 4.2 *List of assumptions used for the model with their justifications and implications*

4.3 Results and discussion

4.3.1 Impact of Luminescent Coupling

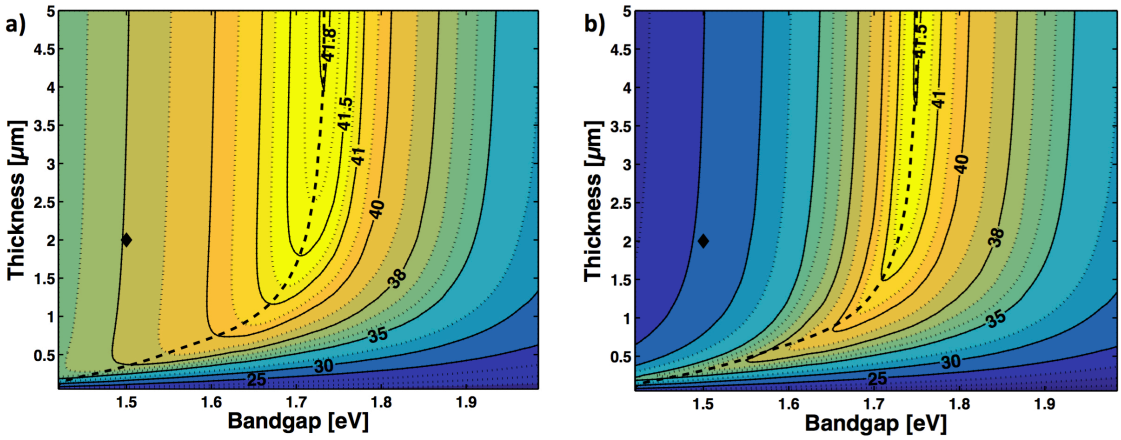

FIGURE 4.5. *Theoretical maximum isoefficiency contours of a Lambertian surface GaAsP/Si dual junction solar cell as a function of the top cell bandgap and thickness with (a) and without (b) taking into account the impact of LC between the cells. The dashed line represents the optimal bandgap-thickness combinations. The diamond-shaped dot is the particular case exposed in FIGURE 4.6.*

FIGURE 4.5 presents the impact of LC on the maximal theoretical efficiency of a Lambertian surface tandem GaAsP/Si dual junction solar cell. Both graphs are isoefficiency contours as a function of the bandgap and the thickness of the GaAsP top cell, with (a) and without (b) taking into account the impact of LC. The dashed line represents the optimal bandgap-thickness combinations. The diamond-shaped dot is the particular case of a 1.5 eV, 2 µm-thick top cell highlighted in FIGURE 4.6.

The impact of LC for non-optimised top cell bandgap-thickness combinations is apparent when a higher than optimal photocurrent is generated in the top cell, as it is the case on top and on the left of the dashed line, with a lower than optimal bandgap/ higher than optimal thickness for the top cell. LC rebalances the currents between the top and bottom cells as shown in FIGURE 4.6, where the boost to the bottom cell J_{sc} amounts to nearly 7 mA.cm^{-2} in the case of a 1.5 eV, 2 µm-thick top cell. In that case, the negative impact of a non-optimised structure on the efficiency of the tandem solar cell is reduced thanks to LC. However, when the bottom cell is the one producing a

higher than optimal current (to the right of and under the dashed line), this cascading process cannot happen, as the energy of the photons reemitted from the bottom cell is too low for these photons to be absorbed in the top cell.

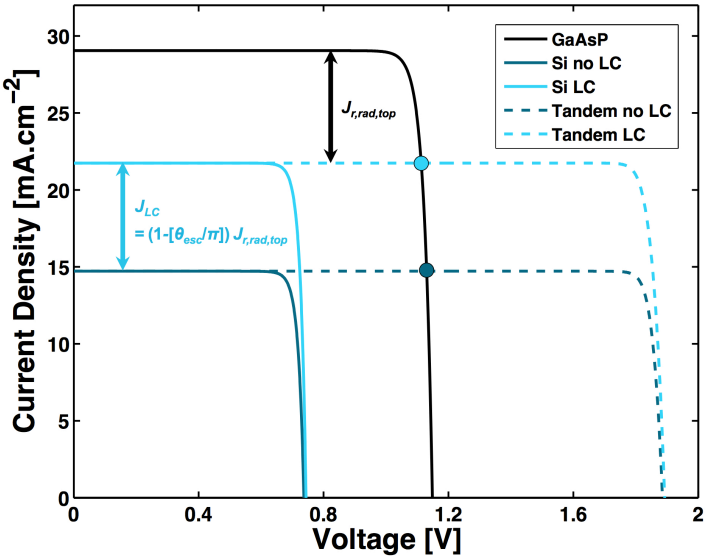

FIGURE 4.6. *J-V characteristic of the GaAsP top cell (black), Si bottom cell (dark/light blue solid line) and full dual junction cell (dark/light blue dashed line) in a tandem GaAsP/Si architecture with (light blue) and without (dark blue) taking into account LC. The top cell has a bandgap of 1.5 eV and is 2 µm-thick. The light and dark blue dots represent the approximate maximal power point of the GaAsP top cell in each case.*

4.3.2 Impact of top cell thickness and surface texturing

FIGURE 4.7 shows the maximal theoretical efficiency (in red, right scale) and the optimal top cell bandgap (in black, left scale) as a function of the top cell thickness L_{top} for both surface geometries investigated, assuming no TDs (no SRH recombination). When L_{top} is higher than 1.5 µm, the surface geometry not only has an impact on the efficiency of the dual-junction cell but also on the optimal bandgap of the top cell. This is due to the strong increase in absorptivity in the bottom cell with a Lambertian surface while the absorptivity in the top cell is only slightly impacted. This difference in optimal top cell bandgaps can represent up to 0.05 eV (1.73 eV with a Lambertian surface versus 1.78 eV with a flat surface) for L_{top} higher than 4 µm. A smaller bandgap in the top cell is then needed to balance the currents in the

two cells: the top cell current is increased while the bottom cell current is decreased. However, for very thin top cells (less than 1 µm), the impact of the textured surface on the top cell absorptivity is much stronger and counterbalances the increase in absorptivity in the bottom cell. Therefore, the optimal bandgaps are nearly identical for both surface configurations.

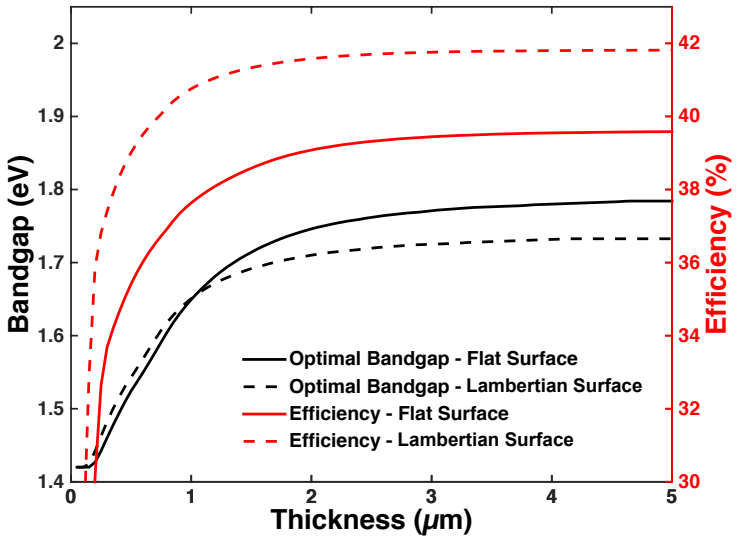

FIGURE 4.7. *Efficiency (in red, right scale) and optimal top cell bandgap (in black, left scale) as a function of the top cell thickness for a flat surface (solid line) and a Lambertian surface (dashed line) $GaAs_xP_{1-x}$ /Si dual-junction solar cell.*

For the same reasons, the impact of the Lambertian surface on the efficiency of the dual-junction solar cell is higher for thin top cells (less than 1 µm-thick), as the improvement in absorptivity happens in both cells. For thicker top cells, a Lambertian surface has a smaller effect on the overall efficiency. The maximal theoretical efficiency for the largest top cell thickness investigated (5 µm) is 41.8 % with a Lambertian surface and 39.6 % with a flat surface.

The overall efficiency increases with the top cell thickness although it plateaus over 2 µm. For a flat surface cell, a 1 µm-thick top cell is able to achieve an efficiency of 37.6 % while a 2.2 µm-thick achieves 39.2 %. This represents 95 % and 99 % of the highest theoretical efficiency calculated, respectively. For a Lambertian surface, 0.7 µm and 1.6 µm top cell thicknesses are able to achieve efficiencies of 39.7 % and 41.4 %, representing 95 % and 99 % of the highest calculated efficiency, respectively.

For the rest of this study, a 2 µm top cell thickness has been chosen. For a dual-junction solar cell with a flat surface, this represents a maximal theoretical efficiency of 39.1 % and an optimal top cell bandgap of 1.75 eV. With a Lambertian surface the efficiency increases to 41.6 % with a top cell optimal bandgap of 1.71 eV.

4.3.3 Impact of the Threading Dislocation Density

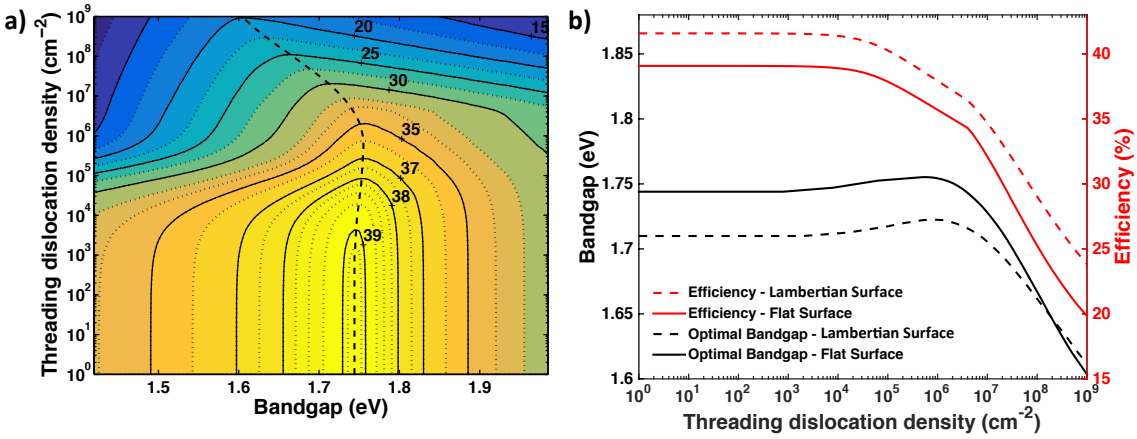

FIGURE 4.8. *a) Maximal theoretical efficiency of a flat surface $GaAs_xP_{1-x}$/Si dual-junction solar cell as a function of the top cell bandgap and TDD. The dashed line represents the optimal bandgap for each TDD. b) Optimal bandgap of the top cell and maximal theoretical efficiency of a flat surface (solid line) and Lambertian surface (dashed line) $GaAs_xP_{1-x}$/Si dual-junction solar cell as a function of the TDD.*

FIGURE 4.8 shows the impact of the TDD ρ_{TD} on the efficiency of a $GaAs_xP_{1-x}$/Si dual-junction solar cell with a 2 µm-thick top cell, considering flat and Lambertian surfaces. FIGURE 4.8a) displays the theoretical maximal efficiency as a function of the top cell bandgap and the TDD for a flat surface only. FIGURE 4.8b) shows the theoretical maximal efficiency and the optimal bandgap as a function of the TDD for both surface geometries. Low TDDs ($\rho_{TD}<10^4$ cm^{-2}) barely have any impact on the maximal efficiency or the optimal bandgap. Above 10^4 cm^{-2} ($\rho_{TD}>10^4$ cm^{-2}), the efficiency begins to slowly drop as a result of the reduction in open-circuit voltage and fill factor of the top cell. This is due to the increased SRH recombination rate related to the increased TDD. This is clear in FIGURE 4.9 where the drop of V_{oc} of the dual-junction solar cell is evident for $\rho_{TD}>10^4$ cm^{-2}. However, the short-circuit current of the top cell is not impacted and its optimal bandgap is only slightly impacted up to

$\rho_{TD}\approx 4\times10^6$ cm^{-2}. When the TDD is increased over 4×10^6 cm^{-2} ($\rho_{TD}>4\times10^6$ cm^{-2}), the diffusion length of minority carriers in the base becomes smaller than the base thickness and the collection of photo-generated charge carriers begins to drop. As shown in FIGURE 4.10, the short-circuit current of the top cell is, thus, reduced and a lower top cell bandgap is needed to rebalance the currents between the two subcells.

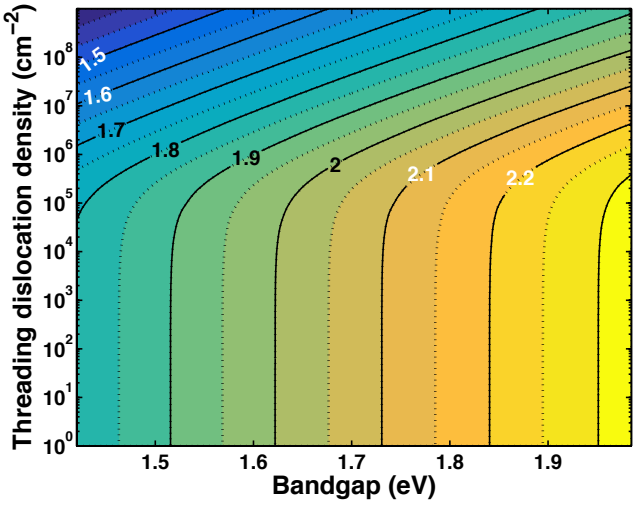

FIGURE 4.9. *Open-circuit voltage V_{oc} of a flat surface $GaAs_xP_{1-x}$/Si dual-junction solar cell as a function of the top cell bandgap and TDD.*

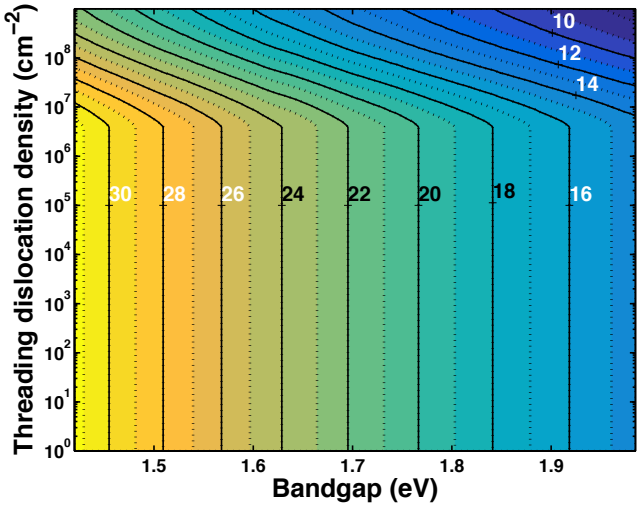

FIGURE 4.10. *Short-circuit current density $J_{sc,top}$ of the top $GaAs_xP_{1-x}$ solar cell (flat surface) as a function of the top cell bandgap and TDD.*

One important aspect is the impact of the TDD on the efficiency of LC. Indeed, when a consequent level of TDs is accounted for, non-radiative SRH recombination takes over radiative recombination and LC is quenched. This is evident in FIGURE 4.11a), which displays the current boost in the bottom cell due to LC, calculated from Equation (4.24), as a function of the bandgap and the TDD. As expected for low TDD values, the boost due to LC is very dependent on the top cell bandgap. For bandgaps lower than the optimum of about 1.7 eV, the LC boost decreases steadily when the top cell bandgap increases. For bandgaps above the optimum, the LC boost is small and does not vary strongly, indicative of the top cell being the limiting one in terms of current density. On the contrary, for TDD values higher than 10^5 cm^{-2}, the current density boost due to LC decreases rapidly when the TDD increases, and its dependency on the top cell bandgap is reduced. As shown in FIGURE 4.11b), which displays the LC boost as a function of the TDD in the particular case of a 1.5 eV top cell bandgap, the LC boost to the bottom cell current density decreases rapidly when the TDD is increased over 10^4 cm^{-2}, and becomes negligible over 10^6 cm^{-2}.

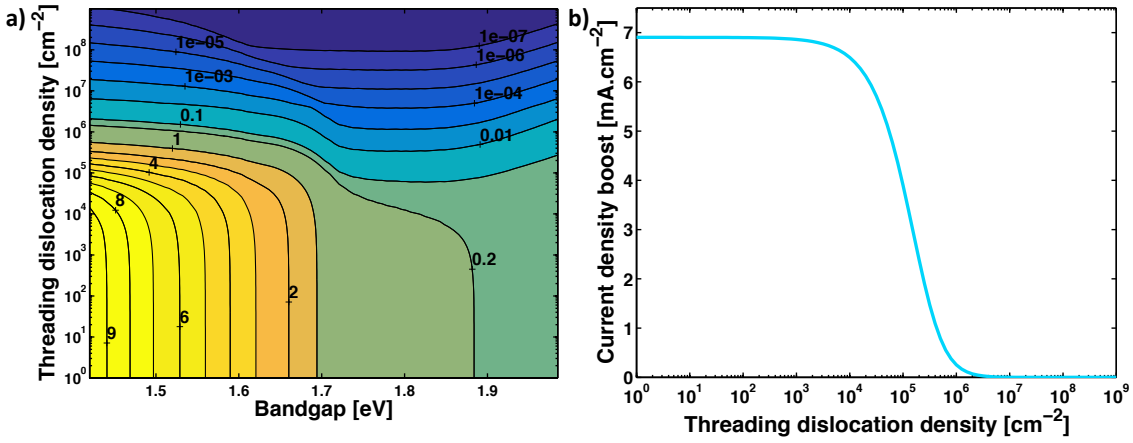

FIGURE 4.11. *a) Current density boost, in mA.cm^{-2}, in the bottom cell due to LC as a function of the top cell bandgap and TDD. Here a 2 µm-thick top cell with a Lambertian surface is modelled. b) Projection in the case of a 1.5 eV top cell bandgap.*

As shown in FIGURE 4.12, the operating current density of the tandem GaAsP/Si dual junction cell is subsequently very dependent of the TDD for lower than optimal top cell bandgaps. This is particularly the case for TDD values between 10^4 cm^{-2} and 10^6 cm^{-2}, as indicated by the iso-current density contours being relatively horizontal

and close one to the other for bandgaps under 1.7 eV. This is also apparent in FIGURE 4.8a), with the iso-efficiency contours being closer to one another and bending horizontally for TDDs between 10^4 cm^{-2} and 10^6 cm^{-2} and top cell bandgaps under 1.7 eV. As a consequence, the welcome flexibility in the design and operations of the cell gained from LC, as demonstrated in Ref. [4.44], is lost for ρ_{TD}>10^4-10^5 cm^{-2}. For ρ_{TD}>10^6 cm^{-2}, non-ideal conditions – such as high temperatures or an incident spectrum different from AM1.5 – will have a strong negative impact on the performance of the cell.

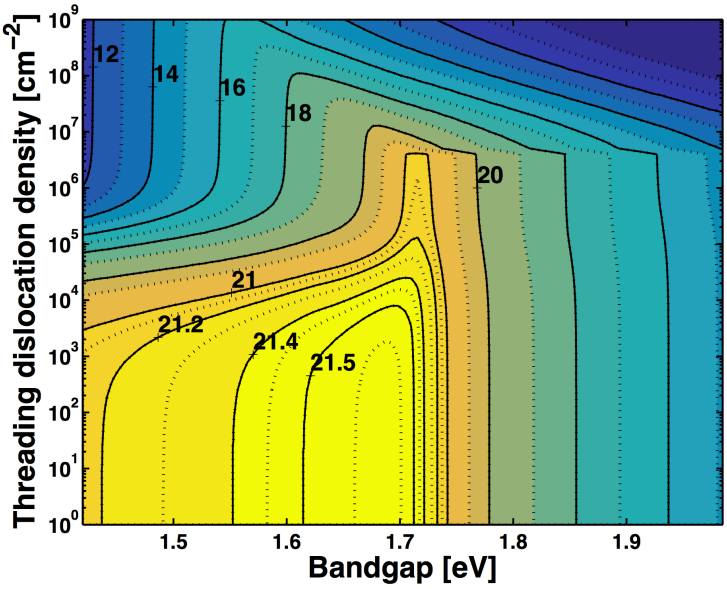

FIGURE 4.12. *Operating current density of a Lambertian surface dual junction GaAsP/Si tandem solar cell as a function of the top cell bandgap and TDD. The top cell thickness is fixed at 2 µm.*

Note that our model only approximates the impact of reduced diffusion lengths on short-circuit currents. In particular for high TDDs, with carrier diffusion lengths shorter than the device thickness, the generation profile becomes very relevant for the carrier collection under short-circuit conditions. Since we work here with the approximation of a uniform generation rate, the results for ρ_{TD}>10^6 cm^{-2} are not a quantitatively accurate description of the impact of the dislocations. The qualitative trend is nevertheless reproduced using this simplifying approximation, allowing valuable insights for the design of future GaAs$_x$P$_{1-x}$/Si dual-junction solar cells. In particular, the quality of approximation increases with decreasing TDD. Therefore,

our model is a good approximation for the range of material qualities targeted in practice. A most notable result is that the efficiency drops rapidly for $\rho_{TD}>10^5$ cm^{-2}. Thus, we conclude that a TDD lower than 10^5 cm^{-2} should be targeted for practical devices. Further reduction in TDD does have a positive impact but does not yield such an increase in efficiency, especially once $\rho_{TD}<10^4$ cm^{-2}.

4.3.4 Evaluation of the real-world potential of the investigated $GaAs_xP_{1-x}$/Si dual-junction architecture

Two factors strongly contributing to the losses of high efficiency industrial solar cells are relatively easy to integrate into our model: non-ideal EQE and non-TD-related SRH recombination, in particular surface recombination at the top and bottom interfaces of both subcells. A non-ideal EQE will mainly reduce the short-circuit current of the subcells while the presence of surface recombination will predominantly reduce their open-circuit voltage.

Dominant processes responsible for a non-ideal EQE are optical losses – such as shading from the front grid and reflection at the top surface – and high recombination rates of carriers generated close to the top and bottom surfaces. This is particularly the case for carriers generated from high energy photons (blue light) in the emitter, where the doping is strong and leads to a high recombination rate. In order to simulate this impact, a multiplication coefficient ξ can be added to the best-case-scenario front absorptivity Equations (4.11-4.12) of individual GaAs and Si cells so that the experimental and theoretical short-circuit current densities fit. Though ξ only represents an average EQE and the wavelength dependence of the actual EQE is lost using this artifice, it allows us to roughly simulate the impact of a non-ideal EQE on the short-circuit current density. Using data for published results of very high efficiency Si and GaAs solar cells [4.45-4.46], average EQE of $\xi_{Si}=0.945$ and $\xi_{GaAs}=0.9$ are calculated. In our dual-junction architecture, as most of the high-energy photons are absorbed in the $GaAs_xP_{1-x}$ top cell, the absorption in the emitter of the silicon bottom cell – where the recombination rate is high – will be small and a higher EQE in the silicon bottom cell is not unreasonable.

Surface recombination can be simulated by directly adding a surface recombination rate $R_{surf}(V)$ with an ideality factor of 1 to the flow-equilibrium Equations (4.22-4.23,4.25). These surface recombination rates are calculated from the surface saturation current density $J_{0e,Si/GaAs}$ so that:

$$R_{surf,Si/GaAs}(V) = \frac{J_{0e,Si/GaAs}}{q}\left(1 - e^{\frac{qV}{k_B T}}\right) \tag{4.26}$$

Experimental data have been published in Ref. [4.46] for the $1k_BT$ component of the saturation current density for very high efficiency GaAs solar cells. The total saturation current density from Ref. [4.46] is the sum of the radiative recombination current density and the surface saturation current density. Using our model adapted to an individual GaAs solar cell, we can calculate the radiative recombination current density expected from such a device. A surface saturation current density $J_{0e,GaAs}$=2.75×10^{-6} fA.cm^{-2} has been estimated this way. As the intrinsic carrier concentration of $GaAs_xP_{1-x}$ is smaller than the one of GaAs, the surface recombination parameter and consequently the surface saturation current density need to be normalized by the ratio $n^2_{i,GaAsP}/n^2_{i,GaAs}$ – the surface recombination rate being linearly dependent on n_i^2 – in order to be applied to our dual-junction model. Therefore, we have:

$$J_{0e,top} = J_{0e,GaAs} \times \frac{n^2_{i,GaAsP}}{n^2_{i,GaAs}} = 2.75\times10^{-6} \times \frac{n^2_{i,GaAsP}}{n^2_{i,GaAs}}\ fA.cm^{-2} \tag{4.27}$$

For the $GaAs_xP_{1-x}$ top cell, surface recombination can be limited by growing passivation layers on both sides the cell – such as a window layer on the front side and a back-surface field on the back side – so the best-in-class surface saturation current densities calculated for individual GaAs solar cells are probably achievable with the architecture investigated. However, for the silicon bottom cell, only advanced surface passivation techniques are able to yield very high efficiencies through low surface saturation current densities (around 25 fA.cm^{-2} each for the top and bottom surfaces [4.47] so around 50 fA.cm^{-2} in total). These advanced passivation techniques are probably not compatible with epitaxial growth of III-V materials on silicon. As the passivation potential of the III-V/Si interface is unknown, the value of 50 fA.cm^{-2} appears very hopeful and only represents an upper limit on the cell performance. In the expected case where the III-V/Si interface does not efficiently

passivate the front surface of the Si cell, it is preferable to use very strong emitter doping densities with a sheet resistance range of about 30-50 $\Omega.\square^{-1}$. This will lead to a surface saturation current density for the bottom cell about one order of magnitude higher: in the range of 300 to 500 fA.cm^{-2} [4.47]. As we seek to provide an upper and a lower bound to the expectable realistic performance of a III-V/Si tandem junction, we have investigated the impact of two values for the silicon bottom cell surface saturation current density: 50 fA.cm^{-2} (unlikely best-case scenario with very good passivation from the III-V/Si interface) and 500 fA.cm^{-2} (highly doped silicon bottom cell emitter).

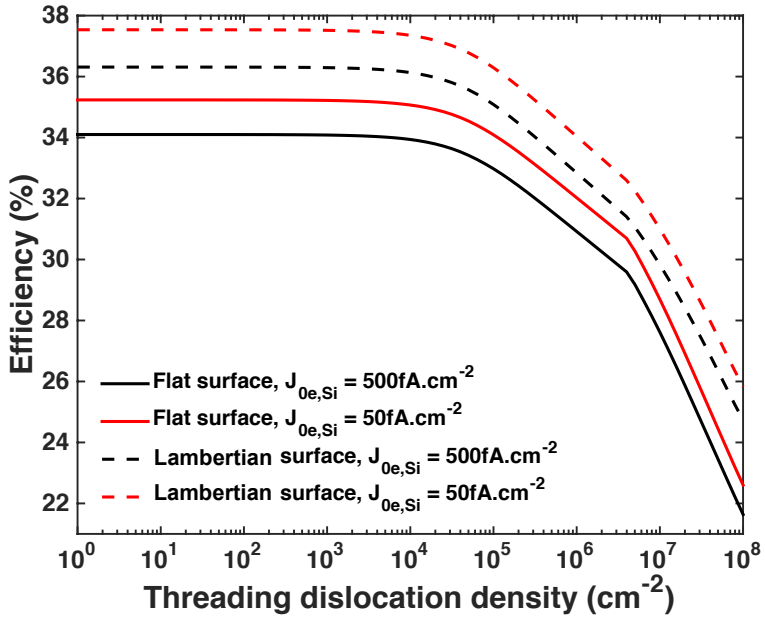

FIGURE 4.13. *Maximal theoretical efficiency as a function of the TDD of flat surface (solid lines) and Lambertian surface (dashed lines) $GaAs_xP_{1-x}$/Si dual-junction solar cells with non-ideal EQE and different surface saturation current densities for the Si bottom cell.*

FIGURE 4.13 shows the results of our model when taking into account these non-ideal EQEs and surface saturation currents for a $GaAs_xP_{1-x}$/Si dual-junction solar cell with a top cell thickness of 2 µm and flat and Lambertian surfaces. Noteworthy results are also detailed in TABLE 4.3. For a flat surface, maximum efficiencies of 35.2 % and 34.1 % are found for silicon bottom cell surface saturation current densities of 50 fA.cm^{-2} and 500 fA.cm^{-2}, respectively (37.5 % and 36.3 % with a Lambertian

surface). Thus, the impact of relatively high surface recombination rates due to a strongly doped emitter is moderate (up to 1.2 % absolute efficiency loss). Though the optimisation of the silicon front-side passivation should be considered at some point, it is not the biggest source of efficiency improvement. Comparatively, texturing the front side presents greater efficiency improvements (up to 2.2 %). These maximal efficiencies are barely impacted by TDDs up to $\rho_{TD}=10^4$ cm^{-2}. For $\rho_{TD}>10^4$ cm^{-2}, the maximal efficiencies drop rapidly and, at $\rho_{TD}=10^7$ cm^{-2}, reach a level comparable with or lower than the best single junction solar cells achieved so far [4.48].

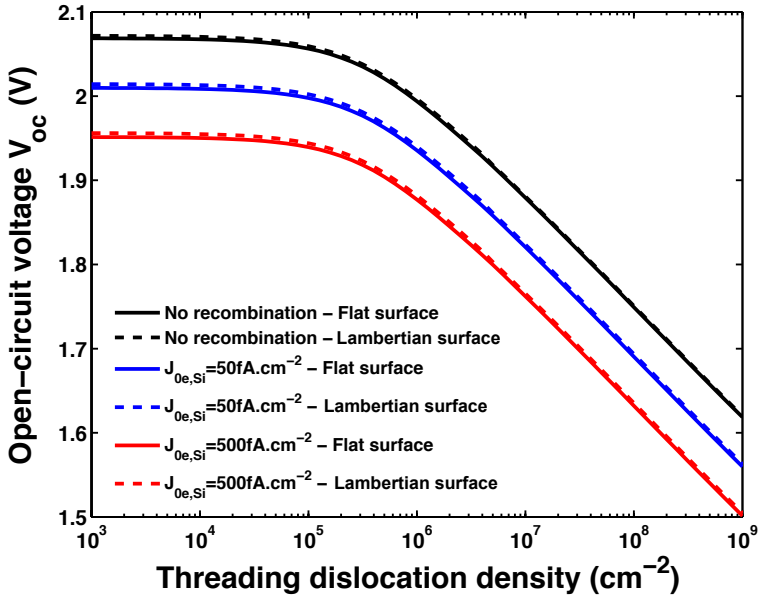

FIGURE 4.14. *Open-circuit voltage V_{oc} as a function of the TDD of flat surface (solid lines) and Lambertian surface (dashed lines) $GaAs_xP_{1-x}$/Si dual-junction solar cells with a 1.7 eV $GaAs_xP_{1-x}$ top cell and different surface saturation current densities for the Si bottom cell.*

FIGURE 4.14 gives more insights on the impact of the surface recombination on the open-circuit voltage of the tandem junction solar cell. When taking into consideration a non-perfect EQE and surface recombination in both cells, the drop of V_{oc} for the dual-junction solar cell is about 60 mV with a Si bottom cell surface saturation current density $J_{0e,bottom}$=50 fA.cm^{-2} and 120 mV with $J_{0e,bottom}$=500 fA.cm^{-2}. It is to be noted that the light trapping barely has any impact on the open-circuit voltage, as the increase in efficiency from light trapping is mainly due to an increase in J_{sc}.

Surface geometry	$J_{0e,Si}$ (fA.cm^{-2})	Efficiency (%)				
		N_{TD} = 10^0 cm^{-2}	N_{TD} = 10^4 cm^{-2}	N_{TD} = 10^5 cm^{-2}	N_{TD} = 10^6 cm^{-2}	N_{TD} = 10^7 cm^{-2}
Flat	50	35.2	35.1	34.1	32.0	28.7
	500	34.1	33.9	33.0	30.9	27.6
Lambertian	50	37.5	37.4	36.3	34.0	31.0
	500	36.3	36.1	35.1	32.8	29.8

Table 4.3 *Efficiencies of dual-junction $GaAs_xP_{1-x}$/Si solar cells for different front surface geometries (flat and Lambertian) and silicon bottom cell surface saturation current densities $J_{0e,bottom}$.*

These results show again that a TDD smaller than 10^5 cm^{-2} in the $GaAs_xP_{1-x}$ active region should be targeted to harness the full potential of $GaAs_xP_{1-x}$/Si tandem solar cells. However, up to $\rho_{TD}=10^6$ cm^{-2}, efficiencies over 30 % are still achievable. It should be noted that these are rough estimations as the model does not take into account series resistance that would reduce the fill factor of the cell and, henceforth, its efficiency by up to a couple of absolute per cent. Moreover, the average EQEs used here do not fully describe the collection efficiency on both ends of the absorption spectrum, in particular for the Si bottom cell.

4.3.5 Comparison with experimental data

As III-V/Si multijunction solar cell technology is still in early stage, directly comparing experimental and theoretical efficiencies of $GaAs_xP_{1-x}$/Si dual-junction cells is of limited practicality. Indeed, early stage devices suffer from a lot of non-idealities – such as high series resistance responsible for low fill factors, absence of an anti-reflection coating leading to low short-circuit currents, poor current-matching between the cells, or non-optimised silicon bottom cell – which are difficult to properly quantify and, thus, model. Moreover, $GaAs_xP_{1-x}$ cells with varying bandgaps have been fabricated, making the comparison even harder. However, an important parameter that can easily be compared between non-optimised cells of different bandgaps is the bandgap-voltage offset of the top cell, defined as $W_{oc}=E_g/q-V_{oc}$. Additionally, as the open-circuit voltage of the top cell is the main limiting parameter

for the performance of the dual-junction device, studying the W_{oc} allows for meaningful comparison between theoretical and experimental results.

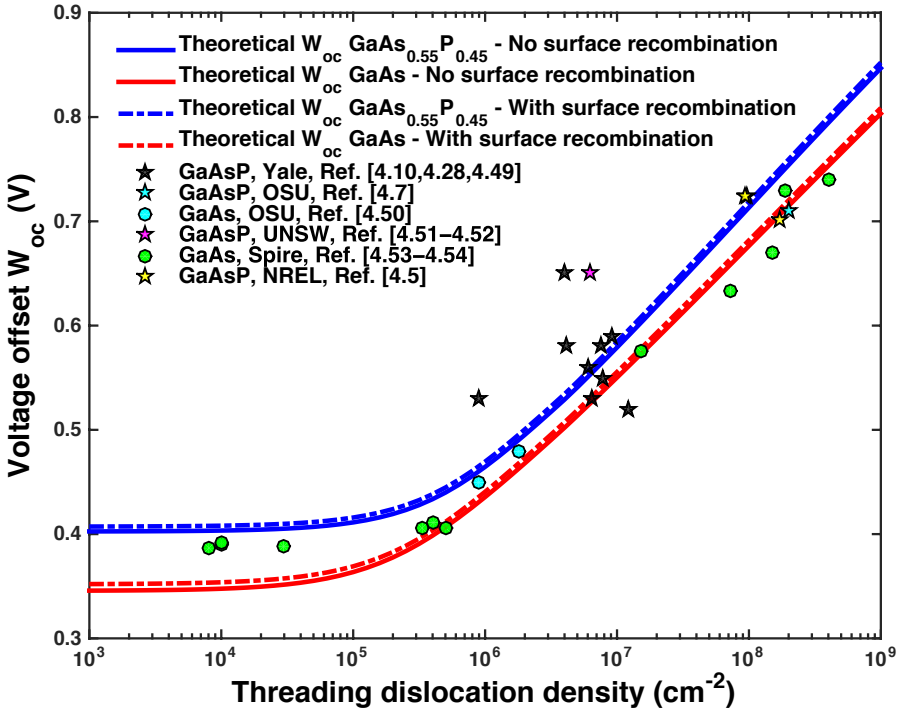

FIGURE 4.15. *Comparison of theoretical and experimental [4.5,4.7,4.10,4.28,4.49-4.54] bandgap-voltage offset values $W_{oc}=qE_g-V_{oc}$ as a function of the TDD for GaAs and $GaAs_xP_{1-x}$ solar cell. The cell is supposed to have a flat surface with no light trapping.*

FIGURE 4.15 shows our calculated W_{oc} for GaAs and $GaAs_{0.55}P_{0.45}$ – representing the boundaries of direct bandgap $GaAs_xP_{1-x}$ – as a function of the TDD with and without surface recombination, as introduced in Section 4.3.4. Experimental data points from different research groups [4.5,4.7,4.10,4.28,4.49-4.54] have been added, with $GaAs_xP_{1-x}$ and GaAs cells grown on different substrates such as GaP, GaP/Si, GaAs, GaAsP/GaAs and SiGe/Si. It is to be noted that, because of the low rate of surface recombination assumed, surface recombination has a limited impact on the calculated W_{oc}. Experimental data are in strong agreement with the theoretical model. For GaAs cells, the full range of TDD has been investigated and reducing the W_{oc} for low TDDs becomes harder as other sources of recombination begin to dominate, hence, the lowest W_{oc} values concentrated around 0.4 V even for TDDs around 10^4 cm^{-2}. For

$GaAs_xP_{1-x}$, few data points are available for a TDD below 4×10^6 cm^{-2}. Further work is needed in order to reduce the TDD by at least an order of magnitude and break the 0.5 V W_{oc} current limit.

4.4 Conclusion

An inclusive, yet simple model has been developed in order to study the impact of the Threading Dislocation Density (TDD) on the performance of $GaAs_xP_{1-x}$/Si tandem dual junction solar cells. The model is an extension of the Shockley-Queisser model [4.15], considering the radiative limit as the ultimate thermodynamic limit [4.16-4.17] on the efficiency of individual subcells. Radiative recombination rates have been calculated from Würfel's relation [4.24], considering two different models for the absorptivity of the subcells depending on the device surface texturing. In the first case a flat surface has been assumed, leading to a one-pass or a two-pass of the light inside the subcells. In the second case, we consider a Lambertian surface perfectly randomizing the incoming light flux, leading to optimal light trapping in the Si subcell [4.30]. The impact of Shockley-Read-Hall (SRH) recombination due to threading dislocations in the $GaAs_xP_{1-x}$ top cell is taken into account using the NTT model developed by Yamaguchi *et. al*. [4.18].

Considering a 2 µm-thick $GaAs_xP_{1-x}$ top cell, theoretical maximal efficiencies of 39.1 % and 41.6 % have been calculated for a flat and a Lambertian surface, respectively. The corresponding optimal bandgaps are 1.75 eV for a flat surface and 1.71 eV for a Lambertian one. The impact of TDs is limited for TDDs up to 10^4 cm^{-2}. For TDDs over 10^4 cm^{-2}, as minority carriers' diffusion lengths and consequently their lifetime are reduced, the open-circuit voltage of the $GaAs_xP_{1-x}$ top cell decreases steadily. Over 4×10^6 cm^{-2}, as the minority carrier diffusion length get smaller than the cell thickness, the photon collection efficiency and, thus, the short-circuit current are also impacted, leading to a faster reduction in efficiency with increasing TDD. Luminescent coupling (LC) between the cells is also strongly impacted by TDs: as non-radiative recombinations take over radiative ones in the top cell, LC is quenched and the current boost in the Si bottom cell drops rapidly. In particular we show that LC starts to be impacted with relatively low TDD levels (10^4 cm^{-2}) and becomes

negligible when the TDD reaches 10^6 cm^{-2}. Cells with a TDD over 10^5-10^6 cm^{-2}, thus, need to be closely current-matched and will be particularly sensitive to spectral mismatch.

Taking into account non-ideal EQEs and the impact of some non-TD-related SRH recombination – in particular surface recombination – in both subcells, an estimation of the real-world potential of the technology has been calculated. The main outcome of the study is that, although efficiencies over 30 % are still achievable with a TDD under 10^6 cm^{-2}, a TDD of 10^5 cm^{-2} or less is needed to obtain devices with efficiencies over 35 %. Although desirable, further reducing the TDD does not yield substantial improvements, particularly once the TDD gets under 10^4 cm^{-2}. Once the TDD gets over 10^7 cm^{-2}, the efficiency of the $GaAs_xP_{1-x}$/Si dual junction solar cell falls to values on par with the best mono-junction solar cells on record.

Finally the model developed, although simple, is relatively versatile and can be easily adapted to other architectures. Theoretical efficiencies of other architectures, such as the AlGaAs/Si one presented in Chapter 5, could be easily calculated provided that the absorption spectra of the materials used are known. Triple junction architectures can also be simulated provided some mathematical improvements in order to increase the equation solving speed of the model. With further information on effective densities of states, mobilities and relative permittivity, the impact of TDs can be estimated with a good accuracy. Although based on empirical considerations, the real-world potential of simulated architectures can also be assessed, leading to valuable insights in the design and material quality requirements for practical devices.

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Chapter 5

MBE growth of 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells on Si using dislocation filters

This chapter presents our experimental results in the development of a 1.7 eV III-V solar cell monolithically grown on Si substrates by Molecular Beam Epitaxy (MBE). The pathway used involves the direct epitaxial growth of AlGaAs on Si substrates, using a superlattice to smooth out the growth front followed by dislocation filters to reduce the Threading Dislocation Density (TDD). 1.7 eV $Al_{0.2}Ga_{0.8}As$ cells are then grown on this low TDD dislocation filter buffer. The growth and fabrication processes are detailed, as well as the characterisation techniques used. We then demonstrate that further reduction of the TDD can be achieved by performing Thermal Cycle Annealing (TCA) steps following the growth of each dislocation filter. Finally, we compare $Al_{0.2}Ga_{0.8}As$ and GaAs solar cells grown lattice-mismatched on Si as well as lattice-matched on GaAs, in order to investigate the sources of non-ideal performance of the $Al_{0.2}Ga_{0.8}As$ devices. These results have been initially presented at Photonics West OPTO 2016 – Physics, Simulation, and Photonic Engineering of Photovoltaic Devices V in San Francisco, CA, USA [5.1], at SiliconPV 2016 – 6th International Conference on Silicon Photovoltaics in Chambéry, France [5.2] and during the 44th IEEE Photovoltaic Specialists Conference (IEEE PVSC) in Washington, DC, USA [5.3].

5.1 Research background and purpose

As highlighted in Chapter 4 in the case of GaAsP/Si tandem architectures, achievement of a high efficiency (>30 %) current-matched III-V/Si dual junction solar cell requires the successful integration of a high material quality III-V top cell, with a bandgap of approximately 1.7 eV, on Si. Research in this direction has attracted a strong interest from academia and the industry in recent years, using epitaxial growth [5.4-5.13] as well as wafer bonding [5.13-5.15] and mechanical stacking approaches [5.16]. Very high efficiency III-V/Si tandem devices have been demonstrated using wafer bonding [5.13-5.15] and mechanical stacking [5.16]. However, the complexity of the processes – with stringent requirements on both of the materials' surface roughness in the case of wafer bonding and, for both techniques, a fabrication step akin to epitaxial lift-off to separate the III-V cells from their growth substrate – leads to issues when scaling up to industrial-size wafers. The industrialization of these technologies has so far proved challenging even for small-size devices, resulting in a high cost structure.

Epitaxial growth presents a straightforward pathway by using fewer processing steps and fewer tools. As detailed in Chapter 3, III-V materials are epitaxially grown on the Si substrate [5.4-5.13] – sometimes using a previously grown intermediary SiGe buffer [5.8-5.12] – which allows for the use of only one growth reactor such as MBE or MOCVD [5.4-5.5]. The main obstacles consist of the nucleation of defects at the III-V/Si interface due to the polar-on-nonpolar nature of the heterostructure, the lattice-mismatch, and the difference of thermal expansion coefficients between the materials. These defects, particularly Threading Dislocations (TDs) due to the lattice-mismatch, propagate upward in the III-V material, to the active regions of the devices where they act as recombination centres. As a result, the lifetime and diffusion length of minority carriers are reduced, leading to poor performance devices.

The issues regarding antiphase domains (APDs), caused by polar-on-nonpolar epitaxy, have been addressed using (100) Si wafers offcut 4 ° to 6 ° towards the [01-1] plane [5.17-5.18]; ensuring a two-step organisation of the Si surface prior to growth. Multiple pathways are under investigation in order to mitigate the nucleation

of TDs and reduce the Threading Dislocation Density (TDD) to a minimum [5.19]. As shown in Chapter 4, in the case of GaAsP/Si tandem cells a TDD below 10^6 cm^{-2} is required to reach efficiencies over 30 %, with efficiencies over 35 % achievable with a TDD below 10^5 cm^{-2}. In order to epitaxially grow III-V photovoltaic solar cells on Si with such a low TDD, the pathway predominantly pursued is the use of metamorphic buffers. This can either be done through a SiGe on Si metamorphic buffer, ending up in a SiGe or full Ge virtual substrate on which lattice-matched GaAsP or GaAs epitaxial growth is performed [5.8-5.12], or through a GaP on Si nucleation layer, followed by a metamorphic GaAsP buffer on which a 1.7 eV GaAsP cell is grown [5.4-5.7,5.13]. However, progress has been relatively slow using these techniques and the best devices demonstrated so far still exhibit a TDD above 10^6 cm^{-2} [5.7,5.11]. Moreover, in order to achieve a low TDD, thick metamorphic buffers are needed, leading to long growth times and a high material consumption.

An alternative pathway, presented in Chapter 3, consists of the direct growth of an AlGaAs nucleation layer, followed by Strained Layer Superlattices (SLSs) acting as Dislocation Filter Layers (DFLs) in order to reduce the TDD. This technique has recently yielded excellent results in the case of III-V on Si lasers for silicon photonics applications [5.20]. However, direct AlGaAs nucleation on Si in order to grow a high bandgap 1.5-1.7 eV AlGaAs solar cell on a Si substrate has not been reported since the work of Umeno *et. al.* and Soga *et. al.* [5.21-5.25] in the 1990's. Moreover, SLS DFLs for III-V on Si solar cell applications have so far only been used by Yamaguchi *et.al.* to grow pure GaAs devices [5.26]. In this chapter, we first present our initial experimental results – applying direct AlGaAs epigrowth and SLS DFLs to the integration of 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells on Si – and we compare these prototype devices with similar $Al_{0.2}Ga_{0.8}As$ reference cells grown lattice-matched on GaAs.

We then explore further reduction of the TDD using a growth technique developed by Soga *et. al.*, namely the use of Thermal Cycle Annealing (TCA) steps. These TCA steps can be combined with the growth of SLS DFLs, in order to improve the filtering capabilities of the DFLs and, thus, achieve a lower TDD in the devices. Annealing of the epilayers increases the mobility of Misfit Dislocations (MDs) and Threading Dislocations (TDs), increasing their chances of meeting one another. The probability

of a dislocation encounter in the DFL – leading to the dislocations merging or self-annihilating – is, thus, increased [5.27]. The best results are obtained by annealing the structure immediately before and/or after the growth of each SLS DFL [5.27]. Chen *et. al*. have recently demonstrated high material quality AlGaAs monolithically grown on Si by MBE, with a reduced TDD, using SLS DFLs coupled with TCA steps. This reduction in TDD led to high-performance quantum dot lasers for silicon photonics applications [5.28]. In particular, a TDD in the 10^5 cm^{-2} range in the active region of the laser has been demonstrated thanks to the use of TCA steps.

Thus, we report on the impact of using such TCA steps, performed immediately after the growth of each SLS DFL, on the TDD and the performance of 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells grown on Si. We demonstrate a reduction of the TDD using TCA, leading to a **new record low TDD value of $8(\pm2)\times10^6$ cm^{-2} for 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells grown on Si**. The performance of the best devices, particularly their open-circuit voltage, are consequently increased compared with the samples grown without TCA steps.

However, the bandgap-voltage offset of these $Al_{0.2}Ga_{0.8}As$ devices – defined as $W_{oc}=(E_g/q)-V_{oc}$ – remains high, with values over 0.55 V for the samples grown lattice-matched on GaAs and over 0.7 V for the samples grown lattice-mismatched on Si. This is in sharp contrast with 1.67-1.71 eV $GaAs_xP_{1-x}$ solar cells grown on Si at Yale and UNSW, using metamorphic buffers. These cells, with TDD values of 4.0-4.6×10^6 cm^{-2} using a $GaAs_xP_{1-x}$ metamorphic buffer [5.7] and 2.8×10^6 cm^{-2} using a Si_xGe_{1-x} metamorphic buffer [5.11], have demonstrated record low W_{oc} of 0.54 V and 0.48 V, respectively [5.7,5.11]. These strong differences in W_{oc} between our devices and the solar cells grown at Yale and UNSW – in spite of TDDs in the same order of magnitude – indicate that the bulk material quality of our $Al_{0.2}Ga_{0.8}As$ solar cells is low, independent of the presence of TDs.

The growth of high material quality $Al_xGa_{1-x}As$ is notoriously challenging. In particular, $Al_xGa_{1-x}As$ device performance is known to be particularly sensitive to potential oxygen contamination of the growth chamber [5.29]. In order to confirm the origin of these poor performance, a comparative study has been carried out: 1.7 eV $Al_{0.2}Ga_{0.8}As$ and 1.42 eV GaAs solar cells have been grown lattice-mismatched on Si

as well as lattice-matched on GaAs, as a reference. GaAs being less sensitive to oxygen contamination, a difference of behaviour between the $Al_{0.2}Ga_{0.8}As$ and GaAs devices is expected, in particular regarding their W_{ocs}. Additionally, the growth of GaAs on Si using DFLs is interesting in itself, as such cells could be used in stand-alone single junction devices or as middle subcells in an $Ga_{0.51}In_{0.49}P$/GaAs/Si triple-junction architecture.

5.2 Experimental methods

5.2.1 Growth

All growth runs were performed at UCL, in the Electrical and Electronic Engineering Department's Veeco GEN930 solid-source Molecular Beam Epitaxy (MBE) reactor. Temperatures were controlled using an infrared pyrometer and a thermocouple mounted on the back of the substrate-holder. Reflection High Energy Electron Diffraction (RHEED) was used to in-situ monitor the evolution of the growth surface during deposition, as well as during the pre-growth high-temperature oxide removal steps.

For each study, the lattice-mismatched growth runs on Si were performed on n-type Si (100) wafers offcut 4 ° toward the [01-1] plane, in order to avoid the formation of Anti-Phase Domains (APDs) due to polar-on-nonpolar epitaxy [5.17]. Standard n-type GaAs wafers were used for the lattice-matched reference samples. Prior to growth, in-situ oxide desorption was carried out at 900 °C for 10 minutes for Si substrates. For GaAs substrates, in-situ oxide desorption was carried out between 580 °C and 610 °C, using RHEED measurements to monitor the desorption process.

For growth on Si substrates, the DFL buffer consists of an $Al_xGa_{1-x}As$ nucleation layer followed by an AlAs/GaAs superlattice before deposition of four to five DFLs. The nucleation sequence has been detailed in previous publications [5.30-5.31]. Because of the large lattice-mismatch between Si and AlGaAs (about 4 %), Stranski-Krastanov (SK) growth mode is observed during the initial growth stages, with formation of islands that later coalesce. This is attested by the spotty RHEED

measurements observed during the first steps of the growth. As a result of this initial SK growth mode, a wavy growth surface is obtained, impeding the fine engineering of 2-dimensional structures such as DFLs. Thus, the 200 to 500 nm-thick AlAs/GaAs superlattice is used in order to flatten out the growth interface and obtain a smooth surface [5.32-5.33], thanks to the wetting properties of Al leading to the high surface tension of AlAs.

Each DFL is comprised of a Strained-Layer Superlattice (SLS) made of alternating compression and tension layers [5.27], inserted between two $Al_{0.2}Ga_{0.8}As$ spacers for the $Al_{0.2}Ga_{0.8}As$ devices and GaAs spacers for the GaAs devices. When used, the TCA cycles were performed immediately following the growth of each SLS DFL. Indeed, as shown in Ref. [5.27], performing TCA steps in-between the growth of DFLs improves the final material quality compared with only one set of TCA steps performed at the end of the growth. The growth was halted during these annealing steps. More details about the annealing sequence can be found in Ref. [5.28]. For the reference samples grown lattice-matched on GaAs, only the active layers of the cells – contacting layer, Back Surface Field (BSF) if present, base, emitter, window, and capping layer – were grown on top of a 200 nm GaAs buffer layer, without any TCA cycles. More detail regarding the structure of each set of devices is presented in Section 5.3.

5.2.2 Device fabrication

Fabrication was carried out in cleanroom environment at the London Centre of Nanotechnology, following the process flow described in Chapter 3, FIGURE 3.15. Patterning was performed by standard photolithography techniques prior to device separation by wet etching and metal contact deposition. The samples were first selectively etched in a H_2SO_4:H_2O_2:H_2O (1:10:80) solution, in order to define 3×3 mm individual mesa-structures and to access the bottom n^+-contacting layer. Before thermal evaporation of the contacts, a NH_4OH:H_2O 1:19 solution was used for 60 seconds to deoxidize the surfaces. The contact to the n-type region consists of a Ni/AuGe/Ni/Au (5 nm/100 nm/30 nm/200 nm) metal structure, thermally evaporated and annealed at 390-400 °C for 60 seconds under N_2 atmosphere. For the front grid contact to the p-type region, two different contact deposition techniques have been

used. For the initial prototype samples and the TCA test samples, a ≈200 nm-thick AuZn contact was thermally evaporated on the p^+-GaAs contacting layer, as this technique is faster and less expensive; although it gives less consistent results due to the difference in partial pressures between Au and Zn leading to disparate deposition rates. For the comparison between $Al_{0.2}Ga_{0.8}As$ and GaAs devices, a Ti/Pt/Au (20 nm/50 nm/400 nm) front grid contact was deposited by sputtering, with a better control of the deposition process and a higher reproducibility between processed batches. These contacts to the p-type region were not annealed in any case.

As the coverage of the top metal grid contact has not been optimised, resulting in a non-negligible shadowing (1.93 mm^2 to 3.14 mm^2), the current densities presented hereafter refer to the 5.86 mm^2 to 7.07 mm^2 designated area of the devices, representing the non-shadowed area of the devices. It is to be noted that the top GaAs p^+-contacting layer was not etched, in order to protect the underlying Al-rich layers from degradation, as AlAs is unstable in most air and produces arsine. Furthermore, no Anti-Reflection Coating (ARC) was applied to the samples, as no process for a high performance broadband ARC was available. As a result, sizeable optical losses arise from reflection at the front surface of the devices and absorption in the top GaAs contacting layer. Using OPAL 2 software [5.34], the short-circuit current density losses due to reflection and absorption are calculated for $Al_{0.2}Ga_{0.8}As$ devices at about 8.8 $mA.cm^{-2}$ and 5.0 $mA.cm^{-2}$, respectively. For GaAs devices, these losses are evaluated at about 12.6 $mA.cm^{-2}$ and 5.3 $mA.cm^{-2}$, respectively.

5.2.3 Characterisation

Atomic Force Microscopy (AFM) and cross-sectional Transmission Electron Microscopy (TEM) have been used to characterise the structural properties of the samples grown. AFM was carried out at UCL in a Veeco Nanoscope V Dimension 3100 SPM system in ambient conditions using tapping mode. For the cross-sectional TEM measurements, performed at University of Arkansas Institute for Nanoscience and Engineering, the samples were prepared using mechanical polishing followed by ion-milling in a Fischione 1010 ion mill. The TEM observations were carried out at 300 keV in an FEI Titan 80–300 S TEM fitted with a CEOS image corrector. The bandgap of the cells was determined by room-temperature steady-state

Photoluminescence (PL), at UCL, using a Nanometrics RPM2000 rapid photoluminescence mapping system.

Optoelectronic characterisation of the samples and devices included Current density versus Voltage (J-V) curve tracing under AM1.5G illumination, Illumination versus Open-circuit voltage (Suns-V_{oc}) characterisation, and External Quantum Efficiency (EQE) measurement. J-V characteristics of the devices were acquired at 25 °C using a Keithley 2400 sourcemeter coupled with ReRa Tracer 3.0 software. 1-sun AM1.5G spectrum illumination was obtained from a LOT solar simulator equipped with a filtered Xenon lamp and calibrated at 100 $mW.cm^{-2}$, using a GaAs calibration cell. Suns-V_{oc} characteristics were acquired using a Sinton Instruments Suns-V_{oc} system. Given the substantial difference between the absorption spectra of the measured high-bandgap III-V cells and of the 1.12 eV c-Si reference cell used to monitor illumination, filters were placed in front of the reference cell in order to reduce the spectral mismatch to a minimum [5.35]. A Schott KG3 filter was used to measure the $Al_{0.2}Ga_{0.8}As$ cells while a Techspec long-pass filter with an 875 nm cut-off wavelength was used to measure the GaAs cells. The 1-sun V_{oc} difference between the J-V measurements and the Suns-V_{oc} measurements was, thus, reduced to under 20 mV. An additional spectral mismatch coefficient was then calculated for each device in order to match the J-V and Suns-V_{oc} measurements [5.35]. Room-temperature EQEs of the best cells were measured with a ReRa SpeQuest quantum efficiency system.

5.3 Results

5.3.1 Initial $Al_{0.2}Ga_{0.8}As$ solar cells prototypes on Si

For the initial $Al_{0.2}Ga_{0.8}As$ solar cells grown on Si, the details of the structures grown are presented in FIGURE 5.1. Five SLS DFLs were grown – each of them consisting of five sets of InAlAs/AlAs superlattice tension layers and AlGaAs compression layers – separated by 300 nm-thick AlGaAs spacers. The classic cell structure consists of a 1000 nm-thick n^+-$Al_{0.2}Ga_{0.8}As$ contacting layer, a 1000 nm-thick n-$Al_{0.2}Ga_{0.8}As$ base, a 300 nm-thick p^+-$Al_{0.2}Ga_{0.8}As$ emitter, a 50 nm-thick p^+-AlAs/GaAs superlattice

window, and finally a 50 nm-thick p^+-GaAs contacting and capping layer. The contacting layer is relatively thick in order to limit the risks of under-etching or over-etching the samples when accessing it. Conversely, the base is relatively thin in order to limit the total thickness of the epilayers and, thus, the risk of thermal cracks, as presented in Chapter 3.

a) Device structure

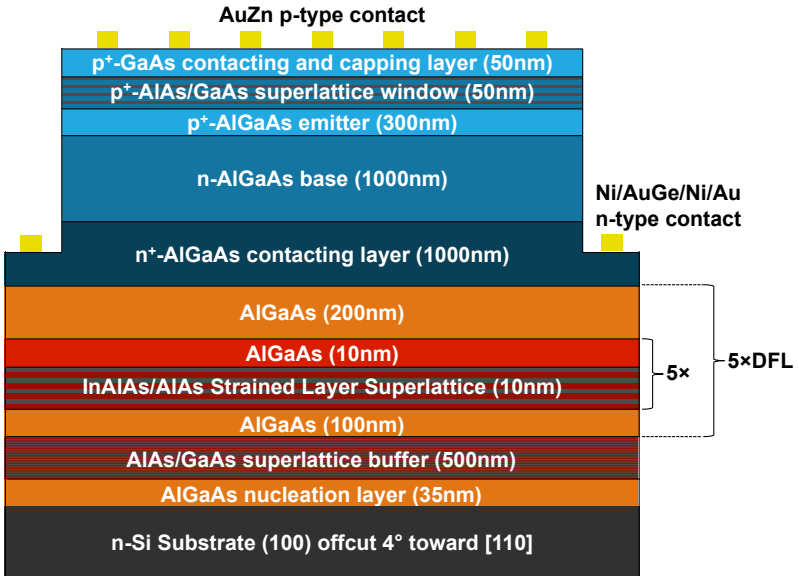

FIGURE 5.1. *Detail of the structure of the devices grown and fabricated on Si. The dislocation filter buffer is in orange/red; the active layers of the cell are in blue. For the sample grown lattice-matched on GaAs, the dislocation filter buffer in orange/red is replaced by a 200 nm-thick GaAs buffer.*

b) Material characterisation

FIGURE 5.2 shows an AFM comparison between the surfaces of the samples grown on Si (a) and GaAs (b). The sample grown on Si is rougher, with a surface roughness RMS of 2.20 nm versus 0.48 nm for the sample grown on GaAs. This greater roughness on Si stems from the relaxation of the strain caused by the 4 % lattice-mismatch between the Si substrate and the AlGaAs epilayers. As previously demonstrated by Xu *et. al.* [5.32] and Petroff *et. al.* [5.33], the AlAs/GaAs superlattice used prior to the growth of the dislocation filters contributed to the reduction of the roughness on Si. This is confirmed by the modification of the

RHEED measurements from a spotty pattern to a streaky pattern during the superlattice growth. PL measurements show very close peaks (729.4 nm on Si and 728.3 nm on GaAs), indicative of a bandgap of 1.70 eV for both samples.

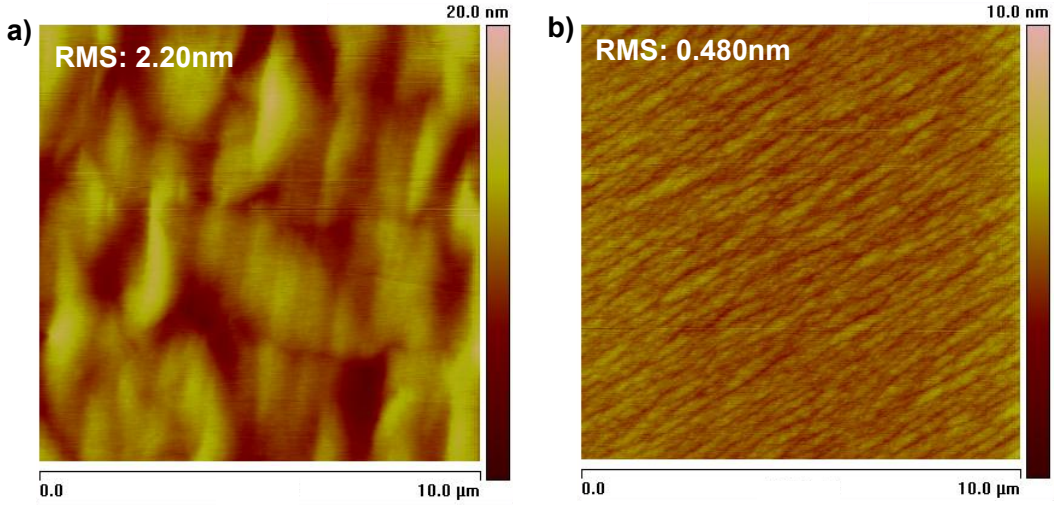

FIGURE 5.2. *AFM images of the surfaces of the samples grown on Si (a) and GaAs (b) substrates.*

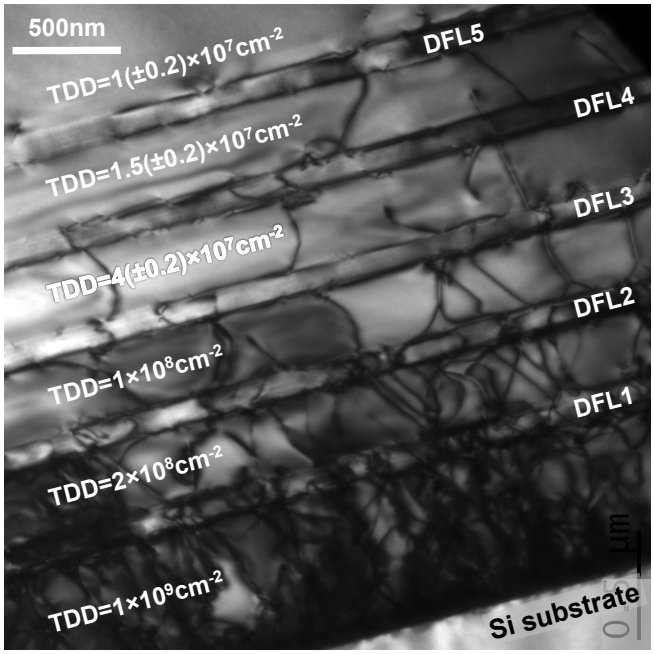

FIGURE 5.3. *Cross-sectional TEM of the sample grown on Si, showing the five Dislocation Filter Layers (DFLs) and the associated reduction of the Threading Dislocation Density (TDD).*

Impact of the DFLs on the TDD for the sample grown on Si is shown on the cross-sectional TEM image in FIGURE 5.3. As demonstrated by Chen *et. al.* [5.18], each SLS DFL reduces the TDD by about a half to a full order of magnitude. The TDD, calculated from TEM images, has been reduced from 1×10^{9} cm^{-2} at the III-V/Si interface to $1(\pm0.2)\times10^{7}$ cm^{-2} in the active layers of the devices. As the TDD approaches 10^{7} cm^{-2}, calculating a precise value becomes challenging and only an approximate count can be given. However, for AlGaAs solar cells with such a high Al content (20 %), the previous lowest TDD published was 2.1×10^{7} cm^{-2} [5.25]. Even considering the upper bound for our sample (1.2×10^{7} cm^{-2}), we demonstrate a 1.7 eV $Al_{0.2}Ga_{0.8}As$ photovoltaic solar cell with a new record low TDD.

TEM imaging of both samples also confirms a difference of thickness of the cells' active layers (base, emitter, window and both contacting layers) between the devices grown on Si and on GaAs: 2.8 µm versus 2.35 µm, respectively. This difference of thickness, due to discrepancies in the calibration of the MBE growth rates, explains the difference in short-circuit current and in EQE presented below.

c) Optoelectronic characterisation

J-V curves, acquired under illumination, of the best devices grown on Si and GaAs are displayed in FIGURE 5.4. The best cells exhibit a V_{oc} of 964 mV on Si versus 1128 mV on GaAs. This difference of V_{oc} between lattice-matched and 4 %-lattice-mismatched samples is an encouraging initial result given the non-negligible TDD on Si. Relatively low J_{sc} values have been measured: 7.30 mA.cm^{-2} on Si and 6.73 mA.cm^{-2} on GaAs. As previously mentioned, the 50 nm-thick GaAs top contacting and capping layer is responsible for a non-negligible parasitic absorption, calculated to be equivalent to a J_{sc} loss of about 5.0 mA.cm^{-2}. Reflection at the front surface, in the absence of an anti-reflection coating, is additionally responsible for a J_{sc} loss of about 8.8 mA.cm^{-2}. The best efficiencies achieved in this early-stage study are 5.46 % on Si and 6.09 % on GaAs. As expected, this difference of efficiency is mainly due to the 164 mV drop of V_{oc} for lattice-mismatched devices, compared with lattice-matched ones. As the light management inside our devices is not optimal – in particular because of high reflection at the front surface and absorption in the top contacting layer – directly comparing the efficiencies of our cells with the work of

other groups is of limited significance and comparing the V_{oc} or the bandgap-voltage offset W_{oc} makes more sense.

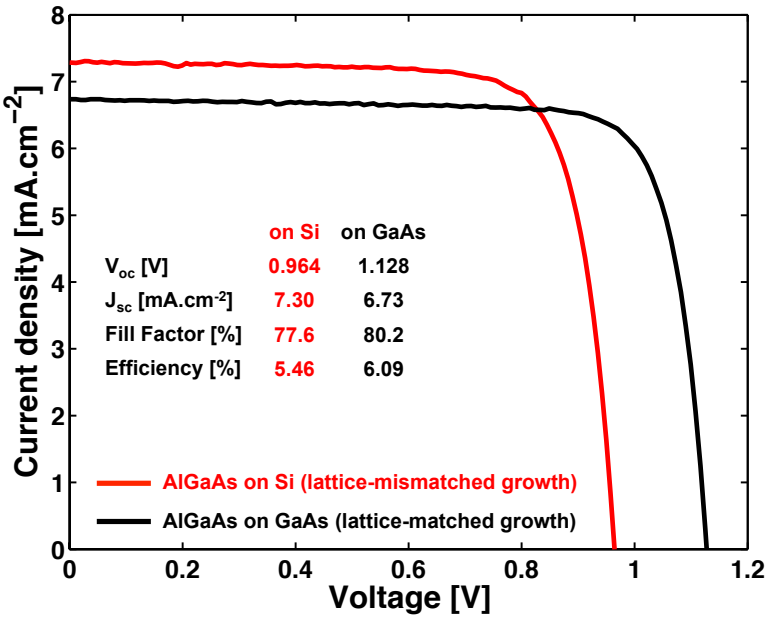

FIGURE 5.4. *J-V curves of the best devices grown on Si (red) and GaAs (black), measured under illumination. Cell parameters are also indicated.*

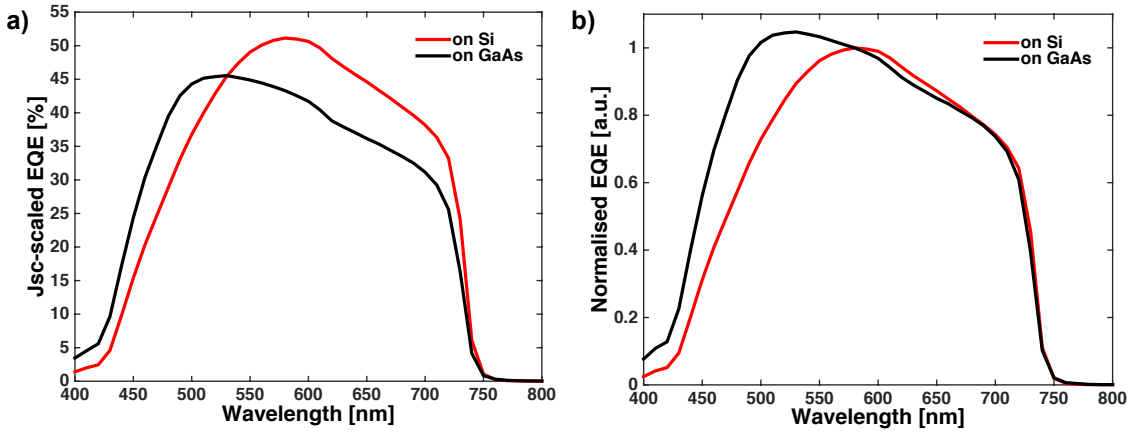

FIGURE 5.5. *J_{sc}-calibrated (a) and normalised at 580 nm (b) EQE of the samples grown on Si (red) and GaAs (black), showing an overall stronger absorption in the sample grown on Si but a better blue response from the sample grown on GaAs.*

Although the lattice-matched sample grown on GaAs exhibits a better V_{oc} than the one grown on Si, the V_{oc} absolute value is relatively low, at 1128 mV. Thus, the

bandgap-offset voltage W_{oc} is large at 572 mV, compared with the ≈0.3-0.4 V semi-empirical value expected for high quality III-V materials. This behaviour suggests a high dark saturation current strongly dominated by non-radiative recombination.

EQE measurements for both samples are displayed in FIGURE 5.5. As the J_{sc}-calibrated measurements (a) show, the principal source of difference between the J_{sc} of the cells is an overall better absorption for the device grown on Si, especially at long wavelengths above 550 nm. However, the normalised at 580 nm EQE (b) indicates a better blue response for the samples grown on GaAs. These results are in line with the difference of thickness between the samples, measured by TEM: the thicker base on Si allows for higher overall absorption but, in return, the thicker contacting layer reduces the blue response. The non-optimised structure of the devices, in particular the thin base (1000 nm), could explain the weak absorption of higher wavelength photons with energy close to the bandgap. Short diffusion lengths could also be responsible for this phenomenon.

5.3.2 Impact of Thermal Cycle Annealing (TCA) steps on the TDD

a) Device structure

For the study of the impact of TCA steps on the TDD, three samples were grown: one on Si with TCA, one on Si without TCA and one reference sample lattice-matched on GaAs. As mentioned above, TCA steps improve the material quality of the epilayers by increasing the mobility of TDs, thus enhancing the probability of TDs self-annihilating or merging [5.27].

The structure of the samples grown and fabricated on Si is presented in FIGURE 5.6. The structure of the DFL buffer, in orange/red in FIGURE 5.6, is identical to the one of our initial devices shown in FIGURE 5.1. The only difference resides in the number of DFLs grown: five in the case of the initial devices, four in the present case. The structure of the cells, in blue in FIGURE 5.6, is also similar, with a few differences: a 30 nm-thick n^+-AlAs/GaAs superlattice Back Surface Field (BSF) has been introduced, the thickness of the base has been doubled to 2000 nm and the thickness of the emitter has been slightly reduced to 200 nm.

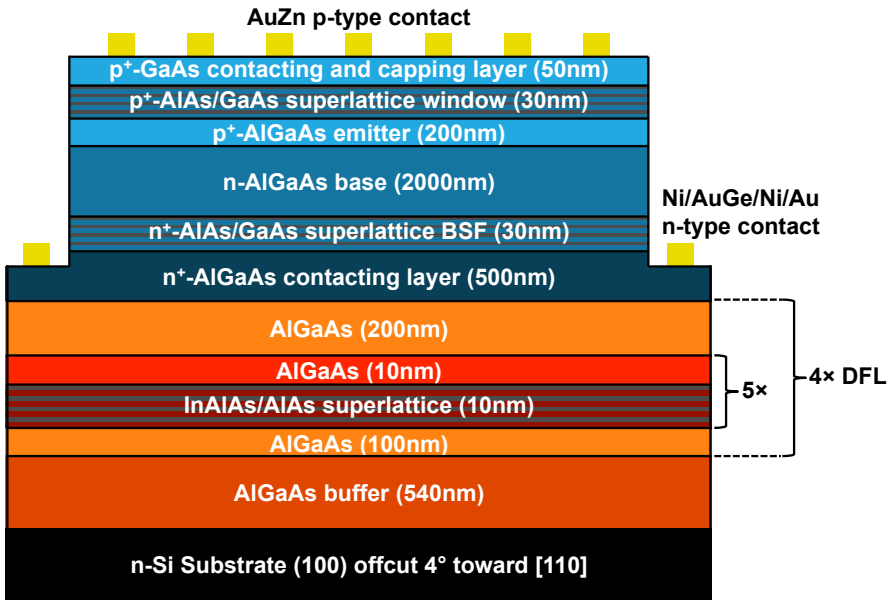

FIGURE 5.6. *Structure of the samples grown lattice-mismatched on Si. The dislocation filter buffer is in orange/red; the active layers of the cell are in blue. For the sample grown lattice-matched on GaAs, the dislocation filter buffer in orange/red is replaced by a 200 nm-thick GaAs buffer.*

b) Material characterisation

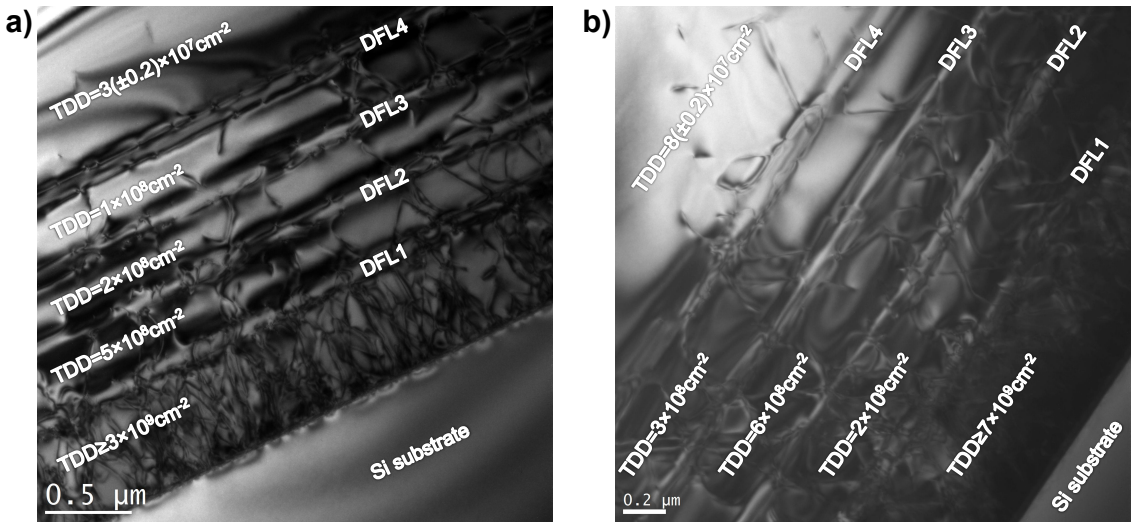

FIGURE 5.7. *TEM images of the samples grown lattice-mismatched on Si with (a) and without (b) Thermal Cycle Annealing (TCA) steps. A Threading Dislocation Density (TDD) 2 to 3 times lower has been measured throughout the sample grown with TCA.*

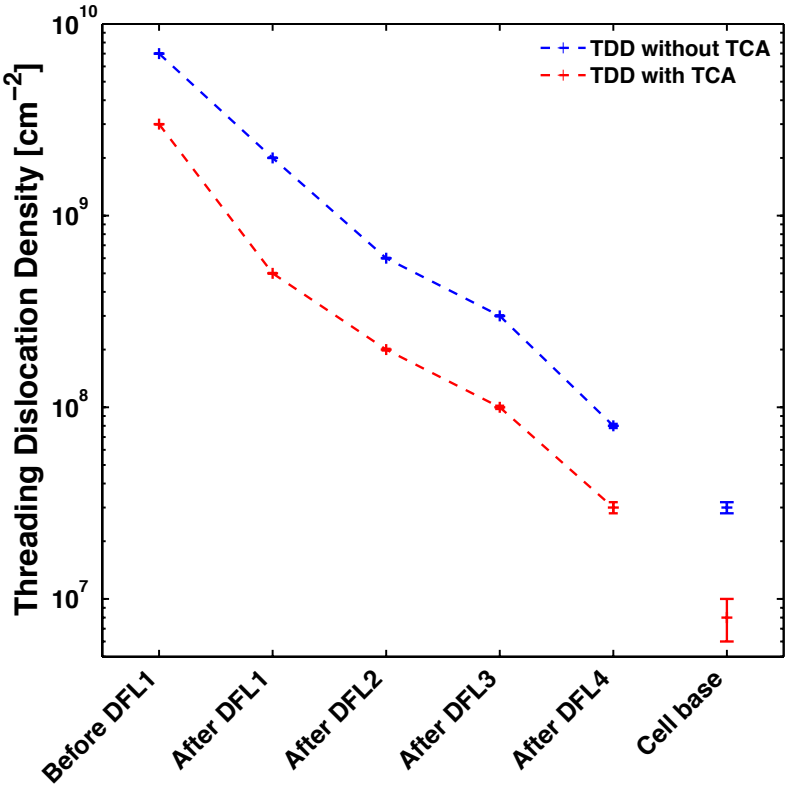

FIGURE 5.8. *Evolution of the Threading Dislocation Density (TDD) in the samples grown lattice-mismatched on Si with (red) and without (blue) TCA.*

Cross-sectional TEM images of the samples grown lattice-mismatched on Si, with (a) and without (b) TCA, are displayed in FIGURE 5.7. TCA steps enable a substantial improvement in material quality, with a TDD reduction of about 2 to 3 times throughout the sample, compared with the sample grown without TCA. In particular, for the sample grown with TCA, the TDD has been reduced from 3×10^{9} cm^{-2} at the III-V/Si interface to $3(\pm0.2)\times10^{7}$ cm^{-2} after the 4th DFL and **$8(\pm2)\times10^{6}$ cm^{-2}** in the base of the cells. Without TCA, the TDD is reduced from 7×10^{9} cm^{-2} at the III-V/Si interface to $8(\pm0.2)\times10^{7}$ cm^{-2} after the 4th DFL and $3(\pm0.2)\times10^{7}$ cm^{-2} in the base of the cells. FIGURE 5.8 shows the evolution of the TDD throughout both samples.

c) Photoluminescence characterisation

PL spectra of the 3 samples are displayed in FIGURE 5.9. As expected, the sample grown lattice-matched on GaAs exhibits a stronger intensity, with a peak at 729.4 nm. Samples grown on Si, with and without TCA, present lower intensities, with peaks at 738.5 nm and 740.6 nm representing 42.4 % and 29.6 % of the peak intensity on

GaAs, respectively. This difference in intensity is expected, given the difference in TDD calculated from TEM, as TDs reduce the probability of band-to-band radiative recombination. The difference in peak wavelength indicates a higher bandgap of exactly 1.70 eV for the sample grown lattice-matched on GaAs, versus 1.68 eV and 1.67 eV for the samples grown on Si with and without TCA, respectively. An incomplete relaxation of the materials grown lattice-mismatched could possibly explain this difference in bandgap, although more work is needed to confirm this hypothesis.

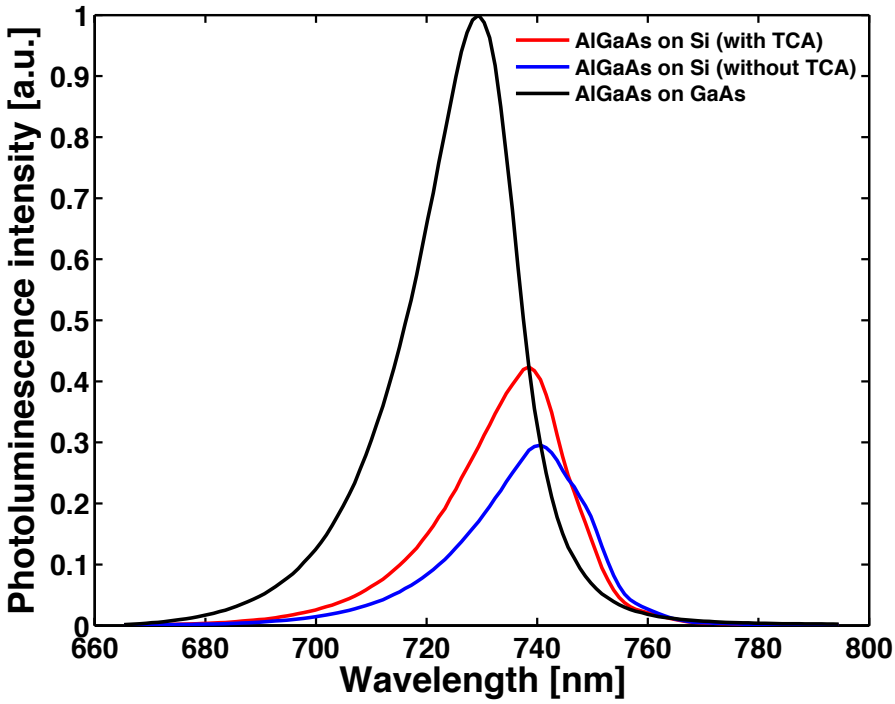

FIGURE 5.9. *Normalized photoluminescence spectra of the samples grown on Si with TCA (red), without TCA (blue) and on GaAs (black).*

d) Optoelectronic characterisation

J-V curves of the best devices fabricated from each sample, acquired under illumination, are displayed in FIGURE 5.10. Due to the presence of TDs in the active region of the cells, the samples grown on Si exhibit lower V_{oc} values than the reference cells grown on GaAs. However, the cell grown with TCA exhibits a non-negligible voltage recovery with a V_{oc} of 895 mV, compared to 833 mV without TCA and 1070 mV on GaAs. This improvement of V_{oc} is in agreement with the higher PL peak intensity and the lower TDD exhibited by the sample grown with TCA.

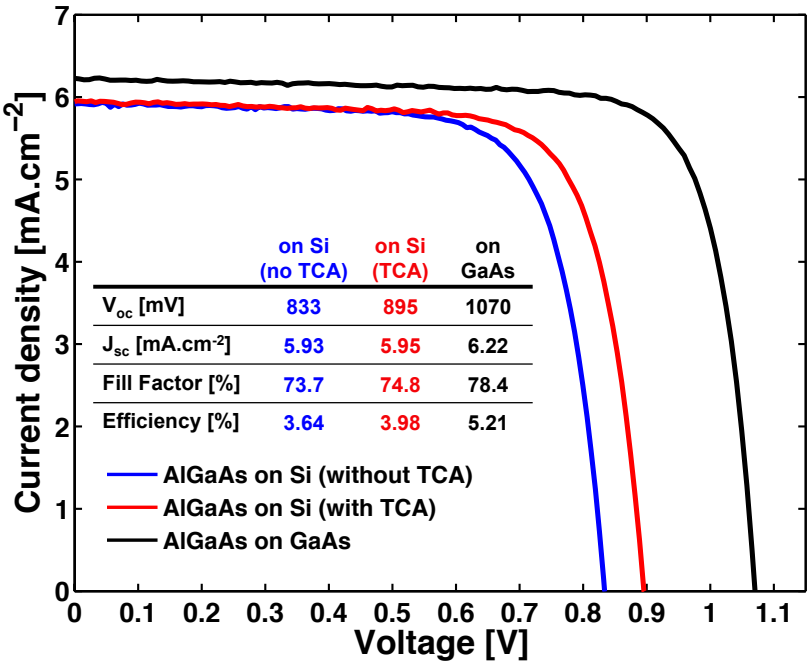

FIGURE 5.10. *J-V curves, acquired under AM1.5G spectrum illumination, of the best devices grown on Si with TCA (red), on Si without TCA (blue) and on GaAs (black). Cells parameters are also indicated.*

Again, for all the cells, the bangap-voltage offset W_{oc} is high compared to the semi-empirical ≈0.3-0.4 V expected from high performance III-V solar cells. Although this result is expected for TD-rich cells grown lattice-mismatched on Si, a high W_{oc} value of 630 mV for the reference cell grown lattice-matched on GaAs suggests issues with the structure or the material quality of the cells. High W_{oc} values have been similarly reported above, for our early prototypes. As the cell structure consists of a state-of-the-art p-n junction III-V solar cell, including a window layer and a BSF, the design of the devices is probably not at fault. Material quality of the bulk AlGaAs, leading to a high defect density on top of potential TDs, is more likely responsible for the low voltage performance of the devices.

The best cell grown on GaAs exhibits a slightly higher J_{sc}, at 6.22 mA.cm^{-2}, compared with the best cells grown on Si with and without TCA, at 5.95 mA.cm^{-2} and 5.93 mA.cm^{-2}, respectively. A longer diffusion length, due to the absence of TDs on GaAs, could potentially explain this difference. Additional characterisation, such as EQE measurement, is needed to confirm the origin of this difference in J_{sc}.

5.3.3 Comparison between $Al_{0.2}Ga_{0.8}As$ and GaAs cells grown on Si and GaAs

a) Device structure

For this comparison study, two samples have been grown for both absorber materials investigated ($Al_{0.2}Ga_{0.8}As$ and GaAs): one reference sample grown lattice-matched on GaAs and one sample grown on Si using Dislocation Filter Layers (DFLs) and Thermal Cycle Annealing (TCA). The structure of the samples grown on Si is presented in FIGURE 5.11. The DFL buffer is depicted in orange/red, the active layers of the devices are in blue. The reference samples grown on GaAs have an identical device structure, the DFL buffer being replaced by a 200 nm-thick GaAs buffer. As only one Al source was available at the time of growth, the Al deposition rate was fixed throughout the growth runs. As a result, the structure of the DFL buffer, Back Surface Field (BSF), and window layers were adapted for the GaAs cells and differ from the $Al_{0.2}Ga_{0.8}As$ samples.

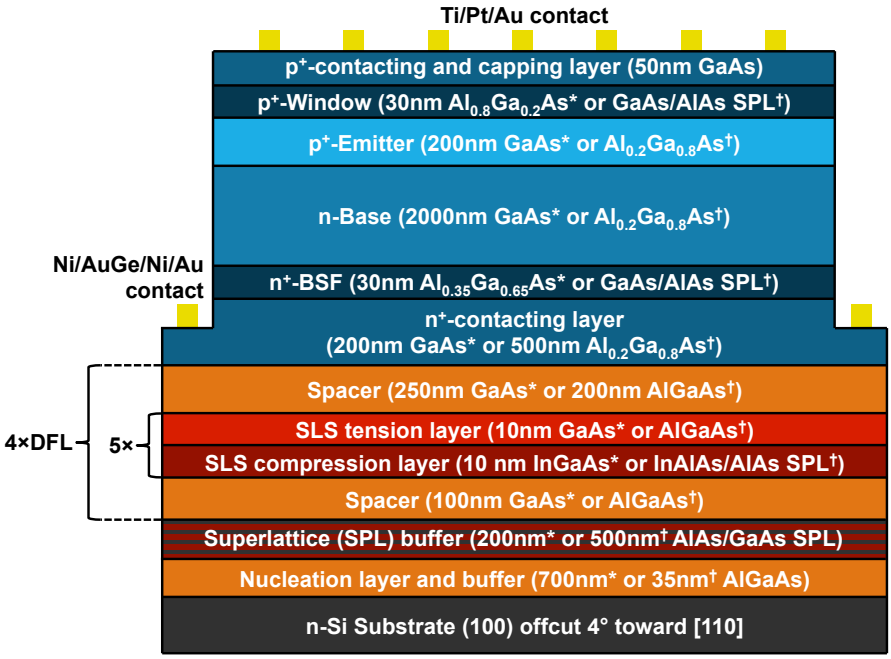

FIGURE 5.11. *Structure of the samples grown on Si. The DFL buffer is in orange/red, the active layers of the devices are in blue. The differing parameters between the two batches are indicated by the "†" symbols for the $Al_{0.2}Ga_{0.8}As$ cells and by the "*" symbols for the GaAs ones. For the reference samples, grown lattice-matched on GaAs, the DFL buffer (in orange/red) has been replaced with a 200 nm-thick GaAs buffer.*

The device structure for both absorber materials is similar to the one used for the TCA test samples shown in FIGURES 5.6. For the $Al_{0.2}Ga_{0.8}As$ cells, AlAs/GaAs superlattices have been used for the BSF and window layers. Conversely, for the GaAs cells, $Al_{0.35}Ga_{0.65}As$ and $Al_{0.8}Ga_{0.2}As$ layers have been used the BSF and window layers, respectively.

a) Impact of the DFLs on the TDD

As shown in FIGURES 5.12 and 5.13, each individual DFL reduces the TDD by a factor of two to six, similarly to what has been presented above in Sections 5.3.1 and 5.3.2. The overall TDD is, thus, reduced by two full orders of magnitude, from over 3×10^{9} cm^{-2} at the III-V/Si interface to $3(\pm0.2)\times10^{7}$ cm^{-2} just after the 4th DFL for the $Al_{0.2}Ga_{0.8}As$ sample. Not shown in FIGURE 5.12a), the TDD in the base of the cell is further reduced to $8(\pm2)\times10^{6}$ cm^{-2}. Similar reductions in TDD are demonstrated for the GaAs sample grown lattice-mismatched on Si, as shown in FIGURES 5.12b) and 5.13. The TDD in the base of the GaAs cell grown on Si has been evaluated at $5(\pm2)\times10^{6}$ cm^{-2}.

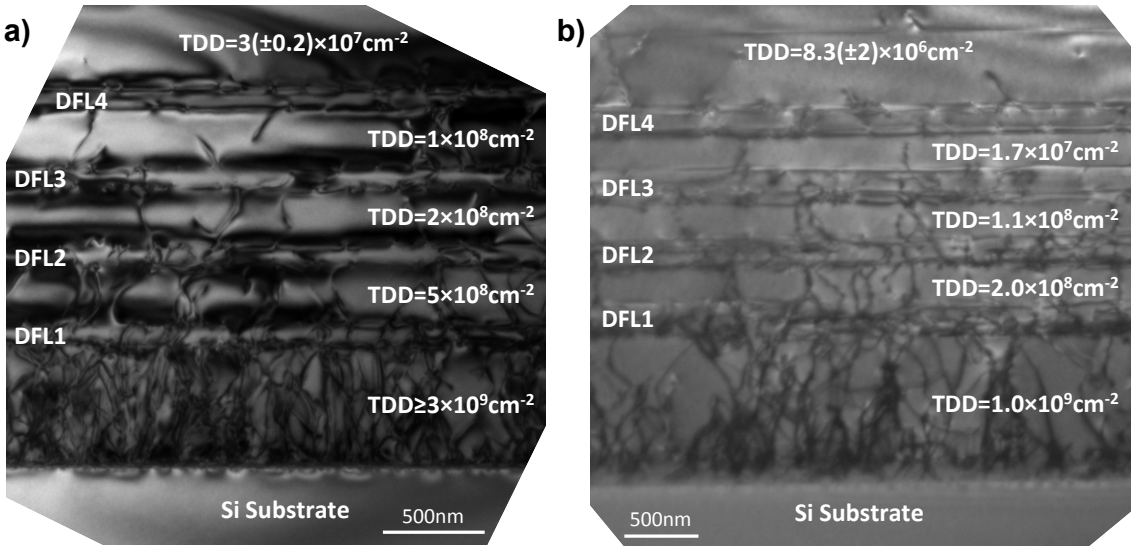

FIGURE 5.12. *Transmission Electron Microscopy (TEM) images of the buffer and Dislocation Filter Layers (DFLs) of the $Al_{0.2}Ga_{0.8}As$ (a) and GaAs (b) samples grown on Si.*

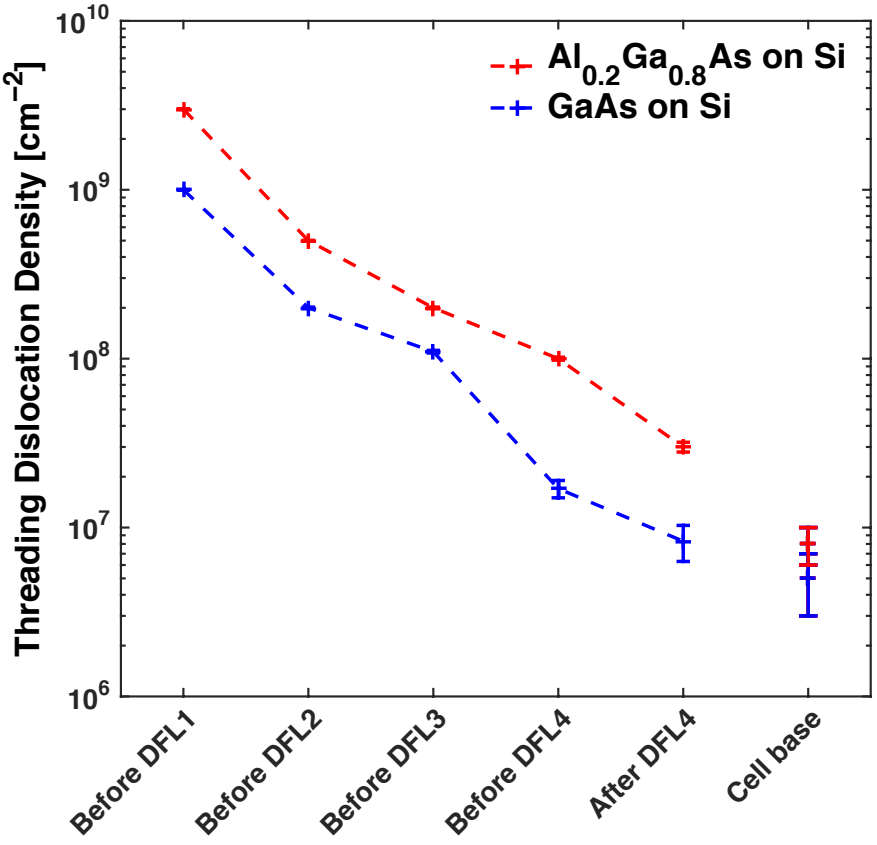

FIGURE 5.13. *Evolution of the TDD in the samples grown lattice-mismatched on Si.*

b) 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells

J-V characteristics, acquired under illumination, of the best devices from both 1.7 eV $Al_{0.2}Ga_{0.8}As$ samples are presented in FIGURE 5.14 (solid lines). The pseudo-J-V curves, extracted from Suns-V_{oc} measurements, are also displayed in dashed lines.

As expected, the impact of the TDD on the performance of the devices is apparent, with a 161 mV reduction in V_{oc} from the sample grown lattice-matched on GaAs to the sample grown lattice-mismatched on Si. This is in agreement with the presence of TDs shown by TEM, leading to a stronger non-radiative recombination rate and a reduced minority carrier lifetime. Ideality factors, extracted from Suns-V_{oc} measurements, also indicate a stronger non-radiative recombination rate on Si, with an increase of the 1-sun ideality factor from n=2.02 on GaAs to n=2.19 on Si.

Again, the V_{oc} values measured are low considering the high bandgap of the material (≈1.7 eV), even for the reference sample grown lattice-matched on GaAs. The

bandgap-voltage offset W_{oc}, thus, deviates notably from the semi-empirical value of 0.3-0.4 V expected from high material quality devices. The ideality factors – higher than 2 for both devices, indicating non-radiative recombination in the depletion zone as the dominant recombination pathway – confirm this relatively poor material quality. The performance of our devices, in particular the V_{oc}, is consequently primarily limited by the bulk material quality of the grown $Al_{0.2}Ga_{0.8}As$, independent of the presence of TDs.

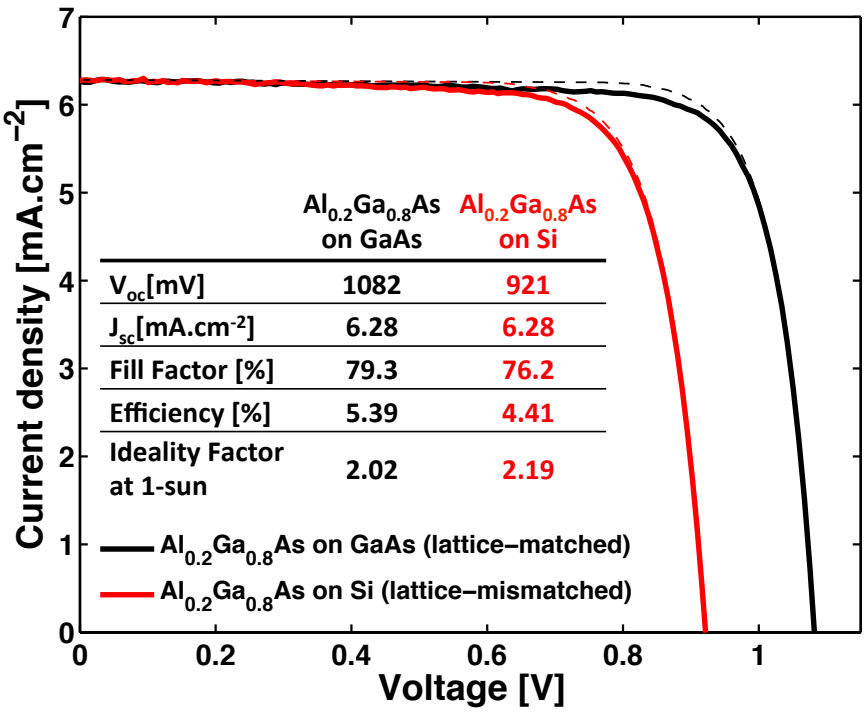

FIGURE 5.14. *J-V characteristics, acquired under illumination, (solid lines) and pseudo-J-V curves, extracted from Suns-V_{oc} measurements, (dashed lines) of the best $Al_{0.2}Ga_{0.8}As$ devices grown on GaAs (black) and on Si (red). The presence of TDs reduces the V_{oc} but not the J_{sc}.*

Both devices present very close J_{sc} values, indicative of a limited impact of the TDs on the carrier collection efficiency. This is confirmed by the similar EQE curves presented in FIGURE 5.15. The bulk $Al_{0.2}Ga_{0.8}As$ material quality, thus, appears to be the limiting factor in the diffusion length of minority carriers in the base of the solar cells, a higher TDD being needed to impact the collection efficiency of the devices and, thus, their J_{sc} and EQE.

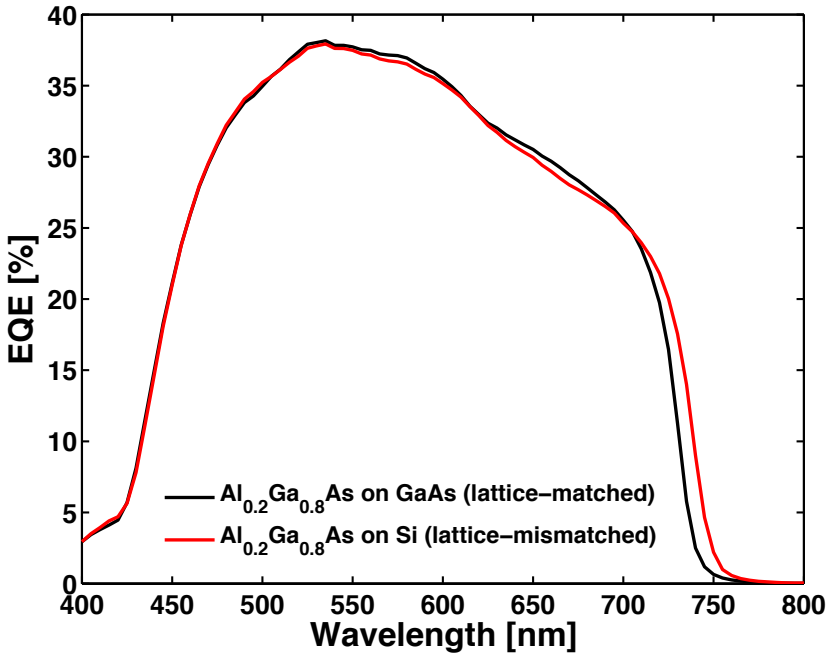

FIGURE 5.15. *External Quantum Efficiency (EQE) measurements of the best devices from the $Al_{0.2}Ga_{0.8}As$ samples grown on GaAs (black) and on Si (red).*

c) 1.42 eV GaAs solar cells

The J-V characteristics, acquired under illumination, (solid lines) and pseudo-J-V curves, extracted from Suns-V_{oc} measurements, (dashed lines) of the best 1.42 eV GaAs devices grown on both substrates are displayed in FIGURE 5.16. Similar to the $Al_{0.2}Ga_{0.8}As$ samples presented above, the impact of the presence of TDs is apparent with a comparable reduction in V_{oc} (151 mV) between the samples grown lattice-matched on GaAs and lattice-mismatched on Si. The 1-sun ideality factors n of the cells also illustrate the impact of TDs, with an increase from n=1.36 on GaAs – characteristic of a balance between recombination pathways – to n=2.02 on Si – characteristic of recombination dominated by SRH recombination in the depletion zone.

The lower ideality factor for the sample grown lattice-matched on GaAs, compared with the $Al_{0.2}Ga_{0.8}As$ sample grown on GaAs, indicates a better bulk material quality. This is confirmed by the lower W_{oc} value: 469 mV for the best lattice-matched GaAs device versus 618 mV for the best lattice-matched $Al_{0.2}Ga_{0.8}As$ device.

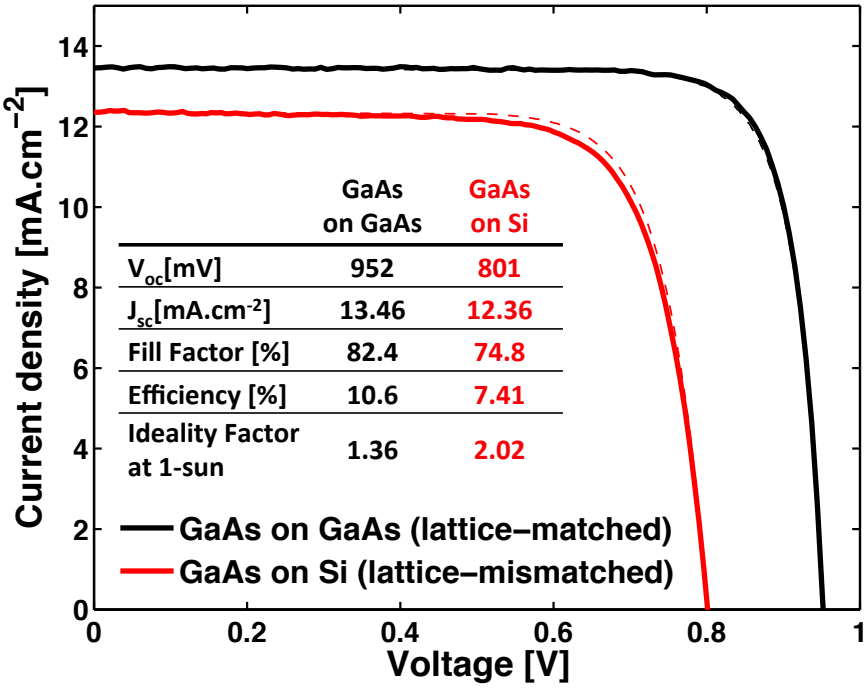

FIGURE 5.16. *J-V characteristics, acquired under illumination, (solid lines) and pseudo-J-V curves, extracted from Suns-V_{oc} measurements, (dashed lines) of the best GaAs devices grown on GaAs (black) and on Si (red). The presence of TDs reduces the V_{oc} and the J_{sc}.*

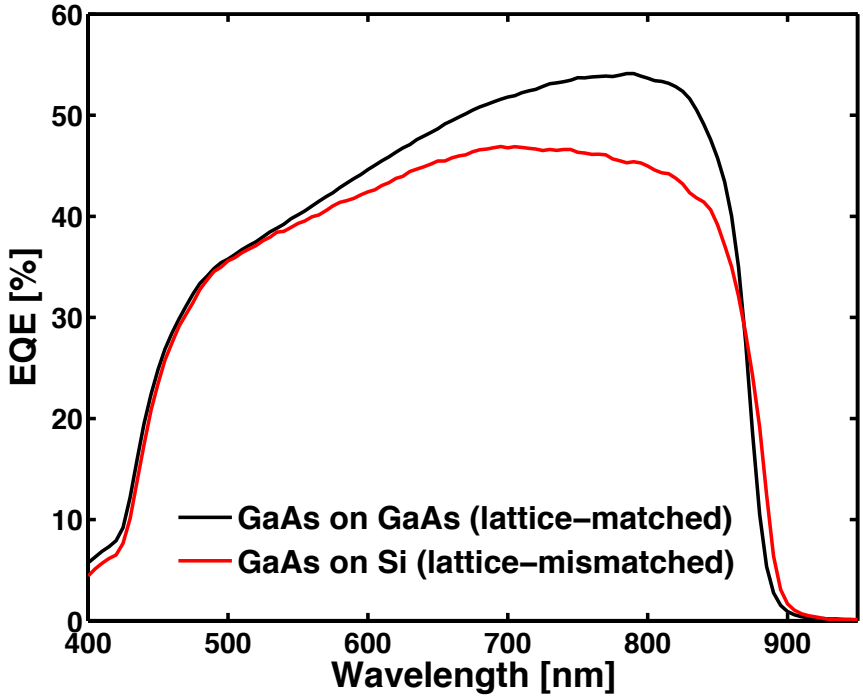

FIGURE 5.17. *External Quantum Efficiency (EQE) measurements of the best devices from the two GaAs samples grown on GaAs (black) and on Si (red).*

Contrary to the $Al_{0.2}Ga_{0.8}As$ devices, the impact of the presence of TDs on the J_{sc} is apparent, with a J_{sc} reduction of 1.10 mA.cm^{-2} between the sample grown on GaAs and the one grown on Si. The EQE measurements, displayed in FIGURE 5.17, confirm the lower collection efficiency for the cell grown on Si, especially at longer wavelengths. This can be directly related to a lower diffusion length of minority carriers in the presence of TDs, with a reduced carrier collection in the base of the cell, away from the depletion zone. As a result, the solar cell grown on Si exhibits a poorer EQE at longer wavelengths, absorbed at the back of the cell. As opposed to the $Al_{0.2}Ga_{0.8}As$ samples, the diffusion length is not limited by the bulk material quality and TDs directly impact the J_{sc} and the EQE in a non-negligible way.

5.4 Discussion

As shown by the comparison between $Al_{0.2}Ga_{0.8}As$ and GaAs devices, the main limitation of our 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells lies in the bulk material quality of the $Al_{0.2}Ga_{0.8}As$, for the samples grown lattice-mismatched on Si as well as for the samples grown with a negligible TDD on GaAs. This poor material quality is confirmed by the low W_{oc} values and high ideality factors measured for both $Al_{0.2}Ga_{0.8}As$ samples while this issue is not as significant for GaAs samples. Growth of high material quality $Al_{0.2}Ga_{0.8}As$ is known to be challenging, with oxygen contamination a main concern leading to a strong deterioration of device performance [5.29]. Optimisation of the $Al_{0.2}Ga_{0.8}As$ growth conditions is, thus, needed in order to improve the $Al_{0.2}Ga_{0.8}As$ material quality. Reducing the Al fraction would very probably improve the AlGaAs material quality, although a lower bandgap and, thus, a lower voltage would then be expected.

As explained earlier, for all of the samples, the best J_{sc} values measured are comparatively small in regard to the J_{sc} target value of around 20 mA.cm^{-2} required for current-matching with a future Si bottom cell. The two main causes of these low J_{sc} values have been previously detailed: reflection on the specular front surface and absorption in the top GaAs contacting layer. An improved cell design, incorporating an anti-reflection coating as well as a state-of-the-art AlInP window layer, instead of the current AlAs/GaAs superlattice window layer, would greatly reduce this parasitic

reflection. The GaAs capping and contacting layer may, thus, be selectively etched, using the AlInP window layer as an etch-stop. This would result in a drastic increase in J_{sc}, from the present 6 $mA.cm^{-2}$ to between 15 $mA.cm^{-2}$ and 18 $mA.cm^{-2}$, as calculated using OPAL 2 software [5.34]. Further improvement of the cell architecture and the growth parameters, particularly to optimise the diffusion length of minority carriers in the base, should yield current density values high enough for current-matching with a future Si bottom cell.

5.5 Conclusion

1.7 eV $Al_{0.2}Ga_{0.8}As$ photovoltaic solar cell prototypes were first grown lattice-mismatched on Si substrates by solid-source MBE. Similar reference cells were grown lattice-matched on GaAs. For the sample grown on Si, Strained Layer Superlattice (SLS) Dislocation Filter Layers (DFLs) were used to reduce the Threading Dislocation Density (TDD) from 1×10^{9} cm^{-2} at the III-V/Si interface to **$1(\pm0.2)\times10^{7}$ cm^{-2}** in the active region of the devices. This initial TDD represents one of the lowest values published for direct epitaxial growth of AlGaAs solar cells on Si substrates, in particular considering the high Al-content (20 %) and the subsequent high bandgap of the grown devices. This low TDD is an encouraging first result, showing the relevance of direct monolithic growth of AlGaAs on Si using DFLs for the development of high efficiency III-V/Si dual junction photovoltaic solar cells.

The best cells from this initial batch exhibit a V_{oc} of 964 mV on Si, compared with 1128 mV on GaAs. The presence of TDs explains this 164 mV drop in V_{oc} between the lattice-matched and lattice-mismatched growth runs. The difference of J_{sc} between the devices (7.30 $mA.cm^{-2}$ on Si, 6.73 $mA.cm^{-2}$ on GaAs) is explained by the difference of thickness between the samples, due to discrepancies in the calibration of the MBE growth rates.

Following this initial exploratory work, we investigated the reduction of the TDD associated with performing TCA steps during growth. 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells, similar to our first prototypes, were grown on Si substrates using four DFLs, along with a reference sample grown lattice-matched on GaAs. TCA steps were performed

during the growth of one of the two samples on Si, immediately after the growth of each DFL. Another sample has been grown on Si without TCA, for comparison purposes.

Without TCA, the TDD is reduced from 8×10^{9} cm^{-2} at the III-V/Si interface to $3(\pm0.2)\times10^{7}$ cm^{-2} in the active layers of the cell. For the sample grown with TCA, the TDD is reduced throughout the epilayers, from 3×10^{9} cm^{-2} in the nucleation layer to $8(\pm2)\times10^{6}$ cm^{-2} in the base of the cell. This reduction in TDD using TCA steps was expected: during each annealing sequence, the temperature ramp-up enhances the mobility of dislocations, thus increasing the probability of dislocations self-annihilating or merging in the DFLs.

PL study demonstrates the higher material quality achieved with TCA, with a stronger peak intensity measured. Similarly, a V_{oc} recovery is demonstrated using TCA, from 833 mV to 895 mV. Similar to our initial devices, high bandgap-voltage offsets W_{oc} of 630 mV, 784 mV and 840 mV have been measured on GaAs, Si with TCA and Si without TCA, respectively. It appears that the $Al_{0.2}Ga_{0.8}As$ bulk material quality, on Si as well as on GaAs, is hindering the performance of the devices

In order to confirm the origin of these poor $Al_{0.2}Ga_{0.8}As$ solar cells performance, a comparison study between $Al_{0.2}Ga_{0.8}As$ and GaAs solar cells, grown lattice-mismatched on Si and lattice-matched on GaAs, was carried out. Using similar buffer structures as the previous growth run, including SLS DFLs coupled with TCA steps, 1.7 eV $Al_{0.2}Ga_{0.8}As$ and 1.42 eV GaAs solar cells were grown on Si, as well as on GaAs as a reference. **TDDs of $8(\pm2)\times10^{6}$ cm^{-2} and $5(\pm2)\times10^{6}$ cm^{-2} were reached in the base of the $Al_{0.2}Ga_{0.8}As$ and GaAs cells grown on Si, respectively**.

In agreement with the previous studies, the presence of Threading Dislocations (TDs) directly impacts the V_{oc} of the cells for both absorber materials investigated, with a reduction in V_{oc} of about ≈150-160 mV between the reference samples grown lattice-matched on GaAs and the test samples grown lattice-mismatched on Si. However, the J_{sc} and the EQE are only impacted by the presence of TDs for the GaAs solar cells. This is due to a relatively low material quality for the $Al_{0.2}Ga_{0.8}As$ cells, leading to high W_{oc} values on both substrates and limited bulk minority carrier diffusion lengths,

independently of the presence of TDs. As a result, the carrier collection efficiency of the $Al_{0.2}Ga_{0.8}As$ is similar on Si and on GaAs substrates.

The main limitation of our 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cell prototypes, thus, lies in the bulk material quality of the $Al_{0.2}Ga_{0.8}As$, for the sample grown lattice-mismatched on Si as well as for the sample grown with a negligible TDD on GaAs. This poor material quality is further confirmed by the high ideality factors measured for both $Al_{0.2}Ga_{0.8}As$ samples while this issue is not as significant for the GaAs samples. Growth of high material quality $Al_{0.2}Ga_{0.8}As$ is known to be challenging, with oxygen contamination a main concern, potentially leading to a strong deterioration of the performance of the devices [5.29]. In order to demonstrate high efficiency – and in particular high V_{oc} – $Al_{0.2}Ga_{0.8}As$ devices grown on Si as well as on GaAs, an optimisation study of the growth conditions of $Al_{0.2}Ga_{0.8}As$, focusing on the substrate temperature, has been carried out. These results are detailed in Chapter 6.

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Chapter 6

Optimisation of 1.70 eV $Al_{0.22}Ga_{0.78}As$ solar cells growth conditions

This chapter presents our efforts to improve the bulk material quality of $Al_{0.22}Ga_{0.78}As$ solar cells grown lattice-matched on GaAs, in particular by optimising the material growth temperature. The findings of this study have been published in the *Journal of Crystal Growth* [6.1]. In the work presented hereafter, a higher degree of confidence has been achieved regarding the AlGaAs composition and bandgap, as the growth was performed nearly lattice-matched. Assuming no relaxation, the composition could, thus, be calculated from X-Ray Diffraction (XRD) with a higher level of certainty. Consequently, composition and bandgap measurements are presented in this Chapter with an additional degree of precision, with the grown material referred to as $Al_{0.22}Ga_{0.78}As$ and its bandgap calculated to be 1.70 eV.

6.1 Research background and purpose

As demonstrated in Chapter 5, the main limiting factor of our 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells monolithically grown on Si is not the presence of Threading Dislocations (TDs) but rather the bulk material quality of the $Al_{0.2}Ga_{0.8}As$ material. The main challenge regarding the epitaxial growth of $Al_xGa_{1-x}As$ lies in the substantial incorporation of contaminants – in particular oxygen [6.2] – during deposition, leading to a high density of deep level defects related to Al-O complexes [6.3-6.4], and subsequently to a reduced minority carrier diffusion length [6.5] and lifetime [6.6]. This issue has been reported for materials grown using Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) systems [6.3-6.6]. As a result, the use of $Al_xGa_{1-x}As$ in applications strongly dependent on long minority carrier lifetimes, such as photovoltaic solar cells, has been limited.

Extensive studies have been carried out in the past on high aluminium content ($x \geq 20$ %) $Al_xGa_{1-x}As$ solar cells grown by MBE [6.5,6.7-6.10] and MOCVD [6.11-6.14]. Most of these early devices exhibit poor performance, in particular a low open-circuit voltage (V_{oc}) in regard of the bandgap of the active material. Consequently, although III-V based multijunction solar cells are commercially available for space and concentrator applications, none of these high efficiency devices currently integrates an $Al_xGa_{1-x}As$ subcell; and $Ga_{0.51}In_{0.49}P$ is now the material of choice for high bandgap (1.9 eV) subcells.

$Al_xGa_{1-x}As$ photovoltaic solar cells have recently experienced a renewal of interest [6.15-6.16], due in part to the need of subcells with a bandgap between 1.4 eV and 1.9 eV for multijunction solar cells using four or more junctions [6.17]. Additionally, high efficiency 1.9-eV $Al_{0.37}Ga_{0.63}As$ could replace $Ga_{0.51}In_{0.49}P$ in current 3-junction multijunction solar cells, avoiding the high cost associated with the use of indium [6.16]. Finally, in the frame of the present PhD thesis project, 1.70-eV $Al_{0.22}Ga_{0.78}As$ presents a strong interest as a top cell absorber material in tandem dual-junction III-V/Si photovoltaic applications. Such low TDD 1.7-eV $Al_{0.2}Ga_{0.8}As$ solar cells, grown by MBE on Si substrates, have been presented in Chapter 5. However, as previously mentioned, these initial devices, all grown at a substrate temperature of

580 °C, have shown poor performance – in particular low V_{oc} values under 1150 mV – even for the reference cells grown lattice-matched on GaAs.

Growth temperature has long been established as a key parameter in order to reduce oxygen contamination, and, thus, to enhance the material quality and performance of $Al_xGa_{1-x}As$ solar cells [6.5,6.7-6.8,6.10], with the optimal temperature greatly dependent on the Al content x. In this chapter, we present and discuss recent progress in the MBE growth of 1.70-eV $Al_{0.22}Ga_{0.78}As$ solar cells on GaAs substrates. The growth temperature in particular has been optimised: five samples have been grown at 580 °C, 600 °C, 620 °C, 640 °C, and 660 °C, respectively. A clear improvement is demonstrated with increasing the growth temperature from 580-600 °C to 620 °C. Above 620 °C, the performance of the cells declines moderately. At 660 °C, the Al to Ga ratio in the cell starts to be impacted, with a lower Ga incorporation, and the bandgap of the cell is increased above the desired 1.70 eV value.

6.2 Experimental Methods

6.2.1 Samples growth

The five samples were grown in a Veeco GEN930 Solid-Source Molecular Beam Epitaxy (SSMBE). Growth temperatures were monitored using a thermocouple mounted on the back of the wafer holder and an external infrared pyrometer. All the growth temperatures reported hereafter correspond to estimate real temperatures, extrapolated from the thermocouple readings. The well-documented transition of the Reflection High Energy Electron Diffraction (RHEED) pattern at 580 °C [6.18] – characteristic of the in-situ thermal desorption of the native oxide present on the substrate prior to growth – was used to calibrate this linear extrapolation. The epilayers were doped using Si (n-type regions) and Be (p-type regions) solid sources. All growth runs have been performed on standard n-type GaAs (100) substrates.

The structure of the cells is presented in FIGURE 6.1. After in-situ desorption of the native oxide layer present on the surface of the substrate, controlled through RHEED, a 200 nm-thick n^+-GaAs ($N_d=1.4\times10^{18}$ cm^{-3}) buffer is grown, followed by a

1 µm-thick n^+-$Al_{0.22}Ga_{0.78}As$ (N_d=1.1×10^{18} cm^{-3}) contacting layer, in order to allow eventual contacting from the top after mesa etching. The cell itself consists of a 2 µm-thick n-type $Al_{0.22}Ga_{0.78}As$ base (N_d=2×10^{17} cm^{-3}), a 120 nm-thick p^+-type $Al_{0.22}Ga_{0.78}As$ (N_a=1×10^{18} cm^{-3}) emitter, and a 50 nm-thick p^+-AlAs/$Al_{0.5}Ga_{0.5}As$ (N_a=4×10^{18} cm^{-3}) superlattice window layer. The cell is capped by a highly doped 50 nm-thick p^+-GaAs (N_a=1×10^{19} cm^{-3}) contacting layer. This contacting layer also protects the underlying AlAs/$Al_{0.5}Ga_{0.5}As$ superlattice from oxidation. The structure grown does not include a Back Surface Field (BSF).

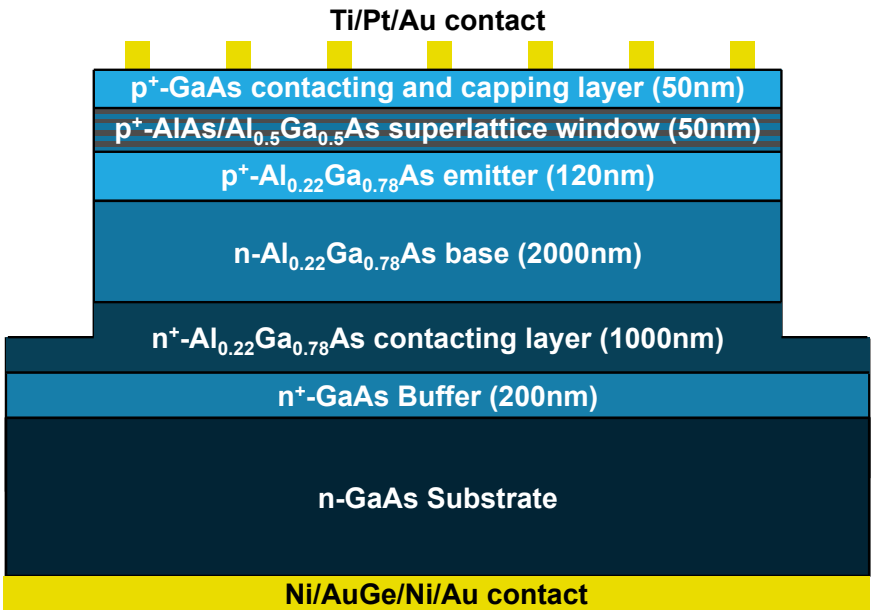

FIGURE 6.1. *Structure of the samples, grown and processed into devices.*

6.2.2 Device fabrication

Following growth, contact to the n-type region was thermally evaporated on the full back surface of the samples. A Ni/AuGe/Ni/Au (5 nm/100 nm/30 nm/200 nm) contact structure was deposited and subsequently annealed at 390 °C for 60 s. Individual devices' front grids were defined by standard photolithography techniques before sputtering of the Ti/Pt/Au (20 nm/50 nm/400 nm) contact to the p-type region. After contact lift-off, another photolithography step was performed to delimit the surface of the devices. Wet mesa etching was then carried out using a H_2SO_4:H_2O_2:H_2O (1:10:80) selective etching solution, thus electrically isolating 5 mm×5 mm and

3 mm×3 mm square devices. No anti-reflection coating was deposited. Moreover, in order to protect the underlying AlAs/$Al_{0.5}Ga_{0.5}As$ superlattice window, the top GaAs capping and contacting layer was not etched around the contacts. This leads to a non-negligible parasitic absorption in the lower bandgap (1.42 eV) 50 nm-thick GaAs contacting layer. Using a classic Beer-Lambert absorption model, the associated short-circuit current density (J_{sc}) loss has been evaluated at around 5.5 $mA.cm^{-2}$ to 6 $mA.cm^{-2}$, in addition to reflection losses.

6.2.3 Characterisation

Structural properties of the samples have been investigated using Atomic Force Microscopy (AFM) and X-Ray Diffraction (XRD). AFM imaging has been carried out at room-temperature in a Veeco Nanoscope Dimension V 3100 SPM system, in tapping mode. A Jordan Valley D1 instrument has been used for XRD measurements. Given the narrow difference in lattice parameters between GaAs and $Al_xGa_{1-x}As$, we assume no relaxation of the epilayers. The Al content x of the samples can, thus, be extracted from the XRD ω-2θ graph, by analysing the difference between the substrate intensity peak and the epilayers intensity peak.

Steady-state room-temperature photoluminescence (PL) emission spectra of the grown samples were acquired in a Nanometrics RPM2000 rapid photoluminescence mapping system, allowing direct comparison between the samples.

Current density versus voltage (J-V) characteristics under illumination, illumination intensity versus open-circuit voltage (Suns-V_{oc}) measurements and External Quantum Efficiency (EQE) measurements were acquired in order to analyse the photovoltaic and diode properties of the fabricated devices.

J-V characteristics were acquired using a Keithley 2400 sourcemeter coupled with ReRa Tracer 3.0 software. A LOT solar simulator, fitted with a filtered xenon lamp calibrated to reproduce the AM1.5G spectrum at 100 $mW.cm^{-2}$, was used for measurements under illumination. As the front grid contact to the p-type region covers a non-negligible portion of the fabricated devices (4.29 mm^2 for the 5×5 mm devices, 1.93 mm^2 for the 3×3 mm devices), the current density results presented

hereafter correspond to the designated area of the devices (20.71 mm^2 for the 5×5 mm devices, 7.07 mm^2 for the 3×3 mm devices) in order to allow meaningful comparison between devices of different size.

Suns-V_{oc} measurements were performed in a Sinton Instruments system. In order to rectify the strong spectral mismatch between the 1.70-eV $Al_{0.22}Ga_{0.78}As$ measured cell and the 1.12-eV Si cell used to determine the illumination intensity [6.19], a Schott KG3 short pass filter was placed in front of the illumination intensity monitoring cell. This reduced the difference in measured V_{oc} at 1 sun between the J-V setup and the Suns-V_{oc} system to 5 to 10 mV, depending on the spectral response of the sample. An additional spectral mismatch coefficient was consequently calculated for each individual device, in order to match the J-V and Suns-V_{oc} measurements [6.19].

Room-temperature EQE measurements were performed with a SpeQuest Quantum efficiency system from ReRa.

6.2.4 Results analysis

The bandgap of the grown material can vary from one sample to another, and even from device to device on the same wafer for high temperature growth runs. As a result, the V_{oc} of an individual cell, directly dependent on the bandgap, can be a misleading parameter to evaluate the material quality of the device. The bandgap-voltage offset W_{oc}, defined as:

$$W_{oc} = \frac{E_g}{q} - V_{oc} \tag{6.1}$$

presents the advantage of allowing comparison between samples with different bandgaps. As a result, a precise evaluation of the bandgap is needed. As presented in ref. [6.20], for direct bandgap materials, the difference between the photons energy E_{ph} and the bandgap E_g verifies:

$$\left[E_{ph} \times \ln(1 - EQE)\right]^2 \propto E_{ph} - E_g \tag{6.2}$$

The bandgap can be precisely calculated for each device, based on the device EQE, by linearly fitting the left part of Equation (2) and finding the intersection of this linear fit with the horizontal axis.

6.3 Results and discussion

6.3.1 Structural characterisation

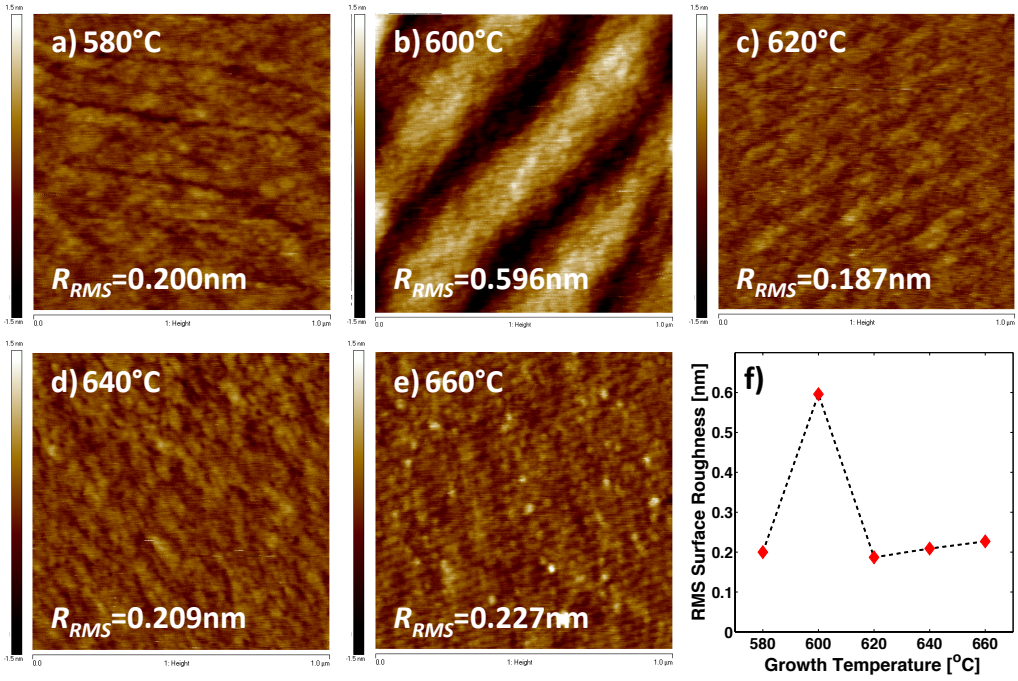

FIGURE 6.2. *Atomic Force Microscopy imaging of the samples grown at 580 °C (a), 600 °C (b), 620 °C (c), 640 °C (d), and 660 °C (e). All images show a surface of 1×1 µm with identical -1.5 nm to +1.5 nm colour bar scales. The root mean squared surface roughness as a function of the growth temperature is also displayed (f).*

AFM images of the five samples grown are displayed in FIGURE 6.2a)-6.2e), each image representing a surface of 1 µm×1 µm with a -1.5 nm to +1.5 nm scale. The root mean squared surface roughness R_{RMS} is also displayed as a function of the growth temperature in FIGURE 6.2f). All samples, except from the one grown at 600 °C, exhibit very smooth surfaces with R_{RMS} in the order of magnitude of 0.2 nm and a discernible linear repetitive pattern with a characteristic distance of approximately 20 to 40 nm. On the other hand, the sample grown at 600 °C exhibits a poor surface

morphology, with an R_{RMS} above 0.5 nm and a wider linear pattern with a characteristic distance of about 350 nm. AFM characterisation of additional samples grown at 600 °C, 620 °C, and 640 °C with an undoped emitter gave comparable results: an R_{RMS} exceeding 0.5 nm for the sample grown at 600 °C, with similar streaks, while the samples grown at 620 °C and 640 °C exhibit a smooth surface, with an R_{RMS} around 0.2 nm. The existence of a "forbidden temperature window" for the growth of high Al content (x>20 %) $Al_xGa_{1-x}As$ – with samples grown in that temperature window exhibiting a poor surface morphology – has been widely reported [6.21-6.22]. Although the exact mechanism responsible for this so-called "forbidden window" is still unclear, we believe that, in the present case, the samples grown at 600 °C are an occurrence of such a "forbidden window".

T **[°C]**	R_{RMS} **[nm]**	**ω-2θ [arcsec]**	**Al content [%]**
580	0.200	79	21.7
600	0.596	80	21.9
620	0.187	80	21.9
640	0.209	80	21.9
660	0.227	102	28.0

Table 6.1. *Root mean squared surface roughness R_{RMS} – calculated from AFM – and Al content x – extracted from XRD – of the samples grown at different temperatures T. The ω-2θ difference between the XRD intensity peaks of the GaAs substrate and the $Al_xGa_{1-x}As$ epilayers is also reported.*

The Al content of the samples, extracted from XRD, are compiled in TABLE 6.1, as well as the corresponding difference between the substrate and epilayers intensity peaks in the ω-2θ graph. The samples grown at or under 640 °C exhibit Al contents close to the 22 % expected from the Ga/Al flux ratio, calibrated through RHEED intensity fluctuation, assuming a sticking coefficient equal to one for both atomic species. The sample grown at 660 °C, however, presents a higher Al content of 28.0 %. This is caused by the re-evaporation of Ga from the growth surface above 650 °C [6.23], leading to a Ga incorporation below unity while Al adatoms are still

fully incorporated. As a result, a higher bandgap is expected for the sample grown at 660 °C.

6.3.2 Photoluminescence

A PL comparison of the samples is displayed in FIGURE 6.3. The PL measurements are taken from the centre of the wafers, where the temperature is measured by the thermocouple during growth. The four samples grown at 580 °C (magenta), 600 °C (black), 620 °C (red), and 640 °C (blue) exhibit a peak intensity wavelength between 726.6 nm and 728.7 nm, corresponding to the 1.70-eV bandgap expected from $Al_{0.22}Ga_{0.78}As$, in agreement with the Al content extracted from XRD. On the other hand, for the sample grown at 660 °C (green), the PL signal peaks at 701 nm, corresponding to a bandgap of 1.77 eV, again in agreement with the Al content of x=28 % calculated from XRD.

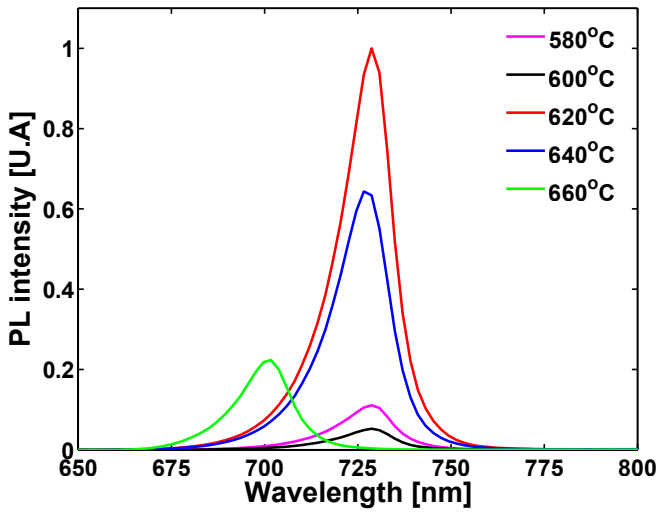

FIGURE 6.3. *Photoluminescence (PL) comparison of the samples grown at 580 °C (magenta), 600 °C (black), 620 °C (red), 640 °C (blue), and 660 °C (green). The higher material quality with a growth temperature of 620 °C is apparent. The higher bandgap with a growth temperature of 660 °C, due to the lower Ga incorporation, is also evident, as revealed by the strong blue shift of the PL peak intensity.*

It is to be noted that, in contrast with the other samples, the wafer grown at 660 °C presents a gradient of peak intensity wavelengths across its surface: from 700 nm in the centre of the wafer to 727 nm on its edge. This unusual PL distribution originates

from the use of a single-filament substrate heater, leading to a temperature gradient across the wafer, with a higher temperature in the centre of the wafer and a lower temperature on the edge, where thermal losses are stronger due to geometry. Although the growth temperature in the centre of the wafer (660 °C) is above the re-evaporation temperature of Ga (650 °C) [6.23], leading to a limited Ga incorporation, the temperature on the edges is likely under this threshold, and the sticking coefficient of Ga is close to 1. Consequently, the PL peak wavelength on the edge of the wafer is closer to the 729 nm expected from a 1.70-eV bandgap material.

Comparatively low peak intensities have been measured for the samples grown at 580 °C and 600 °C, with the sample grown at 600 °C exhibiting a lesser signal. This is in agreement with the poor surface morphology of that sample, observed by AFM. The strongest PL peak intensity is obtained at 620 °C and decreases at higher growth temperatures, indicating a superior $Al_{0.22}Ga_{0.78}As$ material quality at a growth temperature of 620 °C. This is in accordance with the lower surface roughness measured by AFM.

6.3.3 Photovoltaic properties

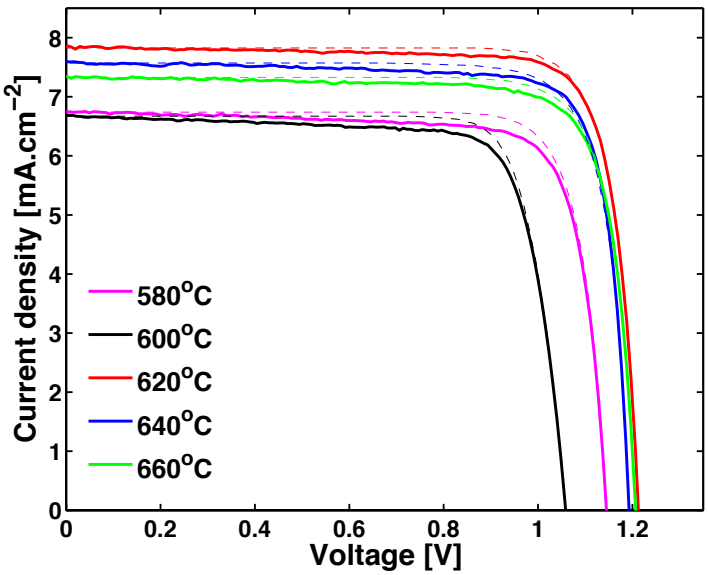

FIGURE 6.4. *Current density versus Voltage (J-V) characteristics (solid lines), acquired under illumination, and pseudo J-V characteristics (dashed lines), extracted from Suns-V_{oc} measurements, of the highest efficiency device fabricated from each sample grown.*

The current density versus voltage (J-V) characteristics, acquired under illumination, of the highest efficiency devices fabricated on each sample are displayed in FIGURE 6.4 (solid lines). No evident difference has been observed between the 3×3 mm and the 5×5 mm devices. Hereafter, they are consequently reported in an undifferentiated manner. The pseudo J-V characteristics, extracted from Suns-V_{oc} measurements, are also displayed (dashed lines). The main parameters of these best-performing cells are reported in TABLE 6.2. As expected from PL and AFM studies, the sample grown at 620 °C (red lines) exhibits the best performance, in terms of short-circuit current density (J_{sc}) as well as in terms of open-circuit voltage (V_{oc}) and efficiency. Moreover, a strong improvement in performance is achieved by increasing the growth temperature from 580-600 °C to 620 °C. The sample grown at 600 °C, presenting a poor surface morphology, exhibit a particularly low V_{oc}. Above 620 °C the performance moderately decreases, in particular due to a reduction of J_{sc}.

T **[°C]**	$\mathbf{V_{oc}}$ **[mV]**	$\mathbf{J_{sc}}$ **[mA.cm^{-2}]**	**FF [%]**	**Efficiency [%]**	**Pseudo FF [%]**	**Pseudo Efficiency [%]**
580	1145	6.75	79.3	6.12	82.0	6.34
600	1058	6.68	78.0	5.52	81.0	5.72
620	1212	7.85	81.7	7.77	82.4	7.84
640	1194	7.58	81.8	7.39	81.5	7.37
660	1207	7.34	80.5	7.12	81.9	7.25

Table 6.2. *Main parameters of the highest efficiency devices fabricated from each sample, extracted from the J-V and pseudo J-V curves presented in FIGURE 6.4.*

For each sample, 22 to 44 devices have been fabricated, depending on the size and the geometry of the portion of wafer processed. In order to better assess the trends at play and to eliminate possible inconsistencies arising from inhomogeneities during growth or fabrication, the main metrics of the highest efficiency device (red diamonds) and, for each of these considered metrics, of the 25 % best performing cells (black cross and dashed line = average value, whiskers = distribution) for each sample are displayed in FIGURE 5. The open-circuit voltages V_{oc} (a), bandgap-voltage offsets W_{oc} (b), short-circuit currents J_{sc} (c) and efficiencies (d) are reported.

In agreement with sections 6.3.1 and 6.3.2 above, the sample grown at 600 °C presents poor V_{oc}, W_{oc}, and efficiency for the best device, as well as a wide distribution of these metrics across the best performing devices. The J_{sc} is however weakly impacted, with a distribution of highest J_{sc} values measured similar to the other samples. The distribution of bandgap across the sample grown at 660 °C is also apparent, with this sample exhibiting the highest V_{oc} values measured, although the measured W_{oc} values are similar to the ones obtained at 620-640 °C. In particular, the highest efficiency device reported in FIGURE 6.4, fabricated from the extreme edge of the wafer – where the Al content and, thus, the bandgap is lower – is not amongst the 25 % highest V_{oc} values measured across the wafer, as higher bandgap devices from the centre of the wafer achieve higher V_{oc} values.

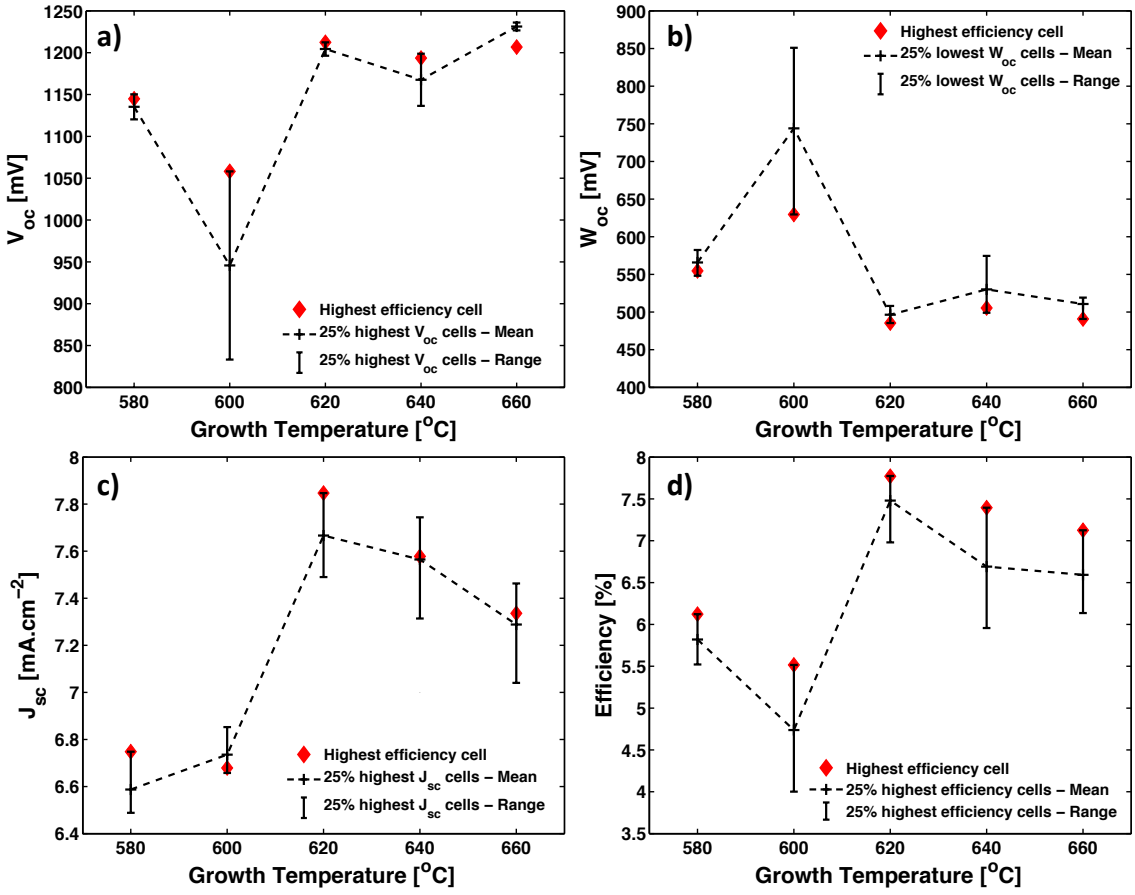

FIGURE 6.5. *Comparison of the open-circuit voltage V_{oc} (a), bandgap-voltage offset W_{oc} (b), short-circuit current J_{sc} (c) and efficiency (d) of the highest efficiency device fabricated on each sample (red diamonds) and of the 25 % best performing devices for the given metric (black cross and dashed lines = mean value, whiskers = range).*

As expected from AFM and PL measurements, the sample grown at 620 °C presents the best performance for J_{sc}, W_{oc}, and efficiency. The measured V_{oc} (1212 mV) is close to the record value of 1.22 V reported for 1.70-eV $Al_{0.22}Ga_{0.78}As$ solar cells grown by MBE [6.9]. This is especially significant given the comparatively low J_{sc} achieved in this study; due to parasitic absorption in the GaAs top capping and contacting layer (not-etched) and the lack of an anti-reflection coating. Assuming a doubling of the J_{sc} with an improved fabrication process, including etching of the GaAs capping layer and deposition of an anti-reflection coating, an expected V_{oc} of 1241 mV has been calculated from the Suns-V_{oc} measurements, as a result of the improved quasi-Fermi levels separation due to stronger light absorption.

The trend in material quality is particularly apparent from the analysis of J_{sc} values (FIGURE 6.5c), with a strong improvement from 580-600 °C to 620 °C and a moderate decrease above 620 °C. Notwithstanding the sample grown at 600 °C, this trend is confirmed by the analysis of the efficiencies of the best devices.

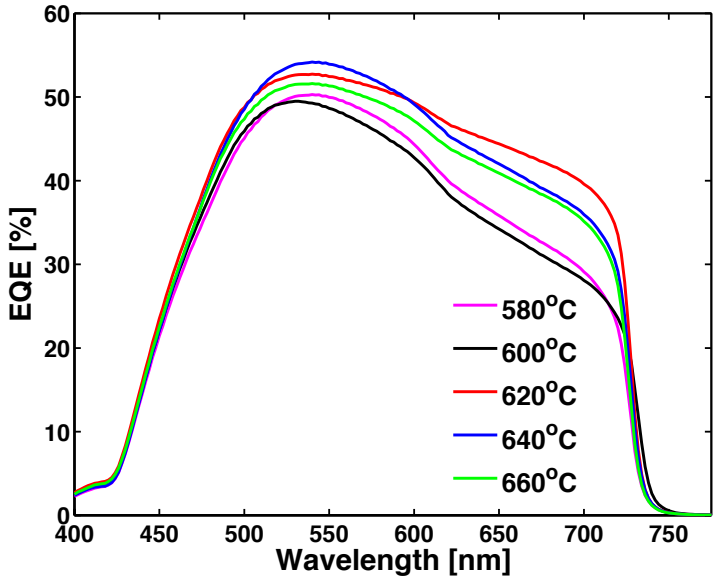

FIGURE 6.6. *External Quantum Efficiency (EQE) of the highest efficiency device fabricated from each grown sample.*

EQE measurements of the highest efficiency device from each sample are reported in FIGURE 6.6. Absolute EQEs have been calculated based on the J_{sc} measured during J-V characterisation under AM1.5G illumination. The improvement in material

quality when increasing the growth temperature from 580 °C to 620 °C is apparent, with an enhancement of the quantum efficiency – especially for lower energy photons – indicating an increase in minority carrier diffusion length. Above 620 °C, the quantum efficiency is reduced at longer wavelengths as the material quality and, thus, the minority carrier diffusion length decrease. The stronger response around 550 nm for the sample grown at 640 °C is of unknown origin and further characterisation is needed to fully understand the phenomenon at play.

The lower EQE at longer wavelengths, with a characteristic shoulder in the EQE curve close to the band-edge, is a well-known phenomenon for $Al_xGa_{1-x}As$ solar cells [6.7-6.11]. It has been demonstrated that this issue can be addressed by using Se instead of Si as the dopant for the n-type regions [6.14].

6.4 Conclusion

In order to optimise $Al_{0.22}Ga_{0.78}As$ material quality, 1.70-eV $Al_{0.22}Ga_{0.78}As$ photovoltaic solar cells have been grown by Molecular Beam Epitaxy (MBE) at 580 °C, 600 °C, 620 °C, 640 °C, and 660 °C. Analyses of the surface roughnesses and photoluminescence (PL) peak intensities show an improvement in material quality with increasing the growth temperature from 580 °C to 620 °C. Notably, the sample grown at 600 °C presents a poor surface morphology, leading to poor optoelectronic performance. The best material properties are achieved at 620 °C, with both surface roughness and PL peak intensity gradually degrading when increasing the growth temperature above 620 °C.

In contrast with the samples grown at lower temperatures, a greater Al content of 28.0 % is obtained when the growth temperature is increased to 660 °C, as demonstrated by X-Ray Diffraction (XRD) measurements. This is due to Ga re-evaporation from the growth surface above 650 °C, leading to a Ga sticking coefficient below unity while Al incorporation is not impacted. As a result, the Ga to Al ratio is reduced and the Al content is increased. Thus, the bandgap of the sample is widened, as confirmed from PL measurements.

Optoelectronic characterisation of the devices fabricated from the five grown samples confirms the trend outlined by the surface roughness and PL analyses, with a clear improvement of photovoltaic properties when increasing the growth temperature from 580-600 °C to 620 °C, and a moderate decrease beyond 620 °C. The trend is particularly apparent when analysing the highest short-circuit currents (J_{sc}) measured across each sample: contrary to the open-circuit voltage (V_{oc}) and bandgap-voltage offset (W_{oc}) – which can suffer from an eventual contamination at the p-n interface – the J_{sc} is directly linked to the minority carrier diffusion length, and hence the lifetime, throughout the epilayers. In case of a potential contamination specific to the depletion region, the J_{sc} is, therefore, a good metric to assess the bulk material quality.

Overall, the sample grown at 620 °C exhibits the best material properties and photovoltaic performance, with the lowest W_{oc} and the highest J_{sc} and efficiency measured. An open-circuit voltage of 1212 mV has been demonstrated, corresponding to a W_{oc} below 500 mV. The exact temperature, between 600 °C and 620 °C, at which the improvement in material quality occurs is not exactly known, and additional experiments in this temperature window may lead to an increase in cell performance. Further improvement could be achieved by adopting a state-of-the-art cell structure, including a GaInP Back Surface Field (BSF) and a high bandgap AlInP window layer. Selective etching of the top GaAs contacting layer and deposition of an anti-reflection coating would also strongly boost the J_{sc}, in order to achieve current-matching with an underlying Si bottom cell. Transfer of such a fully optimised $Al_{0.22}Ga_{0.78}As$ solar cell on Si substrates – using Dislocation Filter Layers (DFLs) in combination with Thermal Cycle Annealing (TCA) steps, as detailed in Chapter 5 – is expected to yield a V_{oc} in excess of 1 V and pave the way toward the achievement of high efficiency 1.70 eV $Al_{0.22}Ga_{0.78}As$ solar cells on Si suitable for dual junction III-V/Si tandem architectures.

6.5 References

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Chapter 7

Conclusions and Future Work

7.1 Summary

As presented in the introductory chapter, the objective of this PhD programme consist of the demonstration of a high material quality, high efficiency III-V solar cell epitaxially grown on a silicon substrate, with a bandgap suitable for a top subcell in a III-V/Si dual junction tandem architecture. The main challenge in growing such structures lies in the difference of lattice parameters between Si and III-V materials of interest, as there is no nitrogen-free direct-bandgap III-V material lattice-matched to Si. Consequently, a lattice-mismatched approach must be adopted. This results in an accumulation of strain in the film grown. Relaxation of the epilayers occurs through the formation of Misfit Dislocations (MDs) and Threading Dislocations (TDs). While MDs are confined to planes parallel to the growth surface, TDs propagate vertically through the epilayers to the active region of the device, where they act as recombination centres, thus greatly impeding the minority carrier lifetime. Reducing

the Threading Dislocation Density (TDD) to a minimum is, thereby, essential in order to achieve high performance minority-carrier-dominant devices, such as photovoltaic solar cells.

1.65-1.75 eV $GaAs_xP_{1-x}$ solar cells grown on Si through GaAsP/GaP/Si [7.1-7.2] or GaAsP/SiGe/Si [7.3-7.4] metamorphic pathways have so far attracted the most academic interest. Due to the limited differences in lattice parameter throughout these metamorphic buffers, the TDD is kept low within the epitaxial film. High bandgap (E_g>1.6 eV) III-V solar cells epitaxially grown on Si with TDDs below 5×10^6 cm^{-2} have been demonstrated, leading to bandgap-voltage offset ($W_{oc}=E_g/q-V_{oc}$) values under 0.55 V [7.2,7.4].

Prior to the start of the present PhD project, the team of Professor Huiyun Liu achieved early successes in the Molecular Beam Epitaxy (MBE) growth of a GaP nucleation layer on Si. Initial investigations consequently focused on the aforementioned GaAsP/GaP/Si pathway. A theoretical study of the GaAsP/Si dual junction tandem architecture was conducted, leading to the development of a model, as detailed in Chapter 4. This model is an extension of the Shockley-Queisser detailed balance limit model [7.5], considering band-to-band radiative recombination as the ultimate thermodynamic limit on the efficiency of the subcells [7.6-7.7]. Radiative recombination rates have been calculated from Würfel's blackbody theory applied to semiconductors [7.8]. This approach allows for the calculation of the theoretical maximal efficiency of a dual junction tandem architecture using the absorption spectra of the subcells' materials as the main input, thus reducing the number of material parameters required. Flat and Lambertian front surface geometries, as well as Luminescent Coupling (LC) between the cells, have been implemented. The impact of Shockley-Read-Hall (SRH) recombination on TDs has been taken into account using the NTT model [7.9], thus giving insight into the impact of the TDD on the overall efficiency of the dual junction device. The GaAsP/Si architecture simulated is, thus, similar to prototypes developed, with some recent successes, at Ohio State University [7.1] and Yale University [7.2].

The main outcome of this theoretical study on GaAsP solar cells grown on Si using a GaAsP metamorphic buffer is that a TDD below 10^5 cm^{-2} should be targeted in order

to achieve very high efficiency devices. When taking into account additional realistic sources of inefficiencies, such as a non-ideal EQE and surface recombination, efficiencies over 35 % can be achieved with a TDD under 10^5 cm^{-2}. The efficiency of the devices decreases rapidly with increasing the TDD, with maximal efficiencies falling under 30 % with a TDD over 10^7 cm^{-2}. Another significant result exhibited is the impact of TDs on LC between cells. Without TDs, radiative recombination is dominant in the III-V top cell, leading in some cases to an appreciable boost to the Si bottom cell current density. However, even with a TDD as low as 10^5 cm^{-2}, non-radiative SRH recombination on TDs takes over radiative recombination and LC is quenched. As a result, the flexibility in the design and operations of the devices gained from LC starts to be impacted with a TDD over 10^4 cm^{-2} and is totally lost once the TDD reaches 10^6 cm^{-2}. Even with a TDD around 10^5 cm^{-2}, GaAsP/Si tandem dual junction solar cells will be noticeably sensitive to deviations from the AM1.5G spectrum. Additionally, the approach we used in our modelling work is fairly flexible and can easily be adapted to other material systems and device architectures.

In the early months of this PhD programme, the use of GaAsP metamorphic buffers on a GaP nucleation layer, similar to the work carried out at Ohio State University [7.1] and Yale [7.2], was considered. Early attempts to grow GaP on Si by MBE – prior to the start of the project – were encouraging. However, replication of these initial results proved more challenging than expected, as growth of GaP on Si is extremely sensitive to the background conditions inside the growth chamber and to the quality of the Si substrate. This research pathway has, thus, been put on hold until appropriate growth conditions could be reached. In parallel, the team of Professor Huiyun Liu achieved promising results for the MBE growth of III-V lasers on Si using direct nucleation of AlGaAs on an Si substrate, followed by the deposition of Strained Layer Superlattice (SLS) Dislocation Filter Layers (DFLs), in order to reduce the TDD in the active layers of the devices [7.10]. Transfer of this growth technique to 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells grown on Si has, hence, been the focus of most of the experimental work carried out during this PhD project.

As presented in Chapter 5, initial 1.7 eV $Al_{0.2}Ga_{0.8}As$ on Si solar cell prototypes have been grown. Following the deposition of the AlGaAs nucleation layer, an AlAs/GaAs

superlattice has been used in order to reduce the growth surface roughness and to achieve a smooth interface. Five InAlAs/AlGaAs SLS DFLs have then been grown, followed by the active layers of the devices. Similar 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells have been grown on lattice-matched GaAs substrates for comparison purposes. The SLS DFLs contributed to a sizable reduction of the TDD from 10^9 cm^{-2} at the III-V/Si interface to $1(\pm0.2)\times10^7$ cm^{-2} in the active regions of the sample. This TDD was, at the time, the lowest one achieved for such high Al content (20 %) AlGaAs solar cells grown on Si. In particular, a narrow difference of V_{oc} (164 mV) has been measured between the best devices fabricated from the reference sample grown lattice-matched on GaAs and the test sample grown lattice-mismatched on Si.

Further reduction of the TDD has been demonstrated using Thermal Cycle Annealing (TCA) steps in combination with DFLs. TCA steps – consisting of a relatively rapid ramp up of the temperature followed by a similar ramp down – improve the mobility of TDs within the epilayers, thus increasing the probability of conjugated TDs and/or MDs to merge or self-annihilate [7.11]. As a result, the TDD is reduced throughout the grown structure. Using only four DFLs this time, a TDD of $8(\pm2)\times10^6$ cm^{-2} has been demonstrated in the active region of the devices grown using TCA, thus improving on our prior record. This compares with $3(\pm0.2)\times10^7$ cm^{-2} for the control sample grown with DFLs but without TCA.

Although low TDDs have been demonstrated using DFLs in combination with TCA steps, all the $Al_{0.2}Ga_{0.8}As$ solar cells fabricated exhibit relatively poor performance, in particular low V_{oc} values. These low V_{oc} values have been measured on the test samples grown lattice-mismatched on Si as well as on the reference samples grown lattice-matched on GaAs. As a result, the calculated W_{oc} values are large in comparison with the semi-empirical value of 0.3-0.4 V expected for high material quality III-V devices, even for samples grown on GaAs. These results suggest a poor material quality of the $Al_{0.2}Ga_{0.8}As$ material, independent of the presence of TDs.

A comparison study between $Al_{0.2}Ga_{0.8}As$ and GaAs solar cells – grown on both GaAs and Si substrates – has been conducted, in order to verify the hypothesis that the $Al_{0.2}Ga_{0.8}As$ material quality is the main limiting factor for the performance of the

$Al_{0.2}Ga_{0.8}As$ devices. Indeed, growth of high material quality AlGaAs is notoriously challenging – as oxygen-related defects [7.12] and doping-related DX centres [7.13] can strongly hinder the performance of AlGaAs devices – while growth of GaAs is less sensitive to growth conditions and potential contamination. Using our standard growth recipes, this comparison study has shown that the J_{sc} and External Quantum Efficiency (EQE) of $Al_{0.2}Ga_{0.8}As$ solar cells are barely impacted by the presence of TDs, whereas the J_{sc} and EQE of GaAs devices are notably reduced for the sample grown lattice-mismatched on Si. The diffusion length of minority carriers, and hence the carrier collection efficiency, is, thus, limited by the presence of TDs for the GaAs devices, while the carrier collection efficiency is limited by the bulk material quality for the $Al_{0.2}Ga_{0.8}As$ solar cells grown on GaAs as well as on Si. Additionally, the GaAs solar cells exhibit lower W_{oc} values on both substrates. In order to demonstrate high material quality 1.7 eV $Al_{0.2}Ga_{0.8}As$ solar cells on Si, optimisation of the $Al_{0.2}Ga_{0.8}As$ bulk material quality, and, thus, of the $Al_{0.2}Ga_{0.8}As$ growth recipe, was consequently required.

It has been shown that the growth conditions, particularly the substrate temperature, have a strong impact on the oxygen contamination of AlGaAs solar cells grown by MBE [7.12,7.14]. The material quality of the devices and their performance can, hence, be greatly improved by optimising the cell growth temperature. Such an optimisation study has, thus, been conducted, as detailed in Chapter 6. 1.70 eV $Al_{0.22}Ga_{0.78}As$ solar cells have been grown at 580 °C, 600 °C, 620 °C, 640 °C, and 660 °C. A strong improvement in V_{oc} and J_{sc} has been demonstrated with increasing the growth temperature from 580-600 °C to 620 °C. The sample grown at 600 °C, specifically, presents a poor surface morphology, leading to poor optoelectronic properties and particularly a low V_{oc}. Above 620 °C, the performance of the cells decreases moderately. Notably, a V_{oc} above 1.21 V has been demonstrated for the sample grown at 620 °C, corresponding to a W_{oc} below 0.5 V. Additionally, at 660 °C, the Al content of the cell is increased to 28 %, as the Ga sticking coefficient falls below unity with growth temperatures above 650 °C, while the Al incorporation is not noticeably impacted. Thus, the bandgap of the sample is widened, as confirmed by photoluminescence measurements.

Although we fell short of the initial objective of demonstrating a low TDD, high material quality, high efficiency III-V solar cell grown on Si by MBE, all the technological building blocks required to get there have been developed. Due to operational challenges related to the maintenance of the MBE system, the project has been somewhat delayed. Transfer of the optimised $Al_{0.22}Ga_{0.78}As$ growth recipe presented in Chapter 6 onto a Si substrate, using DFLs and TCA steps, is expected to yield devices with a V_{oc} in excess of 1 V.

7.2 Future steps

7.2.1 Integration of the improved $Al_{0.22}Ga_{0.78}As$ solar cell growth recipe on Si

As presented above, the main priority of the project is the integration of the improved $Al_{0.22}Ga_{0.78}As$ growth recipe onto a Si substrate, in order to demonstrate devices with a V_{oc} above 1 V. Additional improvement of the DFL structure, so as to achieve a TDD below 10^6 cm^{-2} – similar to what has been recently demonstrated with III-V lasers on Si [7.15] – should lead to further increasing of the cell's V_{oc}.

Replacing the current AlAs/GaAs superlattice Back Surface Field (BSF) and window layers with state-of-the-art GaInP and AlInP layers should also enhance the performance of the cells. Such a structure would allow for a selective etching of the GaAs top contacting and capping layer, thus reducing the optical losses caused by parasitic absorption in that top layer. With the addition of an Anti-Reflection Coating (ARC), J_{sc} values close to 20 $mA.cm^{-2}$, suitable for current matching with a future Si bottom cell, should be feasible.

Such an achievement would be ground-breaking: on top of enabling the growth of low TDD III-V devices on Si, the approach we have detailed in this thesis presents the advantage of a relatively thin buffer compared with the metamorphic pathways previously mentioned. As a result, lower growth times and material consumption can be expected.

7.2.2 Growth on Chemically Polished (CP) Si wafers

One important limitation for the widespread development and deployment of epitaxially grown III-V/Si tandem architectures lies in the use of Chemically-Mechanically Polished (CMP) Si wafers [7.16] as growth substrates. Although these wafers are commonly used in the microchip industry, the CMP process in itself is too expensive for solar cell manufacturing. As a result, using CMP wafers is an important bottleneck and an alternative wafer preparation process prior to growth is required.

The team of Professor Zachary Holman at Arizona State University (ASU) has recently developed a fully chemical process in order to planarise as-cut Si wafers [7.17]. A collaboration with ASU has been initiated, in order to investigate the growth of III-V materials on these Chemically Polished (CP) wafers. Exact (100) Si substrates, as well as (100) wafers offcut 5 ° toward the [110] plane, have been prepared at ASU and sent to UCL for MBE growth. Initial results are encouraging, with the demonstration of an APD-free surface after less than 1 µm of material deposited. Surface roughness, however, is still relatively high and further work is needed in order to achieve a buffer on which growth of devices could be attempted.

7.2.3 Development of MBE-compatible high efficiency Si bottom cells

Another potential bottleneck in the development of high efficiency epitaxially grown III-V/Si dual junction tandem architectures resides in the demonstration of MBE-compatible high efficiency Si bottom subcells. Indeed, as described in Chapter 3, a high-temperature (>900 °C) surface annealing step of the Si substrate is required prior to deposition of the nucleation layer, in order to remove the oxide layer present on the growth surface. This high temperature step also ensures the reorganisation of the growth surface in 2-step terraces, needed to avoid the formation of APDs [7.18]. It has been shown that such a high temperature treatment of Si wafers, in MBE as well as in MOCVD systems, can greatly degrade the minority carrier lifetime of the Si material [7.19-7.20]. Although some mitigation techniques have been investigated [7.21], this issue needs to be addressed in order to make the full integration of an $Al_{0.2}Ga_{0.8}As$/Si tandem junction structure possible.

As mentioned in Chapter 4, the front surface passivation of the Si bottom subcell is also a potential challenge, as the passivation ability of the III-V/Si interface is unknown and may be poor. Moreover, using direct AlGaAs nucleation on Si, a high TDD is obtained at the III-V/Si interface. The impact of such a highly defected interface on the properties and performance of the Si bottom subcell is unknown. This would especially be an issue in the case of bottom subcells consisting of p-AlGaAs/n-Si or n-AlGaAs/p-Si heterojunction structures, using high Al content AlGaAs as a wide bandgap emitter and window. Similar GaP/Si heterojunction cells have been recently studied, with mixed results [7.22-7.23].

7.2.4 Full integration of an $Al_{0.22}Ga_{0.78}As$/Si dual junction tandem structure

Once both a high-efficiency low-TDD 1.7 eV $Al_{0.22}Ga_{0.78}As$ solar cell grown on Si and an MBE-compatible Si bottom cell are developed, demonstration of the full integration of these technological building blocks in a III-V/Si dual junction tandem solar cell will still be needed. The growth of a high-performance low-resistivity tunnel junction is a possible roadblock. Indeed, tunnel junctions are relatively low-dimensional structures and, as a result, need to be grown on a fairly smooth surface. Growth of such a structure just following the AlGaAs nucleation layer would be challenging, as the growth front is wavy at that point. Growth later on, after deposition of the AlAs/GaAs smoothing superlattice, appears more appropriate. Possible interaction between TDs and a future tunnel junction is also a potential bottleneck. Finally, the impact of the presence of TDs on the conductivity of the DFL buffer is unknown. All of these elements are, thus, potential subjects of study for researchers wanting to pursue the epitaxial pathway investigated in this thesis.

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Appendix: MATLAB® code of the GaAsP/Si dual junction model

```
%GaAsP top cell
%1 = Jph top cell
%2 = Voc top cell
%3 = Jmpp top cell
%4 = Vmpp top cell
%5 = FF top cell
%6 = eff top cell

%Si Bottom cell
%7 = Jph bottom cell
%8 = Voc bottom cell
%9 = Jmpp bottom cell
%10 = Vmpp bottom cell
%11 = FF bottom cell
%12 = eff bottom cell

%Dual junction cell
%13 = Jph dual junction cell
%14 = Voc dual junction cell
%15 = Jmpp dual junction cell
%16 = Vmpp dual junction cell
%17 = FF dual junction cell
%18 = eff dual junction cell

%19 = LC photocurrent


%AM=2 --> AM0
%AM=3 --> AM1.5 global
%AM=4 --> AM1.5 direct + circumsolar
AM=3;

%Physical constants
h=4.136*10^(-15); %eV.s
c=2.998*10^17; %nm.s^-1
q=1.602*10^-19; %C
kB=1.380*10^-23; %J.K^-1
T=300; %K
epsilon0=8.85418*10^-12;%F/c
```

```
numberStepsAsRatio=1;
numberStepsCellThickness=1;
numberStepsTDD=1;
AsRatioVector=zeros(numberStepsAsRatio,1);
TDDVector=zeros(numberStepsTDD,1);
EgGaAsPVector=zeros(numberStepsAsRatio,1);
output3D=zeros(numberStepsTDD,numberStepsAsRatio,19);

for m=1:numberStepsAsRatio;
    for n=1:numberStepsTDD;

        %GaAsP top cell parameters
        AsRatio=0.55+(0.45/(numberStepsAsRatio))*(m-1); %0.55<AsRatio<1
        AsRatioVector(m,1)=AsRatio;
        TDD=10^((n-1)/10); %cm^-2
        TDDVector(n,1)=TDD;

        EgGaAsP=1.42*AsRatio+2.78*(1-AsRatio)-0.19*AsRatio*(1-AsRatio); %eV
        EgGaAsPVector(m,1)=EgGaAsP;
        Nc=5.6e19*(0.08-0.039*AsRatio)^(3/2); %cm^-3
        Nv=2.9e19*(0.6-0.18*AsRatio)^(3/2); %cm^-3
        niGaAs=1.8*10^6; %cm^-3
        niGaAsP=sqrt(Nc*Nv)*exp(-q*EgGaAsP/(2*kB*T)); %cm^-3
        EQEGaAsP=1;%0.9;
        Dn=(90/300)*(130-190*AsRatio+360*AsRatio^2); %cm^2.s^-1
        Dp=5-10*AsRatio+12.5*AsRatio^2; %cm^2.s^-1
        Nd=10^17; %cm^-3
        Na=2*10^18; %cm^-3
        epsilonR=12.9;
        nref=3.5;
        thetaEsc=asin(1/nref); %rad
        beta=(pi-thetaEsc)/pi;

        %Si bottom cell parameters
        niSi=9.7*10^9; %cm^-3
        EQESi=1;%0.945;
        CAuger=1.66*10^(-30); %cm^6.s^-1
        JsSi=0;%5*10^-10; %A.m^-2
        cellThicknessSi=150000;%nm

        %Calculation of depletion zone in GaAsP top cell
        psi0=(kB*T/q)*log((Na*Nd)/(niGaAsP*niGaAsP)); %V
        Wdzbase=0.1*sqrt((2*epsilon0*epsilonR/q)*psi0*(Na/Nd)*(1/(Na+Nd))); %cm depletion region in the base
        Wdzemitter=0.1*sqrt((2*epsilon0*epsilonR/q)*psi0*(Nd/Na)*(1/(Na+Nd))); %cm depletion region in the emitter
        Wd=Wdzbase+Wdzemitter; %cm depletion zone width
```

```
        %Wd=0.1*sqrt((2*epsilon0*epsilonR/q)*psi0*((1/Na)+(1/Nd))); %cm

        cellThicknessGaAsP=zeros(numberStepsCellThickness,1);
        output=zeros(numberStepsCellThickness,19);
        syms x;
        syms y;

        %Reads AM1.5 irradiance data (280-1450nm, 0.5nm steps) from American
        %Society for Testing and Materials (ASTM) Terrestrial Reference Spectra
        %for Photovoltaic Performance Evaluation
        irradiance = csvread('/Users/uceealo/Documents/PhD/Models/MatLab/Data/AM1.5/ASTMG173_usuable.csv'); %[lambda]=nm, [irradiance]=W.m^-
2.nm^-1

        %Reads GaAsP absorption spectrum extrapolated data (280nm-1450nm) from
        %SOPRA &amp;amp; D.E. Aspnes and A.A Studna, 'Dielectric functions and optical
        %parameters of Si, Ge, GaP, GaAs, GaSb, InP, InAs, and InSb from 1.5 to
        %6.0 eV', Physical Review B 27(2), pp. 985?1009, 1983
        numberFileAlphaGaAsP = sprintf('%g',round(2*h*c*((1/1.42)-(1/EgGaAsP))));
        alphaGaAsP = csvread(strcat('/Users/uceealo/Documents/PhD/Models/MatLab/Data/III-V/Shifted/GaAsTer',numberFileAlphaGaAsP,'.csv'));
%[lambda]=nm, [alpha]=nm^-1

        % reads Si absorption spectrum data (280-1450nm, 0.5nm steps) from Green,
        % M.A. and Keevers, M. "Optical properties of intrinsic silicon at 300 K
        % ", Progress in Photovoltaics, p.189-92, vol.3, no.3; (1995)
        alphaSi = csvread('/Users/uceealo/Documents/PhD/Models/MatLab/Data/Si/Si.csv'); %[lambda]=nm, [alpha]=nm^-1

        for l=1:numberStepsCellThickness;
            cellThicknessGaAsP(l,1)=l*(2000/numberStepsCellThickness); %nm

            %Calculation of absorptivities and generation rates
            absorptivityFrontGaAsP = zeros(2341,1);
            absorptivityFrontGaAsPEffective = zeros(2341,1);
            absorptivityBackGaAsP = zeros(2341,1);
            absorptivitySi = zeros(2341,1);
            generationRateGaAsP = zeros(2341,1);
            generationRateSi = zeros(2341,1);

            for i = 1:2341

                %{
                %Flat surface ==> TexturingOff
                absorptivityFrontGaAsP(i,1)=EQEGaAsP*(1-exp(-alphaGaAsP(i,2)*cellThicknessGaAsP(l,1)));
                absorptivityBackGaAsP(i,1)=2*nref^2*(integral(@(x) (1-exp(-
alphaGaAsP(i,2)*cellThicknessGaAsP(l,1)./cos(x))).*cos(x).*sin(x),0,asin(1/nref))+integral(@(x) (1-exp(-
2*alphaGaAsP(i,2)*cellThicknessGaAsP(l,1)./cos(x))).*cos(x).*sin(x),asin(1/nref),pi/2));
                absorptivitySi(i,1)=EQESi*(1-exp(-2*alphaSi(i,2)*cellThicknessSi));
```

```
                %}


                %Textured surface ==> TexturingOn
                absorptivityFrontGaAsP(i,1)=EQEGaAsP*2*integral(@(x) (1-exp(-
alphaGaAsP(i,2)*cellThicknessGaAsP(1,1)./cos(x))).*cos(x).*sin(x),0,pi/2);
                absorptivityBackGaAsP(i,1)=2*nref^2*((2*thetaEsc/pi)*(0.5-integral(@(x) (exp(-
alphaGaAsP(i,2)*cellThicknessGaAsP(1,1)./cos(x))).*cos(x).*sin(x),0,pi/2))+((pi-2*thetaEsc)/pi)*(0.5-integral(@(y)exp(-
alphaGaAsP(i,2)*cellThicknessGaAsP(1,1)./cos(y)).*cos(y),0,pi/2)*(integral(@(x) (exp(-
alphaGaAsP(i,2)*cellThicknessGaAsP(1,1)./cos(x))).*cos(x).*sin(x),0,pi/2))));
                absorptivitySi(i,1)=EQESi*4*nref^2*alphaSi(i,2)*cellThicknessSi./(1+4*nref^2*alphaSi(i,2)*cellThicknessSi);

                generationRateGaAsP(i,1) = (irradiance(i,AM)*irradiance(i,1)/(h*c*q))*absorptivityFrontGaAsP(i,1)*0.5;%m^-2.s^-1
                generationRateSi(i,1)= (irradiance(i,AM)*irradiance(i,1)/(h*c*q))*(1-absorptivityFrontGaAsP(i,1))*absorptivitySi(i,1)*0.5;%m^-
2.s^-1

                %Effective cell thickness calculation for low diffusion length
                diffusionLengthSRH=10^7*sqrt(4/(pi^3*TDD)); %nm
                if 100+10^7*Wd+diffusionLengthSRH<cellThicknessGaAsP(1,1)
                    effectiveCellThicknessGaAsP=100+10^7*Wd+diffusionLengthSRH;
                    absorptivityFrontGaAsPEffective(i,1)=EQEGaAsP*(1-exp(-alphaGaAsP(i,2)*effectiveCellThicknessGaAsP));
                    %absorptivityFrontGaAsPEffective(i,1)=EQEGaAsP*2*integral(@(x) (1-exp(-
alphaGaAsP(i,2)*effectiveCellThicknessGaAsP./cos(x))).*cos(x).*sin(x),0,pi/2);
                    generationRateGaAsP(i,1) = (irradiance(i,AM)*irradiance(i,1)/(h*c*q))*absorptivityFrontGaAsPEffective(i,1)*0.5;%m^-2.s^-1
                end

            end

            %Calculation of emission rates
            emissionRateGaAsP = zeros(2340,1);
            emissionRateSi = zeros(2340,1);
            for j = 1:2340
                emissionRateGaAsP(j,1) =
10^18*2*pi*(absorptivityFrontGaAsP(j,1)+absorptivityBackGaAsP(j,1))*(1/(alphaGaAsP(j,1)*alphaGaAsP(j,1)))*exp(-
h*c*q/(alphaGaAsP(j,1)*kB*T))*((c/alphaGaAsP(j,1))-(c/alphaGaAsP(j+1,1)));%m^-2.s^-1
                emissionRateSi(j,1) = 10^18*2*pi*absorptivitySi(j,1)*(1/(alphaSi(j,1)*alphaSi(j,1)))*exp(-
h*c*q/(alphaSi(j,1)*kB*T))*((c/alphaSi(j,1))-(c/alphaSi(j+1,1)));%m^-2.s^-1
            end

            %Calculation photocurrent top cell JphGaAsP
            GRGaAsP=sum(generationRateGaAsP);
            ERGaAsP=sum(emissionRateGaAsP);
            GRSi=sum(generationRateSi);
            ERSi=sum(emissionRateSi);
            JphGaAsP=q*GRGaAsP; %A.m^-2
```

```
            %Calculation of J-V parameters for GaAsP
            tausrh=4/(Dp*TDD*pi^3);
            Rsrh=10000*niGaAsP*Wd/(2*tausrh);
            RsrhQNR=10000*(niGaAsP*niGaAsP/tausrh)*(((-Wdzemitter+10^-5)/Na)+((2*10^-4-10^-5-Wdzbase)/Nd));
            VocIdealGaAsP=(kB*T/q)*log(GRGaAsP/ERGaAsP);
            JsGaAsP=0;%2.75*10^-17*(niGaAsP/niGaAs)^2; %A.m^-2

            expVocGaAsP=vpasolve((ERGaAsP+RsrhQNR+(JsGaAsP/q))*x^2+Rsrh*x-GRGaAsP==0,x,[0,Inf]);
            VocGaAsP=(2*kB*T/q)*log(expVocGaAsP(1,1));

            %Calculation of J-V parameters for Si
            B=CAuger*niSi^3*cellThicknessSi*10^(-3);
            VocIdealSi=(kB*T/q)*log(GRSi/sum(ERSi));

            expVocSi=vpasolve((ERSi+(JsSi/q))*x^2+B*x^3-GRSi==0,x,[0,exp(q/(2*kB*T))]);
            VocSi=(2*kB*T/q)*log(expVocSi(1,1));
            JphSi=q*(GRSi+beta*ERGaAsP);

            %Calculation of maximum power point for tandem cell
            syms z positive
            expqVmppon2kBTGaAsP = @(y) double(sum(solve(-((1+beta)*ERGaAsP+RsrhQNR+(JsGaAsP/q))*z^2-Rsrh*z+GRGaAsP-(-B*y^3-
(ERSi+(JsSi/q))*y^2+GRSi)==0,z)));
            expqVmppon2kBTSi=fminbnd(@(y) (B*y^3+(ERSi+(JsSi/q))*y^2-GRSi-
beta*(ERGaAsP)*(expqVmppon2kBTGaAsP(y))^2)*(log(y)+log(expqVmppon2kBTGaAsP(y))),0,exp(VocIdealSi*q/(2*kB*T)));
            VmppSi=(2*kB*T/q)*log(expqVmppon2kBTSi);
            VmppGaAsP=(2*kB*T/q)*log(expqVmppon2kBTGaAsP(expqVmppon2kBTSi));
            Jmpp=q*(GRGaAsP-(ERGaAsP+RsrhQNR+(JsGaAsP/q))*exp(q*VmppGaAsP/(kB*T))-Rsrh*exp(q*VmppGaAsP/(2*kB*T)));
            JmppSi=q*(GRSi+beta*ERGaAsP*exp(q*VmppGaAsP/(kB*T))-(ERSi+(JsSi/q))*exp(q*VmppSi/(kB*T))-B*exp(3*q*VmppSi/(2*kB*T)));

            ResistanceFactorSi=1;%0.97;
            ResistanceFactorGaAsP=1;%0.95;

            eff=Jmpp*(ResistanceFactorSi*VmppSi+ResistanceFactorGaAsP*VmppGaAsP)/10;

            output(l,1)=JphGaAsP;
            output(l,2)=VocGaAsP;
            output(l,3)=Jmpp;
            output(l,4)=ResistanceFactorGaAsP*VmppGaAsP;
            output(l,5)=Jmpp*ResistanceFactorGaAsP*VmppGaAsP/(JphGaAsP*VocGaAsP);
            output(l,6)=Jmpp*ResistanceFactorGaAsP*VmppGaAsP/10;

            output(l,7)=JphSi;
            output(l,8)=VocSi;
            output(l,9)=JmppSi;
            output(l,10)=ResistanceFactorSi*VmppSi;
            output(l,11)=JmppSi*ResistanceFactorSi*VmppSi/(JphSi*VocSi);
```

```
            output(l,12)=Jmpp*ResistanceFactorSi*VmppSi/10;

            output(l,13)=max(JphSi,JphGaAsP);
            output(l,14)=VocSi+VocGaAsP;
            output(l,15)=Jmpp;
            output(l,16)=ResistanceFactorSi*VmppSi+ResistanceFactorGaAsP*VmppGaAsP;
            output(l,17)=Jmpp*(ResistanceFactorSi*VmppSi+ResistanceFactorGaAsP*VmppGaAsP)/((VocSi+VocGaAsP)*max(JphSi,JphGaAsP));
            output(l,18)=Jmpp*(ResistanceFactorSi*VmppSi+ResistanceFactorGaAsP*VmppGaAsP)/10;

            output(l,19)=q*beta*ERGaAsP*exp(q*ResistanceFactorGaAsP*VmppGaAsP/(kB*T));
            output3D(n,m,:)=output(l,:);
            [n,m]
            output(l,:)

        end
    end
end
```