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Silver Sintering for Power Electronics Integration

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***Abstract*—Silver sintering is an attractive alternative to soldering in power electronics, as it offers higher electrical and thermal performance. Furthermore, sintered attaches can operate at a higher temperature.**

In this paper, we investigate the use of silver sintering for the bonding of passive components, and for the manufacturing of so-called 3D-modules. It is shown that this technique is well suited, as it makes it possible to operate at very high temperature (up to 310 °C demonstrated), and as it simplifies the assembly process (several identical sintering steps can be performed successively without problem).

I. INTRODUCTION

In the last few years, silver sintering has become a very attractive alternative to soldering in power electronics, and is now used in industrial processes [1]. Advantages of silver sintering include high thermal and electrical conductivities [2], compliance to RoHS directives, low process temperature [3] and high reliability [4].

However, the vast majority of the research activity focuses on attaching power semiconductor dies only. Among other uses of silver sintering, one could cite topside contact [5], or filling material for 3D integration [6]. In this paper, we propose to demonstrate the advantages of silver sintering for power electronics integration through two examples: in the first example, components with various packages (gate driver, passives) are mounted directly in the power module, taking advantage of the high temperature capability of silver sintering. In the second example, power dies are attached on both sides using silver sintering. As silver does not melt during the process, both sides can be attached successively without any loss of accuracy. This would not have been possible with soldering. Thanks to this solid state process, it is possible to process all the attaches simultaneously or successively [7].

II. FUNCTIONNAL INTEGRATION

In addition to the power semiconductors, some commercial power module include peripheral functions: temperature monitoring, measurement of the current, or integration of the gate driver circuits [8]. The integration of the gate drivers is especially desirable

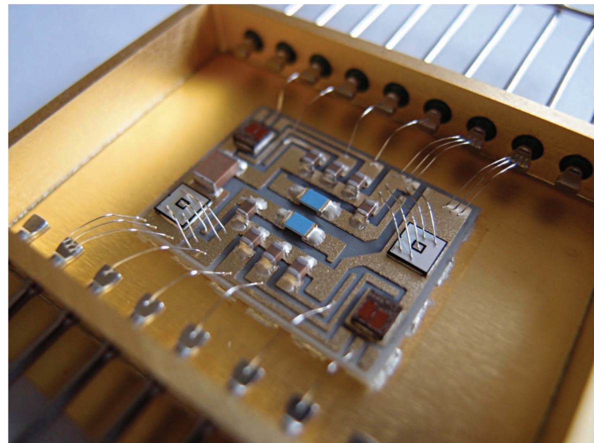

Figure 1: An inverter half bridge, comprizing two silicon-carbide JFETs, their associated gate drivers, and their associated passives (capacitors and gate resistors). All components are attached using silver sintering. The substrate is attached to the case with the same technique. Substrate dimensions are 20 mm by 30 mm.

for SiC or GaN devices to take advantage of their switching speed by reducing the impedance of the gate circuit.

The power module visible in figure 1 integrates two SiC JFETs (to form a half bridge structure), along with their respective gate driver IC, and some passives (decoupling capacitors, gate resistors, etc.). All components were attached in a single step, using a pressure-assisted silver sintering. A presentation of the circuit diagram of this power module, with a special focus on the custom-designed gate driver IC is given in [9]. This gate driver IC (as many commercial drivers) is manufactured using a Silicon-On-Insulator (SOI) technology, which reduces dramatically the leakage current of a junction compared to standard bulk silicon. Thanks to this lower leakage current level, SOI gate driver ICs can also operate at a higher temperature [10].

For fast GaN and SiC power devices, it is preferable to reduce the distance with the gate driver, to reduce the parasitic inductance. Ideally, the gate driver ICs should be located directly near to the power devices, which requires them to sustain the same temperature

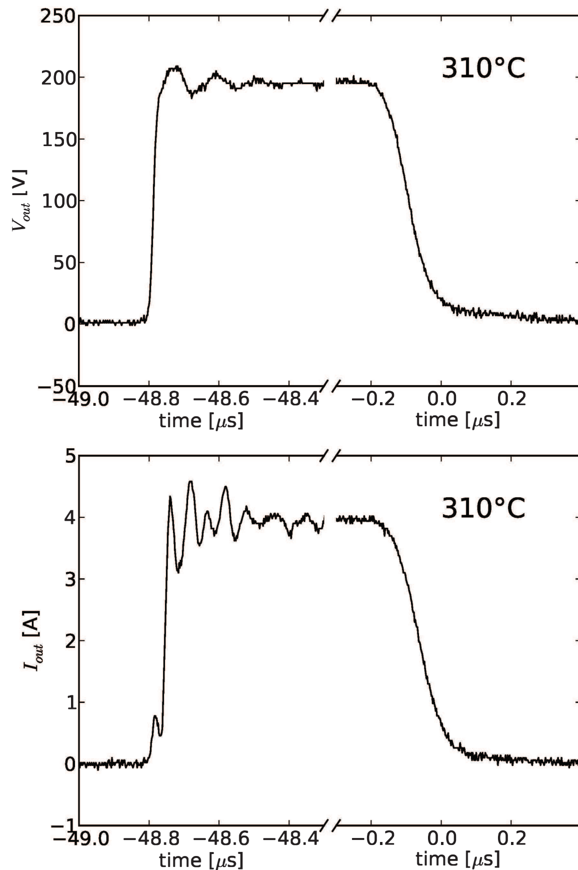

Figure 2: Switching waveforms on a 50 Ω resistive load, for 200 V DC bus measured at 310 °C ambient temperature.

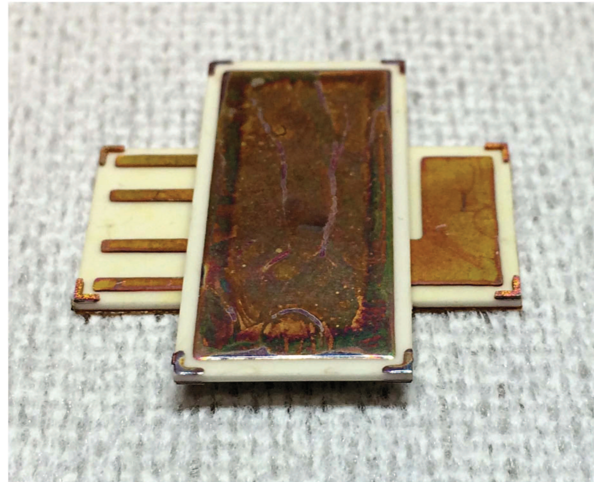

Figure 3: Photograph of the "sandwich" package: two SiC JFETs are placed between both ceramic substrates and form an inverter half bridge. The ceramic tiles are 25.4×12.7 mm^2 each.

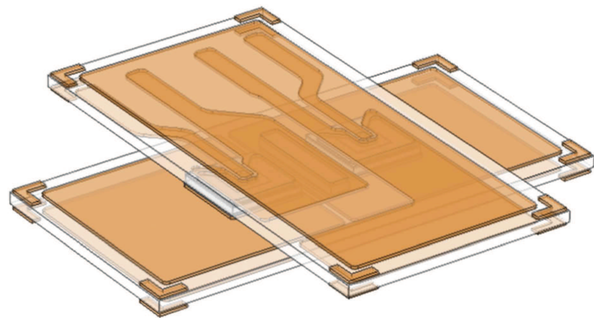

Figure 4: 3D view of the module of fig. 3 showing the internal layout and the two SiC JFET dies.

as the power devices. This is possible with SOI gate drivers, providing their packaging can also sustain the high temperature. Decoupling capacitors are also required to supply the gate driver during switching. Here, we use high-temperature-rated X7R ceramic capacitors.

A sintered-silver attach can in theory operate up to the melting point of silver (961 °C). Providing the parts to bond have a suitable metal finish (for example silver), they can be bonded using silver sintering. In the module from figure 1, all parts (gate driver, SiC JFET dies, decoupling capacitors and gate resistors) are bonded this way. They all have a silver or palladium-silver finish. To achieve better attach, some pressure ($\approx$ 1 MPa) was applied on the assembly during sintering. Because of the difference in height among the various components, a compliant silicone layer ($\approx$1 cm thick) was placed between the components and the top platen of the sintering press. This provides a quasi-isostatic pressure [2].

For testing, the half bridge from figure 1 was attached to a 50 Ω resistive load and mounted on an aluminium block equipped with a cartridge heater. The temperature was gradually increased up to 310 °C. The corresponding current and voltage waveforms at the output of the half bridge are visible in figure 2. At 315 °C, the gate drivers stopped, but they were able to resume operation after cooling-down.

III. 3D INTEGRATION

Another packaging approach is visible in figure 3. Here, only the power semiconductor dies are considered, and the objective is to provide them with an improved thermal management. Although they can operate at a temperature exceeding 300 °C, the SiC JFETs are nonetheless sensitive to thermal runaway [11], and the power they dissipate must be properly evacuated.

Dual-side cooling is an attractive solution to reduce the thermal resistance between a die and its environment. Several solutions have been presented previously [12], and they usually rely on soldering the dies on both sides to ceramic substrates. This requires two solder alloys, one to attach the dies to a first substrate, and a second alloy, with a lower melting temperature (to prevent the first alloy from re-melting), to attach this assembly to a second substrate. As a consequence, the first alloy is required to have a high melting temperature (e.g. AuGe, with a melting point of 361 °C).

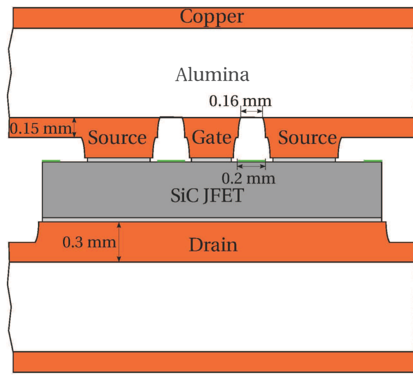

Figure 5: Zoom on the die area of the sandwich structure.

Silver sintering is an attractive replacement for soldering: as no liquid phase is involved in the sintering, and as the melting point of silver is much higher than the sintering temperature (961 °C vs. 240 °C), the first joint is not affected when performing the second. This low-temperature process can therefore be used for the entire module. Furthermore, the positioning accuracy of the die is better with silver sintering, as it cannot move during the thermal processing. With solder, the wetting forces occurring during the reflow may result in displacement of the die. This is sometimes desirable (self-alignment feature for flip-chip bonding), but in our case, we prefer to rely on proper initial alignment.

1) Assembly of the structure: The module visible in figures 3 and 4 relies on two DBC substrates with custom etching of the copper layers: this copper layer must have protruding features that match the layout of the dies, to provide an electrical contact with the pads of the die without creating short circuits. This is presented in figure 5.

We developed an etching process to achieve the high etching resolution required by the SiC JFET dies (for example 200 μm between gate and source) despite the thick layer of copper (300 μm). Indeed, such resolution is beyond the design rules of DBC manufacturers. This custom etching process is presented in figure 6: First, a blank DBC substrate is coated with a photosensitive resin (MC Dip Coating, Microchemicals). This photosensitive resin is patterned to form the protruding parts (fig. 6-1b), and the substrate is etched (fig. 6-2) using ferric chloride in a spray etcher (≈10 min). This results in a half-way etching, where about half of the copper thickness is removed in the exposed areas.

The substrate is cleaned, and coated with a new layer of photosensitive resin. This resin is patterned to form the actual tracks of the circuit (fig. 6-3b). However, it was found that this resin layer does not provide sufficient protection for the sharp edges of the protruding features, because of surface tension effects. Therefore, a layer of photosensitive dry film (Dupont Riston PM275) is laminated on top of the resin, and patterned using the same layout (fig. 6-4b). This film covers the edges properly, but is too thick to conform

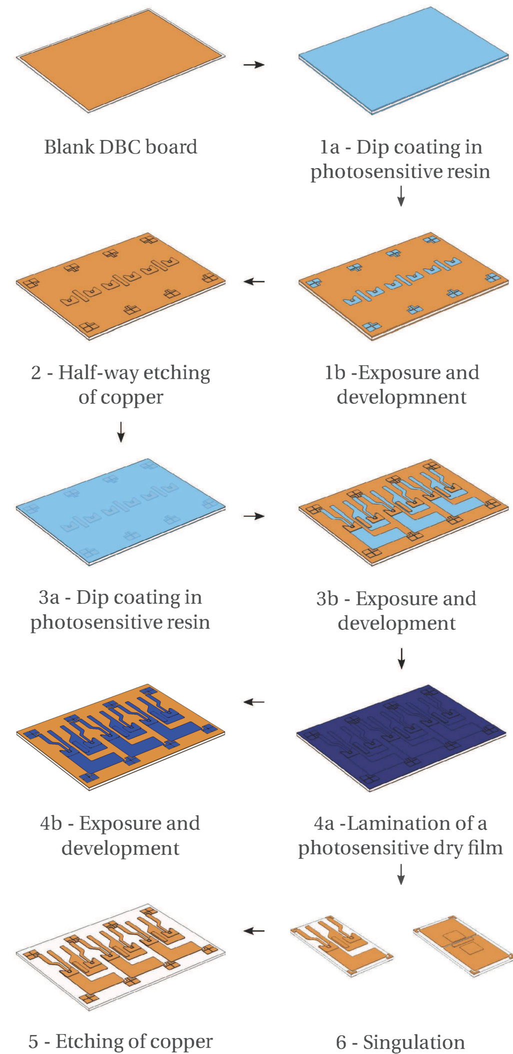

Figure 6: Process flow for the two-step etching of the DBC substrates.

to the vertical surfaces of the copper (“tenting effect”). Therefore, both photosensitive material complement each other to provide complete masking of the copper area to be protected.

The second etching process (fig. 6-5) is then performed, again using ferric chloride in a spray tank (≈10 min). The substrate is then cleaned (acetone to dissolve the photosensitive materials), and the individual tiles are singulated using a high precision saw (disco DAD 3220).

Once the DBC tiles are manufactured, the sandwich structure can be assembled. The assembly workflow is depicted in figure 7. First, some solder paste is stencil-printed on the substrate that will contact with the gate and source of the dies. The silver paste (Heraeus LTS 117 O2P2) contains silver microparticles, and is deposited using a 50 μm-thick stainless-steel stencil. The paste is then dried for 5 minutes at 85 °C. This short drying time is sufficient to make the paste much more viscous (so it will not flow once the dies are placed on top), while keeping some tackiness (so the

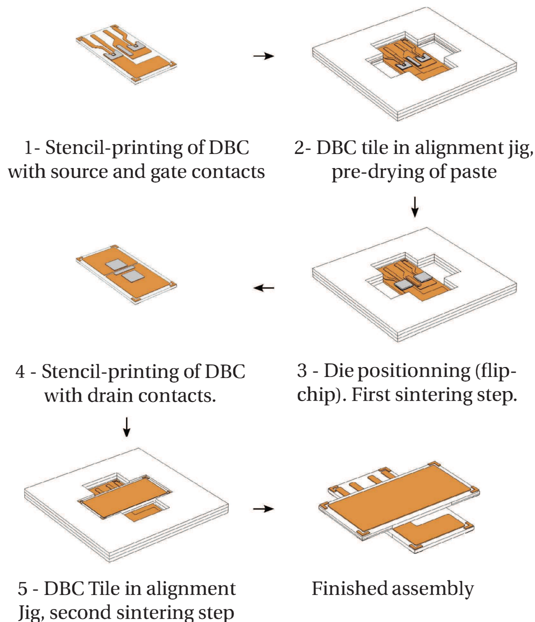

Figure 7: Process flow for the assembly of the "sandwich" module, with two sintering steps.

dies will not move once placed on the silver paste).

The dies are SiC JFETs from SiCED, on top of which a PVD Ti/Ag metallization was deposited using a metal mask, as their standard aluminium topside finish is not suitable for sintering. These dies are then placed (fig. 7-3) using a JFP Microtechnic PP-One die bonder, which has around 100 μm positioning accuracy. The populated DBC tile is placed on the platen of a custom-made sintering press, and submitted to the sintering profile: 30 min at 85 °C for complete drying, followed by a 240 °C, 30 min sintering step. During the sintering step, some pressure is applied to assist the sintering (2 MPa, corresponding to a force of 20 N approximately).

Some silver paste is then stencil-printed on the remaining DBC tile (the one with the drain contacts), dried for 5 min, and then placed on top of the first DBC tile, using an alignment jig (fig. 7-5). The assembly then undergoes a second sintering step, with the same parameters as the first one.

2) Analysis of the sandwich assembly: A cross-section of the power module is visible in figure 8. Detail views of some key areas are also provided. This cross section was obtained by encapsulating one power module in clear acrylic resin (Buehler Varikleer) and cutting it with a low speed diamond saw. The sample was then ground using P320 grit paper until the area of interest was attained. Then a polishing process was performed to achieve a satisfying surface quality (P1200 paper/9 μm, 3 μm, 1 μm diamond slurry/50 nm oxide polishing).

The leftmost detail view shows the silver layer at the top DBC/die interface. It shows some porosity, which indicates that the joint is only partially sintered. A more dense joint could be achieved by using a higher pressure or a higher sintering temperature (or a combination of both). The interface between the silver layer and the copper shows a relatively large gap (the dark area at the interface). This indicates that although the silver was deposited on the copper, it did not bond properly. This is probably related to the relatively low sintering pressure, as well as to the absence of a noble-metal finish on the DBC: direct silver sintering on copper has already been demonstrated, but was found not to be ideal [13]. DBC substrates with a silver finish might result in a better bond. A dark line is also visible between the silver layer and the die, but it is most likely an artefact due to the topside al metallization of the die: it is very regular in thickness, and follows the features of the die. A more detailed investigation would require a scanning electron microscope.

The middle detail view from figure 8 shows the space between the gate and source contacts. It can be seen that the copper layer has a very steep edges, and shows clearly the two-step etching process. The silver layers are well aligned with the copper features, with no bridging of voiding visible. A dark area can be observed on top of the die: it is the polyimide passivation that separates the gate and source pads. This shows that the alignment between the die and the copper features is satisfying.

The rightmost detail from figure 8 shows the bottom contact of the second SiC die. One can see that the die is well aligned with the copper features. The silver layer is shorter than the die ($\approx$100 μm, but this gap is negligible compared to the size of the die (4 mm on a side).

Some electrical characterizations (not shown here) demonstrate that this power module operates properly: both transistors can be turned on or off, without any noticeable change in their characteristics (leakage current, on-resistance) compared to bare dies.

Overall, the cross section in figure 8 shows that the proposed process offers sufficient alignment accuracy. It also demonstrates that the silver layer is thick enough to compensate for the surface roughness of the copper layers, or for differences in height across the module. A thin layer of silver paste (50 μm) was chosen to avoid any risk of short circuit between the contacts. As no such phenomenon was observed, a thicker layer (e.g. 100 μm) might actually be more suitable and might offer more compliance (to avoid the separation between the silver layer and the copper). A noble-metal finish covering the copper metallization should also improve the quality of the silver/copper interface.

IV. Conclusion

In this paper, we presented the application of the silver sintering technique beyond die attach. For high temperature converters, it is possible to use silver sintering to attach all the components (not only dies,

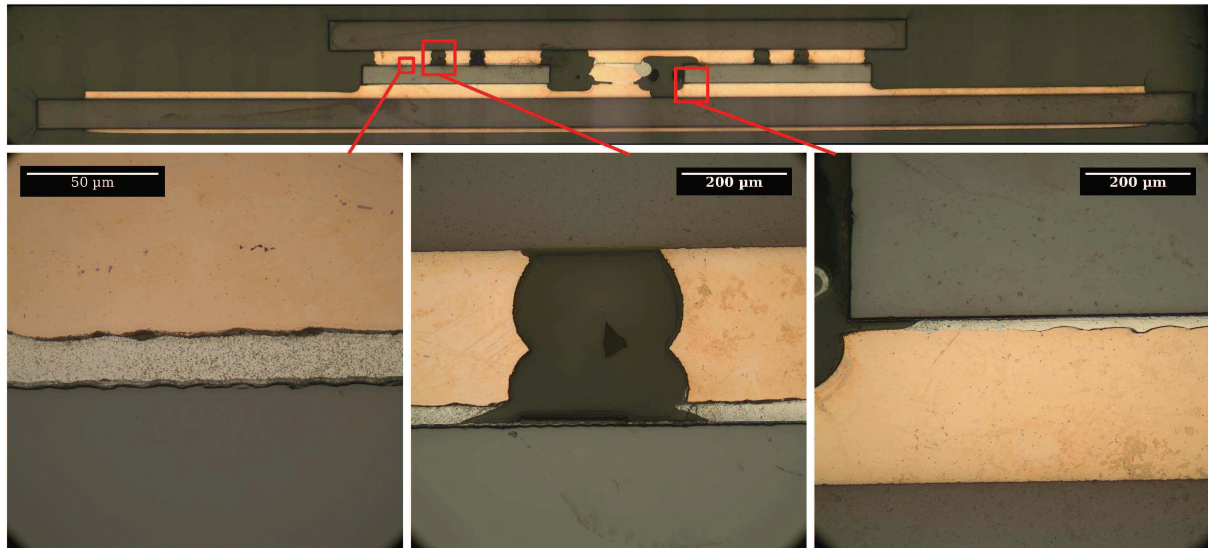

Figure 8: Top picture: cross section of the module from fig. 3. The orange layers correspond to the patterned copper. The top and bottom grey layers are alumina (12.7 mm on the side for the top tile, 25.4 mm for the bottom tile). The two lighter gray rectangles in the middle are the SiC dies (4 mm on the side). Bottom pictures, from left to right: zoom on the topside sintered silver layer, zomm on the space between gate and source contacts, and zoom on the bottomside contact.

but also SMD passives). This makes it possible to overcome the limits of soldering (in particular the low melting point of many alloys).

For 3D structures, silver sintering makes it possible to proceed to successive sintering operation without problem. When solders are used, the alloys must be carefully chosen so that successive soldering steps have decreasing melting temperature. Finally, we demonstrated a relatively simple process to manufacture "sandwich" power modules. A cross-section of this module shows that the alignment accuracy achieved is satisfying.

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