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# M-STORM Reliability model applied to DSM Technologies*

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***Abstract*—Failure mechanisms described in JEDEC publication JEP122G constitute commonly accepted models for silicon device physics of failure. Such models are generally described in term of stress parameters and/or specifically measured drift parameters; however, they consider only a single stress condition, single parameter signature and single failure mechanism at a time. When considering new disruptive technologies for deep submicron integrated circuits, the shrinkage of geometries (down and lower than the 20 nm range) induces shrinkage of electrical parameter limits and condition of use may produce multiple-stress in operation jointly producing multiple failure mechanisms concurrently. This paper is related to the generalized Reliability Model for semiconductor devices called M-STORM for Multi-phySics mulTi-stressOrs predictive Reliability Model.**

## I. INTRODUCTION

Well-known Quality Standards in various industry domains rely or are close to Military Standards MIL-STD [1] and JEDEC methods [2]. Now entering the 4.0 industry paradigm as the fourth Industrial Revolution (the Age of cyber and robots), quality/reliability models and tools headed by Health Monitoring (HM) leads toward more crucial and vital questions. When systems are constructed on innovative and disruptive technologies, such standards and methods are in general obsolete and inadequate to prepare their industrialization and qualification for just-in-time commercialization. This is the case in particular for the Deep-Sub-Micron technologies entering progressively to the More than Moore era.

*How to quantify reliability for such evolving technologies?*

When considering deep submicron (DSM) integrated circuits, the shrinkage of geometries (down and lower than the 20 nm range) induces shrinkage of electrical parameter limits and condition of use may produce multiple-stress in operation jointly producing multiple failure mechanisms concurrently. In such technology, multiple failure mechanisms can be induced simultaneously and are in competition, considering each of them described by its single activation energies defined in the Standards. Existing Quality Standards are considering stress tests and related Physics of Failure (PoF) mechanisms without entanglements. Device failure rates are seen to be a sum of each existing failure rate taken individually. Bathtub curve is an idealized view of instantaneous failure rate scenario generally considered in well-known MIL, JEDEC or TELCORDIA [3] Standards. In 2013, a generalized view of the existing reliability models was presented by E. Suhir et al. [4], [5], describing probabilistic design-for-reliability (PDfR) concepts addressing a version to predict the reliability of aerospace electronics. The Boltzmann-Arrhenius-Zhurkov (BAZ) model very similar to COX model [6], was refined for the evaluation of the Probability of Failure (ProF) under operational application at given temperature and under the various stresses (not necessarily mechanical).

More recently, a complementary set of principles was proposed by J. Bernstein et al. and focused quantifying failure rates as a combination of multiple failure mechanisms thanks to the High Temperature Overstress Lifetest (HTOL) method [7], and [8]. The key novelty of the Multiple-HTOL (M-TOL) testing method proposed is its success in separating different failure mechanisms occurring on devices in such a way that actual reliability predictions can be made for any user operating conditions defined. After a brief description of the M-STORM principles, we will see how this model can be applied to any technology and in particular considering the example of the DSM Bulk CMOS will be reviewed. Advantages and drawbacks of the approach will be highlighted then.

## II. M-STORM DESCRIPTION

### A. Multiple stressor weights

The Arrhenius equation relates reaction rate r of transition from a reactant in state A to a product in state B is depending on temperature and the activation energy as also modeled by Transition state Theory, developed by E. Wigner in 1934 [9] and by M. Evans, M. Polanyi in 1938 [10]:

$$\lambda = \lambda_0 \cdot exp\left(-\frac{E_a}{k \cdot T}\right) \quad (1)$$

where $\lambda o$ is the rate prefactor, $Ea$ the activation energy, $T$ the absolute temperature in Kelvin, k the Boltzmann's constant (8.6174 $10^{-5}$ eV/K).

The BAZ model determines the failure rate r for a material or a device experiencing combined action of an elevated temperature and external stresses S:

$$\tau = 1/\lambda = \tau_0 \cdot exp\left(\frac{E_a - \gamma \cdot S}{k \cdot T}\right) \quad (2)$$

where $S$ is the applied stress, $\tau_0$ is the time constant *and* $\lambda_0$ the failure rate constant defined as $1/\tau_0$, $\gamma$ is a factor of loading characterizing the role of the level of stress (the product $\gamma \cdot S$ is the stress per unit volume and is measured in the same units as the activation energy $E_a$.

### B. Multiple mechanism effects

Standards are generally related to parts and system hardware functions based on constant failure rate considering the element of interest have been manufactured and screened efficiently, operating in a given environment and assuming wearout failure rate well beyond the operating End of Life time (EOL). The common approach for assessing device reliability today is the High Temperature Operating Life (HTOL) testing

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[11], which is based on the assumption that just one dominant failure mechanism is acting on the device [7]. However, it is known that multiple failure mechanisms act on the device simultaneously [12]. The new approach M-TOL method predicts the reliability of electronic components by combining the Failure in Time (FIT) of multiple failure mechanisms [13]. Degradation curves are generated for the components exposed to accelerate testing at several different temperatures and core stress voltage. Data clearly reveals that different failure mechanisms act on the components in different regimes of operation causing different mechanisms to dominate. A linear matrix solution allows the failure rate of each separate mechanism to be combined linearly to calculate the actual reliability as measured in FIT of the system based on the physics of degradation at specific operating conditions.

## III. APPLICATION TO DSM TECHNOLOGIES

An experimental results of the M-TOL method tested on both 45 FPGA devices from Xilinx that were processed at TSMC (according to the Xilinx data sheets) is presented and is running at IRT Saint Exupery, Toulouse (France). The FPGAs are tested over a range of voltages, temperature and frequencies, and the test program is conducted by Bernstein, J., Ariel University, Ariel (Israel). Ring frequencies of multiple asynchronous ring oscillators simultaneously stressed in a single FPGA were read and recorded. Hundreds of oscillators and the corresponding frequency counters were burned into a single FPGA to allow monitoring of statistical information in real time. Since the frequency itself monitors the device degradation, there is no recovery effect whatsoever, giving a true measure for the effects of all the failure mechanisms measured in real time. The common intrinsic failure mechanisms affecting electronic devices are, Hot carrier Injection (HCI), Bias Temperature Instability (BTI), Electromigration (EM) and Time Dependent Dielectric Breakdown (TDDB). The failure mechanisms can be separated due to the difference of physical nature of each individual mechanism [8]. An example of results of three failure mechanisms superposed have been obtained on FPGA 45 nm and is shown in figure 1. The stresses applied degrade the reliability with respect to the temperature range domain. Quality Standards recommend in general to operate at low temperature (close to 25°C) to improve reliability. For such technology, this is no truer when the temperature range is reduced in excess down to negative values. Indeed in the classical approach, the two mechanisms BTI and EM decrease the extrapolated FIT observed at low temperature range because of the positive activation energies. Here the methodology quantify the contribution of the HCI (negative activation energy) compensating the effect of the other mechanisms and demonstrating worst FIT values at low negative temperature range for this DSM technology.

## IV. DISCUSSION AND CONCLUSION

To this day, the users of most sophisticated electronic systems that include GaN power devices, ASIC and Deep-Sub-Micron technologies etc. are expected to rely on a simple reliability value (FIT) published by the supplier. A way to predict reliability assessment based on the system environment including space, military and commercial was presented in this paper, using the common language of Failure In Time or Failure unIT (FIT). A Multi-phySics mulTi-stressOrs predictive Reliability Model (M-STORM) is discussed in this paper for an easy to use, to quantify and to predict probability of failure of new products and technologies.

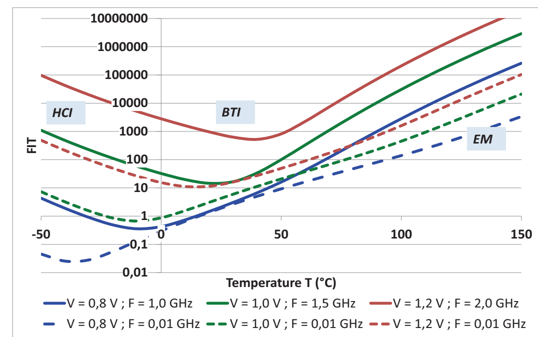


Figure 1: Reliability curves for 45nm technology showing FIT versus Temperature for Voltages above and below nominal (1.2V) and frequencies from 10 MHz (dashed line) to 2GHz (solid line).


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