



Open Archive Toulouse Archive Ouverte (OATAO)

OATAO is an open access repository that collects the work of some Toulouse researchers and makes it freely available over the web where possible.

This is an author's version published in: <https://oatao.univ-toulouse.fr/18216>

Official URL : <http://dx.doi.org/10.1109/ICNF.2017.7985959>

To cite this version :

Durnez, Clementine and Goiffon, Vincent and Rizzolo, Serena and Magnan, Pierre and Virmontois, Cédric and Rubaldo, Laurent Localization of Dark Current Random Telegraph Signal sources in pinned photodiode CMOS Image Sensors. (2017) In: 2017 International Conference on Noise and Fluctuations (ICNF), 20 June 2017 - 23 June 2017 (Vilnius, Lithuania).

Any correspondence concerning this service should be sent to the repository administrator:

tech-oatao@listes-diff.inp-toulouse.fr

Localization of Dark Current Random Telegraph Signal Sources in Pinned Photodiode CMOS Image Sensors

Clémentine Durnez, Vincent Goiffon,
Serena Rizzolo, and Pierre Magnan
ISAE-SUPAERO, Toulouse, France
Email: clementine.durnez@isae.fr

Cédric Virmontois
CNES
Toulouse, France

Laurent Rubaldo
SOFRADIR
Veurey-Voroize, France

Abstract—This work presents an analysis of Dark Current Random Telegraph Signal (DC-RTS) in CMOS Image Sensors (CIS). The objective is to provide new insight on RTS in modern CIS by determining the localization of DC-RTS centers and the oxide interfaces involved. It is shown that DC-RTS centers are located near the transfer gate. In particular, it is demonstrated that both gate oxide and Shallow Trench Isolation (STI) contribute to this parasitic dark current variation.

Index Terms—Random Telegraph Signal, CMOS image sensors, Pinned Photodiode, Dark current, RTS, RTN, Random Telegraph Noise, Transfer Gate, STI, Shallow Trench Isolation

I. INTRODUCTION

DARK Current Random Telegraph Signal (DC-RTS) is a parasitic random process which limits the performance in many modern solid state photodetector (silicon based and others) in low light conditions. Indeed, as the noise impact is reduced and CIS are able to detect low flux, RTS phenomenon tends to be highlighted. Such signal which trend is given in Fig. 1, corresponds to discrete variations of the photodiode leakage current (see Sec. II for the photodiode cross section), and leads to random blinking pixels. This junction leakage current may be similar to the variable retention time observed in DRAM [1][2].

This parasitic fluctuation is different from the well-known RTS mechanism in MOSFET [3][4], which has already been widely analyzed and is due to a channel carrier capture/emission by a trap. The RTS signal studied here is different, because the metastable states can be observed directly at the output of the CIS (it is not the case of MOSFET RTS due to the correlated double sampling stage [5]), it is proportional to the integration time, and time constants between transitions are far longer (the order of magnitude at room temperature is about 120 s [6]). It has been demonstrated that in modern CIS, DC-RTS comes from metastable generation centers which probably change their geometrical configuration with time and induce discrete levels in the dark signal [6]. Previous

The authors would like to thank the ISAE Image Sensor Team for their help, especially Romain Molina for the design of the image sensor, Jean-Baptiste Lincelles and Alexandre Le Roch for their help in the data analysis.

work have shown that RTS centers are most likely situated at oxide interfaces [7] [8] in unirradiated devices. However, the precise location of these sources and the influence of oxide composition on the phenomenon remain unclear.

Thus, two CIS with several pixel designs (change in the transfer gate length and shape) have been realized to determine RTS centers position and the different oxides contribution.

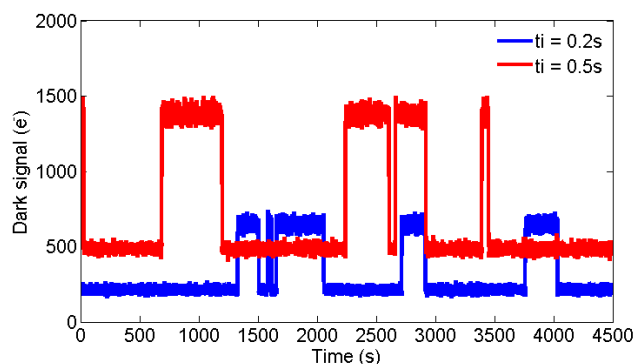


Fig. 1. Typical RTS signals of a same pixel acquired every 0.2 s and 0.5 s during 4500 s in dark conditions at 60°C.

II. EXPERIMENTAL DETAILS

The two studied CIS are constituted of 256x256 4T-Pinned PhotoDiode (PPD)[9] pixels and manufactured using a commercially available 0.18 μm process. They contain respectively 10 and 24 areas of 2560 to 6528 pixels, but for the sake of clarity, only 9 designs will be discussed.

Fig. 2 represents the architecture of a 4T-PPD pixel. It shows that the source of the well known SF-RTS (which is not studied in this work) is located at the Source Follower transistor and may be modeled by a resistance because of the variation of the channel conductance due to the trap capture/emission rate.

Fig. 2 also depicts the cross section of the photodiode considered as the reference one. The photosensitive element, which corresponds to the N-doped volume, collects charges during the integration time. The applied gate voltage is thus

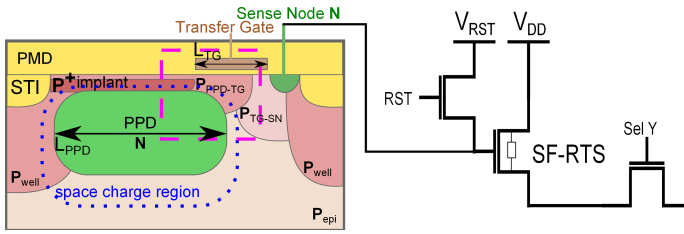


Fig. 2. Pixel architecture and cross section of the pinned photodiode used as a reference. L_{TG} is the transfer gate length and L_{PPD} is the PPD length.

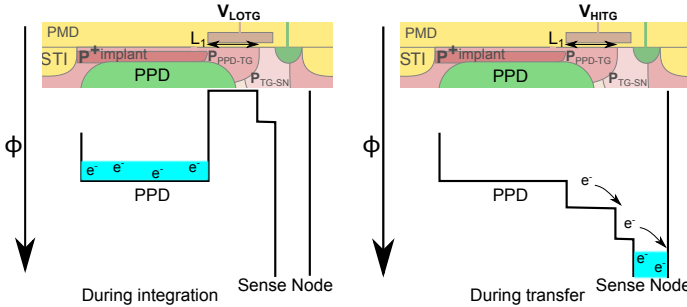


Fig. 3. Potential diagrams of the photodiode during integration time (on the left) and during charge transfer (on the right).

very low in order to separate the sense node and the photodiode (see left side of Fig.3 for the potential diagram of this case). After the integration time, a high voltage is applied to the transfer gate, in order to decrease the potential barrier and transfer charges to the sense node so that the signal is collected (see right side of Fig.3 for the potential diagram of this case). The different P-doped areas permit to enhance charge transfer performances, and the P^+ implant isolates the photosensitive element from the oxides. This technique using different doping is commonly employed in CIS processes.

Fig. 4 represents the behavior of the space charge region extension when the applied transfer gate voltage V_{LOTG} increases is shown. Indeed, as RTS centers are more likely to be near the oxide interface[7] [8], V_{LOTG} variation permits to place the depleted volume in contact or not with the Si/SiO₂ interface, to highlight or not RTS centers contribution.

This assessment is illustrated Fig.5 where the mean dark current is plotted as a function of V_{LOTG} for pixels exhibiting the reference design shown in Fig.2. Indeed, when a negative V_{LOTG} is applied, the transfer gate is accumulating, leading to a low dark current, and when a positive V_{LOTG} is applied, the transfer gate is depleting, and dark current increases.

The RTS pixels are detected thanks to a dedicated tool described in [10].

III. EXPERIMENTAL RESULTS

A. Influence of V_{LOTG} , L_{PPD} , L_{TG} and L_1

The CIS used for this section is the image sensor containing 24 areas. Fig. 6 and Fig. 7 represent the percentage of RTS pixels in 6 different areas for several V_{LOTG} . First of all, it can be seen that whatever the design is, there is no

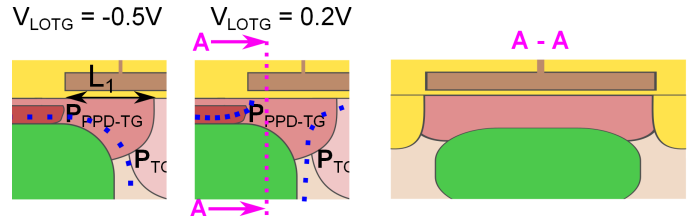


Fig. 4. Cross sectional views of the pinned photodiode drawn in Fig. 2. The first two images show the influence of the transfer gate voltage on the space charge region, and the last image is another sectional view A-A. L_1 is the distance where the implant P_{PPD-TG} and the transfer gate overlap. PMD means Pre-Metal Dielectric and STI Shallow Trench Isolation.

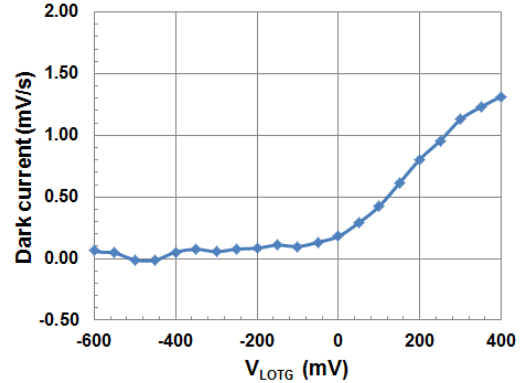


Fig. 5. Mean dark current as a function of V_{LOTG} at room temperature. The layout used for this curve is the reference one given in Fig. 2.

RTS contribution for negative voltage (0.075% of RTS pixels corresponds to 2 pixels in the area). This shows that RTS centers are not located in the bulk, because they participate to the dark current only when the depleted volume is in contact with Si/SiO₂ interfaces.

Moreover, Fig. 6 also reveals that the percentage of RTS pixels at a given V_{LOTG} does not depend on the pinned photodiode length. This means that centers are not located at the interface with the Pre-Metal Dielectric (PMD), which increases when the photodiode size increases too. Consequently, RTS centers seem not to be located near the N doped photodiode, but rather located next to the transfer gate side.

Fig. 7 represents the percentage of RTS pixels for 4 designs, changing the transfer gate length, or the overlap between the P_{PPD-TG} implant and the transfer gate (L_1). It can be seen that the transfer gate length influence on the number of RTS pixels is not significant. However, there is an influence of L_1 .

Indeed, Fig. 8 represents the cross section of Fig.2 in terms of potential wells. As the P_{TG-SN} implant is less doped than the P_{PPD-TG} implant, RTS centers contribution go directly to the sense node instead of being collecting. Hence, they do not participate to measured DC-RTS even if they still exist. That is why the transfer gate length has no incidence on RTS phenomenon, because only the P_{TG-SN} length is enhanced. This hypothesis is in agreement with the fact that when the P_{PPD-TG} implant is extended (L_1 increases), the ratio of RTS pixels

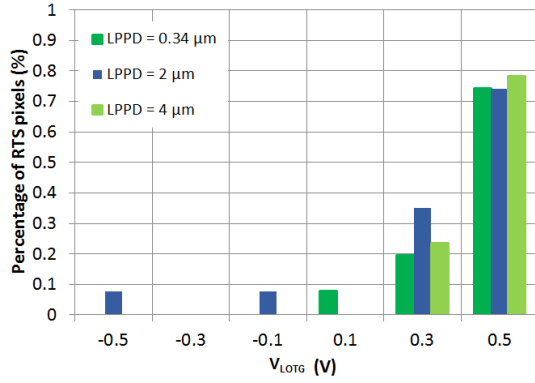


Fig. 6. Percentage of RTS pixels for several transfer gate voltages and 3 designs with different photodiode lengths. Each layout area contains approximately 2500 pixels.

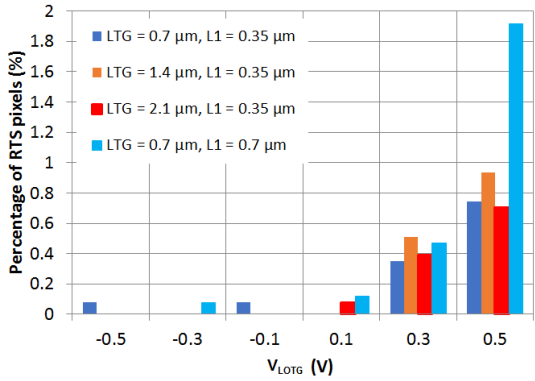


Fig. 7. Percentage of RTS pixels for several transfer gate voltages and 4 designs with different transfer gate lengths or changing parameter L_1 . Each layout area contains approximately 2500 pixels.

increases too even if the transfer gate length remains the same. Finally, it seems that RTS centers are more likely to be located under the TG, but the visible contribution to the dark signal comes from the overlap between the transfer gate and the P_{PPD-TG} implant.

B. Analysis of the transfer gate shape at a given V_{LOTG}

The CIS used for this section is the image sensor containing 10 areas. In this part, some variations in the transfer gate shape are analyzed, in order to better understand the precise location of RTS centers. Fig. 9 represents the three designs that will be studied. The first is the reference one, the second contains an annular transfer gate (no contact with the Shallow Trench Isolation (STI)) and the third one has one side of the annular gate which is extended to the STI. Tab. I sums up the designs parameters around the transfer gate. The overlap between the P_{PPD-TG} implant and the transfer gate will be called PTI (PPD-TG Implant). Additionally, A_{TG-PTI} will be the surface shared by the transfer gate and the P_{PPD-TG} implant, and $L_{STI-PTI}$ will be the distance where the STI and the P_{PPD-TG} implant are in contact under the transfer gate. As the STI depth is the same

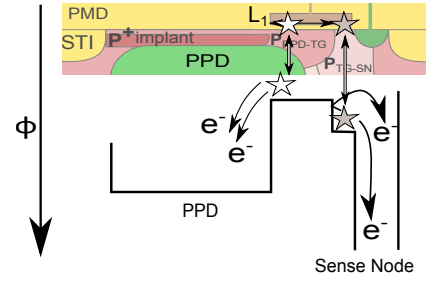


Fig. 8. Potential diagram of the photodiode when V_{LOTG} is applied to the transfer gate. Stars corresponds to RTS centers. Since the P_{TG-SN} area is less doped than P_{PPD-TG} area, its potential is higher. Thus, electrons generated by RTS centers located in P_{PPD-TG} (in white) area tend to go to the PPD, and electrons generated by RTS centers located in P_{TG-SN} (in gray) area go directly to the sense node because they go towards high potentials. Moreover, these electrons encounter a barrier when trying to go towards the PPD.

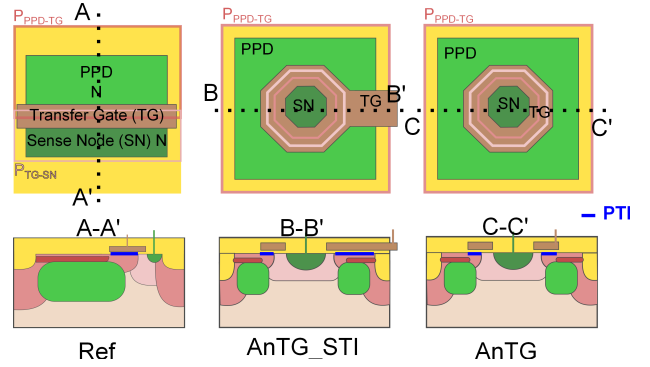


Fig. 9. Three design variations and their sectional views of the photodiodes studied : the first is the reference design, the second contains an annular transfer gate (called AnTG), and the third is extended until STI (called AnTG_STI). The blue lines correspond to the PTI (surface shared by the transfer gate and the P_{PPD-TG} implant).

for each layout, the influence of this parameter (in this case, this would become $A_{STI-PTI}$) cannot be analyzed.

First of all, there are much more RTS centers in the third design (AnTG_STI). The main obvious difference is the extension of the transfer gate area and this should play a role in RTS phenomenon as mentioned in Sec.III-A. However, there are about 2.5 more RTS pixels between AnTG and AnTG_STI, and the ratio of the area parameter (A_{PTI}) is about 1.7. Thus, the AnTG_STI contribution seems important but not sufficient to explain the location of RTS centers.

Another difference between these two designs (AnTG and AnTG_STI) is the contact of the TG depleted region and the STI sidewall. Indeed, in the first layout, the transfer gate has no contact with this oxide. This leads to fewer RTS pixels, but some remain anyway. Consequently, this interface certainly plays a role but cannot be the only contribution.

Hence, there seems to be a combination of several contributions to RTS phenomenon. In order to estimate the influence of each of the two interfaces, one can divide the number of RTS pixels by the total interfaces on the CIS zone :

$$Nb_{RTS} = X_1 \times A_{PTI} + X_2 \times L_{STI-PTI} \quad (1)$$

TABLE I

PARAMETERS OF THE DIFFERENT DESIGNS USED. A_{PTI} IS THE AREA SHARED BY THE TRANSFER GATE AND THE P_{PPD-TG} IMPLANT, $L_{STI-PTI}$ IS THE LENGTH WHERE THE STI, THE TRANSFER GATE AND THE P_{PPD-TG} IMPLANT ARE IN CONTACT. THE NUMBER OF RTS PIXELS IS GIVEN AT $V_{LOTG} = 0.2$ V.

	A_{PTI} (μm^2)	$L_{STI-PTI}$ (μm)	N_{BRTS}
Ref	1.1	0.7	40
AnTG	2.0	0.0	55
AnTG_STI	1.1	0.33	140

TABLE II

CALCULATED CONTRIBUTION OF A_{PTI} AND $L_{STI-PTI}$ AT $V_{LOTG} = 0.2$ V. THE SIZE OF EACH DESIGN AREA IS APPROXIMATELY 6500 PIXELS, AND TOTAL SURFACES ARE GIVEN AS THE SURFACE IN A PIXEL MULTIPLIED BY THE NUMBER OF PIXELS IN THE AREA.

	Total A_{PTI} (μm^2)	Total $L_{STI-PTI}$ (μm)	N_{BRTS} predicted	N_{BRTS} measured
Ref	7000	4600	42	40
AnTG	13000	0	59	55
AnTG_STI	21700	7200	115	140

with X_1 and X_2 respectively the number of RTS centers per μm^2 and per μm for both contributions, and $A_{PTI tot}$ and $L_{STI-PTI tot}$ respectively the total A_{PTI} and $L_{STI-PTI}$ on all pixels of the matrix zone (about 6500 pixels).

Tab. II represents the results obtained for the different contributions. It is found that there are about 0.0045 centers/ μm^2 at the interface between the transfer gate and the P_{PPD-TG} implant, and 0.0022 centers/ μm for the one overlapping the P_{PPD-TG} implant and the STI under the transfer gate (if the depth of STI is considered to be about $0.3 \mu m$ and that half of this depth is depleted, this would become 0.014 centers/ μm^2 and in this case, this contribution would be more important than A_{PTI}). These results are given at $V_{LOTG} = 0.2$ V. For higher transfer gate voltages, both contributions are higher since the depleted volume increases too.

It can be seen that this model seems relevant, even if there are some differences between the values predicted and measured. Indeed, there are not enough statistics to be more accurate, because the overall ratio of RTS pixels is low.

Finally, Fig.10 gives the summary of this work. RTS centers appear to be located at the Si/SiO₂ interfaces, more precisely under the transfer gate because the photodiode size has no influence. Moreover, as the doping P_{TG-SN} is lower than the P_{PPD-TG} one, the electrons generated there go directly to the sense node (and do not participate to the dark current). Consequently, only RTS centers located under the transfer gate, AND in the P_{PPD-TG} implant contribute to the signal collected. Eventually, two main edges seem to be at the origin of RTS phenomenon : the first is the area A_{PTI} and the second is the distance in contact with the STI $L_{STI-PTI}$ (it may also be an area if the depth is considered, but this parameter is difficult to estimate correctly in this work).

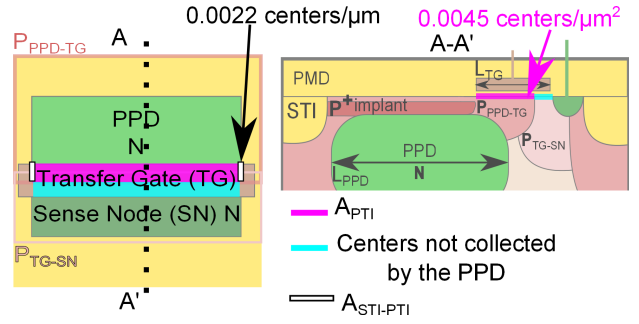


Fig. 10. Cross sections of the photodiode and localization of the main sources of RTS centers. The two contributions are shown in purple and blue.

IV. CONCLUSION

The results of this work provide new insight on RTS in unirradiated modern CIS, and allow a better understanding of noise and electrical temporal fluctuations in photonic devices. It has been demonstrated that there are two major contributions to Dark Current RTS : the interface between the STI and the P_{PPD-TG} implant under the transfer gate, and the area of the transfer gate overlapping the P_{PPD-TG} implant. The first one can be removed with an annular transfer gate which has no contact with the STI. The density has been calculated at a given V_{LOTG} for both contributions and this reveals that the second contribution is responsible for twice more RTS pixels than the first source (in a standard pixel design for a $7 \mu m$ pixel pitch in the studied technology).

REFERENCES

- [1] D.S. Yaney, C.Y. Lu, R.A. Kohler, M.J. Kelly, and J.T. Nelson, "A metastable leakage phenomenon in DRAM charge storage-Variable hold time," *Electron Devices Meeting (IEDM), 1987 IEEE International*, pp. 336-339, 1987.
- [2] P.J. Restle, J.W. Park, and B.F. Lloyd, "DRAM variable retention time," *IEDM Tech. Dig.*, pp. 807-810, 1992.
- [3] M. J. Kirton et. al, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency ($1/f$) noise," *Advances in Physics*, vol. 38, no. 4, pp. 367-468, 1989.
- [4] E. Simoen, and C. Claeys, "Random Telegraph Signals in Semiconductor Devices," *IOP Publishing*, Online ISBN: 978-0-7503-1272-1, 2016.
- [5] X. Wang, P.R Rao, A. Mierop, and A.J.P. Theuwissen, "Random telegraph signal in CMOS image sensor pixels," *Electron Devices Meeting (IEDM), 2006 IEEE International*, pp. 1-4, 2006.
- [6] C. Durnez, V. Goiffon, C. Virmondois, J. M. Belloir, P. Magnan, and L. Rubaldo, (2016). "In-depth Analysis on Radiation Induced Multi-level Dark Current Random Telegraph Signal in Silicon Solid State Image Sensors," *IEEE Trans. Nucl. Sci.*, Dec. 2016.
- [7] V. Goiffon, C. Virmondois, and P. Magnan, "Investigation of dark current random telegraph signal in pinned photodiode CMOS image sensors," *Electron Devices Meeting (IEDM), 2011 IEEE International*, pp. 8-4, 2011.
- [8] K. Ackerson, C. Musante, J. Gambino, J. Ellis-Monaghan, D. Maynard, R.J. Rassel, and K. Ogg, M. Jaffe, "Characterization of" blinking pixels" in CMOS Image Sensors," *Advanced Semiconductor Manufacturing Conference*, pp. 255-258, May. 2008
- [9] E.R. Fossum, and D.B. Hondongwa, "A review of the pinned photodiode for CCD and CMOS image sensors," *IEEE J. Electron Devices Soc.*, vol. 2, no. 3, pp. 33-43, May. 2014.
- [10] V. Goiffon, G. R. Hopkinson, P. Magnan, F. Bernard, G. Rolland, and O. Saint-Pé, "Multilevel RTS in proton irradiated CMOS image sensors manufactured in a deep submicron technology," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 4, pp. 2132-2141, Aug. 2009.