On the time-dependent transport mechanism between surface traps and the 2DEG in AlGaN/GaN devices

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***Abstract*—The physical mechanisms involved in the trapping and de-trapping processes associated to surface donor traps in GaN transistors are discussed in this work. The paper challenges the conventional transient techniques adopted for extrapolating the trap energy level via experiments and TCAD simulations. Transient TCAD simulations were employed to reproduce the time-dependent electrical behavior of a Metal-on-Insulator Field-Effect-Transistor (MISFET) and explain the influence of the electric field and energy barrier on the transient time associated to the trapping and de-trapping mechanisms of surface traps. The comparison between three test-structures and the relative variation of the trapping and de-trapping times with the bias and trap parameters leads to the suggestion of a proposed test-structure and bias configuration to accurately extrapolate the energy level of surface traps in GaN transistors.**

***Index Terms*—Gallium Nitride (GaN), Metal-on-Insulator Field-Effect-Transistors, donor traps.**

I. INTRODUCTION

GALLIUM NITRIDE transistors have superior physical properties such as high electron mobility in the channel (up to 2000 $cm^2/(V \cdot s)$), high electron density in the two-dimensional electron gas, 2DEG (~ 1×10^{13} cm^{-2}), and high critical electric field (3 MV/cm) if compared to their silicon counterparts. These properties make GaN very appealing for the fabrication of high voltage devices in the 600V-1.2kV range [1, 2]. It is widely recognized that donor-like traps are present at the surface of GaN-based transistors and their change in occupancy with the bias affects the electrical performance of such devices [3-6]. Information on trap states such as trap concentration, energy level, and cross section are essential to predict both the robustness and the electrical behavior of the power HEMT in a switching event in a specific power application. This is because these quantities affect the trapping and de-trapping time constants, thus influencing the time-response of the device during the switching or transient state [7]. Based on the knowledge in trap characterization acquired for other semiconductors (e.g. Silicon and Gallium Arsenide), several techniques have been used for GaN-based devices in order to extrapolate the trap-related quantities mentioned above [8-11]. Some of the most followed methods are based on capacitance measurements [11, 12] and transient response of the drain current to an applied stress [4, 10, 13]. These measurements directly correlate the outcome of the experiments to a trap response and characterize the trap states accordingly. Often, such measurements are carried out independently without being corroborated. In this paper, the authors demonstrate via extensive electrical characterization based on transfer characteristics, capacitance and transient analysis that this is not always accurate, and the accuracy and the quality of the analysis could be significantly improved if these techniques are cross-coupled. A detailed analysis on how the outcome of the trap-characterization techniques could be wrongly interpreted due to other mechanisms occurring in the device is performed in this paper via the study of a specifically designed MISFET test structure. The analysis is carried out by means of experiment and TCAD simulations and focuses on the dynamics of trap-states at the surface of the device (i.e. at the interface between the first passivation layer and the top active layer of the structure).

II. THE METHOD

A. Device cross section

The cross section of the device measured and analyzed is schematically reproduced in Fig. 1 (a). The device is based on a GaN on silicon (GaN-on-Si) technology. Details of the process can be found in [14]. The attention of this work is focused on the top layers of the devices formed by a SiN-GaN-AlGaN-GaN sequence of layers. The top SiN layer is a Low-Pressure Chemical Vapor Deposition (LPCVD) grown passivation layer. The 2DEG forms at AlGaN-GaN interface as highlighted in the cross sections of Fig. 1. The interface between the SiN and GaN-cap layer will be referred to as surface and the charge dynamic of both free carriers and trap states present at this surface will be discussed in this work. The gate length of the test-structure in Fig. 1(a) is as long as 76 µm. This allows for a more precise evaluation of the charge and states at the surface. It is worth mentioning that in a standard power HEMT the passivation layer extends along the source-to-gate and gate-to-drain distances only (i.e. the gate metal lies on top of the GaN-cap), and the gate length is shorter (1-2 µm). Fig.1(b) shows the cross section of large area HEMT (L_g = 76 µm) with a Schottky gate. The structure in Fig. 1(c) represents a hypothetical large area MISFET used in TCAD simulations where the source and drain terminals contact directly the 2DEG without a contact to the GaN-cap-SiN surface and (d) a hypothetical short-gate MISFET (L_g = 5 µm) used in simulations where the contacts to the 2DEG and the surface are made through highly doped N-wells extended directly under the gate oxide, as in a conventional MOSFET. One should note from Fig.1 that the devices analyzed are normally-on (i.e. the threshold voltage, V_{th}, is negative).

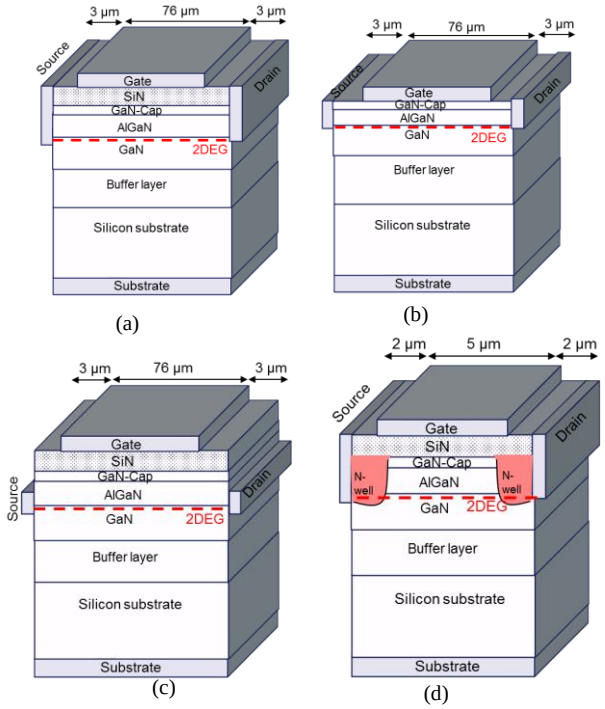


Fig. 1 (a) Cross-section of a fabricated large gate area MISFET; (b) Cross-section of a large gate area HEMT (c) Cross-section of a large area MISFET used in TCAD simulations where the source and drain terminals contact directly the 2DEG without a contact to the GaN-cap- SiN surface; (d) Cross-section of a short-gate MISFET used in simulations where the contacts to the 2DEG and the surface are made through highly doped N-wells extended under the gate oxide as in a conventional MOSFET.

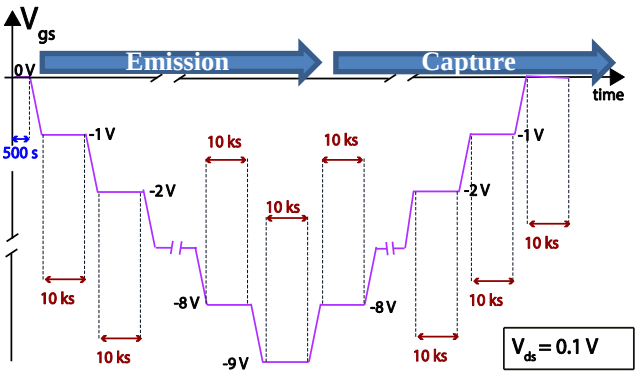


Fig. 2 Step signal applied on the gate for the transient analyses. Every step has 1 V amplitude and it is kept for 10 ks. The V_{ds} is kept constant at 0.1 V. Emission from trap states is observed when applying gate voltage steps from 0 V to -9 V. Capture from trap states is observed when applying gate voltage steps from -9 V to 0 V.

B. Measurement techniques

Three different measurement approaches performed on the test structure in Fig. 1 (a) were combined: (i) DC transfer characteristics (I_dV_g); (ii) Transient response of the drain current to an applied V_g step; (iii) Multi- frequency and multi-temperature gate capacitance vs gate voltage ($C_{gg}V_g$). In all the experimental set-ups the substrate is grounded and given that the 2DEG is at very low potential (between the grounded source and the 100 mV applied to the drain), the traps in the GaN buffer and the transition layers under the 2DEG do not play any significant role. This technique is therefore used to study solely the surface traps.

were used to perform the electrical characterization according to the following details and measurement set-ups:

1) DC transfer characteristics: I_dV_g

Transfer characteristics were measured by sweeping the gate bias and keeping the drain voltage at 0.1 V. Both forward (from negative to positive bias) and reverse (from positive to negative bias) sweeps were performed.

2) Transient drain current

The drain current was monitored over time following a 1 V step applied to the gate with a potential of 100 mV applied to the drain terminal. As shown in Fig. 2, the current was monitored over 10 ks for each step of 1 V amplitude from 0 V to -9 V and back from -9 V to 0 V.

3) Multi frequency gate capacitance vs gate voltage: $C_{gg}V_g$

The gate capacitance was measured as function of V_g at the frequencies 10 kHz, 100 kHz, 1 MHz. Source and drain contacts were connected together to a zero voltage power supply. The same study was performed at T= 35, 45, and 75° C.

C. TCAD model

A TCAD model was built in Sentaurus (by Synopsys) in order to validate the hypothesis made based on experimental results. A positive fixed sheet charge equal to 9×10^{12} cm^{-2} was included at the AlGaN/GaN interface to take into account the piezopolarization effect in III-nitride materials. Bulk acceptor traps were included with a concentration of 1×10^{17} at an energy level 0.9 eV from the valence band. This value is consistent with those reported in other publications [15, 16] and has shown no influence on the surface traps dynamics studied in this work, given the low voltage applied to the structure in this analysis. Acceptor-like traps were also included in the AlGaN barrier layer both as a uniform concentration and as discrete states. Defects in this layer are in fact often present and responsible of leakage paths from the 2DEG to the surface and vice-versa. The uniform concentration included was 1×10^{15} at an energy level 0.9 eV from the valence band. Discrete trap levels were included in the deck to simulate the influence of trap-to-trap tunneling, where each trap state is coupled via tunneling to the next adjacent one. The energy level considered for these discrete states was 1.9 eV from the mid bandgap, which is consistent with the value estimated in [17]. A uniform distribution in energy of surface donors was included at the SiN/GaN interface. Details of the values considered for these donor traps are discussed in the following sections.

III. TRANSFER CHARACTERISTICS

The measured I_dV_g for the test-structure in Fig.1(a) is shown in Fig. 3. The relatively high negative value of the threshold voltage (V_{th} = ~ -27 V) is due to the fact that the thickness of the SiN layer underneath the gate metal is that of the first passivation layer in the drift region of the conventional HEMT. This passivation layer is much thicker than the gate insulator of a normally-off insulated-gate GaN MISFET, hence the high negative V_{th}. It is however worth noting that while the specific results presented here concern a normally-on device with a high threshold voltage, the analysis is also

applicable to normally-on devices with lower threshold voltage or normally-off devices. In Fig. 3 one can clearly note that a strong hysteresis is present between the forward and reverse sweeps. The authors demonstrated in [18, 19] that this hysteresis is associated to the trapping of electrons by surface donor states during the forward sweep and to the de-trapping of electrons during the reverse sweep with an associated de-trapping time constant longer than the sweeping time. Figure 3 also shows the I_dV_g performed on an equivalent large area HEMT structure (without SiN layer underneath the gate electrode as in Fig. 1(b)). No hysteresis or other trap-related signs are present in the HEMT for the same current level, indicating that the MISFET I_dV_g is capturing the signature of surface traps between the SiN and the cap layer. Transient TCAD simulations with sequent ramps of 100mV/0.1s reproducing the measurement step size were performed to validate this hypothesis. Fig. 4 shows the results of this analysis. One can note that transient simulations allowed to match both the plateau characteristic of the forward sweep and hysteresis present in the measured transfer characteristics. The voltage range of the I_dV_g where the current stays constant with the V_g (~ -10 V to ~ 0 V) is associated to a change in occupancy of the donor states [18]. Following a forward sweep from -30 V to +20 V, the donors are 100% empty (i.e. ionized) at V_g = -10 V. As V_g increases, the capture process starts to occur until donor-states get 100% full (i.e. de-ionized). The opposite emission process takes place during the reverse sweep. This observation is crucial for the following analysis that will focus on the transient response of the drain current to V_g voltage steps in this specific gate bias range where donors change their occupancy (0 V, -9 V). The good agreement between experimental results (Fig. 3) and simulations (Fig. 4) is obtained indicating that the time constants associated to the trapping (i.e. capture) and de-trapping (i.e. emission) of electrons from donor-states are fairly estimated. A detailed analysis of the physical mechanisms involved in the capture and emission process is performed in Section IV.

IV. Transient Drain Current

Transient measurements, as described in section II, were performed for gate biases within the region of change in ionization of donor traps. As shown in Fig. 2, the 1 V-amplitude steps in the direction from 0 V to -9 V were performed to analyze the ionization of donors and therefore the emission process associated to it. Vice versa the gate voltage steps from -9 V to 0 V were applied to monitor and describe the capture of electrons into trap states. For each bias step, the initial voltage is indicated as V_{gstart} and the final voltage as V_{gstop}. It is worth mentioning that the quantity measured in this experiment is the drain current and therefore the analysis indicates how the emission and capture processes couple with the variation in the drain current. One should also note that the transient measurement technique applied in this work differs from a standard pulsed measurement. In a pulsed measurement with fill pulses the ΔV step changes for each step, consequently affecting the variation per step of parameters such as vertical and lateral Electric field that in turn influence the trap ionization and de-ionization times. The pulsed measurement with fill pulses does not represent the measurement routine followed to obtain a 'true' DC transfer characteristics which yielded the curve in Fig. 3. This I_dV_g shows a noticeable hysteresis that we aim to explain via the proposed transient measurements. Moreover, by waiting 10ks per step we are sure that each transient response provides information on the ionization or de-ionization of traps per voltage. Fig. 5 shows both measured (circles) and simulated (solid lines) drain current over time. In particular, Fig. 5(a) includes the results corresponding to the capture process of electrons by trap-states for two steps -5 V to -4 V and -7 V to -6 V and Fig. 5(b) shows the results for the corresponding emission process (i.e. step bias from -4V to -5V and -6 V to -7 V). As expected, the current decreases over time as electrons are trapped into the donor-states (Fig. 5(a)) and increases over time as a consequence of electron emission from trap states (Fig. 5(b)). The capture and emission time constants for measurements and simulations for each step are also included in Fig. 5. These constants were calculated taking the point of maximum slope of the first derivative of the transient curves.

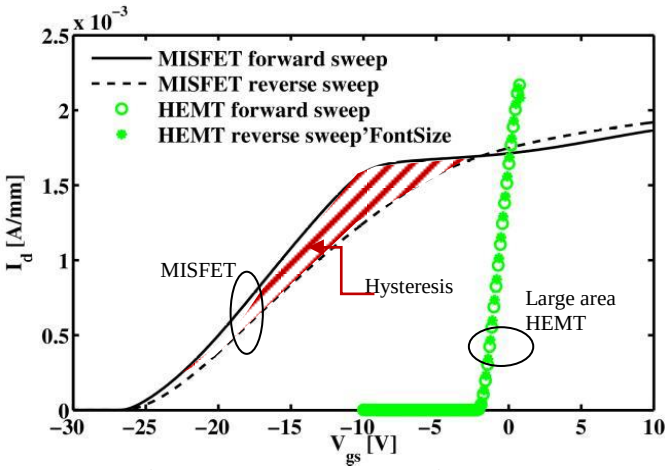


Fig. 3 Measured forward and reverse sweeps I_dV_g for the test-structure in Fig. 1(a) and 1(b). A strong hysteresis is present between forward and reverse sweeps in the MISFET case suggesting trapping of electrons at the surface.

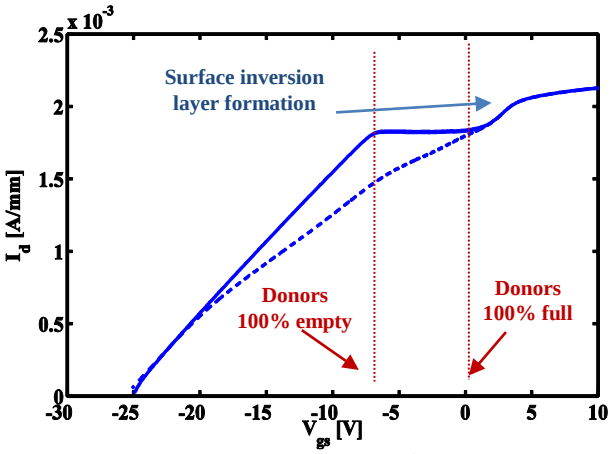
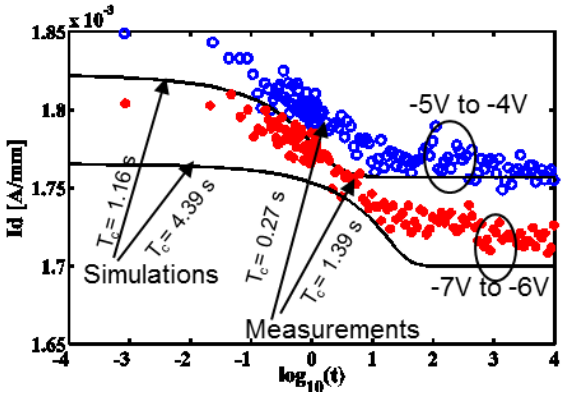
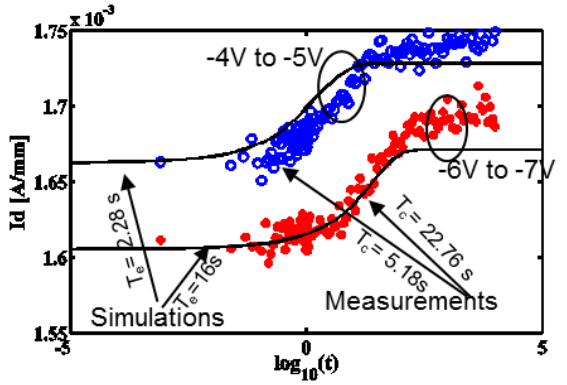


Fig. 4 Transient TCAD simulations of the transfer characteristics in Fig. 4 The ramp speed is 100 mV/ 0.1 s .

In order to obtain the results as presented in Fig. 5, a uniform



(a)



(b)

Fig. 5 Measured and simulated transient drain current of the structure in Fig. 1(a) during (a) capture and (b) emission for two different gate bias steps. The gate voltages are stepped by 1 V and monitored for 10 ks according to the step signal in Fig. 2.

donor concentration of 1.5×10^{13} $cm^{-2}eV^{-1}$ within an energy range of 0.32 to 0.52 eV below the conduction band and a cross section $1e^{-16}cm^2$ was included. Trap-to-trap tunneling and direct tunneling were also activated in the TCAD model. It is worth noting that the duration of the transient - before the current reaches a steady-state condition - depends on the gate bias applied both for emission and capture processes. If one had to follow the classical approach for extrapolating the energy level from an Arrhenius plot, one would obtain two different levels as shown in Fig. 6. The trap energy level extrapolated are in fact 0.55 eV for the -4 V to -5 V step and 0.68 eV for the -6 V to -7 V. This dependence of the energy level on the gate bias level applied is not expected and it does not follow the equations that describe the capture and emission processes, as discussed in the next sections. TCAD simulations were performed to explain this dependence and demonstrate that the time constants extracted depend not only on the capture and emission times from trap-states but also on the physical mechanisms responsible for the movement of carriers from and to trap-states. Capture and emission processes will be discussed separately.

A. Capture process

The electron capture rate is defined as [20]:

$$R_c^n = v_{th} \cdot \sigma^n * n * n_D^{empty} \quad (1)$$

Where $c^n = v_{th} \cdot \sigma^n$ is the electron capture coefficient (cm^3/s) and is given by the product of the thermal velocity v_{th} and the electron capture cross section σ^n; n is the amount of available electrons and n_D^{empty} is the amount of ionized donors (i.e. empty states).

In other words, how fast electron are captured by trap-states depends not only on the trap-related parameters such as cross section but also on how many free electrons are available. The authors have demonstrated that a uniform donor concentration of 1.5×10^{13} $cm^{-2}eV^{-1}$ within an energy range of 0.32 to 0.52 eV below the conduction band is able to reproduce the measured time constants [18]. In this work, the authors want to discuss the complete scenario of the physical mechanisms involved in this process and in particular the role of the drain and source contacts on the time constants, ultimately suggesting the appropriate test-structure to consider for surface trap characterization. Fig. 7(a) depicts the capture process in terms of energy levels (conduction band, Fermi level and uniform distribution of donors) in a 3-D coordinate system. In this way, it is easier to visualize the movements of the carriers involved in the capture process along both directions x and y. As stated by Eq. 1, the time required for the electrons to be captured by traps states (τ_c) depends on how many free electrons are available.

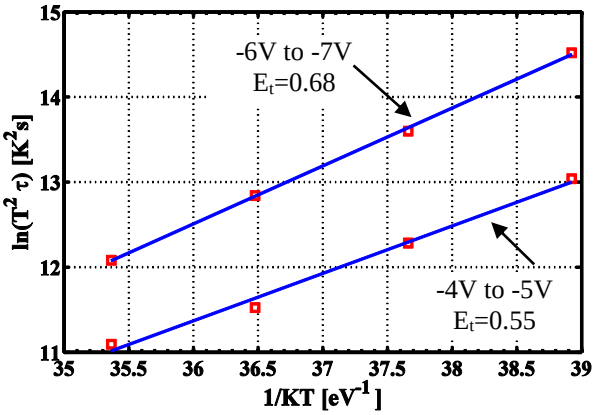


Fig. 6 Arrhenius plot and energy level extrapolation for the test structure in Fig 1(a) for two different gate bias steps (-4V to -5V and -6V to -7V). One can note that two energy levels (0.68 eV and 0.55 eV from the conduction band are extracted. This result proves inconsistency and the use of the Arrhenius plot for structure 1(a) is therefore inappropriate.

Fig. 8(a) explains the complete set of mechanisms involved in the capture process: the fall-into-trap process (C3) follows or at least depends on the mechanisms of crossing the barrier (C1) and lateral drift from the contacts (C2). The crossing of the barrier (C1) takes into account the thermionic emission, the tunneling from the 2DEG, and the trap-to-trap (T2T) tunneling, hence the three arrows in the figure. The authors demonstrate here via TCAD simulations that the position and the nature of the source and drain contacts significantly affect the capture time. This is done by comparing the results obtained by simulating the structure in Fig. 1(a) and Fig. 1(c). The latter having the source and drain electrodes contacting only the 2DEG and not the surface. The V_g step considered in the study that follows is -5 V to -4 V, unless differently specified. Fig. 8 shows the first result of this analysis by plotting the extrapolated time constant as function of the

AlGaN/GaN energy barrier for the two structures under examination. One can note that the impact of the variation of the barrier height is negligible in the case of surface contacted while it is significant if the surface is not contacted. This can be explained via Fig 7(b) and 7(a). When the surface is not contacted (Fig. 7(b)) the dominant mechanism for providing electrons to the surface is via crossing the barrier (mechanism C1). On the other hand, when the surface is contacted (Fig 7(a)) the lateral drift (mechanism C2) is faster, thus any changes in the barrier height will not affect the capture time.

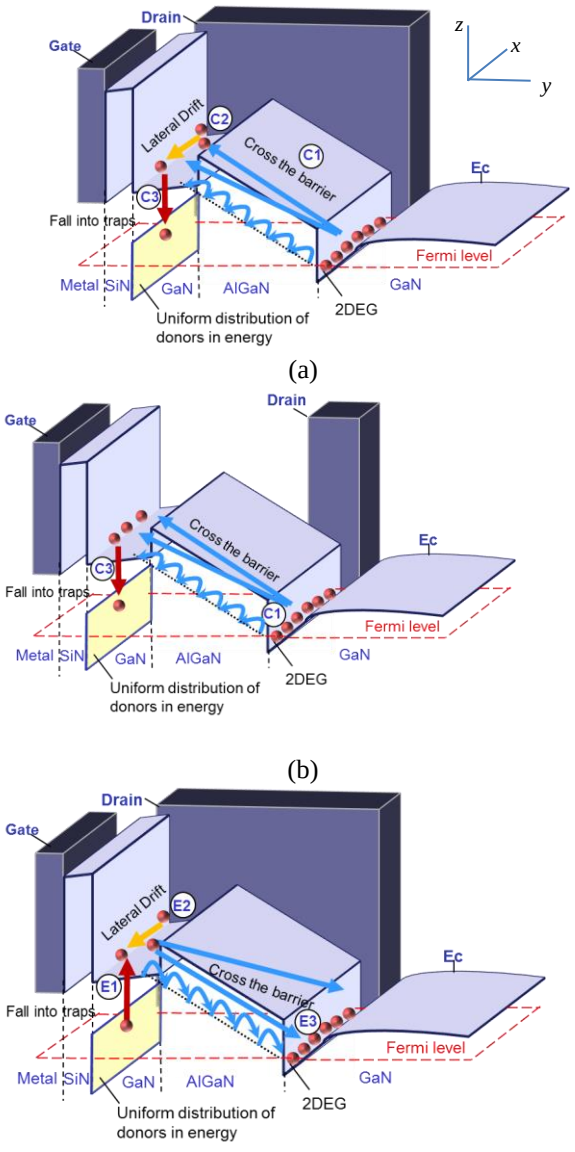


Fig. 7 Schematic representation of the conduction band and fermi level (at zero bias) and physical mechanisms involved in the transport of electrons (a) from the 2DEG to the traps (capture into traps process) for the structure shown in Fig. 1(a); (b) from the 2DEG to the traps (capture into traps process) for the structure shown in Fig. 1(c) and (d) from the traps into 2DEG (emission to 2DEG process) for the structure shown in Fig. 1(a). The processes C1 and E3 identified the possible mechanisms for electron to 'Cross the barrier': (i) Thermionic Emission, (ii) Direct tunneling, (iii) Trap-to-trap tunneling.

Moreover, in Fig. 8 it is included the comparison of the simulated time constants with the only trap-to-trap (T2T) mechanism and with any tunneling activated for the structure where only the 2DEG is contacted. As expected, the variation on the barrier height has much more impact in the case of any tunneling activated. An important proof of concept that more than one mechanism is contributing to the overall capture time is obtained by modifying in the input deck of the TCAD simulator the electron capture cross section (σ^n) of the donor surface traps. Fig. 9 shows the results of these simulations for two different drain biases of 100 mV and 10 V. In both cases, σ^n needs to reach very low values (1×10^{-19} cm^2) to actually have an impact on the capture time. This is due to the fact that for high cross section values ($>1\times10^{-19}$ cm^2) the trap recombination rate is higher (see Eq.1) and therefore the only-trap-related capture time is very small and negligible with respect to the time associated to crossing the barrier and drifting from the contact. As a consequence, the overall trapping time stays constant after a critical value of the capture cross section, which depends on the drain bias. In fact, a higher drain bias affects both the vertical and lateral electric field in the structure, enhancing processes C1 and C2 and thus reducing the overall capture time (Fig. 9). This is of course with the exception of small enough ($<1\times10^{-19}$ cm^2) cross sections where the trap recombination rate is significantly reduced. In this case, processes C1 and C2 have time constants negligible compared to the overall capture time and therefore any further reduction of cross section is directly reflected into an increase of τ_c. It is worth mentioning that although the electron concentration at the surface is not very high ($\approx2\times10^5$ cm^{-2}) electrons can be provided by the 2DEG through the short-circuit created by the drain contact between the 2DEG and surface and contribute to the drift process C2. The lateral drift process C2 is responsible for the difference in time constants at different V_{gs} for the structure 1(a). We also believe that if the surface is not properly contacted (as it should be the case in experiments) we can get closer to the situation of structure 1(b) where other mechanisms such as thermionic emission, tunnelling, and T2T would be the reason why at different gate biases the time constants differ. This is because the barrier and vertical electric field across the barrier is different at different gate biases, thus influencing all these mechanisms. The difference in the capture curves between the experimental and simulated results in Fig. 5(a) could possibly be due to a lateral surface hopping occurring in the structure and providing electrons to the surface, thus accelerating the capture process in experiments. The capture process time constant in fact depends on the number of available electrons in the conduction band as specified by Eq. 1. This dependency is not valid for the emission process, as it will be discussed in the following paragraph. Following this analysis, the authors propose the test structure as drawn in Fig 1(d) to be certain that only the trap-associated time constants are extracted via a transient approach. This would allow to characterize the trap energy level accurately. The advantages of this test structure and analysis over the previous considered are the following:

- The gate is much shorter (5 µm) to reduce the lateral drift time. This gate is still larger than in a normal HEMT, but significantly smaller than in the previous test structure.

- N-wells connect the source and drain contacts to the Metal-on-Insulator stack of the gate in order to ensure a source of electrons for the surface.
- A higher drain bias (~10 V) is suggested when the gate bias is varied and the transient drain current monitored. This will guarantee a negligible impact of time associated to the electron transport from and to the 2DEG across the AlGaN\GaN barrier on the trapping time.

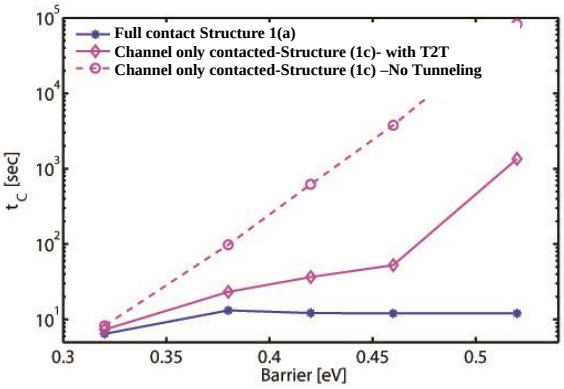


Fig. 8 Simulated capture time constant as a function of the AlGaN/GaN energy barrier for the structure in Fig. 1(a) – full contact, and the structure in Fig.1 (c) – where only the 2DEG is contacted, with the trap-to-trap (T2T) tunneling activated and without any tunneling.

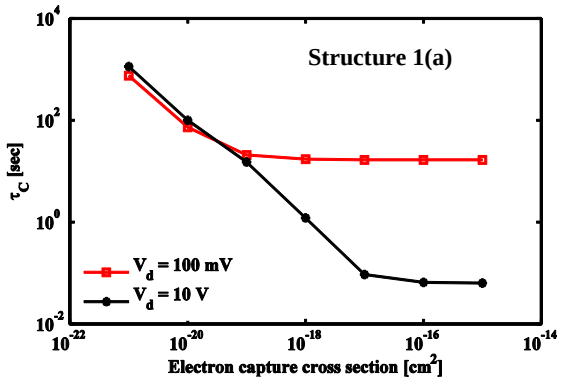


Fig. 9 Capture time constant as a function of the electron capture cross section for two different biases on the drain terminal (100 mV and 10 V) extracted from simulations of the structure shown in Fig. 1(a).

The capture time was extracted from the simulation of the transient response to the -5 V to -4 V gate step of the suggested test structure (with V_d = 10 V). In Fig. 11 the results of this analysis are plotted for different electron capture cross sections and it is clearly shown that τ_c linearly depends on σ^n for any value of σ^n. This demonstrates that no mechanisms other than the trap-related one are affecting τ_c.

B. Emission process

The electron emission rate does not depend on the amount of available carriers as it is for the capture rate but is defined as [20]:

$$R_e^n = e^n * n_D^{full} \quad (2)$$

Where e^n is the emission coefficient for electrons (s^{-1}) and n_D^{full} is the amount of full donor-states.

In an equivalent manner as for the capture process of electron by trap-states, the overall emission process, which corresponds to an increase in drain current, depends on three different mechanisms represented in Fig 7(c): (E1) emission from trap states, (E2) lateral movement or drift, (E3) cross of the barrier via tunneling, T2T, and thermionic emissions. When discussing the extrapolation of the energy level of donor-states via Arrhenius plots, it is therefore essential to consider that the time measured is limited by the time associated to the movement of free carriers (E2 and E3 in Fig. 7(c)).

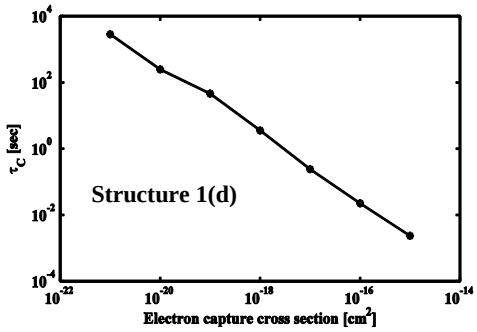


Fig. 10 Capture time constant as a function of the electron capture cross section extracted from simulations of the structure shown in Fig. 1(d). The drain bias is 10V.

As demonstrated for the capture process, the test structure in Fig 1(d) featuring source and drain N-wells extending laterally all the way to the Metal-Insulator gate-stack is ideal to calculate the trap energy level via the Arrhenius plot. The Arrhenius plot was extrapolated for the proposed test structure in Fig. 1(d) where a single level (E_t = 0.39 eV) donor trap was included at the surface and it is plotted in Fig. 11. The extrapolated energy level corresponds to E_t = 0.39 eV and is the same, independently on the gate bias applied. This proves the validity of the suggested structure and the voltage applied to properly caracterize the energy level of surface traps.

V. Gate Capacitance

One of the most used techniques in evaluating surface charges and traps is based on $C_{gg}(V_g)$ measurements at different frequencies and temperatures. Here we show that relatively high frequency $C_{gg}(V_g)$ measurements do not give an indication of deep traps, as these are too slow to react to the AC signal, but instead, could be used to evaluate the presence of a surface inversion layer. Gate capacitance measurements were performed on the MISFET structure in Fig. 1(a) for three different frequencies: 10 kHz, 100 kHz, and 1 MHz. These are included in Fig. 13. One can clearly note that a step in the $C_{gg}(V_g)$ is observed for gate voltages above 0 V and that the voltage at which this steps occurs is frequency dependent. In [21] the increase in gate capacitance was associated to the inversion layer formation at the SiN/GaN-cap interface. The accumulation of electrons at the surface forming the inversion layer follows a very similar dynamic to the one of the capture of electrons by trap-states described in Fig. 7 (a). In fact, in order to form an inversion layer, electrons need to be provided at the interface from the 2DEG via the barrier (mechanism C1) and from the contacts via lateral drift (mechanism C2). In order to validate this hypothesis $C_{gg}(V_g)$ measurements were carried out at increasing temperatures. Fig. 13 shows a zoom-

in of the inversion layer step in the $C_{gg}(V_g)$ at f = 100 kHz and T = 25, 45, 75 °C. It is worth noting that the voltage at which the gate capacitance steps up decreases with temperature. This can be explained by simply considering that an increase in temperature enhances the thermionic process, allowing for a faster reaction of electrons to the AC signal.

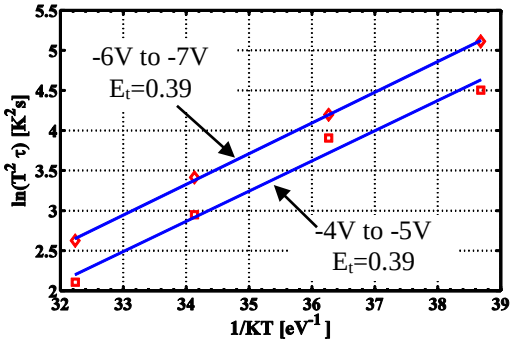


Fig. 11 Arrhenius plot and energy level extrapolation for the proposed test structure in Fig 1(d) for two different gate bias steps (-4V to -5V and -6V to -7V). One can note that unlike in Fig. 7, the energy levels extracted are the same, proving the validity of this Arrhenius plot.

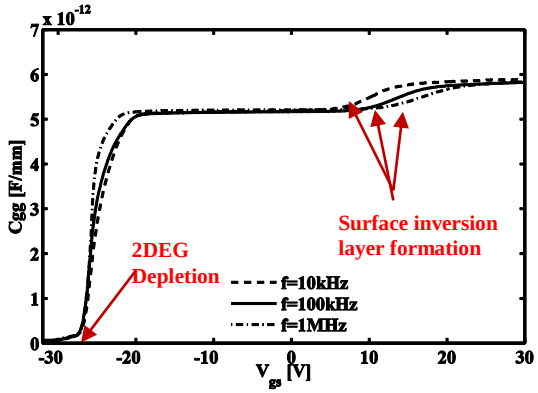


Fig. 12 $C_{gg}(V_g)$ measurements of the MISFFET structure shown in Fig. 1(a) for f= 10 kHz, 100kHz, and 1MHz. The small-signal frequency dispersion only impacts the AC formation of the inversion layer.

It is important to remember that at the gate biases considered (in the positive range of the gate voltages) where the inversion layer is formed, all the donors traps are fully occupied (i.e., the donors are completely de-ionised), and hence the time constants associated with the emission or capture processes from trap states are irrelevant. Based on the explanation given, one would expect not to have any dependence of the $C_{gg}(V_g)$ on the frequency if (i) a reservoir of carriers is present in proximity of the surface where the inversion layer forms, and (ii) the time needed for the electrons to travel to the surface is short enough to follow the AC signal. Fig. 14 shows the simulated $C_{gg}(V_g)$ at 10 KHz and 100 KHz of the MISFET in Fig 1(a) and of the proposed test structure as drawn in Fig. 1(d), where two highly doped N-wells that connect to the source and drain contacts provide a close source of electrons. As expected, no frequency dispersion is present in the case of the structure in Fig. 1(d) compared to the case of the structure of Fig. 1(a) where there is a clear difference between the 10 KHz and 100 kHz capacitance curves, as also observed in the measurements in Fig.12.

VI. CONCLUSIONS

In this paper we have carried out a detailed experimental and TCAD analysis of the surface traps and charges located at the interface between the top GaN-based layer and the first passivation layer.

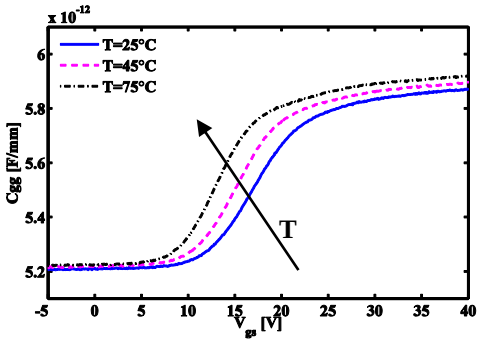


Fig. 13 Zoom-in of the measured gate capacitance for temperatures varying from 25°C to 75° C at f = 100 kHz.

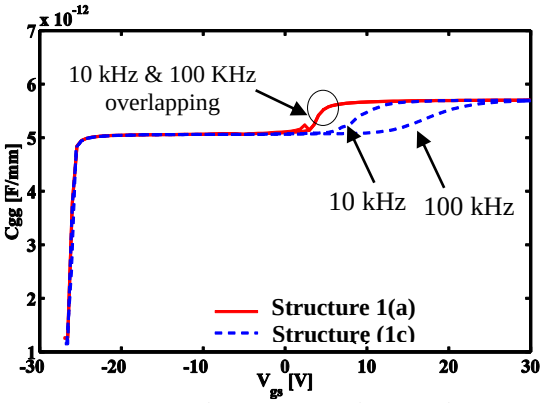


Fig. 14 TCAD simulations of the gate $C_{gg}V_g$) function of the gate-source voltage for two structures shown in Fig 1(a) and Fig. 1(d). Note that the structure Fig 1(a) shows frequency dispersion in the $C_{gg}(V_g)$ characteristics, while for the structure shown in Fig 1(d), the 10KHz and 100 kHz curves overlap.

The analysis was carried out using a specially designed MISFET test structure. We have cross-coupled the I_dV_g transfer characteristics, $C_{gg}(V_g)$ and long-time transient measurements to determine the exchange mechanisms between donor traps and the 2DEG. We have shown that the Arrhenius plots cannot be used to directly extract the energy levels of the donor traps if, for example, the source of electrons is provided by the 2DEG layer and the electrons have to cross the AlGaN/GaN barrier before reaching the trap states. We have also shown that the emission and capture time constants calculated from measurements using transient techniques depend on (i) surface trap energy levels, (ii) the energy barrier that needs to be overcome by either thermionic emission, direct or trap-to-trap tunneling, and (iii) carrier drift to the contacts. The role of electron transport in the trap dynamics was also discussed in [22, 23] via specifically designed test structures. However, these works, that follow [18], have not built a TCAD model for supporting their findings nor they have suggested an optimum test structure for trap characterisation. We have in fact proposed an alternative MISFET test structure that features a source of electrons at the

surface, in close proximity of the surface traps, which can be used to extract accurately the surface trap levels without being affected by the gate voltage level or by the AlGaN barrier width and height. Finally, we have shown that while relatively high frequency $C_{gg}(V_g)$ measurements do not provide surface trap information, they can be used to determine the gate threshold voltage at which the surface inversion layer is created. A similar transport mechanism, across the AlGaN barrier is involved in the exchange of electrons between the 2DEG and the surface inversion layer which leads to frequency dispersion in the $C_{gg}(V_g)$ characteristics. This frequency dispersion no longer exists if the source of electrons is in the close proximity and electrons do not need to cross the AlGaN energy barrier.

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