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Quantum Mechanical Analysis of GaN Nanowire Transistor for High Voltage Applications

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The paper presents the quantum mechanical analysis of Gallium Nitride nanowire transistor. The effect of high *k* gate dielectric and different gate metals on the electrical characteristics of the device is studied. Nanowire width has been reduced to have a proper control on the device characteristics at reduced gate length. A high value of drain current is obtained at gate length of 10 nm and nanowire radius equal to 10 nm, is obtained. Also high voltage operation of the device upto 40 volts has been shown. A flatter transconductance curve is obtained which shows the linearity of the device. The results obtained are comparable with the experimental and simulated data reported in literature

Keywords: Quantum mechanical, Nanowire, High *k* gate dielectric.

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1. INTRODUCTION

Cylindrical Nanowire FET is now gaining much traction in the research areas due to its unique structure and excellent subthreshold characteristics and scalability to different sizes along with noise reduction [1-7]. The reason for such improved performance is because of the structure of the gate which surrounds the channel completely and thus provides a better control over the current by the gate.

Gallium Nitride (GaN) has now been widely used for high electron mobility transistors (HEMT) due to its high mobility and also because of its wide bandgap which endows it the property of high breakdown voltage and allows it to be used for high voltage applications [8-9]. GaN nanowires have been in fabrication processes for a long time[10-11] and been used for photo-detection and photoluminescence applications [12-13]. Extensive research has been done in the area of employing GaN to nanodevices and FET's [14-18]. AlGaN/GaN nanowire FET was studied in details by Kang et.al. [17] which showed a positive drift in threshold voltage at lower gate widths. Li et. al. [18], demonstrated experimentally Ga_2O_3/GaN nanowire transistor with 50 nm and 20 nm gate length where scaling issues and short channel effects were analysed. Chen et.al. [19], investigated on the electrical properties of individual GaN nanowire based ferroelectric FETs. Mussener et et. al. [20], studied the internal electric fields in AlGaN/GaN nanowire heterostructures. Zhao et. al. [21], proposed a low cost green method to synthesize GaN nanowires which could be effectively used in GaN based nanowire FETs. Also, Fang et.al. [22], incorporated Silicon donor in GaN nanowires and FET measurements combined with finite mobility of carriers in the non-intentionally doped nanowires were carried out.

Keeping in view of the wide applications of GaN nanowire transistors and with the devices reaching smaller dimensions quantum mechanical analysis of the device is desired for gate lengths below 20 nm. The scaling down of the device gives rise to many effects which can only be accurately described by employing quantum mechanical model for analysis.

In this paper we propose quantum mechanical analysis of sub-20 nm GaN nanowire FET for high voltage applications. The device has been simulated using Silvaco TCAD device simulation software. Energy band diagram of the device has been shown with different gate and drain bias. The effect of other physical parameters like radius of the nanowire, different gate metals and gate dielectrics are considered. The current voltage and transconductance characteristics of the device have been studied in details by taking into account Schrodinger-Poisson quantum models. A flat gm-Vg curve proves the linearity of the device in a wide range of gate voltages. All the results agree well with the experimentally available data.

2. STRUCTURE OF DEICE AND METHODS

Figure 1 shows the three dimensional view of the device simulated where the metal contacts are made of Gold (Au). The gate dielectric HfO_2 is of 2 nm thickness which is deposited on GaN all around the structure and then the gate metal contact is placed on the dielectric material. The source and drain is doped with *n*-type material with a concentration of 10^{19}/cm^3 and the channel is *p*-type doped with a concentration of 10^{15}/cm^3.

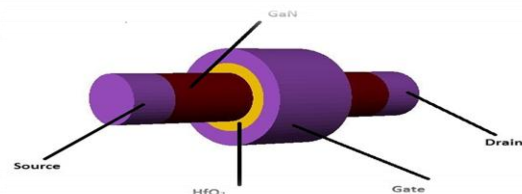

Fig. 1 - 3D structure of the device

There are two main quantum models in Silvaco TCAD: Bohm Quantum Potential and Schrodinger-Poisson. We have employed the latter model for the analysis. The simulation employs the Schrödinger model [23] for the simulation coupled with drift-diffusion

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mode space approach. Also field dependent mobility of the charge carriers has been employed along with Shockley-Read Hall recombination parameter.

Table 1 - Summarizes the parameters considered for device simulation

Parameters Used in Simulation	
Source/Drain Length	10nm
Source/Drain Doping(n-type)	10^{19}/cm^3
Channel Doping (p-type)	10^{15}/cm^3
Gate Thickness	2 nm

The Eigen state energy is given by the following equation:

$$-\frac{h^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{m_y^v(x,y)}\frac{\partial\psi_{iv}}{\partial y}\right)+E_c(x,y)\psi_{iv}=E_{iv}\psi_{iv} \quad (1)$$

Where the various terms used have their usual meanings.

The two dimensional confinement of electron concentration is given as:

$$n(x,y)=2\frac{\sqrt{(2k_BT)}}{h}\sum_v\sqrt{m_z^v(x,y)}\times \times\sum_{i=0}^{\infty}\left|\psi_{iv}(x,y)\right|^2 F_{-\frac{1}{2}}\left(-\frac{E_{iv}-E_F}{k_BT}\right) \quad (2)$$

Where $F_{-1/2}$ is the Fermi integral of order – 1/2.

3. RESULTS AND DISCUSSION

Silvaco TCAD has been used to design and analyze the electrical characteristics of the nanowire FET.

Energy Band Diagram

Figure 2 shows the energy band diagram when the drain voltage is varied from 10 V to 20 V at a constant value of V_g (= 5V). When the drain voltage is increased, the density of electron increases on the source side and hence it tends to lower the energy of the conduction band and valence band as lower energy excitation is required to make an electron move from valence band to conduction band.

Figure 3 shows the conduction and valence band when the gate voltage is varied from 1 V to 5 V. The drain voltage is kept constant at 10 V. The gate voltage is the main controller of the current from the drain to source side (or movement of electrons from source to drain side). As is expected, the potential barrier is reduced when the gate voltage is increased. The band diagram gives us an intuitive explanation of the current surge when gate voltage is increased.

Effect of Radii

The Radii of the GaN Nanowire was varied at 10 nm, 15 nm and 20 nm. The output and transfer characteristics of the device were obtained.

Figure 4 shows the drain current (I_d) versus the drain voltage characteristics at 10 nm nanowire radius and 10 nm channel length. The gate voltage (V_g) was kept constant at 5 V and drain voltage (V_d) was varied from 0 V to 40 V. It can be observed that the device

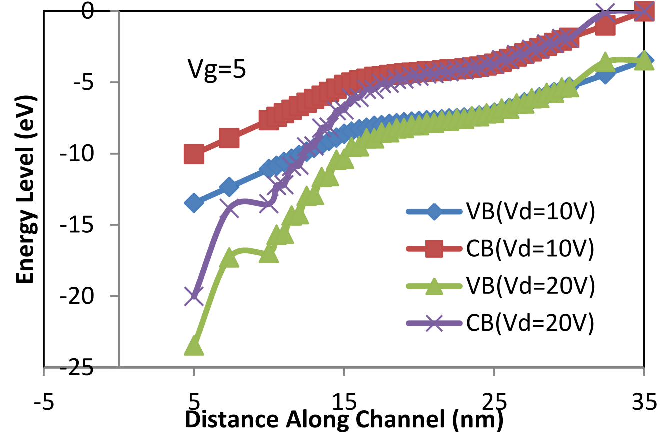

Fig. 2 - Valence and Conduction Band (Variation of Vd from 10 V to 20V) with Vg = 5V

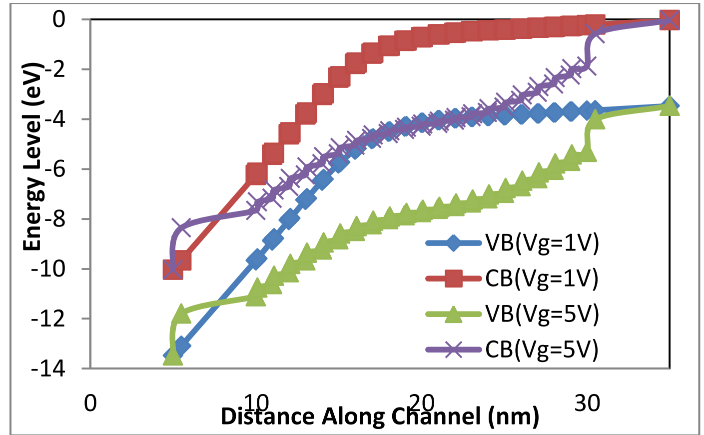

Fig. 3 - Valence and Conduction Band (Variation of V_g from 1 V to 5 V) with V_d = 10V

readily works till 40 V. One of the major observation of the GaN NWT is that the drain current remains fairly constant in the saturation region unlike many other device where the channel length modulation factor deviates the working of the short channel devices from the ideal conditions.

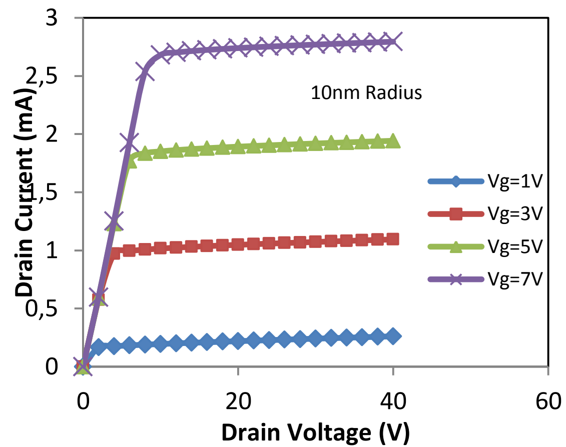

Fig. 4 - Variation of drain current with drain voltage at 10nm radius

Figure 5 shows the variation of the drain current

with the variation of radius of the device. It can be observed that the drain current is higher at higher values of nanowire radius. The reason for high current at larger radius is quite intuitive. When the radius is large, the electron concentration is more which in turn contributes to the high density of the electrons in the channel formed after applying gate voltage. However, choosing a right combination of nanowire radius and nanowire length, optimized value of drain current can be obtained.

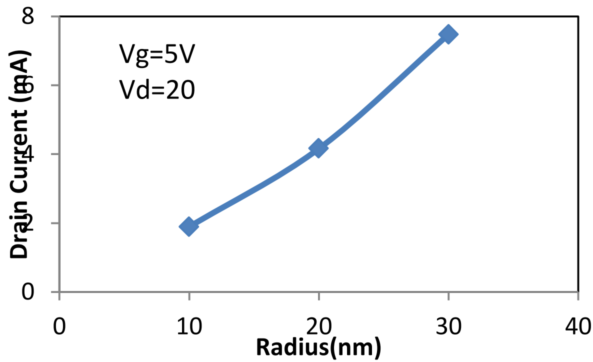

Fig. 5 - Variation of drain current with radius of the nanowire at a constant value of V_d and V_g

Figure 6 shows the I_d vs V_g characteristics of the device, where the gate voltage has been varied between 0 V to 10 V and the drain voltage has been kept constant at 10 V. The reason for keeping the drain voltage at 10 V is because the device is being considered for high voltage applications. The radii has again been kept at 10 nm, 15 nm and 20 nm. It can be observed that the subthreshold characteristic is better in the case of smaller radius and it becomes worse when the channel radius is increased. This can again be explained by the fact that when the gate voltage is reduced, the electron concentration should decrease at the junction of GaN and HfO_2. But when the radius is increased the control over the channel reduces because the channel is farther away from the central axis of the cylinder.

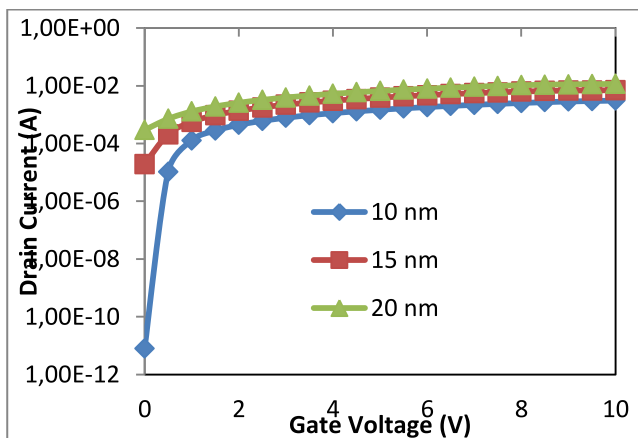

Fig. 6 - I_d vs V_g for different radii

Effect of Gate Dielectric

The transfer characteristic curves of GaN Nanowire have been plotted in Figure 7 using different gate dielectric materials. Here, we compare the characteristics using three different gate dielectrics, SiO_2, Al_2O_3 and HfO_2, the last two being high-k dielectric material. The consideration of high-k dielectric material is very essential because SiO_2 becomes a challenging material when scaled down to sizes below 5nm. So alternatives have to be used which have higher dielectric constants and hence can be scaled down easily and the EOT (Effective Oxide Thickness) can remain the same as before [16-17].

I_d vs V_g characteristics of the device gives an insight to the switching characteristic of the device when different gate dielectric materials are used. This can give us an understanding as to which material is better and by how much degree it is affecting the operation of the device. As can be observed from Figure 7, the subthreshold slope is lowest in the case of HfO_2 and the worst in the case of SiO_2. The dielectric constant of HfO_2 is nearly 25, Al_2O_3 is 10 and that of SiO_2 is 3.9. At the same thickness of 2 nm, HfO_2 provides a better current control in the channel since it has good thermal stability, high recrystallization temperature, sound interface quality, low defects and prevents leakage current.

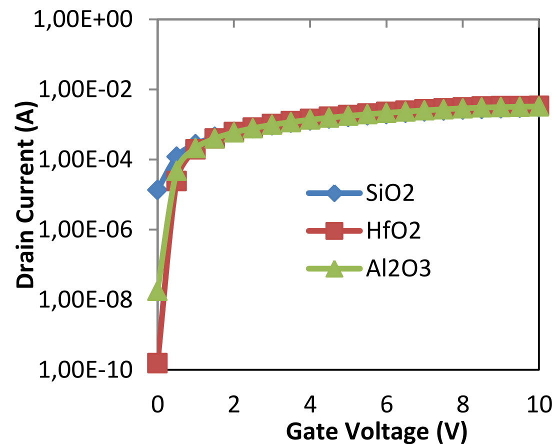

Fig. 7 - I_d vs V_g for different gate dielectric materials

Effect of Gate Metal

Type of gate metals greatly contribute to the device characteristics. The metals that have been employed for this purpose are Aluminium, Titanium and Gold. Also the use of metal stacks is a common practice. The work function of all these metals is different which gives them their unique properties. The work function of the metal is defined as the energy required to pull out an electron from the Fermi energy level to infinity.

First we consider the I_d vs V_g characteristics of the device in Figure 8. The drain voltage is kept at 5 V. This high value of V_d can actually give us an insight how well the gate metal is able to control the drain current under such conditions. It can be observed from the plot that when Al is used as the gate there is drain current of order – 4. But when Gold is used as the gate metal the order is reduced to – 15 at $V_g = 0$ V.

Figures 8 portray two interesting facets of the gate metal contact. If the gate metal to be used has a greater workfunction, then we have a better I_d vs V_g characteristic curve which points to the fact that the device is actually off when gate voltage goes below the threshold

voltage (steeper subthreshold curve indicates lower subthreshold current). But on the other hand, when the drain current vs workfunction is plotted it can be clearly observed that the drain current increases when the workfunction of the gate metal is reduced. So the gate metal is like a trade off factor. Whether we want better switching (steeper subthreshold slope) or better amplification (more drain current), would dictate the choice of gate metal.

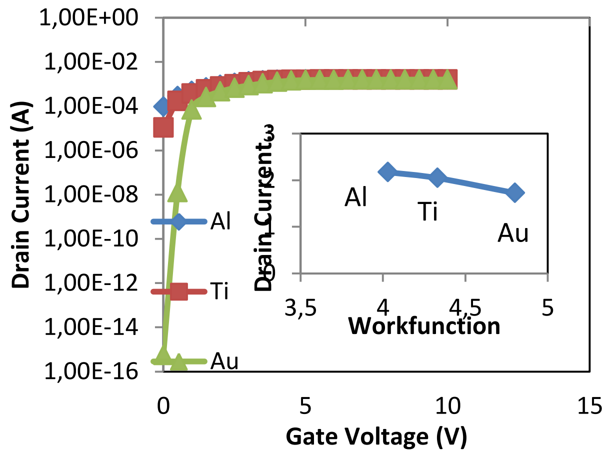

Fig. 8 - I_d vs V_g for different gate contact metals (inset shows Id vs workfunction of three different gate contact metals)

Effect of Gate Length

Now, the GaN nanowire has been considered at different gate lengths. Gate length is a very important factor for consideration owing to the continuous scaling down of the device. Drain current has been computed for three different devices with $L_g = 10$ nm, 20 nm and 30 nm respectively. Figure 9 clearly describes the relationship between varying gate lengths and the drain current at a constant gate voltage of 5V ($V_g = 5$ V).

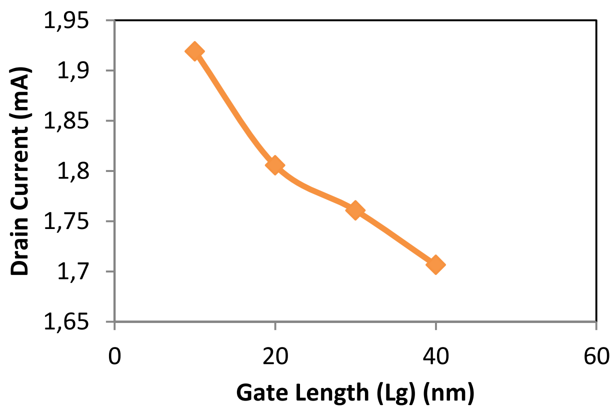

Fig. 9 - Variation of drain current with gate length

The above figure clearly delineates the mentioned relationship. It can be observed that the current decreases with an increase in gate length. One important fact, the slope of the line joining the drain currents at point 10 nm and 20 nm is more than that of the lines connecting other three points (where the slope can be construed to be linear). So the current difference at 10 nm and 20 nm gate length (about 0.1 mA) is more than that of 20 nm and 30 nm or 30 nm and 40 nm (about 0.05 mA). So, reducing the gate length below 10 nm substantially increases the current. Chances of the device failing at such short gate lengths at even high voltages would be difficult because of high value of band gap.

Device transconductance

Transconductance of a semiconductor device is quite an important characteristic wherein it signifies the amplification capability of the device at a certain value of parameters. Transconductance is given as:

$$g_m = \frac{dI_d}{dV_{GS}} \tag{3}$$

The above equation tells us how much the drain current changes when the input voltage is changed. Higher value of transconductance means that a small change in the input signal, V_{GS} brings a large change in the output current, I_d (large amplification). Small value of transconductance means smaller amplification capability.

As shown in the Figure 10, drain voltage has been kept constant at 10 V and gate voltage has been varied between – 2 V and 10 V and transconductance has been traced. It can be observed that the amplification property of the device with $L_g = 10$ nm goes down whereas that of $L_g = 20$ nm and 30 nm decreases at a slower rate. It is also seen from the figure that at $L_g = 10$ nm the maximum value of transconductance is comparable to those at 20 nm and 30 nm at lower gate voltages.

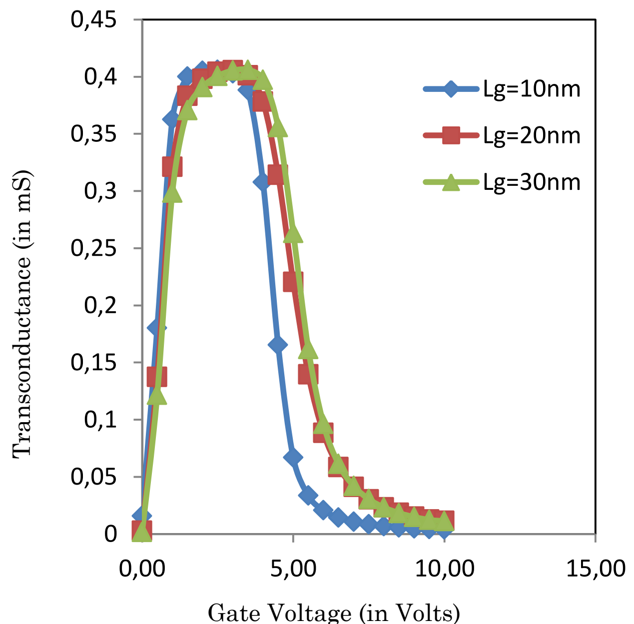

Fig. 10 - Transconductance of the device at three different gate length

Figure 11 shows the transconductance of the device at three different radius. It can be observed that highest transconductance is of the device with greater radius.

As seen from Figure 10 and 11, flatter g_m-V_g curve results in higher third order intercept point (IIP3) value which indicate better linearity performance of the scaled device.

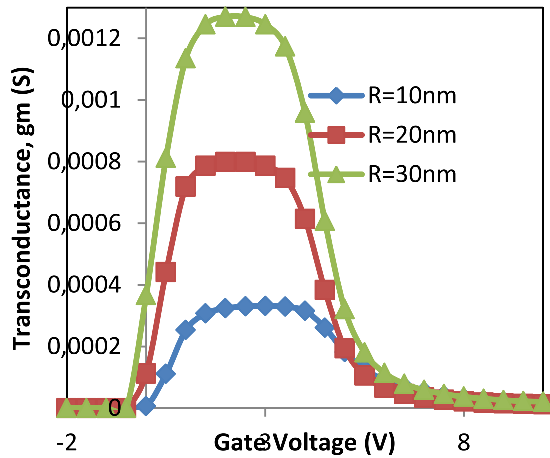

Fig. 11 - Transconductance of the device at three different nanowire radii

Table I shows the comparison of different types of nanowires available

Gate Stack (1 nm/4 nm layers)

The comparison table includes different type of nanowires including Si, Poly-Si, InGaAs and GaN nanowires. Also several types of gate geometries and experimental as well as simulated results have been considered. The important parameters like ON current, subthreshold slope and DIBL have been compared. A high I_{on}/I_{off} achieved in the present case show the usability of the GaN nanowire transistor for digital applications

4. CONCLUSIONS

Nanoscale GaN transistor has been designed and simulated in the cylindrical coordinate. Gate length of 10nm and nanowire radius of 10nm has been used in the analysis. At such low dimensions quantum mechanical analysis of the device characteristics has been done. The effect of high *k* dielectric materials like HfO_2 and Al_2O_3 has been considered. Also the effect of different metal gates on the drain current of the device has been considered. The device has been operated at high voltages up to 40V. This justifies the utilization of this nanowire transistor in high voltage applications. The simulation model can further be extended to obtain the capacitance-voltage and small signal characteristics of the GaN nanowire transistor.

Table II – Comparison of different nanowire transistors

X	Ref [24]	Ref [25]	Ref [26]	Ref [27]	Ref [28]	Ref [18]	Ref [18]	This work	This work
Nanowire type	Si	Poly-Si	Poly-Si JNT	InGaAs	Si	GaN	GaN	GaN	GaN
NW cross sectional type	Rectangular-like	Tri-gate	GAA	Rectangular	GAA - circular	Triangular	Triangular	GAA-cylindrical	GAA-cylindrical
L_g (nm)	65	230	80	50	8	50	20	20	10
EOT or T_{ox} (nm)	3	5	NA	5*	4	13	10	2	2
V_d (Volts)	1	1	0.1	0.5	1.2	4	4	4	4
SS (mV/dec)	70	98	61	110	75	91	112	60	75
DIBL (mV/V)	62	NA	<10	NA	22	40	34	20	50
I_{on}/I_{off}	~ 1×10^6	~ 5×10^4	~ 1×10^7	~ 2×10^3	~ 1×10^6	~ 1×10^8	~ 1×10^8	~ 1×10^8	> 1×10^8

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