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Short Communication

Features of Formation of Ohmic Contacts and Gate on Epitaxial Heterostructure of AlGaN / GaN High Electron Mobility Transistor

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Reported about study of processes of formation of Ti / Al / Ni / Au ohmic contacts to heterostructures AlGaN / GaN and gate Ni / Au. Investigated of process recess the semiconductor layer for minimum resistance of ohmic contact – 0.4 Ohm·mm. Studied influence of encapsulation ohmic contacts on their surface morphology.

Keywords: Gallium nitride, Ohmic contacts, Encapsulation, Gate AlGaN / GaN HEMT.

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1. INTRODUCTION

Modern trends in electronics have focused on the miniaturization of semiconductor devices. For this contributes to the use of wide-gap materials $A^{III}B^{V}$, and more and more wide-gap materials III-N types, in the field of high-power microwave electronics application. Due to the large width of band gap, obtained the high power density. In particular, devices made on heteroepitaxial of AlGaN / GaN structures, give several times greater power density than the conventionally used gallium arsenide devices [1].

Productions of gallium nitride MISs or transistors, requires a special approach in the formation of some of its elements, in particular the ohmic contacts and gate.

Making an ohmic contact is a difficult task, since the width of band-gap of this type of semiconductor by more than two times higher than gallium arsenide. When creating ohmic contacts to heterostructures AlGaN / GaN having difficulty to obtain low resistance and low surface roughness of the metal layer after the annealing process.

Traditionally, formation of ohmic contacts for metallization is used based on titanium and aluminum, then sprayed metal layer which serves as a barrier between the aluminum and the upper metallization - gold. However, it is known from the literature a great variety of metalization systems, which provide a low resistance, and smooth morphology of the upper metal layer [2].

Recess used to reduce the specific resistance of ohmic contacts. As it is known from literature that dependence between the specific contact resistance and the depth of the recess, is a parabola, Fig. 1.

The process of rapid thermal annealing ohmic contacts is need of special attention. Used as a single-stage or multistage annealing modes, wherein the diffusion processes and chemical reactions differ dramatically.

In order to maintain of the morphology and geometry of the ohmic contacts used encapsulation. It is deposition of dielectric layer on the ohmic contacts immediately before the process of annealing metal layers, which greatly reduces the roughness, and maintains form of the contact.

The process of formation the gate has a strong influence on the most important characteristics of the transistor, such as the steepness, the value of the saturation current, breakdown voltage, voltage cutoff.

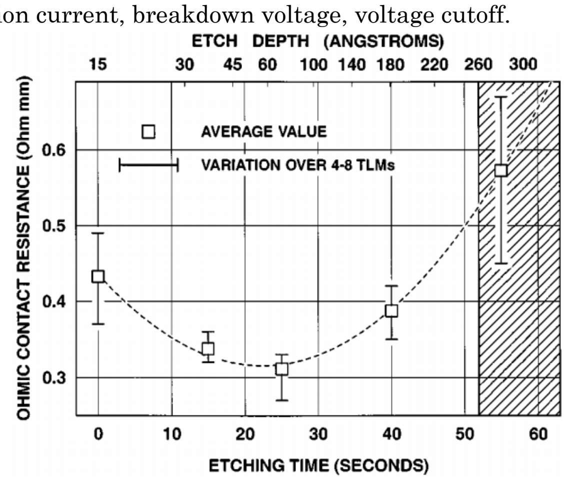

Fig. 1 – Dependence of resistivity ohmic contacts on the etching depth. The shaded part - the area of two-dimensional electron gas [3]

The most suitable metal for forming a Schottky contact to the AlGaN are Pt and Ni, as they have a maximum height of the potential barrier of 1.55 and 1.05 eV respectively, but since the more expensive Pt material, that traditionally, for forming a Schottky contact using Ni [4].

2. EXPERIMENT

At the stage of researching the process of forming ohmic contacts the dependances of resistance ohmic contacts on the resistivity of the deposited thickness of metals, annealing temperature and the depth of the recess were obtained.

Formation of the gate performed with different methods surface pretreatment of the semiconductor: dry (RIE BCl3) and wet (H2O : HCl 1 : 1) and were conducted on a different recess depth of the gate and passivation.

As an initial material used heteroepitaxial structure of AlGaN / GaN (Fig. 2) on sapphire substrates, they were grown in the company "Elma-Malachite".

On the test structures was formed mesa isolation by etching in a plasma mixture of Cl2 / BCl3 gas in an inductively coupled plasma installation «Corial 200IL», as this etching mode is used to recess under the ohmic contacts and gate.

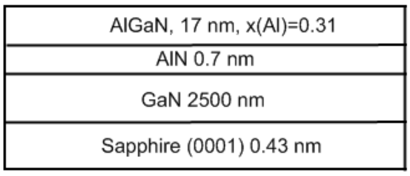

Fig. 2 – Schematic illustration of used heteroepitaxial structure

Spray metallization for ohmic contacts (Ti / Al / Ni / Au) and the gate (Ni / Au) was carried out by vacuum thermal evaporation.

A Rapid thermal annealing of the ohmic contacts were carried out on the installation «As-one». Annealing process carried out in two stages, the first stage - heating up to 600 °C for 30 seconds, then heating to a predetermined temperature for 40 seconds.

The measurements were realized using TLM (Transmission Line Method), linear matrix TLM elements were formed , measurements were performed on the probe station.

For the encapsulating and passivation layer used dielectric layer deposited of Si3N4 on the installation PECVD «Corial D250».

3. RESULTS AND DISCUSSION

3.1 Formation of Ohmic Contact

In the experiment using of metal layers with different thickness to form ohmic contacts. Different annealing temperature is also used. The results are given in Fig. 3.

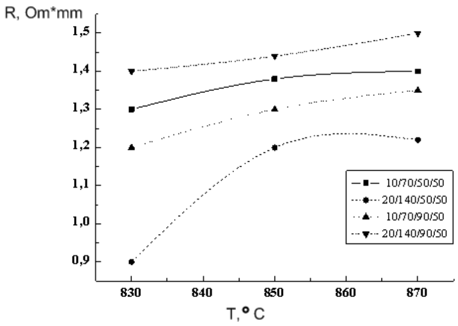

Fig. 3 – Dependent resistance ohmic contacts on the composition of the metal layers of Ti / Al / Ni / Au and the annealing temperature

As can be seen from Fig. 3, at higher annealing temperatures, and also increases the resistivity ohmic contact. Minimum resistance was obtained for the composition of the metal layers of Ti / Al / Ni / Au with a thickness 20/140/50/50 nm. respectively, at a temperature of annealing 830 °C for 40 seconds without recess. At this stage, research is difficult to explain such a dependence of the resistance ohmic contacts on the conditions of their preparation. These values of resistivity more than the literature (0.2-0.7 Om·mm), therefore, requires an even greater decrease in the resistance.

The recess for ohmic contacts (recess) were used to further reduce the resistivity ohmic contacts. Etching the semiconductor layer was carried out in an inductively coupled plasma in a mixture of Cl2 / BCl3 gas.

As can be seen from Fig. 4, the resistivity of ohmic contact decreases as it approaches the border region of the two-dimensional electron gas, then abruptly increases at the intersection of the conductive channel heterostructure. This may be explained as follows. Consider a semiconductor layer between the metallization of the ohmic contacts and the two-dimensional electron gas as a resistor, which influence to the specific contact resistance. By reducing its thickness, there is a reduction of resistance in ohmic contact. When occurrence of lower metal layers below the area of the two-dimensional electron gas, the contact resistance increases rapidly, since the formation of the reaction products of low-resistance occurs below the conducting channel and a good ohmic metal contact with the two-dimensional electron gas does not occur.

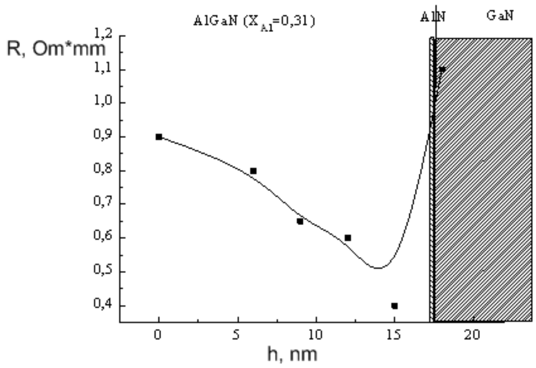

Fig. 4 – Dependence of resistivity ohmic contacts Ti / Al / Ni / Au 20/140/50/50 nm on of depth of recess, at annealing temperature of 830 °C for 40 seconds

Thus it was obtained the minimum resistance ohmic contact Ohm·0.4 mm.

In order to improve the morphology of the ohmic contacts after annealing, encapsulation method was used. It consists in the fact that before the rapid thermal annealing process the entire surface of wafer is coated with a dielectric layer. Thus, the shape of the metal layers of ohmic contacts is fixed on one side surface of the semiconductor and the other dielectric film and therefore it is safied at high temperature exposure.

Fig. 5 shows images of ohmic contacts before and after annealing. It is seen that without of dielectric layer the morphology and geometry of the metal layers is cracking. When using of the silicon nitride layer 100 nm thick contact geometry is retained, but the dielectric layer is destroyed. Also, therea is "cloud" formated. The resistance value is then equal to 0,5 ± 0,07 mm·Ohm.

When using a thinner dielectric – 30 nm, the destruction of the encapsulating layer does not occur, geometry of contact is completely preserved, and violation of the surface morphology is not essential. The resistance value is then equal to 0.53 ± 0,07 mm·Om.

3.2 Formation Gate

During experiment of the formation of the transistor gate were obtained the results given in Table 1.

Saturation current density as transconductance is maximum at the wet treatment, while at a plasma treatment saturation currents are reduced due to the presence of radiation defects on semiconductor surfaces.

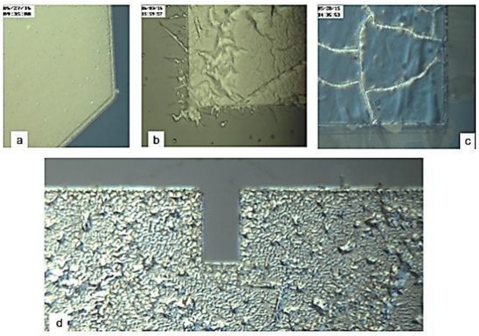

Fig. 5 – Appearance of ohmic contacts (× 50) before and after annealing at $T = 850$ °C 40 using encapsulation of silicon nitride: a) the original sample to rapid thermal annealing; b) without encapsulation; c) encapsulation of 100 nm; d) Encapsulation of 30 nm

Table 1 – Characteristics of the transistor at different surface preparation of AlGaN semiconductor

	Without passivation				Passivation 30 nm Si_3N_4			
	HCl	BCl_3	Recess 4 nm	Recess 8 nm	HCl	BCl3	Recess 4 nm	Recess 8 nm
J, A/mm	1	0,7	0,58	0,51	0,95	0,8	0,56	0,5
S, mS/mm	200	160	180	170	180	180	170	170
$U_{пр}$, V	100	100	110	112	92	90	100	102

Passivation gate leads to an overall reduction of the saturation currents and decries transconductance.

By increasing the depth of the recess, there is a growth of the breakdown voltages and passivation leads to a slight decrease in the breakdown voltage.

CONCLUSION

In the result of this work was formed an ohmic contact on the heterostructure AlGaN / GaN with minimal resistance $0.53 \pm 0{,}07$ Om·mm using a sputtering system Ti / Al / Ni / Au (20/140/50/50 nm), an annealing temperature of 830 °C and encapsulation 30 nm of silicon nitride.

Application of thin layers of dielectric for the encapsulation at the formation of ohmic contacts, the geometry and morphology of the ohmic contact were saved. The use of thick dielectric layers leads to the destruction of the dielectric film when exposed to high temperature, due to the elastic stresses in the film of silicon nitride. The thickness of the encapsulating layer has no significant influence on the specific resistance of the ohmic contact.

The analysis of transistor characteristics obtained after the formation of the gate, identified optimal surface preparation before the gate formation is wet processing in mixture HCl : H2O (1 : 1) 3 min, in this case obtained the best device characteristics: Current density – 1 A/mm, the transconductance – 200 mS/mm and breakdown voltage – 100 V.

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