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Comparison of Three Dimensional Partially and Fully Depleted SOI MOSFET Characteristics Using Mathcad

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In this Paper, comparison of three Dimensional characteristics between partially and fully depleted Silicon-On-Insulator (SOI MOSFET) is presented, this is done through 3D device modeling using mathcad, based on the numerical solution of three dimensional Poisson's equation. Behavior of Various Parameters like Surface Potential, Threshold Voltage, Electric field and Drain current are presented in this paper.

Keywords: Silicon on insulator (SOI), Poisson's Equation, Front surface potential, Threshold voltage, Electric field, Drain Current.

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1. INTRODUCTION

High performance and digital circuits are the current need of electronics industries, Earlier Bulk MOSFET was considered fit for the electronics industry and to satisfy the Moore's law [15], which states that performance of transistors in a dense integrated circuit doubles approximately every two years. Primary method to increase productivity and performance is scaling, But due to Short channel effects and junction leakage current with scaling, it is difficult to follow moore's law with bulk CMOS. So the need to SOI technology arises [17].

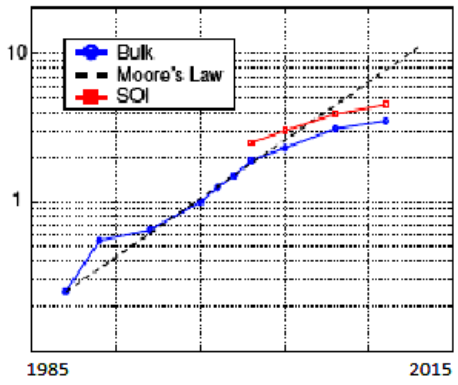

Fig. 1 – Evolution of CMOS Technology with moors Law

2. NEED OF SILICON ON INSULATOR (SOI) MOSFET

SOI Technology is the solution to the limitation of the CMOS bulk technology against various impacts due to Scale down the device.

There are various characteristics of SOI MOSFET due to which it would be beneficial to switch to SOI MOSFET technology. The main advantages of SOI technology are the following.

- Latch can be eliminated as there are no parasitic bipolar devices because of SOI Layer.
- Due to the insulation layer above the substrate, these devices have smaller leakage current.
- High speed of operation due to the very low capacitance between device and substrate.
- Power dissipation of SOI MOSFET is small, because operated at lower voltages and current levels [2].

3. SILICON ON INSULATOR (SOI) MOSFET

Structure of SOI MOSFET is almost similar to that Bulk CMOS, But an insulation layer is inserted underneath the device on the silicon substrate.

On the Basis of the thickness of the SOI layer, there are Two types of SOI MOSFETS [17]:

1. Partially Depleted SOI MOSFET;
2. Fully Depleted SOI MOSFET.

In Partially Depleted SOI MOSFET, SOI layer Thickness is kept more than the Maximum depletion width of the gate. A technology based on this principle is called a partially depleted SOI Technology. PD SOI Structure is as shown in Fig 2.

Top Silicon Layer is Approximately 50 ~ 200 nm Thick, as per the requirement of the design, Following four parameters Make PDSOI Technology as an essential IC Technology for industry compare to Bulk CMOS. (1) Low Power, Can operate at low power with the same performance. (2) High performance, Provides Performance gain of 20-40 % [16]. (3) Easy Process (4) Technology mixing. But the major problem with PD SOI is floating body effect.

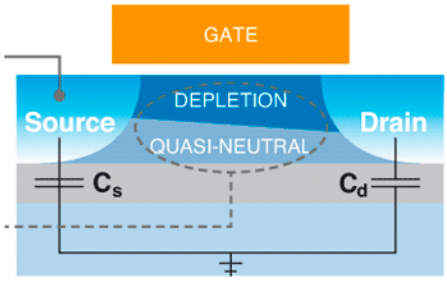

Fig. 2 – Partially Depleted SOI MOSFET Structure [14]

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Table 1 – PD and FD SOI Structure at a Glance

	Structural differences	Advantages
Partial Depletion	1. Doped Channel 2. Top Silicon 50 ~ 90 nm thick 3. Insulating Box Layer is typically 100 to 200 nm thick	1. Well Understood 2. Industrial Proven 3.Easy to Manufacture. 4. Can leverage floating body for performance gain or memory applications.
Fully Depletion	1. Un doped or lightly doped Channel 2. Top Silicon 5 ~ 20 nm thick 3. Insulating Box Layer may be ultra thin 5 to 50 nm	1. Leakage and power consumptions are very low 2. for undoped channel, random voltage fluctuations can be minimized 3. free from floating body effects

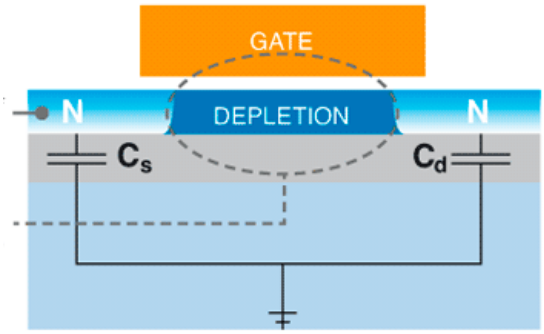

Fig. 3 – Fully Depleted SOI MOSFET Structure [14]

In fully depleted SOI MOSFET silicon thickness is very less hence channel is fully depleted from the majority carriers. ie SOI layer is thinner than the depletion width of the device [14].

Top silicon layer is approximately 5 ~ 20 nm. Thick, as per the requirement of the design silicon under the gate is very thin so, fully depleted by mobile carriers.

In FD SOI technology, floating point effect can be eliminated as there is no Neutral region of MOSFET for charge [14]. FD SOI Structure is shown in Fig 3 and Comparison points between PD SOI and FD SOI are given in Table 1.

4. DEVICE MODELING

Fig. 4 illustrates a three-dimensional view of a typical MOSFET structure with corresponding device dimensions. The source-SOI film and drain-SOI film junctions are located at $y = 0$ and $y = Leff$, respectively, where, *Leff* is the effective channel length. The front and back Si-SiO interfaces are located at $x = 0$ and $x = t_s$, where t_s is the SOI film thickness. t_{oxf} and t_{oxb} are the front and the back gate oxide thicknesses, respectively, where the applied potential to the front and back gates are V_{gf} and V_{gb}.The vertical and the lateral directions are defined as x and y, respectively, while the direction along the width of the transistor is defined as z. The sidewall Si-SiO interfaces are located at $z = 0$ and $z = W$.

In general, in order to analyze this structure, we have Poisson's equation, which is as below.

$$\frac{d^2}{dx^2}\psi(x,y,z)+\frac{d^2}{dy^2}\psi(x,y,z)+\frac{d^2}{dz^2}\psi(x,y,z)=\frac{q\cdot N_a}{\varepsilon_{si}} \quad (1)$$

In order to solve equation (1), it is separated into 1D Poisson's equation, 2-&3-D Laplace equation as:

$$\frac{d^2}{dx^2}\psi 1(x)=\frac{q\cdot N_a(x)}{\varepsilon_{si}} \quad (2)$$

$$\frac{d^2}{dx^2}\psi(x,y)+\frac{d^2}{dy^2}\psi_s(x,y)=0 \quad (3)$$

$$\frac{d^2}{dx^2}\psi_v(x,y,z)+\frac{d^2}{dy^2}\psi_v(x,y,z)+\frac{d^2}{dz^2}\psi_v(x,y,z)=0 \quad (4)$$

Where, $\Psi i = \Psi l(x) + \Psi s(x, y) + \Psi v(x, y, z)$ (A)

Main Equation can be obtained by finding separate solutions for Ψl, Ψs and Ψv and finally putting in Equation (A).

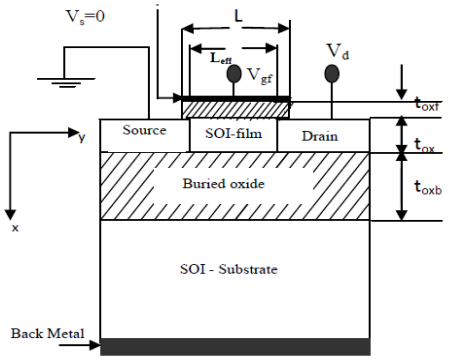

Fig. 4 – Cross sectional view of double gate SOI MOSFET along channel length

5. RESULT AND DISCUSSION

Modeling has been done for Both PD and FD SOI MOSFET and comparison between the PD and FD SOI MOSFET'S for Surface Potential, Threshold Voltage, Electric Field with respect to Channel Length is given here, Variation Comparison for Drain current with respect to Drain voltage, gate source voltage are also presented as below.

5.1 Surface Potential

The variation of front surface potential at the front Si-SiO_2 interface (i.e., $x = 0$) of a PD and FD SOI MOSFETS for different values of channel length is shown in Fig. 5. which shows that FD SOI MOSFET follows better surface potential characteristic as com-

pare to PD SOI MOSFET.

In the Fig. 5, we determine the variation of front surface potential for n-channel SOI MOSFETs along the different values of channel length at the front Si-SiO_2 interface and $z = w/2$. The values we have taken here are: $t_{oxf} = 3$ nm, $t_{oxb} = 400$ nm, $N_A = 1 \times 10^{17}/cm^3$ at $V_{gf} = V_{gb} = 0$ & $V_{ds} = 1.5$ V.

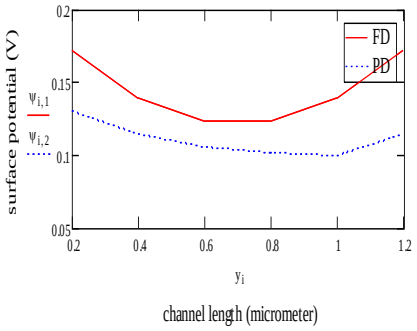

Fig. 5 – Variation of the front Surface Potential along channel length for PD and FD SOI at the front Si-SiO_2 interface

5.2 Threshold Voltage

The Threshold voltage of the short channel MOSFET [5, 11] is defined as the gate voltage at which the minimum surface potential in the channel is the same as the channel potential at threshold for a long channel device, i.e., at threshold.

The variation of threshold voltage with respect to Channel length for PD and FD SOI MOSFET is shown in Fig. 6.

$$VTF = V_{gf} \text{ when } \Psi(0, y, W/2) = 2\varphi_b \qquad (B)$$

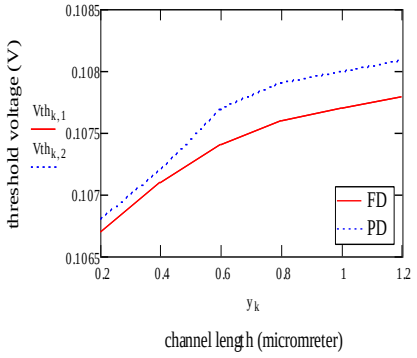

Fig. 6 – Variation of threshold voltage with respect to channel length in PD and FD SOI MOSFET

From Fig. 6, It is evident that FD SOI MOSFET is having Lower threshold voltage characteristic as compare to PD SOI MOSFET along with the channel length. Hence FD SOI will be less affected by short channel effects.

5.3 Elctric Field

The electric field distribution along the channel length for PD and FD SOI MOSFET is given as below, which shows that FD SOI MOSFET follows higher electric field characteristic as compare to PD SOI MOSFET.

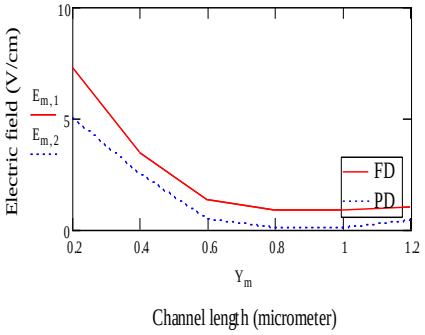

Fig.7 – Variation of electric field along the length of channel for PD and FD SOI MOSFET

5.4 Drain Current

Drain Current is a very important parameter to determine the current capacity of any device, this can be considered as a output characteristics of a device. Drain Current Characteristics comparison along with the Drain voltage for PD and FD SOI MOSFET can be shown as below in Fig. 8, This Shows that PD SOI MOSFET is having Kink Effect whereas FDSOI MOSFET is free from any kind of Kinking effect

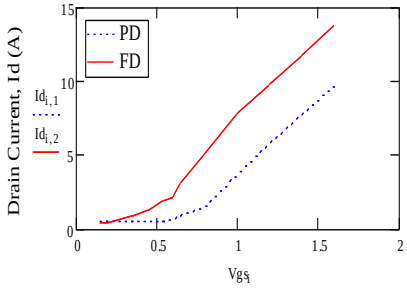

Fig. 8 – Variation of Dain Current with respect to drain to source voltage in PD and FD SOI MOSFET

Drain Current variation along with gate to source voltage for PD and FD SOI MOSFET, which can also be assumed as input characteristic are shown in Fig. 9. It can be seen here that PD SOI MOSFET shows less Drain Current as compare to FDSOI MOSFET for same value of V_{gs}.

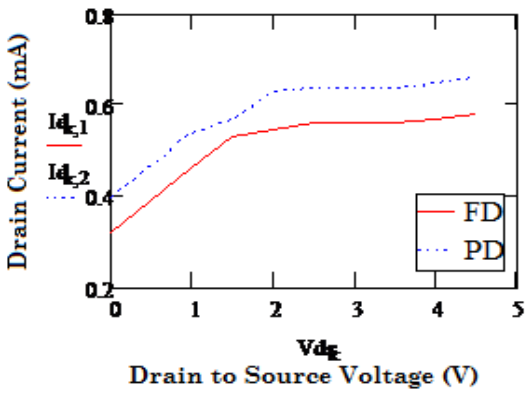

Fig. 9 – Variation of Dain Current with respect to gate to source voltage in PD and FD SOI MOSFET

6. CONCLUSION

A 3D modeling and comparison for PD and FD SOI MOSFET has been shown in the paper, this is based on the solution of the Poisson equation. Surface potential, threshold voltage, electric field along with the channel length & Drain Current variations with drain voltage & gate source voltage are given which shows that FD SOI Performance is giving better Performance results as compare to PD SOI MOSFET.

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