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Temperature Dependent IR-Drop Analysis in Graphene Nanoribbon Based Power Interconnect

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The paper proposes a temperature dependent resistive model of graphene nanoribbon (GNR) based power interconnects. Using the proposed model, IR-drop analysis for 16nm technology node latest by ITRS is performed. For a temperature range from 150 K to 450 K, the variation of resistance of GNR interconnect is ~ 2-5 × times lesser than that of traditional copper based power interconnects. Our analysis shows that GNR based power interconnects can show ~ 2-3 times reduction in Peak IR-drop as compared with copper based interconnects for local, intermediate and global interconnects.

Keywords: Graphene nanoribbon (GNR), Temperature, Peak-IR-Drop, Effective-MFP (mean free path), Interconnect.

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1. INTRODUCTION

IR-drop has been one of most important challenges of power interconnect in sub-nanometer design [1]. It becomes even more challenging for the high density and high performance designs in which it has adverse effects on timing. The increase in chip operating temperature has two-fold effects on timing. Firstly, it increases the interconnect resistance which in turn increases the interconnect delay. Secondly, due to the increase in resistance there is more IR-drop which also increases the gate delay. Therefore, it is very essential to analyze the effects of temperature on IR-drop in sub nanometer designs, since the resistivity of the traditional copper based interconnects increases significantly in nanometer dimensions [2]. GNR is one of the most promising materials for interconnect modeling for future generation technologies [2, 3] due to its excellent properties compared with copper in nanometer dimensions. Recent studies [3-9] on GNR show its superiority over the traditional copper based interconnect. However, to the best of our knowledge no investigation has been performed to analyze the effects of the temperature on IR-drop in GNR interconnect. In this paper, we have proposed a resistive model of graphene nanoribbon (GNR) power interconnect, which is dependent on temperature. Using the proposed model, we have analyzed the IR-drop in GNR based power interconnects. The rest of the paper is organized as follows. Section-II presents the proposed temperature dependent resistive model of GNR interconnect. The results of IR-drop analysis and conclusions are presented in the Sections-III and IV, respectively.

2. TEMPERATURE DEPENDENT RESISTANCE MODEL OF GNR INTERCONNECTS

Due to the presence of large quantum resistance of a monolayer-GNR, a multilayer-GNR structure is proposed for modeling nanointerconnect to utilize the long mean free path as depicted in Fig. 1a. Here, width, thickness, height of multilayer-GNR structure are represented by w, t, ht. The separation between two multilayer GNR structures is sp. We have considered $w = 16$ nm and $t = 32$ nm for 16 nm ITRS technology node [2]. Fig. 1b shows the 2D-honeycomb lattice structure of single layer-GNR.

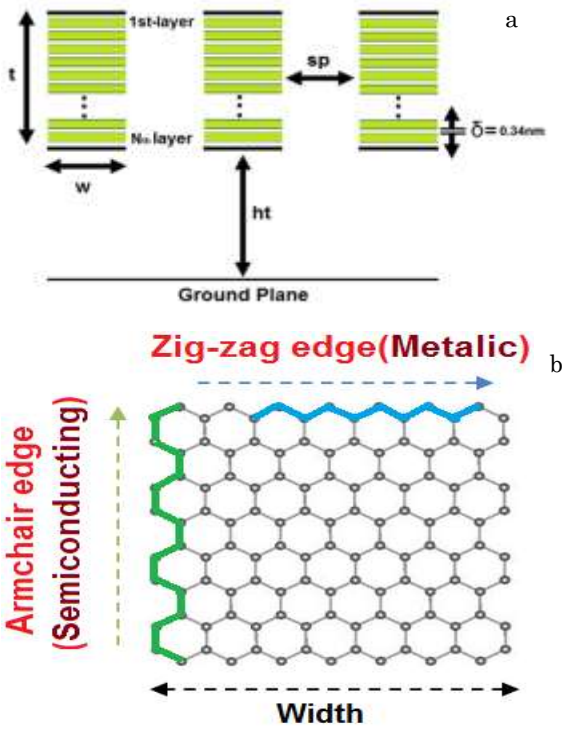

Fig. 1 – Tri-interconnect model of multilayer-GNR structure (a) and 2D honeycomb lattice structure of single layer-GNR (b)

Total number of layers in the multilayer GNR interconnect is reported in as [4]

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$$N_{layer} = \left(1 + Integer\left[\frac{t}{\delta}\right]\right) \quad (1)$$

The spacing (δ) between two graphene layers is 0.34 nm which is known as van der walls gap [7]. Using (1) we obtain the number of layers as $N_{layer} \cong 95$ for 16 nm technology node. The total resistance of MLGNR (multilayer graphene nanoribbon) interconnect is given by [7].

$$R_{Total-MLGNR} = R_Q(1 + \frac{l_{MLGNR}}{\lambda_{effective}}) \quad (2)$$

where l_{MLGNR} is the length of MLGNR based interconnect and $\lambda_{effective}$ is effective-MFP of MLGNR. Here, effective-MFP is a function of temperature which is modeled in this section. The quantum resistance (R_Q) is expressed as [4]

$$R_Q = \left[\frac{\left(\frac{h}{2.e^2}\right)}{N_{ch}.N_{layer}}\right] \Rightarrow \left[\frac{12.94k\Omega}{N_{ch}.N_{layer}}\right] \quad (3)$$

In (3) N_{ch} is the total numbers of conducting channels in monolayer-GNR, N_{layer} is the number of layers present in multilayer GNR, h is Planck's constant, and e is charge of an electron. The total conducting channels present in monolayer-GNR is expressed in [7].

$$N_{ch} = \sum_{i=1}^{n_C}[1 + e^{\left(\frac{(E_{i,n} - E_{Fe})}{k_B T}\right)}]^{-1} + \sum_{i=1}^{n_V}[1 + e^{\left(\frac{(E_{Fe} + E_{i,h})}{k_B T}\right)}]^{-1} \quad (4)$$

where 'i' is a positive integer variable, E_{Fe} is Fermi-energy, T is room temperature, k_B is Boltzmann's constant, n_c and n_v are known as total number of conduction and valance sub-bands. Here, $E_{i,n}$ and $E_{i,h}$ are electron and hole energy for i^{th} sub-band as expressed as [7]

$$E_i = \frac{ihv_F}{2w} \quad (5)$$

The total number of channels (N_{ch}) in metallic GNR is equal to 6 [4-5, 7]. The effective MFP of each layer of GNR depends on three important parameters: electron scattering (λ_e), acoustic phonon scattering (λ_{ap}) and remote interfacial phonon scattering (λ_{rip}). Electron scattering does not depend on the temperature, but the other two parameters vary with temperature. The electron scattering λ_e can be expressed as [8]

$$\lambda_e = \lambda_{defect} + w\sum_{a=1}^{N_{ch}}\sqrt{(\frac{N_{ch}}{a}) - 1} \quad (6)$$

Here, λ_{defect} is a special kind of MFP of graphene. This MFP is due to the defects present in graphene. The value of λ_{defect} is assumed to be 1μm [8]. The acoustic phonon scattering (λ_{ap}) is expressed as [8]

$$\lambda_{ap} = \frac{h^2\rho_s v_s^2 v_f^2 w}{\pi^2 D_A^2 k_B T} \quad (7)$$

In (7), v_f is the Fermi velocity of GNR (= 8×10^5 m/s), v_s is the sound velocity of GNR (= 2.1×10^4 m/s), D_A is deformation potential due to acoustic phonon, k_B is Boltzmann constants, ρ_s is 2D mass density in graphene, and T is known as room temperature. The remote interfacial phonon scattering can be expressed as [8]

$$\lambda_{rip} = \alpha E_F^{1.02} W(e^{\frac{E_0}{kT}} - 1) \quad (8)$$

Here, α is the fitting parameter, E_F is the Fermi potential (= 0.2 eV), and E_0 = 104 mV. The temperature dependent effective MFP of GNR is given by applying Matthiessen's rule [4]

$$\lambda_{effective}^{-1} = \lambda_e^{-1} + \lambda_{ap}^{-1} + \lambda_{rip}^{-1} \quad (9)$$

Substituting the effective MFP of MLGNR in (2) we obtain the temperature dependent resistance of MLGNR.

3. RESULTS

Using the temperature dependent resistance model as discussed in previous section, we have calculated the resistance for different interconnect length and different temperature. In Fig. 2 we have shown the temperature dependent resistance of GNR and Cu interconnect for different interconnect length (5 μm to 50 μm) for 16 nm technology node. GNR shows ~ 2-5 × less resistance than that of Cu as shown in Fig. 2. With the increase in temperature, the effective mean free path reduces, and hence the scattering induced ohomic part of the total resistance of GNR increases. The IR-drop analysis is performed in GNR and Cu interconnects for 5 μm (local), 20 μm (intermediate) and 50 μm (global) interconnect lengths. The analysis is per-formed using equivalent circuit model shown in Fig. 3 [9]. In Fig. 3, ten identical CMOS inverters are connected in series with temperature dependent resistance for both GNR and Cu. In our analysis, we have assumed the supply voltage as 0.7 V, the input-pulse switches from 0 to 0.7 V for all stages and input-pulse rise and fall time is considered as 100 ps.

The CMOS inverters are designed for 16nm ITRS technology node using the SPICE models from predictive technology model [10]. The CMOS model parameter for 16 nm technology as shown in Table 1. The circuit simulations for CMOS inverter circuit are performed using the Cadence spectre simulator. All the inverters are switched simultaneously so that they draw current from the power supply. As a result the power supply voltage decreases progressively away from the power pad. The decrease in power supply causes increase in propagation delay through the gate. As the temperature increases, the resistance of the power interconnects increases which causes more interconnect delay. With temperature as the IR-drop increases, the gates suffer more delay problem. Therefore, increase in temperature has twofold increase in delay: one due to increase in interconnect (RC) delay and the other due to increase in IR-drop. Figs.4 through 6 illustrates the IR-drop in GNR and Cu interconnects for local, intermediate, and global lengths. It is observed that the Peak IR-drop increases with the increase in temperature both for GNR and Cu interconnects but GNR shows

~ 2-3× less Peak IR-drop than Cu at local, intermediate and global lengths.

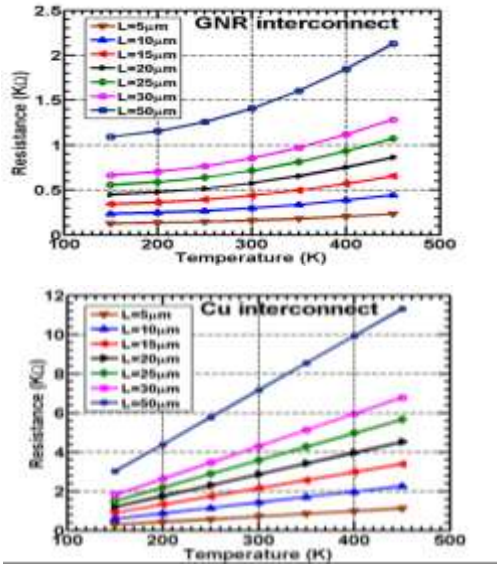

Fig. 2 – Resistance vs. temperature plot for GNR and Cu interconnect at 16 nm technology

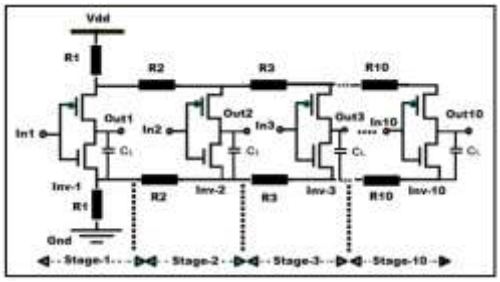

Fig. 3 – Schematic circuit used for power supply voltage drop analysis

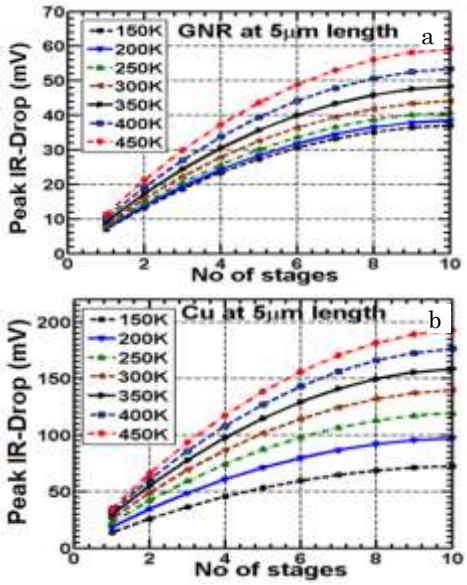

Fig. 4 – Peak IR-drop vs. No of Stages at different temperature for 5 μm length for GNR interconnect (local level interconnect) (a) and peak IR-drop vs. No of Stages at different temperature for 5 μm length for Cu interconnect (local level interconnect) (b)

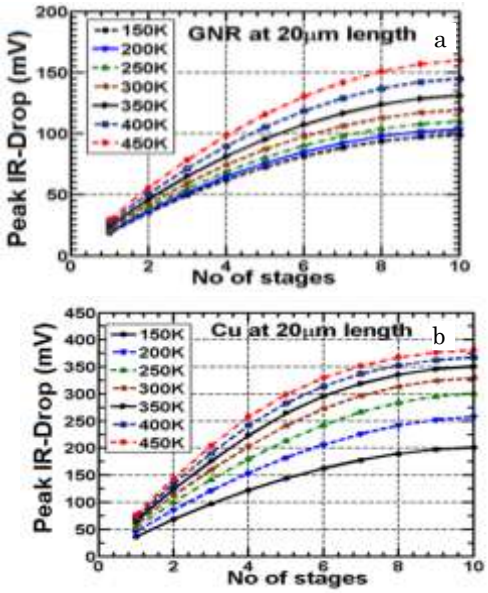

Fig. 5 – Peak IR-drop vs. No of Stages at different temperature for 20 μm length for GNR interconnect (intermediate level interconnect) and peak IR-drop vs. No of Stages at different temperature for 20 μm length for Cu interconnect (intermediate level interconnect) (b)

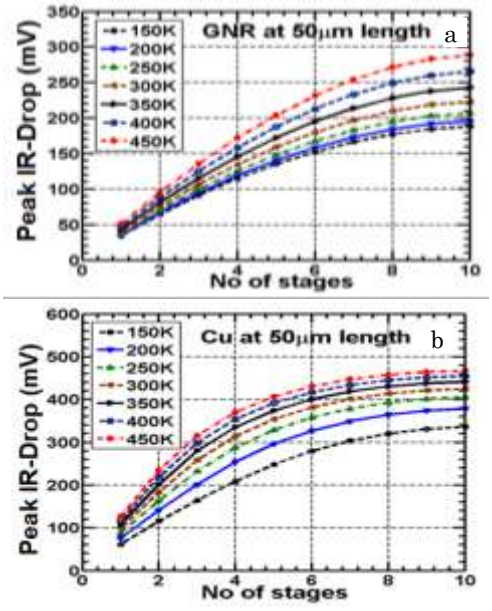

Fig. 6 – Peak IR-drop vs. No of Stages at different temperature for 50 μm length for GNR interconnect (global level interconnect) (a) and peak IR-drop vs. No of Stages at different temperature for 50 μm length for Cu interconnect (global level interconnect) (b)

Table 1 – 16 nm PTM CMOS Model Parameters

Model Parameters [10]	*n*-MOS (Si)	*p*-MOS (Si)
Channel Length (L)	16 nm	
Channel Width (W)	64 nm	128 nm
Threshold Voltage(V_{TH0})	0.47 volt	– 0.43 volt
Dielectric Constant (ε_{ox} for SiO_2)	$\varepsilon_{ox} = 3.9 \times \varepsilon_0$, Where $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m	
Oxide Thickness(t_{ox})	0.95 nm	1 nm
Gate Oxide Capacitance (C_{ox})	0.29 fF	0.28 fF
Junction Depth(X_j)	5 nm	

4. CONCLUSIONS

In this work, we have presented a temperature dependent resistive model of GNR interconnect and analyzed the effect of temperature on power supply voltage drop (IR-drop). It is observed that with the increase in temperature, the resistance is increased for both GNR and Cu, but GNR shows significantly less increase than the Cu interconnects (~ 2-5 × times lesser), which exhibits less power supply voltage variation and hence less impact on the timing of the circuits. It also reduces the power dissipation of GNR based power interconnects as compared with Cu.

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