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Impact of Scaling Gate Insulator Thickness on the Performance of Carbon Nanotube Field Effect Transistors (CNTFETs)

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As scaling down Si MOSFET devices degrade device performance in terms of short channel effects. Carbon nanotube field effect transistor (CNTFET) is one of the novel nanoelectronics devices that overcome those MOSFET limitations. The carbon nanotube field effect transistors (CNTFETs) have been explored and proposed to be the promising candidate for the next generation of integrated circuit (IC) devices. To explore the role of CNTFETs in future integrated circuits, it is important to evaluate their performance. However, to do that we need a model that can accurately describe the behavior of the CNTFETs so that the design and evaluation of circuits using these devices can be made. In this paper, we have investigated the effect of scaling gate insulator thickness on the device performance of cylindrical shaped ballistic CNTFET in terms of transfer characteristics, output characteristics, average velocity, g_m/I_d ratio, mobile charge, quantum capacitance/insulator capacitance, drive current (I_{on}), I_{on}/I_{off} ratio, transconductance, and output conductance. We concluded that the device metrics such as I_{on}, I_{on}/I_{off} ratio, transconductance, and output conductance increases with the decrease in gate insulator thickness. Also, we concluded that the gate insulator thickness reduction causes subthreshold slope close to the theoretical limit of 60 mV/decade and DIBL close to zero at room temperature.

Keywords: CNT diameter, Gate insulator thickness, high- κ, Threshold voltage, CNTFET.

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1. INTRODUCTION

The electronic devices with small size, light weight, low power consumption, high performance and rich in functionalities are highly demanded. For the past 40 years, the semiconductor industry and academia have pushed the downscaling of metal-oxide-semiconductor field-effect transistor (MOSFET) to achieve those requirements. The MOSFET device scaling might not be extended to below 10 nm because of the short-channel effects in devices. It is therefore important to search for alternative devices for Si MOSFET devices [1-3]. Some novel nanoelectronic devices have been suggested to replace the MOSFET to overcome those limitation challenges. Carbon nanotube field effect transistor (CNTFET) appears to be the most promising nanostructure devices in realizing the nanotransistors and replacing current Si MOSFET, due to the superior electrical and mechanical properties of carbon nanotube (CNT) [4-5]. Silicon dioxide (SiO_2) has been used as the gate dielectric material in MOSFET devices for over 40 years. As transistors have decreased in size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current, raising device performance. As the thickness scales below 1.5 nm, leakage currents due to tunneling increase drastically, leading to high power consumption and reduced device reliability. Replacing the silicon dioxide gate dielectric with a high-κ material allows increased gate capacitance without the associated leakage effects. The implementation of high-κ gate dielectrics is one of several strategies developed to allow further miniaturization of microelectronic components, colloquially referred to as extending Moore's Law [6]. The possible application for nanoelectronic devices has been extensively explored since the demonstration of the first carbon nanotube field-effect transistors (CNTFETs) [7-8]. The high strength and high flexibility are unique mechanical properties of CNT and the electronic properties depend drastically on both the diameter and its chirality [9-10]. In a CNT, low bias transport can be nearly ballistic across distances of several hundred nanometers [11]. In addition, deposition of high-κ gate insulators does not degrade the carrier mobility because the topological structure results in an absence of dangling bonds [12]. The conduction and valence bands in CNT are symmetric, which is advantageous for complementary applications. The band-structure is direct, which enables optical emission, and finally, CNT is highly resistant to electromigration [12]. Because of these attractive features, CNTs are receiving much attention for possible device applications. The CNTFET exhibit a wide range of favorable electrical properties; some of them are presented below:

– High transconductance. This property determines the performance of any FET. A higher transconductance results in greater gain or amplification.
– Superior subthreshold slope. This property is very important for low power applications.
– Superior threshold voltage.
– High mobility.
– Ballistic transport. This property results in high speed devices.
– High current density.
– High I_{on}/I_{off} current ratios.

In this paper, we have discussed the various simulation results of cylindrical shaped ballistic CNTFET such as transfer characteristics, output characteristics, average velocity, g_m/I_d ratio, mobile charge, quantum capacitance/insulator capacitance, drive current (I_{on}), I_{on}/I_{off} ratio, transconductance, output conductance, subthreshold slope (SS) and drain induced barrier lowering (DIBL)

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by choosing the parameters like CNT diameter $d = 3$ nm, threshold voltage $V_{th} = 0.4$ V, temperature $T = 300$ K, gate insulator dielectric constant $\kappa = 3.9$ (SiO_2), gate control parameter $\alpha_G = 1$, drain control parameter $\alpha_D = 0$ while the gate insulator thickness is varied.

2. DEVICE STRUCTURE

The structure of cylindrical CNTFET as shown in Fig. 1. In cylindrical CNTFET, a semiconducting CNT is used as the channel which is surrounded by an oxide layer which is finally surrounded by a metal contact. This metal contact serves as the gate terminal. We assume that the metal-nanotube contact resistance, $R_C = 0$, and carrier transport through nanotube is ballistic (no scattering). The channel length is an important parameter when fabricating a device. Depending on the types of scattering that take place in the channel, conduction can fall into either the diffusive or ballistic regimes. Because the model used in FETToy [13] assumes ballistic conduction, there is no consideration of channel length as there would be no effect so long as ballistic conduction is maintained.

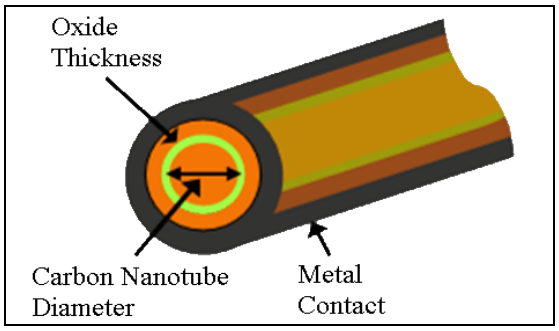

Fig. 1 – Structure of cylindrical Carbon nanotube field effect transistor (CNTFET)

3. RESULTS AND DISCUSSION

In this section, we have discussed the effect of the gate insulator thickness scaling on the various performance parameters and characteristics of cylindrical CNTFET.

3.1 Variation of Drain-Source Current (I_{DS}) w.r.t Gate- Source Voltage (V_{GS})

The variation of drain-source current (I_{DS}) w.r.t gate-source voltage (V_{GS}) for various gate insulator thicknesses of CNTFET as shown in Fig. 2. It has been observed that the drain current of the CNTFET increases with the reduction in gate insulator thickness. It means that when we reduce the gate insulator thickness, the current capability of the CNTFET enhances. This shows that the conductivity of the CNTFET is inversely proportional to the gate insulator thickness.

3.2 Variation of Drain-Source Current (I_{DS}) w.r.t Drain- Source Voltage (V_{DS})

The variation of drain-source current (I_{DS}) w.r.t drain- source voltage (V_{DS}) for various gate insulator thicknesses of CNTFET as shown in Fig. 3. It has been observed that the saturation current increases with the

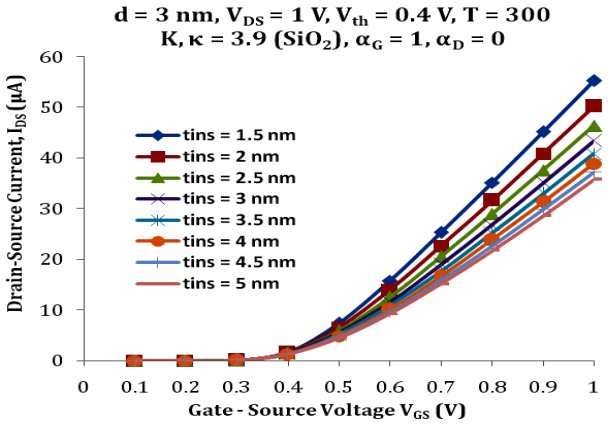

Fig. 2 – Variation of drain-source current (I_{DS}) w.r.t gate-source voltage (V_{GS}) for various gate insulator thicknesses of CNTFET

decrease in gate insulator thickness and degree of this effect increases as we go for lower gate insulator thickness. This means that as we are going for lower gate insulator thickness the increment in saturation current with respect to gate insulator thickness also increases.

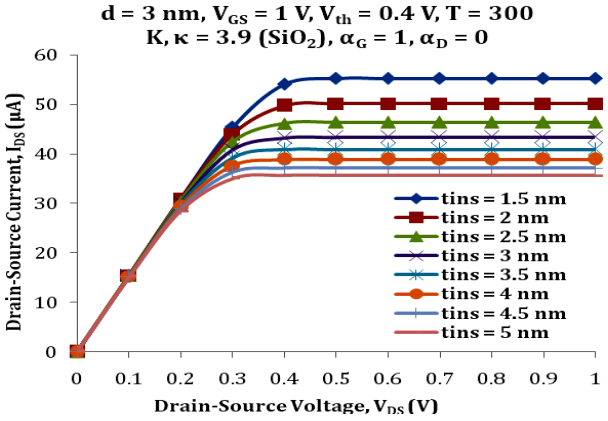

Fig. 3 – Variation of drain-source current (I_{DS}) w.r.t drain-source voltage (V_{DS}) for various gate insulator thicknesses of CNTFET

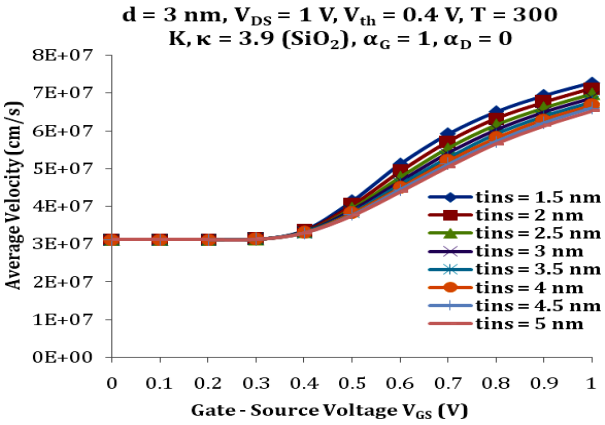

Fig. 4 – Variation of average velocity w.r.t gate-source voltage (V_{GS}) for various gate insulator thicknesses of CNTFET

3.3 Variation of Average Velocity w.r.t Gate-Source Voltage (V_{GS})

The variation of average velocity w.r.t gate-source voltage (V_{GS}) for various gate insulator thicknesses of CNTFET as shown in Fig. 4. It has been observed that the average velocity of carries increases with the increase in drain-source current beyond the threshold voltage. Also, average velocity increases with the reduction in gate insulator thickness.

3.4 Variation of g_m/I_d Ratio w.r.t Gate-Source Voltage (V_{GS})

The variation of g_m / I_d ratio w.r.t gate-source voltage (V_{GS}) for various gate insulator thicknesses of CNTFET as shown in Fig. 5. In order to achieve a relatively large transconductance the CNTFET must have thin gate insulator thickness. The larger the transconductance, the greater the gain it will deliver. It has been observed that as the gate insulator thickness is reduced, the g_m / I_d ratio increases due to the reason that the gate oxide capacitance is increased as the gate insulator thickness is reduced.

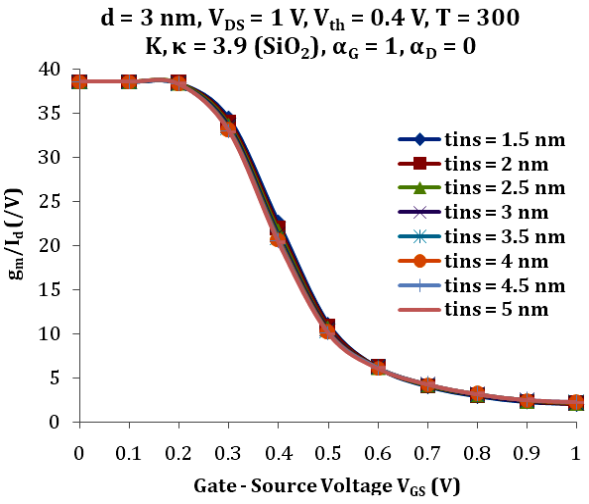

Fig. 5 – Variation of g_m/I_d (/V) ratio w.r.t gate-source voltage V_{GS} for various gate insulator thicknesses of CNTFET

3.5 Variation of Mobile Charge/q w.r.t Gate-Source Voltage (V_{GS})

The variation of mobile charge/q w.r.t gate- source voltage (V_{GS}) for various gate insulator thicknesses of CNTFET as shown in Fig. 6. It is noticed that increasing the drain voltage beyond a specific value has no longer an effect on the shape of the curves since the mobile charge remains constant. It is also observed that low drain voltage produces higher mobile charge and high drain voltage produces lower mobile charge. Also, it has been noticed that the mobile charge increases with the reduction in gate insulator thickness.

3.6 Variation of Mobile Charge/q w.r.t Drain-Source Voltage (V_{DS})

The variation of mobile charge/q w.r.t drain-source voltage (V_{DS}) for various gate insulator thicknesses of CNTFET as shown in Fig. 7. It has been observed that

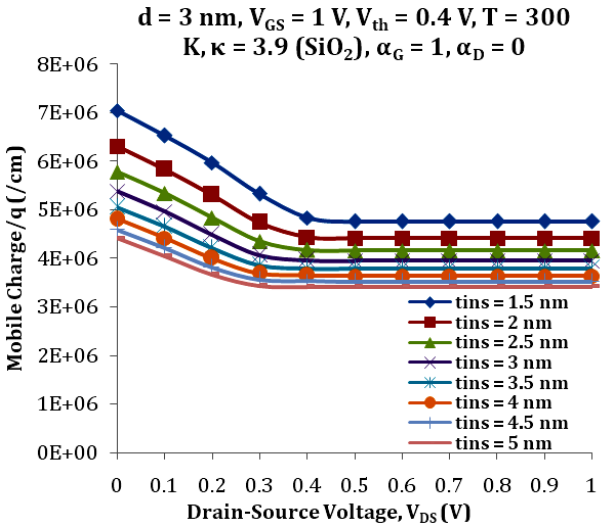

Fig. 6 – Variation of mobile charge/q (/cm) w.r.t gate- source voltage V_{GS} for various gate insulator thicknesses of CNTFET

the mobile charge increases with the increase in gate source voltage beyond 0.3 V. Also, it is noted that with the reduction of gate insulator thickness the mobile charge increases.

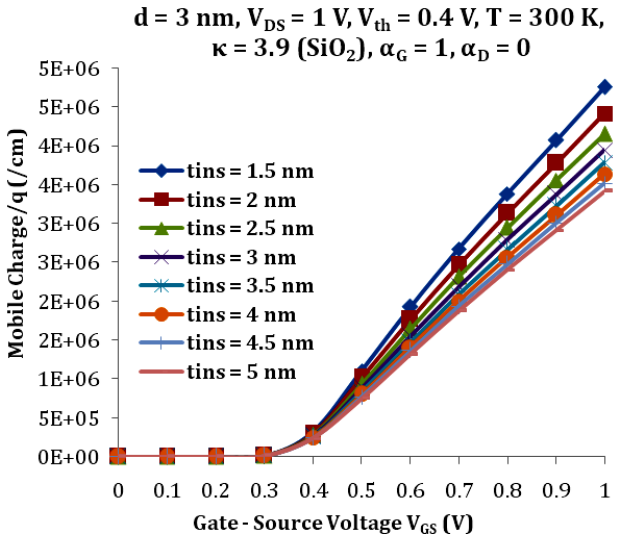

Fig. 7 – Variation of mobile charge/q (/cm) w.r.t drain- source voltage (VDS) for various gate insulator thicknesses of CNTFET

3.7 Variation of QC/Insulator Capacitance w.r.t Gate-Source Voltage (V_{GS})

The variation of QC/Insulator capacitance w.r.t gate- source voltage (V_{GS}) for various gate insulator thicknesses of CNTFET as shown in Fig. 8. It is noted that a higher quantum capacitance/insulator capacitance can be reached at a gate voltage greater than 0.5 V beyond this voltage quantum capacitance/insulator capacitance gets decreased. Lower drain voltage shows significant capacitance effect. Also, it has been observed that the reduction in gate insulator thickness causes quantum capacitance/insulator capacitance reduced.

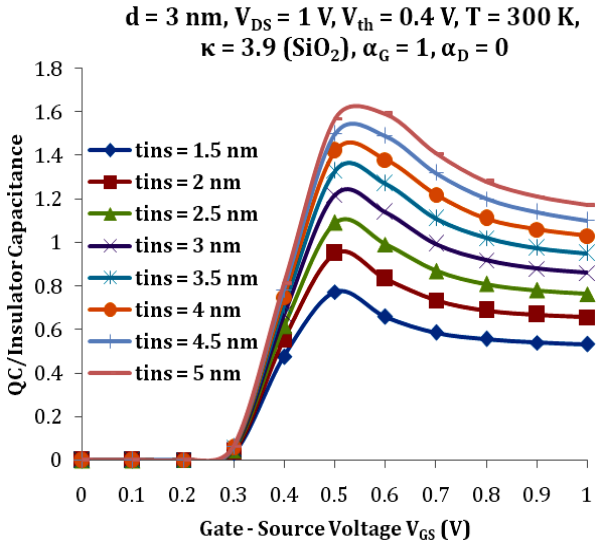

Fig. 8 – Variation of QC/Insulator Capacitance w.r.t gate-source voltage (V_{GS}) for various gate insulator thicknesses of CNTFET

3.8 Effect of Gate Insulator Thickness on Drive Current (I_{on}) and I_{on} / I_{off} ratio

The variation of drive current (I_{on}) and I_{on} / I_{off} ratio w.r.t gate insulator thickness as shown in Fig. 9 and 10 respectively. It has been shown that the drive current and I_{on} / I_{off} ratio increases with the decrease in gate insulator thickness. High I_{on} / I_{off} ratio indicates fast switching speed of the device.

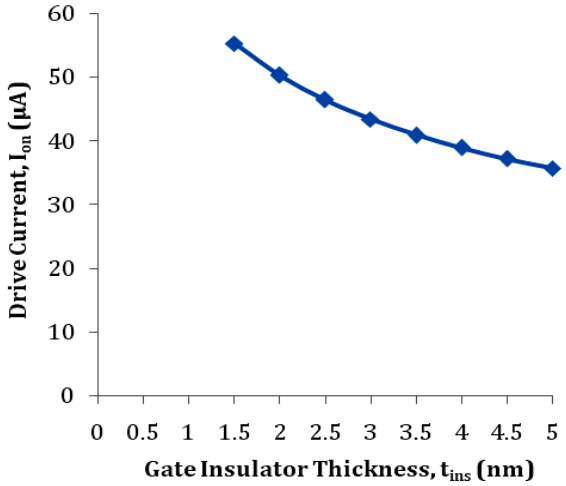

Fig. 9 – Variation of drive current I_{on} w.r.t gate insulator thickness

3.9 Effect of Gate Insulator Thickness on Transconductance (g_m) and Output conductance (g_d)

The variation of transconductance (g_m) and output conductance (g_d) w.r.t gate insulator thickness as shown in Fig. 11 and 12 respectively. It is evident from the figures that the transconductance of device improves with the decrease in gate insulator thickness due to more controllability of gate on the channel. Also, the output conductance of CNTFET increases with the reduction in gate insulator thickness.

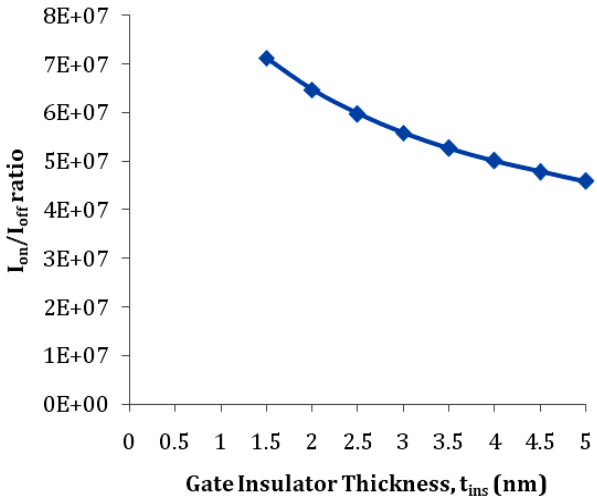

Fig. 10 – Variation of I_{on} / I_{off} ratio w.r.t gate insulator thickness

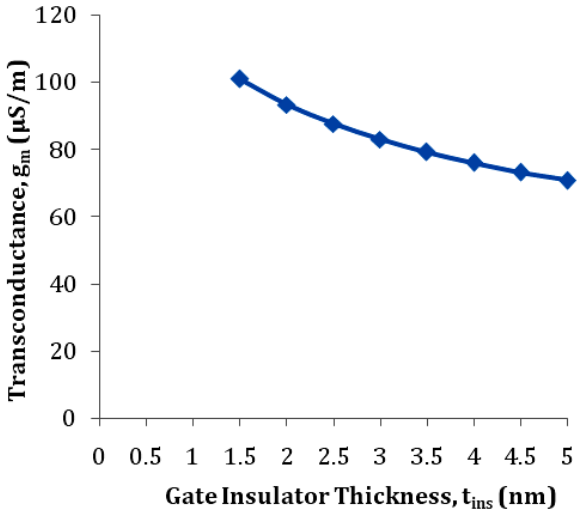

Fig. 11 – Variation of transconductance w.r.t gate insulator thickness

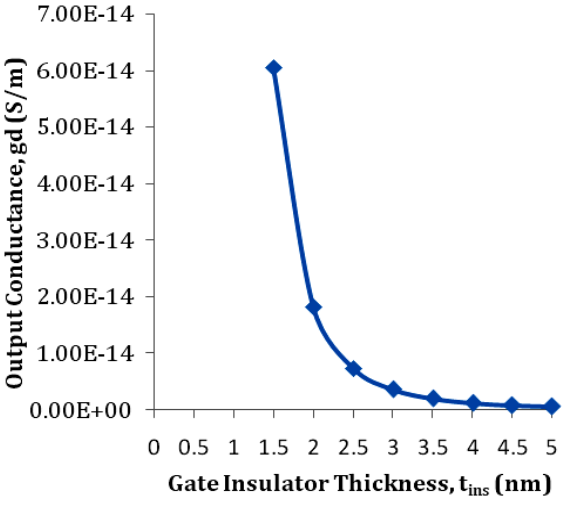

Fig. 12 – Variation of output conductance w.r.t gate insulator thickness

3.10 Short Channel Effect in CNTFET

The short-channel effects are attributed to two physical phenomena such as (i) The limitation imposed on electron drift characteristics in the channel and (ii) The modification of the threshold voltage due to the shortening channel length [16-17]. Two short channel effects has been discussed and analyzed.

3.10.1 Subthreshold Slope (SS)

It indicates how effectively the flow of drain current of a device can be stopped when V_{GS} is decreased below V_{th}. When I_{DS}-V_{GS} curve of a device is steeper subthreshold slope will improve. A device characterized by steep subthreshold slope exhibits a faster transition between off (low current) and on (high current) states. The effect of gate insulator thickness on subthreshold slope as shown in Fig. 13. As can be seen from the figure that the subthreshold slope improves with the gate insulator thickness reduction and close to its theoretical limit at t_{ins} = 1.5 nm. These results imply that the gate-to channel control ability is enhanced due to the assistance of the thin gate insulator thickness.

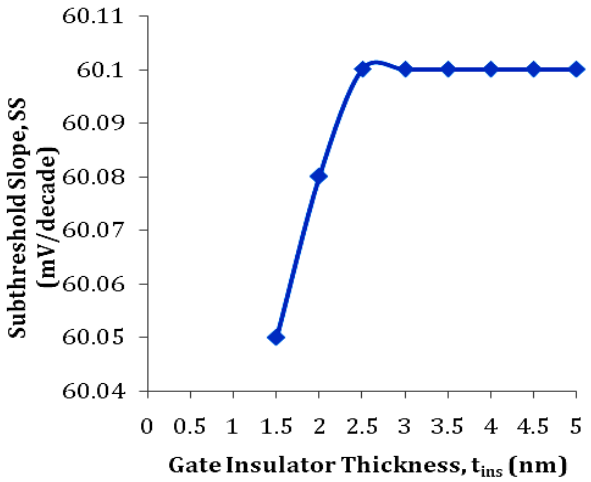

Fig. 13 – Variation of subthreshold slope w.r.t gate insulator thickness

3.10.2 Drain Induced Barrier Lowering (DIBL)

In the weak inversion regime, there is a potential barrier between the source and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between these two regions. The barrier height for channel carriers should ideally be controlled by the gate voltage to maximize transconductance. The DIBL effect [18] occurs when the barrier height for channel carriers at the edge of the source reduces due to the influence of drain electric field, upon application of a high drain voltage. This increases the number of carriers injected into the channel from the source leading to an increased drain off-current. Thus, the drain current is controlled not only by the gate voltage, but also by the drain voltage.

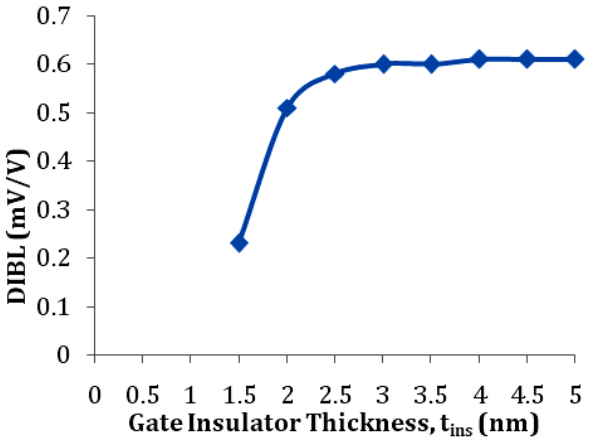

Fig. 14 – Variation of drain induced barrier lowering (DIBL) w.r.t gate insulator thickness

The effect of gate insulator thickness on DIBL as shown in Fig. 14. It can be seen that the DIBL is reduced with the reduction in gate insulator thickness.

4. CONCLUSION

The impact of scaling gate insulator thickness on CNTFETs has been studied. It has been observed that reduction in gate insulator thickness causes the increase in I_{on} / I_{off} ratio and leads to a high drive current (I_{on}). The short channel effects such as subthreshold swing and drain induced barrier lowering also improve and are close to its theoretical limit. Transconductance is larger for thin gate insulator thickness CNTFETs. Thus, thin gate insulator thickness are better option for enhancing the performance of cylindrical shaped ballistic CNTFET.

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