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Electrical Characterization of TiO_2 Insulator Based Pd / TiO_2 / Si MIS Structure Deposited by Sol-Gel Process

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Electrical characterization of a Pd / TiO_2 / Si MIS structure has been reported in this paper. The TiO_2 layer has been deposited on *n*-Si substrate by spin coating sol-gel process using Titanium Tetraisopropoxide [$Ti(OC_3H_7)_4$]. The current-voltage and capacitance-voltage characteristics were studied at room temperature (300 K) by applying the dc bias gate voltage swept from – 3 to 3 V for the frequency range of 50 kHz to 1 MHz. The study reveals that the capacitance in the accumulation region has frequency dispersion in high frequencies (> 10 kHz) which is attributed to leakage behavior of TiO_2 insulating layer, interface states and oxide defects. Different models of current conduction mechanism have been applied to study the measured data. It is found that Schottky-Richardson (SR) emission model is applicable at low bias voltage, Frenkel-Poole (FP) emission model at moderate bias voltages while Fowler-Nordheim (FN) tunneling dominates at higher bias voltages. TiO_2 based MIS devices having high dielectric constant and good interface quality with Si substrate are expected to play a major role in microelectronic applications.

Keywords: TiO_2, Thin film, Sol-Gel, MIS structure.

PACS numbers: 68.35. bt, 68,55. aj, 73.61. Ng

1. INTRODUCTION

Titanium dioxide (TiO_2) films are being sought as a competent alternative dielectric to silicon dioxide (SiO_2) films in ultra large-scale integration (in sub 100 nm silicon technology) because of its much higher dielectric constant and higher breakdown strength than those of SiO_2 [1]. At such a low dimension, SiO_2 becomes vulnerable to direct tunneling which dramatically increases the leakage current [2]. A number of attempts have been made to find alternative oxides with high dielectric constant (κ) such as HfO_2, ZrO_2, Ta_2O_5 and TiO_2 allowing to increase gate capacitance thereby negating the associated leakage effects. Among these high-κ dielectric materials, TiO_2 is being seen as an attractive candidate in order to replace the conventional oxide material SiO_2. Because TiO_2 possesses higher dielectric constant approximately ranging from 10 to 80 depending on the deposition techniques, annealing temperature and annealing ambiance [3, 4] of the former. The electrical properties of the insulator (TiO_2) layer have been found to be affected by the growth technique owing to the reactions at the insulator / Si substrate interface and metal / TiO_2 interface. Furthermore, TiO_2 based MIS structures exhibit relatively large leakage currents. This may be attributed to relatively small bandgap of ~ 3.5 eV of TiO_2, low electron affinity ~ 4 eV and low band offset with silicon [1, 3-4].

A number of thin film deposition techniques are employed in the formation of TiO_2 thin film, including RF- sputtering [5], Metal-organic chemical vapor deposition (MOCVD) [6], E-Beam Evaporation [7], Chemical Vapor Deposition [8] and Sol-Gel process. The Sol-Gel process is becoming popular to prepare thin films coating using simple equipment. The interest in application of Sol-Gel method is due to several advantages including homogenous layers on various substrates at low cost, ease of composition control, large area coatings and tailoring of refractive index. The thickness and the porosity of the film can be easily controlled by changing the concentration of the Sol-Gel. Large surface areas can be coated by spin or dip coating. The Sol-Gel processes are particularly efficient in producing thin, uniform and multicomponent oxide layers of many compositions on various substrates, including Si substrate [9].

The electrical properties of gate dielectrics are usually characterized by capacitance-voltage (C-V) and current-voltage (I-V) measurements in MIS devices. The oxide / semiconductor interface and current transport mechanisms are the factors that determine the effect of interface states on MIS based devices. The performance, reliability and compatibility of the MIS devices depend mainly on the formation of the insulating layer, natives at the MIS interface, interface states (N_{SS}) at insulator / semiconductor interface and series resistance (R_S). Besides, the frequency factor also affects the electrical properties of these devices [10].

In this paper we have studied electrical properties of TiO_2 based Pd/TiO_2/*n*-Si MIS structures by conducting capacitance-voltage (C-V) and conductance-voltage (G-V) measurements for different high frequencies at room temperature. Charge flow mechanisms were determined from current-voltage (I-V) measurements on MIS structures.

2. EXPERIMENTAL

TiO_2 thin film based MIS capacitor was fabricated on <100> *n*-type Si (1-6 Ω·cm) substrate at room temperature. The Si wafer was cleaned by using standard procedures and then loaded in spinner system to deposit TiO_2 thin film through spin coating process [11]. The procedure for the preparation of TiO_2 thin film, involved the dissolution of 12 cc Titanium Tetrai-

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sopropoxide [Ti (OC_3H_7)$_4$, ex. Ti ≥ 98 % Merck] in 170 cc Isopropyl alcohol [$CH_3CH(OH)CH_3$, 99.7 % Merck]. The solution was kept on a magnetic stirrer for 1 h. As a final step, a few drops of Hydrochloric acid [HCl, 2M35 % Merck] were slowly added in the solution and after each additive component is added, the final solution was subjected to the magnetic stirrer for 3 h. The solution was aged at room temperature for one day before deposition. The films were inserted into a furnace and post annealed at 500 °C temperatures in O_2 atmosphere for 30 minutes after deposition. The thickness of the deposited films were determined using an ellipsometer ($\lambda = 633$ nm). The Pd / TiO_2 / Si MIS structure was developed by metalizing with palladium (~ 70 nm) using mask with circular holes of 1 mm diameter on top of the TiO_2 thin film by the vacuum vapor deposition technique using vacuum coating unit (model No.12A4D Hind VAC, India). Later on, whole back side of the Si substrate was first metalized with titanium (~ 40 nm) and then with aluminum (~ 600 nm) for the ohmic contact. Final annealing of Pd / TiO_2 / Si MIS structure had been done in the furnace at 450 °C for 7 minute in nitrogen ambiance to achieve proper front and back contacts. The Hewlett Packard, LCR meter (model No. HP-4284, USA) was used to measure (C-V) and (G-V) characteristics at room temperature with a 100 mV ac sweeping signal. DC leakage current through the structure was measured as a function of the bias voltage using semiconductor device analyzer (Agilent Technology, B-1500 A).

3. RESULTS AND DISSCUSSION

The electrical properties of the thin film type capacitor depend upon the crystalline structure and defects of the films. Note that the defects of the films depend on the post-deposition annealing temperature and ambiance. The thickness of TiO_2 thin films were measured by the ellipsometric technique using a visible laser beam at $\lambda = 633$ nm at an incident angle of 70 °. The thickness was found 22 ± 2 nm. The surface, optical and morphological properties of TiO_2 thin films have already been reported in our previous work [11]. The deposited structure of TiO_2 thin film was found porous in nature with anatase crystalline state. The capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics of Pd / TiO_2 / *n*-Si MIS diode structure measured at different values of high frequencies (50, 100, 200, 300, 500, 800 kHz and 1 MHz) are shown in Fig. 1 and Fig. 2, respectively. All the capacitance-voltage curves contain three distinct regimes: accumulation, depletion and inversion as shown in Fig. 1. The accumulation and depletion regions show dispersion at different high frequencies. In accumulation and depletion regions, the measured capacitances decrease with increasing frequency whereas the changes are negligible in inversion region. Such dispersion in the MIS system may be due to oxide charges at the interface and in the insulator. The main cause for the frequency dispersion in accumulation region of (C-V) characteristics is the formation of an inhomogeneous layer at insulator/semiconductor interface. The (C-V) characteristics were found to be stretched along the voltage axis revealing the presence of both acceptor and donor like interface traps distributed in semiconductor bandgap [12, 13]. This frequency dispersion of the capacitance in accumulation region is attributed to leaky behavior of the TiO_2 thin film because inhomogeneous layer acts in series capacitance with insulator capacitance.

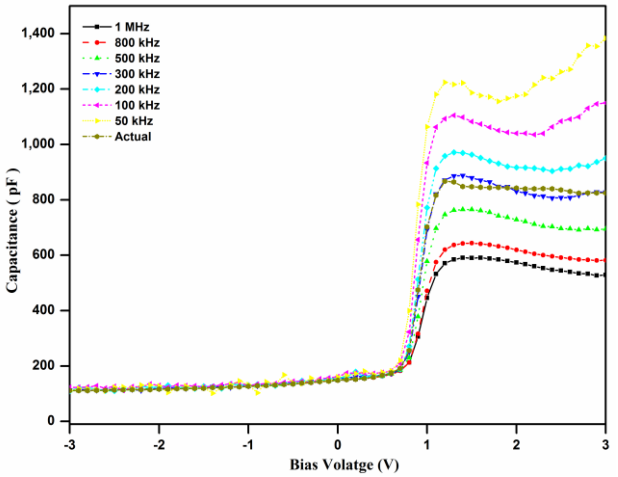

Fig. 1 – C-V characteristic of Pd / TiO_2 / *n*-Si MIS structure at different high frequencies as well as actual frequency

The conductance as a function of gate bias voltage for different high frequencies is shown in Fig. 2. The value of conductance increases with increasing frequency because of insulator capacitance in series with the interface trap resistance-capacitance network. The small peak behavior in the (G-V) characteristics indicates the presence of interface states.

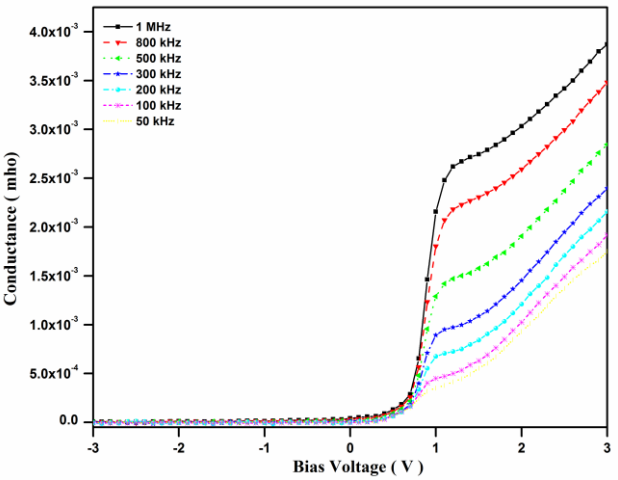

Fig. 2 – G-V characteristic of Pd / TiO_2 / *n*-Si MIS structure at different high frequencies

The frequency error can be minimized by measuring the series resistance (R_S) and applying a correction in measured values of (C-V) and (G-V) characteristics for desired information. When the MIS structure is biased into accumulation region the frequency-dependent properties of MIS devices can be described via the complex impedance as given by [14]

$$Z_m = \frac{1}{G_m + j\omega C_m} \quad (1)$$

The series resistance is the real part of the complex impedance which is given as

$$R_S = \frac{G_m}{G_m^2 + (\omega C_m)^2} \quad (2)$$

where C_m and G_m are the measured capacitance and conductance in the accumulation region. The values of R_S were calculated as a function of gate bias voltage for the frequency range 50 kHz to 1 MHz at room temperature using Eq. 2 (Fig. 3). It is seen that there is a clear peak of R_S in each curve shown in Fig. 3. The peak of R_S increases as the frequency decreases and peak almost disappears at sufficiently high frequencies. Such behavior of R_S is attributed to the particular distribution of interface states (N_{SS}) and localized trap charges at Si / TiO_2 interface states and the interfacial insulator layer at the metal-semiconductor interface.

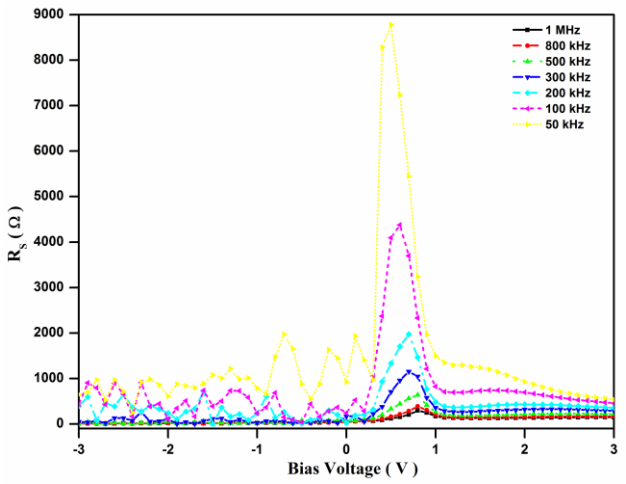

Fig. 3 – The variation of the series resistance of the Pd / TiO_2 / *n*-Si MIS structure as a function of the bias voltage for various high frequencies

The theory proposed by Yang et al. [15] for frequency-independent capacitance was calculated from the measured capacitance at two different measuring frequencies with quantum mechanical correction accordingly. The value of true frequency-independent capacitance (C_{actual}) of TiO_2 thin film is obtained as [15]

$$C_{actual} = \frac{f_i^2 C_i (1 + D_i^2) - f_j^2 C_j (1 + D_j^2)}{f_i^2 - f_j^2} \quad (3)$$

where C_i is the capacitance and $D_i = 1 / \omega_i C_i R_i$ is the measured at a f_i frequency, $i \neq j$ and R_i is the equivalent resistance. The frequency-independent capacitance is found to be compatible to the frequency at 300 kHz and it is also shown in Fig. 1. The interface trap density (D_{it}) has been calculated using Hill's method [16] by considering single frequency (300 kHz) capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) characteristics. The interface trap density (D_{it}), fixed oxide charge density (Q_f), flat-band voltage (V_{Fb}), dielectric constant (ε_r) and effective oxide thickness (EOT) are $3.11 \times 10^{11}\ eV^{-1}cm^{-2}$, $-1.9 \times 10^9\ cm^{-2}$, 0.98 V, 17 and 3.98 nm respectively. TiO_2 thin film based MIS structures generally show high leakage current, hence their applications are limited to ultralarge-scale integrated circuits. Thus it becomes important to study the various conduction mechanisms in leakage current and causes of breakdown in devices. Fig. 4 shows the (J-V) characteristics of Pd / TiO_2 / *n*-Si based MIS structure at room temperature. The measurement has been carried out by sweeping the bias voltage from negative side to positive side. The maximum current density is found to be of 0.068 A/cm^2 at 5 V. There are several carrier conduction mechanisms involved simultaneously in transport process in high-k dielectric material such as Schottky-Richardson (SR) emission, Poole-Frenkel (PF) emission and Fowler-Nordheim tunneling. The current conduction mechanism is mainly dependent on the insulating material composition, gate material, film thickness, voltage dependent insulator property and insulating film growth processing. So, it becomes necessary to check the dominancy of current conduction mechanism for TiO_2 thin films grow by sol-gel process. A number of authors have employed these mechanisms with different biasing voltages. It was found that SR emission conduction mechanism involves at lower bias voltages while at higher bias voltages other two conduction mechanisms generally dominate [17-21]. We have put current density-voltage data as per the trends suggested by previous authors. The closely observed results have been mentioned below.

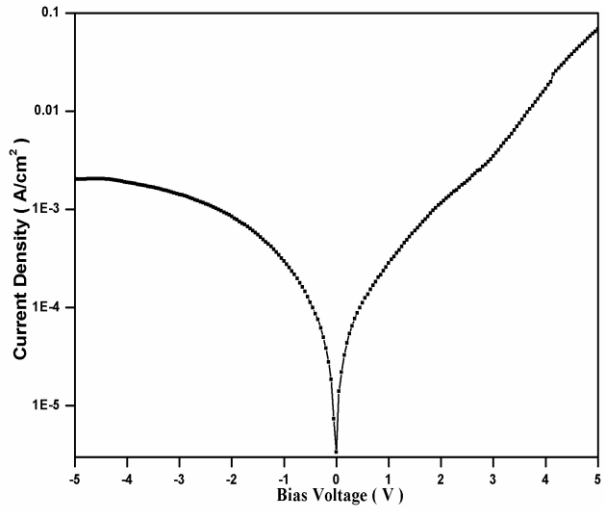

Fig. 4 – Forward and reverse bias J-V characteristic of Pd / TiO_2 / *n*-Si MIS structure

SR emission is dependent on the quality of the metal insulator interface and the insulating film which results from lowering of the barrier due to bias voltage and image forces. The current density owing to SR emission can be expressed as [13, 17, 20-21]

$$J = A^* T^2 \exp\left[-\frac{q}{kT}\left(\Phi_T - \sqrt{\frac{qV}{4\pi\varepsilon_{dyn}\varepsilon_o d_{ox}}}\right)\right] \quad (4)$$

where A^* is the Richardson constant, k is the Boltzmann constant, q is the electronic charge, T is the temperature, Φ_T is the barrier height, ε_{dyn} is the dynamic dielectric constant of the oxide, ε_o is the permittivity of free space, d_{ox} is the oxide thickness and V is the applied bias. SR emission has been illustrated in terms of *ln(J)*

versus the square root of the applied voltage ($V^{1/2}$) using the experimental *J-V* curve measured at room temperature (Fig. 5). The straight line characteristics at relatively low bias voltage confirm that the conduction of current follows SR emission model.

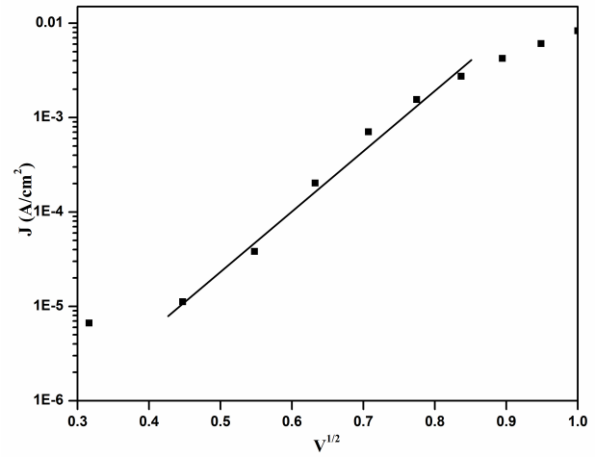

Fig. 5 – The curve of the semi logarithm (*J*) versus square root of the positive applied voltage ($V^{1/2}$) TiO_2 film to describe SR emission

At moderate bias voltage the *J-V* characteristics of MIS structure is the best fitted by FP emission model. FP emission is associated with field enhanced thermal excitation of charge carriers from traps. So mechanism of FP emission is bulk limited and depends on traps within the insulator. The expression for the FP current density is given as [13, 17-21]

$$J = A_{Pf} V \exp\left[-\frac{q}{kT}\left(\Phi_T - \sqrt{\frac{qV}{\pi\varepsilon_{dyn}\varepsilon_o d_{ox}}}\right)\right]. \qquad (5)$$

The $\ln(J/V)$ versus the square root of the applied voltage ($V^{1/2}$) obtained from the experimental *J-V* curve is shown in Fig. 6. The straight line characteristics at moderate bias voltage confirm the validity of FP emission model. Other researchers reported that the self-consistent dynamic dielectric constant $\varepsilon_{opt} < \varepsilon_{dyn} < \varepsilon_{static}$ can ensure the type of current conduction mechanism [22-23]. The optical dielectric constant (ε_{opt} is determined from refractive index (n) of TiO_2 thin film, $\varepsilon_{opt} = n^2 = 2.23 \times 2.23 = 4.97$, measured by ellipsometer (Gaertner scientific corporation, Chicago) with a wavelength of 633 nm. ε_{dyn} can be determined from the slope of a linear portion of curves of SR and FP emission mo-dels. The static dielectric constant (ε_{static}) is obtained from *C-V* characteristics of the MIS structure. The dynamic dielectric constant extracted from the slop of plot $\ln(J)$ versus $V^{1/2}$ for SR mechanism and slop of plot $\ln(J/V)$ versus $V^{1/2}$ is used in the case of the FP mechanism. FP analysis was found to be 68.7 which is higher than static dielectric constant while for SR analysis the value was found to be 15.5 consistent with the expected range of values. The linearity observed in the slopes suggests that current conduction takes place by both the emission processes but SR emission is dominated at room temperature.

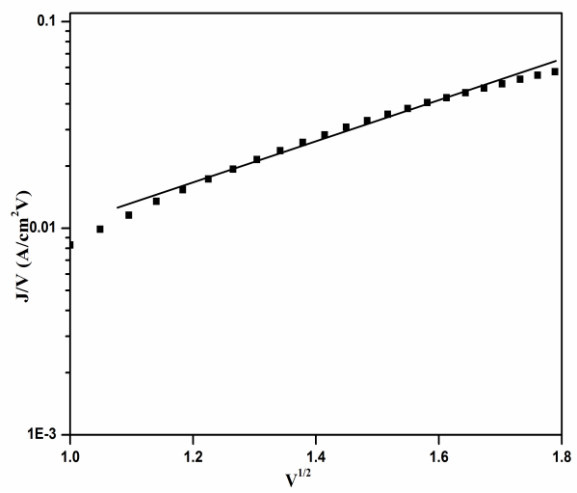

Fig. 6 – The curve of the semi logarithm (J/V) versus square root of the positive applied voltage ($V^{1/2}$) for the TiO_2 film to describe FP emission

At high bias voltage role of tunneling process in the conduction of current cann't be ruled out. FN tunneling model is used to verify the tunneling through the insulator. The expression for FN tunneling is given as [13, 17-19]

$$J = V^2 \exp\left[-\frac{b}{V}\right], \qquad (6)$$

where b is a constant given by

$$b = \frac{8\pi\sqrt{2m^* m_o (q\Phi_T)^3}}{3qh} d_{ox} \qquad (7)$$

m^* is the tunneling effective mass of the charge carrier in the tunnel barrier, m_0 is the free electron rest mass, h is the Planck's constant and Φ_T is the barrier height of oxide. The FN model based on tunneling mechanism is applied to $\ln(J/V^2)$ versus the reciprocal of the applied voltage ($1/V$) curve as shown in Fig. 7. The straight line

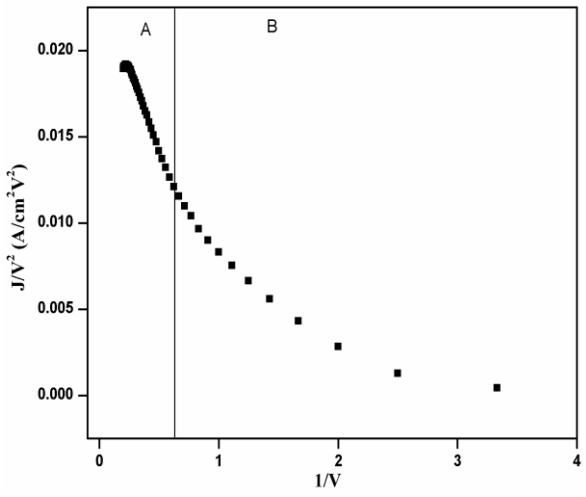

Fig. 7 – The curve of the semi logarithm (J/V^2) versus reciprocal of the positive applied voltage ($1/V$) for TiO_2 film to describe FN tunneling

nature of the variation confirms (regime A) the applicability of FN model at larger bias voltage more than 3 V. The current behavior for lower bias voltages (regime B) shows trap-assisted tunneling and quasi-saturation stages.

4. CONCLUSION

The interfacial and electrical properties of Pd / TiO_2 / *n*-Si based MIS structure were characterized using *C-V* and *G-V* techniques. The *C-V* and *G-V* characteristics exhibit frequency dependence due to traps in the insulating layer and at interface. TiO_2 thin films have high dielectric constant with good interface quality with Si. The leakage current conduction is checked with different conduction model and was found to be consistent with previous reported results. In the low bias range SR emission model is found to dominate followed by FP emission model at moderate bias voltage. The effect of tunneling at high voltage is also confirmed by application of FN model. Leakage current is acceptable for most of the electronics circuits. So high quality TiO_2 films deposited by Sol-Gel process can be used to develop a variety of thin film devices for electronic applications.

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