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IMPACT OF ANNEALING ON $CuInSe_2$ THIN FILMS AND ITS SCHOTTKY INTERFACE

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The room temperature current–voltage (I-V) characteristics of the Al/*p*-$CuInSe_2$ *Schottky Diodes fabricated on thermally evaporated CIS thin films, before and after annealing, were studied. Prior to their diode formation, the undertaken CIS thin films were compared on the basis of structural, morphological and electrical investigations. Wherein, annealed films showed an increase in the grain size and carrier concentration values while decrease in resistivity. I-V analysis of the Schottky diodes depicted decrease in the barrier heights and increase in ideality factors of those formed on annealed films. The diodes, thus, indicated the existence of barrier inhomogenity at the M-S interface. The annealed Schottky diodes also demonstrated better ideality factor values with increased thickness of CIS layer.*

Keywords: *THERMAL EVAPORATION, CIS THIN FILM, VACUUM ANNEALING, STRUCTURAL, MORPHOLOGICAL, ELECTRICAL CHARACTERIZATION.*

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1. INTRODUCTION

Copper Indium Diselenide ($CuInSe_2$), is a ternary semiconductor from I-III-VI_2 group of semiconductors with chalcopyrite crystal structure. The semiconductor was first synthesized in 1953 by Hahn et al. [1]. Since then $CuInSe_2$ has become a widely studied material in view of its applications in the areas of non-linear optics and optical communications. The CIS material has been, in particular, found extremely useful in some Electronics Devices such as Solar Cells [2], Light Emitting Diodes [3, 4] and Photovoltaic Detectors [5, 6] due to its stability and inexpensive means of production. A variety of deposition techniques viz. flash evaporation, sputtering, spray pyrolysis, electrodeposition, screen printing, stacked elemental layer deposition, three source evaporation etc have been used by the researchers to prepare $CuInSe_2$ thin films. As on today, the best results have been achieved by evaporation of the elements, either simultaneously or in sequential processes with adjacent treatment.

Since Schottky barrier diodes (SBD) are the most simple metal–semiconductor (MS) contact devices [7, 8]. Also, for Schottky junctions, the electrical characteristics are more complicated since the junctions form at the free surfaces, which are often defective and contaminated [9], [10]-[14]. Although, the current mechanisms in *p*-type systems have found difficult to

study as these demonstrate high ideality factors even at moderate bias values [10, 14], yet attempts have been made to study it on the basis of thermionic emission mechanism. In view of the potentials of p-$CuInSe_2$ in energy application, we have been studying this material using the simply fabricated Al/p-$CuInSe_2$ Schottky junctions. Al was chosen as the Schottky contact because it is the best compromise between a small work function (4.17 eV [15]) and low chemical resistivity in the metal list. The characteristics of the Schottky diode are normally studied by the three methods; current-voltage measurement, activation energy measurement, and photoelectric measurement method [16]. However, for the very small contacts used in deep submicron technology, it is difficult to use activation energy measurement and photoelectric measurement due to area restriction. Therefore, current-voltage measurement is the best method for very small contacts.

In the present work, thermal evaporation technique has been used to deposit the CIS layers. The thermally evaporated films were also annealed for achieving their better crystallanity and improved grain size. All the deposited films were then undertaken for the structural and electrical characterization. These layers were subsequently used for the formation of Al/p-$CuInSe_2$ Schottky diodes which were investigated for the current transport over the metal-semiconductor interface at room temperature.
Also, the effect of thermal annealing and CIS layer thickness on Schottky behavior was evaluated from the current-voltage characteristics.

2. EXPERIMENTAL DETAILS

The polycrystalline bulk $CuInSe_2$ was synthesized by direct reaction of high-purity (99.99%) elements, viz Copper (Cu), Indium (In) and Selenium (Se) as described earlier [17]. The synthesized pulverized material was used as source material to deposit thin films of $CuInSe_2$ on organically cleaned sodalime glass substrates held at 523 K, by slow thermal heating of molybdenum boat upto 1473 K over a period of approximately 10 minutes. The rate of deposition was 0.8-1.0 nm/s and typical thickness of the film was 300 nm which was continuously monitored during the deposition using a quartz crystal thickness monitor DTM-101 (HindHiVac., India). The substrate temperature was measured using Chromel-Alumel Thermocouple kept in good thermal contact with the substrate. The thin films of $CuInSe_2$ were also thermally annealed at 573 K in a vacuum chamber at a base pressure of 10^{-2} mbar for 1 hr. The deposited films were found to be p-type in nature. The Schottky diodes of CIS were prepared by depositing Aluminum thin films over the deposited CIS thin layer. The area of the diode was 4.775×10^{-3}cm^2. The overall design of CIS based Schottky device is shown in the Fig. 1 where CIS layer act as a p-type semiconductor and Aluminum forms a Schottky contact and Silver (Ag) act as a back ohmic contact to the CIS film. The thicknesses of Silver and Aluminum films were kept to be 150 nm.

The structural characterization of the thin films of $CuInSe_2$, deposited on glass substrates, was carried out using an X-ray diffractometer (XRD), D-Max-III (Rigaku), in 2h range of 10°-80°, at a scan-rate of 0.05°s^{-1}, using CuK_α radiation. The surface morphology of the thin films, were studied using an atomic force microscope (AFM), CP II research head (Veeco, USA), in non contact mode [17]. Hall effect measurements setup having a source meter

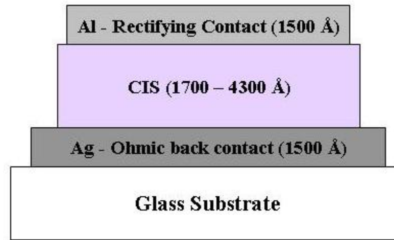


Fig. 1 *– The cross-sectional view of the structure of* Al/p-$CuInSe_2$ *Schottky diode*

2420-C (Keithley) and a $6^1/_2$ digit multimeter 2000, (Keithley), were used for the electrical characterizations of the as-deposited $CuInSe_2$ thin films. The measu-rements of current-voltage (I–V) characteristics were made at room temperature (300 K) using a computer interfaced I-V measurement setup comprising Keithley Source Meter (model 2420) and Pentium-IV personal computer.

3. RESULTS AND DISCUSSIONS

3.1 Structural characterization of $CuInSe_2$ thin films

Fig. 2(a) and Fig. 2(b) shows XRD analysis of $CuInSe_2$ thin films deposited at 523 K substrate temperature (T_s) considered after and before annealing at 573 K respectively. The structural analysis of both the as-deposited thin films suggests that the films were polycrystalline in nature having preferred orientation of grains in (112) direction. Moreover, after annealing the film showed an additional peak as well, at $2\theta = 64.5°$, besides an increase in intensity of the peak. The referred thin films samples have been deposited with changing substrate temperature and there were some additional peaks observed at lower substrate temperatures. However, these smaller peaks disappeared at and around 523 K substrate temperature. Further, annealing of the samples has caused the re-occurrence of an additional peak (400), which confirms the polycrystalline nature of the thin film samples with preferred (112) orientation.

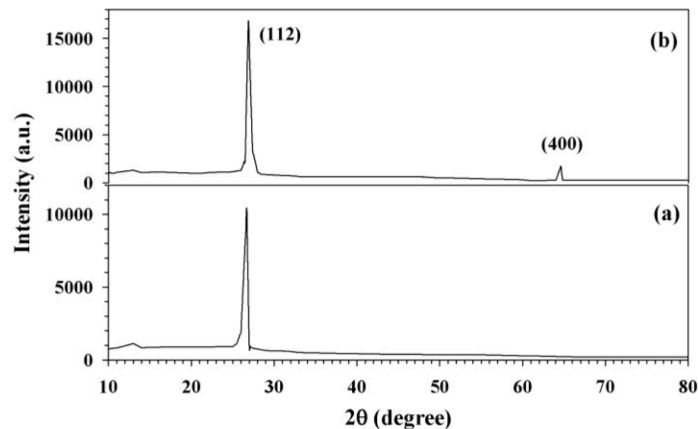


Fig. 2 *– XRD patterns of* $CuInSe_2$ *films at* $T_s = 523$ *K (a),* $T_s = 523$ *K,* $T_a = 573$ *K (b)*

In order to obtain an idea about the grain size distribution in deposited $CuInSe_2$ thin films (t = 300 nm), the particle size for each sample was calculated using Scherrer's formula [18] given as,

$$D = 0.9\lambda/\beta\cos\theta, \tag{1}$$

where D is the crystallite size as measured perpendicular to the reflecting plane, 0.9 is the Scherrer's constant, λ is the wavelength of the X-ray radiation, β is the width at half the maximum intensity and θ is the Bragg's angle. Particle size estimated for all samples are shown in Table 1.

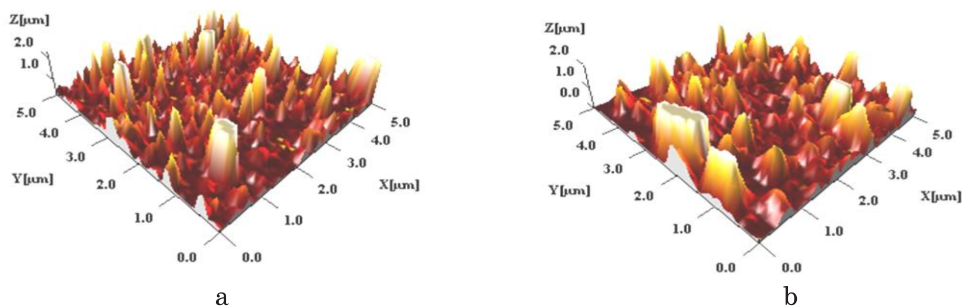
Table 1 *– Crystallite Size of evaporated CIS thin films*

Evaporation method	Substrate Temperature T_s (K)	Annealing Temperature T_a (K)	Position of (112) peak 2θ (degrees)	FWHM (degrees)	Crystallite Size – D (~ nm)
Thermal evaporation	523	Unannealed	26.70	0.249	51
	523	573	26.70	0.202	76

As observed from this table that the crystallite size has increased in case of thermally evaporated film annealed at 573 K in rough vacuum for 1hr. The increase in crystallite size will result in higher conduction in case of CIS film. Here, samples are showing particle sizes varying between 51 nm to 76 nm for different reflections taken into consideration.

3.2 Morphological studies

Fig. 3 (a) and (b) shows the surface topographical images using AFM recorded for before and after annealing of $CuInSe_2$ thin films. AFM images of the CIS thin films before annealing reveals a structure with dense but irregular grains, which suggest that the kinetic energy is not sufficient for the coalescence of the grains. However, the annealing of the films provides more dense regular grains. Thus, it is observed that the thermal annealing of film improves crystallinity.



a b

Fig. 3 *– AFM images of the $CuInSe_2$ film T_s = 523 K (unannealed) (a), T_s = 523 K, T_a = 573 K (annealed) (b)*

3.3 Electrical Analysis

The room temperature resistivity, mobility and carrier concentration of the CIS layer before and after annealed was measured by Hall experiment. Wherein, the resistivity was found to decrease from 3.45 Ω-cm to 0.40 Ω-cm for the annealed layer. However, the Hall mobility of the annealed $CuInSe_2$ thin films also decreases due to increase in point defects. Same behavior was observed by Kazamerski et al. [19] and N.M. Shah et al. [17] when they had annealed $CuInSe_2$ thin films for more than 30 minutes. Whereas the carrier concentration of the thin film was found to increase with annealing. The room temperature electrical properties of $CuInSe_2$ thin films are presented in Table 2.

Table 2 *– Room temperature electrical properties of* $CuInSe_2$ *thin films*

Sample type	Resistivity(ρ) (Ω cm)	Mobility (μ) (cm^2/Vs)	Carrier concentration(p) $(cm)^{-3}$
Before annealing	3.45	138	1.3×10^{16}
After annealing at 573 K	0.40	25	8.6×10^{17}

3.4 Current–Voltage (I–V) Analysis

Schottky barriers on semiconductor are of interest not only because of their applications as rectifying contacts but also due to the insight they afford into the nature of bounding and defect levels in solids. Generally, it is assumed that the forward bias current of the Schottky Diodes is due to thermionic emission mechanism expressed as under [20],

$$I = I_s \left\{ \exp\left(\frac{q(V - IR_s)}{\eta KT} \right) - 1 \right\}; \text{ for } V \geq 3kT/q \tag{2}$$

where I_s, the saturation current and J_s, the saturation current density, defined as:

$$J_s = I_s/S = A^{**}T^2 \exp\left(-\frac{q\varphi_{bo}}{kT} \right) \tag{3}$$

The quantities S is the diode area ($4.775 \times 10^{-3} cm^2$), A^{**} effective Richardson constant for p-type $CuInSe_2$, ($30\ A/cm^2$) [18], T is the measurement temperature in Kelvin (300 K), k is Boltzmann's constant ($1.38 \times 10^{23}\ J/K$), q is the electron charge ($1.6 \times 10^{-19}\ C$), V is the forward applied voltage, φ_{bo} is the zero bias barrier height and R_s is the series resistance. The ideality factor η is a measure of conformity of the diode to pure thermionic emission and if η is equal to 1, pure thermionic emission occurs [21]. The value of ideality factor η, in eq. (2) is given by

$$\eta = \frac{q}{kT} \frac{dV}{d\ln(I)} \tag{4}$$

The current density, J_s and the ideality factor, η were determined from the intercept and the slope respectively drawn out of the linear part of the forward ln(I) versus V plot of the Schottky diodes, shown in Fig. 5(b) using eq. (2). The forward I–V characteristics are linear in the semi logarithmic scale but deviate from linearity due to the effect of interface states and series resistance associated with the CIS layer [30].

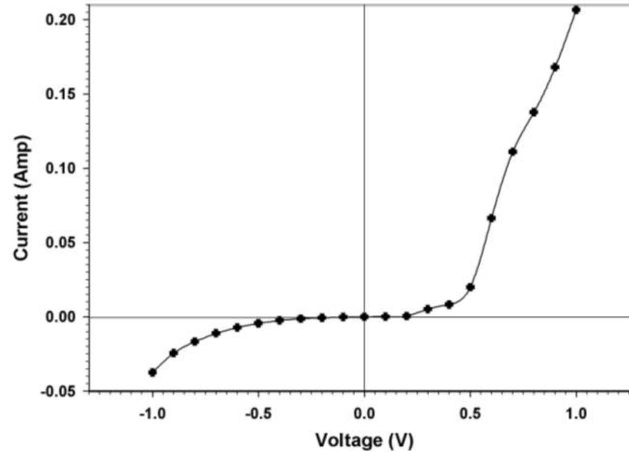


Fig. 4 *– I-V characteristics of* Al/*p*-$CuInSe_2$ *Schottky diode*

Fig. 4 shows the I-V characteristics of Al/p-$CuInSe_2$ Schottky diode studied under forward and reverse bias conditions. The ideality factor, η for Al/p-$CuInSe_2$ Schottky diodes at room temperature has been found higher, which has been attributed to the formation of thin interfacial layer and/or surface effects like, the surface charge and image force effects at Metal-Semiconductor interface. Also, the ideality factor that is determined by the image-force effect only should be close to 1.01 or 1.02 [22]. Our data i.e. $\eta > 2$, clearly shows that the diode has ideality factor considerably larger than the value determined by the image-force effect only. Therefore, the diode is patchy [23].

But in reverse bias, the current measured within the given bias was found to increase slowly with voltage and did not show any trend of breakdown. This could be due to the domination of edge leakage current and the presence of some thin oxide layer at the interface and also due to the generation of excess carriers in the depletion region at higher fields. The existence of SBH inhomogeneity offers a natural explanation for the soft reverse characteristics observed experimentally. For inhomogeneous MS contacts, the reverse current may be dominated by the current which flows through the low-SBH patches, which is controlled by the potential at the saddle point; hence, the reverse current increases with increasing reverse bias and does not saturate [24]. The immediate flow of current in the reverse bias direction is indicative of a 'backward' diode [16]. This current is due to tunneling between degenerate or nearly degenerate semiconductors. Also, two linear regions can be distinguished in Fig. 5b, suggesting that there may be more than one current mechanism at smaller bias.

3.5 Effect of Annealing

In order to study the effect of thermal annealing on the Schottky diode current transport mechanism, Al/p-$CuInSe_2$ Schottky diodes were undertaken for forward I-V analysis. Fig. 5(a) shows the forward and reverse biased I-V characteristics of both types of diodes fabricated on thermally evaporated CIS layer before and after annealing of the samples. The fitted lines used for the slope and intercept are shown in Fig. 5(b) as calculated using equation (2) and (3). The Al/p-$CuInSe_2$ Schottky diode parameters φ_{bo} and η obtained from the linear fitting of the data as shown in Fig. 5(b) are presented in Table 3.

Table 3 *– The experimental values of barrier height (φ_{bo}) and ideality factor (η) for* Al/*p-* $CuInSe_2$ *Schottky diodes with and without annealing*

Sample Type	Barrier height (φ_{bo}) eV	Ideality factor (η)	Current Density (A/cm^2)
Annealed at 573 K	0.43	3.72	2.1×10^{-11}
Unannealed	0.49	3.24	2.1×10^{-13}

From Table 3 it has been observed that the barrier height of the Schottky diodes decreases with thermal annealing. This decrease of barrier height from 0.49 eV to 0.43 eV of the annealed films is due to phase formation at the interfaces [25]. The increases in ideality factor and decrease in barrier height with temperature has been explained on the basis of lateral inhomogenity of the barrier height (BH). The values of ideality factor observed in both diodes are greater than unity. It may be associated with Fermi-level pinning at the interface [26-30] or relatively large voltage drops in interface region. Interfacial oxide layer may also be the possible cause for a higher ideality factor [31]. Surface defects produce electronic energy levels in the band gaps of CIS semiconductor. These levels can pin the Fermi energy at metal-semiconductor interfaces and cause Schottky-barrier formation [30]. The current density value increases from 2.1×10^{-13} A/cm^2 to 2.1×10^{-11} A/cm^2 with annealing thereby resulting in the better conduction over the annealed Schottky diode. Thus, Annealing of the as-deposited CIS film can significantly alter the electrical properties due to the formation of epitaxial layer, formation of new phases at the interfaces, and most importantly inter-diffusion between metal layer and CIS film [25].

3.6 Effect of Thickness of Semiconductor Layer

As conduction level in the Schottky diodes increases with the annealing of CIS layer, therefore, studies have also been undertaken to investigate the effect of thickness of the annealed CIS film on the current transport analysis of the Schottky diodes. For this purpose, current-voltage (I-V) characteristics of Al/p-CIS Schottky diode, with semiconducting layer thicknesses of 1700 Å and 4300 Å were considered. The typical current-voltage (I-V) characteristics of Al/p-CIS Schottky diode, for CIS layer thicknesses of the value of 1700 Å and 4300 Å have been shown in Fig. 6(a) and 6(b). In the simple I-V characteristics, the knee voltage is very sharp for 4300 Å CIS layer than that of the 1700 Å layer. Further, the current-voltage (I-V) characteristics of 4300 Å thick CIS layer Schottky diode shows a higher current value with respect to 1700 Å layer, in both forward as well as

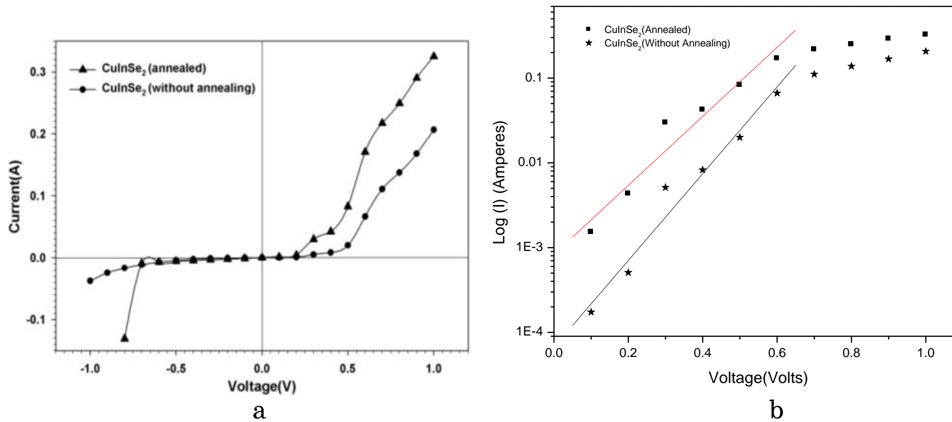


***Fig. 5** – (a) The I-V characteristics of* Al/*p*-$CuInSe_2$ *Schottky diodes with CIS film of the thickness* (1700 Å) *annealed and without annealing (b) Forward* log*(I)-V characteristics of* Al/*p*-$CuInSe_2$ *Schottky diodes with diodes with CIS film annealed and without annealing*

reverse bias. This increase in the conductivity with film thickness can be explained by the increase in grain size and the enforcement of crystal growth [32]. However, the electrical resistivity of thin films systematically decreases with increasing film thickness which ultimately results in increase in conductivity of the thin film [33]. It has also been observed that in reverse bias characteristics, the leakage current did not demonstrate saturation or breakdown in the operated region in 4300 Å thick CIS layer Schottky diode. However, the leakage current value is more in case of Schottky diode with 4300 Å thick CIS layer than 1700 Å. The parameters η, and φ_{bo} as obtained experimentally are reported in Table 4.

The values of electrical parameters η and φ_{bo} as determined by the I–V measurements decreases while the current density increases with increase in CIS layer thickness which indicates that the η and φ_{bo} values for thick CIS layer (4300 Å) as better in comparison with thin layer (1700 Å). Thus, η and φ_{bo} are closer to reported values for 4300 Å thick CIS layer, which demonstrates 4300 Å as a better thickness option for Al/p-$CuInSe_2$ Schottky diodes.

***Table 4** – The experimental values of barrier height (φ_{bo}) and ideality factor (η) for* Al/p-$CuInSe_2$ *Schottky diodes with thicknesses* (1700 Å & 4300 Å)

Thickness	Barrier height(φ_{bo}) (eV)	Ideality factor(η)	Current Density (A/cm^2)
1700 Å	0.43	3.72	2.1×10^{-11}
4300 Å	0.41	2.89	2.1×10^{-10}

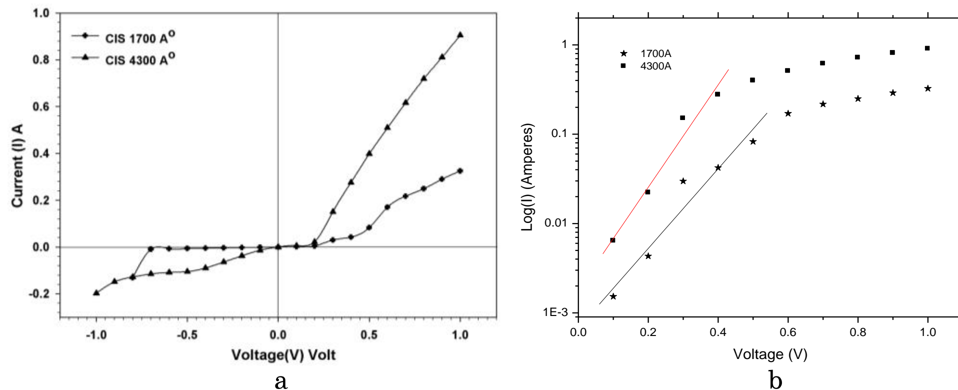


Fig. 6 *– (a) I-V Characteristics of Al/p-CIS Schottky barrier diodes with thicknesses (*1700 Å *&* 4300 Å*) (b) Forward log(I)(Ampere) versus V(voltage) characteristics of* Al/*p*-$CuInSe_2$ *Schottky diodes with thicknesses (*1700 Å *&* 4300 Å*)*

4. CONCLUSION

Structural analysis of $CuInSe_2$ thin films revealed that the thermal annealing has significant impact on structural properties of films. The XRD diffraction peaks for both types of CIS films revealed single phase with preferred orientation of grains in (112) direction. Wherein the thermally annealed film showed greater intensity and bigger crystallite size. The AFM results suggested that thermally evaporated annealed CIS thin films were denser and have less irregular shaped grains as compared to thermally as-deposited thin films. The electrical analysis of Al/p-CIS Schottky diodes prepared on thermally annealed and without annealed CIS layers revealed better conduction in case of thermally annealed sample and thereby verifying the results obtained on the basis of XRD and AFM. The effect of film thickness on the electrical properties of the films was also studied by the I-V characterization. As it was found that the conductivity increases with film thickness which has been attributed to the increase in its grain size. Thus, annealing have been found useful for better use of material for device application in view of the fact that the grain size increases, resistivity decreases, current density increases and barrier height decreases on annealing of CIS thin film and its Schottky diode formation.

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