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A DOPING DEPENDENT THRESHOLD VOLTAGE MODEL OF UNIFORMLY DOPED SHORT-CHANNEL SYMMETRIC DOUBLE-GATE (DG) MOSFET'S

P.K. Tiwari, S. Dubey, S. Jit

Department of Electronics Engineering
Institute of Technology, Banaras Hindu University,
Varanasi-221005, U.P, India
E-mail: sjit.ece@itbhu.ac.in

The paper presents a doping dependent threshold voltage model for the short-channel double-gate (DG) MOSFETs. The channel potential has been determined by solving the two-dimensional (2D) Poisson's equation using the parabolic potential approximation in the vertical direction of channel. Threshold voltage sensitivity on acceptor doping and device parameters is discussed in detail. The threshold voltage expression has been modified by incorporating the effects of band gap narrowing for highly doped DG MOSFETs. Quantum mechanical corrections have also been employed in the threshold voltage model. The theoretical results have been compared with the ATLAS^{TM} simulation results. The present model is found to be valid for acceptor doping variation from $10^{14}\ cm^{-3}$ *to* $5 \times 10^{18} cm^{-3}$.

Keywords: *DG MOSFET, SHORT-CHANNEL EFFECTS, BAND GAP NARROWING, QUANTUM MECHANICAL EFFECTS, THRESHOLD VOLTAGE*

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1. INTRODUCTION

In keeping pace with state-of-the-art CMOS technology, the present MOS devices are found incompetent to be scaled below 45 nm node[1]. Henceforth, it becomes urgent to look for novel devices, like double-gate (DG) MOSFETs, to overcome current scaling crisis [2-6]. Researchers have found intense scaling opportunities in DG MOSFETs in which undoped and doped channel DG MOSFETs are becoming popular because of their specific features [7, 8]. Basically, the DG MOSFET structure was envisaged to have an undoped body for the following reasons: (1) undoped DG MOSFETs can avoid the dopant fluctuation effect, which contributes to the variation of the threshold voltage and drive current [9]; (2) the undoped body in DG MOSFETs can enhance the carrier mobility owing to the absence of depletion charges which can significantly contribute to the effective electric field and hence degrading the mobility [10]. However, without body doping as a tool to adjust the threshold voltage, undoped DG MOSFETs need to rely on gate work function to achieve multiple threshold voltages on a chip. Tunable metal gate technology thus needs to be used for DG MOSFETs which is yet to be developed [11, 12]. In the light of this fact, body doping remains a sole alternative to set appropriate threshold voltages for DG MOSFETs [13]. In addition to these facts, doped DG MOSFETs have found wide application in memory (1T SRAM), analog circuit and RF circuit applications [14]. DG

MOSFET based circuit implementation in the subthreshold regime of device operation is the current trend in low-power VLSI design. For proper design of such type of circuits, threshold voltage determination of DG MOSFET becomes important.

Various attempts have been made to model the threshold voltage of double-gate MOSFET device after the first model presented by Sekigawa et al. [15] where reported the novel structure of DG MOSFET and presented the threshold voltage model for long channel device only. To study the short-channel threshold voltage, they[15] used numerical simulation. Agrawal et al. [16] presented the short-channel threshold voltage model for DG MOSFET, but their model was valid only for highly doped devices. Bhattacherjee et al. [17] have also presented the short-channel threshold voltage model for doped DG MOSFETs by utilizing the evanescent mode analysis to solve the 2D Poisson's equation. Both the models of Agrawal [16] and Bhattacherjee et al. [17] utilized the conventional definition of threshold voltage (gate voltage at which minimum surface potential becomes twice of Fermi potential i.e. $\psi_{S\,\min} = 2\Phi_F$). Later on, it was demonstrated that conventional definition of threshold voltage is not entirely valid for DG MOSFET and hence based on some alternative definitions [8, 18-23] threshold voltage models have been presented.

Francis et al. [18] and Moldovan et al. [8] have used the maximum transconductance change (TC) method to present the threshold voltage model. However, their model was valid only for long channel devices. Lu et al. [19] derived the threshold voltage model based on the approximation that the threshold voltage is the gate voltage at which the minimum surface potential equals to $E_g/2q$, where, E_g is the band gap of silicon channel. Suzuki et al. [20] have also derived the threshold voltage expression by defining the threshold voltage as the gate voltage which can "cause a voltage drop γ times the built in voltage due to the depleted charge" where γ is an empirically assigned value. The model reported by Tsormpatzoglou et al. [21] and El Hamid et al. [22] considered the threshold voltage as the gate voltage at which the minimum carrier charge sheet density Q_{inv} could reach a threshold charge density Q_{th}. Chen et al. [23] obtained the threshold voltage by equating the sum of front and back gate inversion charges to the substrate doping of the device. Note that, models of Refs. [16, 17] and Refs. [8, 18-23] are valid for doped channel DG MOSFET and undoped channel DG MOSFETs, respectively. From the above literature survey, it is obvious that short channel threshold voltage model for wide acceptor doping variation is still missing.

In this paper, a short-channel threshold voltage model is presented for acceptor doping range from 10^{14} cm^{-3} to 5×10^{18}cm^{-3}. Two-dimensional Poisson's equation has been solved with the parabolic potential approximation method because of its simplicity compared to the complex evanescent method. The unified threshold voltage definition for undoped and doped channel DG MOSFETs is utilized [24]. Quantum mechanical effects and band gap narrowing effects have been taken into consideration to modify the threshold voltage expression. The present model is in continuation with our previous works [4, 25] to study the subthreshold characteristics of DG MOSFETs. The proposed model results have been compared with the 2D ATLAS^{TM} device simulation data where a reasonably good matching has been found between the two.

2. THEORETICAL MODELING

Schematic structure of DG MOSFET, utilized for modeling and simulation is shown in Fig. 1; where where L, t_{si}, and t_{ox} are the gate-length, channel thickness and gate-oxide thickness of the device respectively. A uniform p-type impurity doping concentration N_a has been assumed in the silicon channel region. Suppose that $\psi(x, y)$ represents the 2D potential function in the channel. Assuming a fully-depleted channel, $\psi(x, y)$ can be obtained by solving the 2D Poisson equation

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{si}} \tag{1}$$

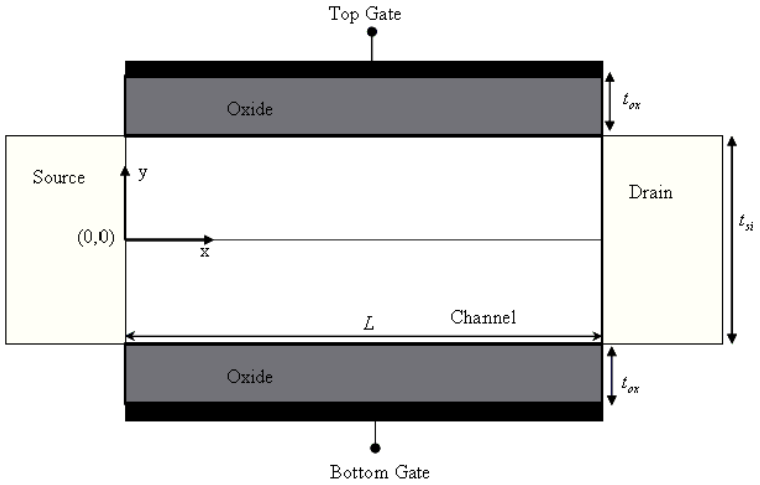

***Fig. 1** – Schematic structure of DG MOSFET*

by using the following boundary conditions [4]

$$\psi(x,y)\big|_{y=0}=\psi_0(x)\,, \tag{2}$$

$$\left.\frac{\partial\psi(x,y)}{\partial y}\right|_{y\,=\,0}=0\,, \tag{3}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left[V_G-V_{fb}-\psi(x,\pm\frac{t_{si}}{2})\right]=\pm\,\varepsilon_{si}\left.\frac{\partial\psi}{\partial y}\right|_{y\,=\,\pm\frac{t_{si}}{2}}, \tag{4}$$

$$\psi(0,0)=V_{bi} \tag{5}$$

$$\psi(0,L)=V_{bi}+V_{DS} \tag{6}$$

Where $\psi_0(x)$ is assumed to be the potential function along the SOI center, ε_{si} is the permittivity of silicon, ε_{ox} is the permittivity of the gate-oxide SiO_2,

V_{bi} is the built-in voltage at the source-channel and drain-channel junctions, V_G is the gate-source voltage, V_{DS} is the drain-source voltage and $V_{fb} = \varphi_m - \chi_s - E_g/2q - (kT/q)\ln(N_a/n_{ie})$ is the flat-band voltage, where φ_m (V) is the workfunction of the gate-electrode; χ_s (V), E_g (eV) and n_{ie} are the electron affinity, bandgap energy and effective intrinsic carrier concentration of silicon respectively. Note that effective carrier density can be obtained by $n_{ie} = n_i \exp(\Delta E_g/2kT)$; where n_i is intrinsic carrier concentration of the silicon, k is Boltzmann constant, ΔE_g refers band-gap narrowing due to heavy doping of channel and can be given as $\Delta E_g = 19\ln(N_a/10^{17})$ meV.
Now with help of Eqs.(8) and (17) of Ref. [3], the minima of surface potential can be given as

$$\psi_{S\min} = \psi_{0\min} + \frac{V_G - V_{fb} - \psi_{0\min}(x)}{\lambda_u} \times \frac{t_{si}^2}{4} \tag{7}$$

where,

$$\lambda_u = \frac{t_{si}^2}{4}\left[1 + \frac{4\varepsilon_{si} t_{ox}}{\varepsilon_{ox} t_{si}}\right] \tag{8}$$

is the character length associate with the centre channel potential.
Substituting the value of $\psi_{0\min}$ from Eq. (17) of Ref. [3], into Eq. (7) gives

$$\psi_{S\min} = 2\sqrt{k_1 k_2} + V_G - V_{fb} - \frac{\lambda_u q N_a}{2\varepsilon_{si}}\left(1 - \frac{t_{si}^2}{4\lambda_u}\right) \tag{9}$$

where, k_1 and k_2 are the constants [3].
Now, following the method reported in Ref. [24] for SOI MOSFETs, we can define the threshold voltage of the device as the gate voltage at which the minimum surface potential is given by

$$\psi_{S\min}\big|_{V_G = Vth} = \psi_{S\min-th} = \Phi_0 + \Phi_F \tag{10}$$

where V_{th} denotes the threshold voltage of uniformly doped DG MOSFET and

$$\Phi_0 = \begin{cases} \Phi_F = V_T \ln\left(\dfrac{N_a}{n_{ie}}\right); & N_a > n_T \\ V_T \ln\left(\dfrac{n_T}{n_{ie}}\right); & N_a < n_T \end{cases} \tag{11}$$

where n_T is the threshold charge density [21, 22]. The threshold charge density n_T has been evaluated by the charge calibration method as suggested by Chen et al. [7] and Lee et al. [24].

Substituting $\psi_{S\min}$ by $\psi_{S\min-th}$ in Eq. (9) and putting $V_G = V_{th}$, we can write the threshold voltage V_{th} in the polynomial form as

$$V_{th} = \left(\psi_{S\min-th} + V_{fb} + \frac{\lambda_u q N_a}{2\varepsilon_{si}}\left(1 - \frac{t_{si}^2}{4\lambda_u}\right)\right) - 2\left(1 - \frac{t_{si}^2}{4\lambda_u}\right)\sqrt{(D_u - Q_u V_{th})(E_u - R_u V_{th})}\,, \tag{12}$$

where,

$$D_u = \frac{V_{DS} + \left(V_{bi} + V_{fb} + \frac{\lambda_u q N_a}{2\varepsilon_{si}}\right)\left(1 - \exp\left(-\sqrt{\frac{2}{\lambda_u}}L\right)\right)}{\exp\left(\sqrt{\frac{2}{\lambda_u}}L\right) - \exp\left(-\sqrt{\frac{2}{\lambda_u}}L\right)}, \tag{13}$$

$$Q_u = \frac{\left(1 - \exp\left(-\sqrt{\frac{2}{\lambda_u}}L\right)\right)}{\exp\left(\sqrt{\frac{2}{\lambda_u}}L\right) - \exp\left(-\sqrt{\frac{2}{\lambda_u}}L\right)}, \tag{14}$$

$$E_u = \frac{\left(V_{bi} + V_{fb} + \frac{\lambda_u q N_a}{2\varepsilon_{si}}\right)\left(\exp\left(\sqrt{\frac{2}{\lambda_u}}L\right) - 1\right) - V_{DS}}{\exp\left(\sqrt{\frac{2}{\lambda_u}}L\right) - \exp\left(-\sqrt{\frac{2}{\lambda_u}}L\right)} \tag{15}$$

$$R_u = \frac{\left(\exp\left(\sqrt{\frac{2}{\lambda_u}}L\right) - 1\right)}{\exp\left(\sqrt{\frac{2}{\lambda_u}}L\right) - \exp\left(-\sqrt{\frac{2}{\lambda_u}}L\right)} \tag{16}$$

It may be noted that under the limiting condition of $L \to \infty$ (i.e. long channel device), last term of Eq. (12) tends towards zero; and long channel threshold voltage V_{th-L} can be obtained as

$$V_{th-L} = \psi_{S\min-th} + V_{fb} + \frac{\lambda_u q N_a}{2\varepsilon_{si}}\left(1 - \frac{t_{si}^2}{4\lambda_u}\right) \tag{17}$$

With the help of Eqs. (12) and (17), threshold voltage for short-channel DG MOSFET can be given as

$$V_{th} = \frac{-b_u + \sqrt{b_u^2 - 4a_u c_u}}{2a_u} \tag{18}$$

where,

$$a_u = 1 - 4\left(1 - \frac{t_{si}^2}{4\lambda_u}\right)^2 Q_u R_u \tag{19}$$

$$b_u = 4\left(1 - \frac{t_{si}^2}{4\lambda_u}\right)^2 \left(D_u R_u + Q_u E_u\right) - 2V_{th-L} \tag{20}$$

$$c_u = V_{th-L}^2 - 4\left(1 - \frac{t_{si}^2}{4\lambda_u}\right)^2 D_u E_u \tag{21}$$

Note that threshold voltage roll-off ΔV_{th} can be obtained as

$$\Delta V_{th} = V_{th-L} - V_{th} \tag{22}$$

Eq. (18) is the proposed model for the threshold voltage for short-channel DG MOSFET with channel doping variation from 10^{14} cm^{-3} to 5×10^{18} cm^{-3}.

It is well known fact that for a given bias voltage at gate, the quantum potential voltage is lower than the classical one. The difference between the two potentials accounts for the increase in the threshold voltage V_t by an amount

$$\Delta V_t^{QM} = \frac{h^2}{8qm_{eff}t_{si}^2} \tag{23}$$

Note that the ΔV_t^{QM} should be added in V_t (Eq.(18)) to obtain the threshold voltage of ultrathin ($t_{si} < 5$ nm) DG MOSFET devices.

3. RESULTS AND DISCUSSION

In this section, we have compared some theoretical and simulation results of the proposed model. The simulation results are obtained by using the two-dimensional ATLAS^{TM} Ref. [26] device simulator. The device has been simulated using the mid gap material tungsten as gate electrode ($\varphi_m = 4.7$ eV). Drift-diffusion (DD) model has been used instead of the energy balance (EB) model, since the DD model can predict *I-V* characteristics of short-channel MOS devices more realistically than the EB model [26]. Doping dependent mobility model has been implemented in the ATLAS^{TM} along with the suitable modification in the saturation velocity of the electron (*vsta.n*) [26]. The modified saturation velocity is well suited for the devices having $L \geq 10$ nm. Fermi-Dirac carrier statistics has been used in the simulation along with the standard recombination models (*srh*, *aug*). The variation of the surface potential $\psi_S(y)$ along the channel length has been shown in Fig. 2 for the device parameter values of $L = 30$ nm, $t_{Si} = 10$ nm , $t_{ox} = 1.5$ nm; and for different gate-source voltages V_G and drain-source voltage V_{DS}.

Note that the reference of potential measurement is Fermi level of intrinsic silicon in both simulation and our model. Minor changes in the source-channel barrier height of a surface due to the increase in the drain-voltage (i.e. the drain-induced barrier lowering (DIBL)), is observed in this case for a fixed value of gate voltage V_G. Like the conventional MOSFETs, the source-channel barrier is reduced by increasing the gate voltage V_G. Long channel threshold voltage $V_{th\text{-}L}$ variation with channel doping is shown in Fig. 3 for fixed values of silicon channel thickness and gate-oxide thickness.

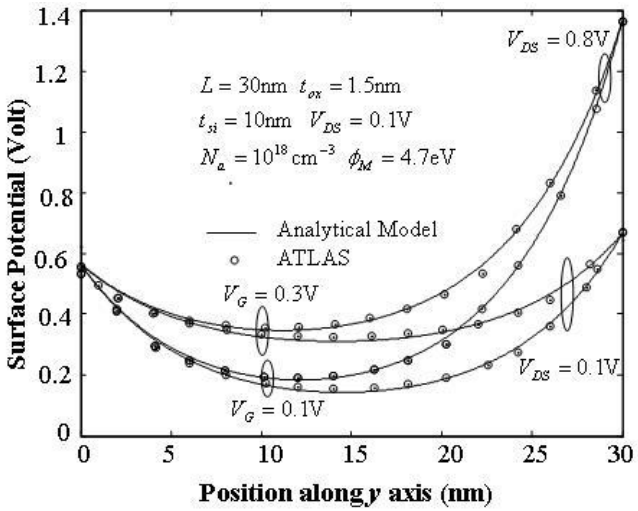

Fig. 2 – *Surface potential variation along the y axis*

Threshold voltage increases with the channel doping only for $N_a > 10^{17}$ cm^{-3}. Unlike conventional MOSFET, threshold voltage becomes almost insensitive with the channel doping $N_a < 10^{17}$ cm^{-3}. Fig. 4 demonstrates the variation of threshold voltage with the channel length for different values of channel doping. Threshold voltage decreases with channel length due to short-channel effects. Increment in channel doping increases threshold voltage and hence setting threshold voltage by channel doping may be a good alternative of immature metal work-function engineering. It is also obvious that a short-channel effect improves with channel doping. Fig. 5 depicts threshold voltage roll-off ΔV_{th} with channel length for different silicon channel

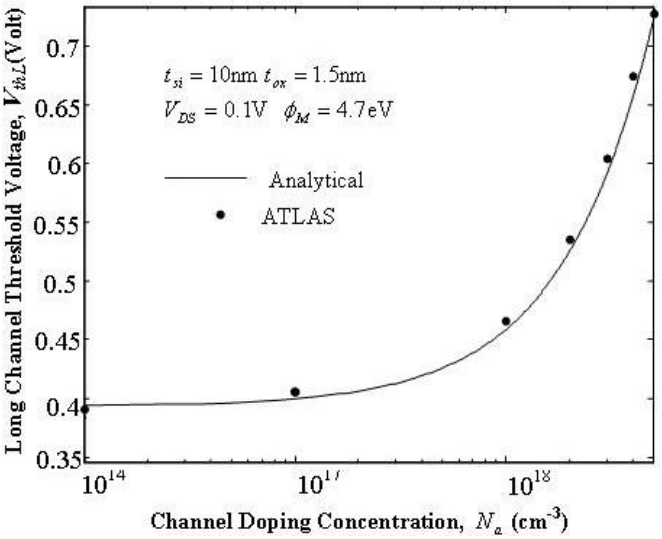

Fig. 3 – *Long channel threshold voltage with channel doping*

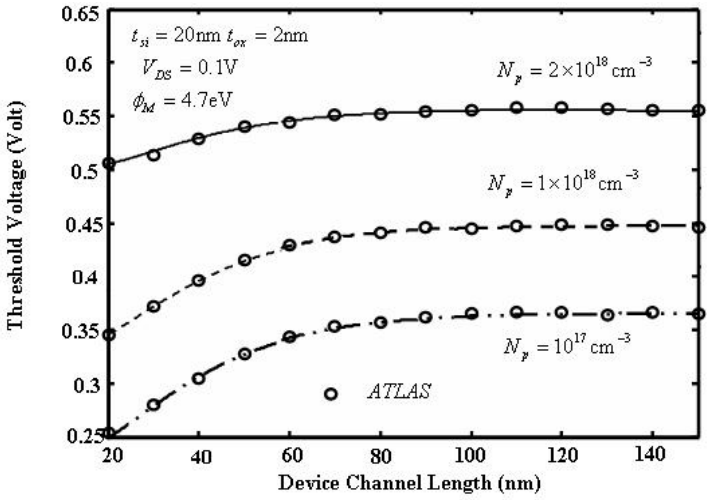

Fig. 4 *– Variation of threshold voltage with channel length for different channel doping*

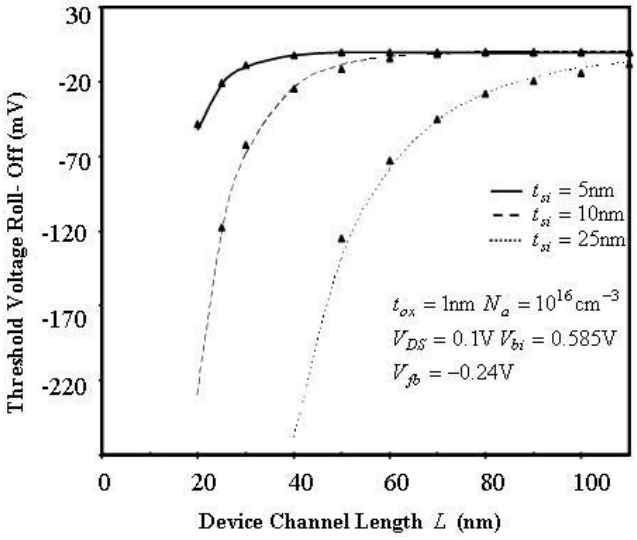

Fig. 5 *– ΔV_{th} with channel length for t_{ox} = 1 nm*

thicknesses t_{si} and gate-oxide thicknesses of $t_{ox} = 1$ nm. At higher channel thickness threshold voltage roll-off increases severely because gate losses it control over the channel. Further threshold voltage roll-off ΔV_{th} is shown with channel length in Fig. 6 for $t_{ox} = 1.5$ nm. Thicker gate oxide is responsible for the larger roll-off in threshold voltage.

4. CONCLUSION

In this paper, a threshold voltage model for short-channel DG MOSFET is presented. The effect of doping on threshold voltage is studied in detail. It

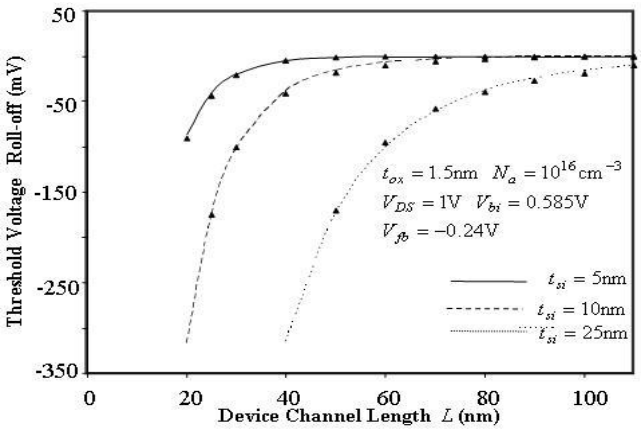

Fig. 6 – ΔV_{th} *with channel length for* t_{ox} = 1.5 nm

is found that unlike bulk MOSFET threshold voltage of DG MOSFET is constant for mild doping. Threshold voltage roll-off is improved for thinner silicon body and oxide thickness.

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