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ROLE OF INTERFACE CHARGES ON HIGH-K BASED POLY-SI AND METAL GATE NANO-SCALE MOSFETS

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*The characteristics of typical sub-*100 *nm high K gate dielectrics MOSFET with different gate materials are simulated by two dimensional device simulators (ATLAS and ATHENA). The impact of interface charges on the characteristics of Poly-*Si *and* TiN *metal gate MOSFETs are investigated. The simulation results shows that, at high interface charge densities, the devices with Poly-Si gate degrade much compared to metal gate MOSFET structures. Emphasis is given to study the mobility degradation which stands as a major hurdle with the implementation of high-k dielectrics in nano-scale devices. The advantages of using Watt model over other models for the extraction of channel mobility is also clearly explained. The performance of the high-k MOSFET with metal electrode and poly-silicon electrode is also compared for various interface state charges.*

Keywords: *MOSFET, HIGH-K, INTERFACE CHARGES, MOBILITY, METAL GATES.*

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1. INTRODUCTION

The need for high drivability with low standby power consumption has made the high-k dielectrics indispensable in advanced Complementary Metal Oxide Semiconductor (CMOS) devices. In devices with a channel length of 100 nm or below, the oxide thickness reduces to below 3 nm as per scaling laws. Dielectric thicknesses lower than 3 nm result in quantum mechanical tunneling through the device. This results in tunneling of charge carriers through the gate oxide into the channel and increase in leakage current through the device [1]. Passage of charge carriers through the thin oxide layer may result in creation of traps which further results in oxide degradation and breakdown [2, 3]. For this reason high-k materials are used to physically increase the thickness of the gate dielectric without reducing the effective gate capacitance. However, the use of high K dielectric on MOSFET does not just simply increase the thickness of high K dielectric layer but also affects the characteristics of MOSFETs which needs to be studied in detail. As-deposited HfO_2 layer have a number of defects which results in increased fixed oxide and interface charges [4-5]. These charges are formed during the high-k deposition and/or post deposition processing which affect the device performance. Another unresolved issue that still affects high-k MOSFETs is the reduction of channel effective carrier mobility. Various sources of this degradation like Remote Coulomb Scattering (RCS), Remote soft-optical Phonon Scattering (RPS), interfacial layer thickness, permittivity and

roughness have been identified. Yet there has been no consensus on which particular phenomenon dominates [6-7]. Hence, the role of interface charges on mobility and other device figures of merit should be investigated.

2. DESIGN AND SIMULATION

In our study, we have process modeled 0.1 μm n-channel MOSFETs using HfO_2 as gate dielectric material. Two MOSFET structures, one with Poly-Si gate and the other with TiN metal gate electrode were designed using ATHENA 2D simulator of the SILVACO© suite. The simulated structures, which are based on fully scaled 100 nm gate length MOSFET's proposed in the International Technology Roadmap for Semiconductors (ITRS) [8], have gate length of 100 nm, with effective oxide thicknesses (EOT) of 3 nm. The dielectric constant of HfO_2 gate dielectric was considered to be 20 [9]. The substrate doping concentration is $N_{sub} = 3 \times 10^{17}$ cm^{-3}. The source / drain extensions and deep source/drain junction depths are 45 and 75 nm, respectively. Titanium Silicide is used at source drain contacts to reduce the sheet resistance. The gate work-function for TiN is chosen to be 4.5 and 4.17 for Poly-Si. Once the process modeling is done in ATHENA, the device is simulated in ATLAS to determine the device characteristics. The device parameters were studied for three surface state densities viz. 5×10^{11} Charges/cm^2, 1×10^{12} Charges/cm^2, 5×10^{12} Charges/cm^2. The schematic of the design structure with TiN metal gate is as shown in Fig. 1.

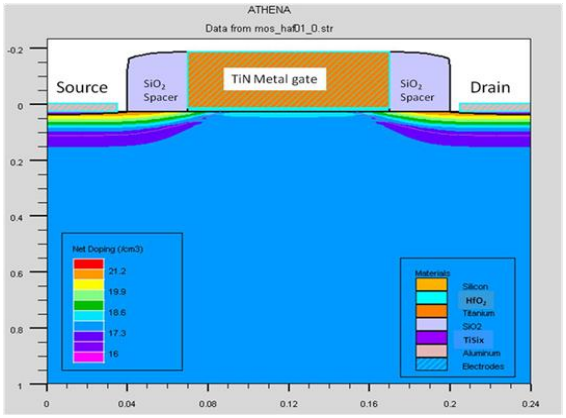

Fig. 1 *– Simulated structure of* TiN *gate MOSFET*

3. RESULTS AND DISCUSSION

We have investigated the effect of interface charges on the performance of both Poly-Si and metal gated MOSFETs. It is seen from Fig. 2 that threshold voltage of both the design structures decreases with increase in interface charges. The degradation is found to be more in case of Poly-Si gated device structure than device with metal gate at higher interface charge densities. The threshold voltage degradation results in increased current (I_D) in the devices with increase in interface charge density. The trans-conductance (g_m) also decreases for the same. Sub-threshold swings ($1/S$) and drain current (I_D) increases. On comparison with poly Si electrode, metal gate electrodes seem to

perform better with a more I_D, transconductance and lower sub-threshold swing. This proves that high-k dielectrics perform better in combination with metal gates. The simulated results are summarized in Table 1.

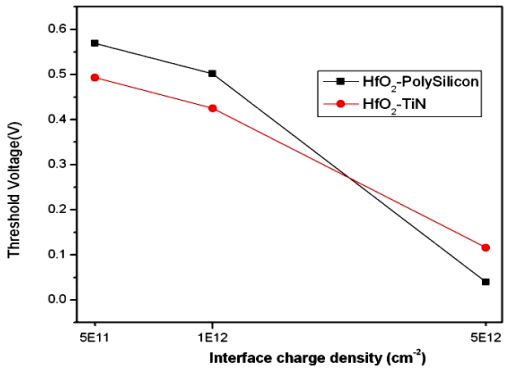

Fig. 2 *– Threshold voltage degradation of Poly-Si and TiN gate MOSFET*

Table 1 *– Simulated results of MOSFET structures for various interface charge densities*

Interface Charges (cm^{-2})	Design Structure	V_T (V)	I_D (mA/μm)	g_m ($\times 10^{-4}$ mho)	$1/S$ (mV/decade)	R_O (Ohms)
5×10^{11}	HfO_2-TiN	0.49	0.73	7.12	74.48	13159
	HfO_2-Poly Si	0.56	0.31	5.86	85.66	20573
1×10^{12}	HfO_2-TiN	0.42	0.79	7.15	75.59	12768
	HfO_2-Poly Si	0.50	0.36	5.92	85.62	19166
5×10^{12}	HfO_2-TiN	0.11	1.32	6.75	196.58	10488
	HfO_2-Poly Si	0.04	0.81	5.59	162.5	13104

Among various challenges presented by high-k gate oxides, mobility degradation has received the utmost attention as it proposes a serious concern when it comes to MOSFET performance. Hence it is very important to accurately model the effective mobility of the carriers in Silicon MOSFET. The total mobility in the inversion layer is given by Matthiessen's rule which is formulated as follows:

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{coul}}$$

Where, μ_{total} is the total mobility in the inversion region, μ_{ph} is mobility due to phonon scattering, μ_{sr} is mobility due to surface scattering and μ_{coul} is mobility due to coulombic scattering. Numerous models have been included in the ATLAS viz. CVT (Lombardi's model), Watt, modified Watt, SHI (Shirahata's model), CONMOB (concentration dependent low field mobility), FLDMOB (transverse electric field dependent mobility), KLA (Klaassens' low field mobility), modified CVT, YAMAGUCHI and TASCH model. Most of

these models have the Matthiessen's rule built within them. However all these models have some trade-off. The Watt [10] model includes all the effects of phonon scattering, surface roughness scattering and charge impurity scattering effects caused by the inversion charge carriers and the ions located in the oxide and interfaces. This was in line with our requirements. Hence this model was selected specifically to show the scattering effects due to interface charges in high-k materials. The role of interface charges on the high field mobility of TiN metal gated and Poly-Si gated MOSFET structures are shown in Fig. 3 and Fig. 4, respectively. It can be observed that the electric field increases with the increase in interface charges while the mobility degrades.

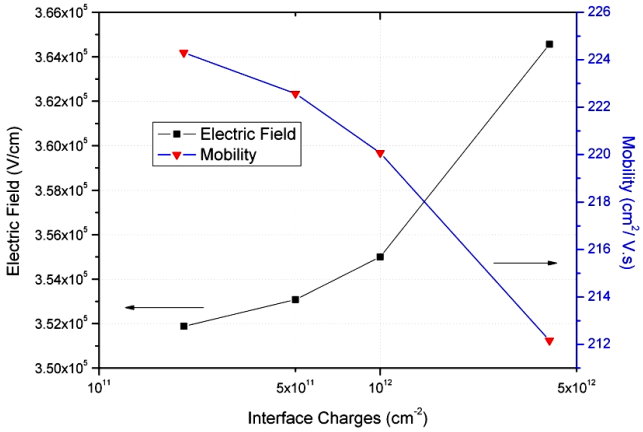

Fig. 3 *– Channel mobility of* TiN *gated MOSFET structure for various interface charge densities*

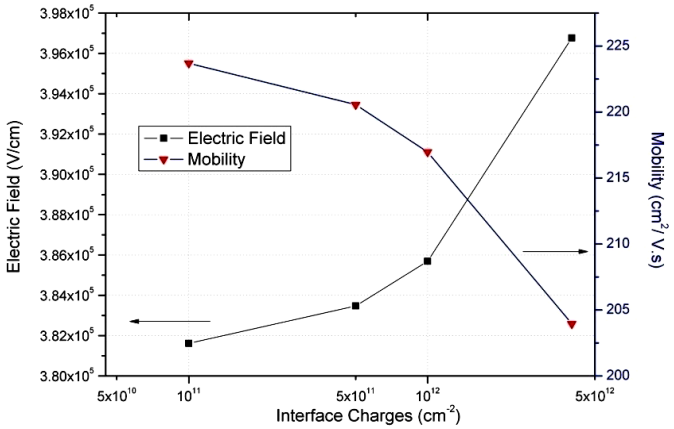

Fig. 4 *– Channel mobility of Poly-*Si *gated MOSFET structure for various interface charge densities*

The components affecting the effective mobility of the carriers in the transistor channel are the horizontal electric field, vertical electric field and carrier velocity. As devices are reduced in size, the electric field typically

also increases and the carriers in the channel have an increased velocity. However at high fields there is no longer a linear relation between the electric field and the velocity. When the horizontal electric field is high, the carriers in the transistor channel are accelerated to a maximum velocity. Above a critical field, the velocity is no longer related to electric field and reaches a constant level. This velocity saturation is caused by the increased scattering rate of highly energetic electrons, primarily due to optical phonon emission. This effect increases the transit time of carriers through the channel. When the vertical electric field is high the carriers in an n channel device are strongly attracted to the silicon surface where they rebound. This results in surface scattering causing a reduction in the recombination time and the mobility of the carriers [11]. Surface scattering due to irregularities of the surface near the interface and coulomb scattering due to presence of interface charges very near to the interface can be considered as the main reasons for mobility degradation.

4. CONCLUSION

The role of interface charges on the high-k based MOSFETs have been compared for Poly-Si and metal gate electrodes. At high interface charge densities, the MOSFET with Poly-Si gate are found to degrade more compared to metal gate structures. The replacement of polysilicon with metal gate seems to tackle the mobility degradation issue in high-k based devices to a greater extent. The non-linearity of mobility curves at high electric fields has been studied for various interface trap densities. The Watt model was found to be the most suitable model for mobility extraction, which includes most of the scattering phenomena.

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