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MANUFACTURING PRACTICES FOR SILICON-BASED POWER DIODE IN FAST RECOVERY APPLICATIONS

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This paper reports a fast recovery semiconductor diode that was developed for use in high power applications. The diode constructed in disc-type ceramic package with a peak-inverse voltage rating of 2800 *V and current rating of* 710 *A was fabricated using float-zone (FZ) silicon wafer as the starting raw material. Alternate processes viz. gold diffusion, gamma irradiation and electron irradiation were explored for control of carrier lifetime required to tune the switching response of the diode to the desired value of* 8 *μs. The paper compares the results of these alternate processes. The diodes were fabricated and tested for forward conduction, reverse blocking and switching characteristics. The measured values were observed to be comparable with the design requirements. The paper presents an overview of the design, manufacturing and testing practices adopted to meet the desired diode characteristics and ratings.*

Keywords: *SEMICONDUCTOR DEVICES, FAST RECOVERY DIODES, ELECTRON IRRADIATION, GOLD DIFFUSION, REVERSE RECOVERY CHARACTERISTICS.*

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1. INTRODUCTION

Development of power semiconductor diodes involves a series of design steps that include computation of the silicon wafer parameters, framing of manufacturing process parameters, selection of encapsulation components and preparation of a suitable test plan that helps to verify and validate the design. The paper details the approach adopted in the design, the manufacturing process steps and the tests carried out in the development of the 2800 V / 710 A disc-diode of fast recovery type with a reverse recovery time of 8 μs.

2. SELECTION OF SILICON WAFER

Silicon wafer, used as raw material to manufacture the high power diodes, has a crystal orientation ⟨111⟩ grown using Float-zone technique and doped uniformly as n-type using Neutron Transmutation Doping. The level of n-type doping, defined in terms of phosphorus atoms per cm^3 and resistivity (Ω-cm), is chosen based on the peak inverse voltage requirement (U_{RRM}) using the relationship

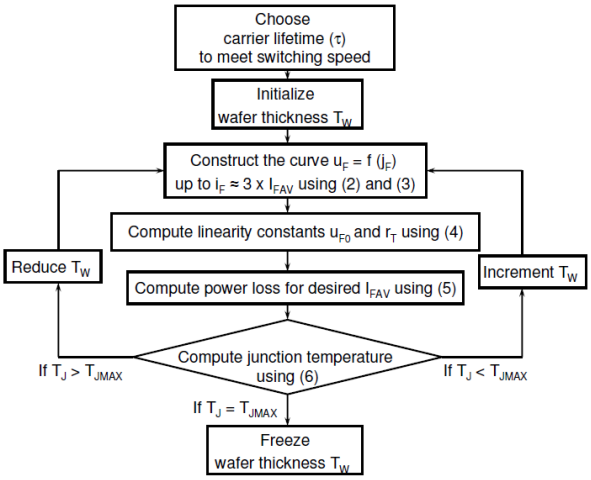

Fig. 1 *– Flow-chart showing design steps in selection of silicon wafer thickness*

$$\rho = A(U_{\mathrm{RRM}})^B \tag{1}$$

where ρ is the resistivity and A, B are constants that depend upon the deep-junction profile of the p-type dopant in the vicinity of the p-n junction and also the wafer thickness, T_W [1, 2]. In an industrial situation, A and B are established empirically based on the measured data of reverse voltage corresponding to known values of resistivity and wafer thickness, taking into account the appropriate design margins. Usually, a p^+-p-n-n^+ structure is employed, where the heavily doped n+ layer acts as a field-stop layer to curtail the electrical field distribution abruptly within the rated voltage U_{RRM}. This is to limit the thickness of the wafer to a minimum value that provides the desired current rating, since a higher wafer thickness results in higher power loss due to increased conduction drop [3]. The following relationships (2) – (6) help in establishing the wafer thickness. The design approach to select the thickness is as shown in Fig. 1. Forward current density is given by the relationship

$$j_F = i_F/A, \tag{2}$$

where A is the cross sectional area based on chip diameter that is limited by the chosen diode package. Forward conduction drop is given by the relationship,

$$u_F = f(\tau, T_W) \text{ for a given } j_F, T_J \tag{3}$$

where τ is carrier lifetime that is selected appropriately to achieve the switching speed of 8 μs, T_W is wafer thickness and T_J is junction temperature. Forward conduction characteristic curve, with linear approximation, is governed by the relationship

$$u_F = f(i_F) \approx U_{F0} + r_T . i_F \tag{4}$$

where U_{F0} and r_T are constants representing the linear line. Average power loss is governed by the relationship

$$P = U_{F0}\, I_{FAV} + r_T\, (I_{RMS})^2 \tag{5}$$

where I_{FAV} is the average conduction current and I_{RMS} is the corresponding rms value of the waveform. The desired rating of this diode is $I_{FAV} = 710$ A with $I_{RMS} = (\pi/2) \times I_{FAV}$ for single-phase, half sine waveform. Max Junction temperature is governed by

$$T_{JMAX} = T_{CMAX} + P.\, R_{TH,J\text{-}C}, \tag{6}$$

where T_{CMAX} is the maximum allowable case temperature of the diode, $R_{TH,\,J\text{–}C}$ is thermal resistance between p-n junction and outer case of the diode. For this diode, the current rating is specified at T_{CMAX} of 100 °C and the chosen diode package offers a thermal resistance of $R_{TH,J\text{-}C}$ of 0.035 K/W.

3. SEMICONDUCTOR STRUCTURE OF DIODE CHIP

The semiconductor structure of the diode is p^+-p–n-n^+, which is basically a simple p-n junction with heavily doped p^+ and n^+ regions on either side. The design principles adopted for construction of the structure are as follows:

(a) The p-n junction shall have a deep-junction gradient profile.

(b) The p-side and n-side shall be sufficiently wide to accommodate the depletion region at the rated reverse voltage U_{RRM}.

(c) The n^+ and p^+ shall be heavily doped ($\approx 10^{20}$ atoms per cc) to inject sufficient electrons and holes into the middle n-type base region in order to minimize the resistance during forward conduction and, also to offer ohmic contact with the respective cathode and anode electrodes.

4. MANUFACTURING OF THE DIODE CHIP

The manufacturing process chart is as shown in Fig. 2. The p^--n-n^+ structure of the diode is fabricated using a double p-type diffusion process (Aluminium and Boron as dopants) followed by n^+ diffusion using phosphorus as dopant. The silicon wafer is then attached to a molybdenum disc on the anode side using a high-vacuum (10^{-6} Torr) brazing process using

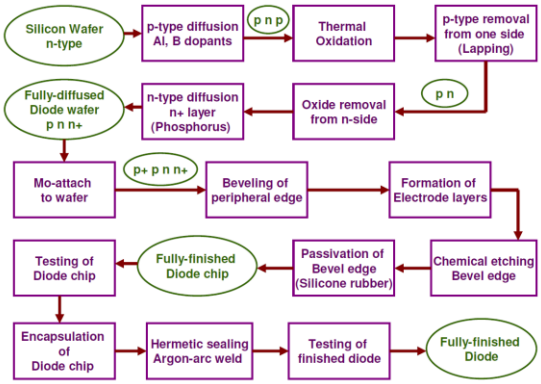

Fig. 2 *– Process flow diagram adopted for manufacturing of fast recovery diode*

an Aluminium-based solder alloy that helps to realize the p^+-p-n-n^+ structure. Physical Vapour Deposition (PVD) process is employed to deposit high purity metal layers that act as anode and cathode electrodes. The circular periphery of the diode chip is shaped at an angle using surface-lapping and chemical-etching procedures in order to minimize the value of surface electric field during blocking mode operation of diode [4]. A suitable rubber coating is then formed on the beveled edge to neutralize surface charges present on the silicon surface and to complete the fabrication of diode chip that is ready to encapsulate. The final structure of the diode chip is as shown in Fig. 3.

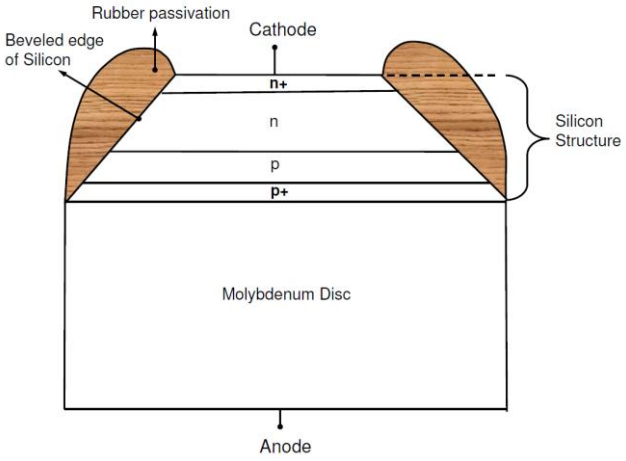

Fig. 3 *– Cross-section view of the structure of semiconductor diode chip*

5. CONTROL PROCESS FOR FAST RECOVERY CHARACTERISTICS

Reverse recovery characteristic is determined by the speed with which the diode turns off from its conduction state. Higher the recombination rate of electron-hole pairs, faster is the switching. Energy levels introduced deep into the forbidden energy gap of silicon act as traps and expedite the rate of recombination by capturing the electrons and holes. Introducing gold impurities into silicon crystal structure, prior to attaching molybdenum disc to the silicon wafer, is one method of creating deep energy levels [5].

An alternative method is to expose the fully-finished diode chip to high energy particles such as gamma, electron, etc [6]. In the present case, both possibilities were explored. Gamma irradiation was found ineffective, as no significant changes were observed in the recovery characteristics even with repeated and long-duration exposures. With the other two methods viz. gold diffusion and electron irradiation, the target recovery time t_{RR} was achieved within the specified 8 μs. The forward voltage drop (U_F), which increases with recombination rate, was also found within the upper specification limit. However, gold diffusion gave rise to substantially higher reverse leakage current as compared to electron irradiation. Fig. 4 compares the measured reverse I-V characteristics of gold-diffused and electron-irradiated diode chips of similar U_F and t_{RR} values. The leakage current is observed to be considerably lower in the entire range of blocking voltage for the electron-irradiated chips.

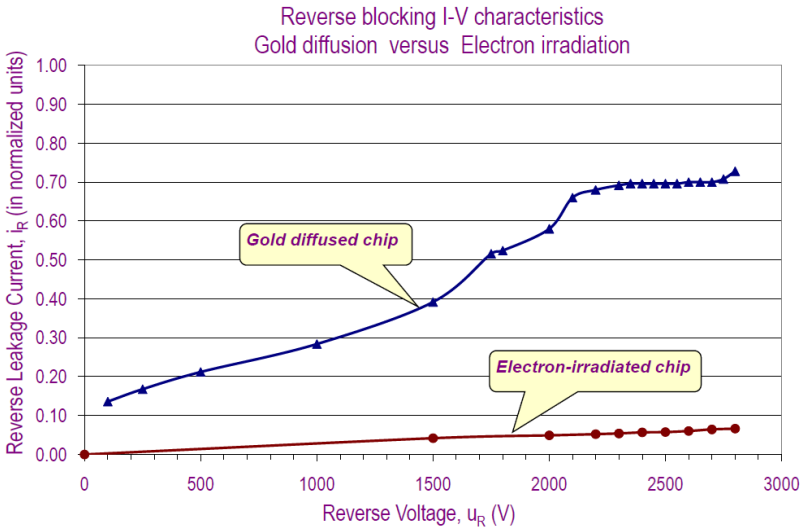

Fig. 4 *– Comparison of measured I-V characteristics of gold diffused and electron irradiated diode chips of similar switching speed and forward conduction drop*

Based on this result, electron irradiation was adopted as the optimum process. For the purpose of selection of appropriate dose of irradiation (in Grays), an empirical relationship was established by measuring the reverse recovery time, t_{RR} (switching speed) at different irradiation doses. Fig. 5 shows the empirical dosage chart constructed for the selection of dosage required to lower the t_{RR} value from its original value (t_{RR0}) to the target range (t_{RRE}).

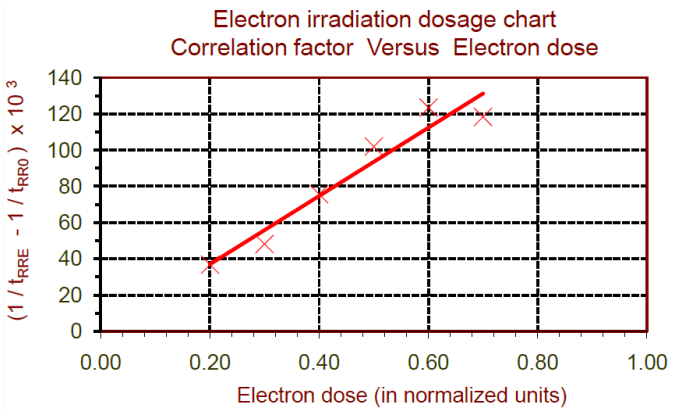

Fig. 5 *– Electron irradiation dosage chart used for selection of dose based on initial and target tRR values*

6. ENCAPSULATION

The electron-irradiated diode chip is further encapsulated in a disc-type package that has ceramic isolation between cathode and anode. The external contact surfaces are nickel plated to protect the diode against corrosion. The internal build-up components along the path of current transport are made of

high-conductivity copper to minimize electrical and thermal resistance. Stress-relieved silver contacts are used between the adjacent components to compensate for camber and surface roughness in the assembly components. Teflon-based insulation is used, wherever required. The diode capsule is hermetically sealed using a suitable method that fuses the capsule along the circular periphery. The outline diagram of the complete diode is shown in Fig. 6.

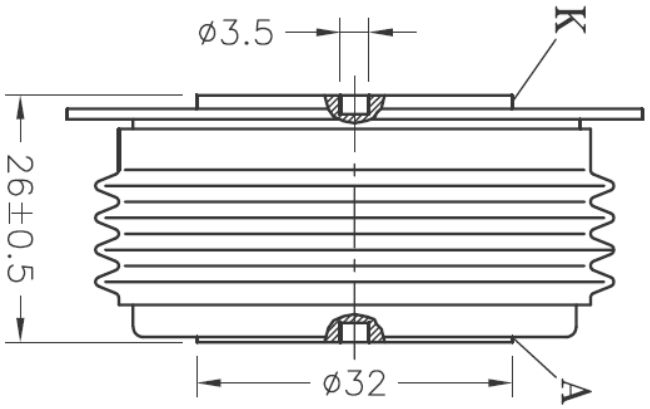

Fig. 6 *– Outline diagram of the disc-type fast recovery diode*

7. TESTING AND CHARACTERIZATION

The fabricated diodes were tested as per IEC 60 747-2:

(a) Encapsulation test to check the leak rate of the inert gas within the capsule. Helium Mass Spectroscopy Leak detection method is used for this purpose.
(b) Forward voltage drop test (U_F) at 3000A, 15 kN, T_{JMAX}
(c) Reverse leakage current test (I_R) at 2800V, T_{JMAX}
(d) Reverse voltage test (U_R) at 50 mA, T_{JMAX}
(e) Reverse recovery charge, current and time (Q_{RR}, I_{RR}, t_{RR} at T_{JMAX})
(f) High temperature reverse bias (HTRB) storage test for 16 hours at rated temperature T_{JMAX} and at applied reverse bias of 100% U_{RRM} (2800V)
(g) Thermal resistance test (R_{TH})

All measured device parameters are observed to be within the acceptance limits. In Fig. 7, a plot of the measured forward I-V characteristics at T_{JMAX} is given. The measured values of threshold voltage and forward slope resistance, U_{F0} and r_T (0.90 V, 0.28 mΩ) respectively, are within the design limits (0.98V, 0.45mΩ). The measured range of thermal resistance values (0.025-0.027 K/W) are also within the design limit of 0.035 K/W. The achieved values of U_{F0}, r_T and R_{TH} validate the design requirements of power loss and current rating at maximum junction temperature. Long-term reverse voltage stability of the diode is verified by the burn-in test (HTRB) conducted on 100% sampling basis. In this test, the change in reverse voltage is recorded at rated leakage current of 50 mA before and after subjecting the diodes to the rated reverse bias of 2800 V at T_{JMAX} for 16 hours.

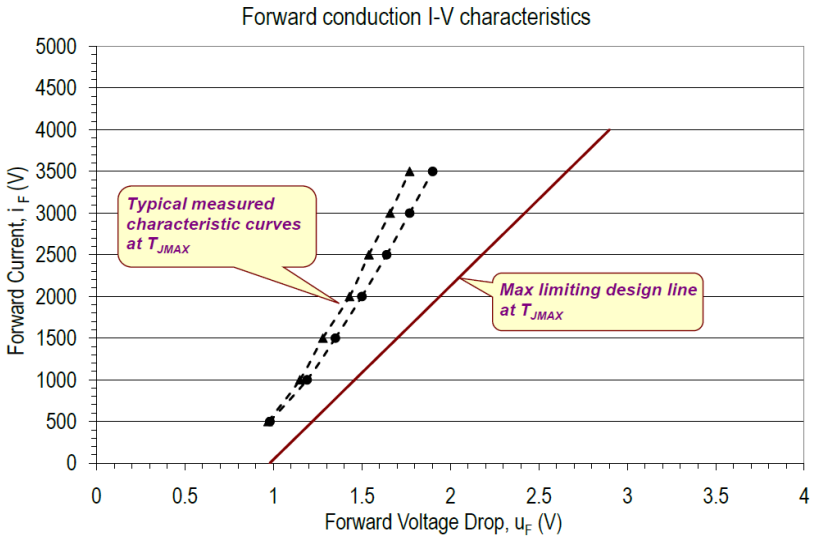

Fig. 7 *– Forward conduction characteristics – measured curve versus limiting design curve*

8. SUMMARY

Disc-type fast recovery diode of rating 2800 V, 710 A, 8 μs for use in high power applications was designed and developed. Alternative processes were explored for control of switching speed. High energy electron irradiation was found to be an optimum process satisfying both the static reverse blocking and the transient switching parameters. The characteristics of the diodes fabricated were measured through various tests and found to conform to the design specifications. This diode design has an inherent advantage in the economic selection of snubber circuits by virtue of its faster response and consequently, facilitates efficient space management for the circuit designer in critical applications such as generators where the size is a significant factor for the rectifier.

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REFERENCES

1. S.M. Sze, K.K. Ng, *Physics of Semiconductor Devices*, (John Wiley & Sons, 3rd Edition: 2006).
2. B.J. Baliga, *Fundamentals of Power Semiconductor Devices*, (Springer-Verlag New York, LLC: 2008).
3. F. Berz, *Solid State Electron.* **20**, 709 (1977).
4. V.A.K. Temple, M.S. Adler, *IEEE T. Electron. Dev.* **23**, 950 (1976).
5. B.J. Baliga, E. Sun, *IEEE T. Electron. Dev.* **24**, 685 (1977).
6. R.O. Carlson, Y.S. Sun, H.B. Assalit, *IEEE T. Electron. Dev.* **24**, 1103 (1977).