

Design and Implementation of a Hybrid SET-CMOS Based Sequential Circuits

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Single Electron Transistor is a hot cake in the present research area of VLSI design and Microelectronics technology. It operates through one-by-one tunneling of electrons through the channel, utilizing the Coulomb blockade Phenomenon. Due to nanoscale feature size, ultralow power dissipation, and unique Coulomb blockade oscillation characteristics it may replace Field Effect Transistor (FET). SET is very much advantageous than CMOS in few points. And in few points CMOS is advantageous than SET. So it has been seen that Combination of SET and CMOS is very much effective in the nanoscale, low power VLSI circuits. This paper has given an idea to make different sequential circuits using the Hybrid SET-CMOS. The MIB model for SET and BSIM4 model for CMOS are used. The operations of the proposed circuits are verified in Tanner environment. The performances of CMOS and Hybrid SET-CMOS based circuits are compared. The hybrid SET-CMOS circuit is found to consume lesser power than the CMOS based circuit. Further it is established that hybrid SET-CMOS based circuit is much faster compared to CMOS based circuit.

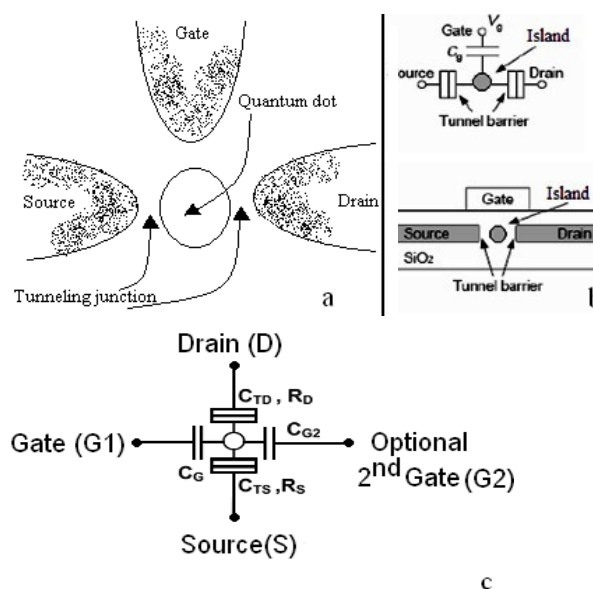
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1. INTRODUCTION

For the improvement of the VLSI devices a new strategy was taken, that is the downscaling of the devices. However, there have been reports suggesting that the MOS transistor cannot shrink beyond certain limits said by its operating principle [1]. Over recent years this realization has led to exploration of possible successor technologies with greater scaling potential such as single electron device technology. Single Electron Device (SED) Technology is the most promising future technology to meet the demand for increase in density, performance and decrease in power dissipation in future VLSI circuits. The Single Electron devices have potential to manipulate electrons on the level of elementary charge, are thus considered to be the devices that will allow such a charge. In addition to their low-power nature, the operation of SED is more guaranteed even when device size is reduced to the molecular level. It is also mentionable that the performance of the SED improves as its size reduces more. These properties are quite beneficial for large scale devices. The most important three-terminal SED is single-electron transistor. The schematic structure of SET is shown in Fig. 1. As shown in the figure, the structure of SET is almost same as that of a MOSFET. The SET has one Coulomb blocked island. It has another voltage source and tunnel capacitor. The electrode with the normal capacitor is gate and other two electrodes are drain and source.

SET has attracted attention as a candidate for future VLSI mainly due to its three virtues: nanoscale feature size, ultralow power dissipation, and unique Coulomb blockade oscillation characteristics. In spite of such interesting properties, the practical implementation of the SET is questionable because of its low current drive and lack of mature room temperature

**Fig. 1** – Schematic structure of SET and its equivalent circuit

operable technology. A comparison between the advantages and limitations of CMOS and SET technologies is presented in Table 1.

From this table it is seen that SET has much more advantages than CMOS. But it has its limitations too. However, Table 1 also suggests that CMOS and SET are rather complementary. SET advocates low power consumption and new functionality (related to the Coulomb blockade oscillations), while CMOS has advantages such as high-speed driving and voltage gain that can compensate for the intrinsic drawbacks of SET. Though a complete replacement of CMOS by SET is not easy, but simultaneously it is also true that the combination of SET and CMOS can bring a new era in

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Table 1 – Comparison between Advantages and Limitations of SET and CMOS Technologies

	SET	CMOS
Advantages	Nanoscale feature size. Unique Coulomb blockade. Ultralow power dissipation. Oscillation characteristics.	High gain and current drive. High speed technology Very matured fabrication.
Disadvantages	Low current drive Lack of room temperature operable technology. Background charge effect	Sub-10-nm physical limits. Power density.

VLSI technology. Already these thoughts have drawn the attentions in academia and industry. Toshiba has recently demonstrated the performance of a hybrid MOS-SET inverter (see Fig. 1) on a SOI wafer [2, 3]. The unique periodic Coulomb blockade oscillation feature of the SET can be exploited to engender several novel analog functionalities, which are very difficult to realize in a pure CMOS approach. In this paper we have discussed how we can make Sequential circuits using Hybrid SET CMOS and how it is more advantageous than the same circuit built by CMOS only. In this paper we have designed a Master-slave J-K flip-flop, and using that we have designed D flip-flop, T flip-flop, 2 bit ring counter. All the circuits are verified by means of T-Spice simulation software. The MIB compact model for SET devices and BSIM4.6.1 model for CMOS are used. This paper is been done according to our concept, you may follow some better one if you want.

2. SINGLE-ELECTRON TRANSISTOR (SET)

We have to understand that the characteristics of SET are different than the characteristics of CMOS. A Single electron transistor is based on tunnel junction. The two tunnel junctions create what is known as a “Coulomb island or Quantum dot” that electrons can only enter by tunnelling through one of the insulators. A tunnel junction and its schematic diagram are shown in Fig. 2. The transport of electron through a tunnel junction is called tunnelling. Through a tunnel junction electrons tunnel one after another [4, 5]. Even only one electron tunnelling may produce a charge e/C across the tunnel junction (where C is total capacitance and $e = 1.602 \times 10^{-19}$ C). The critical voltage V_C , It is the threshold voltage, which is needed across the tunnel junction to make a tunnelling event. This threshold voltage can be calculated with the equation [1]

$$V_C = 0.5e/(C_e + C_T) \tag{1}$$

C_T is the junction capacitance and C_e is the equivalent capacitance for remainder circuit as viewed from the tunnel junction’s perspective. Tunnel event will occur across the tunnel junction if and only if the voltage across the tunnel junction is greater than or equal to the threshold voltage (V_C), otherwise the tunnel event cannot occur.

An SET can be made by placing two tunnel junctions in series. These two tunnel junctions create “Quantum dot” (Fig. 3). Electrons have to pass through at least one insulator to enter into the dot. The SET

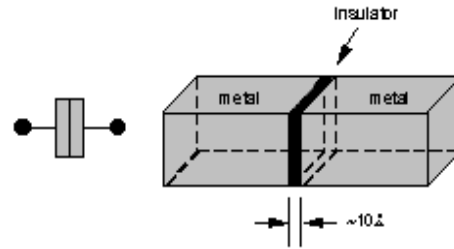


Fig. 2 – Schematic structure and symbol of tunnel junction

has three terminals like an ordinary Field Effect Transistor: source, drain and gate. The gate terminal is capacitively coupled to the node between the two tunnel junctions. The capacitor may seem like a third tunnel junction, but it is much thicker than the others so that no electrons can tunnel through it. The capacitor simply serves as a way of setting the electric charge on the coulomb island.

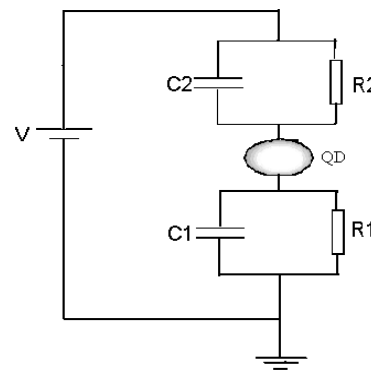


Fig. 3 – Quantum dot structure

For normal operation of the SET, electrons have to tunnel through the junction from the source to the drain via the central island. In order for tunnelling to happen, it is required that the charging energy E_C should be greater than the thermal energy and also the tunnelling resistance R_T should be greater than the resistance quantum h/e^2 . Therefore the conditions for observing single-electron phenomenon is expressed as $E_C = e^2/2C_\Sigma \gg K_B T$ and $R_T \gg h/e^2$ where C_Σ is the total island capacitance with respect to the ground, K_B is the Boltzmann’s constant, T is the temperature and h is the Planck’s constant. SETs may also have an optional 2nd gate connected to the island that can be used for controlling the phase shift of coulomb oscillation. The circuit schematic of such an SET is shown in Fig. 1(c). In the schematic diagram, C_{TD} is the drain tunnel junction capacitance, C_{TS} is the source tunnel junction capacitance, R_D is the drain tunnel junction resistance, R_S is the source tunnel junction resistance, C_G is the gate capacitance and C_{G2} is the optional 2nd gate capacitance.

3. MIB MODEL: A QUASI-ANALYTICAL SET MODEL FOR FEW ELECTRONS CIRCUIT SIMULATION

Single Electron Transistors (SETs), which are attractive candidates for post-CMOS VLSI and hybrid (CMOS-SET) ICs due to their ultra-small size and low power dissipation, demand accurate analytical models

in order to obtain more insights into SET characteristics and to design SET/hybrid circuits, rather than Monte-Carlo (MC) simulation [6, 7] or macro-modeling [8], [9]. The MIB model obeys the orthodox theory of single-electron tunnelling and the interconnect capacitances associated with the source, drain and gate are much larger than the device capacitance so that the total capacitance of the island with respect to ground will be equal to the summation of all device capacitances i.e. $C_{\Sigma} = C_{TD} + C_{TS} + C_{G1} + C_{G2}$. The MIB model has been developed in three major steps [10]:

- calculation of the island potential;
- shifting the drain current window;
- calculation of the drain current.

The drain current in the MIB model is computed from reference no [10].

4. HYBRID CMOS SET SEQUENTIAL CIRCUITS

An SET can be made to function as a switch by pushing into the Coulomb blockade state (OFF condition) or allowing it to conduct current (ON condition), it is possible to mimic MOSFET logic architecture in order to develop a hybrid CMOS-SET logic family. It is formed by a PMOS transistor as the load resistance of an SET. It may also be noted that in the gates in these design, PMOS transistor has the SET as its load. Although these resemble CMOS inverter, there are two differences:

- the pull transistor is an SET;
- V_{DD} is defined by the SET device parameters.

Here we have implemented sequential circuits. First we have implemented a Master-slave J-K flip-flop, and using that we have implemented D flip-flop, T flip-flop and 2 bit ring counter.

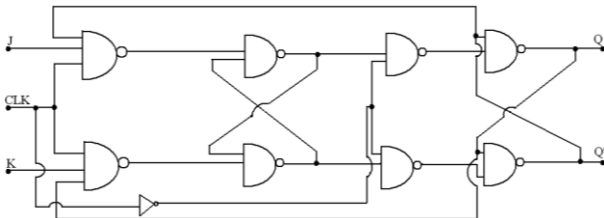


Fig. 4 – Master-slave J-K flip-flop

In Fig. 5, there is a J-K Master-slave flip-flop circuit. In this paper every gates are replaced using hybrid CMOS-SET. The total circuit is made of hybrid SET-CMOS NAND gate. In Fig. 5, 3 input NAND and 2 input NAND gates are shown.

Using these hybrid NAND gates and hybrid NOT gate (Fig. 6) we have replaced all the gates of the circuit. The operations of the gates are discussed below.

4.1 Operation of a 2 i/p NAND Gate

1. When $I/P1 = 0$ and $I/P2 = 0$

V_{gs} of M1 will be $-0.8V$ ($0-0.8V$) and also V_{gs} of M2 will be $-0.8V$ ($0-0.8V$). Since the gate voltages are negative with respect to sources, both M1 and M2 are ON. Since the gate voltages of SET1 and SET2 are equal to $0V$, both SETs are OFF.

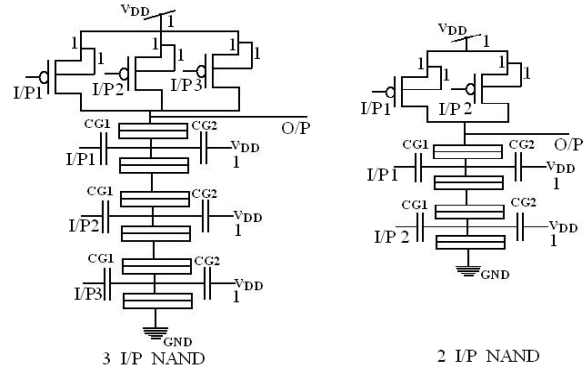


Fig. 5 – 3 input NAND and 2 input NAND gate

With SET1 &n SET2 OFF, V_{OUT} is connected to V_{DD} via M1/M2 and the Output is high.

2. When $I/P1 = 0$ and $I/P2 = 1$

V_{gs} of M1 will be $-0.8V$ ($0-0.8V$) and also V_{gs} of M2 will be $0V$ ($0.8-V_{DD}$). Therefore M1 is ON and M2 is OFF. Since the gate voltage of SET1 is equal to $0V$ and SET2 is equal to $0.8V$, SET1 is OFF and SET2 is ON.

V_{OUT} is connected to V_{DD} via M1 and the Output is high.

3. When $I/P1 = 1$ and $I/P2 = 0$

V_{gs} of M1 will be $0V$ and V_{gs} of M2 will be $-0.8V$. Therefore M1 is OFF and M2 is ON. Since the gate voltage of SET1 is equal to $0.8V$ and SET2 is equal to $0V$, SET1 is ON and SET2 is OFF.

V_{OUT} is connected to V_{DD} via M2 and the Output is high.

4. When $I/P1 = 1$ and $I/P2 = 1$

V_{gs} of M1 will be $0V$ and V_{gs} of M2 will be also $0V$. Therefore, M1 is OFF and M2 is also OFF. Since the gate voltages of SET1 & SET2 are both equal to $0.8V$, both SETs are ON. With SET1 and SET2 ON, V_{OUT} is connected to ground via SET1 & SET2 and the Output is low.

Thus 3 input NAND gate also operate.

4.2 Operation of the NOT Gate: [11] (Fig. 6)

When V_{IN} is at $0V$ (Logic 0), the SET is in Coulomb blockade state (OFF condition), but the PMOS conducts. The output (V_{OUT}) is connected to V_{DD} via the PMOS and the output is high. When the input is equal to V_{DD} , the SET conducts but the PMOS remains OFF. Therefore, output V_{OUT} is low as it is shorted by the SET to ground. Thus we find NOT operation is performed here. Thus we can design any gate of digital circuits [11]. Here we have also designed D flip-flop (Fig. 8), T flip-flop (Fig. 9) and a 2 bit ring counter (Fig. 10). Fig. 7 shows the input-output voltage transfer characteristic of the hybrid inverter [11]. The output voltage gain is estimated to be about 4.8 as determined from the slope of the transitional region which guarantees possible signal transfer to the next logic gates. Since the SET and CMOS are placed in series, the hybridization is found to improve the gain of the inverter while the delay remains the same. In a pure

SET inverter, in logic 1 or 0 regimes the output V_{OUT} is not constant with V_{IN} and never reaches V_{DD} in contrast with CMOS inverter. But in our hybrid circuit, we found from the transfer characteristic that V_{OUT} is almost constant with V_{IN} in logic 1 or 0 regimes.

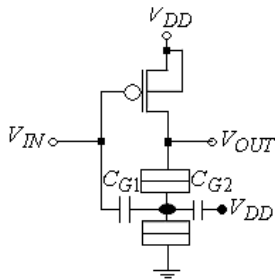


Fig. 6 – Circuit of hybrid SET-CMOS inverter. V_{IN} is the input voltage and V_{OUT} is the output voltage

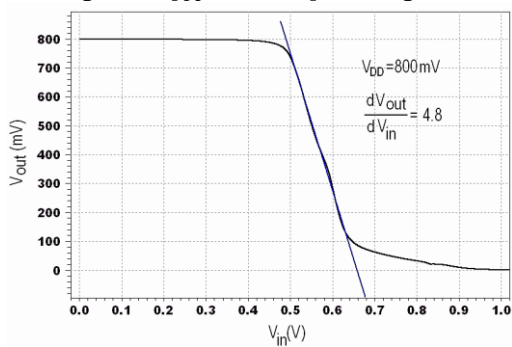


Fig. 7 – Input-output voltage transfer characteristic of the hybrid inverter [11]

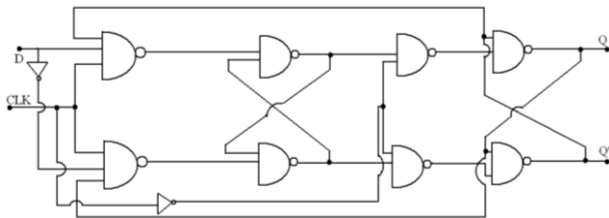


Fig. 8 – Master-slave J-K flip flop to D flip-flop

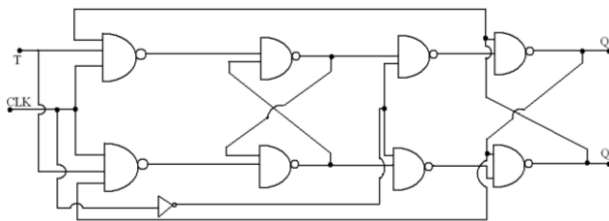


Fig. 9 – Master-slave J-K flip flop to T flip-flop

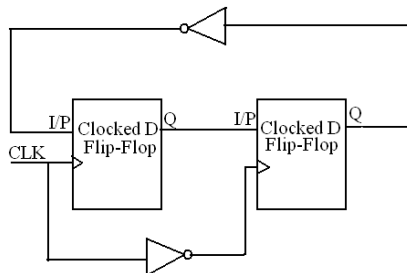


Fig. 10 – Master-slave J-K flip flop to T flip-flop

5. RESULTS AND DISCUSSION

The proposed circuits are simulated using the MIB compact model described by Analog Hardware Description Language (AHDL) for SET and BSIM4.6.1 model for MOSFET in Tanner environment. The values of the parameters used for our simulation are given in Table 2.

Table 2 – Values of Parameters used for the simulation

Device	Parameters	Voltage Level
SET	$R_{TD} = R_{TS} = 1 \text{ M}\Omega$, $C_{TD} = C_{TS} = 0.1 \text{ aF}$, $C_{G1} = 0.27 \text{ aF}$, $C_{G2} = 0.125 \text{ aF}$	Logic 0 = 0 V Logic 1 = 0.8 V $V_{DD} = 0.8 \text{ V}$
PMOS	$V_{TH} = -220 \text{ mV}$, $W/L = 100 \text{ nm}/65 \text{ nm}$ and default values of BSIM4.6.1 model for other parameters	

The logic operations of the circuits were first examined by simulation using T-Spice simulation software. The simulated input-output waveform is depicted in Figures. The logic operation is found to be correct. For Master-slave J-K flip-flop the simulation waveform is shown in the Figure 11. For T flip-flop the simulation result is shown in Fig. 12, the simulation waveform of D flip-flop is shown in Fig. 13 and the output of 2 bit ripple counter is shown in Fig. 14. The results obtained from the simulation are found to be satisfactory. The logic operations of the circuits are found to be satisfactory.

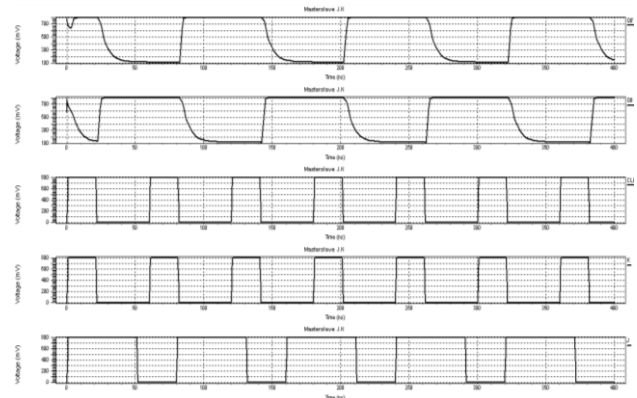


Fig. 11 – Master-slave J-K flip-flop

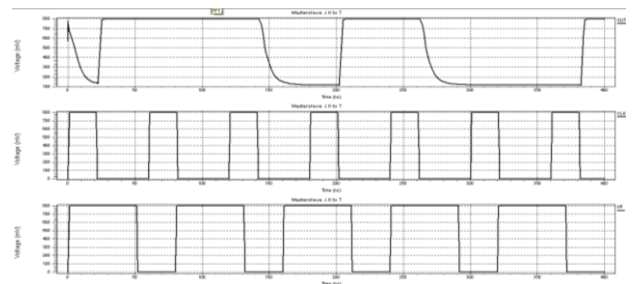


Fig. 12 – Master-slave J-K flip flop to T F/F

5.1 Power & Delay Calculation

We have taken an example of Master-slave J-K flip flop for calculating power & delay. For designing in CMOS technology, it consists of 2 nos of 3 input NAND gate & 7 nos of 2 input NAND gate. As per the parame-

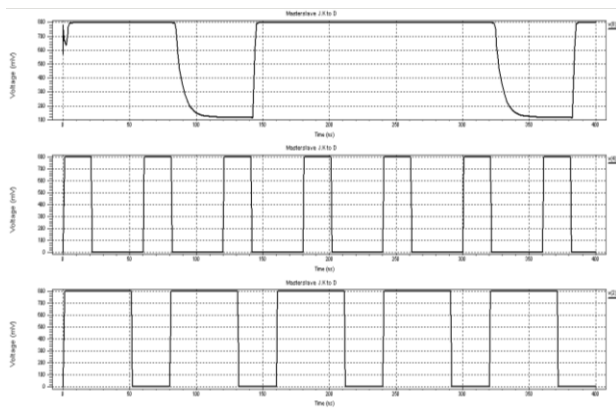


Fig. 13 – Master-slave J-K flip flop to D F/F

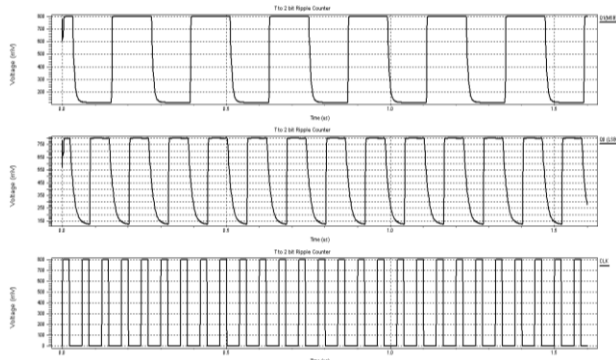


Fig. 14 – Master-slave J-K to 2 bit ripple counter

ters given above in Table 1, the power consumption of CMOS FET is 1000nW & delay is 40 ps.

The power consumption of each 3 input NAND gate and 2 input NAND gate are 6000 nW and 4000 nW successively. So, the total power consumption of the circuit is 40000 nW. In each 3 input NAND gate 3 nos of MOSFET in the PULLUP circuit are in parallel and 3 nos MOSFET in the PULLDOWN circuit are in series. So, the delay for one 3 input NAND gate is 160ps. Similarly for 2 input NAND gate, 2 nos of MOSFET in the PULLUP circuit are in parallel and 2 nos MOSFET in the PULLDOWN circuit are in series. So, the delay for one 2 input NAND gate is 120 ps. In the Master-slave J-K flip flop 2 nos of 3 input NAND gates are in parallel connection, but the other 6 nos 2 input NAND gates are in 3X2 series connection. So, the total delay will be 1 time delay of 3 input NAND gate and 3 times delay of 2 input NAND gate. The total delay for Master-slave J-K flip flop will be 520 ps.

For designing in Hybrid CMOS-SET technology,

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each 3 input NAND gate consists of 3 nos of CMOS Transistor in PULLUP network and 3 nos of SET in PULLDOWN network. As per the parameters given above in Table1,the power consumption of SET is 50 nW & delay is 1 ps. Power consumption of each 3 input NAND gate is 3150 nW.

Power consumption of each 2 input NAND gate is 2150 nW. So, the total power consumption of Master-slave J-K flip flop in Hybrid CMOS-SET technology is 21000 nW. Similar to the CMOS design, in each 3 input NAND gate, 3 nos MOSFET in the PULLUP circuit are in parallel connection and 3 nos of SET in the PULLDOWN circuit are in series connection. So, the delay for one 3 input NAND gate is 43 ps. Similarly for 2 input NAND gate, 2 nos MOSFET in the PULLUP circuit are in parallel connection and 2 nos SET in the PULLDOWN circuit are in series connection. So, the delay for one 2 input NAND gate is 42 ps. So the total delay for Master-slave J-K flip flop in Hybrid CMOS-SET design is 169 ps.

From the above calculation, we can show that Power Consumptions & delay are quite less in Hybrid CMOS-SET technology compared to CMOS technology. In the similar way we can calculate the power consumption & delay for other circuits also.

6. CONCLUSION

The design and simulation of hybrid CMOS-SET sequential circuits are presented here. The output voltage gain is estimated to be about 4.8 as determined from the slope of the transitional region. Since the SET and CMOS are placed in series, the hybridization is found to improve the gain of the inverter while the delay remains the same. Based on the hybrid CMOS-SET inverter, the circuits are designed and implemented. The performances of the proposed circuits are verified by simulation using T-Spice. The simulation results show that the performances of the circuits presented in this paper are satisfactory thereby establishing the feasibility of using the proposed hybrid circuits in future low power ultra-dense VLSI/ULSI circuits.

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