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ON THE TRANSCONDUCTANCE OF POLYSILICON THIN FILM TRANSISTORS

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In order to achieve both driver and display capability for a number of display devices, TFT has attracted attention, model calculations are therefore presented for the grain boundary barrier height, in a polysilicon TFT considering the charge neutrality between the intrinsic free carriers and the grain boundary trap states. The formation of the potential barrier at a grain boundary is considered due to the trapping of carriers at the localized grain boundary trap states. The trapped charges, influenced by the gate bias voltage and the trapping states density, in turn, have been taken to deplete free carriers near the grain boundary in a device such as polysilicon TFT. The present predictions reveal that the barrier height diversely depends on the gate source voltage (V_{GS}) of a TFT along with other crystal parameter. Finally to obtain the transconductance, the contributions of transverse and longitudinal grain boundary resistances are incorporated in the I-V characteristics of a TFT. For all values of grain size, the transconductance of the device is seen to increase initially with the gate voltage (V_{GS}) which finally appears to be saturated. The dependence of the transconductance on grain size and drain voltage has been thoroughly explored. Good agreement with experimental results is achieved.

Keywords: *POLYSILICON THIN FILM TRANSISTOR, GRAIN BOUNDARY, GRAIN BOUNDARY BARRIER HEIGHT, GRAIN BOUNDARY TRAP STATES, TRANSCONDUCTANCE.*

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1. INTRODUCTIONS

Because of recent applications of high speed pixel switching devices in active matrix liquid crystal displays (AMLCDs), polycrystalline silicon thin film transistors (TFT) are receiving significant attention. The miniaturization of poly-Si TFTs is being pursued in order to improve the aperture ratio and the high performance of the devices. Accordingly the device simulation of poly-Si TFT is playing an important role in predicting and analyzing the device characteristics. Poly-Si TFT is the most promising display for PMP (personal multimedia player) and CNS (car navigation system) because of higher resolution, lower power consumption smaller module size and higher module durability [1]. Polysilicon material consists of silicon crystallites (grains) separated by grain boundaries which are the regions with high density of trap states and cause the performance

degradation of the device. The grain boundary effects can be reduced either by passivating the dangling silicon bonds at the grain boundary states in the film or by enhancing the grain size thereby reducing the number of grain boundaries present with the active channel of the TFT device [2]. Many technologies have been applied to improve the performance of polysilicon TFT through grain enlargement and reduction of the grain boundary and the intra grain defect densities. In polysilicon films the defects are mainly located at grain boundaries. In the polycrystalline material the formation of a potential barrier at a grain boundary is due to fact that carriers are trapped at the localized grain boundary states and these trapped charges deplete free carries near the grain boundaries. In a polysilicon TFT the trapped charge is influenced by the gate bias and the trapping states at the grain boundaries. For circuit integration, it is essential to miniaturize the dimension of poly-Si TFT to meet the requirement and challenges of higher circuit density and higher driver current. The carrier trapping model is used, as the basis, for the explanation of conduction mechanism in the poly-Si films [3, 4]. In this model, a potential barrier is considered to be formed by trapping the free carriers at the trap states located at the grain boundaries. As a consequence, the boundary becomes negatively charged and a positively charged depletion region forms both the sides of the boundary. To satisfy charge neutrality this results in the bending of energy bands thus forming a potential barrier at the grain boundary.

2. THEORY

The material of polycrystalline silicon TFT is considered to be composed of a large number of identical crystallites with square cross section of size L_g. When such a TFT is appropriately biased to allow the carrier transport through the semiconductor material on the substrate, a potential barrier is created at each grain boundary. The formation of the potential barrier at the grain boundaries is due to the trapping of the carriers at the localized grain boundary states.

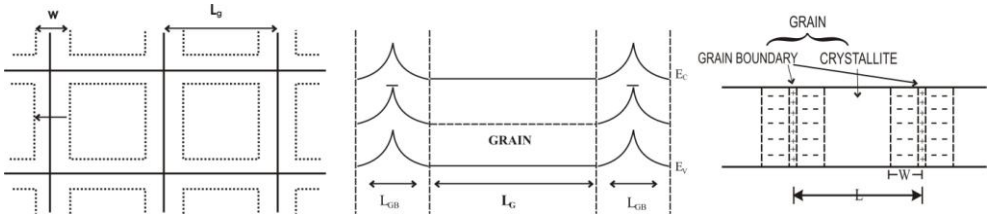

***Fig. 1** – Schematic diagram of polysilicon TFT (a), Energy band diagram of poly-crystalline silicon (b), one dimensional grain structure (c)*

The trapped charge carriers deplete the free carrier region near the grain boundaries and are influenced by the gate bias. In order to express the dependence of barrier height (ψ_B) on the gate voltage (V_{GS}), the following assumptions are made:

- The crystallites (bulk grain) are partially depleted.
- The traps are assumed to be initially neutral and become charged by trapping carriers.

- The induced free charge by the gate voltage is treated as an effective doping level.
- The traps are filled below the Fermi level.

In the case of high gate voltage when the grains are not fully depleted, the overall charge neutrality condition [5] $Q_{sc} + Q_t = 0$ is used to calculate the grain boundary barrier height (ψ_B). This means that the space charge density (Q_{sc}) in the depletion region of the grain is compensated by the trapped charge density (Q_t) at the grain boundary trap states. One dimensional Poisson's equation is

$$\frac{d^2\psi}{dx^2} = -\frac{1}{\varepsilon_s}\rho_s \tag{1}$$

The charge density per unit volume of semiconductor $\rho_s = -qN_A$, q is the charge of carrier, ε_s is the dielectric permittivity and N_A is the acceptor impurity concentration. Taking W to be the grain boundary depletion width, the surface potential (ψ_s) is obtained as

$$\psi_s = \frac{qN_A W^2}{2\varepsilon_s} \tag{2}$$

Employing the simple criterion that the charges in the inversion layer become significant when the electron concentration at the surface is equal to the substrate impurity concentration, the barrier height is easily obtained as

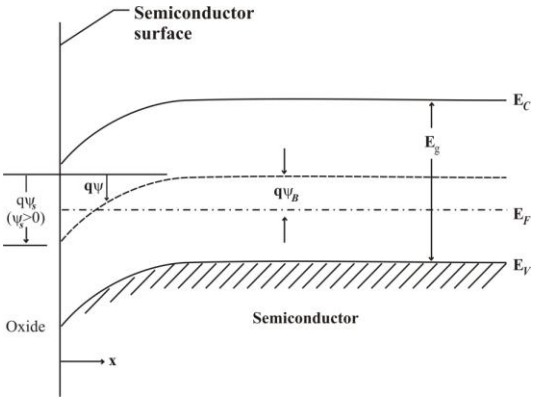

Fig. 2 *– Bending of a semiconductor bands at the onset of strong inversion. The surface potential twice the value of ψ_B in the neutral p material*

$$\psi_B = \frac{KT}{q}\ln\frac{N_A}{n_i} \tag{3}$$

The intrinsic carrier concentration is $n_i = N_A \exp(-q\psi_B/KT)$ where KT is the thermal energy.

Further since $\psi_s = 2\psi_B$ (Fig. 2) [6], one can write

$$\psi_S(inv) = \frac{2KT}{q} \ln \frac{N_A}{n_i} \tag{4}$$

The charge per unit area in the semiconductor is $Q_s = -qN_AW_M$, where W_M is the maximum width of the surface depletion region.

$$Q_s = -\sqrt{2q\varepsilon_s N_A(2\psi_B)} \tag{5}$$

The applied voltage must be larger enough to create this depletion charge and the surface potential. The threshold voltage required for strong inversion

$$V_T = \frac{qN_AW_M}{C_{OX}} + \psi_s(inv)$$

$$V_T = \frac{\sqrt{2q\varepsilon_s N_A(2\psi_B)}}{C_{OX}} + 2\psi_B \tag{6}$$

C_{OX} is the gate oxide capacitance per unit area.
Assuming the partially depleted grains the potential barrier height is given by [7]

$$\psi_B = \frac{qN_T^2}{8N\varepsilon_S}$$

where N_T is the trap state density and N is the gate induced electron concentration given by [8]

$$N = \frac{C_{OX}(V_G - V_T)}{qt_{Si}} \tag{7}$$

where t_{si} is the inversion layer thickness and V_G is the gate voltage.
The grain boundary potential barrier (ψ_B) is expressed as

$$\psi_B = \frac{q^2N_T^2t_{Si}}{8\varepsilon_S C_{OX}(V_G - V_T)} \tag{8}$$

The dependence of barrier height (ψ_B) on the grain size is predicted through the relationship [7, 9] $N_T = [35 + 2.55L_g^{-0.363}] \times 10^{10}$ per cm^2.
Now turning to the transport of carriers through the transverse and longitudinal, in an array of square grains the current prefers two conduction paths. Along the grain boundaries or through the grains and across grain boundaries. For such conduction paths total channel resistance R_{ch} is a combination of two resistances $R_{ch\perp}$ and $R_{ch\parallel}$. $R_{ch\perp}$ denotes the resistance of the interior grain and grain boundary regions and $R_{ch\parallel}$ denotes the resistance of the longitudinal grain boundaries. Because of the current flowing through the channel in two parallel paths (through transverse and longitudinal grain boundaries) the effective resistance becomes [10-13].

$$\frac{1}{R_{ch}} = \left(\frac{Z}{L}\right)\mu_{eff} Q_{inv} = \frac{1}{R_{ch\perp}} + \frac{1}{R_{ch\parallel}} \tag{9}$$

Z corresponds to channel width, L corresponds to channel length, μ_{eff} is the effective mobility and Q_{inv} is the charge density in inversion layer.
The values of $R_{ch\perp}$ and $R_{ch\parallel}$ are given as

$$R_{ch\perp} = \frac{nL_g}{m\ (L_g - w)\ \mu_g Q_{invg}} + \frac{nL_{gb}}{m\ (L_g - w)\ \mu_{gb} Q_{invgb}} \tag{10}$$

$$R_{ch\parallel} = \frac{L}{mL_{gb}\mu_{gb} Q_{invgb}} \tag{11}$$

Throughout the text the indices g and gb will be referred to the intra grain and grain boundary region respectively. m, n are the grains within the channel width and within the channel, w is the width of the depletion region at the grain boundary, L_g is the average intra grain length (grain size), L_{gb} is the average grain boundary length, μ_g is the mobility for a carrier passing through grain interiors and μ_{gb} is the mobility for a carrier passing along grain boundaries.

Now substituting the values of $R_{ch\perp}$ and $R_{ch\parallel}$ the effective mobility [14] μ_{eff} is expressed as

$$\mu_{eff} = \frac{\mu_g\ (L_g - w)}{L_g + (L_{gb}/\mu_{gb})[\mu_g \exp(q\psi_B/KT)]} + \frac{L_{gb}}{L_g}\mu_{gb} \tag{12}$$

Now putting the value of μ_{eff} in standard drain current equation we get

$$I_D = \frac{Z}{L} C_{ox}(V_G - V_T)V_D \frac{\mu_g\ (L_g - w)}{L_g + (L_{gb}/\mu_{gb})[\mu_g \exp(q\psi_B/KT)]} + \frac{L_{gb}}{L_g}\ \mu_{gb}$$

This is the final equation to interperate the dependence of drain current (I_D) on the gate voltage (V_G). Here V_D is the drain voltage. The transconductance (g_m) is then obtained by the ratio of drain current to the gate voltage as

$$g_m = \frac{Z}{L} C_{ox}\left(1 - \frac{V_T}{V_G}\right)V_D \frac{\mu_g\ (L_g - w)}{L_g + (L_{gb}/\mu_{gb})[\mu_g \exp(q\psi_B/KT)]} + \frac{L_{gb}\mu_{gb}}{L_g V_G}$$

3. RESULT AND DISCUSSION

The standard values of parameters taken for the present computations are t_{Si} = 4 nm, C_{ox} = 354 μF and V_T = 1 V. The increase of trap state density (N_T), increases the potential barrier height (ψ_B) at the grain boundary over the entire range of gate voltage. The effect is found to be more pronounced for lower values of grain source voltage (V_{GS}) while the values of barrier height (ψ_B) is observed to saturate for higher V_{GS}. The computed values have been compared with the experimental results of Argyrios T. Hatzo-

poulos and C.A. Dimitriadis [15]. A reasonably good agreement is predicted. The computed variations of grain boundary potential barrier height (ψ_B) as a function of the gate source voltage (V_{GS}) for different values of trapping states density (N_T) and grain size (L_g) for a polycrystalline silicon thin film transistor have been presented in Fig. 3a and b. It is observed that the barrier height diversely depends on calculating parameters such as the density of trap states (N_T) and the grain size (L_g). In the region of low gate voltage, the barrier height (ψ_B) slightly increases with increase in gate source voltage reaches a maximum and thereafter decreases and finally approaches almost saturation for all grain sizes.

The present predictions show that the current transport mechanism is controlled by the gate voltage. The grain boundaries are seen to influence the effective carrier mobility and hence the drain current (I_D). At lower values of gate voltage, the longitudinal grain boundaries do obstruct the

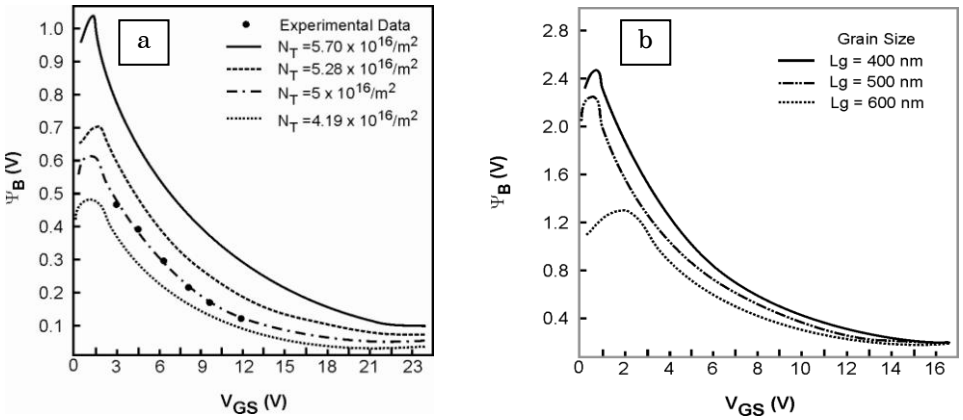

Fig. 3 *– Variation of GB barrier height with gate voltage, for different values of trap state density (a). Variation of GB barrier height with gate voltage, for different values of grain size with gate source voltage (b)*

current mechanism while at higher values of the same, the transverse grain boundaries has larger impact to the current flow. It may be due to the reduction of the potential barrier at the grain boundaries. As the gate voltage increases the longitudinal grain boundaries are observed to have no effect on the transfer characteristics of the TFT because the carriers are expected to follow the path of low resistance offered by the bulk grain and the transverse grain boundaries with reduced barrier height [15].

Quantitative comparisons of measured current with the experimental results establish a good evidence for the validation of our model. The exponential growth of the drain current (I_D) as shown in Fig. 4a and b is observed to be in good agreement with the experimental observations [16-20]. The saturation in drain current may be explained as due to the saturation of grain boundary trap states and there being no change in barrier height when the gate voltage is increased [16]. The transconductance of

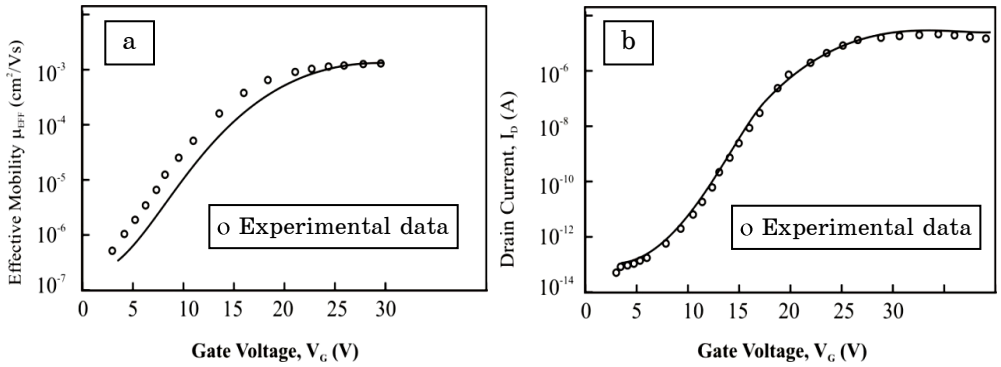

Fig. 4 *– Effective carrier mobility of polysilicon TFT against gate bias voltage (V_g) for gate width $Z = 10$ μm and gate length $L = 10$ μm (a). Transfer characteristics of a polysilicon TFT for gate width $Z = 10$ μm and gate length $L = 10$ μm at drain voltage $V_D = 0.1$ V (b)*

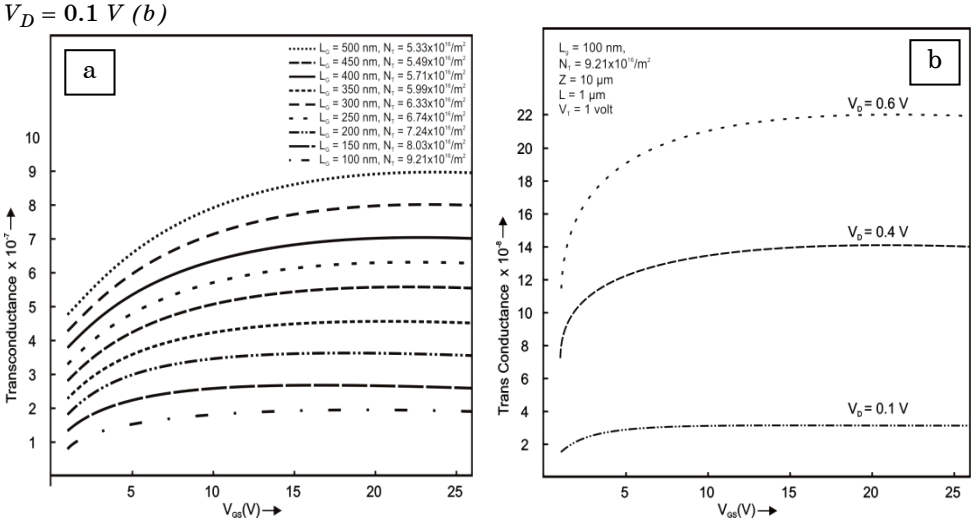

Fig. 5 *– Variation of transconductance with gate voltage for different values of gain sizes (L_g) (a). Variation of transconductance with gate voltage for different drain voltage (V_D) (b)*

polycrystalline silicon TFT is seen to be influenced by the grain size. This may be because of the change in the number of grain boundaries over a given length of channel and hence the number of potential barriers obstructting the carrier flow. For all values of grain size, the transconductance of the device initially increases with the gate-source voltage (V_{GS}) and finally appears to be saturated as depicted in Fig. 5a. The dependence of the transconductance on drain voltage (V_D) is shown in Fig. 5b. It may thus be concluded that to have large value of transconductance one should optimize the large grain polysilicon TFT technology. It is apparent from the results that a large grain size leads to better device performance. This results in high value of transconductance which is good for device performance.

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