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A STRATEGIC REVIEW OF REDUCTION OF DISLOCATION DENSITY AT THE HETEROGENIOUS JUNCTION OF GAN EPILAYER ON FOREIGN SUBSTRATE

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Now-a-days for long range microwave communication, especially for space applications, devices capable to operate at a high power and high frequency are desired. Compound Semiconductor (CS), mainly Gallium Nitride (GaN) based heterostructure electronic devices are the only available solutions till now to fulfil these criteria. However, looking from a cost and manufacturing perspective, GaN substrate has considerable drawbacks like non-availability, expense as well as compulsion to use older technologies for device designing as the wafer diameter is small. A potential solution for performance/cost dilemma is to grow high quality GaN as active layer on a well matured substrate by metamorphic technique. Metamorphic buffer technology allows the device designer an additional degree of freedom to optimize the transistor at high frequency for high gain and power applications. But this metamorphic buffer technology has some drawbacks, too. The main limiting factor for this technology is the propensity to develop dislocation at the heterojunction due to lattice mismatch between the grown layer and the substrate. A good quality metamorphic buffer can only be achieved by reduction of dislocation density at the heterojunction. This paper reviews the progress being made towards reduction of dislocation density of GaN based devices grown on Silicon Carbide (SiC), Sapphire (Al_2O_3) and Si substrate, respectively, in terms of material parameters and growth issues.

Keywords: *GALLIUM NITRIDE, SILICON CARBIDE, SAPPHIRE, DISLOCATION DENSITY, EPITAXIAL GROWTH, CRYSTAL STRUCTURE.*

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1. INTRODUCTION

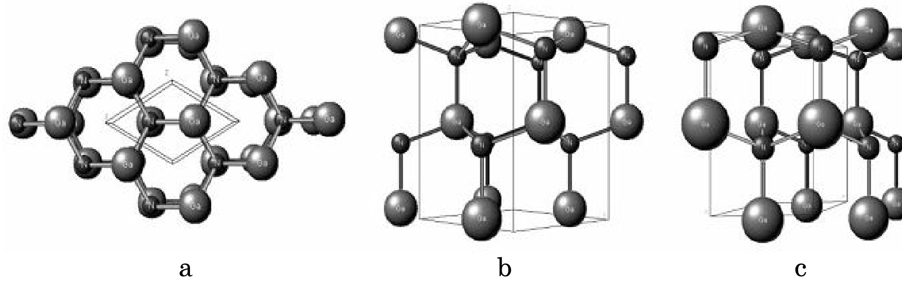
To improve carrier transport in GaN films as well as to improve the efficiency and to reduce the cost of GaN-made optoelectronic devices, reduction of threading dislocation density is the most important [1, 2]. The main reason of dislocation density is lattice mismatch between the substrate and the GaN layer. Moreover, material's crystal structure, surface finishes, composition, reactivity, chemical, thermal and electrical properties are also considered for choosing a substrate-material for GaN growth (since the substrate properties are ultimately responsible for the efficiency of GaN-made devices) [3]. Some of the above mentioned substrate properties are considered to reduce the dislocation density of GaN.

Dislocation free GaN devices can be realized by growing the same on GaN substrate, as there will be no lattice mismatching. Defect-free bulk GaN can be grown at very high temperature (1400 - 1600 °C) and pressure (15 - 20 kbar) on GaN substrate, but it took very large growth time [4]. Moreover, bulk GaN substrate is not commercially available. The resultant of this fact is that the researchers are tending towards the growth of GaN film on foreign (e.g., Si, SiC Al_2O_3 (sapphire) etc.) substrates, called heteroepitaxial growth of GaN film. Heteroepitaxial growth is highly dependent on the properties of the substrates – both the inherent properties (lattice constant, thermal expansion co-efficient) and process-induced properties (e.g., surface roughness, step height, etc.) [3].

2. PROPERTIES OF GAN

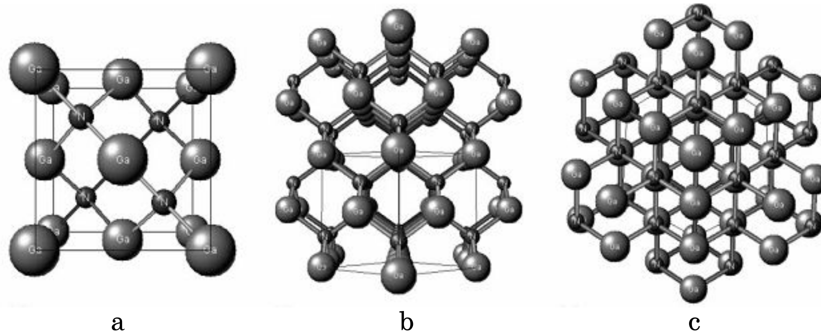
2.1 Structure of GaN

In stable condition Gallium Nitride has Wurtzite structure [3]. It has alternating biatomic close-packed (0001) planes of Ga and N pairs stacked in an ABABAB sequence. Fig. 1 shows the [0001], $[11\bar{2}0]$, and $[10\bar{1}0]$ directions, among which [0001] is closed-packed. The most favorable orientation for growth of smooth GaN film is [0001]. There is another structure of GaN, called the Zincblende structure. This structure of GaN (shown in Fig. 2), having the (111) closed-packed planes can be stabilized in the epitaxy.



a b c

Fig. 1 – *Perspective views of wurtzite GaN along various directions:* [0001] *(a);* $[11\bar{2}0]$ *(b);* $[10\bar{1}0]$ *(c) (Ref. [5])*



a b c

Fig. 2 – *Perspective views of Zincblende GaN along various direction:* [1000] *(1 × 1 × 1 unit) (a);* [110] *(2 × 2 × 2 units) (b);* [111] *(2 × 2 × 2 units) (c) [5]*

2.1 Dislocation Densities of GaN

Generally for the heteroepitaxial growth of GaN, two types of dislocations are found: (i) Misfit Dislocation (MD) and Threading Dislocation (TD). Generally, there are three kinds of TDs [5-7]; a pure-edge dislocation with Burgers vector $\vec{b} = 1/3[11\bar{2}0]$, a screw dislocation with $\vec{b} = [0001]$, and a mixed dislocation with $\vec{b} = 1/3[11\bar{2}\bar{3}]$. The structures of the Burgers vectors in GaN film is shown in Fig. 3 [8]. According to Dadgar et al. [9], pure-edge dislocation lying in the [0001] direction, is predominant, in GaN.

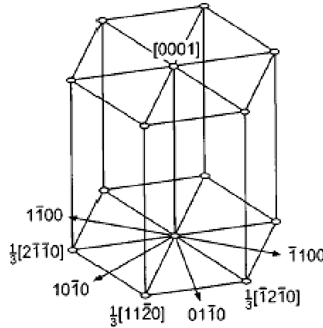


***Fig. 3** – Directions and Burgers vector notations for the hexagonal structure of GaN (Ref. [8])*

Table 1 shows the mismatch between the GaN layer with Si, SiC and Sapphire substrate. The MD and TD for heteroepitaxy of GaN layer grown on sapphire and SiC substrate is found to be of the order of 10^8 - 10^{10} cm^{-2} while that for homoepitaxy on Si substrate is 10^2 - 10^4 cm^{-2} [10]. Other defects like stacking faults, inversion domain boundaries are also obtained during heteroepitaxy [11]. These also affect the GaN-made semiconductor device quality, by reducing charge carrier mobility, minority carrier lifetime, and thermal conductivity.

***Table 1** – Lattice constants and lattice mismatches of GaN with various substrates*

Material	Structure	Lattice Constants			Lattice Mismatch (In %)
		a	*b*	*c*	
W-GaN	Wurtzite	0.31885	-	0.5185	NA
SiC	4H-W	0.3073	-	1.0053	~ 3.1 %
Si	Diamond	0.5431	-		~ 16.9 %
Sapphire (Al_2O_3)	Rhombohedral, Hexagonal	0.4765	-	1.2982	~ 15 %

3. GAN FILM ON SAPPHIRE SUBSTRATE

3.1 Choice of plane of sapphire substrate for growth of GaN

Due to the large lattice-mismatch between sapphire and GaN, many threading dislocations (~ 10^{10} cm^{-2}) are found along the c-plane of the interface of the epitaxial layer of GaN grown on sapphire substrate.

Coalescence of the nucleation islands are generated by the thermal treatment of buffer layers before the growth of high temperature GaN over-layers. It creates low angle grain boundary, resulting in threading dislocations along the c-axis. There are other planes of sapphire, which could be chosen for growth of GaN. Specially, a-plane of sapphire can be easily cleaved along r-plane as well as oriented along [0001] direction, resulting in lower lattice mismatch (2 % only) [3]. But c-plane is extremely important for growing GaN. The Al-O bond in the sapphire surface is anti-parallel to the N-III bonds in the III-N films. As a result of that AlN nucleation layer is formed by the growth technique and it is asymmetrically strained for *a*-plane of sapphire [12]. The *r*-plane and m-plane of sapphire are very rough, since inverted twins are formed there creating very high dislocation density [3]. Thus, analyzing the PL and HRXRD spectra, it is concluded that c-plane of sapphire is the best for growing GaN.

3.2 Disadvantages of sapphire substrate

Large lattice mismatch between sapphire and GaN gives a complete relaxation (no strain) for the GaN film during growth, though it increases dislocation density. Another important aspect is availability of sapphire substrate, making the process is very cheap. Moreover, sapphire is electrically insulator. Hence, the available area for device operation decreases, but it creates a low leakage of current [3].

3.3 Advantages of sapphire substrate

Lattice mismatch of sapphire with GaN is very high (~ 15%) [3]. It creates a very large dislocation density (1010 cm^{-2}) [3], which creates (a) Low minority carrier lifetime, (b) Low charge carrier mobility, (c) Low thermal conductivity. All of these aspects reduce the efficiency of the GaN-made device. Sapphire has higher thermal expansion co-efficient than GaN, which creates biaxial stress, generating crack [13]. Cleavage plane of epitaxial GaN is not parallel to those of sapphire, for which facet formation is difficult [3].

3.4 Reduction of threading dislocation density of GaN on sapphire substrate

Growth of GaN on planar substrate of sapphire, SiC or Si (111) substrate gives high TD (~ 10^{10} cm^{-2}) density. Longevity of p-n junction devices, GaN-made sophisticated devices like LEDs, decreases and leakage current increases to a very high value. This can be solved only when TD density decreases below 10^6 cm^{-2}.

To minimize the threading dislocation density, nucleation layer growth on c-plane sapphire substrate for different conditions were studied by S. Keller et al. [1]. They showed that exposure of GaN film to NH_3 before deposition of GaN layer by MOCVD reduces dislocation density. The dislocation density reduces from 2×10^{10} to 4×10^8 cm^{-2} for shorter NH_3 preflow times and for symmetric plane [1].

Kurai et al. has made high-thickness-low-diameter epitaxial GaN layer on sapphire substrate using sublimation method [15]. Now let us consider the case of growth of GaN film selectively, using HVPE (Hydride Vapor Phase Epitaxy). Several-hundred-micron-thick high quality GaN with ZnO buffer layer was selectively grown by HVPE using GaCl and NH_3 [16-18] at high

growth rate [19], but cracks occur in the layer [20]. To overcome this problem, using MOVPE (Metalorganic vapor phase epitaxy), a thin layer (thickness 1 - 1.5 μm) of GaN was grown on the sapphire substrate first, then very thick layer (up to 4 μm) of crack-free GaN (growth temperature 1000 °C) was grown [21]. The schematic diagram of the structure is shown in Fig. 4.

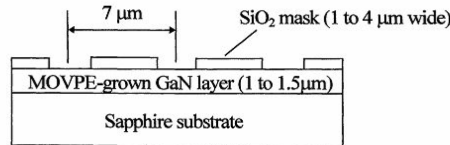


Fig. 4 *– Schematic diagram of the substrate structure (Ref. [21])*

Moreover, the coalescence of the selectively grown structure in this process abolishes the gap between the facets and finally makes a [0001] mirror-like flat surface. The defect density was measured by TEM, which gave a very low value (~ 6×10^7 cm^{-2}). Dislocations provide very low resistance against strain due to thermal expansion co-efficient difference, making a harder GaN film.

The same technique was applied by Sakai et al. to reduce the dislocation density. Selective growth of GaN layer by HVPE, in which growth on SiO_2-striped-patterned GaN layers was made by MOVPE on sapphire [0001] substrates (Fig. 5) [8].

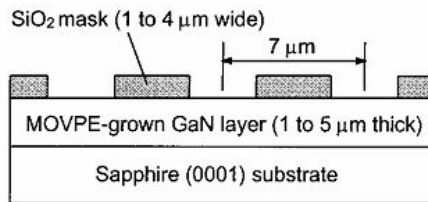


Fig. 5 *– Schematic diagram of the substrate structure used for HVPE growth (Ref. [8])*

When TEM was performed for both the layers (i.e., MOVPE grown and HVPE grown), it was observed that for MOVPE grown layer, most of the threading dislocations were pure-edge threading dislocations, some are of mixed character and very few are screw-type [5-7], which were vertically aligned. Almost all the dislocations in MOVPE layer propagated into HVPE layer laterally during the selective growth of the HVPE layer. The dislocations in HVPE layer parallel to the interface formed an angled configuration, generating no defect in the interface. These angled dislocations piled up with the [0001] direction. TEM reveals that angled dislocation depends on their Burger vectors of either $1/3[11\overline{2}\overline{0}]$ or $1/3[11\overline{2}\overline{3}]$. Since the pure-edge threading dislocations changed into screw dislocation after lateral propagation from MOVPE layer to HVPE layer, it was concluded that most of the dislocation cannot thread the HVPE layer [8]. The lateral propagation occurs mainly around the SiO_2 mask for non-pure-edge dislocations (which are very few in MOVPE layer). Moreover the lateral segments do not lie on the slip planes. This kind of morphology reduces the threading dislocation in the thicker HVPE layer.

A great reduction of dislocation density is obtained by Lateral Overgrowth from Trenches (LOFT) in which trenches are formed by etching the GaN layer (with threading dislocation 8×10^9 cm^{-2}) grown on sapphire substrate where the GaN layer is regrown (2 - 6 μm with reduced threading dislocation 6×10^7 cm^{-2}) laterally [22]. The residual dislocations are mainly due to the merging between two lateral growths or extended from the trench sidewalls. Schematic diagram of the structure is shown in Fig 6.

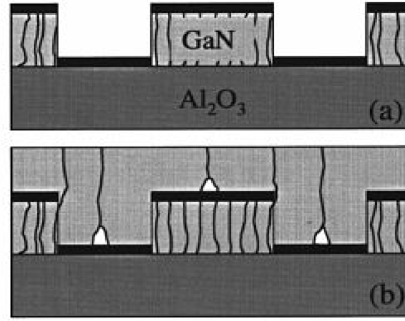


Fig. 6 *– The structure of GaN film before and after regrowth are shown schematically in (a) and (b) respectively. The TD and the voids possibly formed in GaN thin films are also shown schematically. (Ref. [22])*

A new method of applying NH_3 and SiH_4 gases simultaneously at low temperature with a certain time before the growth of a low-temperature (450 °C) GaN buffer layer followed by growth of undoped GaN layer (growth temperature 1075 °C and thickness 2μm) by MOCVD decreases the threading dislocation from 7×10^8 cm^{-2} to almost invisible under TEM, observed by Wang et al. [23]. Introduction of SiH_4 and NH_3 creates nano-sized holes, which increases the lateral growth to the next layer creating reduction of TDs. In practice, this can also be done by deposition of SiN layer (2 nm, deposition time 125 s) on sapphire, which covers the substrate up to 90 % to make 66 % of the surface area almost dislocation-free [23].

In undoped GaN increasing staking faults plays a crucial role in the reduction of dislocation density [24]. GaN buffer layers of various thicknesses on sapphire substrate were operated with various (from 10 - 80 μmole/min) TMGa (Trimethyle Gallium) flow-rates (f_{TMGa}). H. Cho et al. showed that the maximum TMGa flow rate (80 μmole/min) gives maximum intense PL peak related to increase in stacking faults as well as decrease in dislocations (1×10^8 cm^{-2}), as threading dislocations interact with stacking faults and bend towards $[1\bar{1}01]$ planes and finally disappears [25].

Many techniques have been followed (i.e., LEO [26, 27], pendeoepitaxy [28], LOFT [22] to lower TD density below 10^6 cm^{-2}. All are time-consuming, complex, multi-step processes which need *ex-situ* lithography. A simple process for it is Cantilever Epitaxy (CE) in which pre-patterned (with narrow lines) sapphire substrate is used to provide reduced-dimension mesa regions for nucleation. Then etched trenches are employed for suspended lateral growth of GaN/AlGaN. The substrate is etched to a depth that allows coalescence of laterally growing GaN nucleation on the mesa surfaces before

vertical growth fills the etched trench. Low dislocation density is obtained in the cantilever region, almost 1 μm less than the mesa region [29]. The SEM micrograph and CL image are shown in Fig. 8 and 9 respectively.

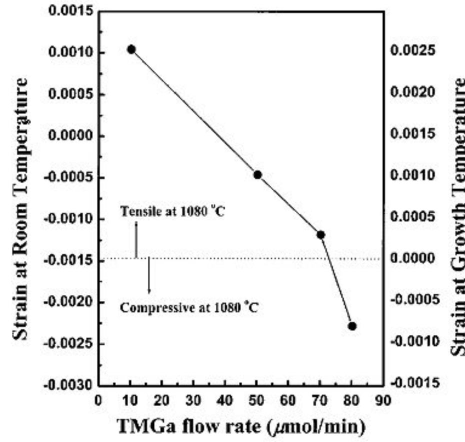


***Fig. 7** – Relationship between the f_{TMGa} of buffer layers and the strain of GaN overlayers at room temperature after cool down and growth temperature (*1080 °C*) (Ref. [25])*

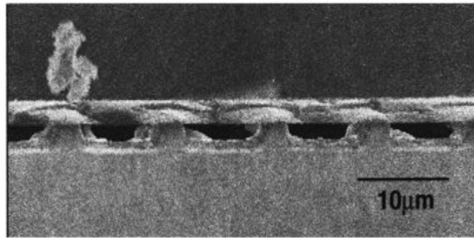


***Fig. 8** – Cross-section SEM micrograph of cantilever epitaxy (Ref. [29])*

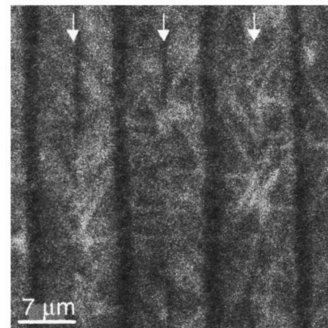


***Fig. 9** – CL image of CE reducing partial absence of TDs (dark regions) along coalescence fronts (arrows). (Ref. [29])*

In OMVPE process, a single thin interlayer of low temperature (700 - 900 °C for 15 minutes) can be introduced after initial growth on sapphire substrate with low-temperature buffer layer and before final growth (both at high temperature i.e., 1000 °C) to reduce the threading dislocation density (below 8×10^7 cm^{-2}). The process is called single intermediate temperature interlayer (IT-IL), schematically shown in Fig. 10 [30]. After the sudden drop of the temperature, 3D growth mode is generated instead of 2D growth mode (generated in the initial layer) and after increase in temperature again 2D growth mode is generated again. Large amount of threading dislocations present into initial layer are bent into the interlayer, become confined as

these cannot propagate in the 2D mode from 3D and are not exposed in the final surface [30].

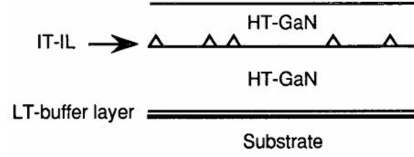


Fig 10 *– Schematic diagram of IT-IL process. Ref. [30]*

Another important technique to grow GaN layer with lower dislocation density (10^7 cm^{-2}) is by growth interruption modulation in HVPE method with modulating the growth process by switching on/off the GaN layer. In this process, thick multilayered structure of GaN is grown on c-Al_2O_3 (i.e., c-plane of sapphire) substrate in which dislocation reduces by and by from the lowermost layer (10^{10} cm^{-2}) towards the uppermost layer (10^7 cm^{-2}). During growth, continuous flow of NH_3 and periodic flow of HCl (shown in figure 11) are applied to modulate the growth [31].

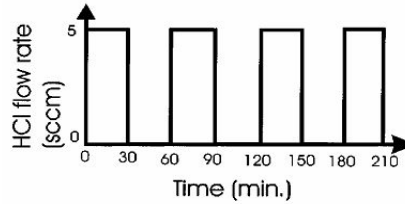


Fig. 11 *– Time chart of HCl flow in GIM with deposition of* 30 *min and HCl interruption of* 30 *min for each run. Ref. [31]*

K. Pakula et al. [32] showed that lateral overgrowth of GaN on sapphire (using MOCVD) with a growth interruption followed by annealing with SiH_4 decreases the TD density up to 5×10^7 cm^{-2}. This is due to pyramidal pits (approx. 40 nm deep) of the GaN surface, which are selectively etched by SiH_4 (Fig. 12) resulting in a radical change in direction of propagation of dislocation (being horizontal from the direction parallel to the c-plane). In contrast with other epitaxial methods, in this method large area of low dislocation density can be formed without formation of sub-grains with significant tilt [33, 34].

Shen et al. [35] proposed a method of reduction of both tilting and twisting of grain features causing high TD density of GaN grown on vicinal sapphire (0001) surface by RF-MBE making the vicinal angle larger than 0.50. Use of SiN, Si_xN_y, $Si_xAl_{1-x}N$, Si irradiation etc need complicated growth processes [23, 36, 37]. Fig. 13 shows the XRD rocking curves of the GaN surface. For better morphological GaN surface on vicinal substrate, MBE has higher advantages upon MOCVD [35] by reducing the density of TD to ~ 10^7 cm^{-2}.

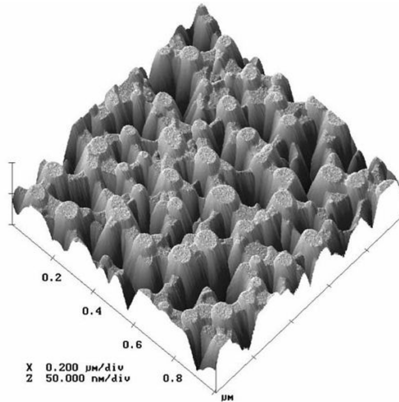


Fig. 12 *– AFM image of GaN surface after* 30 *s in situ treatment by silane at* 1100 *°C (Ref. [32])*

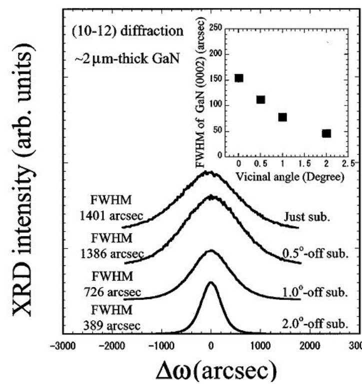


Fig. 13 *– Asymmetric (*10-12*) rocking curve of GaN films grown on vicinal sapphire* [0001] *substrate with various vicinal angles. The inset is the dependence of the FWHM of the symmetric* [0002] *diffraction peaks on the vicinal angles. Ref. [35]*

Use of in-situ thin discontinuous SiNx interlayer (deposited at 860 °C) coverage for GaN growth on c-plane sapphire (0001) substrate by OMVPE can reduce TD density up to a factor of 50 to 9×10^{7} cm^{-2} mainly due to construction of facetted islands on the GaN surface as well as generation of half-loops between bent-over TDs during the lateral overgrowth [38]. Dependence of TD density with the interlayer thickness is shown in Fig. 14. Here c-plane sapphire with 0.25 % miscut towards the a-axis is used as substrate. Same kind of growth by MOCVD shows TD density to be 4.4×10^{7} (screw-type) and 1.7×10^{7}(edge-type) [39].

Chakraborty et al. [40] showed that SiN_x *in-situ* nanomask is also important for TD density reduction in non-polar a-plane GaN films on r-plane sapphire by MOCVD. Increase in SiN_x layer leads to on-axis and off-axis FWHM of HRXRD, rms surface roughness and submicron pit density as well as stacking fault density decrease from 8.0×10^{5} to 3.0×10^{5} cm^{-2} which finally decreased defects (both SFs and TDs) up to 9×10^{9}cm^{-2}. Increase in deposition time leads to decrease in TDs.

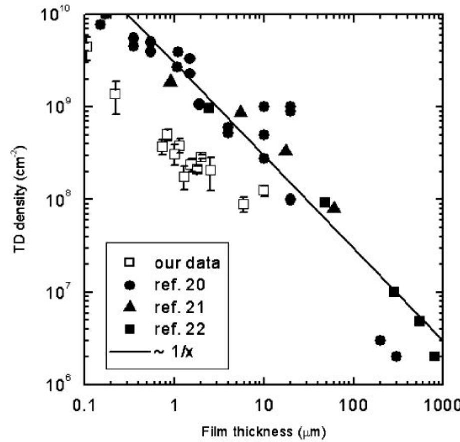


Fig. 14 *– TD density vs. GaN layer thickness of SiN_x compared with HVPE-grown sample from Mathis et al. (Ref. [20]), Morkoc (Ref. [21]) and Lee et al. (Ref. [22]). The solid line represents the trend of the TD reduction with thickness of the HVPE-grown layers. (Ref. [39])*

C.J. Tun et al. showed that multiple Mg_xN_y/GaN buffer layers, which can form a textured surface, were used for growth of GaN on sapphire using MOCVD at 530 °C. Reduction of dislocation (associated with the grain boundary) was obtained. Propagation of TD after coalescence occurs here, lowering its density on the exposed surface, as shown in Fig. 15 [41].

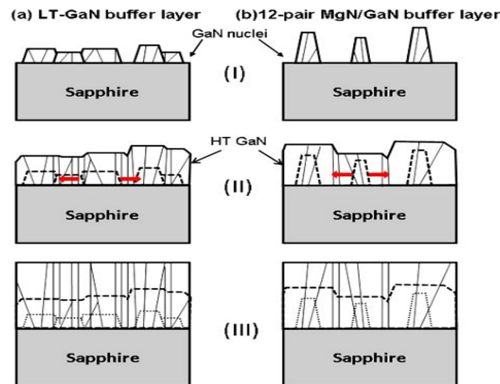


Fig. 15 *– (color online) schematic representations of the morphological evolution and associated TDs generation and propagation in GaN epitaxial layers grown on (a) LT-GaN, (b) 12 pairs of Mg_xN_y buffer layers on sapphire: (I) heat-treated buffer layers on sapphire, (II) coalescence of HT-GaN with accompanying TDs generation, (III) propagation of TDs after coalescence. (Ref. [41])*

M.A. Moram et al. [42] showed that a 500 nm deposition of lattice-matched, dislocation-blocking scandium nitride interlayer introduction using a single step without lithography for growth of GaN on sapphire template can reduce TD density reduction up to ~ 10^7cm^{-2} for coalesced films and ~10^6 cm^{-2} for partially-coalesced film. Reduction of TD density depends on the thickness of scandium interlayer, as shown in Fig. 16. The reasons of TD

density reduction are – (1) limited chemical stability under MOVPE growth condition, (2) void formation and bending of dislocation during annealing, creating no threading of dislocations in exposed template area, (3) matching of interatomic spacing between GaN and ScN mask layer, resulting in nucleation of overgrown GaN islands without forming dislocation.

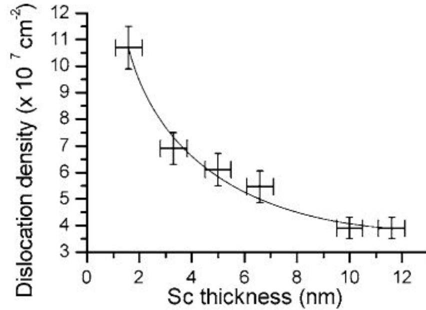


Fig. 16 *– Plot of TD density of coalesced GaN layer vs. Scandium thickness (Ref. [42]*

Q. Li et al. used self-assembled close-packed monolayer of silica microspheres as selective growth mask for growth of GaN on sapphire epilayer. Silica microspheres are formed during regrowth of GaN layer, which terminated the propagation of dislocation, causing a huge reduction of dislocation by bending and blocking (~ 4×10^7 cm^{-2}) [43]. Fig. 17 shows the dependence of TD density with the silica microsphere diameter.

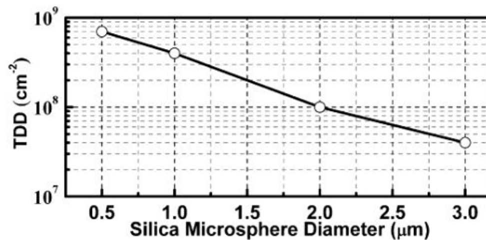


Fig. 17 *– TDD of GaN layer as a function of silica sphere diameter (Ref. [43])*

Dislocation density of three-fourth of the exposed area of GaN, grown on sapphire substrate was reduced extremely (~ 10^2 cm^{-2}) during the two-step method of LPE growth using Na-flux [2]. The thickness of the GaN crystal was made intentionally very high (2 mm) here to show that dislocation reduces with increase in growth thickness. The schematic diagram of the mechanism of TD reduction in this process is given in Fig. 18.

4. GAN FILM ON SIC SUBSTRATE

Relatively high quality of GaN epitaxial device on Sapphire substrate is a bit difficult to achieve because of their large lattice mismatch (~ 15 %). On the other hand better lattice mismatch between GaN and Silicon Carbide as a substrate has gained popularity in recent years for both MOCVD/MOVPE and MBE growth technology.

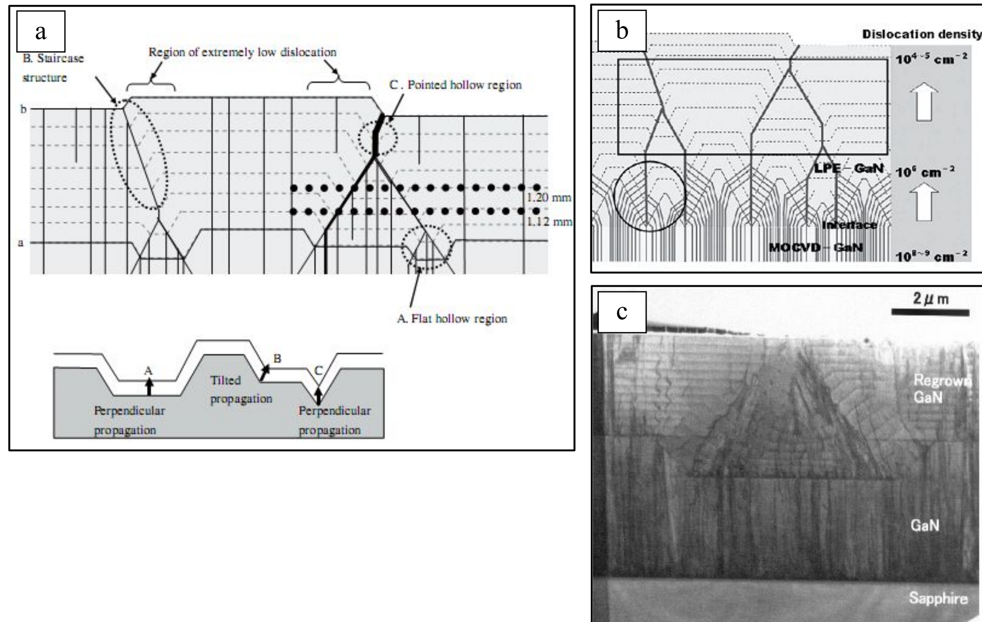


Fig. 18 *– The dislocation reduction process after the middle stage of the LPE growth. Dislocations existing at positions A and C propagate along the c-axis, while those at the staircase structures (positions B) propagate along the development of the stair edge, resulting in oblique propagation from the c-axis. By following the bold line in the figure, we can summarize the propagation of the dislocations as follows: Type A dislocations are aggregated to Type B ones as the LPE growth progresses, followed by their aggregation to Type C and eventually back to Type B. Although the transformation of the dislocations from Type B to Type C and subsequently back from Type C to Type B occurred naturally, transformations into Type A were not allowed after extinction of the concave portions. Therefore, the dislocation types transformed in the order A, B, C, B, C, B ..., reducing the number of dislocations. Ultimately, almost all dislocations were categorized as Type B (a). The entire process of dislocation reduction, including the Initial growth stage, is summarized (Ref. [2]) (b). TEM shows very low DD in the grooved side-walls [59] (c)*

The process which creates lowest DD is ELOG (epitaxial lateral overgrowth). Here, regrowth technique is applied on the periodically grooved surface with controlled V/III ratio. Groove is completely buried in the thinner exposed layer, for which DD is unexposed in TEM. It creates very low DD (6×10^{6} cm^{-2}) in the regrown GaN surface. Fig. 18c shows the TEM of this phenomenon [59].

4.1 Comparison of SiC substrate over sapphire for growth of GaN layer

Table 2 – *Advantages of SiC in comparison with sapphire*

Parameters	**SiC**	**Sapphire**
Lattice constant mismatch	3.1 % along [0001] direction, but contribution of Screw Dislocation creates large overall DD	Very large (approx. 15 %), creating high DD.
Thermal conductivity[11]	3.8 W/cm K	0.25 W/cm K (<< SiC)
Electrical conductivity	Relatively higher value	Insulator
Orientation of crystal planes with respect to GaN	Parallel (facet formation easier by cleaving)	Not parallel (facet formation is not easy)
Polarity	GaN film polarity is easier on SiC substrate, as it has both C and Si polarity.	GaN film polarity is problematic on sapphire, as mentioned before in this review.
Surface roughness	Higher than sapphire (1 nm rms), disadvantageous with respect to sapphire.	Lower than SiC (0.1 nm rms), better for GaN growth.
Thermal expansion coefficient	Less than GaN, generating bi-axial tension.	Higher than GaN, generating bi-axial stress.

4.2 Choice of SiC plane as substrate

SiC has 250 polytypes, among which only two (4H-SiC and 6H-SiC) have same space group {p6$_3$mc (no. 186)} as Wurtzite GaN. 6H-SiC is more commercially available than 4H-SiC. Thus, 6H-SiC is the mostly used polytypes of GaN growth on SiC substrate [3].

4.3 Reduction of threading dislocation density of GaN film on SiC substrate

The main problematic TD in SiC substrate is hollow-core screw dislocations (called micropipes or nanopipes), which have Burgers vector ($\vec{b}$) twice and three times of c-lattice constant of 6H-SiC and 4H-SiC respectively. These holes are oriented along the c-axis; as a result, these can propagate throughout the crystal [45]. Here are some techniques of reduction of dislocation density of GaN layer grown on SiC substrate.

The lateral overgrowth via Organometalic Vapor Phase epitaxy (OMVPE) of GaN stripes patterned in a SiO_2 mask deposited on GaN-film/AlN-buffer/6H-SiC (0001)-substrate at 1000 - 1100 °C and at 45 Torr, oriented along $[11\bar{2}0]$ and $[1\bar{1}00]$ is required here. Fig. 19 shows the schematic diagram. A very low dislocation density of 10^6 cm^{-2} GaN layer is obtained due to coalescence of the GaN homoepitaxial stripes on SiO_2 mask. The coalesced layers for this case had a surface roughness of rms value, i.e., 0.25 nm [46].

The low-edge grain boundary during growth of GaN on SiC substrate is the main source of dislocation for this heterostructure. Two possible sources of dislocation are (i) dislocation half-loop and (ii) island edges. Accumulation of misfit strains after a certain thickness creates misfit, which ultimately generates TDs. The GaN layer (1.5 μm)/AlN buffer/SiC (typically tilted 3 to 4 degrees off towards the direction $[11\overline{20})$ substrate grown by MOCVD using

ultra-thin AlN buffer layer of 1.5 nm (< the critical value for misfit dislocation) and a smooth AlN surface reduces the threading dislocation very much (2-3 order less than the value of dislocation for the thicker buffer). Island edges can be reduced by smooth surface. Hence TD density reduction is obtained [5].

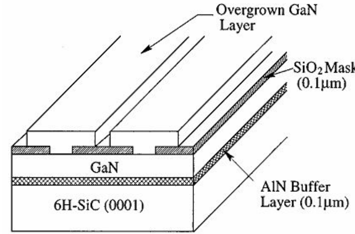


Fig. 19 *– Schematic diagram showing lateral epitaxial overgrowth of GaN layer on SiO2 mask from GaN deposited within striped window openings on GaN/AlN/6H–SiC substrates (Ref. [46])*

The defects in the GaN grown within the SiO_2 windows were predominantly threading dislocations of mixed character with Burgers vector $b = 1/3[11\bar{2}3]$ and edge dislocations with $b = 1/3[11\bar{2}0]$. Hexagonal pyramids of GaN are grown under the SiO_2 mask during lateral epitaxial overgrowth (LEO) of GaN on patterned GaN/AlN/6H-SiC substrate (Fig. 20a). Fig. 20b shows the schematic diagram of LEO. Stresses due to the mismatches in the thermal expansion coefficients during LEO-GaN growth, existing initially at the underlying AlN/6H-SiC and GaN/AlN interfaces, propagate through the selectively grown GaN and are accommodated in these regions both via the continued propagation of numerous TDs and short dislocation segments and the bending of the stripes or pyramids. As a result, LEO-GaN has lower dislocation density (approximately 4 order less) than the vertical-growth region [47, 48].

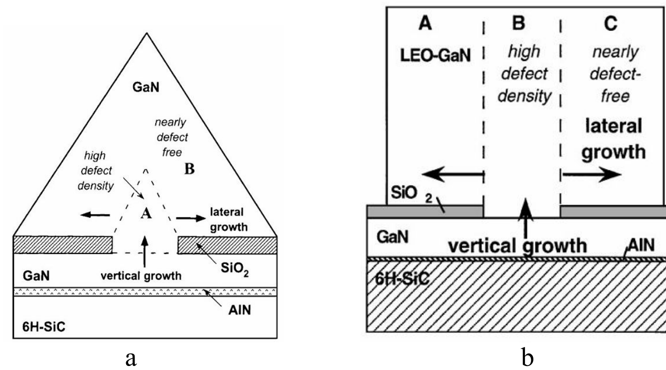


Fig. 20 *– Lateral Epitaxial Overgrowth of selectively grown GaN hexagonal pyramid (a). A schematic diagram of the lateral epitaxial overgrowth (LEO) in a selectively grown GaN stripe (b) (Ref. [48])*

Selectively grown (i.e., using SiO_2 mask) GaN hexagonal pyramids and stripes on circularly patterned GaN [0001] on sapphire [49-51] and 6H-SiC

[0001] substrate [52, 53], i.e., on GaN/AlN/6H-SiC heterostructure by the lateral epitaxy method (a two-stage mechanism containing vertical and lateral growth [54]) has also low dislocation density [27]. Nearly defect-free single crystal GaN is obtained during the lateral growth while analyzing with TEM. The thicknesses of the AlN buffer layer and the GaN layer are 1000 Å and 1.75 μm. The coalescence of the laterally grown volumes yields nearly defect-free regions. Curved surfaces are formed within the heterostructure, to accommodate mismatches due to the co-efficient of thermal expansions among the different phases [48].

GaN film grown on SiC by plasma-assisted MBE can reduce dislocation density significantly. Reduction of width of TEM $[10\bar{1}2]$ rocking curves with reduction of Ga/N flux ratio results in the change in morphology from flat to rough, creating reduction in edge-dislocation by cluster formation with topological valleys of the rough surface [55].

5. GAN ON SILICON SUBSTRATE

5.1 Advantages of Si substrate

Very low price is the most important advantage for choosing it as substrate. It is available in very large size; it has good thermal stability too. These aspects are suitable for GaN growth. Moreover, crystal perfection is very high in comparison with the other substrates for growth of GaN.

5.2 Disadvantages of Si Substrate

Lattice constant mismatch with GaN is very high (~ 16.9 % [56]). Thermal expansion co-efficient mismatch with GaN is also very high. Moreover, tendency of formation of amorphous SiN is noticeable during growth of GaN on it. All of these aspects are responsible for high defective interface formation (between GaN layer and Si substrate).

5.3 Choice of orientation for Si substrate for GaN growth

Generally (111) Si is taken as substrate for GaN growth. The GaN-made device quality using this substrate has much improved quality than any other orientation. It can support 2-D growth of GaN.

5.4 Reduction of Threading Dislocation density for GaN layer grown on Si substrate

Dadgar et al. showed that buffer layers were used to reduce TD density of GaN layer grown on Si substrate. The large mismatch (17 %) between GaN (a = 3.1891 Å) and Si (111) (a = 3.8403 Å) generated a biaxial tensile stress in the heterostructure [57]. Misfits and cracks were generated due to residual tensile stress [57]. Reduction of tensile stress as well as dislocation density was achieved by partial masking. For *in situ* masking of AlN seed layer with thin SiN mask [9] GaN-layer quality is improved. A thin SiN mask was used here. Fig. 22 shows that reduction of stress depends on the deposition time of SiN layer.

Insertion of Si_xN_y layer (along with AlN buffer layer grown by MOCVD) for GaN grown on a Si (111) layer, as shown in Fig. 23, reduced dislocation density much more. The growth temperature was 1080 °C here. With the increasing growth time, rms surface roughness decreases, pits due to TD decreases as Si_xN_y layer acted as a filter for TD [57].

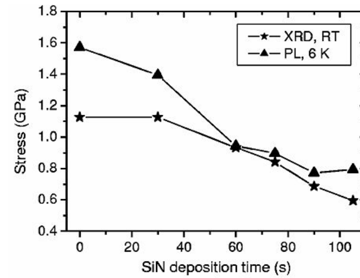


Fig. 22 *– Stress of the samples determined from PL (triangles) and x-ray diffraction (stars) measurements vs SiN deposition time. (Ref. [9])*

Growth time > 100 s can remove all types of dislocations (misfit dislocations too) resulting in a high quality GaN layer. K. Cheng et al. showed that instead of MOCVD, if high temperature MOVPE is applied for the same structure using a combination of AlGaN intermediate layer along with Si_xN_y layer, smooth and fully coalesced layer of dislocation density 3.0×10^8 - $5.0 \times 10^{8-2}$ cm can be obtained [58].

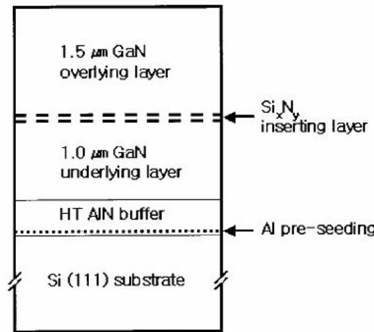


Fig. 23 *– Schematic cross-section of GaN epilayer (Ref. [57])*

6. CONCLUSION

Here we have studied different techniques of reduction of dislocation density of GaN layer grown on foreign substrates. We have chosen here three most commonly used substrates: sapphire, SiC and Si. We have studied the lattice mismatching percentage at the interface between the substrate and layer as well as other reasons of threading dislocations. reduction of dislocation density during the different growth techniques like MOCVD, MBE, HVPE, MOVPE etc., on three above mentioned substrates have been studied here separately.

Current researchers prefer sapphire substrate when comparing with SiC, though it has much higher lattice mismatch, thermal conductivity, difficulty in facet formation etc. Sapphire costs lower, provides relaxation to the growth and has lower surface roughness in comparison with SiC. Due to these reasons, researchers tried to reduce its dislocation density to increase its use as substrate.

Silicon has a very large lattice mismatch with GaN, resulting in very high dislocation density. Due to very low cost and thermal stability people have started working on GaN/Si growth technique recently. Still it has not extended in the industrial level. A good-quality low-cost GaN-on-Si substrate is still a good area of research.

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