University of Glasgow

Paterson, G.W. and Longo, P. and Wilson, J.A. and Craven, A.J. and Long, A.R. and Thayne, I.G. and Passlack, M. and Droopad, R. (2008) *Gallium oxide and gadolinium gallium oxide insulators on Si δ-doped GaAs/AlGaAs heterostructures.* Journal of Applied Physics, 104 . p. 103719. ISSN 0021-8979

http://eprints.gla.ac.uk/6526/

Deposited on: 23 July 2009

Enlighten – Research publications by members of the University of Glasgow
http://eprints.gla.ac.uk

Gallium Oxide And Gadolinium Gallium Oxide Insulators On Si δ-Doped GaAs / AlGaAs Heterostructures

G. W. Paterson,[1,*] P. Longo,[1] J. A. Wilson,[1] A. J. Craven,[1] A. R. Long,[1] I. G. Thayne,[2] M. Passlack,[3,†] and R. Droopad[3,‡]

[1]*Department of Physics and Astronomy, Faculty of Physical Sciences - University of Glasgow, Glasgow G12 8QQ, UK*

[2]*Department of Electrical and Electronic Engineering, Faculty of Engineering - University of Glasgow, Glasgow G12 8QQ, UK*

[3]*Freescale Semiconductor Inc., Tempe, Arizona 85284, USA*

(Dated: May 28, 2009)

Test devices have been fabricated on two specially grown GaAs / AlGaAs wafers with 10 nm thick gate dielectrics composed of either Ga_2O_3 or a stack of Ga_2O_3 and $Gd_{0.25}Ga_{0.15}O_{0.6}$. The wafers have two GaAs transport channels either side of an AlGaAs barrier containing a Si δ-doping layer. Temperature dependent capacitance-voltage (C-V) and current-voltage (I-V) studies have been performed at temperatures between 10 K and 300 K. Bias cooling experiments reveal the presence of DX centres in both wafers. Both wafers show a forward bias gate leakage that is by a single activated channel at higher temperatures and by tunnelling at lower temperatures. When $Gd_{0.25}Ga_{0.15}O_{0.6}$ is included in a stack with 1 nm of Ga_2O_3 at the interface, the gate leakage is greatly reduced, due to the larger band-gap of the $Gd_{0.25}Ga_{0.15}O_{0.6}$ layer. The different band-gaps of the two oxides result in a difference in the gate voltage at the onset of leakage of $\sim$3 V. However, the inclusion of $Gd_{0.25}Ga_{0.15}O_{0.6}$ in the gate insulator introduces many oxide states ($\geq 4.70\times10^{12}$ cm^{-2}). Transmission electron microscope images of the interface region show that the growth of a $Gd_{0.25}Ga_{0.15}O_{0.6}$ layer on Ga_2O_3 disturbs the well ordered Ga_2O_3 / GaAs interface. We therefore conclude that, while including $Gd_{0.25}Ga_{0.15}O_{0.6}$ in a dielectric stack with Ga_2O_3 is necessary for use in device applications, the inclusion of Gd decreases the quality of the Ga_2O_3 / GaAs interface and near interface region by introducing roughness and a large number of defect states.

PACS numbers: 71.55.Eq, 72.20.-i, 73.20.At

I. INTRODUCTION

Hafnium-based oxides are widely expected to succeed SiON in planar bulk MOSFETs to allow the performance increases that have been achieved through scaling in CMOS IC's to continue. However, beyond the 22 nm node, no solution yet exists.[1] One possibility is to change the semiconductor system from Si to III-V's, to take advantage of their intrinsically high electron mobility in low power field effect technologies. III-V's have been used in high-speed applications for many years, but have not undergone the scaling that the Si system has because of a lack of a suitable gate insulator.

Recent work by Passlack[2] and Hale et al.[3] on oxides on GaAs has advanced their quality and the understanding of Fermi-level pinning and unpinning, respectively. When Ga_2O is deposited on a clean (001)2×4 GaAs surface in UHV by MBE, it adsorbs (onto the surface) by bonding to the As dimer atoms, leaving the surface charge in a bulk-like, unpinned, state. STS[3] and PL[2] studies have shown this interface to be of high quality, i.e. with few localised electronic

states, $\leq 1\times10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ after appropriate treatment.[2]

However, the conduction band offset (CBO) from GaAs to Ga_2O_3 is only 0.8 eV,[4] and there can be large leakage current in structures using this oxide when they are forward biased. This can severely limit the voltage region over which the C-V characteristics can be observed at room temperature,[5] and can prevent the use of standard C-V techniques to characterise the oxide-semiconductor interface in n^+ MOS samples.

The presence of Ga_2O_3 is necessary to unpin the Fermi-level. When a $Gd_{0.25}Ga_{0.15}O_{0.6}$ layer is included in an oxide stack with a thin Ga_2O_3 template layer, the gate leakage at positive gate voltage is greatly reduced, due to $Gd_{0.25}Ga_{0.15}O_{0.6}$ having a larger CBO to GaAs. Afanas'ev et al.[4] have measured the offsets in a similar dielectric stack on GaAs and obtain a value of 1.5 eV for the Gd_2O_3 subnetwork.

In previous work,[5] we reported the results of studying the C-V and I-V characteristics of the wafer shown in Fig. 1 with a Ga_2O_3 insulator at room temperature and below to reveal the transport mechanism and the characteristics of any oxide and donor states. The wafer has two GaAs transport channels either side of an $Al_{0.3}Ga_{0.7}As$ layer with a Si δ-doping layer in the middle which is clad by 1 monolayer (ML) of GaAs on each side to reduce DX centre formation.

The benefits of this structure over more simple structures are three fold. Firstly, compared to a MOS sample with an n^+ substrate, the additional barriers present between the centre of mass of the charge carriers in the semiconductor and the oxide reduce the gate leakage and allow the C-V characteristics to be observed over a greater voltage range. This opens the opportunity to directly compare the C-V characteristics of the same structure with different gate oxides. Secondly, the observed properties will be more characteristic of those one would expect to see in a real device. Thirdly, magnetotransport measurements can be performed and the results compared with the C-V characteristics of the same structure. The purpose of the inclusion of the surface GaAs layer is to allow the effect of proximity to the insulator of the conduction channels that form to be inferred from magnetotransport measurements. Preliminary magnetotransport measurements were reported in Ref. 5, more detailed analysis will be published elsewhere.

n-doped III-V materials can contain DX states, or deep level donor states. DX states in $Al_xGa_{1-x}As$ are localised electronic ground states of isolated substitutional donors in distorted configurations, with each state occupied by two electrons.[6,7] These states are polaronic and thus have barriers to both entry to and exit from them, with the latter being greater than the former. Up to four deep donor related states with different abundances and energetics, corresponding to the four configurations of Ga and Al neighbours of the Si atoms, have been observed in Si doped $Al_xGa_{1-x}As$.[8] We will use the same nomenclature for the four DX levels as that used by Mooney: DX0, DX1, DX2 and DX3,[9]; where the number refers to the number of surrounding Al atoms. The strength of lattice polarisation upon capture of electrons and the depths of the resulting levels increase from DX0 to DX3 and the capture and emission rates decrease.

Because of the presence of barriers in DX states, bias cooling techniques can be used to investigate them. In a traditional bias cool experiment, a metastable trap configuration is generated in a sample by applying a bias at a high temperature, cooling the sample under bias to a low temperature, and then observing the threshold voltage. By applying different biases in this way to populate and deplete the states, the changes in threshold voltages at low temperature can be used to determine the density of DX states, if the effect of other states is negligible. If other states are present, their effects must be deconvolved from those of DX states. In the bias cool experiment performed here, the threshold will be measured at low temperature and as the sample is annealed and the gate voltage is cycled. This is done to provide additional information about the states that are present.

In this work we report the results of similar C-V and I-V studies on an identical wafer with a $Gd_{0.25}Ga_{0.15}O_{0.6}$ / Ga_2O_3 insulator (wafer 2). These are performed as a function of temperature to reveal the electron trapping and transport mechanisms, and to compare them directly with those from the Ga_2O_3 wafer (wafer 1). This allows assessment of the effect on the electrical properties and hence the trap distribution of including $Gd_{0.25}Ga_{0.15}O_{0.6}$ in the dielectric.

In both wafers, the oxide was deposited by MBE on an As stabalised (001)2×4 GaAs surface under UHV conditions. In wafer 2, the first oxide layer was a thin template layer of Ga_2O_3. After the template layer reached a thickness of 1 nm, $Gd_{0.25}Ga_{0.15}O_{0.6}$ was deposited to make up an oxide stack with a total thickness of 10 nm. Growth of the template layer in wafer 1 was identical to that in wafer 2. After the template layer has formed, the deposition of Ga_2O_3 continued until the oxide was 10 nm thick. Further details of the oxide growth can be found in Ref 10.

II. EXPERIMENTAL

The electrical measurements presented here have been made on samples with annular surface ohmic and gate contacts defined using standard electron beam lithography techniques. A platinum / gold stack was used for the gate metal in all samples. The samples were measured at temperatures between 10 K and 300 K in a closed-circuit He cryostat using a Keithley System 82 for C-V measurements and Keithley 236 SMU for I-V measurements. The TEM images were obtained in an FEI Tecnai F20 from samples that were dimpled and then thinned to electron transparency using a Gatan PIPS ion mill.

III. RESULTS AND DISCUSSION

Fig. 2 shows the gate leakage in wafer 2 at positive gate voltages and different temperatures. At temperatures below around 100 K, the leakage is approximately independent of temperature, indicating the dominant transport mechanism is tunnelling. The threshold voltage for leakage at 10 K is approximately 3 V higher here (∼ 3.75 V) than in wafer 1, which indicates that the oxide CBO to GaAs is significantly larger when Gd is included in the oxide. At temperatures above ∼ 250 K, leakage is strongly dependent on temperature, indicating the dominant mechanism has a thermally activated component.

The two most commonly used and successful models of thermally activated conduction processes in insulators are those of Poole-Frenkel and Schottky emission, the general equations for which are given by Eq. 1 and Eq. 2, respectively,[11]

$$J_{SE} = AT^{3/2} exp\left(-q\left(\phi_b - \sqrt{q\xi/4\pi\varepsilon_i}\right)/k_BT\right) \tag{1}$$

$$J_{P-F} \propto \xi exp\left(-q\left(\phi_b - \sqrt{q\xi/\pi\varepsilon_i}\right)/k_BT\right) \tag{2}$$

where J, A, T, q, ϕ_b, ξ, ε_i, and k_B are the current density, the 2D Richardson constant, the absolute temperature, the electronic charge, a potential barrier height, the field in the insulator, the dynamic absolute permittivity of the insulator, and Boltzmann's constant.

The second term in the exponential in both equations is the image charge induced barrier lowering (ICIBL). The field at which the barrier lowering becomes significant depends on the CBO, the barrier height and the dynamic permittivity. It is important to consider for each wafer whether barrier lowering will have a significant effect on the derived barrier height.

The conduction processes are shown schematically in Fig. 3. In the Poole-Frenkel model, transport is by field enhanced thermal excitation of carriers between adjacent states in the insulator. The barrier height is the potential between the state and the oxide conduction band edge and is independent of gate voltage (there may of course be some dependence of the barrier height on gate voltage through ICIBL). In the Schottky emission model, the current is also by carriers thermally excited over a barrier, but the carriers are in states in the conduction band of the semiconductor and the barrier is formed by the oxide conduction band edge. The current is dependent on the density of states in the conduction band of the semiconductor, which in our case is a two dimensional electron gas and thus is proportional to $T^{3/2}$. Because the electrons that flow over the barrier are excited from energies at the Fermi-level, and the Fermi-level is a function of gate voltage, unlike in the Poole-Frenkel model, the barrier height in the Schottky emission model is a function of gate voltage. As in the case of Poole-Frenkel transport, ICIBL may also have an effect on the dependence of the barrier height to gate voltage.

Because the pre-exponent in both models is very much weaker than the exponent, both processes can be analysed using the Schottky emission model to give reasonably accurate values for the barrier height. This approach has the benefit that, if the ICIBL can be ignored, the characteristics can be analysed without having accurate knowledge of, or making assumptions about, the field in the oxide. Thus, an Arrhenius plot of $ln\left(J/T^{3/2}\right)$ vs. $1/T$ should yield a straight line with $q\phi_B$ as its gradient in both cases. Examples of the Arrhenius plots for the data in Fig. 2 are shown in the inset to Fig. 4 and are approximately linear at temperatures of 270 K and above and at voltages above 3.55 V. The barrier heights have been extracted by fitting straight lines to the data and are plotted against voltage in the main figure.

Clearly, the barrier height is not independent of gate voltage and thus the gate leakage in this temperature and voltage range is not by the Poole-Frenkel process. Although this result is in contrast to the work of Chen et al.[12], who extract a constant barrier height over a range of gate voltages from analysing the current from samples with an n^+ substrate using the Poole-Frenkel model, the structure of the wafers on which their experiments were based is different from our more device-like structures. As in our earlier work on wafer 1,[5] the barrier height varies linearly with voltage, suggesting that Schottky emission is the dominant mechanism. We believe electrons are being emitted from the surface GaAs channel to the metal over a conduction band edge or through localised states that are distributed over a wide energy range near the band edge. In wafer 1, the gradient of the $q\phi_b(V_g)$ plots was -1.02 eV/V. This figure is close to the ideal value of 1, indicating that barrier lowering can be ignored. In wafer 2 however, the gradient is -0.58 eV/V, and other mechanisms in addition to Schottky emission must be considered.

In the voltage region of interest, the conduction band profile will be similar to that shown in Fig. 3, where the field in the oxide is in a direction pointing away from the gate, towards the substrate. Increasing the gate voltage increases the field in the oxide, which causes the effect of ICIBL to increase with increasing gate voltage. If this were the dominant mechanism, then the extracted barrier height would be lower than expected in the ideal case by an amount which increases with gate voltage and, thus, the gradient of the $q\phi_b(V_g)$ plot would be greater than unity. This is not the case and ICIBL cannot account for the gradient. One explanation for the reduced gradient is electrons tunnelling

through the top of the barrier. In wafer 1, the CBO is low, causing significant thermionic emission currents to develop at low gate voltages and limiting the field that can be created in the oxide. In wafer 2, the CBO is larger and the bands must be pulled down further, creating a much larger field in the oxide before significant thermionic emission occurs. Thus, the shape of the conduction band at the energy which determines the barrier height will be different in the two wafers, when the current increases significantly with gate voltage. The barriers will be triangular in both cases, but will be broad in wafer 1 and narrow in wafer 2. The narrow barrier in wafer 2 will make it easier for the electrons in the GaAs channel to tunnel through the barrier and will reduce the dependence of the measured barrier height on gate voltage. In this model, thermionic emission is still the dominant mechanism, so the characteristics of the mechanism, such as temperature dependence, are still present in the I-V characteristics.

In a similar way to that reported in Ref. 5, the C-V characteristics of both wafers have been measured as a function of temperature in zero, negative, and positive bias cool experiments to assess the barriers present to entry and exit of states. In these experiments, the sample is cooled to 10 K under the appropriate bias and the gate voltage is swept through the cycle $0 \rightarrow V_a \rightarrow V_b \rightarrow V_a \rightarrow V_b \rightarrow 0\,\mathrm{V}$ every 10 K as the sample is annealed to 300 K, where V_a and V_b are the limits of the gate voltage sweep. This gives rise to the five sweep regions shown in Table I, in each of which a threshold voltage can be defined. For simplicity, we define V_c to be the gate voltage at a capacitance of $1{\times}10^{-3}\,\mathrm{Fm}^{-2}$ and use it as a measure of threshold voltage (the voltage corresponding to this capacitance lies just above threshold). If V_a and V_b are chosen correctly, there are always at least three V_c values in each full sweep; V_{c2}, V_{c3}, and V_{c4}. The existence of V_{c1} and V_{c5} is dependent on the threshold voltage and the hysteresis present in a given sweep. Measures of the hysteresis can be defined by $V_{c3} - V_{c2}$ for trapping, $V_{c4} - V_{c3}$ for de-trapping and $V_{c4} - V_{c2}$ for net-trapping. The values can be plotted against temperature to reveal how the threshold voltages and hysteresis change with temperature and, therefore, can reveal the characteristics of the states.

The V_a values were chosen to deplete the two channels and the V_b values to populate the channels whilst not entering the high leakage current region. As can be seen in Fig. 5, which shows a sample of the C-V characteristics of wafers 1 and 2 at temperatures between 10 K and 300 K in 0 V bias cool experiments, the required gate voltage sweep limit values are smaller for wafer 1 ($V_a = -1.5V$, $V_b = +1V$) than for wafer 2 ($V_a = -3V_b$, $V_b = +3V$). The values differ because of oxide state and gate leakage effects (discussed later). If these values had been used, the range of energies through which the Fermi level would pass at the oxide-semiconductor interface and at the donors would be different for the two wafers. Because of this, the smaller of the two sets of gate voltage sweep limits were used for both wafers in the remainder of this work.

Returning to Fig. 5, the rise in capacitance at high voltage in both wafers results from a decrease in the distance between the electrons in the semiconductor and the gate as electrons begin to populate the surface channel. The drop in capacitance in wafer 1 is due to excessive gate leakage that occurs in that voltage region. Beginning with wafer 1 (Fig. 5(a)), there are several important features:

1. The threshold voltage is a function of temperature.

2. There are temperature ranges where hysteresis between positive and negative going traces is observed, and others where there is little or no hysteresis.

3. There are two temperature regions where the transition between depletion and accumulation widens and the threshold moves to more negative gate voltage, while the hysteresis peaks and then decreases to zero, as the

temperature is increased.

4. Below temperatures of around 80 K there is little hysteresis and only small changes in the threshold voltage.

Note that some of these features are more easily seen in Fig 6(a), (b), and (c).

These characteristics can only be explained by the presence of two populations of states with different capture and emission cross sections, where, for both populations, the former is greater than the latter and the latter increases rapidly with temperature.

Following Mooney,[9] for 30 % AlGaAs we expect there to be 3 DX levels below the conduction band edge, the DX1, DX2, and DX3 states. The DX3 states are the deepest and are relatively few in number, so we expect there to be two significant populations of active and accessible DX states. Because of their position in energy, the DX0 and DX3 states most likely remain respectively fully occupied and completely ionised throughout the voltage range explored. For a given population of DX states and gate voltage sweep rate, there will be a temperature at which some states will not be in equilibrium with the gate voltage for at least a portion of the sweep. When this is the case, hysteresis and threshold voltage shifts will be seen in the C-V characteristics. The temperature at which these features will be seen increases with the depth of the state. Thus, the behaviour seen in the C-V characteristics fits well with the characteristics of DX states. We conclude that the high temperature effects are due to the deeper DX2 state, while the lower temperature effects are due to the shallower DX1 state.

To confirm the presence of DX states, bias cool experiments were performed. Fig. 6(a) shows how the threshold voltage changes with temperature in different bias cooling experiments on wafer 1. We believe that all of the threshold voltage changes are caused by DX states and find no evidence of oxide states in this wafer. However, this does not mean that there are no oxide states or that they do not contribute to the threshold voltage changes, which may be the case. All that can be said with certainty is that the density of oxide states is very much less than that of the donors. The calculations performed to support this statement are given in detail in Ref. 5. It should be noted that we attribute the irreversible hysteresis at 10 K to the filling of DX1 states despite the fact that all DX states have a barrier to entry. This is not inconsistent, however, as it may be possible for the electrons to tunnel through the relatively low barrier.

The de-trapping hysteresis plots for wafer 1 (along with those for wafer 2) are shown in Fig. 6(c). For wafer 1 the plots are identical to one another, despite the different DX state occupations at the start of the experiment. This is because the barrier to exit is higher than that to entry into DX states and, therefore, any states that can be occupied at a given temperature can be subsequently ionised. The shape of this profile is, we believe, a result of DX states alone. The details of the DX state trapping and de-trapping processes and how they change with temperature are shown in annotations on the figures.

The C-V characteristics of wafer 2 are qualitatively similar to those of wafer 1. However, when examined in detail there are important differences. Fig. 6(b) shows the threshold voltage plots for wafer 2. The same general shape of threshold voltage shifts and hysteresis in wafer 1 are present in the characteristics of wafer 2, which we believe are the result of DX states, but the magnitudes of the shifts and hysteresis are in places larger than those in wafer 1. The difference between the characteristics from the two wafers is directly related to the presence of oxide states. The initial irreversible hysteresis at 10 K in wafer 2 is seen in Fig 6(b) as a vertical line and is a factor of ~ 4 larger than that in wafer 1. We ascribe this to oxide states in wafer 2 which easily trap charge at 10 K. This suggests that the

oxide states have little or no barrier to entry.

The effect of oxide states can also be seen at temperatures between 130 K and 280 K. In this region, the zero and positive bias cool data of wafer 2 are similar to one another and, in the negative bias cool data, the threshold is more positive and there is greater hysteresis than in the zero or positive bias cool data (Fig. 6(c)). This is surprising, but may be explained by the depletion of oxide and DX states at room temperature making accessible a greater number of oxide states at low temperature. These states then become occupied when the gate voltage is swept and this results in greater hysteresis as the system moves towards equilibrium conditions. This idea is supported by the absence of this effect in wafer 1, which has far fewer oxide states, and by the similarity in the maximum temperature at which the feature is present to that at which the oxide states remain in a non-equilibrium state. Fig. 6(d) makes this clear by plotting the difference between the de-trapping hysteresis characteristics for the two wafers in the two different regions highlighted in the hysteresis plots. Region 1 is the difference between the 0 V bias cool of each wafer. Region 2 is the difference between the 0 V and -2 V bias cool of wafer 2. At temperatures below 130 K, de-trapping in the oxide states is effectively frozen and the hysteresis is close to zero. As the temperature is increased, the hysteresis goes through a peak and then decreases to close to zero while, relative to wafer 1, the threshold becomes more negative. At temperatures above 280 K, the oxide states are able to de-trap in equilibrium with the gate voltage and the hysteresis is similar to that in wafer 1 and is mainly due to DX states.

If a charge centroid of carriers occupying oxide states, $\overline{x}$, is assumed, a lower limit of the density of oxide states, N_t, in wafer 2 can be found from the maximum total threshold hysteresis caused by the states, ΔV, using Eq. 3

$$N_t = \frac{\varepsilon_o \varepsilon_{ox}}{q\overline{x}} \Delta V \tag{3}$$

where ε_{ox} and ε_o are the oxide relative permittivity and the permittivity of free space. The maximum total hysteresis, found by summing the individual hysteresis from the two regions shown in Fig. 6(d), is 0.425V. Assuming an oxide relative permittivity of 20, and that the charge centroid is located at the oxide / semiconductor interface, gives a density of oxide states of $4.70\times10^{12}\,\text{cm}^{-2}$. This number is comparable to those reported by Passlack[2] on similar oxide stacks using conventional C-V analysis techniques.

The features of oxide states discussed here have also been observed in n^+ wafers with similar dielectric stacks, where DX are absent. In n^+ wafers, as in wafer 2, after a negative bias cool there is a large irreversible hysteresis at 10 K and, in positive bias cools, the de-trapping hysteresis starts at a temperature of around 150 K, see Fig 7. However, unlike in wafer 2, the de-trapping in the n^+ sample hysteresis profile increases smoothly with temperature without any of the fine structure seen in the characteristics of wafer 2. This confirms that the fine structure in the data from the heterostructures is related to the DX states alone.

Although oxide states produce apparently similar features to those produced by DX states, we must be careful about how we interpret the results. For interface states with no barrier to entry or exit, i.e. non-polaronic states, the capture and emission times, τ_c and τ_e, for a state at energy E_T within the band gap are given by

$$\tau_c = \frac{1}{v_{th}\sigma_n n} \tag{4}$$

and

$$\tau_e = \frac{exp\left(\frac{E_C - E_T}{k_B T}\right)}{v_{th}\sigma_n N_C} \tag{5}$$

where v_{th}, σ_n, n, E_C, and N_C are the electron thermal velocity, the capture cross section, the free carrier concentration in the conduction band, the energy of the conduction band edge minimum, and the effective density of states in the conduction band.

A measure of the response of a trap when the gate voltage is cycled is given by $\tau_e/\tau_c = exp\left(\frac{E_F - E_T}{k_B T}\right)$, where E_F is the Fermi energy. The capture and emission times are symmetric only when the Fermi level is at the energy of the trap. Unless the gate voltage sweep rate is such that all states remain in equilibrium with the gate voltage at all times, there will be hysteresis resulting from the non-equilibrium occupation of states that fill only after they have passed through and fallen below the Fermi level, for these states fill quicker than they can be emptied.

If this mechanism were the dominant one and the temperature were varied in bias cool experiments, one would expect the hysteresis to change and the threshold voltages to move in the same way as they do in the experimental results that we ascribe to oxide states. Because of this and despite the similarity of the oxide and DX state features, we cannot conclude that the oxide states are polaronic.

Fig. 8 shows bright-field transmission electron microscopy (TEM) images of the oxide-semiconductor interface for the two wafers. In bright-field imaging, regions of higher atomic number tend to be darker, so, GaAs, $Gd_{0.25}Ga_{0.15}O_{0.6}$ and Ga_2O_3 image with increasing brightness. In wafer 1, the GaAs interface with Ga_2O_3 is atomically flat over lateral ranges of 10 to 15 nm, where the first ML or so of Ga_2O_3 has grown epitaxially. At the interface between the flat regions, the step height is typically 1 ML. The remainder of the oxide is amorphous. In wafer 2, however, the Ga_2O_3 / GaAs interface, which was grown under the same conditions, is less well ordered, exhibiting a roughness of 1 or 2 MLs on a lateral scale of about 1 nm. The interface between the Ga_2O_3 template layer and the $Gd_{0.25}Ga_{0.15}O_{0.6}$ layer in wafer 2 is not clearly visible in this image. This suggests that the interface is graded, despite not being grown as such. Thus, as well as introducing a second interface, the growth of the $Gd_{0.25}Ga_{0.15}O_{0.6}$ layer on the Ga_2O_3 template layer disturbs the underlying Ga_2O_3 / GaAs interface.

It is at these two interfaces that the differing bond lengths of the component materials is likely to result in defect states in addition to those that may be present in the bulk of the layers. Although from this work it is not possible to assign the oxide states seen in wafer 2 to any particular region with absolute certainty, it seems reasonable to suggest that these changes relative to wafer 1 may introduce fast interface states at the Ga_2O_3 / GaAs interface and slower states with longer response times deeper in the oxide, perhaps at the second interface. This view is supported by the recently published results of photoluminescence intensity studies[13] which are sensitive only to the immediate semiconductor/oxide interface region and show that this interface is not severely affected when $Gd_{0.25}Ga_{0.15}O_{0.6}$ is deposited on Ga_2O_3, and by the work of Afanasev et al.[4] who suggest the presence of bulk states in $Gd_xGa_{0.4-x}O_{0.6}$ from internal photoemission measurements..

Despite these issues, using similar oxide stacks to those used in this work, enhancement mode $In_{0.3}Ga_{0.7}As$ channel devices with a mobility of over 5000 $cm^2V^{-1}s^{-1}$ and a transconductance of over 475 μS/μm have been made.[14]

IV. CONCLUSIONS

Clear evidence of two DX centres have been seen in the C-V characteristics from bias cooling experiments. We find no evidence of oxide states in the Ga_2O_3 wafer. However, the CBO of Ga_2O_3 to GaAs is low and causes large currents to flow through the oxide in forward bias. When Gd is included in the form of $Gd_{0.25}Ga_{0.15}O_{0.6}$ in a stack with 1 nm

of Ga_2O_3 at the GaAs interface, the gate leakage is greatly reduced as a result of the larger CBO to GaAs, but many oxide states are also introduced. Because of the masking effect of the DX centres, we are not able to measure directly the density of states at the oxide-semiconductor interface in these wafers. By comparing the characteristics of the two wafers, however, we estimate that the minimum density of oxide states in the $Gd_{0.25}Ga_{0.15}O_{0.6}$ / Ga_2O_3 wafer is $4.70\times10^{12}\,\mathrm{cm}^{-2}$. The oxide states in this wafer have little or no barrier to entry. We cannot say whether there is one to exit.

In both wafers, the gate leakage in forward bias is strongly dependent on temperature and has a thermally activated component. The barrier heights obtained by analysing this component at temperatures above 270 K and 170 K for the stack and Ga_2O_3, respectively, vary linearly with gate voltage, showing that gate leakage is by a single activated channel, most likely formed by the oxide conduction at the band edge. The threshold of current onset at low temperatures is 0.75 V in the Ga_2O_3 wafer and is $\sim$3 V larger in the wafer with the stack, reflecting the different barrier heights.

The different electrical characteristics correlate with the differing microstructures of the two wafers: the Ga_2O_3 / GaAs interface is well ordered and there are few defect states, but when Gd is included, the interface is disturbed and a large number of states are introduced. We therefore conclude that, while including $Gd_{0.25}Ga_{0.15}O_{0.6}$ in a dielectric stack with Ga_2O_3 is necessary for use in device applications, the inclusion of Gd decreases the quality of the Ga_2O_3 / GaAs interface and near interface region by introducing roughness and defect states.

V. ACKNOWLEDGEMENTS

This work was supported by the EPSRC of the UK under grant number GR/S61218/01. The authors would like to acknowledge the assistance of Brian Miller, who prepared the TEM samples.

---

* Electronic address: g.paterson@physics.gla.ac.uk

† Now at University of California - San Diego, Department of Chemistry and Biochemistry, 9500 Gilman Dr., La Jolla, California, 92093, USA

‡ Now at Texas State University-San Marcos, Department of Physics, 601 University Drive, San Marcos, Texas, 78666, USA

[1] International Technology Roadmap for Semiconductors (2006), available at http://www.itrs.net/Links/2006Update/2006UpdateFinal.htm.

[2] M. Passlack, In Material Fundamentals of Gate Dielectrics, Springer, 411 (2005), Edt. A. A. Demkov and A. Navrotsky.

[3] M. J. Hale, S. I. Yi, J. Z. Sexton, and A. C. Kummel, J. Chem. Phys., 119, 6719 (2003).

[4] V. V. Afanas'ev, A. Stesmans, M. Passlack, and N. Medendorp, Appl. Phys. Lett., 85, 597 (2004).

[5] G. W. Paterson, J. A. Wilson, D. Moran, R. Hill, A. R. Long, I. Thayne, M. Passlack, and R. Droopad, Mater. Sci. Eng., B, 135, 277 (2006).

[6] D. J. Chadi and K. J. Chang, Phys. Rev. Lett. 61, 873 (1988).

[7] D. J. Chadi and K. J. Chang, Phys. Rev. B 39, 10063 (1989).

[8] P. M. Mooney, T. N. Theis, and S. L. Wright, Appl. Phys. Lett,. 53, 2546 (1988).

[9] P. M. Mooney, Semicond. Sci. Technol., 6, B1 (1991).

[10] R. Droopad, K. Rajagopalan, J. Abrokwah, and M. Passlack, J. Vac. Sci. Technol. B., 24, 1479 (2006).

[11] See, for example, S. M. Sze, Physics of Semiconductor Devices: 2nd Ed, New York, (1981).

[12] A. Chen, M. Passlack, N. Medendorp, and D. Braddock, Appl. Phys. Lett., 84, 2325 (2004).

[13] M. Passlack, R. Droopad, Z. Yu, N. Medendorp, D. Braddock, X. W. Wang, T. P. Ma, T. Buyuklimanli, IEEE Electron Device Lett. 29, 1181 (2008).

[14] R. J. Hill, D. A. J. Moran, Li Xu, Zhou Haiping, D. Macintyre, S. Thoms, A. Asenov, P. Zurcher, K. Rajagopalan, J. Abrokwah, R. Droopad, M. Passlack, and I. G. Thayne, Electron Device Letters, IEEE, 28, 1080 (2007).

TABLE I: Threshold voltage and its position in the gate voltage sweep of $0 \rightarrow V_a \rightarrow V_b \rightarrow V_a \rightarrow V_b \rightarrow 0\,\mathrm{V}$, where $V_b > V_a$.

Order	Sweep Region	Threshold
1	$0 \rightarrow V_a$	V_{c1} [a]
2	$V_a \rightarrow V_b$	V_{c2}
3	$V_b \rightarrow V_a$	V_{c3}
4	$V_a \rightarrow V_b$	V_{c4}
5	$V_b \rightarrow 0$	V_{c5} [a]

[a] Threshold voltage not always available.

FIG. 1: The structure of the wafer from which the heterostructure samples used in this work were fabricated. The insulator was either entirely Ga_2O_3 or a stack of 1 nm of Ga_2O_3 followed by $Gd_{0.25}Ga_{0.15}O_{0.6}$. The locations of the two transport channels, the oxide states, and the DX states are indicated.

FIG. 2: (Colour online) Dc gate leakage current density versus gate voltage at temperatures between 300 K and 10 K in wafer 2, showing the strong temperature dependence of the current at temperatures above ~ 250 K, and the independence of temperature at temperatures below 100 K.

FIG. 3: An example conduction band edge diagram showing the Poole-Frenkel and Schottky emission conduction processes and the associated activation energies E_{PF} and E_{SE}, respectively, drawn in a condition of far forward bias and including ICIBL.

FIG. 4: (Colour online) Arrhenius activation energy, or barrier height, extracted from the data in Fig. 2, as a function of gate voltage and a linear fit to the data. Inset are examples of the Arrhenius plots and straight line fits.

FIG. 5: (Colour online) C-V characteristics of the two wafers at the temperature indicated as the sample is annealed after a 0 V bias cool. The arrows indicate the direction of hysteresis.

FIG. 6: (Colour online) Threshold voltage for wafer 1, (a), & wafer 2, (b), and de-trapping hysteresis for both wafers, (c), as a function of temperature from different bias cool experiments at the voltages shown. The various trapping and de-trapping processes and how they vary with temperature are shown in the annotation. The hatched regions in (c) show the effect of oxide states. The vertical extent of the two regions are plotted against temperature in (d). Note that the hysteresis at 10 K in (a) and (b), which is seen as a vertical line, has been added from the V_{c2} values.

FIG. 7: De-trapping hysteresis as a function of temperature for an n^+ wafer with a thick oxide stack after a +3 V bias cool.

FIG. 8: Bright-field TEM images of the oxide semiconductor interface for (a) wafer 1, and (b) wafer 2, in as grown condition.

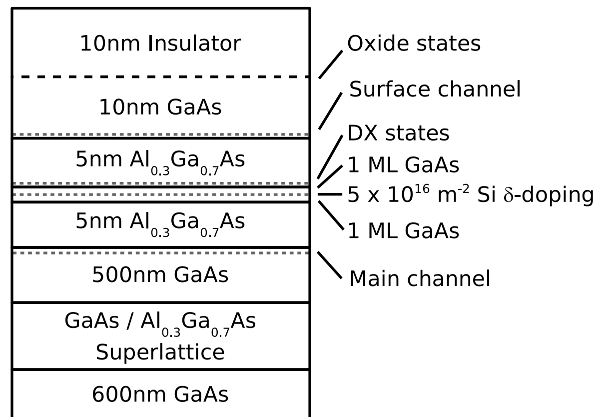

FIG. 1:

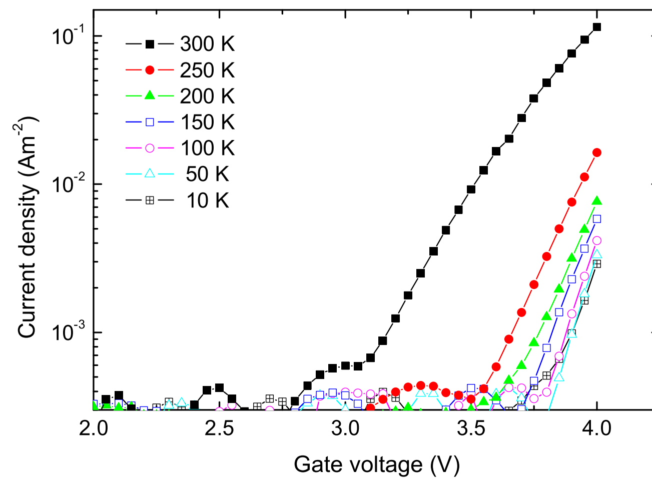

FIG. 2:

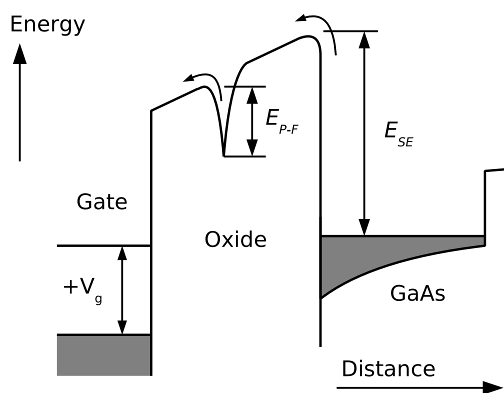

FIG. 3:

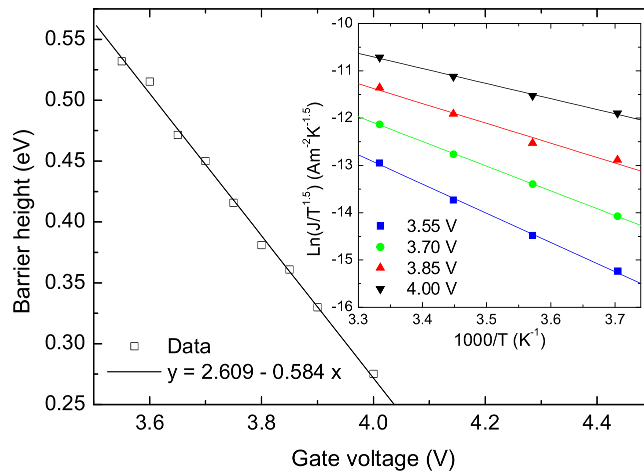

FIG. 4:

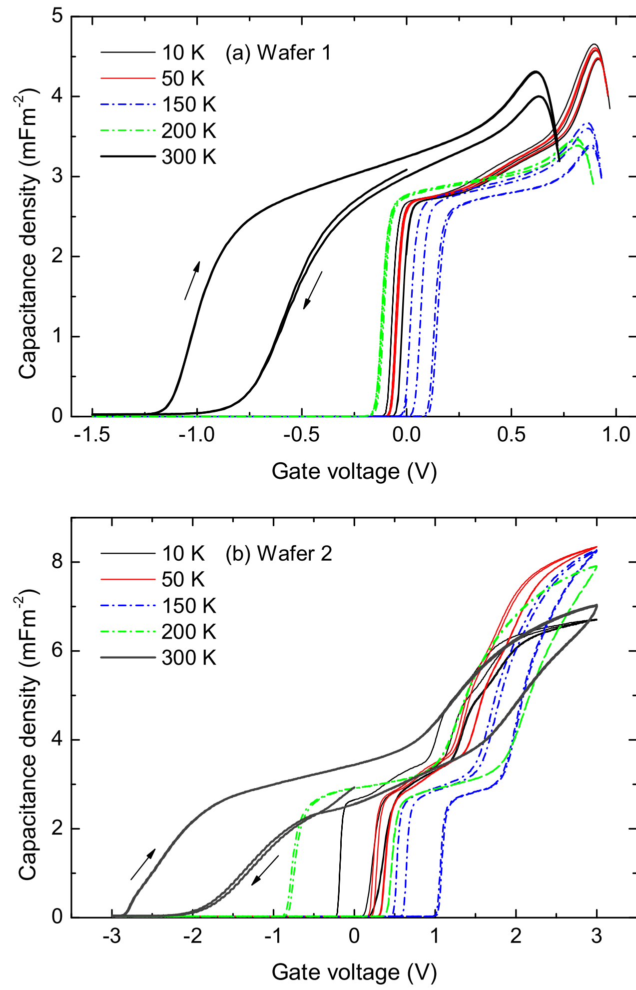

FIG. 5:

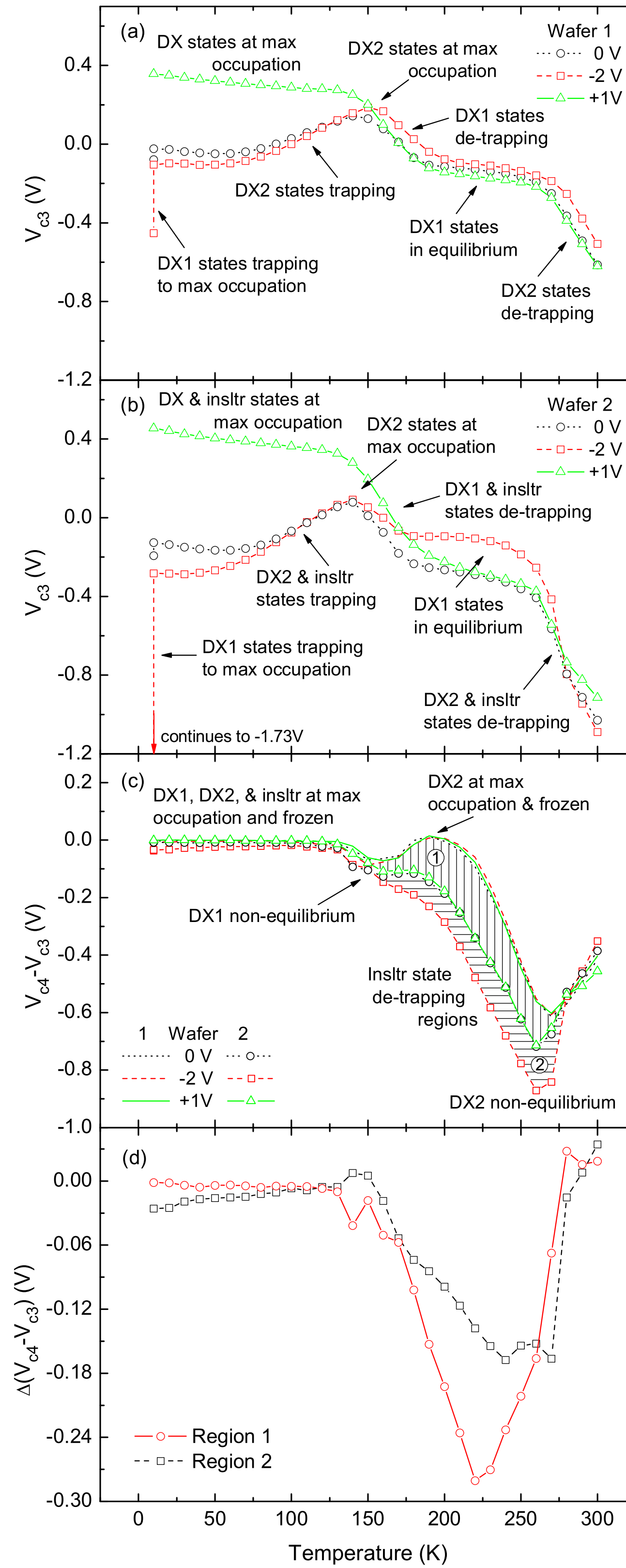

FIG. 6:

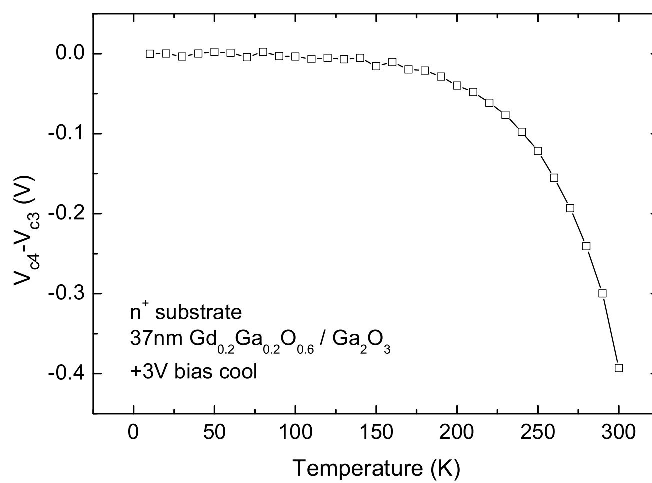

FIG. 7:

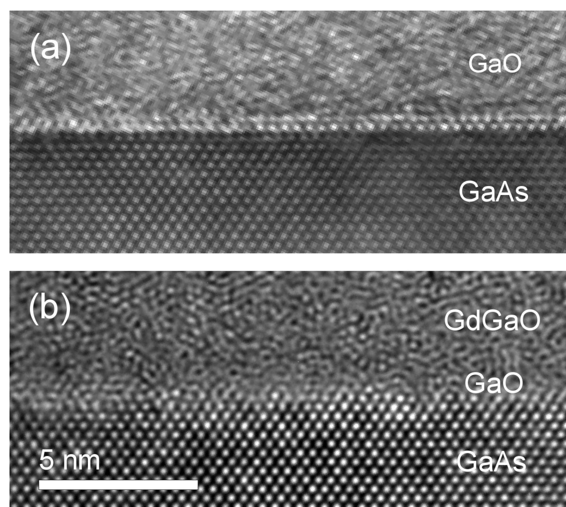

FIG. 8: