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Thin Film Crystal Growth Template Removal: Application to stress reduction in Lead Zirconate Titanate Microstructures.

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Abstract

A key issue for the design and reliability of micro devices is process related, residual stresses in the thin films from which they are composed, especially for sol-gel deposited $Pb(Zr_x,Ti_{1-x})O_3$ ceramics, where use of Pt as a template layer, though essential for the nucleation of the perovskite phase, results in structures with levels of stress high and largely fixed by the thermal expansion coefficient mismatch between Pt and Si. Here a technique for the elimination of this stress is presented, involving the use of adhesive wafer bonding and bulk micromachining procedures to remove the Pt layer following the $Pb(Zr_x,Ti_{1-x})O_3$ deposition.

Interest in $Pb(Zr_xTi_{1-x})O_3$ (PZT), as a functional material for Micro Electro Mechanical Systems (MEMS) applications has grown significantly in the past few years. PZT

ceramics in thin film form have already been incorporated into various MEMS devices for sensing or actuating purposes, in particular those demanding exceptionally high linearity in response and/or high actuation forces. However, the high levels of thin film stress incorporated in these structures are a serious problem, as they increase both the likelihood of early device failure and the risk of unwanted deformation of the device after release. The only approach to combating these effects available so far, has been stress balancing in which the individual layer stresses and thicknesses are adjusted, so that the null bending moment condition for the equilibrium of the released structure gives zero deformation [1]. This has been practically realized in a number of ways, at either device or wafer level, such as Ar bombardment of the completed device [2] or inclusion of stress compensating layers [3], where the respective adjustments are made by varying ion dose or film thickness- with all such techniques the overall level of thin film stress of course is little changed. In an investigation into the stress in our microstructures using the wafer curvature technique it has been found, in common with other workers [2, 4, 5], that the stress is largely the result of the thermal mismatch between the Si substrate and the various device layers and so cannot be reduced by conventional means but it is also predominantly localized to the layers beneath the PZT. This has led to the proposal of a technique for the elimination of this stress by the removal of the high stressed under layers following the PZT deposition step.

Good quality PZT thin films of uniform thickness can be prepared at relatively low temperatures (~530 ^{o}C– 600^{o}C) using the sol-gel deposition method, provided only that there is a Pt or other template layer underneath to promote crystallization of the perovskite phase [6]. If Pt is used, a barrier layer is also needed, since Pt is not stable in contact with Si at high temperatures and a thermally grown SiO_2 layer is commonly used for this, especially when electrical contact between Pt and Si is not desired. Use of Pt as the template layer for PZT

nucleation gives rise to high mechanical stress in the stack which is mainly attributable to the large mismatch in thermal expansion coefficients between Pt and Si.

The wafer curvature technique has been used to investigate the stress in our PZT/Pt/SiO_2 transducer structures. For these trials the PZT stack was fabricated on top of a 425 μm thick, 4" Si wafer, coated with a 0.2 μm thick thermal oxide. The first step was the room temperature RF magnetron sputtering of a 100 nm thick Pt template layer with underlying 8nm Ti adhesion layer. This was followed by deposition of ten layers of $Pb(Zr_{0.3}Ti_{0.7})O_3$ by a sol-gel method, which gave a total PZT film thickness of 1 μm. X-ray diffraction confirmed that the PZT film was well crystallized with the expected (111) orientation. Finally a 100 nm thick Au layer with thin (8nm) Ti adhesion layer was RF magnetron sputtered for the top electrode. The contribution of the individual layers to the overall stress was calculated from the modified Stoney equation [7] in which the stress in a particular layer, σ_f, is given by:

$$\sigma_f = \frac{E_s}{6(1-\nu_s)}\left(\frac{1}{R}-\frac{1}{R_0}\right)\frac{t_s^2}{t_f} \qquad (1)$$

Where E_s, ν_s are the elastic modulus and the Poisson's ratio of the substrate, t_s and t_f are the substrate and film thickness respectively and R_0 and R are the substrate radii of curvature without (R_0) and with (R) the particular layer present, as measured using a DEKTAK surface profiler.

As PZT crystallization is a high temperature process (530 ^oC- 600 ^oC) alterations in Ti/Pt residual stress have been reported [4, 8-11] due to interactions between the adjacent films and/or annealing out of the as-deposited stress. Process induced changes were investigated by comparing the stresses in the layers as measured during the building of the PZT stack with those measured for the same layers during their sequential removal. A series of wet etches were used for the stripping process.

In the table of results presented in Table I it can be seen that, as deposited, the Au has a high compressive stress which is very close to the value measured on etch back. This would be expected since the wafer did not undergo any high temperature processing between the two steps. In contrast, it appears that the stress in both the PZT and Pt have changed significantly during processing. However, looking more closely at the PZT stress data a high value close to that shown in column 1 was only measured for the first layer of PZT, all subsequent layers had values similar to that in the second column. It is clear, therefore, that only the residual stress in the Ti/Pt bottom electrode had changed during PZT crystallization. This change, from compressive to tensile, is mainly attributed to the annealing out of the original compressive stress and the subsequent introduction of a purely thermal stress due to the large thermal expansion coefficient mismatch between Pt and the Si substrate. The thermal stress which arises in the Pt film during PZT crystallization, ignoring other interactions and assuming bulk values for the film properties, is given by [4]:

$$\sigma_{th} = \frac{E_f}{(1-\nu_f)} \int_{T_{crysr}}^{T_0} (\alpha_f - \alpha_s) dT \qquad (2)$$

Where E_f=170 GPa and ν_f=0.39 are the elastic modulus and Poisson's ratio of bulk Pt and α_f=9x10^{-6} deg^{-1}, α_s=2.5x10^{-6} deg^{-1} are the thermal expansion coefficients of bulk Pt and bulk Si respectively. For T_0=30 ^{o}C, T_{cryst}=530 ^{o}C, Eq.2 gives a thermal stress equal to 0.91 GPa, close to the value of 0.877 GPa obtained experimentally and consistent with previous works [3, 4].

There are other changes that take place during processing, such as Ti diffusion into the Pt as well as formation of TiO_2 [12-14] which since the Ti layer is extremely thin have been assumed to have little effect on the calculated stress. Other values to be noted in Table I are the low tensile stress in the PZT and the relatively high compressive stress in the SiO_2.

The identification of a largely fixed stress in the PZT stack localized in the Pt and (to a lesser extent) SiO_2 layers below the PZT, has led to the proposal of a technique, for the elimination of this stress by the complete removal of the under layers. The idea is to attach the wafer by its top face to a second wafer and to remove the initial substrate and the highly stressed films using dry etching techniques. At this point processing of the device structure can be resumed using low stress bottom electrode and structural layers.

The feasibility of this technique was investigated using 4" wafers containing the same Au/PZT/Pt/SiO_2 layer structure as described earlier. The main steps in the process are illustrated in Figure 1. The attachment of the two wafers was carried out using a recently developed transfer bonding technique [15] the key features of which are: the relatively low bonding temperature, the ability to bond any kind of wafer material, the high tolerance to 3D surface topographies and the wide range of polymers that can be used for the adhesive layer, including benzocyclobutene (BCB) [16] and photoresists such as SU8 and the mr-I 9000 nano-imprint series resist from Microresist Technology GmBH [17] used in the current work. The adhesive was spun onto the wafer (Figure 1(b)) and also onto a second wafer Figure 1(c) with spin speed adjusted to give a nominal thickness of 2.5 μm. Then, using a Karl Suss SB6 substrate bonding tool, the wafers were bonded together (Figure 1(d)) at a chuck pressure of 4 bar and a curing temperature of 200°C for 50 minutes [17].

Figure 1 (a) Ferroelectric stack (b, c) Coating of adhesive on both wafers (d) Adhesive wafer bonding (e) removal of Si, SiO_2 and Pt layers.

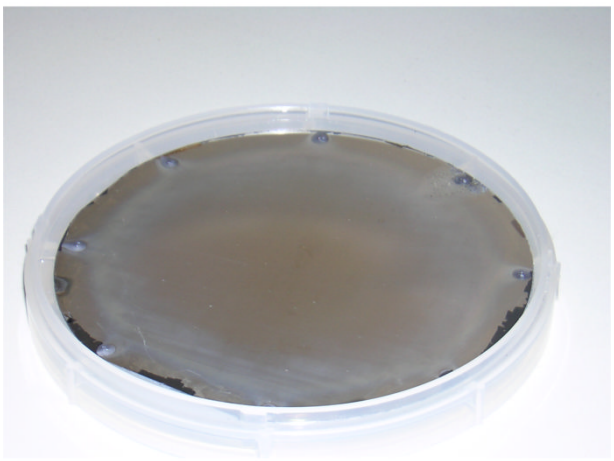

Figure 2 The Pt base layer revealed after Si substrate and SiO_2 layer removal. The black markings at the edges are areas of Si remaining under the supporting fingers needed to clamp the wafer, during the DRIE process.

The SiO_2 and Pt films were then removed using plasma etching to expose the back surface of the PZT: Figure 2 shows the Pt surface, exposed after the removal of the SiO_2 layer and Figure 3 the PZT surface after Pt etch.

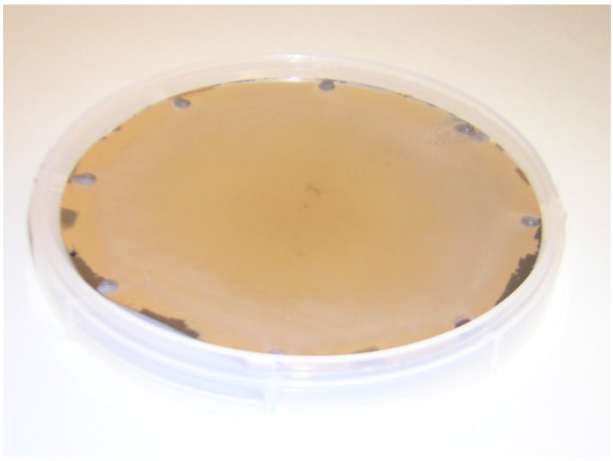

Figure 3 Full view of the base of the back etched PZT supported by the backing wafer.

The effects on the stress in the remaining layers caused by the removal of the silicon substrate were measured by the wafer curvature technique and the results are presented in the

last column of Table I. Once the Pt is released from the substrate the Pt layer is under a low compressive stress while the PZT is again under tensile stress, though less than in the initial stack. This can be explained by assuming that removal of the Si eliminates the force constraining the Pt, dictated by the difference in thermal expansion coefficients (Eq 2), so allowing the Pt film to relax. As expected the stress in the Au top electrode is unaltered.

In order to demonstrate the effectiveness of the Pt layer removal technique in lowering stress and hence distortion in piezoelectric microstructures a comparison has been made of the tip deflections to be expected from two micromachined cantilevers, one composed of the above Au/PZT/Pt/SiO2/Si structure and the other with the Pt, SiO_2 and Si layers removed and replaced by low stress Au and SiN_x for the bottom electrode and structural layers, respectively, giving a Au/PZT/Au/SiN_x structure. The stress values used for the Au, PZT, Pt and SiO_2 were those which had been measured on the real structure during etch back i.e. those given in column 4 of Table I. The SiN_x was assumed to have negligible stress with Young's modulus E=290 GPa and was given the same thickness (10μm) as the Si structural layer: a 10μm beam width was assumed in both cases. The analysis generally followed the treatment by Pulskamp et al.[1] which was based on the well known Bernoulli-Euler beam bending equation:

$$\frac{\dfrac{d^2w}{dx^2}}{\left(1+\left(\dfrac{dw}{dx}\right)^2\right)^{3/2}} = \frac{M(x)}{EI} \tag{3}$$

In Eq. (3), w is the vertical deflection as a function of the distance along the beam, x; M(x) is the total bending moment due to the residual stresses in the films comprising the beam and E and I are the composite Young's modulus and moment of inertia with respect to the beam's width, respectively. In both cases the elastic properties of the films were assumed to be

constant and equal to their bulk values while stress gradients in the films were assumed negligible. The equation was solved numerically using a Runge-Kutta method of fourth order accuracy.

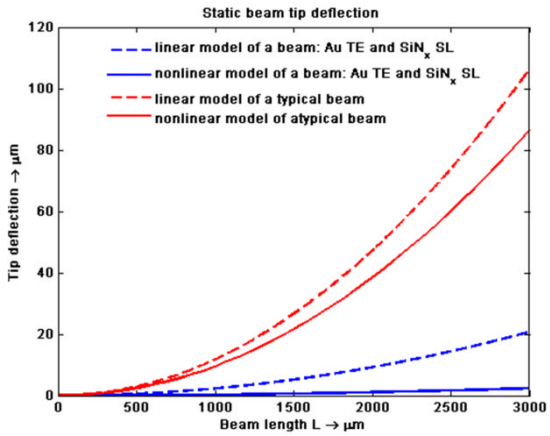

Figure 4 Static tip deflection of a cantilever beam as a function of the beam's length. Red curves correspond to a beam fabricated from a pzt stack on top of a 10 µm thick Si substrate. Blue curves correspond to a beam fabricated from a back etched stack using a SiN_x low stressed 10 µm thick film as the structural layer (SL) and a sputtered Ti/Au film as the top electrode (TE).

The resulting beam tip deflections as a function of beam length are given in Figure 4 which also shows for comparison the result to be expected in the limit of small displacements. In this latter case it is assumed that $(dw/dx)^2$ is small compared to 1 in Eq (3) and so can be ignored thus rendering the equation amenable to analytical solution. It can be seen that the assumption of small displacements is not valid for the full range of beam lengths investigated in the present work but both approximate solutions show clearly the great reduction in beam deformation achievable by replacement of the high stress layers.

This demonstrated ability to remove the Pt and SiO_2 base layers in a PZT stack following PZT deposition is a significant milestone towards achieving truly low stress/low

deformation piezoelectric microstructures. Work is currently underway in applying this processing concept to the fabrication of piezoelectrically actuated RF MEMS switches.

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Table I Experimental stress layer values in the as deposited and etched layers of a typical PZT stack. For comparison the film stresses obtained from back-etching the bonded sample are presented.

Layer	**Thickness (µm)**	**Measured Layer Stresses (GPa)**		
		In the as deposited films	**In the etched layers after stack completion**	**In the etched layers of the bonded stack**
Ti-Au	0.108	-0.310	-0.310	-0.225
PZT	1	0.227	0.054	0.021
TI-Pt	0.108	-0.830	0.877	-0.267
SiO_2	0.2	-	-0.162	-