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180 nm metal gate, high-k dielectric, implant free III-V MOSFETs with transconductance of over 425μS/μm

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Abstract: We report data from 180 nm gate length GaAs n-MOSFETs with drive current ($I_{ds,sat}$) of 386 μA/μm (V_g = V_d = 1.5 V), extrinsic transconductance (g_m) of 426 μS/μm, gate leakage ($J_{g,limit}$) of 44 nA/cm^2, and on resistance (R_{on}) of 1640 Ω.μm. The g_m and R_{on} metrics are the best values reported to date for III-V MOSFETs, and indicates their potential for scaling to deca-nanometre dimensions.

Introduction: Novel device architectures, high-k gate dielectrics, metal gates and high mobility channel materials will be required to continue CMOS device scaling according to Moore's Law and the ITRS [1, 2]. It is now widely accepted that high mobility channel materials are likely to be required beyond the 22 nm node and for this reason, activity has escalated in both Ge-based p-MOSFET and III-V-based n-MOSFET device research [3]. The potential benefits of III-V n-MOSFETs [4] have been explored extensively by Monte Carlo simulations [5], and include significantly higher drive current at lower supply voltage compared with silicon-based devices for a given device geometry. The lack of a device quality III-V semiconductor/insulator interface has, in the past, prevented the exploitation of the high electron mobility of compound semiconductors in MOSFETs [6-8], but recent progress using an in-situ MBE grown $Ga_2O_3/(Ga_xGd_{1-x})_2O_3$ (GGO) stack has demonstrated the

long channel potential of this technology [9-12]. The implant-free flat-band architecture described in [11] uses a modulation doped channel to provide connection between the ohmic contacts and the gate, where enhancement mode (e-mode) operation is achieved through judicious selection of gate metal work-function and doping strategy in a high electron mobility III-V heterostructure.

Layer structure and device fabrication: Material growth was carried out on a 3" semi-insulating GaAs substrate using a dual chamber molecular beam epitaxy (MBE) system by the method detailed in [9]. The III-V heterostructure was grown in one chamber before being transferred under ultra high vacuum to a second chamber for high-κ dielectric deposition. Fig. 1 gives the layer compositions and dimensions of the III-V MOSFET structure. A two-level wrap-around gate design (where the gate encircles the drain) was used to simplify the device process flow, removing the need for isolation. The source-drain separation was 1.65 μm. Both the gate (Pt/Au) and ohmic contacts (Ni/Ge/Au) were defined by direct write e-beam lithography and patterned by the lift-off method. The GGO dielectric was removed by wet chemical etching prior to deposition of the ohmic contacts, which underwent rapid thermal annealing at 430°C for 60 s. Transmission line measurement (TLM) data obtained from process control structures alongside the devices gave a contact resistance (R_c) of 470 Ω.μm and a sheet resistance (R_{sh}) of 433 Ω/sq.

Results: Fig. 2 gives typical output characteristics of the 180 nm gate length devices, the shortest gate length III-V MOSFET thus far reported. These well

behaved devices have R_{on} (which at this device geometry can be used as a first order approximation for parasitic series resistance) of 1640 $\Omega.\mu$m - the lowest value reported to date [13]. For the given device geometry, this is in close agreement with the value calculated from the R_c and R_{sh} values extracted from TLM structures (1650 $\Omega.\mu$m).

Typical transfer characteristics, given in Fig. 3, exhibit a threshold voltage (V_t) of -0.47 V, a maximum drain-source saturation current ($I_{ds,sat}$) of 386 μA/μm, and a peak extrinsic transconductance of 426 μS/μm, - the highest value reported to date [12]. We expect that with relatively minor refinements to the gate metal effective work-function, gate-to-channel separation or doping strategy, a positive V_t and e-mode operation can be achieved. The gate leakage at V_{gs} = V_{ds} = 1.5 V ($J_{g,limit}$) was 44 nA/cm^2.

Fig. 4 compares the extrinsic g_m with previously published data for III-V MOSFETs. This work and [12, 14-17] were carried out on GaAs wafers, but [13] used an InP substrate, allowing the use of a higher indium concentration channel with higher mobility, which should translate into higher drive current and higher transconductance. Despite this, the data presented in this letter represents an increase in g_m of 68% over the previously published best results [12].

Conclusion: In this letter, we have presented data on the shortest gate length III-V MOSFETs realised to date. These devices have the highest g_m (68% improvement on recently achieved results [12]) and lowest R_{on} (34% lower

than previous best result [13]) reported, and demonstrate the potential for scaling III-V MOSFETs to deca-nanometre dimensions.

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Figure captions:

Fig. 1 III-V MOSFET layer structure.

Fig. 2 Output characteristics of a typical 180 nm gate length III-V MOSFET.

Fig. 3 Transfer characteristics of a typical 180 nm gate length III-V MOSFET (V_d = 1.5V).

Fig. 4 Comparison of published III-V MOSFET g_m with values obtained in this work.

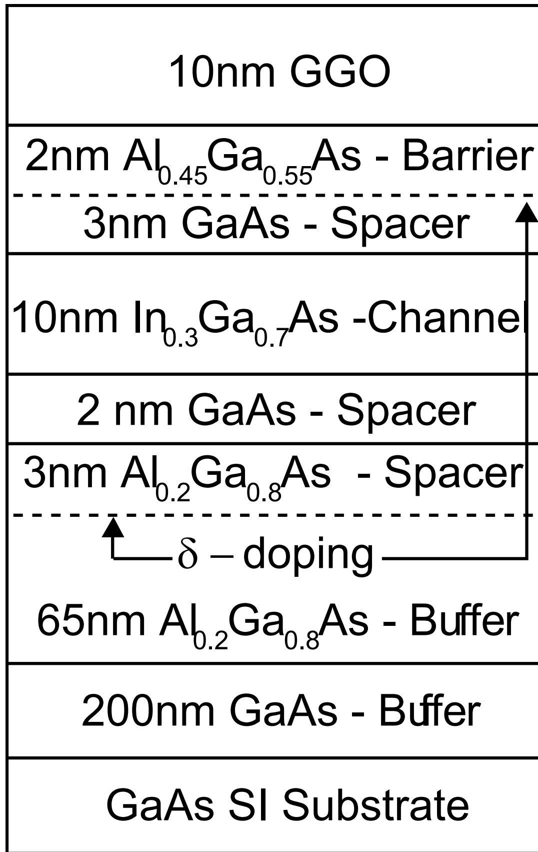

Figure 1

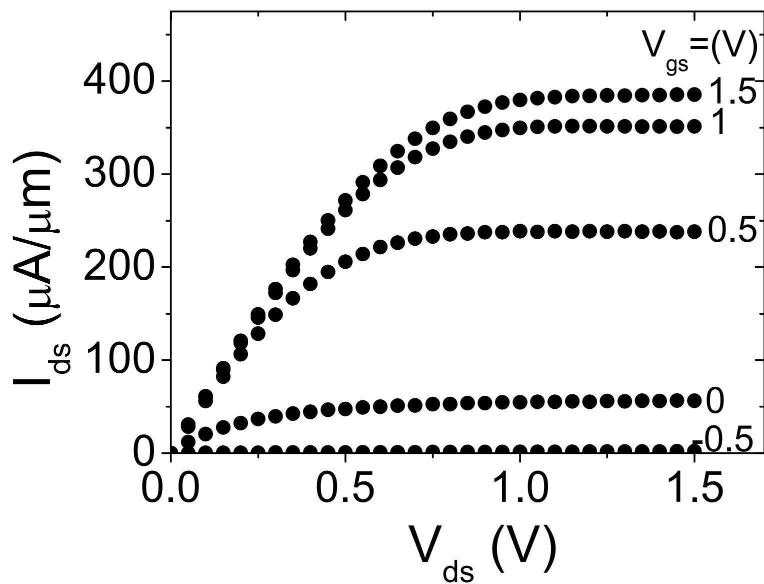

Figure 2

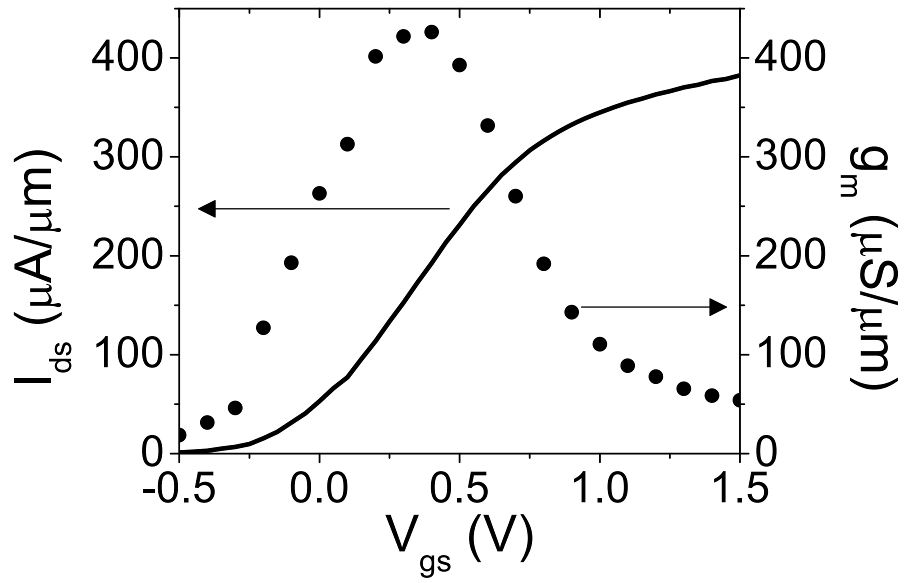

Figure 3

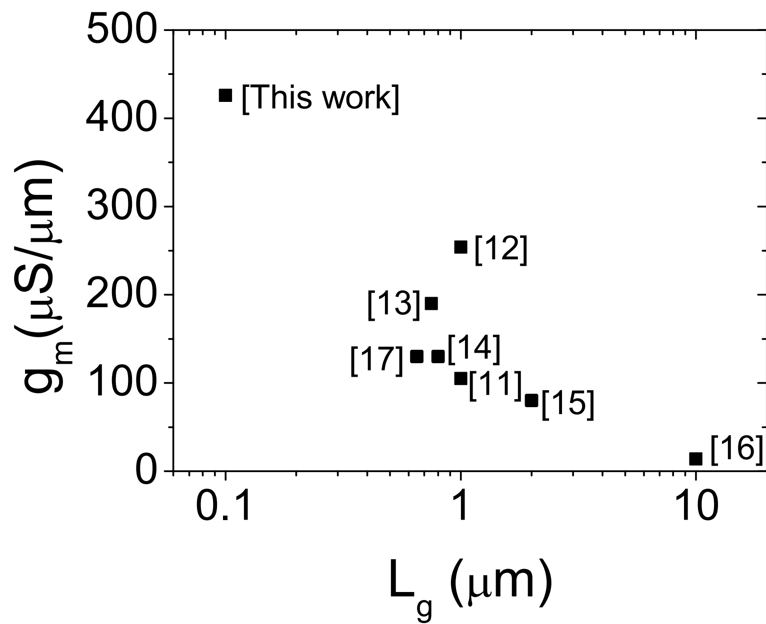

Figure 4

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