1 μm gate length, $In_{0.75}Ga_{0.25}As$ channel, thin body n-MOSFET on InP substrate with transconductance of 737μS/μm.

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Abstract: We report the first demonstration of implant-free, flatband-mode (FB) $In_{0.75}Ga_{0.25}As$ channel n-MOSFETs. These 1μm gate length MOSFETs, fabricated on a structure with average mobility of 7720 cm^2/Vs and sheet carrier concentration of $3.3x10^{12}$ cm^{-2}, utilise a Pt gate, a high-κ dielectric (κ≈20), and a δ-doped InAlAs/InGaAs/InAlAs heterostructure. The devices have a typical maximum drive current ($I_{d,sat}$) of 933μA/μm, extrinsic transconductance (g_m) of 737 μS/μm, gate leakage (I_g) of 40 pA, and on-resistance (R_{on}) of 555 Ω.μm. The g_m and R_{on} figures of merit are the best reported to date for any III-V MOSFET.

Introduction: It is widely accepted that beyond the 22nm technology generation of the International Technology Roadmap for Semiconductors (ITRS), strained silicon may no longer deliver the performance required by the roadmap and that channel materials with better transport properties may be required [1]. Possible alternatives include Ge, GaAs, InGaAs, InAs, InSb, GaN, and perhaps others [2-8]. Recently published results from high performance flatband-mode [9] $In_{0.3}Ga_{0.7}As$ channel enhancement-mode MOSFETs on GaAs substrate conclusively demonstrate that the historical issue of Fermi-level pinning at the GaAs/dielectric interface can be overcome

[10]. Although $In_{0.3}Ga_{0.7}As$ n-channel MOSFETs are well suited to mobile RF applications, technological issues and intrinsic properties limit their ability to challenge aggressively scaled silicon nMOS devices for digital applications. For example, it is extremely demanding to reduce contact resistance to shallow $In_{0.3}Ga_{0.7}As$ 2 dimensional electron gas (2DEG) layers below 300-400 $\Omega.\mu m$, which is far in excess of the total parasitic series source drain resistance (R_{SD}) requirement of 75 $\Omega.\mu m$ set by the ITRS for the 22nm technology generation [1]. In addition, Monte Carlo simulations have shown that $In_{0.3}Ga_{0.7}As$ devices have limited drive current improvement over silicon below a gate length of 15nm, but that significant drive current benefit can be achieved by $In_{0.75}Ga_{0.25}As$ channels due to reduced access resistance, increased source-injection velocity and a very high degree of ballisticity [11]. A further benefit of high indium content structures is the ability to form low resistivity, shallow source/drain contacts. As the indium concentration of InGaAs is increased, the Fermi-level pinning energy of a metal semiconductor contact moves from mid-gap towards the conduction band, reducing the barrier height and hence ohmic contact resistance [12]. For these reasons high indium concentration InGaAs channels are attractive candidates for nMOS devices beyond the 22 nm technology generation.

Layer structure and device fabrication: Material growth was carried out on a 2" semi-insulating InP substrate using a dual chamber system by a method similar to [13]. Fig. 1 gives the layer structure of the III-V MOSFET material, which consisted of the following layers; a 400nm lattice matched $In_{0.52}Al_{0.48}As$ buffer, a $3x10^{12}cm^{-2}$ Si δ - doped plane, a 6 nm $In_{0.52}Al_{0.48}As$ spacer, a 10nm

$In_{0.75}Ga_{0.25}As$ channel, a 2nm $In_{0.52}Al_{0.48}As$ barrier, a 2 monolayer (ML) $In_{0.53}Ga_{0.47}As$ semiconductor surface layer, and a 5nm high-κ metal oxide layer with $\kappa \approx 20$. A TEM cross-section of the layer structure can be seen in Fig. 2. The oxide and barrier layers have an equivalent oxide thickness (EOT) of 1.7 nm. To calculate the capacitance equivalent thickness (CET) the position of the charge in the channel must be considered. The charge centroid moves from the rear of the channel toward the front with increasing positive gate bias, so calculating an accurate CET is complex. As a first order approximation, half the channel thickness can be used to calculate the CET to be 3 nm. Fig. 3 gives a 2 dimensional map of mobility from contactless measurements of a wafer with a similar structure to that used for the devices. The average carrier concentration was $3.3x10^{12}$ cm^{-2} and the average mobility was 7720 cm^2/Vs. This is comparable to earlier reported data on similar layer structures [14].

As detailed in [10] a two-level wrap-around gate design (where the gate encircles the drain) was used to simplify the device process flow, removing the need for isolation. The gate length was 1μm and the source drain separation was 3μm. Both the gate and ohmic contacts were defined by direct write e-beam lithography and patterned by the lift-off method. The dielectric was removed by wet chemical etching prior to deposition of the ohmic contacts, which subsequently underwent rapid thermal annealing.

Results: Transmission line measurement (TLM) structures gave the contact resistance (R_c) and sheet resistance (R_{sh}) to be 78 $\Omega.\mu$m and 195 Ω/sq

respectively, which are the lowest III-V MOSFET parasitic access resistance components reported to date. Using a self-aligned process [15], which reduces the access length from 1μm to 50nm, the total parasitic access resistance (R_{SD}) could be reduced to 165 Ω.μm. This value is equivalent to current Si technology and could be improved to meet the ITRS 22nm target by further optimisation [1].

Fig. 4. gives typical output characteristics of a 1μm gate length device. These devices show excellent drive current ($I_{d,sat}$) of 933μA/μm (V_{ds} = V_{gs} = 2 V) , peak transconductance ($g_{m,max}$) of 737 μS/μm (V_{ds} = 2V, V_{gs} = 0.275 V) and R_{on} of 555 Ω.μm (V_{ds} = 0.05 V, V_{gs} = 2 V). The g_m and R_{on} values are the best reported to date for III-V MOSFETs, and considering the non-optimised layout and relaxed gate length, show the potential of this technology when scaled to the deca-nanometre regime. The electron saturation velocity (ν_{sat}) can be estimated using $I_{dsat} \approx \nu_{sat}*q*n_s$ to be $1.8x10^7$ cm/s, where q is the elementary charge, and n_s the sheet carrier density. This value is considerably greater than that found from $In_{0.3}Ga_{0.7}As$ channels ($1.2x10^7$ cm/s) [16] confirming the improved transport properties of higher indium concentration channels. The difficulties in turning off the transistor are attributed to donor-type traps, mainly located in the lower portion of the band-gap at the semiconductor/oxide interface. In order to achieve a device quality interface, further significant improvements to the semiconductor/oxide interface are required.

Conclusion: We have demonstrated for the first time flatband-mode MOSFETs with high indium content in the channel. The excellent on-state

performance of these 1 μm gate length devices ($I_{d,sat}$ = 933μA/μm, $g_{m,max}$ = 737μS/μm and R_{on} = 555 Ω.μm) indicates the potential of this material system and device architecture for post 22nm technology generation n-MOS solutions.

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Figure captions:

Fig. 1 InP MOSFET layer structure.

Fig. 2 TEM cross section of InP MOSFET material with 15 nm thick oxide layer.

Fig. 3 Contactless mobility map of InP MOSFET wafer (in units of cm^2/Vs)

Fig. 4 Output characteristics of a typical 1 μm gate length InP MOSFET.

5nm Oxide
2 ML $In_{0.53}Ga_{0.47}As$ - Surface
2 nm $In_{0.52}Al_{0.48}As$ - Barrier
10 nm $In_{0.75}Ga_{0.25}As$ - Channel
6 nm $In_{0.52}Al_{0.48}As$ - Spacer
$3x10^{12}cm^{-2}$ δ – doping 400nm $In_{0.52}Al_{0.48}As$ - Buffer
InP SI Substrate

Figure 1

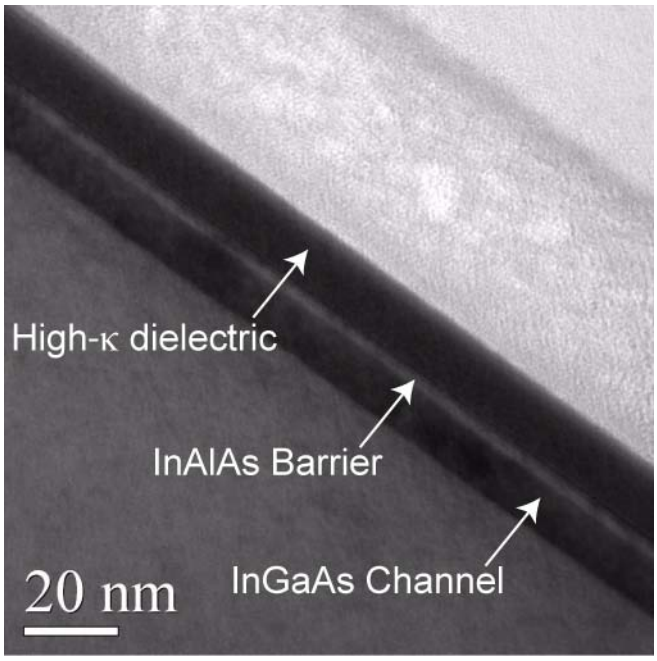

Figure 2

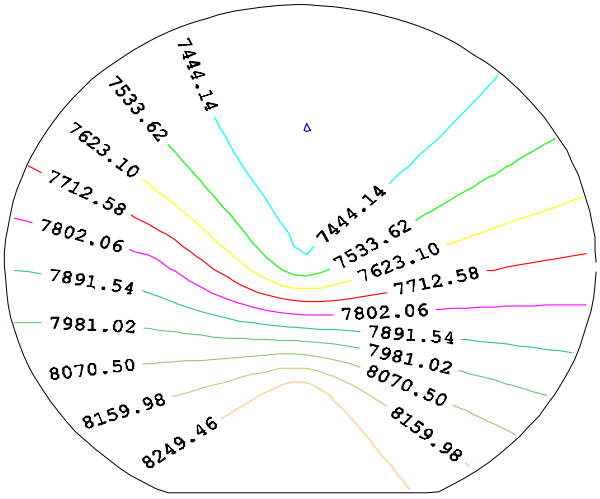

Figure 3

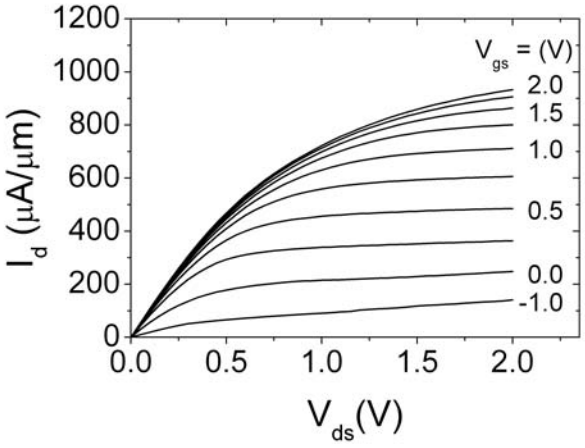

Figure 4

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