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# Very High Performance 50 nm T-gate III-V HEMTs Enabled by Robust Nanofabrication Technologies

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***Abstract* — In this paper, we review a range of nanofabrication techniques which enable the realization of uniform, high yield, high performance 50 nm T-gate III-V High Electron Mobility transistors (HEMTs). These technologies have been applied in the fabrication of a range of lattice matched and pseudomorphic InP HEMTs and GaAs metamorphic HEMTs with functional yields in excess of 95%, threshold voltage uniformity of 5 mV, DC transconductance of up to 1600 mS/mm and $f_T$ of up to 480 GHz. These technologies and device demonstrators are key to enabling a wide range of millimeter-wave imaging and sensing applications beyond 100 GHz, particularly where array-based multi-channel solutions are required.**

***Index Terms* — Nanofabrication, III-V semiconductor devices, millimeter-wave ICs.**

## I. Introduction

The millimeter-wave frequency bands from 30-300 GHz have a number of significant applications including broadband radio communications; high data rate fibre systems; automotive collision warning; concealed weapon detection; passive imaging systems capable of "seeing" through rain, snow and fog; environmental, atmospheric and pollution monitoring systems.

Many of the applications have operating frequencies of around 100 GHz and beyond. A significant percentage of the markets are in the areas of sensing and imaging where receiver sensitivity, determined primarily by the noise performance of the front-end low noise amplifier, where High Electron Mobility Transistors (HEMTs) outperform all other available technologies, is a key performance metric. Finally, there are numerous cases where imaging arrays would be the preferred system solution.

These requirements place huge demands on the active device and sub-system technologies for millimeter-wave applications in terms of inherent bandwidth and noise performance, but also require these parts be available in significant volumes at reasonable cost.

The challenge for the device technologist therefore is to realize a manufacturable, high yield process where significant effort is taken in the complete optimization of the active device technology.

Working at critical dimensions of 50 nm results in the requirement to develop robust nanofabrication technologies with tight tolerances and high reproducibility if high performance devices are to be realized based on modifying the vertical and lateral architectures. Only by having a robust 50 nm critical dimension testbed such as the one described in this paper, can the optimized devices reported here be realized.

## II. 50 nm T-gate Processes

The key to the realization of a robust 50 nm T-gate process for III-V HEMTs is having a large process latitude gate lithography technology and highly controllable gate recess etch strategy.

In the work reported in this paper, all gate definition is by electron beam lithography using a Leica Cambridge EPBG5-HR Beamwriter operated at 100 kV. Significant improvements to device yield and uniformity were achieved by utilizing a beam focusing technique based on a set of structures defined on the substrate, rather on the substrate holder as is more commonly the case. In this way, defocusing due to height errors and sample tilt are minimized.

Two gate resist strategies have been investigated in detail – one based on a PMMA/P(MMA/MAA) bi-layer structure and the other based on a PMMA/LOR/UVIII resist stack. The PMMA/P(MMA/MAA) stack is a simplification of a more widely used tri-layer resist stack. We have found that moving to a bilayer stack results in improved resist thickness uniformity in the source-drain gap of a device, with no reduction in device yield. The latter is a consequence of the sub-100 nm features being realized in this work. Figure 1 shows an SEM cross-section of a typical 50 nm footprint device realized using the bilayer resist approach.

The PMMA/LOR/UVIII resist stack in contrast, has advantages in terms of process latitude offered by using

chemically amplified deep UV resists patterned by electron beam lithography[4].

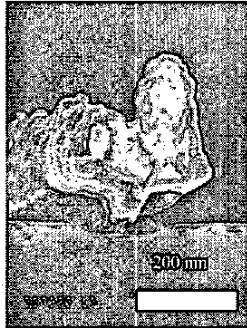


Figure 1 SEM Cross-section of 50 nm T-gate realised using bilayer resist strategy.

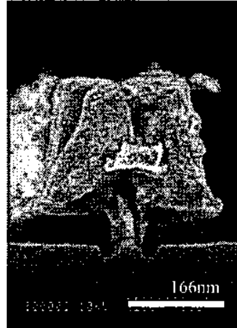


Figure 2 SEM Cross-section of 50 nm T-gate realised using trilayer resist strategy.

Figure 2 shows an SEM cross-section of a typical 50 nm footprint devices realized using this tri-layer approach.

The other key factor in 50 nm footprint T-gate realization is the formation of a gate recess etch. The gate recess etch can be clearly seen in both Figures 1 and 2.

In this work, two gate recess etch approaches, based on wet chemical etching, have been utilized. The first etch is selective to the incorporation of aluminium containing layers in the device vertical architecture. A succinic acid based etch etches InGaAs layers, stopping on any InAlAs layers. Having reached the etch stop layer in the vertical architecture, further etching resulting in a lateral increase in the length of the etch trench, which controls both the breakdown voltage and threshold voltage of the device.

A second approach is to use a non-selective "digital" etching strategy which is based on a 2 step etching method whereby the semiconductor surface is oxidized, followed by removal using an acid etch. Interestingly, we have found that lateral etching control can be achieved in this non-selective approach by varying the composition of the acid etch solution, due to changes in surface wetting.

Figure 3 SEM Image of 70 nm double recessed device

Finally, both selective and non-selective etches can be used to form a "double recess" which becomes more important in optimizing device characteristics as the gate length is reduced below 70 nm. Figure 3 shows an SEM micrograph of a "double recess".

## III. DEVICE RESULTS

### *A. 50 nm GaAs Metamorphic HEMTs using bilayer resist strategy and succinic acid based selective etching*

This family of devices were fabricated on a metamorphic GaAs wafer. The design of the layer structure consisted of a highly n-doped 20nm $In_{0.53}Ga_{0.47}As$ cap, a $In_{0.52}Al_{0.48}As$ barrier layer with a thickness of 8nm and a spacer layer with a thickness of 4nm making the material suitable for the fabrication of scaled 50nm gate length devices. Mesa isolation was performed using a non-selective wet etch, the ohmic contacts were defined using electron beam lithography and metallised using a Ni:Ge:Au metallisation scheme.

The T-shaped gates were formed using a bilayer resist stack. The gate recess was formed using a succinic acid based selective wet etch. The gates were formed by depositing and lifting off Ti:Pt:Au.

The devices were characterised on-wafer using Cascade Microtech V-band probes and an HP4155C parameter analyser. A number of devices were measured across the wafer, the electrical yield was greater than 95%. The threshold voltage of forty devices across the wafer were measured, the histogram of these values is shown in Figure 4, it is seen that the large majority of devices tested had a threshold voltage in the range of –0.425V and –0.475V.

The average threshold voltage of the devices is 0.445V with a standard deviation of 0.005V this is, to the author's knowledge, the most uniform threshold voltage demonstrated for HEMT of this gate length. The average

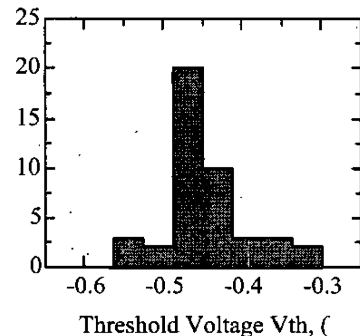


Figure 4 Histogram of Threshold Voltage of forty devices across the wafer.

transconductance was found to be 1169±83mS/mm across the wafer.

### *B 50 nm Non-annealed Ohmic Contact Lattice Matched InP HEMTs*

Non-annealed Ohmic contacts offer the opportunity to minimize the thermal budget of a III-V HEMT process flow which can be important in aggressive scaling where layer thicknesses and dopant plane placement are crucial to device operation. In addition, moving to a non-annealed process flow enables the gate to be defined before the Ohmic contacts, thereby removing the concern about gate resist thickness uniformity in a source drain gap.

The device presented in this section include optimized placement of additional layers of dopant in the vertical architecture to facilitate the formation of non-annealed Ohmic contacts and improve the linearity of the devices, which has impact in complex modulation strategies in advanced wireless communications applications. These devices utilize the tri-layer PMMA/LOR/UVIII resist stack and a double recess processes described above.

DC characterisation indicates excellent performance with an extrinsic transconductance $g_m$ of 1600mS/mm across a wide gate voltage range (Figure 5). High drive current was also observed including $I_{ds}$ of 900mA/mm at 1.2V $V_{ds}$ and zero gate bias. Multi-bias S-parameter measurements and equivalent circuit extraction then yielded de-embedded RF performance figures of 430GHz for $f_T$ (Figure 6).

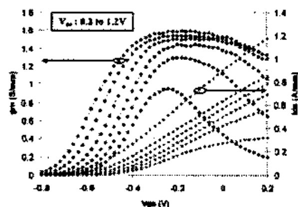

Figure 5 – Transconductance plot for 50 nm lattice matched InP HEMT

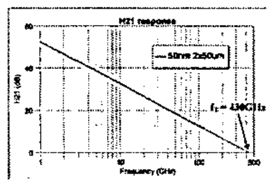

Figure 5 – h21 plot for 50 nm lattice matched InP HEMT

### *C 50 nm pseudomorphic InP HEMTs*

By moving to higher indium channel concentrations, in particular pseudomorphic InP HEMTs with 70% indium channel concentration, the device $f_T$ can be further enhanced.

Using either "digital" or succinic acid based gate recess etching, high performance, high yield (85%) 50µm gate width 50nm T-gate InP HEMTs with gm of 1150ms/mm and Idss of 600mA/mm have been fabricated using the trilayer resist stack. As shown in Figure 7, an $f_T$ of up to 480 GHz, the highest for any device at this technology node has been achieved. In addition, these devices have up to 12 dB gain at 94 GHz, making them ideal for the millimeter-wave applications mentioned earlier.

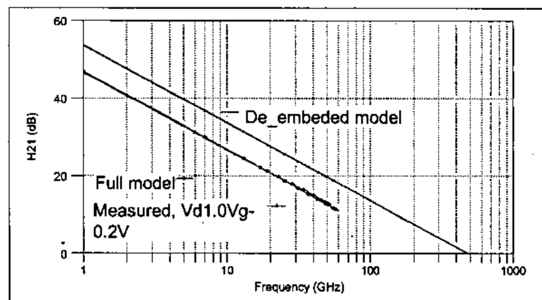


Figure 7 – h21 plot for 50 nm pseudomorphic InP HEMT with $f_T$ of 480 GHz

## IV. CONCLUSION

The robust nanofabrication technology described in this paper is key to the demonstration of the wide range of high performance 50 nm III-V HEMT data presented here. The device characteristics demonstrate very high yield and uniformity with excellent DC and RF performance metrics.

All the above are required to realize high specification millimeter-wave sensing and imaging integrated circuits, particularly if array-based systems requiring large volumes of components are required.

## ACKNOWLEDGEMENT

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