Enhancement Mode n-MOSFET with High-κ Dielectric On GaAs Substrate

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Challenges faced by Silicon CMOS technology, as device scaling reaches physical limits, have prompted the proposal of solutions based on compound semiconductor channels in the recent ITRS Roadmap for Semiconductors 2006. The key drawback of compound semiconductors like GaAs has been the lack of a suitable surface passivating dielectric that could yield a good quality electrical interface between the oxide and the semiconductor.

Here we report MOS heterostructures grown by molecular beam epitaxy on III-V substrates, employing a high-κ dielectric stack ($\kappa \approx 20$) comprised of gallium oxide and gadolinium gallium oxide. Mobilities exceeding 12,000 and 6,000 cm^2/Vs, for sheet carrier concentration n_s of about $2.5x10^{12}$ cm^{-2} were measured on MOSFET structures on InP and GaAs substrates, respectively. These structures were designed for enhancement mode operation and include a 10 nm thick strained $In_xGa_{1-x}As$ channel layer with In mole fraction x of 0.3 and 0.75 on GaAs and InP substrates, respectively. Fig. 1 shows the heterostructure on GaAs substrate and its corresponding TEM image.

n-MOSFETs with a gate length of 1 μm and a source-drain spacing of 3 μm were fabricated on the heterostructure shown in Fig. 1. Fig. 2 shows the I-V characteristics of the 1 μm x 100 μm device. The drain current at 2V gate bias was measured to be in excess of 400 mA/mm. A threshold voltage of 0.27 V, transconductance of 428 mS/mm and on-resistance of 2 ohm-mm were also measured. The output conductance was measured to be 10 mS/mm. Fig. 3 shows a comparison of the transconductance measured on our fabricated devices as compared to g_m values reported for similar devices, over a period of thirty years.

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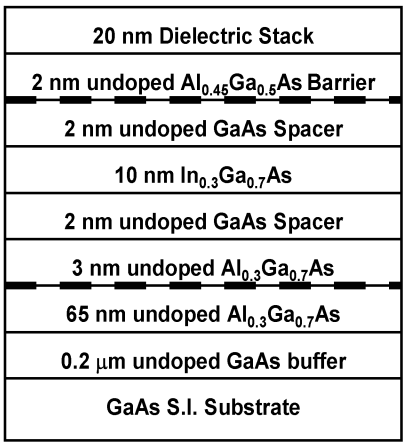
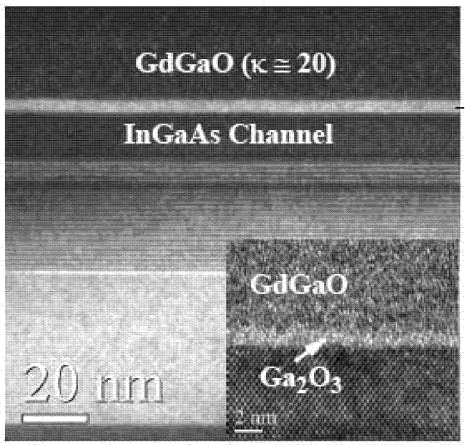
Figures



(a)



(b)

Fig. 1. (a) n-MOSFET layer structure on GaAs substrate (b) TEM image of n-MOSFET layer structure on GaAs Substrate

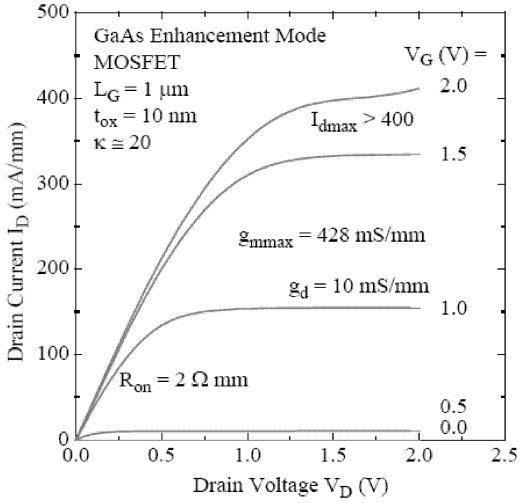


Fig. 2

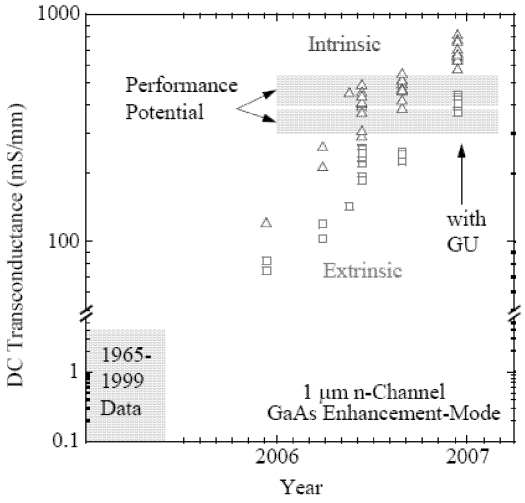


Fig. 3

Fig. 2. ID-VD of 1 μm x 100 μm n-MOSFET on GaAs substrate

Fig. 3. Comparison of g_m from this work with prior data. The range of expected intrinsic and extrinsic performance potential of our 1 μm MOSFETs is also shown.