Monte Carlo Simulations of High-Performance Implant Free $In_{0.3}Ga_{0.7}As$ Nano-MOSFETs for Low-Power CMOS Applications

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***Abstract*—The potential performance of implant free heterostructure $In_{0.3}Ga_{0.7}As$ channel MOSFETs with gate lengths of 30, 20, and 15 nm is investigated using state-of-the-art Monte Carlo (MC) device simulations. The simulations are carefully calibrated against the electron mobility and sheet density measured on fabricated III-V MOSFET structures with a high-κ dielectric. The MC simulations show that the 30 nm gate length implant free MOSFET can deliver a drive current of 2174 μA/μm at 0.7 V supply voltage. The drive current increases to 2542 μA/μm in the 20 nm gate length device, saturating at 2535 μA/μm in the 15 nm gate length one. When quantum confinement corrections are included into MC simulations, they have a negligible effect on the drive current in the 30 and 20 nm gate length transistors but lower the 15 nm gate length device drive current at 0.7 V supply voltage by 10%. When compared to equivalent Si based MOSFETs, the implant free heterostructure MOSFETs can deliver a very high performance at low supply voltage, making them suitable for low-power high-performance CMOS applications.**

***Index Terms*—InGaAs nano-MOSFETs, implant free, high performance, Monte Carlo simulation.**

I. Introduction

HIGH-MOBILITY channel materials are expected to play an important role in high-performance CMOS transistors near and beyond the end of the current ITRS edition [1]. The favored channel material for p-channel devices is Ge [2]. However, the experimentally observed electron mobility in a n-channel Ge device is unsatisfactory [3]. Therefore, the attention is shifting towards the introduction of compound semiconductors to boost the performance of the n-channel device [4], [5]. The recent development of a suitable high-κ gate dielectric for GaAs with a low interface state density [6], [7] has brought the prospects for manufacturable III-V MOSFETs closer to reality [8]. Previous Monte Carlo (MC) simulation studies have shown that 80 nm gate length $In_{0.2}Ga_{0.8}As$ MOSFETs with a conventional surface-channel architecture could outperform by more than a factor of two the equivalent Si and strained Si counterparts [9], [10]. However, when the conventional $In_{0.2}Ga_{0.8}As$ MOSFETs are scaled down to 35 nm, the performance improvement margin shrinks [9], [11].

The introduction of high-mobility III-V materials in MOSFETs requires new device concepts which can benefit from the high channel mobility with scaling. These new device concepts have to be based on a thin body architecture due to its superior electrostatic integrity and higher channel mobility resulting from low-dimensional transport [12], [13]. The design and particularly the vertical device architecture have to be optimized with respect to the channel material and its orientation bearing in mind that at small channel thicknesses the mobility is degraded due to enhanced scattering of carriers with confined phonons [14]. One such recently proposed new device concept which does not require implanted source/drain regions and extensions is the enhancement mode implant free MOSFET [15], [16] illustrated in Fig. 1. The implant free design can take full advantage of the high injection velocity into the channel which is inherent to III-V materials. The band-to-band tunnelling which seriously affects devices with implanted source/drain regions is expected to be highly reduced due to the small channel thickness and the wide bandgap materials surrounding the channel. In this work, using state-of-the-art ensemble Monte Carlo (MC) device simulations, we have studied the potential performance of n-type implant free $In_{0.3}Ga_{0.7}As$ channel MOSFETs with a high-κ gate dielectric scaled to gate lengths of 30, 20, and 15 nm. The simulation study is based on careful calibration against room temperature electron mobility and sheet carrier density measurements performed using gated Hall structures fabricated on relevant $In_{0.3}Ga_{0.7}As$ channel material with a high-κ gate dielectric. The I_D-V_G characteristics obtained from MC simulations demonstrate the excellent performance and the good scalability of the implant free device architecture.

II. Monte Carlo Simulation Approach

The reported simulations of scaled implant free $In_{0.3}Ga_{0.7}As$ MOSFETs have been carried out using our ensemble MC compound semiconductor device simulator MC/MOS described in detail elsewhere [10], [17]. The MC module includes electron scattering with polar optical phonons, inter- and intravalley optical phonons, nonpolar optical phonons, acoustic phonons, and ionized impurities. Alloy scattering and the impact of

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A color version of Fig. 1 is available online at http://ieeexplore.ieee.org.

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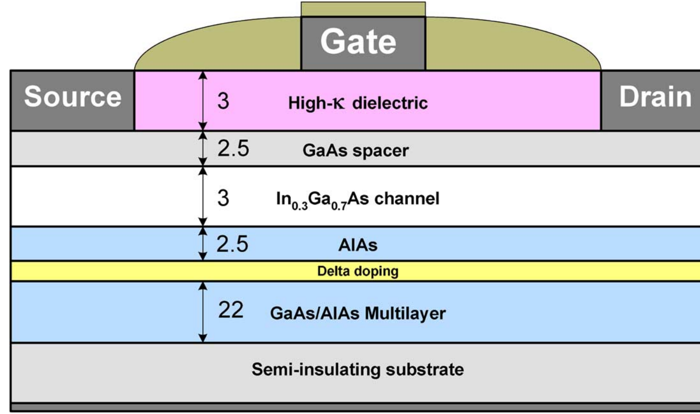

Fig. 1. Cross-section of the 30 nm gate length implant free $In_{0.3}Ga_{0.7}As$ MOSFET considered in MC device simulations.

strain on the bandgap, electron effective mass, optical phonon deformation potential, and optical phonon energy in the InGaAs channel are also included in our simulations [17]. In the past, the MC device simulator was used extensively to study and design high electron mobility transistors (HEMTs) and has been carefully calibrated against measured *I–V* characteristics of fabricated 120 nm gate length pseudomorphic HEMT [17] with an $In_{0.2}Ga_{0.8}As$ channel. It was also used to study the electron transport in a 120 nm double doped InGaAs/InAlAs lattice matched HEMT showing an excellent agreement with the measured *I–V* characteristics of conventional and self-aligned devices [18]. Recently, the simulator has been also calibrated against the measured characteristics of a 50 nm gate length InP HEMT with a high indium content ($In_{0.7}Ga_{0.3}As$) channel [19]. This confirms the validity of the transport model embedded in the simulator in describing highly nonequilibrium electron transport in aggressively scaled ultrafast devices with a high-mobility channel.

The simulator MC/MOS has been enhanced by including quantum confinement effects. The quantum corrections are incorporated adopting a relatively simple effective quantum potential (EQP) approach which is easy to implement into MC simulations [20]. The classical potential P at every position in real space $\mathbf{r}$ is convoluted with a Gaussian distribution, G, in order to obtain an EQP, P_{eff}, using the relation [20]

$$P_{\text{eff}}(\mathbf{r}) = \int d\mathbf{r}' P(\mathbf{r}+\mathbf{r}')G(\mathbf{r}'),$$
$$G(\mathbf{x}) = \frac{1}{a\sqrt{2\pi}} \exp\left(-\frac{x^2}{2a^2}\right) \tag{1}$$

where a is a smoothing parameter. The resulting EQP is then used to propagate MC particles. The values of a were obtained by matching the results of a self-consistent one-dimensional (1-D) Poisson–Schrödinger solution of the relevant layer structures in the subthreshold region [9] leading to $a = 1.3, 0.9$, and 0.75 nm for the 30, 20, and 15 nm gate length implant free MOSFETs, respectively.

The EQP approach mimics a shift of the lowest subband in the quantum wells relevant to transport and the shape of the electron distribution [20]. Therefore, it shifts the electron density centroid away from the semiconductor and dielectric interfaces thus correctly changing the threshold voltage and decreasing the

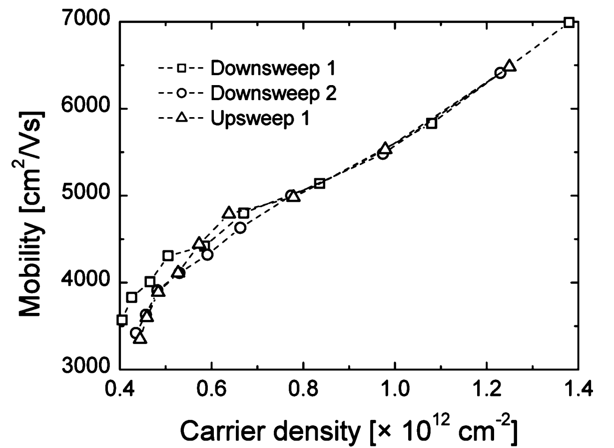

Fig. 2. Measured room temperature electron mobility vs electron carrier concentration of gated Hall Bar structures for gate biases in the range 0–0.8 V.

gate-to-channel capacitances. These effects, in concert, reduce the saturation current [9], [21].

III. Electron Mobility and Sheet Density

The electron drift mobility obtained from the MC simulations has been verified against room temperature mobility measurements of an implant-free $In_{0.3}Ga_{0.7}As$ MOSFET layer structure performed on gated Hall structures. The sheet carrier density obtained from these measurements was used to calibrate the active δ-doping concentration in the device heterostructure. The Pt/Au gated Hall bars were 12 μm wide with a spacing between adjacent arms of 40 μm. A magnetic field of 0.58 T was used in the Hall measurements. Fig. 2 illustrates the dependence of the electron mobility on carrier concentration in the channel for gate biases in the range of 0–0.8 V. The figure contains three traces: 1) for the gate voltage swept up from 0 V to +0.8 V labelled "upsweep"; 2) for the gate voltage swept down from +0.8 V to 0 V labelled "downsweep 1"; and 3) for the gate voltage swept down from +0.8 V to 0 V one week after the initial measurement labelled "downsweep 2."

The measured Hall mobilities were in the range of 3000–6000 cm^2/Vs which is an order of magnitude higher than the mobilities typically measured in Si channels [22]. In addition, for the bias range explored, the mobility increases with carrier concentration up to values of at least 1.4×10^{12} cm^{-2}. This suggests that as the carriers in the device channel

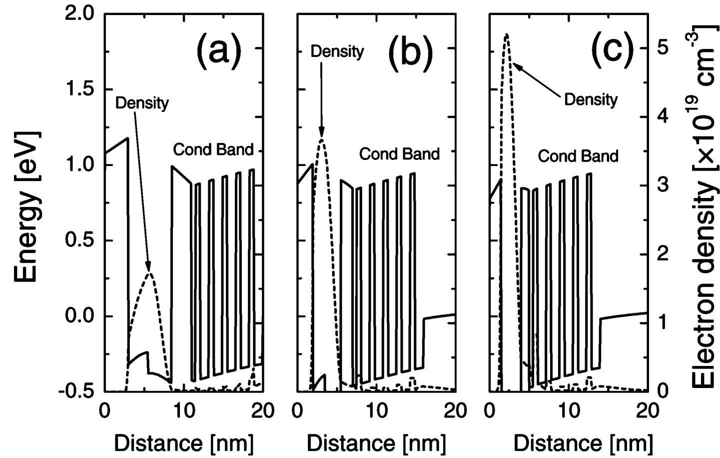

Fig. 3. Conduction band and electron density in the (a) 30; (b) 20; and (c) 15 nm implant free MOSFETs at V_G-V_T = 0.8 V.

are pulled towards the interface between the InGaAs channel and the upper GaAs barrier layer with increasingly positive applied gate bias, there is likely to be a reduction in ionized impurity scattering due to a combination of increased spatial separation from the δ-doped layer and enhanced screening due to increasing channel electron concentration. The monotonic increase of mobility with carrier concentration also suggests that, in this bias range, the transport properties of the channel are not being influenced significantly by any interface roughness scattering from the gate dielectric/GaAs spacer interface. Finally, the data of Fig. 2 indicate that the mobility measurements are repeatable. The lack of significant hysteresis between the up and down sweeps suggests only modest trapping effects due to DX centres from the δ-doped plane.

IV. InGaAs Implant-Free MOSFETs

The layout of the simulated implant free $In_{0.3}Ga_{0.7}As$ MOSFET with a gate length of 30 nm including the vertical layer structure grown on a semi-insulating substrate is illustrated in Fig. 1. The high-κ dielectric is assumed to be $Ga_2O_3/(Gd_xGa_{1-x})_2O_3$ with a dielectric constant of 20 [23]. In order to maintain the electrostatic integrity in the 30, 20, and 15 nm gate length transistors, the oxide thickness is scaled to 3, 2, and 1.5 nm and the $In_{0.3}Ga_{0.7}As$ channel thickness is scaled to 3, 2, and 1.5 nm, respectively. The channel thickness is still sufficiently large to not reduce electron transport significantly due to electron interaction with confined phonons (a considerable increase in the electron-phonon scattering rate is reported for GaAs/AlAs quantum wells below a thickness of 1.5 nm [24]). All layer thicknesses of the scaled layer structures are summarized in Table I. The active δ-doping concentration is kept the same in each of the scaled transistor. The threshold voltage is adjusted by selecting a gate metal with an appropriate workfunction. The selection process for a particular scaled device may be assisted by adjusting the δ-doping concentration and subband engineering (by varying channel thickness and material composition in the channel and surrounding layers). Finally, we would like to stress that the predicted performance of all implant free InGaAs MOSFETs corresponds to that of intrinsic devices which means that the impact of the external contact resistances is neglected.

TABLE I
Layer Dimensions for the Implant Free InGaAs MOSFETs Scaled With Respect to Given Gate Lengths

	Gate length [nm]		
Thickness of [nm]	30	20	15
High-κ dielectric	3	2	1.5
GaAs spacer	2.5	1.5	1
$In_{0.3}Ga_{0.7}As$ channel	3	2	1.5
AlAs doping spacer	2.5	1.5	1
δ-doping	0.5	0.5	0.5
GaAs/AlAs multilayer	22	22	22
$Al_{0.3}Ga_{0.7}As$ buffer	400	400	400

Fig. 3 shows the conduction band profile and electron density distribution obtained from the 1-D self-consistent solution of the Poisson-Schrödinger equations. The peak of the electron density steadily increases as the layer heterostructure is scaled from a gate length of 30 nm to 20 and 15 nm, respectively. In addition, the electron sheet density as a function of applied gate bias also increases with the scaling as shown in Fig. 4 where both results obtained from 1-D Poisson and Poisson-Schrödinger simulations are plotted.

Fig. 5 shows the drain current I_D as a function of the difference between the gate voltage V_G and the threshold voltage V_T for the 30 nm gate length implant free $In_{0.3}Ga_{0.7}As$ MOSFET at a low drain bias of 0.1 V and two high drain biases of 0.7 and 1.0 V. Source and drain contacts have been considered to be self-aligned with 30 nm source-to-gate and gate-to-drain separations. The work function of the gate contact is assumed to be adjusted for a threshold voltage of 0.0 V. The drain current delivered by the 30 nm gate length implant free MOSFET is 2174 μA/μm at a supply voltage of 0.7 V and 2753 μA/μm at a supply voltage of 1.0 V. This intrinsic on-current at 1.0 V overdrive is approximately 170% larger than the current reported for a 30 nm effective gate length Si MOSFET ($I_{\rm on} = 1020$ μA/μm at V_G-V_T = 1.0 V and V_D = 1.2 V) obtained using MC simulations [25] and 100% larger than the current in a strained $\langle 100 \rangle$ Si MOSFET ($I_{\rm on} = 1380$ μA/μm at V_G-V_T = 1.0 V and V_D = 1.2 V) [25]. Since the heavily doped regions are not present in the device source/drain, the *I–V* characteristics obtained from MC simulations exhibit very low noise below

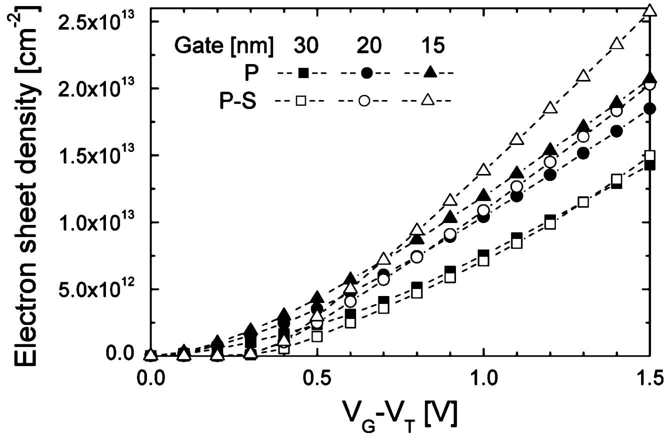

Fig. 4. Electron sheet density versus difference between the applied gate bias and threshold voltage for the 30, 20, and 15 nm gate length MOSFETs. Results obtained using both Poisson (P) and Poisson–Schrödinger (P-S) solutions are shown.

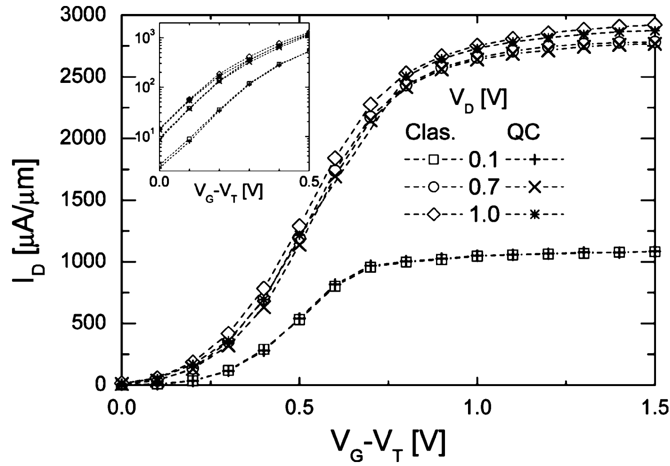

Fig. 5. I_D-(V_G-V_T) characteristics of the 30 nm gate length $In_{0.3}Ga_{0.7}As$ implant free MOSFET at indicated drain voltages V_D versus the difference between applied gate bias V_G and threshold voltage V_T. Both results from simulations including (QC) and excluding (Clas.) quantum confinement corrections are shown. The inset illustrates the subthreshold slope of the transistor.

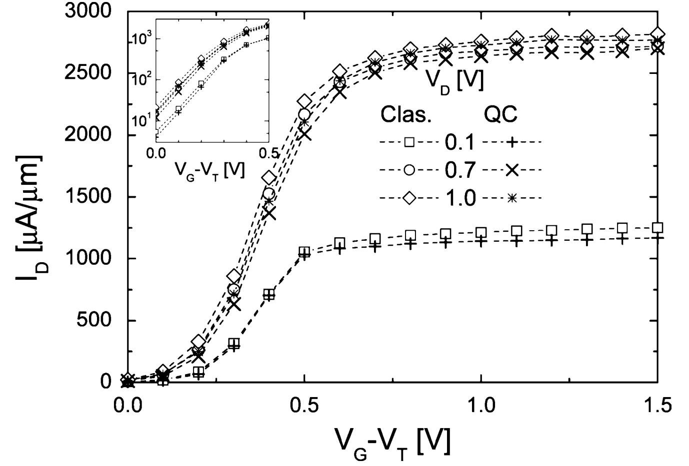

Fig. 6. I_D-(V_G-V_T) characteristics of the 20 nm gate length $In_{0.3}Ga_{0.7}As$ implant free MOSFET at indicated drain voltages as a function of the difference between applied gate bias and threshold voltage. The classical simulations (Clas.) have not used quantum confinement corrections while simulations with quantum confinement corrections (QC) used the EQP approach. The inset shows the device subthreshold slope.

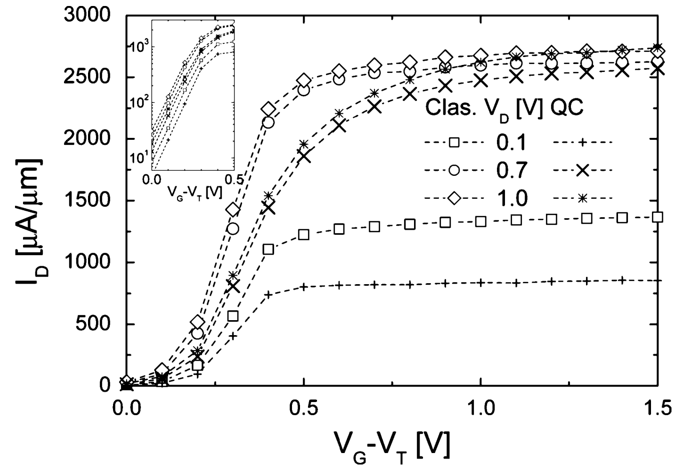

Fig. 7. I_D-(V_G-V_T) characteristics of the 15 nm gate length $In_{0.3}Ga_{0.7}As$ implant free MOSFET at various drain voltages as a function of V_G-V_T. The simulations without and with quantum confinement corrections are shown. The subthreshold swing of the device can be seen in the inset with the drain current on logarithmic scale.

the threshold voltage. Therefore, it was possible to extract subthreshold slopes from the MC simulations. For the 30 nm gate length implant free MOSFETs, we have obtained a subthreshold slope of 167 mV/dec as shown in the inset of Fig. 5. This subthreshold slope is comparable with the figures of equivalent Si MOSFETs reported in [26]. The moderate slope is the consequence of: 1) the low density of states typical for III-V materials [27] and 2) the buried channel of the implant free MOSFET with an additional GaAs spacer between the channel and the oxide layer. Therefore, the gate control over the channel transport is weakened not just by the low density of states in the InGaAs channel but also by the increased separation between the gate and the channel.

When the implant free transistor with the $In_{0.3}Ga_{0.7}As$ channel is scaled down to a gate length of 20 nm, the drain current increases by approximately 17% to 2542 μA/μm at 0.7 V supply voltage as illustrated in Fig. 6. However, the drain current delivered at a supply voltage of 1.0 V remains nearly the same as in the 30 nm transistor, 2757 μA/μm. This on-current is still 150% larger than the current reported for the 20 nm effective gate length Si MOSFET and 83% larger than for the equivalent strained $\langle 100 \rangle$ Si MOSFET [25]. The subthreshold slope is slightly lowered to 161 mV/dec. Finally, further scaling of the implant free MOSFET to 15 nm gate length does not provide more benefit at 0.7 and 1.0 V supply voltages in terms of drive current. As shown in Fig. 7, the drive current delivered by the 15 nm gate length implant free MOSFET stays at 2535 μA/μm at 0.7 V supply voltage and even slightly decreases to 2694 μA/μm at 1.0 V supply voltage (without quantum confinement correction). When compared to the equivalent Si based MOSFETs with implanted source/drain regions, an increase of 135% and 95% is still observed against the 15 nm effective gate length Si and strained $\langle 100 \rangle$ Si MOSFETs, respectively [25]. The subthreshold slope of the 15 nm gate length implant free $In_{0.3}Ga_{0.7}As$ transistor lowers to 155 mV/dec. However, if the supply voltage is further dropped to 0.5 V (it should be noted that the drain current at $V_D = 0.5$ V is not shown on Figs. 5, 6, and 7), the 15 nm transistor

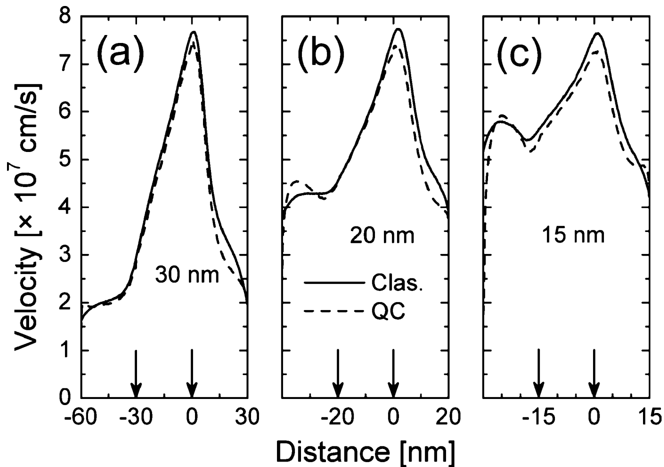

Fig. 8. Average electron velocity along the $In_{0.3}Ga_{0.7}As$ channel of scaled implant free MOSFETs with indicated gate lengths at V_G-$V_T = 0.5$ V and $V_D = 0.7$ V. The beginning of the gate is depicted by arrows while the end of the gate is always set at zero. The simulations excluding and including the quantum confinement corrections are shown for comparison.

outperforms the 20 and 30 nm counterparts delivering a drive current of 2330 μA/μm as compared to a drive current of 2050 and 1090 μA/μm, respectively.

The quantum confinement corrections incorporated into MC/MOS simulator via the EQP formalism have the most pronounced impact on the I_D-(V_G-V_T) characteristics of the 15 nm gate length device. When quantum corrections are included into MC simulations of the 30 nm gate length implant free MOSFET, their impact on the drain current as a function of V_G-V_T is very small (less than 2%). The impact of quantum confinement corrections is more pronounced at 0.1 V drain voltage decreasing the drain current by approximately 7%. The effect of quantum corrections is also negligible in the 20 nm gate length device. The relatively small impact of the quantum corrections on the 30 and 20 nm gate length transistors is related to the fact that the EQP neither includes electron intersubband transitions nor low-dimensional screening. Finally, quantum confinement corrections start to play a significant role in the 15 nm gate length device. The corresponding drive current drops by nearly 40% at $V_D = 0.1$ V. The drain current as a function of V_G-V_T at high drain voltages of 0.7 and 1.0 V is also affected although the impact on the saturation drain current is less pronounced. The drain current at 0.5 and 0.7 V overdrives delivered by the 15 nm gate length transistor is reduced to 1820 and 2265 μA/μm, respectively. The failure of the 15 nm gate length implant free MOSFET to improve further its performance can be attributed to the aggressively scaled channel thickness which reduces carrier density due to lifting of the lowest ground state to a relatively high energy when compared to the Fermi energy.

The average electron velocity along the $In_{0.3}Ga_{0.7}As$ channel of the implant free transistors with gate lengths of 30, 20, and 15 nm is plotted in Fig. 8 at V_G-$V_T = 0.5$ V. The behavior of the average velocity along the channel indicates that electrons are accelerated immediately after the injection into the channel. When the electrons enter the region under the gate where a very high fringing electric field is present, the electron transport becomes highly nonequilibrium. Their peak velocity of more than 7.6×10^7 cm/s appears close to the drain side of the gate. After that, the electrons start quickly to lose energy due to enhanced phonon scattering and frequent transitions to the upper L and X valleys with larger electron effective masses. Their average velocity quickly drops but remains still relatively large when entering the drain contact. The peak average electron velocity does not change much with device scaling when the quantum corrections are excluded from MC simulations. When the quantum corrections are included, the peak of the average electron velocity decreases from 7.45×10^7 cm/s in the 30 nm gate length transistor to 7.38×10^7 and 7.26×10^7 cm/s in the 20 and 15 nm gate length devices, respectively. The peak velocity reduction by approximately 4% as compared to the simulations excluding quantum confinement corrections indicates that the gate control is less effective due to an increase in the separation between the metal gate and the centroid of the electron density in the InGaAs channel. On the other hand, the injection velocity and the velocity at which electrons enter the drain contact progressively increases with scaling. A clear drop in the average electron velocity in the 15 nm gate length transistor can be observed when electrons enter the region under the gate. This reduction is caused by a very high fringing electric field at the source end of the gate which facilitates electron transfer to the upper valleys. This sudden drop of the electron velocity along the channel of the 15 nm gate length transistor might be one of the factors causing stagnation in its performance when compared to the 20 nm gate length device.

V. Conclusion

Using state-of-the-art MC device simulations we have predicted that implant free heterostructure MOSFETs with $In_{0.3}Ga_{0.7}As$ channels can deliver a very high drive current at 0.7 V supply voltage. The MC device simulations have been verified by comparing the simulated electron mobility and sheet density against measured data obtained from relevant epitaxial layer structures. Based on the layer structure design used in measurements, the implant free MOSFETs have been scaled to gate lengths of 30, 20, and 15 nm.

The excellent drive current of implant free heterostructure transistors at very low supply voltages makes them excellent candidates for very low-power, high-performance CMOS applications. Furthermore, the drive currents in this low drain bias regime show excellent scalability except in the 15 nm gate length transistor. Assuming that a 0.0 V threshold can be achieved by appropriate choice of the gate workfunction, the 30 nm implant free $In_{0.3}Ga_{0.7}As$ MOSFET delivers a drive current of 2174 μA/μm at 0.7 V supply voltage, increasing to 2542 μA/μm at the 20 nm, but saturating to 2535 μA/μm at the 15 nm channel length. However, if the quantum confinement corrections are included into MC simulations, the drive current of the 15 nm transistor drops to 2265 μA/μm while the drive currents of the 20 and 30 nm gate length counterparts are not significantly affected.

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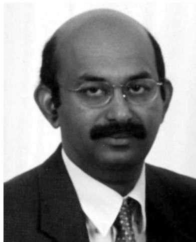

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