50-nm Self-Aligned and "Standard" T-gate InP pHEMT Comparison: The Influence of Parasitics on Performance at the 50-nm Node

David A. J. Moran, Helen McLelland, Khaled Elgaid, Griogair Whyte, Colin R. Stanley, and Iain Thayne

***Abstract*—Continued research into the development of III–V high-electron mobility transistors (HEMTs), specifically the minimization of the device gate length, has yielded the fastest performance reported for any three terminal devices to date. In addition, more recent research has begun to focus on reducing the parasitic device elements such as access resistance and gate fringing capacitance, which become crucial for short gate length device performance maximization. Adopting a self-aligned T-gate architecture is one method used to reduce parasitic device access resistance, but at the cost of increasing parasitic gate fringing capacitances. As the device gate length is then reduced, the benefits of the self-aligned gate process come into question, as at these ultrashort-gate dimensions, the magnitude of the static fringing capacitances will have a greater impact on performance. To better understand the influence of these issues on the dc and RF performance of short gate length InP pHEMTs, the authors present a comparison between $In_{0.7}Ga_{0.3}As$ channel 50-nm self-aligned and "standard" T-gate devices. Figures of merit for these devices include transconductance greater than 1.9 S/mm, drive current in the range 1.4 A/mm, and f_T up to 490 GHz. Simulation of the parasitic capacitances associated with the self-aligned gate structure then leads a discussion concerning the realistic benefits of incorporating the self-aligned gate process into a sub-50-nm HEMT system.**

***Index Terms*—Access resistance, fringing capacitance, InP, MODFETs, nonalloyed, parasitics, self-aligned gate.**

I. Introduction

THE CONTINUOUS demand for increased performance from modern microwave/millimeter integrated circuit (MMIC) applications has led to extensive research dedicated to the development of the transistor technology inherent to MMIC design. The high-electron mobility transistor (HEMT) provides a route to the realization of high-frequency response and low-noise applications and hence plays a lead role in modern MMIC technology. By adopting a III–V based material system and, in particular, by including a high-indium-content InGaAs channel layer, higher electron saturation velocities result in higher frequency performance. This combined with advanced lithography techniques, allowing the minimization of the device gate length and reducing carrier transit times, also improves the device frequency performance dramatically. These techniques have led to the realization of the fastest three terminal devices to date [1].

Beyond the material and lithographic issues that require attention for high-speed device realization, extrinsic device elements such as access resistance and fringing capacitance are found to impact on device performance, restricting the potential performance of the short gate length system [2]. Also, for shorter gate length devices ($\sim$100 nm and below), effort must be made to appropriately scale the device geometry to ensure efficient operation and reduce short-channel effects [3]. More recently, this has been combined with intricate fabrication techniques in an effort to suppress the deteriorative effects of parasitic elements on the well-scaled short gate length system [4].

The self-aligned T-gate process, successfully adopted into a short gate length HEMT process by Nguyen *et al.* [5], allows for a reduction in the device access resistance by reducing the physical separation between the metallized ohmic contacts and the intrinsic gate region. Conversely, by bringing the ohmic contacts in closer proximity to the gate, the magnitude of the gate fringing capacitance will be larger with the self-aligned architecture than with a "standard" device geometry. A tradeoff therefore exists with the self-aligned gate process dependent on the increased performance achieved through access resistance reduction, compared with the deterioration in performance that results from increased fringing capacitance for a particular gate-length node.

For this paper, the characteristics and performance of 50-nm self-aligned and standard T-gate InP pHEMT devices are compared. Both of these device types are realized using our InP double delta doped (DDD) material and nonalloyed ohmic contact methodologies that provide very high device performance and good device uniformity at the 50-nm node [6].

II. Methodology

The material layers used for this paper are presented in Fig. 1. These layers resemble a typical InP pHEMT layer structure, with semi-insulating InP substrate, $In_{0.52}Al_{0.48}As$ buffer layer, pseudomorphic 15-nm $In_{0.7}Ga_{0.3}As$ channel, 15-nm $In_{0.52}Al_{0.48}As$ barrier, and a 20-nm bulk-doped $In_{0.53}Ga_{0.47}As$ cap layer. Instead of a single delta doping layer positioned within the barrier layer, however, an additional layer is added closer to the barrier/cap layer interface. As has been described elsewhere, this double doping technique allows the use of a nonalloyed ohmic process by tailoring the conduction band

Manuscript received March 22, 2006; revised June 14, 2006. This work was supported in part by the Engineering and Physical Sciences Research Council (EPSRC) and in part by Bookham Technology Ltd., Caswell. The review of this paper was arranged by Editor Y. Chan.

The authors are with the Nanoelectronics Research Centre, University of Glasgow, G12 8QQ Glasgow, U.K. (e-mail: d.moran@elec.gla.ca.uk).

Digital Object Identifier 10.1109/TED.2006.885674

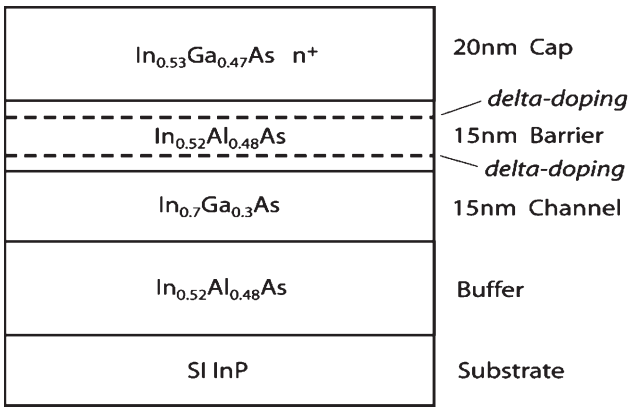


Fig. 1. DDD InP pHEMT material layer structure.

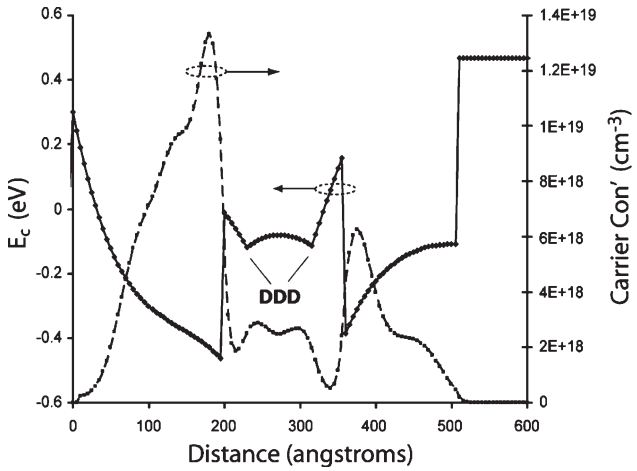


Fig. 2. Conduction edge band trend (left axis) and carrier concentration profile (right axis) through active material layers from left to right showing cap, barrier, channel, and buffer layers. The nonalloyed contact forms a Schottky barrier height of ∼0.3 eV above the Fermi level (0 eV) to the doped InGaAs cap, and the DDD strategy acts to minimize the potential barrier formed by the barrier layer.

profile vertically through the structure and hence favoring better vertical conduction through the layers [7], [8]. This is demonstrated in Fig. 2, which shows the conduction band and carrier concentration profiles through the active layers as generated by Poisson–Schrödinger simulation. The effect of introducing the additional doping is seen in the reduction of the effective potential barrier at the cap and barrier layer interface. Similarly, the region below the gate, i.e., after recess etching, is simulated and is shown in Fig. 3. In this instance, the gate-to-channel separation is taken to be 11 nm, i.e., below the upper delta doping layer, as this represents the double-gate recess etch developed for this technology, which is described later.

We have found the use of this nonalloyed process to be superior to a standard alloyed ohmic process for several reasons. First, the route by which conduction occurs between the ohmic metal and intrinsic gate region is less restricted with the DDD layer structures. Ordinarily for single doped layers, the alloying or thermal treatment of the ohmic metal provides a low-resistance route across the Schottky barrier at the cap/metal interface and the barrier layer of the material into the device channel. Current is then predominantly limited to flow vertically through this region and horizontally through

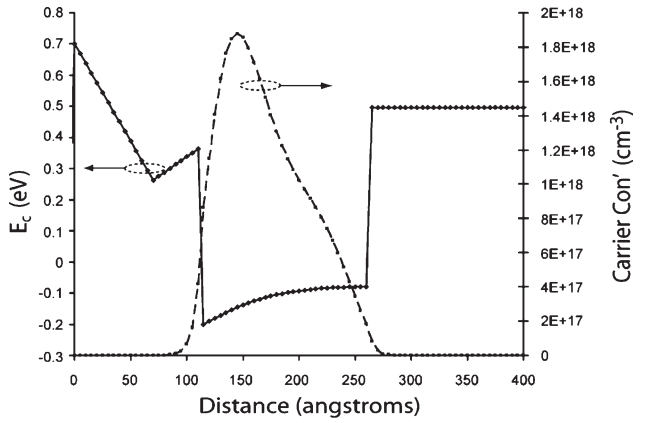


Fig. 3. Conduction band (left axis) and carrier concentration (right axis) profiles through device gate region, i.e., after the double-gate recess etch. The gate metal makes contact with the barrier layer to the left of the plot, forming a Schottky barrier of ∼0.7 eV above the Fermi level.

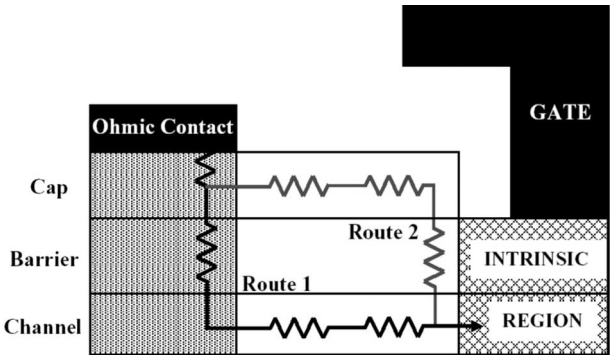


Fig. 4. Current paths through access resistance region to intrinsic device. Route 1 denotes current path with typical alloyed ohmic device, whereas Route 2 denotes path available with nonalloyed device.

the channel to the gate region, as the intrinsic impedance of the barrier layer of the material is large. As this impedance is minimized uniformly with the DDD material, transport will occur through the cap, barrier, and channel layers to the intrinsic gate region, substantially reducing the access resistance. These processes are illustrated in Fig. 4.

Various other nonalloyed ohmic processes have also been demonstrated [9]–[11], which often rely on more exotic or highly doped cap layers to promote better vertical conduction through the layers. By introducing additional doping to the barrier, however, we benefit from higher carrier concentration around the gate region for higher drive current and transconductance plus a suppression in the kink effect often observed in short gate length InP HEMT technology [12].

In addition to device performance, uniformity of device operation is also improved with the use of the nonalloyed ohmic process [13]. By avoiding thermal treatment of the ohmic contacts, the gate level is performed prior to the ohmic level without concern for thermal degradation of the Schottky gate contact. For ultrashort gate length lithography, it becomes essential to pattern the gate profile onto a planar surface as opposed to between the ohmic contacts, thus avoiding potential resist thickness fluctuations that result from spinning gate resist between the ohmic contacts. As the self-aligned gate process relies on the ability to define the gate prior to the ohmic

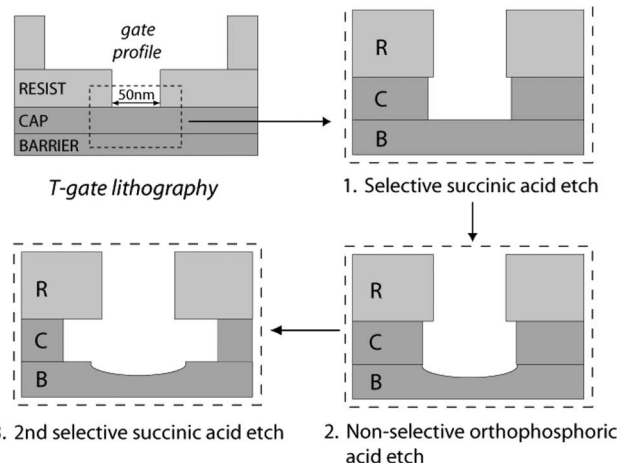


Fig. 5. Following writing of the 50-nm T-gate profile into the resist stack, a selective succinic acid etch step removes the cap layer to the barrier layer with minimized resist undercut. A nonselective orthophosphoric etch widens this initial etch into both cap and barrier layers. The final succinic acid etch widens the cap etch, creating the double recess profile.

contacts, the use of a nonalloyed ohmic process is ideal for the investigation into self-aligned gate device operation.

III. Device Fabrication

Characterization of the DDD pHEMT material by the Van der Pauw method indicated values of 10 000 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ for electron mobility and 2.4×10^{12} cm^{-2} for the sheet carrier concentration after selective removal of the InGaAs cap layer by succinic acid etching. Nonalloyed ohmic contact resistance values were extracted using a recessed transmission-line matrix (TLM) technique, indicating an extremely low contact resistance figure of $0.06\pm0.01\ \Omega\cdot\mathrm{mm}$.

The 50-nm self-aligned and standard T-gate devices were fabricated using the following generic process flow, with only the physical separation between the gate and ohmic contacts differing for each.

Electron beam (e-beam) lithography using a Leica EBPG5-HR 100 e-beam tool was used to lithographically define each level of the fabrication process. Following definition of the marker level to allow alignment of further levels, the active geometry of each device was defined through orthophosphoric acid-based mesa etching. The T-gate level was then patterned on the planar isolated mesa using a PMMA/LOR/UVIII resist stack written at 100 keV. A double-gate recess process combining succinic and orthophosphoric acid-based etch steps was developed and tailored for the material at the 50-nm node. The details of this process are shown in Fig. 5. Following recess etching, the gate profile was metallized with Ti:Pt:Au onto the etched surface of the InAlAs barrier layer. A scanning electron microscope (SEM) cross-sectional image of the resultant 50-nm gate and double recess is given in Fig. 6. Following gate-level definition, a thin (45 nm) Au:Ge:Ni-based ohmic metallization was deposited to form the nonalloyed ohmic contacts. For the self-aligned devices, the ohmic metal was deposited across the gate, forming the source and drain contacts at a separation defined by the head of the gate ($\sim$300 nm). For the standard device, the ohmic contact separation was set to 1.6 μm to

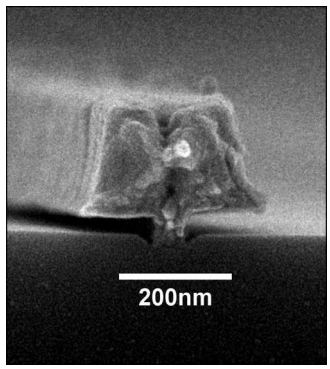


Fig. 6. SEM cross section of metallized 50-nm T-gate within double-gate recess.

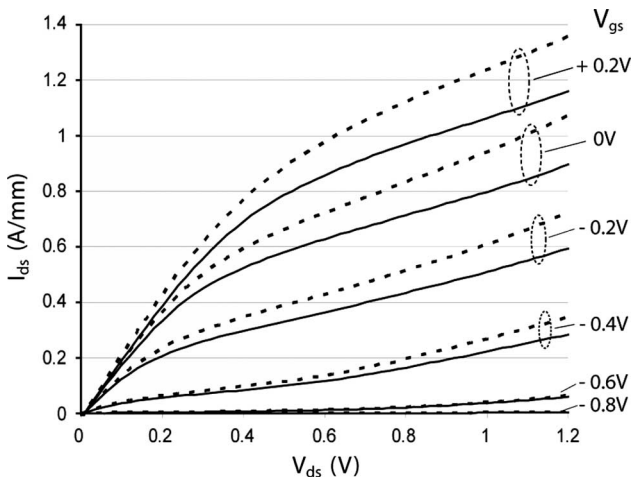


Fig. 7. Self-aligned (broken line) and standard (continuous line) device output characteristics, i.e., I_{ds} versus V_{ds} for fixed V_{gs}.

emulate our typical device geometry. Finally, NiCr:Au coplanar waveguide bond pads were defined to allow on-wafer device characterization.

IV. Device Characterization

DC characterization of the completed 50-nm self-aligned and standard devices was performed using an Agilent 4155 semiconductor parameter analyzer (SPA). The output response of both device types is given in Fig. 7, with the extrinsic transconductance response for each shown in Fig. 8. Extremely high drive current is observed for both types of device, with the self-aligned exhibiting an increase of $\sim$15% over the standard with an I_{ds} close to 1.4 A/mm at a gate bias of $+0.2$ V. Both devices, however, demonstrate a similar threshold voltage of -0.68 V V_{gs}. In addition, little kink is observed in the output characteristics for either device, which we attribute to a high carrier concentration within the vicinity of the gate as a result of using the DDD material. The self-aligned device is also found to outperform the standard when comparing the transconductance curves for each. A peak g_m of 1.6 S/mm is measured for the standard device, compared to an extremely high figure of more than 1.9 S/mm for the self-aligned device, corresponding to an increase of $\sim$19% in g_m by moving to a self-aligned gate structure.

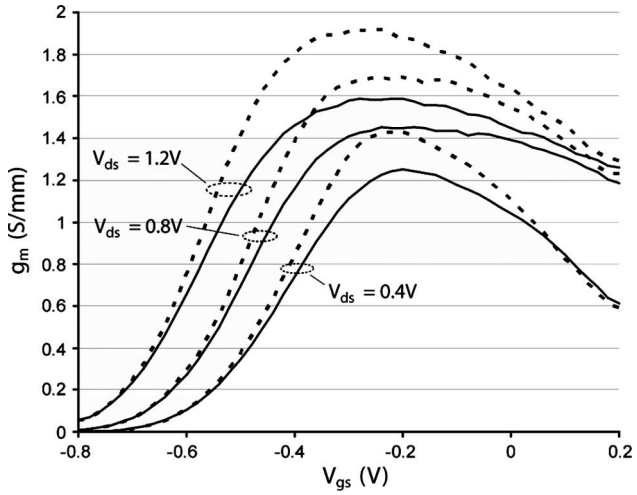


Fig. 8. Self-aligned (broken line) and standard (continuous line) device extrinsic transconductance characteristics, i.e., g_m versus $V_{\rm gs}$ for fixed $V_{\rm ds}$.

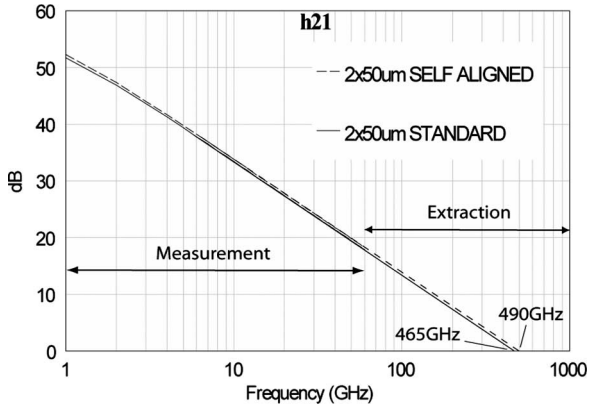


Fig. 9. H21 measurement and extraction for self-aligned (broken line) and standard (continuous line) 2×50 μm width devices.

RF device characterization was performed through S-parameter data extraction from 24 MHz to 60 GHz using Picoprobe high-frequency probes and an Aritsu 360B vector network analyzer. Biasing of the two-finger 50-μm-wide devices was performed using the Agilent SPA. Linear extraction of the deembedded H21 device response at a decay rate of 20 dB/dec produced a cutoff frequency figure f_T for each device type (Fig. 9). These included an f_T figure of 465 GHz for the standard device and 490 GHz for the self-aligned. Again, increased performance is observed with the self-aligned gate architecture.

V. Discussion

Unsurprisingly, superior dc performance is observed with the self-aligned gate structure over that for the standard device due to reduced voltage drop across the device access regions. This appears to be equally beneficial when comparing the increase in drive current and transconductance for the two device types, whereas both exhibit similar threshold voltage. Measurement of the total access resistance for each using a recessed TLM technique indicated a normalized total resistance of 0.27 and 0.15 $\Omega \cdot$ mm for the standard and self-aligned devices, respectively, i.e., a reduction of 0.06 $\Omega \cdot$ mm in both the source and drain resistances. Thus, the total access resistance between ohmic contact and gate region is approximately halved under these conditions using the self-aligned structure. Avalanche breakdown of the self-aligned device is exacerbated, however, due to the increased field concentration through the device as a result of reduced source–gate–drain separation. This produced an on-state breakdown voltage of 1.3 V $V_{\rm ds}$ for the self-aligned device compared to 1.6 V $V_{\rm ds}$ for the standard. Comparison between the gate leakage current for the two device types across the bias ranges associated with peak transconductances, i.e., $V_{\rm ds}$ up to 1.2 V and $V_{\rm gs}$ to -0.5 V, is presented in Fig. 10. The gate current, observed to be slightly larger with the self-aligned device and although entering the milliamperes per millimeter range at larger bias, does not demonstrate any sudden increase and remains a small fraction of the drain current (0.1% to 0.2%), suggesting no onset of impact ionization within this bias range.

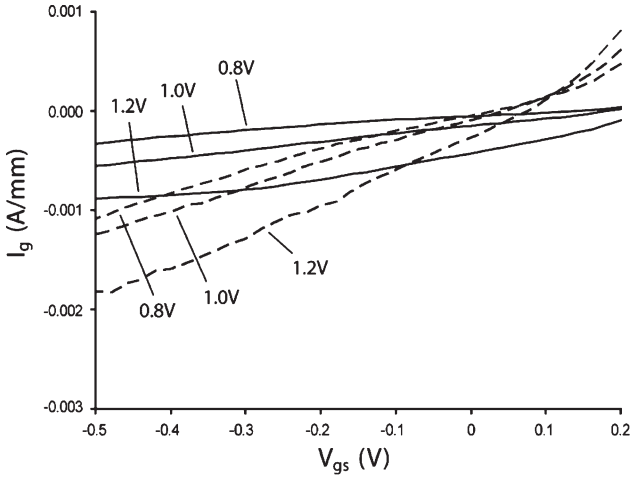


Fig. 10. Gate current versus gate bias for self-aligned (broken line) and standard (continuous line) devices at drain bias steps of 0.8, 1, and 1.2 V.

Although the self-aligned process provides a significant increase in dc device performance, the benefits are not as pronounced when comparing the f_T performance for the two types of device. The approximately 5% increase seen in f_T, although significant, does not correspond to the expected increase when comparing the dc transconductances for the two devices, i.e., 1600 mS/mm and more than 1900 mS/mm. The suppression in the expected self-aligned device performance is therefore arguably due to the increase in parasitic fringing capacitance as a result of forming the ohmic contacts within close proximity to the gate, as otherwise the two types of device are identical. This is corroborated on inspection of the parasitic capacitance elements of the equivalent circuit device models. For the standard device, gate-to-source and gate-to-drain fringing capacitances are extracted to be 50 and 24 fF/mm, respectively. These are compared with those for the self-aligned of 72 fF/mm for gate-to-source capacitance and 34 fF/mm for gate-to-drain capacitance. These values represent an increase in gate-to-source fringing capacitance of 44% and in gate-to-drain fringing capacitance of 42% between standard and self-aligned gate devices.

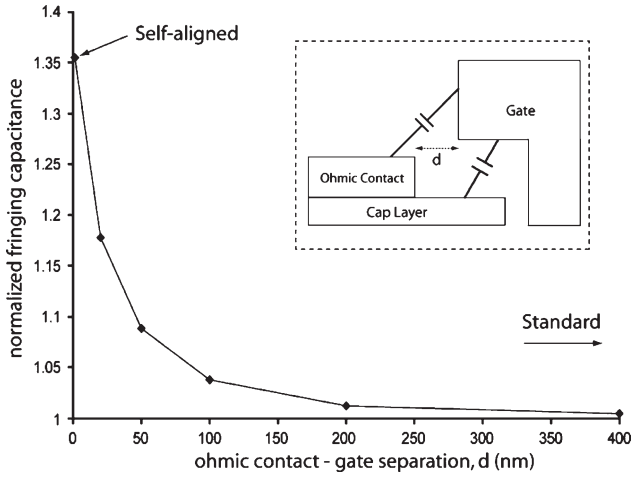


Fig. 11. Simulated parasitic gate capacitance between gate and ohmic contact/cap layer for varied gate–ohmic contact separation d. Capacitance values are normalized to that simulated for $d = \infty$, i.e., between cap layer and gate.

To better estimate the increase in gate fringing capacitance as a function of ohmic contact and T-gate separation, three-dimensional capacitance simulation of the structure treating the gate as one electrode and the cap/ohmic as the other was performed using Fastcap2 software [14]. The geometry of the simulated structure was chosen to best emulate the source side of our 50-nm T-gate devices, i.e., a vertical ohmic contact to T-gate head separation of 15 nm with a 45-nm-thick ohmic contact and a 20-nm-deep, 30-nm-long recess etch (Fig. 11). The aim of this simulation was not to calculate discreet values for the fringing capacitances for a given device geometry, but rather to better understand the trend in the increase in such capacitance as a function of ohmic contact–gate separation. The results of this simulation are shown in Fig. 11. The simulated capacitance is shown normalized to that for a structure with an infinite gate to ohmic contact separation, i.e., that solely between the gate and doped cap layer in the absence of an ohmic contact. As the ohmic contact is brought closer to the gate, the additional fringing capacitance remains insignificant until at a separation of 100 nm, an increase of approximately 4% is observed. As the separation is reduced below 100 nm, more electric field lines begin to terminate on the ohmic contact, leading to higher capacitance until at a separation of 0 nm, i.e., that for the self-aligned gate structure, an increase of $\sim$36% is observed. Although this simulation considers only the effective capacitance through the air between gate and ohmic contact, we find considerable agreement with the increase in fringing capacitance extracted from our equivalent standard and self-aligned circuit data, i.e., an increase of $\sim$42% to 44%.

Although we have observed significant RF performance enhancement by adopting a self-aligned gate architecture at the 50-nm node, the potential performance increase when considering a shorter gate length device becomes questionable. As the intrinsic gate capacitance is reduced with the gate length, the magnitude of these fringing capacitances will arguably not scale with this reduction. Indeed, the use of ultrashort gate length processes often relies on a dielectric support layer between the gate and ohmic contacts/cap layer, leading to enhanced fringing capacitance due to the higher dielectric support material. Our simulation has suggested, however, that the majority of the increase in fringing capacitance will occur mainly with the ohmic contact within the 100-nm range from the gate. To maximize the performance of such an ultrashort gate length device, therefore, the ohmic contact with proper alignment could be situated just beyond this range, reducing the access resistance without introducing a substantial increase in gate fringing capacitance.

VI. Conclusion

By adopting a self-aligned T-gate process in conjunction with our nonalloyed ohmic process, 50-nm self-aligned and standard gate length devices have been fabricated and characterized. The significant performance improvement observed from reducing the proximity of the ohmic contacts to the gate has been demonstrated for a 50-nm gate length, with self-aligned gate devices exhibiting extremely high dc g_m of more than 1900 mS/mm and an f_T in the range of 490 GHz. Moreover, the slightly reduced RF performance compared to that expected for the self-aligned device is arguably due to the increase in parasitic fringing capacitance inherent to the device architecture. We conclude that for sub-50-nm gate lengths, high accuracy alignment of the ohmic contacts would result in the optimization of access resistance and gate fringing capacitance, leading to a maximization of the device RF performance.

Acknowledgment

The authors would like to thank the various members of the Ultrafast Systems Group and Nanoelectronics Research Centre who contributed to this research, as well as J. Davies for various discussions.

References

[1] Y. Yamashita, A. Endoh, K. Shinohara, M. Higashiwaki, K. Hikosaka, T. Mimura, S. Hiyamizu, and T. Matsui, "Pseudomorphic $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As$ HEMTs with an ultrahigh f_T of 562 GHz," *IEEE Electron Device Lett.*, vol. 22, no. 8, pp. 367–369, 2001.

[2] P. J. Tasker and B. Hughes, "Importance of source and drain resistance to the maximum f_T of millimeter-wave MODEFET's," *IEEE Electron Device Lett.*, vol. 10, no. 7, pp. 291–293, Jul. 1989.

[3] K. Kalna, S. Roy, A. Asenov, K. Elgaid, and I. Thayne, "Scaling of pseudomorphic high electron. Mobility transistors to decanano dimensions," *Solid State Electron*, vol. 46, no. 5, pp. 631–638, May 2002.

[4] H. Matsuzaki, T. Maruyama, M. Tokumitsu, and T. Enoki, "Laterally scaled-down tiered-edge-shaped ohmic structure of InP-based HEMTs for 2-S/mm g_m and 500-GHz f_T," in *IEDM Tech. Dig.*, Washington, DC, 2005, pp. 775–778.

[5] L. D. B. Nguyen, A. S. Brown, M. A. Thompson, and L. M. Jelloian, "50-nm self-aligned-gate pseudomorphic AlInAs/GaInAs high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 39, no. 9, pp. 2007–2014, Sep. 1992.

[6] D. A. J. Moran, E. Boyd, K. Elgaid, H. McLelland, C. R. Stanley, and I. G. Thayne, "50 nm T-gate lattice-matched InP HEMTs with f_T of 430 GHz using a non-annealed ohmic contact process," in *Proc. GAAS, Eur. Microw. Week*, Amsterdam, The Netherlands, 2004.

[7] D. A. J. Moran, K. Kalna, E. Boyd, F. McEwan, H. McLelland, L. L. Zhuang, C. R. Stanley, A. Asenov, and I. Thayne, "Self-aligned 0.12 mm T-gate $In_{.53}Ga_{.47}As/In_{.52}Al_{.48}As$ HEMT technology utilising a non-annealed ohmic contact strategy," in *Proc. ESSDERC*, Estoril, Portugal, pp. 315–318.

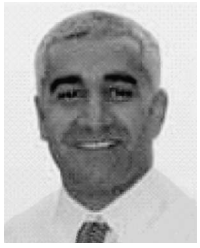
[8] S. Kraus, H. Heiss, D. Xu, M. Sexl, G. Bsohm, G. Trankle, and G. Weimann, "InGaAs/InAlAs HEMTs with extremely low source and drain resistances," *Electron. Lett.*, vol. 32, no. 17, pp. 1619–1621, Aug. 1996.

[9] K. J. Chen, T. Enoki, K. Maezawa, K. Arai, and M. Yamamoto, "High-performance InP-based enhancement-mode HEMTs using non-alloyed ohmic contacts and Pt-based buried-gate technologies," *IEEE Trans. Electron Devices*, vol. 43, no. 2, pp. 252–257, Feb. 1996.
[10] S. Chen, C. Lin, W. Lan, S. Tu, and C. Peng, "Characteristics of nonalloyed pseudomorphic high electron mobility transistors using InAs/In_xGa_{1-x}As $(x = 1 - 0)$/Al_yGa_{1-y}As $(y = 0-0.3)$ contact structures," *Jpn. J. Appl. Phys.*, vol. 36, no. 6A, pp. 3443–3447, Jun. 1997.
[11] K. Shinohara, Y. Yamashita, A. Endoh, I. Watanabe, K. Hikosaka, T. Matsui, T. Mimura, and S. Hiyamizu, "547-GHz f_t $In_{0.7}Ga_{0.3}As - In_{0.52}Al0.48As$ HEMTs with reduced source and drain resistance," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 241–243, May 2004.
[12] T. Suemitsu, T. Enoki, N. Sano, M. Tomizawa, and Y. Ishii, "An analysis of the kink phenomena in InGaAs/InAlAs HEMT's using two-dimensional device simulation," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2390–2399, Dec. 1998.
[13] D. A. J. Moran, E. Boyd, F. McEwan, H. McLelland, C. R. Stanley, and I. G. Thayne, "Sub 100 nm T-gate uniformity in InP HEMT technology," in *Proc. GaAs Mantech Conf.*, Miami, FL, pp. 39–42.
[14] K. Nabors and J. White, "Fastcap: A multipole accelerated 3-D capacitance extraction program," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 10, no. 11, pp. 1447–1459, Nov. 1991.

David A. J. Moran received the B.Sc degree in physics (with honors), before venturing into the field of nanoelectronics, and the Ph.D. degree, after specializing in short gate length III–V HEMT technology, predominantly working with GaAs and InP material systems, from the University of Glasgow, Glasgow, U.K., in 2000 and 2004, respectively. He is currently working toward the postdoctoral degree at the University of Glasgow, looking into the development of III–V MOSFET technology for digital applications.

His research interests include III–V HEMT device technology for high-frequency applications.

Helen McLelland, photograph and biography not available at the time of publication.



Khaled Elgaid received the B.Sc. degree from the University of Evansville, Evansville, IN, in 1984, the M.Sc. degree from Marshall University, Huntington, WV, in 1986, the M.Sc. degree from the University of Cincinnati, Cincinnati, OH, in 1989, and Ph.D. degree from the Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow, U.K., in 1998.

He is a Lecturer with the Electronic Design Centre, Department of Electronics and Electrical Engineering Department, University of Glasgow, leading a group in the area of millimeter-wave monolithic integrated circuits (MMICs). He has authored or coauthored more than 70 journal and conference papers. He has more than 12 years of experience in the design, fabrication, and on-wafer characterization of MMICs and millimeter-wave active and passive devices for imaging, radar, and communications applications. He has extensive experience in three-dimensional lithography using both e-beam and photolithography tools.

Griogair Whyte received the B.Sc. degree in electronics and electrical engineering (with honors) and the M.Sc. degree in microsystems engineering (with distinction for his report on the effects of PCB surface finish and no-clean flux solder effect on parasitic capacitance) from Heriot-Watt University, Edinburgh, U.K. He is currently working toward the Ph.D. degree at the University of Glasgow, Glasgow, U.K., researching the application of electrically small antennas for use in the Specknet project and carrying out high-frequency three-dimensional electromagnetic modeling for the Ultrafast Systems Group.

Colin R. Stanley received the B.Eng. (hons) degree in electronic engineering from the University of Sheffield, Sheffield, U.K., in 1966 and the Ph.D. degree from the University of Southampton, Southampton, U.K., in 1970.

He has been Professor of Semiconductor Materials since 1992. He is author or coauthor of more than 300 journal publications and conference presentations. His research has covered the molecular beam epitaxial growth and characterization of III–V semiconductors and III–V device applications. His current research interests include the growth and fabrication of intermediate band solar cells based on InAs quantum dots, the growth of III–V structures including photovoltaics on Ge, and high-k dielectrics research for III–V MOSFETs.

Iain Thayne received the B.Sc. (hons) and Ph.D. degrees in Physics and electronics from the University of Glasgow, Glasgow, U.K., in 1986 and 1992, respectively.

He is an Engineering and Physical Sciences Research Council Advanced Research Fellow with the Department of Electronics and Electrical Engineering, University of Glasgow, where he leads the Ultrafast Systems Group. His research interest are in the design, fabrication, and testing of a range of III–V HEMT and MOSFET technologies for millimeter-wave, digital, and ultralow-power applications. He has coauthored around 160 journal and conference papers in the above areas.