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RF performance of strained Si MODFETs and MOSFETs on virtual SiGe substrates: A Monte Carlo study

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We employ a comprehensive RF analysis technique based on transient ensemble Monte Carlo simulations to study and compare the high frequency potential of strained Si channel MODFETs and MOSFETs - correctly accounting for realistic device geometries and parasitics. Both devices show well pronounced overshoot effects. The MOSFET channel is more closely confined by the self aligned source and drain contacts, resulting in a shorter effective channel length and better device performance. The cut-off frequency f_T *is robust in the presence of realistic device contact and gate resistances, unlike the maximum frequency of oscillation* f_{max}*, which is strongly effected by the device parasitics.*

1 INTRODUCTION

In Si layers grown pseudomorphically on SiGe substrates, induced strain breaks the six-fold degeneracy of the Si conduction band Δ valleys. Two valleys shift downwards resulting in a type II heterojunction. Electrons in a 2DEG formed at this interface have transverse effective mass in the plane of the heterojunction. These effects combine to give reduced intervalley scattering, higher in-plane mobility and enhanced velocity overshoot in the strained layer. MODFETs with pseudomorphic Si channels have been demonstrated and show clear potential for RF applications [1]. Even greater RF performance has been predicted for strained Si channel MOSFETs, although these conclusions are based on simplified hydrodynamic simulations [2]. Both types of device rely on relaxed SiGe 'virtual substrates' with graded Ge concentration, grown on Si. Compatibility with Si VLSI processing technology makes the devices important candidates for Si MMICs and microwave signal processing applications integrated on conventional Si chips.

We employ, for the first time, a comprehensive RF analysis technique to study and compare the high frequency potential of strained Si channel MODFETs and MOSFETs grown on SiGe 'virtual substrates'. RF analysis requires a realistic simulation geometry and correct handling of device parasitics. Our technique is based on transient ensemble Monte Carlo simulations, using the Monte Carlo module of the Heterojunction 2D Finite Element simulator H2F [3].

2 MONTE CARLO SIMULATION OF THE DEVICES

Figure 1a describes the structure of a 120nm gate length pseudomorphic MODFET. It has a δ-doping layer separated by a 2.5nm spacer from the channel, a T shape recess gate with 50nm recess offset and heavily doped (n-type 10^{18} cm^{-3}) cap layer. An effective δ-doping of 5×10^{12} cm^{-2} and p-type background substrate doping of 10^{14} cm^{-3} is assumed. The structure of this device corresponds to that of a state of the art InGaAs pseudomorphic HEMT fabricated at the Glasgow Nanoelectronics Research Centre and used for validation of the RF analysis technique described below [4]. We note that advances in processing technology will be required to fabricate the described SiGe MODFET. (e.g. the ability to form a well defined As δ-doping supply layer.) The MOSFET structure in figure 1b is designed to have an equivalent effective gate-to-channel separation and channel length.

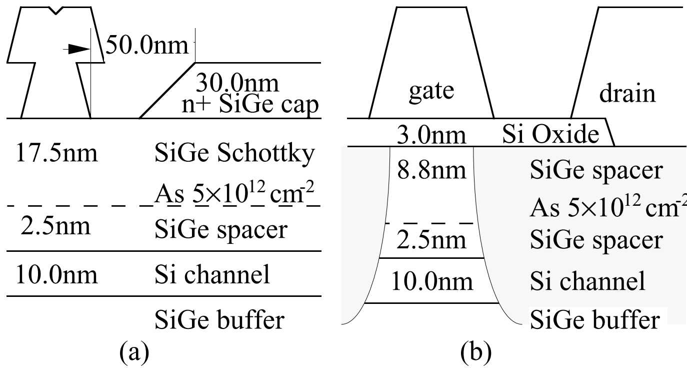

Fig.1a,b Vertical layer structure of 120nm channel length strained Si, Si:SiGe pseudomorphic MODFET (a) and MOSFET (b). Assume negligible Si layer above spacer.

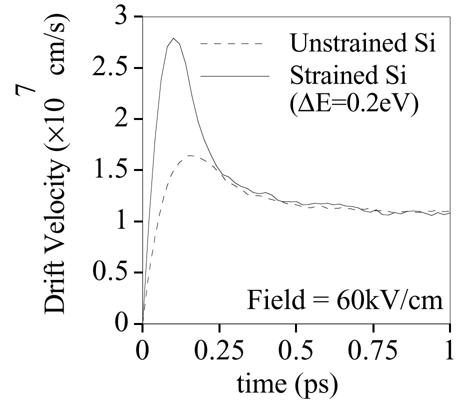

Fig.2 Drift velocity in bulk Si on application of field in (100) direction at t=0, to initially thermal electron distribution.

Inclusion of strained Si material parameters into the Monte Carlo model follows Yamada [5]. Conduction band Δ valleys split by $\Delta E_C = 0.67x$ (eV) and there is a modified band gap of $E_g = 1.11 - 0.74x$ (eV) where x is the fractional Ge content of the relaxed SiGe substrate. For simplicity of modelling, a uniform SiGe substrate is assumed, instead of a 'virtual substrate' with graded Ge concentration. Parameters for $Si_{1-x}Ge_x$ are obtained from [6]. We implement the six phonon scattering model of Jacoboni [7], including acoustic and ionised impurity scattering modes. Modelled bulk velocity-field characteristics are in agreement with experimental unstrained Si data and previous results for strained Si [5]. Calculations of velocity overshoot in strained and unstrained Si are shown in figure 2.

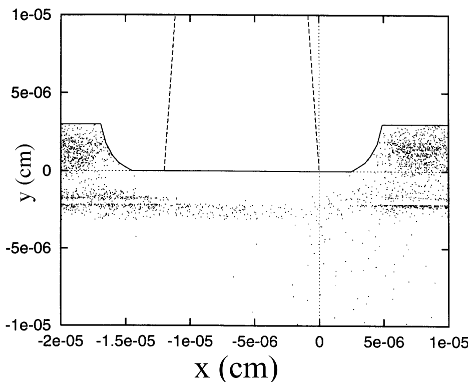

Fig.4 Distribution of superparticles within Monte Carlo model of a pseudomorphic MODFET at V_D=1.5V, V_G=−0.25V, showing deconfinement at drain end of gate.

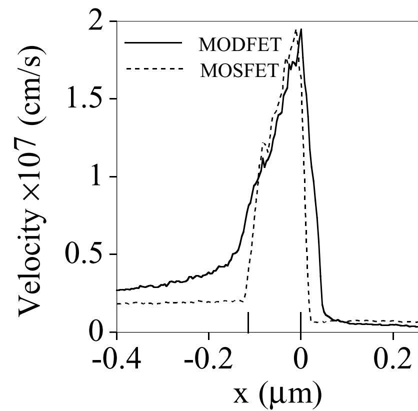

Fig.3 Velocity profile in the channel of pseudomorphic MODFET and MOSFET at V_D=1.5V, V_G=−0.25V, below onset of significant parallel conductance

The distribution of superparticles within the device is shown in figure 3. Due to the modest band offset of the pseudomorphic Si channel, real space transfer and parallel

conductance significantly affect the device performance. The gate biasing conditions chosen for figure 3 are below the onset of parallel conduction in the δ-doping region. However deconfinement of high energy carriers at the drain end of the device is still obvious.

3 R.F. ANALYSIS

The transient Monte Carlo simulations begin by following 5×10^4 superparticles for 2ps settling time at d.c. bias, then a further 2.0→2.6ps during which device statistics are recorded at 1fs intervals. A step change $\Delta V_G = 0.2V$, or $\Delta V_D = 0.3V$ is then consecutively applied, and the transient response measured for a further 2ps. According to the Ramo-Shockley theorem [8] the instantaneous transient current at each device electrode i due to a step perturbation of a terminal voltage ΔV_j on electrode j, can be separated into two parts. Firstly a term describing the current due to the step voltage perturbation on electrode j, and calculated from the capacitance matrix coefficients C_{ij} associated with the device electrodes. Secondly, a term summing the current contribution due to each of N charged particles within the device. This result allows efficient calculation of terminal transient currents.
It is found that structure and doping dependant THz oscillations in device drain current (possibly due to plasma oscillations in the channel, or in the heavily doped cap layer) may mask the detailed form of the transients, and so multiple traces are averaged to define the response. Complex y-parameters are derived by Fourier transforming the terminal currents, and used to extract the small signal equivalent circuit. The cut-off frequency of the simulated device f_T is extracted by solving $\log\left[G_c(\log f)\right] = 0$ where $G_c = dI_d/dI_g$ is the current gain expressed as a function of y-parameters. In order to extract the maximum frequency of oscillation of the simulated device f_{max}, the y-parameters are transformed into the s-parameters. f_{max} is then extracted by solving $\log\left[MAG(\log f)\right] = 0$ where MAG is the maximum available gain. Finally, the small signal equivalent circuit is augmented by the addition of external gate and contact resistances, and thus the effect of contact and gate resistance on the 'real' device operation estimated.

4 RESULTS

The average velocity profiles in the Si channel of the MODFET and MOSFET at $V_G = -0.25V$ and $V_D = 1.5V$are illustrated in figure 4. Both exhibit a well established spatial overshoot region. In the MOSFET this overshoot region is more closely constrained under the gate, and its magnitude is somewhat improved along the channel. This is due to the self aligned doping of the source and drain contact regions. Device transfer characteristics are presented in figure 5, which also graphs the proportion of current flowing outside the channel of each device. Parallel conduction for typical biasing conditions is equivalent for the two devices. The MOSFET, however, shows a somewhat improved output current and transconductance, as a result of the constrained overshoot region effectively shortening the gate length in comparison with the MODFET.
Complex y-parameters are derived by Fourier transforming the terminal current transients associated with small changes in the gate and drain voltages, from which the small signal equivalent circuit and figures of merit f_T and f_{max} are extracted. Results are given in Table 1. f_T is only modestly effected by the inclusion of realistic device parasitics. However f_{max} is strongly eroded by the inclusion of the contact and gate resistances. The variation of f_{max} as a function of these resistances is shown in figure 6. This underlines the need for parasitics to be included in the realistic modelling of ultrasmall devices. Equivalent simulations for the complimentary MOSFET are in progress and will be presented.

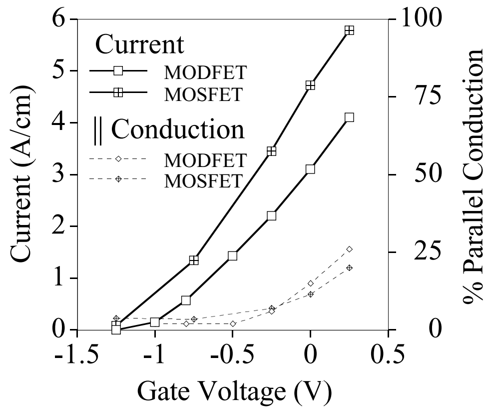

Fig.5 V_G - I_D characteristic (and parallel conduction fraction) for a pseudomorphic MODFET and MOSFET. V_D=1.5V.

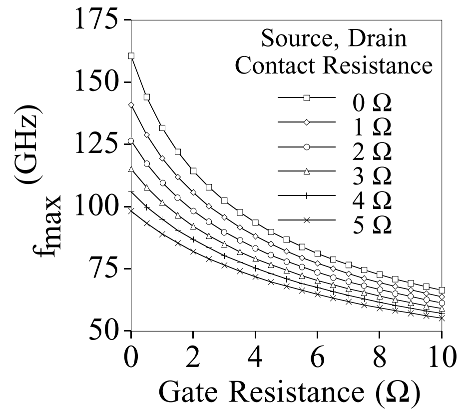

Fig.6 Variation of f_{max} in a pseudomorphic MODFET as a function of gate and contact resistances.

RF figure of merit (GHz)	with negligible contact resistance	gate, source and drain resistance all 5Ω
f_T	77.4	63.9
f_{max}	161	68.0

Table1 calculated RF figures of merit for pseudomorphic MODFET at bias V_D=1.5V, V_G=-0.25V. Device width of 100μm is assumed.

5 CONCLUSIONS

An RF analysis technique based on transient ensemble Monte Carlo simulations has been used to comprehensively study strained Si channel MODFETs and MOSFETs. Both the d.c. characteristics and microwave potential of realistic device structures have been investigated, correctly accounting for device parasitics. It was noted the velocity overshoot region in the channel of the pseudomorphic MOSFET is better constrained over that of the MODFET, due to its self aligned source and drain contacts. This shortens its effective channel length and improves device performance. f_T was shown to be robust in the presence of realistic device contact and gate resistances. However f_{max} is strongly effected by these device parasitics.

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