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Random Dopant Threshold Voltage Fluctuations in 50 nm Epitaxial Channel MOSFETs: A 3D 'Atomistic' Simulation Study

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Abstract

3D 'atomistic' simulations are used to study random dopant related threshold voltage fluctuations in 50 nm MOSFETs. Comparisons are made between conventionally doped transistors and transistors with thin epitaxial silicon layers on heavily doped silicon. Issues related to both the optimum threshold voltage control and the suppression of the threshold voltage dispersion are addressed.

1. Introduction

At the end of the Silicon Roadmap [1] the channel length of integrated MOSFETs will be below 50 nm. Random fluctuations of relatively small numbers of impurities, and their discrete microscopic arrangement in the channel depletion layer of such devices, will cause an average decrease and spread in the threshold voltage, degradation of the subthreshold slope and variations in drive current [2]. Experimental results confirming these predictions are readily available [3]. The device parameter fluctuations may seriously affect the integration, performance and yield of corresponding integrated circuits.

There is, however, theoretical [4] and experimental [5] evidence that the introduction of ultrathin undoped channel layers grown epitaxially on heavily doped silicon substrates can substantially supperss the random dopant induced threshold voltage fluctuations in deep submicron MOSFETs. The use of such undoped epitaxial layers on heavily doped silicon may become mandatory in sub 0.1 micron devices offering also enhancement of the channel mobility and efficient suppression of short channel effects without compromising the optimum threshold voltage control.

The theoretical study of effects associated with the discrete, stochastic distribution of impurity atoms requires 3D simulations with fine grain discretization on a statistical scale and is a computationally demanding task. Very few papers have been published recently in this area [2, 4].

In this paper we use an efficient 'atomistic' 3D simulation approach to study the threshold voltage fluctuations in thin epitaxial channel MOSFETs with 50 nm channel length. The next section gives details of our simulation approach. Section 3 summarises results for uniformly doped devices and highlights the problems associated with control of the threshold voltage and its fluctuations. Result for MOSFETs with various thickness of the epitaxial layer and different doping conditions in the low and heavily doped regions are presented in Section 4.

2. Simulation aspects

We focus our analysis on the threshold voltage fluctuations. The simulations and extraction of the threshold voltage are carried out in the subthreshold region at low drain voltage. They are based on a single solution of Poisson's equation and a modified current continuity equation for each bias point. The threshold voltage is determined using current criteria and efficient search algorithm. The solution domain for a MOSFET with effective channel length L_{eff} = 50 nm and effective channel width W_{eff} = 50 nm is given in Fig 1.

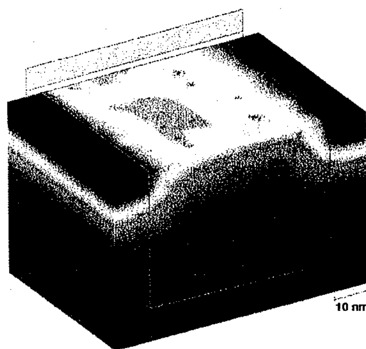

Figure 1. Solution domain and potential distribution in the 'atomistic' simulation of a 50x50 nm MOSFET

In order to resolve the effects associated with random discrete impurities down to an individual impurity level, we use a uniform grid with 1 nm spacing in the region of the device incorporating the random impurities (outlined in Fig. 1). The average number of impurities in the random impurity region is calculated by integrating the doping distribution within it. The actual number of impurities is chosen from a Poisson distribution with the same mean. Impurities with distribution corresponding to the doping distribution are placed randomly in the random impurity region using a rejection technique. They are assigned to the nearest point of the grid. An efficient multigrid solver [7] is used to solve the Poisson and current continuity equations. Approximately three hours are required to accumulate statistics for the threshold voltage of 200 devices with a 50x50x70 nm grid on a PowerMaus 4 processor Parsytec system.

3. Conventional MOSFET

The prevention of short channel effects in MOSFETs with a channel length of 50 nm and below will require doping concentrations in the range 2 - 5x10^{18} cm^{-3}. Fig. 2 illustrates the 'atomistically' calculated dispersion in the threshold voltage in an ensemble of 2000 statistically different devices with L_{eff} = 50 nm W_{eff} = 50nm. The oxide thickness is 3 nm and doping concentration in the channel region N_A = 5x10^{18} cm^{-3}.

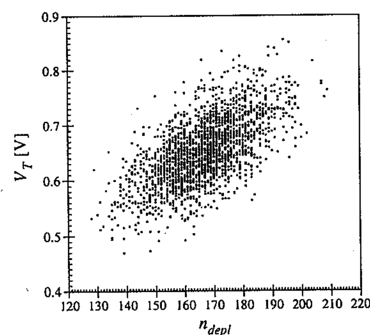

Figure 2. Threshold voltage fluctuations in a 50x50 nm MOSFET with channel doping 5x10^{18} cm^{-3} as a function of the number of impurities in the channel depletion region. Sample of 2000 transistors.

Bearing in mind that the optimum threshold voltage for the 50 nm MOSFET generation is likely to be 0.2 - 0.3 V with

supply voltage of 1.2 V the above picture highlights serious problems. Firstly, the average threshold voltage, even without taking into account the quantum corrections, is too high. Secondly, due to the impurity number and position fluctuations, the threshold is scattered across the whole region between the desirable threshold and supply voltages.

The dependence of the average threshold voltage as a function of the doping concentration is given in Fig. 3. For comparison the threshold voltage calculated from a continuous charge density distribution is presented in the same figure. The dependence the threshold voltage standard deviation σV_T as a function of the doping concentration is also given in the same figure.

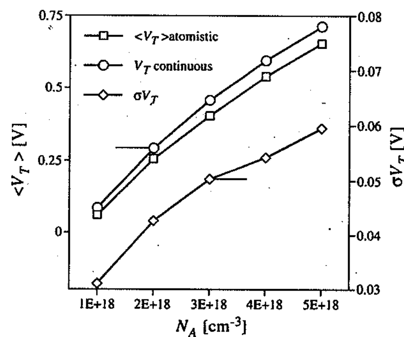

Figure 3. Average threshold voltage in a 50x50 nm MOSFET as a function of the doping concentration. Samples of 200 transistors

The atomistic simulations lead to a reduction in the average threshold voltage ranging from 30 mV at doping concentration $1x10^{18}$ cm^{-3} to 60 mV at doping concentration $5x10^{18}$ cm^{-3}. Although this reduction will compensate part of the threshold voltage increase associated with quantum mechanical effects, doping concentrations above $2x10^{18}$ cm^{-3} will result in unacceptably high values of the threshold voltage.

In agreement with [2] the standard deviation at doping level of $1x10^{18}$ cm^{-3} is approximately 30 mV and increases to 60 mV at doping level $5x10^{18}$ cm^{-3}. Calculations for transistors with an effective width-to-length ratio of 10 give σV_T = 20 mV which is still unacceptably large bearing in mind that $6\sigma V_T$ approaches 1/2 of the optimum threshold.

4. Epitaxial channel MOSFET

The introduction of an undoped epitaxial layer give new degree of freedom in controlling both the threshold voltage and its fluctuations. However the thickness of this layer is restricted to approx. 1/5th of the effective channel length due to short channel effects. Fig. 5 illustrates the dependence of the threshold voltage and its standard deviation in a 50x50 nm MOSFET as a function the thickness of the epitaxial layer for two doping concentrations of the heavily doped underlying silicon ($3x10^{18}$ cm^{-3} and $5x10^{18}$ cm^{-3} respectively).

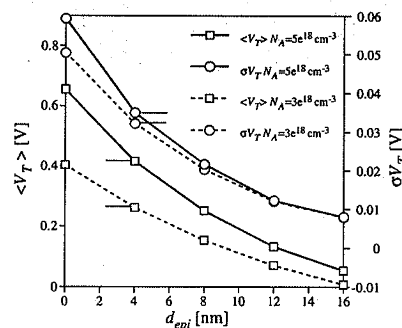

Figure 4. Average threshold voltage and its standard deviation in a 50x50 nm MOSFET as a function of the thickness of the undoped epitaxial layer. Samples of 200 transistors

With an increase in the epitaxial layer width the differences between the two doping concentrations diminishes. To

achieve the optimum average threshold voltage of 0.2 - 0.3 V the epitaxial layer thickness needs to be between 8 and 10 nm. The corresponding threshold voltage standard deviation is approx. 20 mV.

Currently the background doping in the epitaxial silicon layer could be kept below $1x10^{16}$ cm^{-3}. One legitimate question is at what level the doping concentration in the epitaxial layer starts to adversely effect the threshold voltage dispersion. Figure 5 illustrates the dependence of the threshold voltage and its standard deviation in a 50x50 nm MOSFET on the doping concentration in a 12 nm epitaxial layer for $5x10^{18}$ cm^{-3} doping in the underlying silicon.

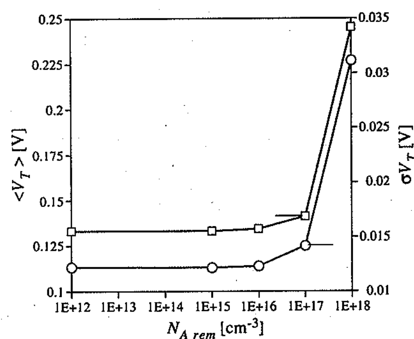

Figure 5. Average threshold voltage and its standard deviation in a 50x50 nm MOSFET as a function of the doping concentration in a 12 nm epitaxial layer. Samples of 200 transistors.

Doping concentrations in the epitaxial layer up to $1x10^{16}$ cm^{-3} effect minimally both the threshold voltage and its standard deviation. Both the threshold voltage and its standard deviation rapidly increase for doping concentrations above $1x10^{17}$ cm^{-3}. However by comparing Fig. 2 and Fig. 5 it becomes clear that the increase of the doping in the epitaxial layer does not offer any advantage in terms of controling the threshold voltage and its dispersion.

5. Conclusions

In conclusion we have demonstrated that the introduction of a thin epitaxial layer in the channel of a 50 nm MOSFET can significantly suppress the random dopant induced threshold fluctuations, and offers additional degree of freedom in the optimum threshold voltage control. The design margins, however, are becoming very tight and new means of controlling of the threshold and its fluctuations may be required when crossing the 50 nm MOSFETs barrier.

6. References

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