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RF analysis methodology for Si and SiGe FETs based on transient Monte Carlo Simulation

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Abstract

A comprehensive analysis methodology allowing investigation of the RF performance of Si and strained Si:SiGe MOSFETs is presented. It is based on transient ensemble Monte Carlo simulation which correctly describes device transport, and employs a finite element solver to account for complex device geometries. Transfer characteristics and figures of merit for a number of existing and proposed RF MOSFETs are discussed.

1. Introduction

The rapidly expanding wireless communications industry has highlighted the need to integrate microwave signal processing functions onto conventional Si chips, reducing system component count and complexity [1]. To fulfil this need there is an urgent requirement for accurate analysis of Si and strained Si (on SiGe virtual substrates) MOSFET performance for RF device design, accounting for both non-equilibrium channel carrier transport in deep submicron devices and realistic device parasitics.
RF analysis requires a realistic simulation geometry and correct handling of device parasitics. We have developed a comprehensive RF analysis methodology based on transient ensemble Monte Carlo simulation to study and compare the high frequency performance of Si and strained Si:SiGe MOSFETs. In addition to detailed Monte Carlo analysis of charge transport, the finite element simulator H2F [2] uses quadrilateral elements to accurately describe complex device geometries (including gate and contact geometries). Originally developed to analyse III-V devices it has been extensively modified to handle both Si and strained Si on relaxed SiGe buffers.

2. RF Analysis Methodology

We perform time domain Monte Carlo RF analysis to model RF performance. Step changes are applied to first the gate, and then the drain contacts of a device under simulation after allowing for 2.0 ps settling time and 6.0 ps to determine device steady state. Gate and drain transient currents are recorded. The Ramo-Shockley formalism is implemented to reduce statistical noise in these transient terminal currents [3].
As laid out in fig. 1, Fourier transforming the transient terminal currents provides the complex y-parameters, from which we may obtain the cut-off frequency f_T and, after a further transformation to s-parameters, the maximum frequency of oscillation, f_{max}. However, the 2D domain of Monte Carlo simulation is chosen to minimise computational effort in order to improve the speed of analysis. The access resistances (R_{sI} and R_{dI} in fig. 1) are included, whilst the gate and contact impedances (R_g, L_g, R_c, L_d and L_s in fig. 1) are not. The small signal equivalent circuit for the active portion of the device must be obtained by a further transformation to z-parameters, allowing simple removal of access resistances, and then retransformation back to y-parameters

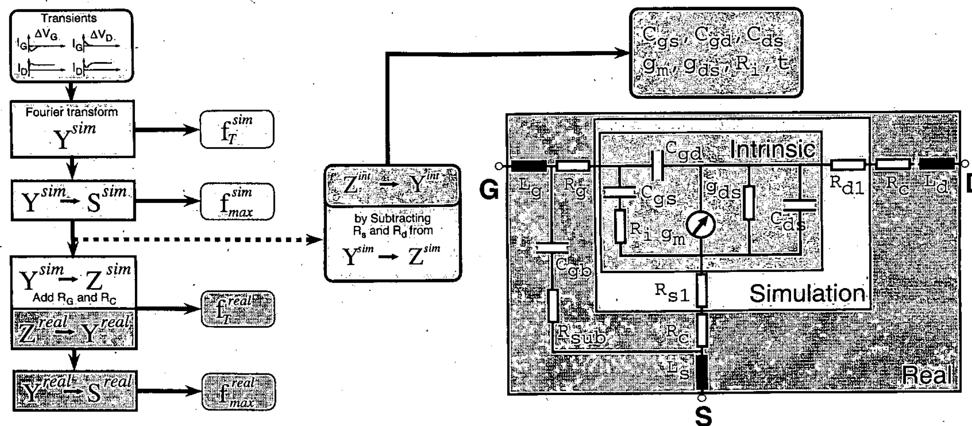

Fig. 1 RF analysis of Monte Carlo transient response and extraction of both Figures of Merit and Small Signal Equivalent Circuit Parameters.

before analytical small signal equivalent circuit extraction. To obtain figures of merit for a 'real' device the z-parameters are augmented with the contact impedances. From these augmented Z^{real} an equivalent set of retransformations gives Y^{real} and thence S^{real} from which the figures of merit f_T^{real} and $f_{\max}^{real}$ can be extracted.

Note the inclusion of the gate-bulk capacitance and substrate resistance C_{gb}, R_{sub} in the equivalent circuit. While C_{gb} for the active gate region is negligible due to the shielding effect of the inversion layer under normal device operation, the gate-bulk capacitance of the gate contacts becomes significant for typical multi-fingered RF CMOS style structures [4]. Inclusion of C_{gb}, R_{sub} makes the small signal equivalent circuit of fig. 1 more appropriate to the devices described in fig. 2(c,d).

3. Devices Structures Analysed

Fig. 2(a) describes a strained Si:SiGe T-gate MOSFET presently under construction at the University of Glasgow. To avoid the onset of parallel conduction at the oxide interface the spacer and supply layers should be as thin as possible. However practical limitations are set both by the need to avoid supply layer dopants diffusing into the channel, and by present oxide growth technology. 1D Poisson-Schrödinger simulation suggests that the operating regime of this device will be constrained by parallel conduction.

Fig. 2(b) describes a 0.12 μm gate length (0.1 μm effective channel length) Si:SiGe MOSFET incorporating best practice design techniques from the III-V RF device

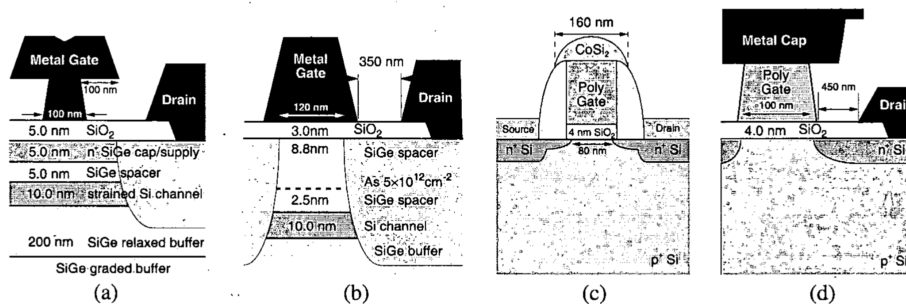

Fig. 2 Device structures of the various Si and SiGe RF MOSFETs studied in this work: (a) realistic SiGe MOSFET, (b) SiGe modulation doped MOSFET, (c) state-of-the-art Si MOSFET, (d) RF enhanced Si MOSFET.

community. Although technologically challenging, analysis of this FET is expected to show the performance potential of Si:SiGe.

Fig. 2(c) shows an aggressively scaled state-of-the-art silicon device, a Co salicided T-gate style RF device with measured f_T = 65 GHz, f_{max} = 70 GHz developed by Toshiba [5]. Fig.2(d) is a Si MOSFET presently under investigation at the University of Glasgow to investigate RF enhancements to present Si processing technology.

4. Results and Discussion

The Monte Carlo nature of the analysis methodology accounts for non-equilibrium transport effects in the active regions of short channel devices. Fig. 3 shows the higher drift velocity and improved effective channel length in the 100 nm strained Si channel of device (b) compared with that of device (a). Note that the high drift velocity exhibited by device (d) is partially because of its shorter effective channel length, but also due to exclusion of surface roughness (interface) scattering from the Si model.

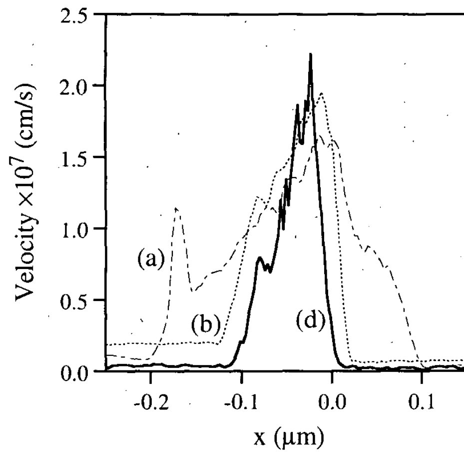

Fig. 3 Electron drift velocities in the channels of devices (a,b,d). V_D = 1.5V with V_G chosen for maximum transconductance. In each case the RH edge of the gate metal is at x = 0.

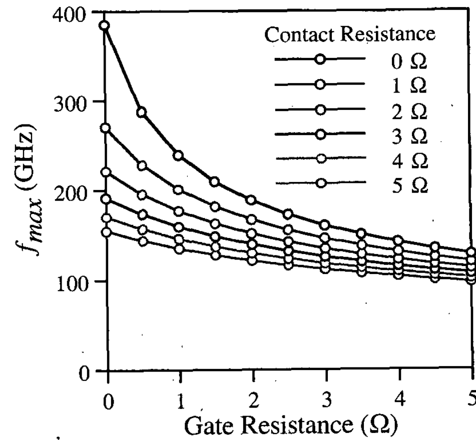

Fig. 4 Simulated variation in the f_{max} of device (c) as a function of gate and source / drain contact resistances.

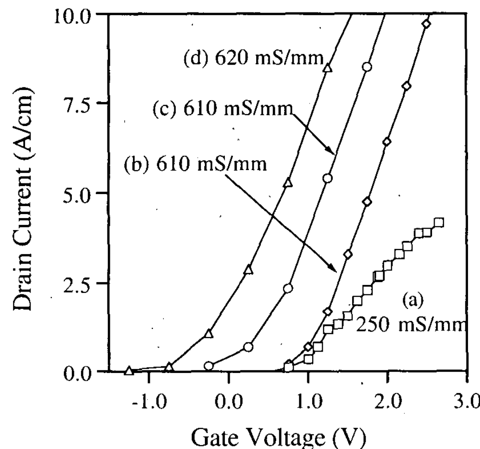

Fig. 5 Transfer characteristics of devices (a,b,c,d). Monte Carlo simulation for 6.0 ps after 2.0 ps settling time. V_D = 1.5V. Device width of 100μm assumed. Traces (d,c) have been successively offset by -1.0V for clarity.

Figures of Merit	(a)	(b)	(c)	(d)
	gate, source and drain resistance 5Ω			
f_T (GHz)	43/34	71	80	85
f_{max} (GHz)	77/49	66	100	63

Table 1 RF figures of merit for devices (a,b,c,d) biased about maximum transconductance and obtained from a simulated 5.0 ps transient response to ΔV_D = 0.3V, ΔV_G = 0.2V. Device (a) outwith/within parallel conduction regime.

Fig. 4 shows the variation of f_{max} in device (c) over a range of low resistance gate and source/drain contacts. The interaction of even nominal resistances with device parasitic capacitances have a marked effect on its figures of merit, emphasising the need to correctly include both transport and parasitics in an RF analysis methodology.
Fig. 5 and Table 1 present the transfer characteristics (including maximum transconductance) and figures of merit obtained from RF analysis of devices (a) to (d). Single fingered structures with negligible C_{gb} and contact resistances of 5Ω are assumed. The expected limitations of device structure (a) are obvious. A parasitic conduction layer at the oxide interface forms only 0.5V above threshold, dropping the maximum g_m to 250mS/mm. Even before the formation of this layer the T-gate structure fails to control the effective channel length of the device, resulting in a reduced channel velocity and lower f_T.
Devices (b), (c) and (d) all exhibit similar transconductances, and thus broadly similar f_T values, accepting that simulation of pure Si devices overestimates f_T due to the omission of interface scattering from the Monte Carlo model. In addition f_T of the physically measured devices is lower due to their increased gate resistance (> 30 Ω). It is clear from fig. 4 that f_{max} values are critically dependant on device parasitics, and this is emphasised by device (c) where a radically different contact geometry leads to increased f_{max}.

In conclusion, we have presented an RF analysis methodology for Si and SiGe MOSFETs based on Monte Carlo simulation and accounting for both non-equilibrium carrier transport and realistic device parasitics. The methodology has been successfully applied to a range of existing and proposed device designs.

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